winbond

CONSUMER PRODUCT DESCRIPTION

Winbond
Mobile Keyboard and
Embedded Controller

W83L951ADG

Date: November 21, 2007 Reversion: 0.7

DATA SHEET REVISION HISTORY

NO	DATE	VERSION	MAIN CONTENTS
1	2007/March	0.5	First Release
2	2007/May	0.6	
3	2007/June	0.7	1. Grammar check

Table of Contents-

1. GENERAL DESCRIPTION

The W83L951ADG architecture consists of the Winbond mobile keyboard controller and embedded controller, including a Turbo-8051 core logic controller. The W83L951ADG integrates various components: 2K+256 bytes of RAM, 2K initial boot ROM, 64K on-chip FLASH, LPC host interface, 13 general purpose I/O ports with 24 external interrupt source, 4 timers, 1 serial port, 2 SMBus interfaces for master and slave modes, 2 PS2 ports, 4 16-bits PWM channels, 2 D-A and 8 A-D converters, 1 Consumer Infrared Communications Receiver, 2 Fan Tachometer , 1 Real Time Clock Generator, 1 Simple peripheral Interface and Matrix Interface.

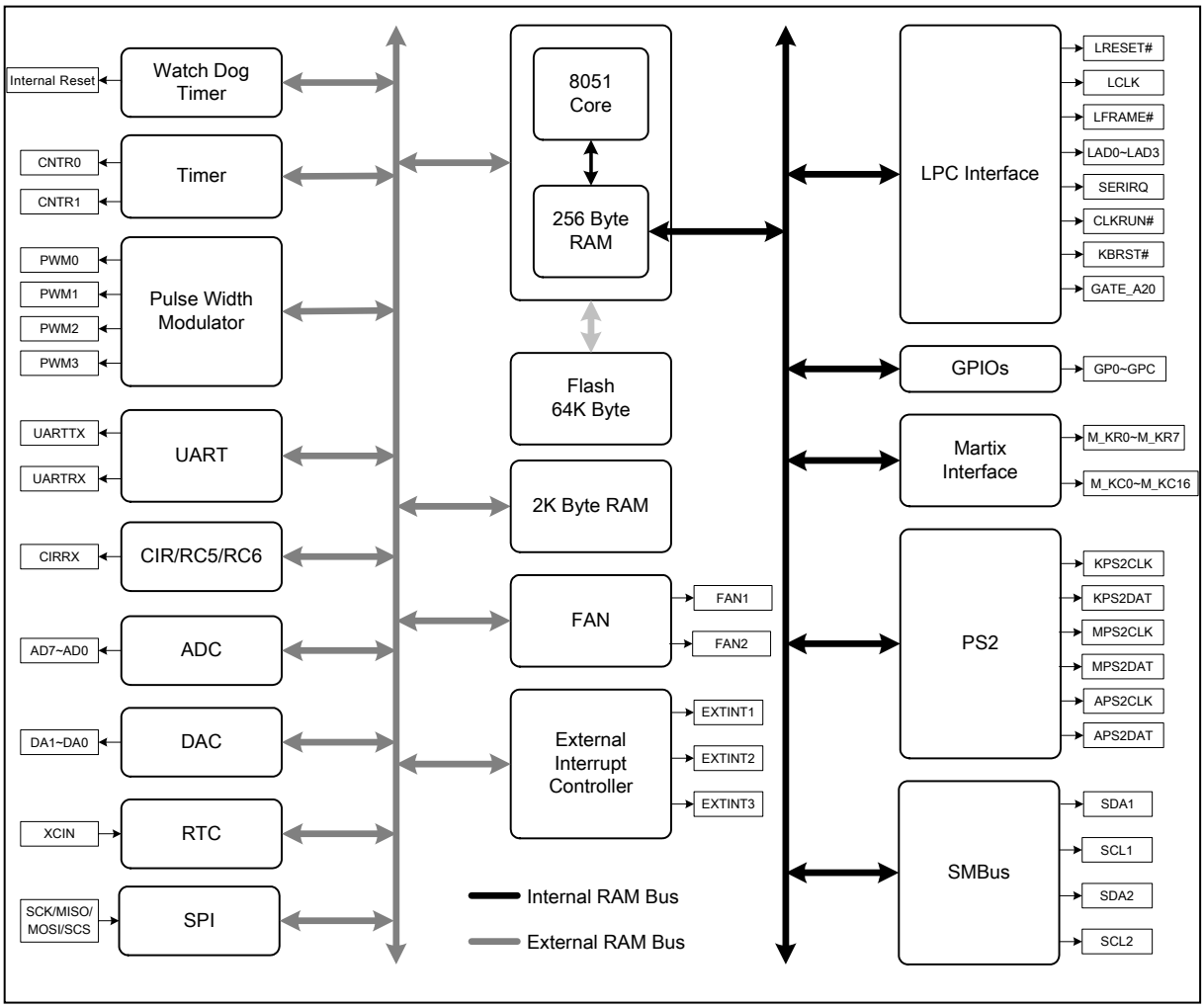


Figure 1-1.W83L951ADG Function Block Diagram

Note: This Block Diagram should not used for pin count.

2. PIN CONFIGURATION

2.1 128-Pin Low Profile Quad Flat Pack (LQFP)

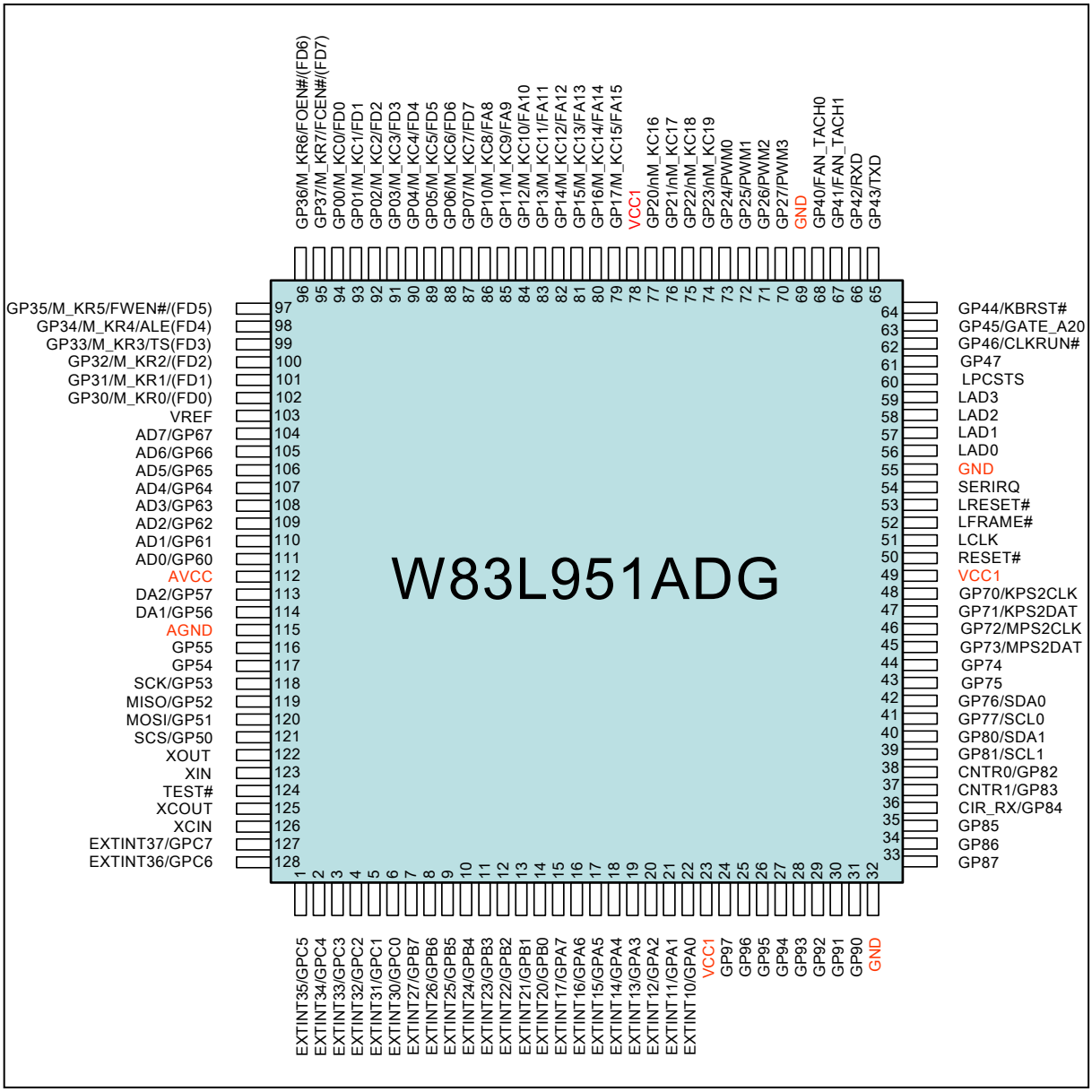


Figure 2-1.Pin Configuration Block Diagram of W83L951ADG

Note: The Pin Configuration is only for 128-pin LQFP Package.

2.2 Pin Type

Table 2-1 Pin Type Description

TYPE	DESCRIPTION
I/O_{12tsm}	Bi-directional pin, TTL level, Schmitt-trigger input, selectable 250uA/12mA sink capability, 12mA select source capability
I/O_{12tsai}	Bi-directional pin, TTL level, Schmitt-trigger input, Analog Input, 12mA source-sink capability
I/O_{12tsao}	Bi-directional pin, TTL level, Schmitt-trigger input, Analog Output, 12mA source-sink capability
I/O_{16tsh}	Bi-directional pin, TTL level, Schmitt-trigger input, 5V Tolerant, 16mA source-sink capability
I/O_{24ts}	Bi-directional pin, Schmitt-trigger input, 24mA source-sink capability
I_{ts}	TTL level, Schmitt-trigger input
$I_{c,}$ O_c	Clock Input, Clock Out
I_{vdd}	Voltage Input
I_{vss}	Ground Input

Note: t – TTL level, s – Schmitt-trigger, m – matrix keyboard, ai – analog input, ao – analog output, h – 5V Tolerant, c – clock.

2.3 Pin configuration table

Table 2-2 Pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GPC5 EXTINT35	1	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC4 EXTINT34	2	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC3 EXTINT33	3	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC2 EXTINT32	4	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC1 EXTINT31	5	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC0 EXTINT30	6	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB7 EXTINT27	7	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB6 EXTINT26	8	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

Pin configuration table, continued

SYMBOL	PIN	I/O	FUNCTION
GPB5 EXTINT25	9	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB4 EXTINT24	10	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB3 EXTINT23	11	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB2 EXTINT22	12	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB1 EXTINT21	13	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB0 EXTINT20	14	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA7 EXTINT17	15	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA6 EXTINT16	16	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA5 EXTINT15	17	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA4 EXTINT14	18	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA3 EXTINT13	19	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA2 EXTINT12	20	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA1 EXTINT11	21	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA0 EXTINT10	22	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
VCC1	23	Ivdd	Normal Power Input, +3.3V
GP97	24	I/O_{16tsh}	General Purpose I/O Function
GP96	25	I/O_{16tsh}	General Purpose I/O Function
GP95	26	I/O_{16tsh}	General Purpose I/O Function
GP94	27	I/O_{16tsh}	General Purpose I/O Function
GP93	28	I/O_{16tsh}	General Purpose I/O Function

Pin configuration table, continued

SYMBOL	PIN	I/O	FUNCTION
GP92	29	I/O_{16tsh}	General Purpose I/O Function
GP91	30	I/O_{16tsh}	General Purpose I/O Function
GP90	31	I/O_{16tsh}	General Purpose I/O Function
GND	32	Ivss	Normal GND
GP87	33	I/O_{16tsh}	General Purpose I/O Function
GP86	34	I/O_{16tsh}	General Purpose I/O Function
GP85	35	I/O_{16tsh}	General Purpose I/O Function
GP84 CIR_RX	36	I/O_{16tsh}	General Purpose I/O Function Consumer Infrared Communication Receiver Function
GP83 CNTR1	37	I/O_{16tsh}	General Purpose I/O Function Timer Y Signal
GP82 CNTR0	38	I/O_{16tsh}	General Purpose I/O Function Timer X Signal
GP81 SCL1	39	I/O_{16tsh}	General Purpose I/O Function SMBus 1 Clock Signal
GP80 SDA1	40	I/O_{16tsh}	General Purpose I/O Function SMBus 1 Data Signal
GP77 SCL0	41	I/O_{16tsh}	General Purpose I/O Function SMBus 0 Clock Signal
GP76 SDA0	42	I/O_{16tsh}	General Purpose I/O Function SMBus 0 Data Signal
GP75	43	I/O_{16tsh}	General Purpose I/O Function
GP74	44	I/O_{16tsh}	General Purpose I/O Function
GP73 MPS2_DAT	45	I/O_{16tsh}	General Purpose I/O Function Mouse PS2 Data Signal
GP72 MPS2_CLK	46	I/O_{16tsh}	General Purpose I/O Function Mouse PS2 Clock Signal
GP71 KPS2_DAT	47	I/O_{16tsh}	General Purpose I/O Function Keyboard PS2 Data Signal
GP70 KPS2_CLK	48	I/O_{16tsh}	General Purpose I/O Function Keyboard PS2 Clock Signal
VCC1	49	Ivdd	Normal Power Input, +3.3V

Pin configuration table, continued

SYMBOL	PIN	I/O	FUNCTION
RESET#	50	I_{ts}	System Reset.
LCLK	51	I_{ts}	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	I_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	I_{ts}	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O_{24ts}	Serial IRQ input/Output.
GND	55	Ivss	Normal GND
LAD0	56	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LPCSTS	60	I_{ts}	Power status. Indicates current power status of LPC interface.
GP47	61	I/O_{16tsh}	General Purpose I/O Function
GP46 CLKRUN#	62	I/O_{16tsh}	General Purpose I/O Function Advance LPC function: It is used to request starting the clock
GP45 GATE_A20	63	I/O_{16tsh}	General Purpose I/O Function Gate A20 output
GP44 KBRST#	64	I/O_{16tsh}	General Purpose I/O Function CPU reset output
GP43 TXD	65	I/O_{16tsh}	General Purpose I/O Function UART TX output
GP42 RXD	66	I/O_{16tsh}	General Purpose I/O Function UART RX Input
GP41 FAN_TACH1	67	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 1
GP40 FAN_TACH0	68	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 0
GND	69	Ivss	Normal GND
GP27 PWM3	70	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP26 PWM2	71	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP25 PWM1	72	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output

Pin configuration table, continued

SYMBOL	PIN	I/O	FUNCTION
GP24 PWM0	73	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP23 KC19	74	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP22 KC18	75	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP21 KC17	76	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP20 KC16	77	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
VCC1	78	Ivdd	Normal Power Input, +3.3V
GP17 KC15 FA15	79	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP16 KC14 FA14	80	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP15 KC13 FA13	81	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP14 KC12 FA12	82	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP13 KC11 FA11	83	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP12 KC10 FA10	84	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP11 KC9 FA9	85	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP10 KC8 FA8	86	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address

Pin configuration table, continued

SYMBOL	PIN	I/O	FUNCTION
GP07 KC7 FA7/FD7	87	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP06 KC6 FA6/FD6	88	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP05 KC5 FA5/FD5	89	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP04 KC4 FA4/FD4	90	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP03 KC3 FA3/FD3	91	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP02 KC2 FA2/FD2	92	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP01 KC1 FA1/FD1	93	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP00 KC0 FA0/FD0	94	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP37 KR7 CE#	95	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash chip select enable
GP36 KR6 OE#	96	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash output enable
GP35 KR5 WE#	97	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash write enable
GP34 KR4 ALE	98	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Address latch enable

Pin configuration table, continued

SYMBOL	PIN	I/O	FUNCTION
GP33 KR3	99	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP32 KR2	100	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP31 KR1	101	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP30 KR0	102	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
VREF	103	Ivdd	Analog Reference Voltage Input
GP67 AD7	104	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP66 AD6	105	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP65 AD5	106	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP64 AD4	107	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP63 AD3	108	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP62 AD2	109	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP61 AD1	110	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP60 AD0	111	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
AVCC	112	Ivdd	Analog Power Input, +3.3V
GP57 DA2	113	I/O_{12tsai}	General Purpose I/O Function DA Converter Output
GP56 DA1	114	I/O_{12tsai}	General Purpose I/O Function DA Converter Output
AGND	115	Ivss	Analog GND
GP55	116	I/O_{16tsh}	General Purpose I/O Function
GP54	117	I/O_{16tsh}	General Purpose I/O Function
GP53	118	I/O_{16tsh}	General Purpose I/O Function

Pin configuration table, continued

SYMBOL	PIN	I/O	FUNCTION
GP52	119	I/O_{16tsh}	General Purpose I/O Function
GP51	120	I/O_{16tsh}	General Purpose I/O Function
GP50	121	I/O_{16tsh}	General Purpose I/O Function
XOUT	122	O_c	System Clock Output
XIN	123	I_c	System Clock Input
TEST#	124	I_{ts}	Test pin to provide different operation.
XCOUT	125	O_c	32.768 KHz Clock Output for RTC function
XCIN	126	I_c	32.768 KHz Clock Input for RTC function
GPC7 EXTINT37	127	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC6 EXTINT36	128	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

2.4 RESET# & TEST# Part

SYMBOL	PIN	I/O	FUNCTION
RESET#	50	I_{ts}	System Reset.
TEST#	124	I_{ts}	Test pin to provide different operation.

In the W83L951ADG, RESET# Pin and TEST# Pin decide the status of the W83L951ADG to provide 4 operations.

TEST#	RESET#	CHIP CURRENT STATUS
0	0	Internal Flash Access Interface Enable
0	1	Reserved
1	0	Normal Reset
1	1	Normal Operation

2.5 LPC Interface Part

LPC Interface is formed by LAD0~LAD3, SERIRQ, LRESET#, LFRAME#, LCLK and LPCSTS. These pins, except LPCSTS, are defined by LPC interface Spec. Below are the descriptions about all LPC pins:

SYMBOL	PIN	I/O	FUNCTION
LCLK	51	I_{ts}	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	I_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	I_{ts}	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O_{24ts}	Serial IRQ input/Output.
LAD0	56	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.

Note: For other pins about LPC interface, CLKRUN#, please see “GP4” part. For LPCSTS, please see “power & clock” part.

2.6 GPIO0 Part

This part contains:

General Purpose I/O Function

General Purpose I/O is the default function. Change the value of GPIO0 and GPIOD0 register to determine 8 input/output.

Keyboard Matrix Column Output

Use Chipctrl2 register bit 3 to enable {GP0, GP1, GP20~23} keyboard scan and GP3 key wakeup interrupt function.

Internal Flash Access Interface

When TEST# and RESET# are both low, Internal Flash Access Interface is enabled and other functions are disabled.

SYMBOL	PIN	I/O	FUNCTION
GP07 KC7 FA7/FD7	87	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP06 KC6 FA6/FD6	88	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP05 KC5 FA5/FD5	89	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP04 KC4 FA4/FD4	90	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP03 KC3 FA3/FD3	91	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP02 KC2 FA2/FD2	92	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP01 KC1 FA1/FD1	93	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP00 KC0 FA0/FD0	94	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data

2.7 GPIO1 Part

This part contains:

General Purpose I/O Function

General Purpose I/O is the default function. Change the value of GPIO1 and GPIOD1 register to determine 8 input/output.

Keyboard Matrix Column Output

Use Chipctrl2 register bit 3 to enable {GP0, GP1, GP20~23} keyboard scan and GP3 key wakeup interrupt function.

Internal Flash Access Interface

When TEST# and RESET# are both low, Internal Flash Access Interface is enabled and the other functions are disabled.

SYMBOL	PIN	I/O	FUNCTION
GP17 KC15 FA15	79	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP16 KC14 FA14	80	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP15 KC13 FA13	81	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP14 KC12 FA12	82	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP13 KC11 FA11	83	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP12 KC10 FA10	84	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP11 KC9 FA9	85	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP10 KC8 FA8	86	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address

2.8 GPIO2 Part

This part contains:

General Purpose I/O Function

General Purpose I/O is the default function. Change the value of GPIO2 and GPIOD2 register to determine 8 input/output.

Pulse Width Modulator Output

Use Pulse Width Modulator Registers to control 4 Pulse Width Modulator Output.

Keyboard Matrix Column Output

Change the value of chip control 2 register bit 3 (Keyboard Scan Function Enable) to enable {GP0, GP1, GP20~23} keyboard scan function and GP3 key wakeup interrupt function.

SYMBOL	PIN	I/O	FUNCTION
GP27 PWM3	70	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP26 PWM2	71	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP25 PWM1	72	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP24 PWM0	73	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP23 KC19	74	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP22 KC18	75	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP21 KC17	76	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP20 KC16	77	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output

2.9 GPIO3 Part

This part contains General Purpose I/O function, external flash interface, and keyboard matrix row input. General Purpose I/O is the default function.

General Purpose I/O Function

Change the values of GPIO 3 data register (GPIO3) and GPIO 3 direction register (GPIOD3) to determine 8 input/output.

Keyboard Matrix Row Input

Change the value of chip control 2 register bit 3 (Keyboard Scan Function Enable) to enable GP3 key wakeup interrupt function.

Note:

GPIO3 must be set as input when this function is enabled

The sample frequency about KEY Interrupt Mode is a system cycle, trigger for ' Low ' of input of GP3 and only take a sample once (unless the input of GP3 returns 'High', and then enters 'low'). If the signal debounces, then the interrupt may request again.

Internal Flash Access Interface

GPIO30~33: Reserved (Must assign low)

SYMBOL	PIN	I/O	FUNCTION
GP37 KR7 CE#	95	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash chip select enable
GP36 KR6 OE#	96	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash output enable
GP35 KR5 WE#	97	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash write enable
GP34 KR4 ALE	98	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Address latch enable
GP33 KR3	99	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP32 KR2	100	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP31 KR1	101	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP30 KR0	102	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input

2.10 GPIO4 Part

General Purpose I/O Function

Change the values of GPIO 4 data register (GPIO4) and GPIO 4 direction register (GPIOD4) to determine 8 input/output.

Universal Asynchronous Serial I/O Function

Change the value of chip control 1 register bit 3 (UART Function Enable) to enable Universal Asynchronous Serial I/O Function.

Hardware Keyboard Reset Function

Change the values of keyboard control register bit4 (Port 92 Enable) and bit3 (Hardware Keyboard Reset Control Enable) to enable Hardware Keyboard Reset Function.

Hardware Gate A20 Function

Change the values of keyboard control register bit4 (Port 92 Enable) and bit2 (Hardware Gate A20 Control Enable) to enable Hardware Gate A20 Function.

SYMBOL	PIN	I/O	FUNCTION
GP47	61	I/O_{16tsh}	General Purpose I/O Function
GP46 CLKRUN#	62	I/O_{16tsh}	General Purpose I/O Function Advance LPC function: It is used to request starting the clock
GP45 GATE_A20	63	I/O_{16tsh}	General Purpose I/O Function Gate A20 output
GP44 KBRST#	64	I/O_{16tsh}	General Purpose I/O Function CPU reset output
GP43 TXD	65	I/O_{16tsh}	General Purpose I/O Function UART TX output
GP42 RXD	66	I/O_{16tsh}	General Purpose I/O Function UART RX Input
GP41 FAN_TACH1	67	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 1
GP40 FAN_TACH0	68	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 0

2.11 GPIO5 Part

General Purpose I/O Function

Change the values of GPIO 5 data register (GPIO5) and GPIO 5 direction register (GPIOD3) to determine 8 input/output.

D/A Converter Function

Change the value of chip control 2 register bit 7 (D/A 2 Function Enable) and Bit 6 (D/A 1 Function Enable) to enable D/A Converter Function.

SYMBOL	PIN	I/O	FUNCTION
GP57 DA2	113	I/O_{12tsai}	General Purpose I/O Function DA2 Converter Output
GP56 DA1	114	I/O_{12tsai}	General Purpose I/O Function DA1 Converter Output
GP55	116	I/O_{16tsh}	General Purpose I/O Function
GP54	117	I/O_{16tsh}	General Purpose I/O Function
GP53	118	I/O_{16tsh}	General Purpose I/O Function
GP52	119	I/O_{16tsh}	General Purpose I/O Function
GP51	120	I/O_{16tsh}	General Purpose I/O Function
GP50	121	I/O_{16tsh}	General Purpose I/O Function

2.12 GPIO6 Part

General Purpose I/O Function

Change the values of GPIO 6 data register (GPIO6) and GPIO 6 direction register (GPIOD6) to determine 8 input/output.

A/D Converter Function

Change the value of chip control 2 register bit 5 (A/D Function Enable) to enable A/D Converter Function.

SYMBOL	PIN	I/O	FUNCTION
GP67 AD7	104	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP66 AD6	105	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP65 AD5	106	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP64 AD4	107	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal

Continued

SYMBOL	PIN	I/O	FUNCTION
GP63 AD3	108	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP62 AD2	109	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP61 AD1	110	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP60 AD0	111	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal

2.13 GPIO7 Part

General Purpose I/O Function

Change the values of GPIO 7 data register (GPIO7) and GPIO 7 direction register (GPIOD7) to determine 8 input/output.

Keyboard PS2 Function Enable Function

Change the value of chip control 3 register bit 2 (Keyboard PS2 Function Enable) to enable Keyboard PS2 Function Enable Function.

Mouse PS2 Function Enable Function

Change the value of chip control 3 register bit 3 (Mouse PS2 Function Enable) to enable Mouse PS2 Function Enable Function.

SMBUS 0 Function

Change the value of chip control 3 register bit 0 (SMBUS 0 Function Enable) to enable SMBUS 0 Function.

SYMBOL	PIN	I/O	FUNCTION
GP77 SCL0	41	I/O_{16tsh}	General Purpose I/O Function SMBus 0 Clock Signal
GP76 SDA0	42	I/O_{16tsh}	General Purpose I/O Function SMBus 0 Data Signal
GP75	43	I/O_{16tsh}	General Purpose I/O Function
GP74	44	I/O_{16tsh}	General Purpose I/O Function
GP73 MPS2_DAT	45	I/O_{16tsh}	General Purpose I/O Function Mouse PS2 Data Signal
GP72 MPS2_CLK	46	I/O_{16tsh}	General Purpose I/O Function Mouse PS2 Clock Signal
GP71 KPS2_DAT	47	I/O_{16tsh}	General Purpose I/O Function Keyboard PS2 Data Signal
GP70 KPS2_CLK	48	I/O_{16tsh}	General Purpose I/O Function Keyboard PS2 Clock Signal

2.14 GPIO8 Part

General Purpose I/O Function

Change the values of GPIO 8 data register (GPIO8) and GPIO 8 direction register (GPIOD8) to determine 8 input/output.

Consumer Infrared Communications Receiver Function

Change the value of chip control 3 register bit 5 (CIR Function Enable) to enable Consumer Infrared Communications Receiver Function.

Wave Measurement Function

Change the values of timer X/Y mode register bit 5-4 and bit 1-0 to enable Wave Measurement Function.

SMBUS 1 Function

Change the value of chip control 2 register bit 1 (SMBUS 1 Function Enable) to enable SMBUS 1 Function.

SYMBOL	PIN	I/O	FUNCTION
GP87	33	I/O_{16tsh}	General Purpose I/O Function
GP86	34	I/O_{16tsh}	General Purpose I/O Function
GP85	35	I/O_{16tsh}	General Purpose I/O Function
GP84 CIR_RX	36	I/O_{16tsh}	General Purpose I/O Function Consumer Infrared Communication Receiver Function
GP83 CNTR1	37	I/O_{16tsh}	General Purpose I/O Function Timer Y Signal
GP82 CNTR0	38	I/O_{16tsh}	General Purpose I/O Function Timer X Signal
GP81 SCL1	39	I/O_{16tsh}	General Purpose I/O Function SMBus 1 Clock Signal
GP80 SDA1	40	I/O_{16tsh}	General Purpose I/O Function SMBus 1 Data Signal

2.15 GPIO9 Part

General Purpose I/O Function

Change the values of GPIO 9 data register (GPIO9) and GPIO 9 direction register (GPIOD9) to determine 8 input/output.

SYMBOL	PIN	I/O	FUNCTION
GP97	24	I/O_{16tsh}	General Purpose I/O Function
GP96	25	I/O_{16tsh}	General Purpose I/O Function

Continued

SYMBOL	PIN	I/O	FUNCTION
GP95	26	I/O_{16tsh}	General Purpose I/O Function
GP94	27	I/O_{16tsh}	General Purpose I/O Function
GP93	28	I/O_{16tsh}	General Purpose I/O Function
GP92	29	I/O_{16tsh}	General Purpose I/O Function
GP91	30	I/O_{16tsh}	General Purpose I/O Function
GP90	31	I/O_{16tsh}	General Purpose I/O Function

2.16 GPIOA Part

General Purpose I/O Function

Change the values of GPIO A data register (GPIOA) and GPIO A direction register (GPIODA) to determine 8 input/output.

External Interrupt Source Input Function

Change the value of external interrupt enable 1 register to determine External Interrupt.

SYMBOL	PIN	I/O	FUNCTION
GPA7 EXTINT17	15	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA6 EXTINT16	16	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA5 EXTINT15	17	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA4 EXTINT14	18	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA3 EXTINT13	19	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA2 EXTINT12	20	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA1 EXTINT11	21	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA0 EXTINT10	22	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

2.17 GPIOB Part

General Purpose I/O Function

Change the values of GPIO B data register (GPIOB) and GPIO B direction register (GPIODB) to determine 8 input/output.

External Interrupt Source Input Function

Change the value of external interrupt enable 2 register to determine External Interrupt.

SYMBOL	PIN	I/O	FUNCTION
GPB7 EXTINT27	7	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB6 EXTINT26	8	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB5 EXTINT25	9	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB4 EXTINT24	10	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB3 EXTINT23	11	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB2 EXTINT22	12	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB1 EXTINT21	13	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB0 EXTINT20	14	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

2.18 GPIOC Part

General Purpose I/O Function

Change the values of GPIO C data register (GPIOC) and GPIO C direction register (GPIODC) to determine 8 input/output.

External Interrupt Source Input Function

Change the value of external interrupt enable 3 register to determine External Interrupt.

SYMBOL	PIN	I/O	FUNCTION
GPC7 EXTINT37	127	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC6 EXTINT36	128	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC5 EXTINT35	1	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC4 EXTINT34	2	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC3 EXTINT33	3	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC2 EXTINT32	4	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC1 EXTINT31	5	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC0 EXTINT30	6	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

2.19 Power & Clock Part

SYMBOL	PIN	I/O	FUNCTION
XOUT	122	O_c	System Clock Output
XIN	123	I_c	System Clock Input
XCOUT	125	O_c	32.768 KHz Clock Output for RTC function
XCIN	126	I_c	32.768 KHz Clock Input for RTC function
VCC1	23 49 78	I_{vdd}	Normal Power Input, +3.3V
LPCSTS	60	I_{ts}	Power status. Indicates current power status of LPC interface.
GND	32 55 69	I_{vss}	Normal GND
AVCC	112	I_{vdd}	Analog Power Input, +3.3V
AGND	115	I_{vss}	Analog GND
VREF	103	I_{vdd}	Analog Reference Voltage Input

3. ARCHITECTURE DESCRIPTION

In W83L951ADG, memory organization and RAM are designed based on Turbo 51 core controller. Register sets of various function blocks are accessed by Special Function Register (SFR).

According to the differences of accessing approaches, SFR are divided into Address Mapping and External RAM Address Mapping. The relation is showed in Figure 3-1.Function Block Diagram.

- Internal RAM Address Mapping:

  Using direct addressing to access 128 bytes from internal RAM address 80H to 0FFH.
- External RAM Address Mapping:

  Using MOVX to access 256 bytes from external RAM addressing FF00H~FFFFH.

3.1 Internal RAM Address Mapping (Via Direct Addressing)

Function blocks that use Internal RAM Address Mapping are listed below:

Table 3-1.Reset Source Table

NAME	1MHZ USED	RESET SOURCE
8051 Core	No	System Reset.
Internal Interrupt Controller	No	System Reset
PS2 Device Interface	Yes	System Reset + PS2 Reset
Low Pin Count Interface Controller	No	System Reset + LPC Power Fail + LPC Reset
SMBus 0	No	System Reset + SMBUS 0 Reset
SMBus 1	No	System Reset + SMBUS 1 Reset
GPIO Controller	No	System Reset.

Table 3-2.Internal RAM Address Mapping Table

BASE ON 00H	INDEX							
Offset	0	1	2	3	4	5	6	7
80	+GP0	SP	DPL0	DPH0	DPL1	DPH1	ID	VERSION
88	+GP1	CHIPCTRL0	CHIPCTRL1	CHIPCTRL2	DPSEL	INTEN	MMEN	CHIPCTRL3
90	+GP2	KBCCON	LPCCON	DBB0STS	DBB0	DBB0ADDH	DBB0ADDL	SIRQ0
98	+GP3	DBB1STS	DBB1	DBB1ADDH	DBB1ADDL	SIRQ1		
A0	+GP4	KPS2DATA	KPS2CON	KPS2STS	MPS2DATA	MPS2CON	MPS2STS	PS2HSEN
A8	+GP5				DBB2STS	DBB2	DBB2ADDH	DBB2ADDL
B0	+GP6	SM0CR	SM0IREQ	SM0IE	SM0FIFOCON	SM0MFIFO	SM0MCON	SM0MSTS
B8	+GP7	SM0MFIFOSTS	SM0SFIFO	SM0SCON	SM0SSTS	SM0SFIFOSTS		
C0	+GP8	SM1CR	SM1IREQ	SM1IE	SM1FIFOCON	SM1MFIFO	SM1MCON	SM1MSTS
C8	+GP9	SM1MFIFOSTS	SM1SFIFO	SM1SCON	SM1SSTS	SM1SFIFOSTS		
D0	+PSW	GPD0	GPD1	GPD2	GPD3	GPD4	GPD5	GPD6
D8	+GPA	GPD7	GPD8	GPD9	GPDA	GPDB	GPDC	
E0	+ACC	IE1	IE2	IE3	IE4			
E8	+GPB	IREQ1	IREQ2	IREQ3	IREQ4			
F0	+B	IP1	IP2	IP3	IP4			
F8	+GPC	FCON	FADDH	FADDL	FDATA			
Index + 8	8	9	A	B	C	D	E	F

Read Only Reserved + a bit addressable register

3.2 External RAM Address Mapping (Via Indirect Address)

Function blocks that use External RAM Address Mapping are listed below:

Table 3-3.Reset Source Table

NAME	1MHZ USED	RESET SOURCE
Watch Dog Block	Yes	System Reset + WDT Reset
Timer Block	No	System Reset
PWM0/1/2/3 Block	No	System Reset + PWM0/1/2/3 Reset
Serial I/O Block	No	System Reset + SIO Reset
CIR Block	No	System Reset + CIR Reset
AD Convert Block	No	System Reset + AD Reset
DA Convert Block	No	System Reset + DA Reset
External Interrupt Block	No	System Reset + System Reset.
FAN Block	Yes	System Reset + FAN Reset
RTC Block	No	System Reset + RTC Reset
SPI Block	No	System Reset + SPI Reset
RC Block	Yes	System Reset + RC Reset

Table 3-4.External RAM Address Mapping Table

BASE ON FF00H	INDEX							
Offset	0	1	2	3	4	5	6	7
00h	WDTCON	WDTSTS						
08h	SFICON	SFIFWH	SFIADDH	SFIADDL				
10h	PRE1	T1	PRE2	T2				
18h	TM	PREX	TX	PREY	TY		PWMCON0	PWMCON1
20h	PWM0PL	PWM0PH	PWM0HL	PWM0HH	PWM1PL	PWM1PH	PWM1HL	PWM1HH
28h	PWM2PL	PWM2PH	PWM2HL	PWM2HH	PWM3PL	PWM3PH	PWM3HL	PWM3HH
30h	UARTCON	UARTSTS	BRGH	BRGL	UARTBUF			
38h	SPCON	SPSTS	SPDAT	SPER				
40h	CIR	BRD	CIRDATA0	CIRDATA1	CIRDATA2	CIRDATA3	RCDAT	RCCON
48h	RCSTS	RCBL	RCWH	RCWL	RAWLCH	FIFOSTS	RAWFIFOH	RAWFIFOL
50h	ADCCON	ADCDATA	DA1	DA2	ADCPWDN	ADCTEST0	ADCTEST1	
58h								
60h	FAN0	FAN1						
68h								
70H	RTCSEC	RTCSECAL	RTCMIN	RTCMINAL	RTCHR	RTCHRAL		
78H								
80H	EIE1	EIE2	EIE3	EIREQ1	EIREQ2	EIREQ3		
88H	EINTT1	EINTT2	EINTT3	EINTT4	EWKUP0	EWKUP1		
Index + 8	8	9	A	B	C	D	E	F

Read Only Reserved

4. TURBO 8051 CORE BLOCK

Turbo 8051 is fully instruction compatible. It features faster processing speed and better performance. It improves the performance not just by running at high frequency but also reduces the machine cycle duration from the standard 8051 period of twelve clocks to four clock cycles for the majority of instructions. This improves performance by an average of 1.5 to 3 times. Turbo 8051 also provides dual Data Pointers (DPTRs) to speed up block data memory transfers.

In the W83L951ADG, External Wakeup Source will only be controlled by external wakeup configure register, and will not be influenced by internal interrupt configuration. Even relevant interrupt enable or global interrupt enable are not set, the chip can still be waken up.

Table 4-1.8051 Configure Register Definition

8051 CONFIGURE REGISTER (12)									
IntAddr	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D0	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
E0	ACC	Accumulator [7:0]							
F0	B	B[7:0]							
81	SP	Stack Pointer [7:0]							
82	DPL1	Data Pointer 0 [7:0]							
83	DPH1	Data Pointer 0 [15:8]							
84	DPL2	Data Pointer 1 [7:0]							
85	DPH2	Data Pointer 1 [15:8]							
86	ID	Device ID Register							
87	REV	Device Revised Version Register							
8C	DPSEL								DPS
8D	INTEN								INTEN
8E	MMC								MMEN
89	CHIPCTRL0	PWM3EN	PWM2EN	PWM1EN	PWM0EN	UARTEN	ALPCEN	CLKSEL	
8A	CHIPCTRL1	DAEN2	DAEN1	ADEN	RTCEN	KEYEN	WDTEN	PD	IDLE
8B	CHIPCTRL2	FAN2EN	FAN1EN	CIREN	R	MPS2	KPS2	SM1EN	SM0EN
8F	CHIPCTRL3	GP2GK	R	RCEN	SPIEN	SFIEN	R	R	R

Table 4-2.External Wakeup Configure Register Definition

POWER DOWN CONFIGURE REGISTER									
ExtAddr	Name	7	6	5	4	3	2	1	0
8C	EXTWKP0	Reserved				KEY	EXTINT3	EXTINT2	EXTINT1
8D	EXTWKP1	R	R	CIR	RTC	LPC	R	MPS2	KPS2

4.1 Register Description

4.1.1 Program Status Word Register (PSW) (Default Value: 0000_0000)

Bit7: Carry Flag (CY):

Set for an arithmetic operation, which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.

Bit6: Auxiliary Carry (AC):

Set when the previous operation resulted in a carry (during addition) or borrow (during subtraction) from the high order nibble.

Bit5: User Flag 0 (F0):

General-purpose flag can be set or cleared by the user by software.

Bit4~3: Register bank selects bits (RS1, RS0):

RS1	RS0	REGISTER BANK	ADDRESS RANGE
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

Bit2: Overflow Flag (OV):

Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation and vice versa.

Bit1: User Flag 1 (F1):

General-purpose flag that can be set or cleared by the user by software

Bit0: Parity flag (P):

Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

Please refer to MCS-8051 definitions for the details.

4.1.2 Accumulator Register (ACC) (Default Value: 0000_0000)

Bit7~0: Accumulator (A)

The A or ACC register is the standard 8032 accumulator. Please refer to MCS-8051 definitions for the details.

4.1.3 B Register (B) (Default Value: 0000_0000)

Bit7~0: B

The B register is the standard 8032 accumulator. Please refer to MCS-8051 definitions for the details.

4.1.4 Stack Pointer Register (SP) (Default Value: 0000_0111)

Bit7~0: Stack Pointer

Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack. Note: The address range is 00h~FFh.

Please refer to MCS-8051 definitions for the details.

4.1.5 Data Pointer 0 High Byte Register (DPH0) (Default Value: 0000_0000)

This is the high byte of the standard 8032 16-bit data pointer.

4.1.6 Data Pointer 0 Low Byte Register (DPL0) (Default Value: 0000_0000)

This is the low byte of the standard 8032 16-bit data pointer.

4.1.7 Data Pointer 1 High Byte Register (DPH1) (Default Value: 0000_0000)

Same as Data Pointer 1 High Byte Register. It is selected by DPSEL@DPS.

4.1.8 Data Pointer 1 Low Byte Register (DPL1) (Default Value: 0000_0000)

Same as Data Pointer 1 High Byte Register. It is selected by DPSEL@DPS.

4.1.9 Device ID Register (ID) (Default Value: 0001_0010)

Device ID Number = 12h.

4.1.10 Revised Version Register (REV) (Default Value: 0000_0000)

Version Number = 00h

4.1.11 Data Pointer Select Register (DPSEL) (Default Value: 0000_0000)

Bit7~1: Reserved

Bit0: Select Data Pointer 0/1 Register (Default Value: 0)

1: Data Pointer 1 Register

0: Data Pointer 0 Register

4.1.12 All Interrupt Enable Register (INTEN) (Default Value: 0000_0000)

Bit7~1: Reserved

Bit0: Enable 8051 All Interrupt Procedure

1: Enable All 8051 Interrupt Procedure

0: Disable

4.1.13 Memory Mapping Control Register (MMC) (Default Value: 0000_0000)

Bit7~1: Reserved

Bit0: Enable Memory Mapping

1: Enable, 0000~07FFh Data Address Mapping to F800~FFFFh Code Address.

0: Disable

4.1.14 Chip Control 0 Register (CHIPCTRL0) (Default Value: 0000_0000)

Bit 7: Pulse Width Modulator 3 Function Enable

1: Enable Pulse Width Modulator 3 (GP27 GPIO Function Disable)

0: Power down Pulse Width Modulator 3

Bit 6: Pulse Width Modulator 2 Function Enable

1: Enable Pulse Width Modulator 2 (GP26 GPIO Function Disable)

0: Power down Pulse Width Modulator 2

Bit 5: Pulse Width Modulator 1 Function Enable

1: Enable Pulse Width Modulator 1 (GP25 GPIO Function Disable)

0: Power down Pulse Width Modulator 1

Bit 4: Pulse Width Modulator 0 Function Enable

1: Enable Pulse Width Modulator 0 (GP24 GPIO Function Disable)

0: Power down Pulse Width Modulator 0

Bit 3: UART Function Enable

1: Enable UART Block (GP42、GP43 GPIO Function Disable)

0: Power down UART Block

Bit 2: Advance LPC Function Enable

1: Enable CLKRUN# Function. (GP46 GPIO Function Disable)

0: Disable

Bit 1~0: System Clock Select

00: 24MHz, 01: 16MHz, 10: 12MHz, 11: 8MHz

4.1.15 Chip Control 1 Register (CHIPCTRL1) (Default Value: 0000_0000)

Bit 7: D/A 2 Function Enable

1: Enable DAC2 Block (GP57 GPIO Function Disable)

0: Power down DAC2 Block

Bit 6: D/A 0 Function Enable

1: Enable DAC1 Block (GP56 GPIO Function Disable)

0: Power down DAC1 Block

Bit 5: A/D Function Enable

1: Enable ADC Block (GP6 GPIO Function Disable)

0: Power down ADC Block

Bit 4: Real Time Clock Function Enable

1: Enable RTC Block

0: Power down RTC Block

Bit 3: Keyboard Scan Function Enable

1: Enable {GP0, GP1, GP20~23} Keyboard Scan Function and GP3 Key Wakeup Interrupt Function.

0: Disable

Note: To enable Keyboard Scan Function will switch {GP0, GP1, GP20~23} drive current from 12mA to 250uA.

Bit 2: Watch Dog Timer Function Enable

1: Enable WDT Block

0: Power down WDT Block

Bit 1: Whole Chip Power down Enable

1: Power down mode:

When there is not any external interrupt, including CIR interrupt, Key Wake-up interrupt and LPC interrupt, occurs or when PS2 data line is low, the W83L951ADG will stop the external clock to enter power down mode. Otherwise it will clear this bit to 0 automatically.

0: Normal Mode:

When any external interrupt or Key Wake-up interrupt occurs or when PS2 data line goes low, this bit will be cleared to 0 automatically.

Note: If whole chip power down mode and idle mode are both enabled, after leaving power down mode, the W83L951ADG will enter idle mode to wait for internal interrupt.

Bit 0: Whole Chip Idle Enable

1: Idle Mode:

When no interrupt occurs, the W83L951ADG will enter idle mode. Otherwise it will clear this bit to 0 automatically.

0: Normal Mode:

It will clear this bit to 0 when all interrupt events occur.

4.1.16 Chip Control 2 Register (CHIPCTRL2) (Default Value: 0000_0000)

Bit 7: FAN 0 Function Enable

1: Enable FAN0 Block (GP40 GPIO Function Disable)

0: Power down FAN0 Block

Bit 6: FAN 1 Function Enable

1: Enable FAN1 Block (GP41 GPIO Function Disable)

0: Power down FAN1 Block

Bit 5: CIR Function Enable

1: Enable CIR Block (GP84 GPIO Function Disable)

0: Power down CIR Block

Bit 4: Reserved

Bit 3: Mouse PS2 Function Enable

1: Enable Mouse PS2 Block (GP72、GP73 GPIO Function Disable)

0: Power down Mouse PS2 Block (Wakeup by MPS2 is also disabled)

Bit 2: Keyboard PS2 Function Enable

1: Enable Keyboard PS2 Block (GP70、GP71 GPIO Function Disable)

0: Power down Keyboard PS2 Block (Wakeup by KPS2 is also disabled)

Bit 1: SMBUS 1 Function Enable

1: Enable SMBUS1 Block (GP80、GP81 GPIO Function Disable)

0: Power down SMBUS1 Block

Bit 0: SMBUS 0 Function Enable

1: Enable SMBUS0 Block (GP76、GP77 GPIO Function Disable)

0: Power down SMBUS0 Block

4.1.17 Chip Control 3 Register (CHIPCTRL3) (Default Value: 0000_0000)

Bit 7: GP2 Keyboard Scan Function Enable

1: Enable {GP20~23} Keyboard Scan Function and GP3 Key Wakeup Interrupt Function.

0: Disable

Note: To enable Keyboard Scan Function will switch {GP20~23} drive current from 12mA to 250uA.

Bit 6: Reserved

Bit 5: RC Function Enable

1: Enable RC Block (GP84 GPIO Function Disable)

0: Power down CIR Block

Bit 4: SPI Function Enable

1: Enable SPI Block (GP50~53 GPIO Function Disable)

0: Power down SPI Block

Bit 3: SFI Function Enable

1: Enable SFI Block (GP50~53 GPIO Function Disable)

0: Power down SFI Block

Bit2: Reserved

Bit1: Reserved

Bit0: Reserved

4.1.18 External Wake-up 0 Register (EXTWKP0) (Default Value: 0000_0000)

Bit7~4: Reserved

Bit3: Enable Key Wake-up Interrupt to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Bit2: Enable External Interrupt 2 to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Bit1: Enable External Interrupt 1 to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Bit0: Enable External Interrupt 0 to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

4.1.19 External Wake-up 1 Register (EXTWKP1) (Default Value: 0000_0000)

Bit7~5: Reserved

Bit2: Enable CIR Interrupt to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Bit4: Enable RTC Interrupt to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Bit3: Enable LPC Interrupt to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Bit2: Reserved

Bit1: Enable MPS2 Interrupt to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Mouse PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

Bit0: Enable KPS2 Interrupt to wake up the W83L951ADG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Keyboard PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

5. LOW PIN COUNT INTERFACE BLOCK

Table 5-1.Low Pin Count Interface Register Definition

Low Pin Count Interface(LPC) & Serial IRQ & Data Buffer Block(10)									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
91	KBCCON	Reserved			P92EN	HKBEN	HGAEN	GA20SET	GA20CLR
92	LPCCON	DBB1En	DBB0En	SIRQ2EN	SIRQ1EN	SIRQ01EN	SIRQ00EN	DBB2EN	R
93	DBB0STS	UDF[3:0]				CD0	UDF	IBF0	OBF0
94	DBB0	Data Buffer 0 [7:0]							
95	DBB0ADDH	Data Buffer 0 Address High Byte							
96	DBB0ADDL	Data Buffer 0 Address Low Byte							
97	SIRQ0	OBF01 SIRQ Number				OBF00 SIRQ Number			
99	DBB1STS	UDF[3:0]				CD1	UDF	IBF1	OBF1
9A	DBB1	Data Buffer 1 [7:0]							
9B	DBB1ADDH	Data Buffer 1 Address High Byte							
9C	DBB1ADDL	Data Buffer 1 Address Low Byte							
9D	SIRQ1	OBF2 SIRQ Number				OBF1 SIRQ Number			
9E	RESERVED	RESERVED							
AC	DBB2STS	UDF[3:0]				CD2	UDF	IBF2	OBF2
AD	DBB2	Data Buffer 2 [7:0]							
AE	DBB2ADDH	Data Buffer 2 Address High Byte							
AF	DBB2ADDL	Data Buffer 2 Address Low Byte							

Gray: Only with System Reset to initial.

5.1 Register Description

5.1.1 DBB0/1/2 Status Register (DBB0/1/2STS) (Default Value: 0000_?0?0)

Bit7~4: User Define Flag

Bit3: Indicate IDBBx Command/Data (By LRESET_N Pin to reset)

1: Command, 0: Data.

Bit2: User Define Flag

Bit1: Input Buffer Full Flag (By LRESET_N Pin to reset)

1: Full, 0: Empty

Bit0: Output Buffer Full Flag

1: Full, 0: Empty

5.1.2 Data Bus Buffer 0/1/2 Register (DBB0/1/2) (Default Value: 0000_0000)

Write data to the output buffer, and read data from the input buffer.

5.1.3 Data Bus Buffer 0/1/2 Address High Byte Register (DBB0/1/2ADDH) (Default Value: 0000_0000)

DBB0 address is decided according to {DBBxADDH, DBBxADDL}. The default I/O address is 0x00h.

If the transmission is in progress, the address is encoded and decoded in next package.

5.1.4 Data Bus Buffer 0/1/2 Address Low Byte Register (DBB0/1/2ADDL) (Default Value: 0000_0000)

DBB0 address is decided according to {DBBxADDH, DBBxADDL}. The default I/O address is 0x00h.

If the transmission is in progress, the address is encoded and decoded in next package.

5.1.5 Low Pin Count Control Register (LPCCON) (Default Value: 0000_0000)

Bit7: Data Bus Buffer 1 Enable

1: Enable (If the transmission is in progress, the address is encoded and decoded in next package.)

0: Disable

Bit6: Data Bus Buffer 0 Enable

1: Enable (If the transmission is in progress, the address is encoded and decoded in next package.)

0: Disable

Bit5: Serial IRQ 2 Enable

1: Enable (Start generating Serial IRQ for OBF2)

0: Disable (Stop generating Serial IRQ for OBF2)

Bit4: Serial IRQ 1 Enable

1: Enable (Start generating Serial IRQ for OBF1)

0: Disable (Stop generating Serial IRQ for OBF1)

Bit3: Serial IRQ 01 Enable

1: Enable (Start generating Serial IRQ for OBF01)

0: Disable (Stop generating Serial IRQ for OBF01)

Bit2: Serial IRQ 00 Enable

1: Enable (Start generating Serial IRQ for OBF00)

0: Disable (Stop generating Serial IRQ for OBF00)

Bit1: Data Bus Buffer 2 Enable

1: Enable (If the transmission is in progress, the address is encoded and decoded in next package.)

0: Disable

Bit0: Reserved

5.1.6 Serial IRQ 0 Number (SIRQ0) (Default Value: 0000_0000)

Bit7~4: Serial IRQ 01 Number

If the transmission is in progress, IRQ number will be changed in next transmission. Set as 0000, SIRQ01 is disabled.

Bit3~0: Serial IRQ 00 Number

If the transmission is in progress, IRQ number will be changed in next transmission. Set as 0000, SIRQ00 is disabled.

5.1.7 Serial IRQ 1 Number (SIRQ1) (Default Value: 0000_0000)

Bit7~4: Serial IRQ Number for OBF2

If the transmission is in progress, IRQ number will be changed in next transmission. Set as 0000, SIRQ for OBF2 is disabled.

Bit3~0: Serial IRQ Number for OBF 1

If the transmission is in progress, IRQ number will be changed in next transmission. Set as 0000, SIRQ for OBF1 is disabled.

5.1.8 Keyboard Control Register (KBCCON)(Default Value: 0000_0001)

Bit7~5: Reserved

Bit4: Port 92 Enable (Default Value: 0)

1: Enable W83L951ADG's hardware logic to receive the data written in I/O address@0092h. Bit1 and bit0 of port92 control Gate A20 and the KBRST pin. Gate A20 will drive high when bit1 is 1 and KBRESET pin drives {14us High → 6us Low → High} waveform when bit 0 is 1. The default of Gate A20 is high after LPC reset and GP44, GP45 GPIO functions are disabled.

0: Disable

Bit3: Hardware Keyboard Reset Control Enable (Default Value: 0)

1: Enable W83L951ADG's hardware logic to set KBRESET. When the KBC receives data that follow a "FE" command, the KBRESET pin drives {14us High → 6us Low → High} waveform. GP44 GPIO function is disabled.

0: Disable

Bit2: Hardware Gate A20 Control Enable (Default Value: 0)

1: Enable W83L951ADG's hardware logic to set Gate A20. When the KBC receives data that follow a "D1" command, the Gate A20 pin drives high. GP45 GPIO function is disabled.

0: Disable

Bit1: Gate A20 Set

Set directly Gate A20 Output Register. If the host is setting from LPC Interface, the request will be ignored. Such a setting has to be done through software control.

Bit0: Gate A20 Clear/Gate A20 Status

Clear directly Gate A20 Output Register. If the host is setting from LPC Interface, the request will be ignored. Such a setting has to be done through software control.

6. PERSONAL SYSTEM 2 BLOCK

The Winbond Keyboard controller has two independent PS/2 serial ports implemented in hardware, which are directly controlled by the 8051 chip. Each of the two PS/2 serial channels uses a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has two signal lines: Clock and Data. Both signal lines are bi-directional and open-drain. The PS2DATA, PS2CON and PS2STS are defined individually for each PS/2 channel. PS2HSEN is only one register to control all of the handshake actions of PS/2 device.

Table 6-1.Personal System 2(PS2) Register Definition

Keyboard & Mouse & Auxiliary PS2 Block(9)									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A1	KPS2DATA	KPS2 Data register [7:0]							
A2	KPS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	KPS2T/R
A3	KPS2STS	KPS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY
A4	MPS2DATA	MPS2 Data register [7:0]							
A5	MPS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	MPS2T/R
A6	MPS2STS	MPS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY
A7	PS2HSEN	Reserved							HSEN

Gray: Only with System Reset to initial.

6.1 Register Description

6.1.1 PS/2 Handshake Enable Register (PS2HSEN) (Default Value:: 0000_0000)

Bit 7~1: Reserved (always return 'LOW')

Bit 0: Handshake Mode Enable (HSEN)

0: The handshake mode of PS2 disabled.

1: The handshake mode of PS2 enabled.

When the handshake mode of PS2 is enabld, the TR bit (BIT 0) of PSCON is automatically set high when the START_DEC bit (bit 6) of PS2STS of the other channel is set.

Note:

1) The priority of the three PS2 interface is KPS2 > MPS2

2)Whether the handshake mode of PS2 is enabled or not, the TR bit (BIT 0) of PSCON is automatically set high when the RDATA_RDY bit (bit 0) of PS2STS of this channel is set.

6.1.2 PS/2 T/R DATA Registers (PS2DATA) (Default Value: 1111_1111)

Transmit:

The byte written to this register, when PS2_T/R = 1, PS2_EN = 1 and XMIT_BUSY = 0, is transmitted automatically by the PS/2 channel control logic. On successful start of this transmission, the PS2 logic will automatically set XMIT_BUSY to high. If PS2_T/R = 0, PS2_EN = 0 or XMIT_BUSY = 1, writes to this register are ignored.

On successful completion of this transmission or upon a Transmit Time-out condition the PS2_T/R and XMIT_BUSY bits are automatically set to low. The PS2_T/R bit must be written to HIGH before initiating another transmission to the remote device.

Note:

1)Even if PS2_T/R = 1, PS2_EN = 1 and XMIT_BUSY = 0, writing the transmit Register will hold the current transmission if RDATA_RDY is set. The automatic PS2 logic forces data to be read from Receive Register before allowing a transmission.

2) An interrupt is generated in the high-to-low transition of XMIT_BUSY.

3) All bits of this register are write-only for transmit data, because the received data are always read.

Receive:

When PS2_EN=1 and PS2_T/R=0, the PS2 Channel is set to automatically receive data on that channel (both the CLK and DATA lines will float waiting for the peripheral to initiate a reception by sending a start bit followed by the data bits). After a successful reception, the data are placed in this register with the RDATA_RDY bit set and the CLK line forced low by the PS2 channel logic. RDATA_RDY is cleared and the CLK line is released to hi-z following a read of this register. This automatically holds off further receive transfers until the 8051 has had a chance to receive the data.

Note:

1)The Receive Register is initialized to 0xFF after a Timeout has occurred.

2) The channel can be enabled to automatically transmit data (PS2_EN=1) by setting PS2_T/R while RDATA_RDY is set. However, a device (host not included) transmission can hold until the data has been read from the Receive Register.

3)An interrupt is generated in the low-to-high transition of RDATA_RDY.

4)If a receive timeout (REC_TIMEOUT=1) or a transmit timeout (XMIT_TIMEOUT =1) occurs the, channel is busy (CLK held low) for 300us (Hold Time) to guarantee that the peripheral aborts. Writing to the Transmit Register will be allowed; however, the data written will not be transmitted until the Hold Time expires.

5)In the foregoing case, RDATA_RDY will not automatically clear.

6.1.3 PS/2 Control Registers (PS2CON) (Default Value:: 0000_0000)

Bit 7: NOISE FILTER ENABLE (NFEN)

0: Disable noise filter for clock line

1: Enable noise filter for clock line

Bit 6: Inhibit bit

The low-to-high transition of the inhibit bit will hold the clock line low for 100us.

Bit 5-4: STOP

Bits [5:4] of the Control Register are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits [5:4] =

00: Receiver expects an active high stop bit.

01: Receiver expects an active low stop bit.

10: Receiver ignores the level of the Stop bit (The 11th bit is not interpreted as a stop bit).

11: Reserved.

Bit 3-2: PARITY

Bits [3:2] of the Control Register are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits [3:2] =

00: Receiver expects Odd Parity (Default Value).

01: Receiver expects Even Parity.

10: Receiver ignores level of the parity bit (The 10th bit is not interpreted as a parity bit).

11: Reserved.

Bit 1: PS2_EN PS2 Channel Enable

When PS2_EN=1 the PS/2 State machine is enabled, allowing the channel to perform automatic reception or transmission depending on the bit value of PS2_T/R. When PS2_EN = 0, the channel's automatic PS/2 state machine is disabled.

Note:

1)If the PS2_EN bit is cleared prior to the rising edge of the 10th (parity bit) clock edge, the received data are discarded (RDATA_RDY remains low).

2)If the PS2_EN bit is cleared following the rising edge of the 10th clock signal, then the received data are saved in the Receive Register (RDATA_RDY goes high) assuming no parity error.

3)In the foregoing two cases, ps2 device cannot tell whether the data are received successfully or not, and therefore this function is not recommended. It shall set to high before any operation of PS2 is started.

Bit 0: PS2_T/R PS/2 Channel Transmit/Receive

This bit is valid only when PS2_EN=1 and sets the PS2 logic for automatic transmission or reception when PS2_T/R equals HIGH or LOW respectively (This bit may be modified, after unsetting PS2_EN).

When set, the PS/2 channel is enabled to transmit data. To properly initiate a transmit operation this bit must be set prior to writing to the Transmit Register; writes are blocked to the Transmit Register when this bit is not set.

Upon setting the PS2_T/R bit the channel will drive its CLK line low, float the DATA line and hold this state until a write occurs to the Transmit Register or until the PS2_T/R bit is cleared. Writing to the Transmit Register initiates the transmit operation. KB controller drives the data line low and, within 100us, floats the clock line (externally pulled high by the pull-up resistor) to signal the external PS/2 device that data are now available.

The PS2_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Timeout error occurs.

Note:

1)If the PS2_T/R bit is set while the channel is actively receiving data prior to the rising edge of the 10th (parity bit) clock edge, the received data are discarded. If this bit is not set prior to the 10th clock signal then the received data are saved in the Receive Register.

2) When the PS2_T/R bit is cleared, the PS/2 channel is enabled to receive data. Upon clearing this bit, whether RDATA_RDY=0 or not, the channel's CLK and DATA will float waiting for the external PS/2 device to signal the start of a transmission to receive data. But if RDATA_RDY=1, the hardware will not generate interrupt to indicate finishing receiving data.

3) If the PS2_T/R bit is set while RDATA_RDY=,1 then the channel's DATA line will float but its CLK line will be held low, holding off the peripheral, until the Receive Register is read.

6.1.4 PS/2 Status Registers (PS2STS) (Default Value: 0000_0000)

Bit 7: Receiver Busy (RX_BUSY)

This bit is the indicator for each of the three PS/2 Channels. When a RX_BUSY bit is set, the associated channel is actively receiving PS/2 data; when a RX_BUSY bit is cleared, the channel is idle.

Bit 6: Start Bit Detect (START_DEC)

This bit is set on detecting the start bit of receiving conditions. Writing high will clear this bit.

Bit 5: Transmitter Timeout (XMIT_TIMEOUT)

This bit is set on one of the 3 transmitting conditions. The channel's CLK line is automatically pulled low and held for a period of 300us following the assertion of the XMIT_TIMEOUT bit, during the same period of time, PS2_T/R is also held low:

1)When the transmitter bit time (time between falling edges) exceeds 300us.

2)If the transmitter start bit is not received within 25ms from signaling a transmit start event.

3)If the time from the 1st (start, falling edge) bit to the 11th (stop, falling edge) bit exceeds 2ms.

Writing high will clear this bit.

Bit 4: Transmitter Busy (XMIT_BUSY)

When high, the XMIT_BUSY bit is a status bit indicating that the PS2 channel is actively transmitting data to the PS2 peripheral device. Writing to the Transmit Register despite whether the channel is ready for transmission will cause the XMIT_BUSY bit to assert and remain asserted until one of the following conditions occurs and an Interrupt is generated.

1)The falling edge of the 11th CLK; upon a Transmit Timeout condition (XMIT_TIMEOUT goes high);

2)Upon the PS2_T/R bit being written to 0.

3)Upon the PS2_EN bit being written to 0.

Note: An interrupt is generated on the high-to-ow transition of XMIT_BUSY.

Bit 3: Framing Error (FE)

When receiving data, the stop bit is clocked in on the falling edge of the 11th CLK edge. If the channel has been set to expect either a high or low stop bit and the 11th bit is contrary to the expected stop polarity, then the FE and REC_TIMEOUT bits are set following the falling edge of the 11th CLK edge and an Interrupt is generated. Writing high will clear this bit.

Bit 2: Parity Error (PE)

When receiving data, the parity bit is clocked in on the falling edge of the 10th CLK edge. If the channel has been set to expect either even or odd parity and the 10th bit is contrary to the expected parity, then the PE and REC_TIMEOUT bits are set following the falling edge of the 10th CLK edge and an Interrupt is generated. Writing high will clear this bit.

Bit 1: Receiver Timeout (REC_TIMEOUT)

Under PS2 automatic operation, PS2_EN=1, this bit is set on one of the 4 receive error conditions. The Channel's CLK line is automatically pulled low and held for a period of 300us following the assertion of the REC_TIMEOUT bit:

1)When the receiver bit time (time between falling edges) exceeds 300us.

2)If the time from the 1st (start, falling edge) bit to the 10th (stop, falling edge) bit exceeds 2ms.

3)On a receive parity error along with the parity error (PE) bit.

4)On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit. Writing high will clear this bit.

Note: An Interrupt is generated on the low-to-high transition of the REC_TIMEOUT bit.

Bit 0: Data Ready (RDATA_RDY)

Receive Data Ready: Under normal operating conditions, this bit is set on the falling edge of the 11th clock which successfully receives a data byte from the PS/2 peripheral (i.e., no parity, framing, or receive timeout errors) and indicates that the received data byte is available to be read from the Receive Register. This bit may also be set in the event that the PS2_EN bit is cleared following the 10th CLK edge (see the PS2_EN bit description for further details). Reading the Receive Register clears this bit.

Note: An Interrupt is generated on the low to high transition of the RDATA_RDY bit.

7. SYSTEM MANAGEMENT BUS BLOCK

The W83L951ADG provides 2 System Management Bus (SMBus) host controllers. The SMBus host controllers is SMBUS 2.0 compatible. It also provides 32 bytes FIFO. The FIFO contains SMBus0 Master Data FIFO(8), SMBus1 Master Data FIFO(8).

Table 7-1.SMBus 0 Register Definition

SMBus 0 Block									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
B1	SM0SCR	Reserved		Baud Rate Select			RBIM	Reserved	Reserved
B2	SM0IREQ	MSTS	MFIFORdy	MFIFOReq	MPktFinish	SSTS	SFIFORdy	SFIFOReq	SPktFinish
B3	SM0IE	Interrupt Enable [7:0]							
B4	SM0FIFOCON	STOP	RepStart	Master Level[1:0]		ClrMFIFO	ClrSFIFO	Slave Leve[1:0]	
B5	SM0MFIFO	Master Data FIFO [7:0]							
B6	SM0MCON	MasterEn	RMS	Read Byte Count[5:0]					
B7	SM0MSTS	RxTMO	TxTMO	AlFull	AlEmty	WrErr	NACKRec	ArbFail	ClrFinish
B9	SM0MFIFOSTS	Full	Empty	FIFO Data Length[5:0]					
BA	SM0SFIFO	Slave Data FIFO[7:0]							
BB	SM0SCON	SlaveEn	Slave Address[6:0]						
BC	SM0SSTS	RxTMO	TxTMO	AlFull	AlEmty	WrErr	R	ArbFail	ClrFinish
BD	SM0SFIFOSTS	Full	Empty	FIFO Data Length[5:0]					

Table 7-2.SMBus 1 Register Define

SMBus 1 Block									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C1	SM1SCR	Reserved		Baud Rate Select			RBIM	Reserved	Reserved
C2	SM1IREQ	MSTS	MFIFORdy	MFIFOReq	MPktFinish	SSTS	SFIFORdy	SFIFOReq	SPktFinish
C3	SM1IE	Interrupt Enable [7:0]							
C4	SM1FIFOCON	STOP	RepStart	Master Level[1:0]		ClrMFIFO	ClrSFIFO	Slave Leve[1:0]	
C5	SM1MFIFO	Master Data FIFO [7:0]							
C6	SM1MCON	MasterEn	RMS	Read Byte Count[5:0]					
C7	SM1MSTS	RxTMO	TxTMO	AlFull	AlEmty	WrErr	NACKRec	ArbFail	ClrFinish
C9	SM1MFIFOSTS	Full	Empty	FIFO Data Length[5:0]					
CA	SM1SFIFO	Slave Data FIFO[7:0]							
CB	SM1SCON	SlaveEn	Slave Address[6:0]						
CC	SM1SSTS	RxTMO	TxTMO	AlFull	AlEmty	WrErr	R	ArbFail	ClrFinish
CD	SM1SFIFOSTS	Full	Empty	FIFO Data Length[5:0]					

Gray: Only with System Reset to initial.

7.1 Register Description

7.1.1 System Control Register (SM0/1SCR) (Default Value: 0001_10?0)

Bit 7~6: Reserved (Must Assign Low)

Bit 5~3: Baud Rate Select

Select SMBus baud rate.

000: 12.5 KHz, 001: 25 KHz, 010: 50 KHz, 011: 100 KHz

100: 200 KHz, 101: 400 KHz, 110: 800 KHz, 111: 800 KHz

Bit 2: Rx Byte Interrupt Mode

Select the mode that SMBus receives data bytes to generate Master/Slave Data Ready interrupt.

0: Only First Byte and FIFO Full Byte:

Master/Slave Data Ready Interrupt only occurs in receiving the first byte after Start phase or Repeat_Start phase and any byte that makes FIFO enter Full state.

1: Every Byte:

Master/Slave Data Ready Interrupt occurs every time when finishing receiving one byte.

Bit 1: SMBALERT Pin Status (Reserved)

Bit 0: SMBALTER Event Control (Reserved)

Control the occurrence of SMBALTER Event

0: Disable

1: Enable.

7.1.2 Interrupt Register (SM0/1IREQ) (Default Value: 0000_0000)

Bit 7: Master Status

Indicate Master Status Register is changed.

Bit 6: Master FIFO Data Ready Interrupt

Indicate that FIFO finishes receiving the first data byte when Master is under MSR (Master at Receiving) mode.

Bit 5: Master FIFO Data Request Interrupt

Indicate that FIFO request micro-processor provides data for transmitting to Salve when Master is under MST (Master at Transmitting) mode and empty.

Bit 4: Master Packet Finished Interrupt

Indicate that Master finishes package transmission (Include Rx and Tx).

Bit 3: Slave Status

Indicate Slave Status Register is changed.

Bit 2: Slave FIFO Data Ready Interrupt

Indicate that FIFO finishes receiving the first data byte when Slave is under SLR (Slave at Receive) mode.

Bit 1: Slave FIFO Data Request Interrupt

Indicate that FIFO Request provides data to transmit to Master.

The request occurs in two conditions:

1) Slave is at SLT (Slave at Transmitting) and furthermore FIFO is empty state.
2) Slave receives a read-type package.

Bit 0: Slave Packet Finished Interrupt

Indicate that Slave finishes package transfer (Include Rx and Tx).

7.1.3 Interrupt Enable Register (SM0/11IE) (Default Value: 0000_0000)

All Bits:

1: Enable Interrupt.
The content of Interrupt Register via OR operation will convert into Microprocessor Internal Interrupt Source.

0: Disable Interrupt.
Disable convert into Microprocessor Internal Interrupt, but relative interrupt flag will still be produced.

7.1.4 FIFO Control Register (SM0/11FIFOCON) (Default Value: 0000_0000)

Bit 7: STOP Tag Flag (Only for Master)

Indicate that the writing byte is the last byte.

Bit 6: Repeat_Start Tag Flag (Only for Master)

Indicate that the writing byte is Repeat_Start Byte.

Bit 5~4: Master FIFO Threshold Level Select

00: AE – 2, AF – 6, 01: AE - 3, AF – 4

10: AE – 4, AF – 3, 11: AE – 6, AF - 2

Note: AE is Almost Empty Flag, AF is Almost Full Flag.

Bit 3: Clear Master FIFO

Clear Master FIFO. Master will stop transfer immediately and generate a Stop phase. After SMBus finishes the action, SMBus responds to micro-processor via FIFO Clear Finished Event in Master Status Register.

Bit 2: Clear Slave FIFO

Clear Slave FIFO. After slave responds as NACK, next byte transfer will be stopped immediately. SMBus responds to micro-processor via FIFO Clear Finished Event in Slave Status Register.

Bit 1~0: Slave FIFO Threshold Level Select

00: AE – 2, AF – 6, 01: AE - 3, AF – 4

10: AE – 4, AF – 3, 11: AE – 6, AF - 2

Note: AE is Almost Empty Flag, AF is Almost Full Flag.

7.1.5 Master Data FIFO Register (SM0/11MFIFO) (Default Value: 0000_0000)

This FIFO register stores the data from Master.

In MST mode, only writing is allowed, and in MSR mode, only read is allowed. The default is MST mode and the transforming is through Data_Ready_Interrupt.

7.1.6 Master Control Register (SM0/1MCON) (Default Value: 0100_0000)

Bit 7: Master Enable

Bit 6: Read Mode Select

1: Host Read One Byte Hold Mode.
Master holds the bus (drives SCL low) after finishing receiving every byte.

0: Host Read Continue Mode.

Master finishes {Receiving Package -> Stop Phase -> Release Bus} automatically according to read byte count.

Note: If the Read Byte Count initial value is 1, Master will ignore the criterion of "Host Read One Byte Hold Mode".

Bit 5~0: Read Byte Count

Indicate Read Byte Count. The allowed maximum is 64 bytes block read.

FILLED VALUE	ACTUAL VALUE
0	64
1~63	1~63

7.1.7 Master Status Register (SM0/1MSTS) (Default Value: 0000_0000)

Bit 7: Master Rx Timeout Event

Indicate Master generates RX_TIMEOUT (When Master FIFO is full, SCL drive low to generate timeout). After Master generates Stop Phase, it will return to the initial state and clear FIFO.

Note: If timeout is not generated by Master, the response will occur in FIFO Clear Finished Event in Master Status Register.

Bit 6: Master Tx Timeout Event

Indicate Master generates TX_TIMEOUT (When Master FIFO is empty, SCL drives low to generate timeout). After Master generates Stop Phase, it will return to initial state and clear FIFO.

Note: If timeout is not generated by Master, the response is in FIFO Clear Finished Event in Master Status Register.

Bit 5: Master Almost Full Event

Indicate that Master generate Almost Full Event. It occurs only up to Almost Full level.

Bit 4: Master Almost Empty Event

Indicate that Master generates Almost Empty Event. It occurs only down to Almost Empty level.

Bit 3: Master FIFO Data Write Error Event

Indicate that Microprocessor writes to Master FIFO; Master FIFO is full or Read Mode.

Bit 2: NACK Received Event

Indicate that Master receives NACK. After generating Stop Phase, Master will return to the initial state and clear FIFO.

Note: Wait for the response of Clear Finished Event in Master Status Register to start next transfer.

Bit 1: Bus Arbitration Failed Event

Indicate failed bus arbitration. Master will return to the initial state and clear FIFO.

Bit 0: FIFO Clear Finished Event

Indicate that Master finishes the request to clear FIFO.

7.1.8 Master FIFO Status Register (SM0/1MFIFOSTS) (Default Value: 0100_0000)

Bit 7: Full Flag

Bit 6: Empty Flag

Bit 5~4: Reserved

Bit 3~0: FIFO Data Length

7.1.9 Slave Data FIFO Register (SM0/1SFIFO) (Default Value: 0000_0000)

This FIFO register stores the data from Slave. In SLT mode, only writing is allowed, and in SLR mode, only read is allowed. The default is SLR mode and the transforming is through Data_Request_Event.

7.1.10 Slave Control Register (SM0/11SCON) (Default Value: 0000_0000)

Bit 7: Slave Enable

Bit 6~0: Slave Address

In addition to receiving data from the address, the slave receives data from 00h and 62h.

7.1.11 Slave Status Register (SM0/11SSTS) (Default Value: 0000_0000)

Bit 7: Slave Rx Timeout Event

Indicate that Slave generates RX_TIMEOUT (When Slave FIFO is full, SCL is driven low to generate timeout). Slave will enter to the initial state and clear FIFO.

Note: If timeout is not generated by Slave, the response is in FIFO Clear Finished Event in Slave Status Register.

Bit 6: Slave Tx Timeout Event

Indicate the generation of TX_TIMEOUT (When Slave FIFO is empty, SCL is driven low to generate timeout). Slave will enter the initial state and clear FIFO.

Note: If timeout is not generated by Slave, the response is in FIFO Clear Finished Event in Slave Status Register.

Bit 5: Slave Almost Full Event

Indicate that Slave generates Almost Full Event upward.

Bit 4: Slave Almost Empty Event

Indicate that Slave generate Almost Empty Event downward.

Bit 3: Slave FIFO Data Write Error Event

Indicate that Microprocessor writes to Slave FIFO, Slave FIFO is in the full or Read Mode.

Bit 2: SMBALTER Event

Indicate that the SMBALERT pin enters low level.

Bit 1: Bus Arbitration Failed Event

Indicate failed bus arbitration, Slave will enter the initial state and clear FIFO.

Bit 0: FIFO Clear Finished Event

Indicate that Slave finishes the request to clear FIFO.

Note:

After clearing FIFO data, Slave waits for Stop Phase to end the transfer.

7.1.12 Slave FIFO Status Register (SM0/1SFIFOSTS) (Default Value: 0100_0000)

Bit 7: Full Flag

Bit 6: Empty Flag

Bit 5~4: Reserved

Bit 3~0: FIFO Data Length

8. INTERNAL INTERRUPT CONTROLLER BLOCK

The W83L951ADG Interrupts occur by 32 sources, 24 external and 29 internal interrupt.

About Interrupt Control, each interrupt is controlled and corresponding to a bit in Interrupt Enable Register (IE1/2/3/4), the Interrupt Priority Control Register (IP1/2/3/4) and the Interrupt Request Register (IREQ1/2/3/4).

An interrupt occurs if the corresponding Interrupt Request occurs and enabled bits are HIGH. If several interrupts occur at the same time, the interrupts are received according to priority setting. If no interrupt priority is set, it is decided by hardware internal checking rule.

Table 8-1.Internal Interrupt Controller Register Definition

Interrupt Block(17)									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
E1	IE1	TimerY	TimerX	Timer2	Timer1	OBE1	IBF1	OBE0	IBF0
E2	IE2	CNTR1	CNTR0	ADC	RTC	KEY-WP	EXINT2	EXTINT1	EXTINT0
E3	IE3	FAN1	FAN0	CIR	R	MPS2	KPS2	SMBUS1	SMBUS0
E4	IE4	R	R	RC	SPI	OBE2	IBF2	UARTRX	UARTTX
E9	IREQ1	TimerY	TimerX	Timer2	Timer1	OBE1	IBF1	OBE0	IBF0
EA	IREQ2	CNTR1	CNTR0	ADC	RTC	KEY-WP	EXINT2	EXTINT1	EXTINT0
EB	IREQ3	FAN1	FAN0	CIR	R	MPS2	KPS2	SMBUS1	SMBUS0
EC	IREQ4	R	R	RC	SPI	OBE2	IBF2	UARTRX	UARTTX
F1	IP1	TimerY	TimerX	Timer2	Timer1	OBE1	IBF1	OBE0	IBF0
F2	IP2	CNTR1	CNTR0	ADC	RTC	KEY-WP	EXINT2	EXTINT1	EXTINT0
F3	IP3	FAN1	FAN0	CIR	R	MPS2	KPS2	SMBUS1	SMBUS0
F4	IP4	R	R	RC	SPI	OBE2	IBF2	UARTRX	UARTTX

Table 8-2 Internal Interrupt Vector & Trigger Type Table

SOURCE	VECTOR ADDRESS	TRIGGER TYPE
Non-mask Interrupt	0x0003	Edge Trigger
LPC Power Fail Interrupt	0x000b	Edge Trigger
Input Buffer 0 Full Interrupt	0x0013	Edge Trigger
Output Buffer 0 Empty Interrupt	0x001b	Edge Trigger
Input Buffer 1 Full Interrupt	0x0023	Edge Trigger
Output Buffer 1 Empty Interrupt	0x002b	Edge Trigger
Timer 1 Interrupt	0x0033	Edge Trigger
Timer 2 Interrupt	0x003b	Edge Trigger
Timer X Interrupt	0x0043	Edge Trigger
Timer Y Interrupt	0x004b	Edge Trigger
External Interrupt Group 0	0x0053	Level Trigger
External Interrupt Group 1	0x005b	Level Trigger
External Interrupt Group 2	0x0063	Level Trigger
Key Interrupt	0x006b	Edge Trigger
Real Time Clock Alarm Interrupt	0x0073	Edge Trigger
ADC Interrupt	0x007b	Edge Trigger
CNTR0 Interrupt	0x0083	Edge Trigger
CNTR1 Interrupt	0x008b	Edge Trigger
SMBUS 0 Interrupt	0x0093	Level Trigger
SMBUS 1 Interrupt	0x009b	Level Trigger
Keyboard PS2 Interrupt	0x00a3	Edge Trigger
Mouse PS2 Interrupt	0x00ab	Edge Trigger
Reserved	0x00b3	Edge Trigger
CIR Interrupt	0x00bb	Edge Trigger
FAN 0 Interrupt	0x00c3	Level Trigger
FAN 1 Interrupt	0x00cb	Level Trigger
UART Tx Interrupt	0x00d3	Edge Trigger
UART Rx Interrupt	0x00db	Edge Trigger
Input Buffer 2 Full Interrupt	0x00e3	Edge Trigger
Output Buffer 2 Empty Interrupt	0x00eb	Edge Trigger
SPI interrupt	0x00f3	Edge Trigger
RC interrupt	0x00fb	Edge Trigger

8.1 Register Description

8.1.1 Interrupt Enable 1 Register (IE1) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor to generate Interrupts, and writes down '1' in Interrupt Request 1 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor to generate Interrupts, but writes down '0' in Interrupt Request 1 Register.

8.1.2 Interrupt Enable 2 Register (IE2) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor to generate Interrupts, and writes down '1' in Interrupt Request 2 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor to generate Interrupts, but writes down '0' in Interrupt Request 2 Register.

8.1.3 Interrupt Enable 3 Register (IE3) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor that Interrupt will be produced, and write down in Interrupt Request 3 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor that Interrupt will be produced, but write down in Interrupt Request 3 Register.

8.1.4 Interrupt Enable 4 Register (IE4) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor to generate Interrupts, and writes down '1' in Interrupt Request 4 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor to generate Interrupts, but writes down '0' in Interrupt Request 4 Register.

8.1.5 Interrupt Request 1 Register (IREQ1) (Default Value: 0000_0000)

Read:

1: Requested

0: Not Requested

Write:

1: Clear

0: No Change

8.1.6 Interrupt Request 2 Register (IREQ2) (Default Value: 0000_0000)

Read:

1: Requested

0: Not Requested

Write:

1: Clear

0: Not Change

8.1.7 Interrupt Request 3 Register (IREQ3) (Default Value: 0000_0000)

Read:

1: Requested

0: Not Requested

Write:

1: Clear

0: Not Change

8.1.8 Interrupt Request 4 Register (IREQ4) (Default Value: 0000_0000)

Read:

1: Requested

0: Not Requested

Write:

1: Clear

0: Not Change

8.1.9 Interrupt Priority 1 Register (IP1) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

8.1.10 Interrupt Priority 2 Register (IP2) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

8.1.11 Interrupt Priority 3 Register (IP3) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

8.1.12 Interrupt Priority 4 Register (IP4) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

9. GPIOS BLOCK

The W83L951ADG provides 13 GPIO blocks, and every GPIO block has 8 GPIO that can be set individually. I/O Pad has three states by data register and direction register setting. The input register always reads the current pad status.

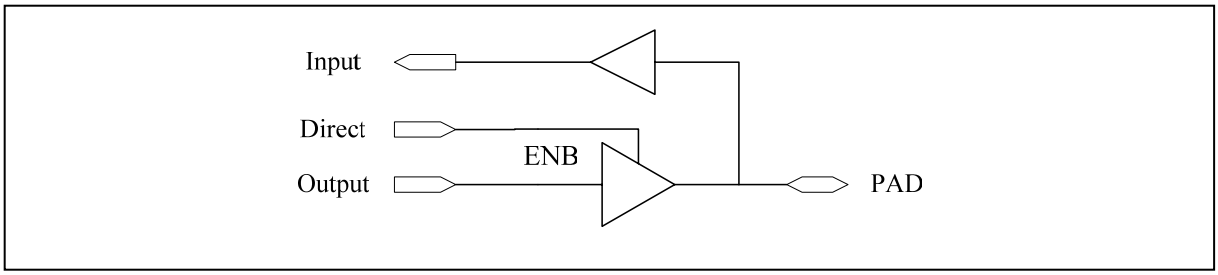


Figure 9-1.GPIO Block Diagram

Table 9-1.GPIOs Type Setup Definition

TYPE	OUTPUT REGISTER(WRITE)	DIRECTION REGISTER
Input	Don't Care	0
Output	Output Data	1
Open-Drain	0	Output Data'

Table 9-2.GPIOs Control Register Definition

GPIO BLOCK(26)									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
80	GPIO0	GPIO 0 Input/Output Register[7:0]							
88	GPIO1	GPIO 1 Input/Output Register[7:0]							
90	GPIO2	GPIO 2 Input/Output Register[7:0]							
98	GPIO3	GPIO 3 Input/Output Register[7:0]							
A0	GPIO4	GPIO 4 Input/Output Register[7:0]							
A8	GPIO5	GPIO 5 Input/Output Register[7:0]							
B0	GPIO6	GPIO 6 Input/Output Register[7:0]							
B8	GPIO7	GPIO 7 Input/Output Register[7:0]							
C0	GPIO8	GPIO 8 Input/Output Register[7:0]							
C8	GPIO9	GPIO 9 Input/Output Register[7:0]							
D8	GPIOA	GPIO A Input/Output Register[7:0]							
E8	GPIOB	GPIO B Input/Output Register[7:0]							
F8	GPIOC	GPIO C Input/Output Register[7:0]							

Continued

GPIO BLOCK(26)									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D1	GPIOD0	GPIO 0 Direction Register[7:0]							
D2	GPIOD1	GPIO 1 Direction Register[7:0]							
D3	GPIOD2	GPIO 2 Direction Register[7:0]							
D4	GPIOD3	GPIO 3 Direction Register[7:0]							
D5	GPIOD4	GPIO 4 Direction Register[7:0]							
D6	GPIOD5	GPIO 5 Direction Register[7:0]							
D7	GPIOD6	GPIO 6 Direction Register[7:0]							
D9	GPIOD7	GPIO 7 Direction Register[7:0]							
DA	GPIOD8	GPIO 8 Direction Register[7:0]							
DB	GPIOD9	GPIO 9 Direction Register[7:0]							
DC	GPIODA	GPIO A Direction Register[7:0]							
DD	GPIODB	GPIO B Direction Register[7:0]							
DE	GPIODC	GPIO C Direction Register[7:0]							

9.1 GPIO Data Register Description

9.1.1 GPIO 0 Input/Output Register (GPIO0) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result.

For example "CPL Bit" Instruction

1) Read Pin Status into temp Register.

2) Invert temp register.

3) The results are written independently to Output Data Register according to the bit address, and the values of the other bits are not influenced.

9.1.2 GPIO 1 Input/Output Register (GPIO1) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.3 GPIO 2 Input/Output Register (GPIO2) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.4 GPIO 3 Input/Output Register (GPIO3) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.5 GPIO 4 Input/Output Register (GPIO4) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.6 GPIO 5 Input/Output Register (GPIO5) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.7 GPIO 6 Input/Output Register (GPIO6) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.8 GPIO 7 Input/Output Register (GPIO7) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.9 GPIO 8 Input/Output Register (GPIO8) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.10 GPIO 9 Input/Output Register (GPIO9) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.11 GPIO A Input/Output Register (GPIOA) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.12 GPIO B Input/Output Register (GPIOB) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.1.13 GPIO C Input/Output Register (GPIOC) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: The bit command and the byte command have the same result

9.2 GPIO Direction Register Description

9.2.1 GPIO 0 Direction Register (GPIOD0) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.2 GPIO 1 Direction Register (GPIOD1) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.3 GPIO 2 Direction Register (GPIOD2) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.4 GPIO 3 Direction Register (GPIOD3) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.5 GPIO 4 Direction Register (GPIOD4) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.6 GPIO 5 Direction Register (GPIOD5) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.7 GPIO 6 Direction Register (GPIOD6) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.8 GPIO 7 Direction Register (GPIOD7) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.9 GPIO 8 Direction Register (GPIOD8) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.10 GPIO 9 Direction Register (GPIOD9) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.11 GPIO A Direction Register (GPIODA) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.12 GPIO B Direction Register (GPIODB) (Default Value: 0000_0000)

1: Output,

0: Input.

9.2.13 GPIO C Direction Register (GPIODC) (Default Value: 0000_0000)

1: Output,

0: Input.

10. SROM BLOCK

10.1 Register Define

10.1.1 Control Register

Bit7: SFI Enable

Bit6-5: BIOS Range

00: 1M, 01: 2M, 10: 4M, 11: 8M

Bit4: Disable E0000~EFFFF

Bit3: Disable FFE0000~FFEFFFF

Bit2: BIOS Write Enable

Bit1: BIOS Enable

Bit0: Disable F0000~FFFFF

10.1.2 FWH Control Register

Bit7-4: Reserved

Bit3-0: IDSEL

10.1.3 Address High/Low Register

Configuration Base Address, default 0x004E.

11. WATCH DOG BLOCK

The watchdog timer gives means of returning to the reset state when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit timer L and an 8-bit timer H. At reset or writing to the watchdog timer control register WDTCON [7] (START), each watchdog timer H and L is set to 0FFh.

About Watchdog timer H count size selection, Bit 5 of the watchdog timer control register (SIZE) can be used to permit the selection of the watchdog timer H count source. When this bit is set to LOW, the count source becomes the underflow signal of watchdog timer L.

Table 11-1.Watch Dog Register Definition

Watch Dog Block(1)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00	WDTCON	START	INTTYPE	SIZE	Clock Prescale Number[4:0]				
01	WDTSTS	Reserved							+WDT

Gray: Only with System Reset (Pin Reset + WDT Reset) to Initial.

+: Only with Pin Reset to Initial

11.1 Register Description

11.1.1 Watch Dog Control Register (WDTCON) (Default Value: 0000_0000)

Reset with Power Reset & Pin Reset.

Bit 7: Start

1: Start / Reload

0: Stop

This bit enables/disables the watchdog timer. Writing LOW to this bit will stop the watchdog timer. Writing HIGH to this bit will reload the watchdog timer (watchdog timer H and L is set to 0FFh) even this bit is already HIGH. After written HIGH, the watchdog timer is running. Once this timer is timed-out, the chip is reset. Also the watchdog timer is stopped to prevent the next time-out.

Bit 6: Interrupt Type

1: NMI

0: Hardware reset

Bit 5: Size

Select the counter size. The counter starts from low to overflow, and then generates interrupt or hardware reset.

1: One Byte Counter. WDT Timeout Limit ≈ 256/Count Frequency .

0: Two Byte Counter. WDT Timeout Limit ≈ 65536/Count Frequency .

Bit 4~0: Clock Prescale Number

Count frequency is 1MHz / 4(Clock Prescale Number +1).

Watch Dog Status Register (WDTSTS) (Default Value: 0000_0000)

Reset with Power Reset.

Bit 7~1: Reserved

Bit 0: WDT Reset Finished

1: Finished, 0: Not Happened.

12. TIMER BLOCK

The Keyboard controller has four timers: timer X, timer Y, timer 1, and timer 2. The division ratio of each timer or pre-scalar is given by 1/n + 1, where n is the value in the corresponding timer or pre-scalar latch. All timers count down. When the timer reaches "00H", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer is underflow, the corresponding interrupt request bit is set to 1.

In Timer 1 and Timer 2, the count source of pre-scalar 1/2 is the oscillator frequency divided by 16. The output of pre-scalar 1/2 is counted for both timer 1 and 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y can work in one of the four operating modes by setting the timer XY mode register.

Table 12-1.Timer Register Definition

Timer Block(9)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10	PRE1	TM1ST	Prescale 1 [6:0]						
11	T1	Timer 1 [7:0]							
12	PRE2	TM2ST	Prescale 2 [6:0]						
13	T2	Timer 2 [7:0]							
18	TM	TMYST	CNTR1	TMYMODE		TMXST	CNTR0	TMXMODE	
19	PREX	Prescale X [7:0]							
1A	TX	Timer X[7:0]							
1B	PREY	Prescale Y [7:0]							
1C	TY	Timer Y [7:0]							

12.1 Register Description

12.1.1 Clock Prescale Number of Timer 1 (PRE1) (Default Value: 0111_1111)

Bit 7: Timer 1 Start Bit

Write: Start Timer 1 counter.

1: Enable (Prescale Counter Reload & Start, but Timer 1 Data Keep)

0: Disable

Read: Always Read ‘LOW’.

Bit 6~0: Clock Prescale Number

Write: Prescale Counter Reload.

Read: Current Prescale Counter Value

12.1.2 Timer 1 Register (T1) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer 1 Counter Reload.

Read: Current Timer 1 Counter Value

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in the first prescale period width.

12.1.3 Clock Prescale Number of Timer 2 (PRE2) (Default Value: 0111_1111)

Bit 7: Timer 2 Start Bit

1: Start (Prescale Counter Reload & Start, but Timer 2 Data Keep)

0: Stop

Bit 6~0: Clock Prescale Number

Write: Prescale Counter Reload.

12.1.4 Timer 2 Register (T2) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer 2 Reload.

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in the first prescale period width.

12.1.5 Timer X/Y Mode Register (TM) (Default Value: 0000_0000)

Bit 7: Timer Y Start Bit

Start internal Time Y counter and

1: Enable (Prescale Y & Timer Y Data Keep after Stop)

0: Disable

Bit 6: CNTR1 active edge selection bit

0: Interrupt at falling edge Count at the rising edge in the event counter mode.

1: Interrupt at rising edge Count at the falling edge in the event counter mode.

Bit 5-4: Timer Y operating bit

00: Timer mode

Timer Y can select the count by XIN/16.

01: Pulse output mode (Disable GP83 Function, Pin Direct Force "Output")

Timer Y counts XIN/16. Whenever the contents of the timer reach "00H", the signal output from the CNTR1 pin is inverted. If the CNTR1 active edge selection bit is 0, the pin is "H" after initializing. If it is 1, the pin is 'L' after initializing. When using a timer in this mode, set the corresponding direction register of port GP83 to output mode.

10: Event count mode (Disable GP83 Function, Pin Direct Force "Input")

Operating in the event counter mode is almost the same as in the timer mode, except that the timer counts signal inputs through CNTR1. When the CNTR1 active edge selection bit is 0, the rising edge on the CNTR1 pin is counted. When the CNTR1 active edge selection bit is 1, the falling edge on the CNTR1 pin is counted.

11: Pulse width measurement mode (Disable GP83 Function, Direct Force "Input")

If the CNTR1 active edge selection bit is 0, the timer counts XIN/16 while the CNTR1 pin is H. If the CNTR1 active edge selection bit is 1, the timer counts while the CNTR1 pin is 'L'.

Bit 3: Timer X Start Bit

1: Enable (Prescale X & Timer X Data Keep)

0: Disable

Bit 2: CNTR0 active edge selection bit

0: Interrupt at falling edge Count at rising edge in event counter mode.

1: Interrupt at rising edge Count at falling edge in event counter mode.

Bit 1-0: Timer X operating bit

00: Timer mode

The Timer X only counts XIN/16.

01: Pulse output mode (Disable GP82 Function, Direct Force "Output")

Timer X counts XIN/16. Whenever the contents of the timer reach "00H", the signal output from the CNTR0 pin is inverted. If the CNTR0 active edge selection bit is 0, the pin is "H"

after initial. If it is 1, the pin is 'L' after initial. When using a timer in this mode, set the corresponding direction register of port GP82 to output mode.

10: Event count mode (Disable GP82 Function, Direct Force "Input")

Operating in the event counter mode is almost the same as in the timer mode, except that the timer counts signal inputs through the CNTR0. When the CNTR0 active edge selection bit is 0, the rising edge on the CNTR0 pin is counted. When the CNTR0 active edge selection bit is 1, the falling edge on the CNTR0 pin is counted.

11: Pulse width measurement mode (Disable GP82 Function, Direct Force "Input")

If the CNTR0 active edge selection bit is 0, the timer counts XIN/16 while the CNTR0 pin is H. If the CNTR0 active edge selection bit is 1, the timer counts while the CNTR0 pin is 'L'.

Note: The count can be stopped by setting a "0" to the timer X (or timer Y) count start bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

12.1.6 Clock Prescale Number of Timer X (PREX) (Default Value: 1111_1111)

Bit 7~0: Clock Prescale Number

Write: Prescale Counter Reload.

Read: Current Prescale Counter Value

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in the first prescale period width.

12.1.7 Timer X Register (TX) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer X Reload.

Read: Current Timer X Counter Value

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in the first prescale period width.

12.1.8 Clock Prescale Number of Timer Y (PREY) (Default Value: 1111_1111)

Bit 7~0: Clock Prescale Number

Write: Prescale Counter Reload.

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in the first prescale period width.

Read: Current Prescale Counter Value

12.1.9 Timer Y Register (TY) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer Y Reload.

Read: Current Timer X Counter Value

13. PULSE WIDTH MODULATOR BLOCK

The W83L951ADG provides 4 Pulse Width Modulator Outputs.

The 16-bit PWM has four: PWM0, PWM1, PWM2 and PWM3. The minimum resolution can be selected by frequency select in PWM Control Register.

Table 13-1.Pulse Width Modulator Register Definition

Pulse Width Measurer Block(13)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1E	PWMCON0	Reserved	PWM1 Freq. Select			Reserved	PWM0 Freq. Select		
1F	PWMCON1	Reserved	PWM3 Freq. Select			Reserved	PWM2 Freq. Select		
20	PWM0PH	PWM 0 Period Register [15:8]							
21	PWM0PL	PWM 0 Period Register [7:0]							
22	PWM0HH	PWM 0 High Level Register [15:8]							
23	PWM0HL	PWM 0 High Level Register [7:0]							
24	PWM1PH	PWM 1 Period Register [15:8]							
25	PWM1PL	PWM 1 Period Register [7:0]							
26	PWM1HH	PWM 1 High Level Register [15:8]							
27	PWM1HL	PWM 1 High Level Register [7:0]							
28	PWM2PH	PWM 2 Period Register [15:8]							
29	PWM2PL	PWM 2 Period Register [7:0]							
2A	PWM2HH	PWM 2 High Level Register [15:8]							
2B	PWM2HL	PWM 2 High Level Register [7:0]							
2C	PWM3PH	PWM 3 Period Register [15:8]							
2D	PWM3PL	PWM 3 Period Register [7:0]							
2E	PWM3HH	PWM 3 High Level Register [15:8]							
2F	PWM3HL	PWM 3 High Level Register [7:0]							

Gray: Only with System Reset to initial.

Note:

1) If {PWM High Level Register} = 0, the output keeps at the low level.

2) If {PWM High Level Register} >= {PWM Period Register}, the output keeps at the high level.

3) PWM is {PWM Period Level Register} > {PWM High Level Register} >0, then

Period Width: {PWM Period Level Register} + 4units.

Low Width : {PWM Period Level Register} — {PWM High Level Register} + 1unit.

High Width : {PWM High Level Register} + 3units.

The unit is 1/F in PWM. F is defined in PWM Control Register.

4) All PWM is default low.

13.1 Register Description

13.1.1 PWM Control 0 Register (PWMCON0) (Default Value: 0000_0000)

Bit 7: Reserved

Bit 6~4: PWM 1 Frequency Select

111: Reserved, 110: 375 KHz, 101: 750 KHz, 100: 1.5 MHz.

011: 3 MHz, 010: 6 MHz, 001: 12 MHz, 000: 24 MHz.

Bit 3: Reserved

Bit 2~0: PWM 0 Frequency Select

111: Reserved, 110: 375 KHz, 101: 750 KHz, 100: 1.5 MHz.

011: 3 MHz, 010: 6 MHz, 001: 12 MHz, 000: 24 MHz.

13.1.2 PWM Control 1 Register (PWMCON1) (Default Value: 0000_0000)

Bit 7: Reserved

Bit 6~4: PWM 3 Frequency Select

111: Reserved, 110: 375 KHz, 101: 750 KHz, 100: 1.5 MHz.

011: 3 MHz, 010: 6 MHz, 001: 12 MHz, 000: 24 MHz.

Bit 3: Reserved

Bit 2~0: PWM 2 Frequency Select

111: Reserved, 110: 375 KHz, 101: 750 KHz, 100: 1.5 MHz.

011: 3 MHz, 010: 6 MHz, 001: 12 MHz, 000: 24 MHz.

13.1.3 PWM 0 Period Register (PWM0PH, PWM0PL) (Default Value: 0000h)

Use the 16-bit register to control the width of a full period output.

13.1.4 PWM 1 Period Register (PWM1PH, PWM1PL) (Default Value: 0000h)

Use the 16-bit register to control the width of a full period output.

13.1.5 PWM 2 Period Register (PWM2PH, PWM2PL) (Default Value: 0000h)

Use the 16-bit register to control the width of a full period output.

13.1.6 PWM 3 Period Register (PWM3PH, PWM3PL) (Default Value: 0000h)

Use the 16-bit register to control the width of a full period output.

13.1.7 PWM 0 High Level Register (PWM0HH, PWM0HL) (Default Value: 0000_0000)

(PWM0HH, PWM0HL) is defined as high signal width for PWM0 output. It is a 16-bit register.

13.1.8 PWM 1 High Level Register (PWM1HH, PWM1HL) (Default Value: 0000_0000)

(PWM1HH, PWM1HL) is defined as high signal width for PWM1 output. It is a 16-bit register.

13.1.9 PWM 2 High Level Register (PWM2HH, PWM2HL) (Default Value: 0000_0000)

(PWM2HH, PWM2HL) is defined as high signal width for PWM2 output. It is a 16-bit register.

13.1.10 PWM 3 High Level Register (PWM3HH, PWM3HL) (Default Value: 0000_0000)

(PWM3HH, PWM3HL) is defined as high signal width for PWM3 output. It is a 16-bit register.

14. UART BLOCK

The W83L951ADG supports one Universal asynchronous serial I/O mode (UART). Eight serial data transfer formats can be selected, for various selection of Stop bit, Parity, Parity check, and Data length. The transfer formats used by a transmitter and receiver must be identical.

The transmitter and receiver shift registers have their individual buffer, but the two buffers have the same address in memory. Since the shift register cannot be written or read directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register. The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a byte while the next byte is being received.

Table 14-1.UART Register Definition

UART Block(5)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
30	UARTCON	TxEn	TS	RxEn	PARE	PARS	STPS	CHAS	Reserved
31	UARTSTS	ParErr	FrameErr	OverErr	Reserved			RxBFull	TxBFull
32	BRGH	Baud Rate Generator High Byte[7:0]							
33	BRGL	Baud Rate Generator Low Byte[7:0]							
34	UARTBUF	UART Transmit / Receive Buffer[7:0]							

Gray: Only with System Reset to initial.

14.1 Register Description

14.1.1 UART Control Register (UARTCON) (Default Value: 0000_0000)

Bit 7: Transmit enable bit (TE)

0: Transmit disabled. 1: Transmit enabled.

Bit 6: Transmit Speed up bit (TS) (Reserved)

0: Disable.

1: Enable.

Bit 5: Receive enable bit (RE)

0: Receive disable. 1: Receive enable.

Bit 4: Parity enable bit (PARE).

0: Parity Bit disable. 1: Parity Bit enable.

Bit 3: Parity selection bit (PARS).

0: Odd parity. 1: Even parity.

Bit 2: Stop bit length selection bit (STPS)

0: 1 stop bit. 1: 2 stop bits.

Bit 1: Character length selection bit (CHAS) .

0: 8 bits 1: 7 bits.

Bit 0: User Define Register

14.1.2 UART Status Register (UARTSTS) (Default Value: 0000_0000)

Bit 7: Parity Error Status for Packet at Receive Buffer (PE)

Read: 0 - No error, 1 - Parity error

Bit 6: Framing Error Status for Packet at Receive Buffer (FE)

Read: 0 - No error, 1 - Framing error

Bit 5: Overrun Error Interrupt (OE)

For UART Rx Interrupt, users need to write this bit to clear.

Read:

0 - No error

1 - Overrun error

Write:

0 - No Change

1 - Clear

Bit 4~2: Not used (return 'L' when read)

Bit 1: Receive Buffer Full Status Flag (RBF)

Receive Buffer Full generates the interrupt. Read buffer can clear the flag.

0: Buffer empty

1: Buffer full

Bit 0: Transmit Buffer Full Status Flag (TBF)

Transmit Buffer Empty generates the interrupt. Write buffer can clear the flag. And next byte is allowed to write into the buffer.

0: Buffer empty

1: Buffer full

14.1.3 Baud Rate Generator High/Low Byte Register (BRGH/BRGL) (Default Value: 0000_0000_0000_0000)

Baud Rate Period Width = 2(N+1) / 3MHz.

And N = {BRGH, BRGL}

14.1.4 UART Transmit / Receive Buffer (UARTBUF) (Default Value: 0000_0000)

Read: Receive Buffer

Write: Transmit Buffer

15. CONSUMER INFRARED COMMUNICATIONS RECEIVER BLOCK

The CIrCC implements hardware-level decoding for the NEC Consumer IR Remote Control format. The hardware decoder may be used to generate a wake-up event or to send parts of the received message frame to the FIFO. The No Care Custom Code (NCCC), No Care Data Code (NCDC), PME Wake and Frame bits of the Consumer IR Control register configure the hardware decoder.

About NEC Consumer IR Format, the NEC Consumer IR Remote Control format specifies a 38 kHz carrier, 13ms of sync framing, and 32 bits of pulse-position modulated (PPM) message data. The message data includes an 8 bit Custom Code field, an 8 bit Custom Code' field, an 8 bit Data Code field, and an 8 bit Data Code' field. A single frame of the NEC PPM Consumer Remote Control signal is shown in Figure 14-1.

The Custom Code fields in this protocol uniquely address message frames for specific devices. The Custom Code fields can be used as a 16 bit address or as an 8 bit address followed by the bit-wise complement of the Custom Code field Custom Code. The Data Code field is an 8 bit command code, Data Code' is the bit-wise complement of Data Code.

Note: The CIrCC hardware can decode NEC protocol framing (sync pulse, 32 bit PPM message data) at any data rate, depending on the programmed Bit Rate Divider (BRD).

Table 15-1.Consumer Infrared Communications Receiver Register Definition

CIR Block(3)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
40	CIRCON	DFE	SFE	REP	FINISH	DM	SM	RM	RXINV
41	CIRBRD	Baud Rate Divider[7:0]							
42	CIRDATA0	CIR Receive Data 0[7:0]							
43	CIRDATA1	CIR Receive Data 1[7:0]							
44	CIRDATA2	CIR Receive Data 2[7:0]							
45	CIRDATA3	CIR Receive Data 3[7:0]							

Gray: Only with System Reset to initial.

15.1 Register Description

15.1.1 CIR Configure Register (CIRCON) (Default Value: 0000_0000)

Bit 7: Data Frame Error Status Flag (Write 'HIGH' to Clear)

When Data Frame Error flag occurs, CIR Interrupt is generated. Writes to the bit can clear Data Frame Error Flag.

Read:

0 - No error

1 - Data frame Error

Write:

0 - No Change

1 - Clear

Bit 6: Start Frame Error Status Flag (Write 'HIGH' to Clear)

When Start Frame Error flag occurs, CIR Interrupt is generated. Writes to the bit can clear Start Frame Error Flag.

Read:

0 - No error

1 – Start Frame Error

Write:

0 - No Change

1 - Clear

Bit 5: Repeat Status Flag (Write 'HIGH' to Clear)

When Repeat Flag occurs, CIR Interrupt is generated. Writes to the bit can clear Repeat Flag.

Read:

0 - Nothing happened

1 – Repeat Packet Received.

Write:

0 - No Change

1 - Clear

Bit 4: Finish Status Flag (Write 'HIGH' to Clear)

When Finish Flag occurs, CIR Interrupt is generated. Writes to the bit can clear Finish Flag.

Read:

0 - Nothing happened

1 – Packet Received is finish.

Write:

0 - No Change

1 - Clear

Bit 3: Data Frame Error Interrupt Mask Enable

0 – Enable.

1 – Disable.

Bit 2: Start Frame Error Interrupt Mask Enable

0 – Enable.

1 – Disable.

Bit 1: Repeat Interrupt Mask Enable

0 – Enable.

1 – Disable.

Bit 0: Rx Signal Invert Enable

Enable CIR Rx signal Convert Function

0 – Enable.

1 – Disable.

15.1.2 Baud Rate Divider (CIRBRD) (Default Value: 0101_0101)

The Transmit and Receive Bit Rate Divider register is used to extract a serial NRZ data stream for the CIrCC SCE. The divider is eight bits wide. The input clock to the Bit Rate Divider is 50 KHz (Carrier Frequency Divider input clock 16). The relationship between the Bit Rate Divider (BRD) and the Bit Rate (Fb) is as follows:

BRD = (.05MHz/Fb) – 1

For example, program the Bit Rate Divider with 55 ('37'Hex) for a .562ms Remote Control bit cell the same way as for the NEC remote control frame format: Fb = 0.893 KHz. This is ~.5% accuracy. Table 9 contains representative BRD vs. BitRate relationships. The Bit Rate range is 50 KHz to 190Hz.

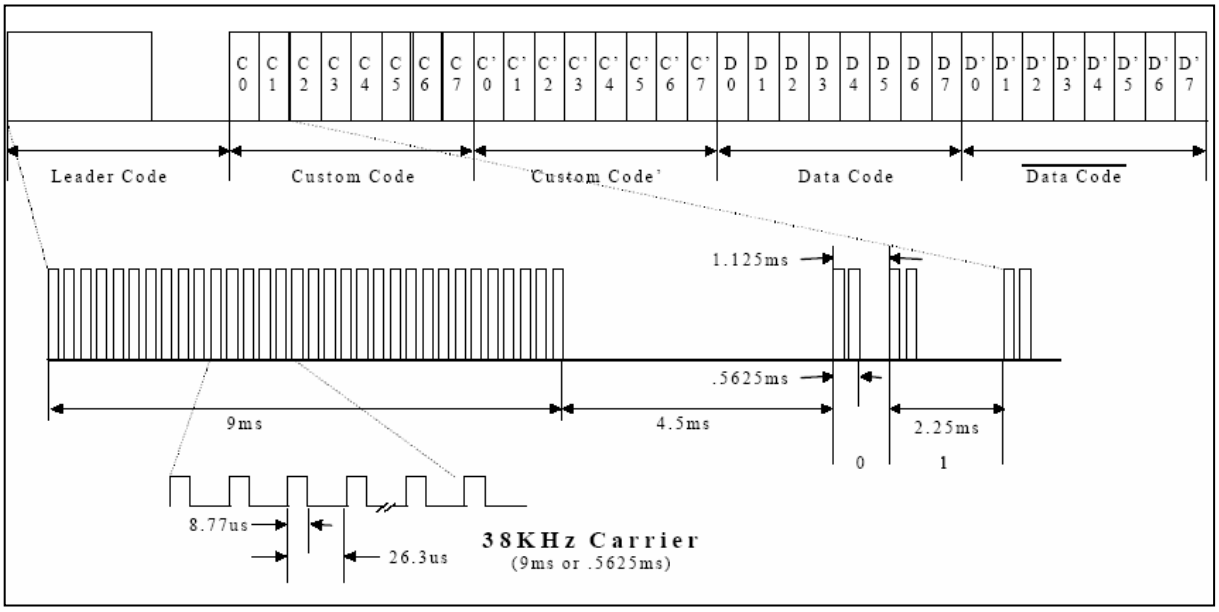


Figure 15-1.NEC CIR Frame Format

Table 15-2.Bit Rate Divider (BRD) V.S Bit Rate (Fb)

BRD	Fb (kHz)	BRD	Fb (kHz)	BRD	Fb (kHz)	BRD	Fb (kHz)
003	12.5	067	0.7355	131	0.379	195	0.255
007	6.25	071	0.6945	135	0.3675	199	0.25
011	4.1665	075	0.658	139	0.357	203	0.245
015	3.125	079	0.625	143	0.347	207	0.2405
019	2.5	083	0.595	147	0.338	211	0.236
023	2.0835	087	0.568	151	0.329	215	0.2315
027	1.7855	091	0.5435	155	0.3205	219	0.2275
031	1.5625	095	0.521	159	0.3125	223	0.223
035	1.389	099	0.5	163	0.305	227	0.2195
039	1.25	103	0.481	167	0.2975	231	0.2155
043	1.1365	107	0.463	171	0.2905	235	0.212
047	1.0415	111	0.4465	175	0.284	239	0.2085
051	0.9615	115	0.431	179	0.278	243	0.205
055	0.893	119	0.4165	183	0.2715	247	0.2015
059	0.8335	123	0.403	187	0.266	251	0.1985
063	0.78125	127	0.781	191	0.521	255	0.19

15.1.3 CIR Receive Data 0(CIRDATA0) (Default Value: 0000_0000)

Read: CIR 1st Received Data Buffer

15.1.4 CIR Receive Data 1 (CIRDATA1) (Default Value: 0000_0000)

Read: CIR 2nd Received Data Buffer

15.1.5 CIR Receive Data 2(CIRDATA2) (Default Value: 0000_0000)

Read: CIR 3rd Received Data Buffer

15.1.6 CIR Receive Data 3(CIRDATA3) (Default Value: 0000_0000)

Read: CIR 4th Received Data Buffer

16. A/D CONVERTER BLOCK

The W83L951ADG provides 8 A/D inputs. The analog input pin is selected in A/D Converter Register 0. The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read. ADC sampling frequency will be changed with different input system clock. On 24MHz, the sampling frequency is 24.4375KHz (800us); on 16MHz is 15.625KHz (1.2ms); on 12MHz is 12.21875KHz (1.6ms), and on 8MHz is 7.8125KHz (2.4ms).

Table 16-1.A/D Convert Register Definition

A/D Convert Block(4)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
50	ADCCON	ADCST	Analog Input Select			ADCC	Reserved	Analog [1:0]	
51	ADCDATA	Analog [9:2]							
54	ADCPWDN	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Gray: Only with System Reset to initial.

16.1 Register Description

A/D converter is 10-bit converter. The V_{REF} is Input of VREF pin.

The formula: A/D converter result= (Analog [9:0] / 1024) × V_{REF}

16.1.1 A/D Control Register (ADCCON) (Default Value: 0000_00??)

Bit 7: ADC Start Bit

1: Start (Only one time)

0: No change.

When A/D Conversion Complete Status Bit is high, write 1 to this bit to start A/D convert. ADC Start Bit keeps low until the hardware receives this request and can receive next request. ADC Start Bit changes from low to high at the same time.

Bit 6~4: Analog Input Pin Select

000: GP60, 001: GP61, 010: GP62, 011: GP63,

100: GP64, 101: GP65, 110: GP66, 111: GP67.

Bit 3: A/D Conversion Complete Status Bit (Read Only)

0: Conversion in progress.

1: Conversion completed.

Bit 2: Reserved

Bit 1~0: A/D Converter Result [1:0]

A/D converter result bit1 is LSB.

When A/D Conversion Complete Status Bit is high, A/D Converter Result is valid.

16.1.2 A/D Data Register (ADCDATA) (Default Value: ????_????)

Bit 7~0: A/D Converter Result [9:2]

A/D Converter Result bit 9 is MSB.

When A/D Conversion Complete Status Bit is high, A/D Converter Result is valid.

16.1.3 ADC Powerdown Register (ADCPWDN) (Default Value: 0000_0000)

Bit 7~0: Pad mode select

0: Normal Mode

1: AD Mode (GPIO Function always is “Input”)

17. D/A CONVERTER BLOCK

The keyboard controller has two internal D-A converters with 8-bit resolution. The result of D-A conversion is output to the DA1 or DA2 pin.

Table 17-1.D/A Converter Register Definition

D/A Convert Block(4)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
52	DA1	D/A 1 Convert Register [7:0]							
53	DA2	D/A 2 Convert Register [7:0]							

Gray: Only with System Reset to initial.

17.1 Register Description

17.1.1 D-A conversion register 0(DA1) (Default Value: 0000_0000)

$$V_{GP57} = V_{REF} \times (N/256)$$

VREF is the reference voltage.

17.1.2 D-A conversion register 1(DA2) (Default Value: 0000_0000)

$$V_{GP56} = V_{REF} \times (N/256)$$

VREF is the reference voltage.

18. FAN TACHOMETER BLOCK

Fan Tachometer Block provides two groups of Fan Tachometer. GP40, GP41 inputs the wave form to the W83L951ADG and the corresponding Count of cycle of rotational speed is counted automatically. When real RPM is lower than the set value, the interrupt request will occur.

Table 18-1.Fan Tachometer Register Definition

FAN Block(2)									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
60	FAN0	Fan 0 Count[7:0]							
61	FAN1	Fan 1 Count[7:0]							

Gray: Only with System Reset to initial.

18.1 Register Description

18.1.1 FAN 0/1 Count/Limit Register (FAN0/1) (Default Value: ????_????)

Read:

Current Count. RPM = (60 × 1 × 10e6) / (2 × Count × 256) = 117187.5 /Count.

Write:

Set Count of tolerance of minimum RPM. When real RPM is lower than the set value, the interrupt request will occur. The relation between RPM and Count is as follows:

RPM = (60 × 1 × 10e6) / (2 × Count × 256) = 117187.5 / Count.

Count = 117187.5/RPM.

19. RC BLOCK

Table 19-1.RC5 Register Definition

RC Block

ExtAddr	Name	7	6	5	4	3	2	1	0
46	RCDAT	Received Data							
47	RCCON	RAWEN	FIFOCLR	Trigger Level		R	R	FSTART	MODE
48	RCSTS	DR	TR	FU	FO	Overrun	Full	FrameEnd	Fail
49	RCBL	Expect Bit length(W) / Received Bit Count(R)							
4A	RCWH	RC Sample Width High Byte(setup before CHIPCTRL enable bit turn on)							
4B	RCWL	RC Sample Width Low Byte							
4C	RAWLCH	RAW Limit Count High Byte(Total 15 Bit, base unit is 128)							
4D	FIFOSTS	R	FTA	Empty	Full	FIFO Count			
4E	RAWFIFOH	Raw FIFO Data High Byte							
4F	RAWFIFOL	Raw FIFO Data Low Byte							

Gray: Only with System Reset to initial.

Gray: Only for RAW Mode.

19.1 Register Configuration

19.1.1 RC Data Register [RCDAT]

Bit7~0: Received Data

19.1.2 RC Control Register [RCCON]

Bit7: Raw Mode Enable

Bit6: RAW FIFO Clear

Bit5~4: RAW FIFO Trigger Level

00: 1, 01: 4, 10: 6, 11: 8.

Bit3: Reserved

Bit2: Rx Invert

Bit1: Start Receive RC Frame

Bit0: RC Mode

0:RC5, 1: RC6

19.1.3 RC Status & Interrupt Enable Register [RCSTS/RCIE]

As the Status Register for reading and as the Interrupt Enable Register for writing.

Bit7: RAW Data Ready

Bit6: RAW FIFO Trigger Level Reach

Bit5: RAW FIFO Underrun

Bit4: RAW FIFO Overrun (occur concurrently Overrun and Data Ready)

Bit3: RC Data Register Overrun

Bit2: RC Data Register Full

Bit1: End of Frame

Bit0: Receive Fail

19.1.4 RC Bit Length [RCBL]

Expected bit length of current receiving frame.

19.1.5 RAW Limit Count High-byte Register [RAWLCH]

(RAWLCH, RAWLCL) is defined as the count limit in the raw mode while RAWLCL is an internal register. It is a 16-bit register.

19.1.6 RC Sample Width High/Low Byte Register [RCWH] [RCWL]

Baud Rate Period Width = (N+1) / 24MHz.

And N = {RCWH, RCWL}

19.1.7 RAW FIFO Data Register [RAWFIFOH] [RAWFIFOL]

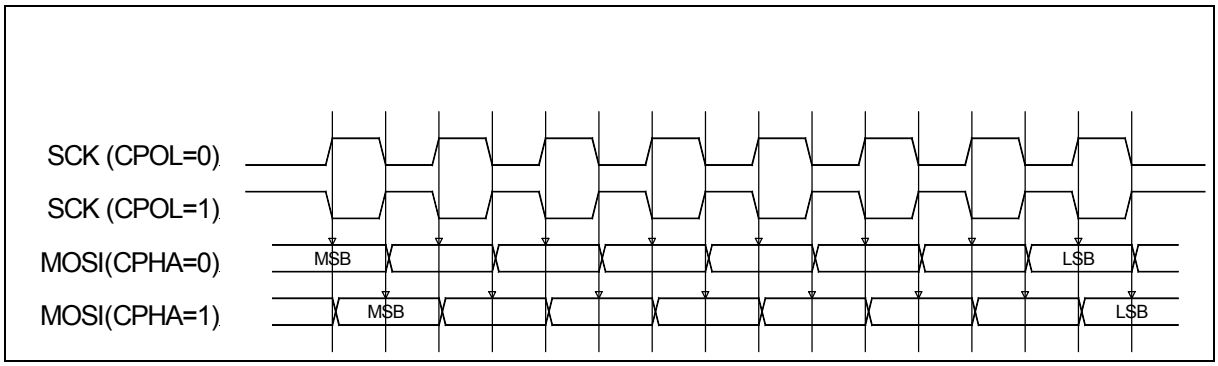
In the raw mode, there is an eight-element FIFO with 16-bit size for each element to store the IR data. (RAWFIFOH, RAWFIFOL) is used to read from the head of the FIFO.

20. SIMPLE PERIPHERAL INTERFACE

20.1 SPI Transfers

During an SPI transfer, the data are simultaneously transmitted and received. The serial clock line [SCK] synchronizes shifting and sampling of the information on the two serial data lines. The master places the information onto the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.

Four possible timing relationships can be chosen by using the Clock Polarity [CPOL] and Clock Phase [CPHA] bits in the Serial Peripheral Control Register [SPCR]. Both the master and the slave devices must operate with the same timing.



20.2 Initiating transfers

20.2.1 Transmitting data bytes

After programming the core's control register, SPI transfers can be initiated. A transfer is initiated by writing to the Serial Peripheral Data Register [SPDR]. Writing to the Serial Peripheral Data Register is actually writing to a 4-entry deep FIFO called Write Buffer. Each write access adds a data byte to the Write Buffer. When the core is enabled – SPE is set ('1') – and the Write Buffer is not empty, the core automatically transfers the oldest data byte.

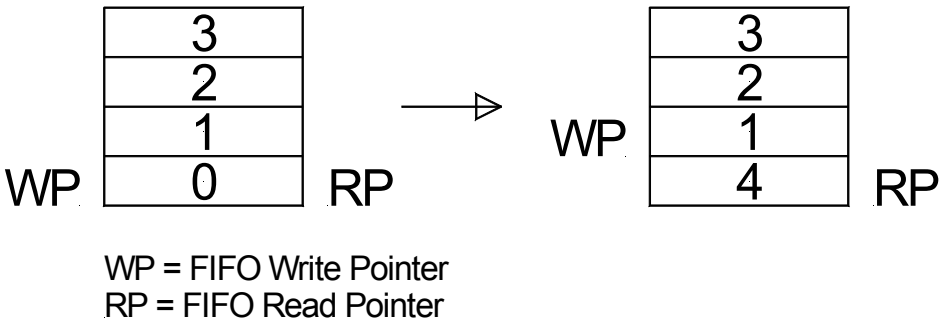
20.2.2 Receiving data bytes

Receiving data is done simultaneously with transmitting data; whenever a data byte is transmitted, a data byte is received. For each byte that needs to be read from a device, a dummy byte needs to be written to the Write Buffer. This instructs the core to initiate an SPI transfer, simultaneously transmitting the dummy byte and receiving the desired data. Whenever a transfer is finished, the received data byte is added to the Read Buffer. The Read Buffer is the counterpart of the Write Buffer. It is an independent 4-entry deep FIFO. The FIFO contents can be read from the Serial Peripheral Data Register [SPDR].

20.2.3 FIFO Overrun

Both Write Buffer and Read Buffer are FIFOs that use circular memories to simulate the infinite big memory needed for FIFOs. Thus, writing to a FIFO while it is full will overwrite the oldest data byte. Writing to Serial Peripheral Data Register [SPDR] while the Write Buffer if full will set the WCOL bit to '1'. The next byte to be transferred is not the oldest data byte, but the latest (newest) one.

The only way to recover from this situation is to reset Write Buffer. Both Read Buffer and



Write Buffer are reset when the Serial Peripheral Enable [SPE] bit is cleared ('0').

Read Buffer overruns might be less destructive, especially when the SPI bus is used to transmit data only; e.g. when sending data to a DAC. The received data is simply ignored. The fact that the Read Buffer overruns is irrelevant. If the SPI bus is used to transmit and receive data, it is important to keep Read Buffer aligned. The easiest way to do this is to perform a number of dummy reads equal to the amount of bytes transmitted modulo 4.

$$Ndummy\_reads = Ntransmitted\_bytes \bmod 4$$

Note that a maximum sequence of 4 bytes can be stored in Read Buffer before the oldest data byte is overwritten. It is therefore necessary to empty (read) Read Buffer every 4 received bytes.

Table 20-1.Simple Peripheral Interface Register Definition

CIR Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
38	SPCON	SPIE	SPE	R	MSTR	CPOL	CPHA	SPR	
39	SPSTS	SPIF	WCOL	R	R	WFFULL	WFEMPTY	RFFULL	RFEMPTY
3A	SPDAT	Write Buffer / Read Buffer							
3B	SPER	ICNT		R	R	R	R	ESPR	

20.2.4 Serial Peripheral Control Register [SPCON]

BIT #	ACCESS	DESCRIPTION
7	R/W	SPIE
6	R/W	SPE
5	R/W	*Reserved*
4	R/W	MSTR
3	R/W	CPOL
2	R/W	CPHA
1:0	R/W	SPR

Reset Value: 0x10

SPIE – Serial Peripheral Interrupt Enable

When Serial Peripheral Interrupt Enable is set (‘1’) and Serial Peripheral Interrupt Flag in the status register is set, the host is interrupted. Setting this bit while the SPIF flag is set generates an interrupt.

‘0’ = SPI interrupts disabled

‘1’ = SPI interrupts enabled

SPE – Serial Peripheral Enable

When the Serial Peripheral Enable bit is set (‘1’), the core is enabled. When it is cleared (‘0’), the core is disabled. The core only transfers data when the core is enabled.

‘0’ = SPI core disabled

‘1’ = SPI core enabled

MSTR – Master Mode Select

When the Master Mode Select bit is set (‘1’), the core is a master device. When it is cleared (‘0’), it is a slave device. Currently only master mode is supported. This bit is set, and can not be cleared.

‘0’ = Slave mode

‘1’ = Master mode

CPOL – Clock Polarity

The Clock Polarity bit, together with the Clock Phase bit, determines the transfer mode. Refer to the *SPI Transfers* section for more information

CPHA – Clock Phase

The Clock Phase bit, together with the Clock Polarity bit, determines the transfer mode. Refer to the *SPI Transfers* section for more information.

SPR – SPI Clock Rate Select

These bits select the SPI clock [sck_o] rate. Refer to the ESPR bits in Extension Register for more information.

20.2.5 Serial Peripheral Status Register [SPSTS]

BIT #	ACCESS	DESCRIPTION
7	R/W	SPIF
6	R/W	WCOL
5:4	R	*Reserved*
3	R	WFFULL
2	R	WFEMPTY
1	R	RFFULL
0	R	RFEMPTY

Reset Value: 0x05

SPIF – Serial Peripheral Interrupt Flag

The Serial Peripheral Interrupt Flag is set upon completion of a transfer block. If SPIF is asserted (‘1’) and SPIE is set, an interrupt is generated. To clear the interrupt, write the status register with the SPIF bit set (‘1’).

WCOL – Write Collision

The Write Collision flag is set when the Serial Peripheral Data register is written, while the Write FIFO is full. To clear the Write Collision flag, write the status register with the WCOL bit set (‘1’).

WFFULL – Write FIFO Full

The Write FIFO Full and Write FIFO empty bits show the status of the write FIFO.

WFEMPTY – Write FIFO Empty

The Write FIFO Full and Write FIFO empty bits show the status of the write FIFO.

RFFULL – Read FIFO Full

The Read FIFO Full and Read FIFO empty bits show the status of the read FIFO.

RFEMPTY – Read FIFO Empty

The Read FIFO Full and Read FIFO empty bits show the status of the read FIFO.

20.2.6 Serial Peripheral Data Register [SPDAT]

BIT #	ACCESS	DESCRIPTION
7:0	W	Write Buffer
7:0	R	Read Buffer

Reset Value: undefined

Write Buffer

The Write Buffer is a 4-entry deep FIFO. Writing to Write Buffer adds the data to the FIFO. Writing to Write Buffer while the FIFO is full sets the Write Collision [WCOL] bit. When the Serial Peripheral Enable [SPE] bit is cleared (‘0’), Write Buffer is reset. When the [SPE] bit is set (‘1’) and the write buffer is not empty, the core initiates SPI transfers. When the transfer is initiated, the data byte is removed from the FIFO.

Read Buffer

The Read Buffer is a 4-entry deep FIFO. When the Serial Peripheral Enable [SPE] bit is cleared (‘0’), Read Buffer is reset. When an SPI transfer is finished, the received data byte is added to Read Buffer. There is no overrun detection; it is possible to overwrite the oldest data. This is done to maintain the highest level of compatibility with the M68HC11 type SPI port, and to minimize overhead for systems where the SPI bus is used to transfer data only (e.g. when accessing a DAC).

20.2.7 Serial Peripheral Extensions Register [SPER]

BIT #	ACCESS	DESCRIPTION
7:6	R/W	ICNT
5:2	R/W	*Reserved*
1:0	R/W	ESPR

Reset Value: 0x00

ICNT – Interrupt Count

The Interrupt Count bits determine the transfer block size. The SPIF bit is set after ICNT transfers. Thus it is possible to reduce kernel overhead due to reduced interrupt service calls.

ICNT	Description
00	SPIF is set after every completed transfer
01	SPIF is set after every two completed transfers
10	SPIF is set after every three completed transfers
11	SPIF is set after every four completed transfers

ESPR – Extended SPI Clock Rate Select

The Extended SPI Clock Rate Select registers are decided by ESPR and SPR. ESPR and SPR each has two registers. Thus, there will be 4 register combinations in total. When ESPR = '00' the original M68HC11 coding is used.

ESPR	SPR	Divide 24MHz clock by
00	00	2
00	01	4
00	10	16
00	11	32
01	00	8
01	01	64
01	10	128
01	11	256
10	00	512
10	01	1024
10	10	2048
10	11	4096
11	xx	*Reserved*

21. SFI BLOCK

Table 21-1.IrDA Register Definition

SFI Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
8	SFICON	SFIEN	BIOSRANGE		DIS_E0000	DIS_FFE0000	BIOSWEN	BIOSEN	DIS_F0000
9	SFIFWH	R				IDSEL			
0A	SFIADDH	SFI Configuration Address [15:8]							
0B	SFIADDL	SFI Configuration Address [7:0]							

21.1 Register Configuration

21.1.1 SFI Configuration Register [SFICON]

Bit 6~5: BIOS Range

00: 1M, 01: 2M, 10: 4M, 11: 8M

Bit 4: Disable Address E0000 ~ EFFFF Decode

Bit 3: Disable Address FFE0000~FFEFFFF Decode

Bit 2: BIOS Write Enable

Bit 1: BIOS Enable

Bit0: Disable Address F0000 ~ FFFFF Decode

21.1.2 SFI FWH Register [SFIFWH]

Bit 7~4: Reserved

Bit 3~0: IDSEL

21.1.3 SFI Configuration Address High Byte Register [SFIADDH] (Default Value: 0000_0000)

Bit 7~0: SFI Configuration Address [15:8]

21.1.4 SFI Configuration Address Low Byte Register [SFIADDL] (Default Value: 0100_1110)

Bit 7~0: SFI Configuration Address [7:0]

21.2 LPC Configuration

21.2.1 Overview

The Configuration is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. SFI is designed for motherboard designs in which the resources required by their components are known. With its flexible resource allocation architecture, SFI allows the BIOS to assign resources at POST.

21.2.2 Configuration Register Access

Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

The desired configuration registers are accessed in two steps:

a. Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT

b. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note: If accessing the Global Configuration Registers, step (a) is not required.

21.2.3 Primary Configuration Address Decode (Reserved)

The logical devices are configured through three Configuration Access Ports (CONFIG, INDEX and DATA). The Port Address can be modified by KBC Firmware.

PORT NAME	PORT ADDRESS	TYPE
Config Port	0x04E	Write
Index Port	0x04E	Read/Write
Data Port	0x04F	Read/Write

Entering the Configuration State

The INDEX and DATA ports are effective only when the chip is in the Configuration State. The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = < 0x26>

Config Key = < 0x26>

Exiting the Configuration State

The device exits in the Configuration State when the following Config Key is successfully written to the CONFIG PORT address.

Config Key = < 0xAA>

Read Accessing Configuration Port

The Configuration Port reads back a float condition when not in the Configuration State. The Configuration Port reads back 0x00, after the Configuration Key 0x55 has been written to the Configuration Port, but prior to any further writes to the Configuration Port. After the Configuration Index Register has been written at least once (in the Configuration State,) the last value written to the Configuration Index Register (via the Configuration Port) can be read back.

21.2.4 Configuration Sequence Example

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode
2. Configure the Configuration Registers
3. Exit Configuration Mode. The following is an example of a configuration program in Intel 8086 assembly language.

21.2.5 Chip Level Control/Configuration Register

REGISTER	ADDRESS	DESCRIPTION
Logical Device #	0X07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: The Activate command operates only on the selected logical device.

21.2.6 Configuration Register Map

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER NAME
Global Configuration register				
0x07	R/W	0x00	0x00	Logical Device Name
0x20	R	0x8D	0x8D	Device ID
0x21	R	0x00	0x6E	Device Rev
0x22	R/W	0x00	0x00	BIOS Configuration
0x26	R/W	0x00	0x00	Reserved
Logic Device 1 Configuration Register(SFI)				
0x60,0x61	R/W	0x00	0x00	SFI Base I/O Address

REGISTER	ADDRESS	DESCRIPTION
BIOS Configuration	0x20	Bit 7: 0: use KBC SFICON Register 1: use BIOS Configuration Register Bit 6~5: BIOS Range 00: 1M, 01: 2M, 10: 4M, 11: 8M Bit 4: Disable Address E0000 ~ EFFFF Decode Bit 3: Disable Address FFE0000~FFEFFFF Decode Bit 2: BIOS Write Enable Bit 1: BIOS Enable Bit0: Disable Address F0000 ~ FFFFF Decode

21.2.7 Logical Device 1 Configuration/Control Register

REGISTER	ADDRESS	DESCRIPTION
IO Base Address	0x61 - 0x6F(R/W) 0x60=A[15:8], 0x61= A[7:0]	SFI Control Register Base Mapping Address.

Address Offset

0	COMMAND	
1*	**MODE**	ADDRESS2
2	ADDRESS1	
3	ADDRESS0	
4	DATA0	
5	DATA1	
6	DATA2	
7	DATA3	

Notice: **Address Offset 1 is High Nibble for *Mode* and Low Nibble for *Address2* keep last byte write.**

Mode

1. （WRITE）	COMMAND
2. （WRITE）	COMMAND-DATA1
3. （READ）	COMMAND-DATA2
4. （WRITE）	COMMAND-ADDRESS3
5. （WRITE）	COMMAND-ADDRESS3-DATA1
6. （WRITE）	COMMAND-ADDRESS3-DATA4
7. （READ）	COMMAND-ADDRESS3-DATA4
8. （READ）	COMMAND-ADDRESS3-DATA1
9. （READ）	COMMAND-ADDRESS3-DATA2
10. （READ）	COMMAND-ADDRESS3-DATA3
11. （READ）	COMMAND-ADDRESS3-DATA4

22. REAL TIME CLOCK GENERATOR BLOCK

Based on 32.768KHz, Real Time Clock Generator Block finishes counts which include seconds, minutes, and hours automatically. It also provides the alarm function.

When {RTCHR, RTCMIN, RTCSEC} and {RTCHRAL, RTCMINAL, RTCSECAL} are equal, an interrupt will occur to Microprocessor automatically.

Table 22-1.Real Time Clock Generator Register Definition

Real Time Clock Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
70	RTCSEC	RTC Seconds Register[7:0]							
71	RTCSECAL	RTC Seconds Alarm Register[7:0]							
72	RTCMIN	RTC Minutes Register[7:0]							
73	RTCMINAL	RTC Minutes Alarm Register[7:0]							
74	RTCHR	RTC Hours Register[7:0]							
75	RTCHRAL	RTC Hours Alarm Register[7:0]							

Note:

Gray: Only with System Reset to initial.

RTCSEC, RTCMIN, RTCHR should initial after local reset.

22.1 Register Description

22.1.1 RTC Second Register (RTCSEC) (Default Value: 0000_0000)

Read: Indicate RTC second value at present.

Write: Set RTC second value at present.

22.1.2 RTC Second Alarm Register (RTCSECAL) (Default Value: 0000_0000)

Read: Indicate RTC second alarm at present.

Write: Set RTC second alarm value at present.

22.1.3 RTC Minute Register (RTCMIN) (Default Value: 0000_0000)

Read: Indicate RTC minute value at present.

Write: Set RTC minute value at present.

22.1.4 RTC Minute Alarm Register (RTCMINAL) (Default Value: 0000_0000)

Read: Indicate RTC minute alarm value at present.

Write: Set RTC minute alarm value at present.

22.1.5 RTC Hour Register (RTCHR) (Default Value: 0000_0000)

Read: Indicate RTC hour value at present.

Write: Set RTC hour value at present.

22.1.6 RTC Hour Alarm Register (RTCHRAL) (Default Value: 0000_0000)

Read: Indicate RTC hour alarm minute value at present.

Write: Set RTC hour alarm value at present.

23. EXTERNAL INTERRUPT CONTROL BLOCK

External Interrupt, External Interrupt Group 1 (EXTINT1[7:0]), External Interrupt Group 2 (EXTINT2[7:0]) and External Interrupt Group 3 (EXTINT3[7:0]) interrupt source pins are the same as GPA[7:0], GPB[7:0] and GPC[7:0].

Table 23-1.External Interrupt Control Register Definition

Interrupt Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
80	EIE1	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10
81	EIE2	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
82	EIE3	INT37	INT36	INT35	INT34	INT33	INT32	INT31	INT30
83	EIREQ1	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10
84	EIREQ2	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
85	EIREQ3	INT37	INT36	INT35	INT34	INT33	INT32	INT31	INT30
88	EINTT1	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10
89	EINTT2	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
8A	EINTT3	INT33		INT32		INT31		INT30	
8B	EINTT4	INT37		INT36		INT35		INT34	

Note: All register initial after system reset.

23.1 Register Description

23.1.1 External Interrupt Enable 1/2/3 Register (EIE1/2/3) (Default Value: 0000_0000)

1: Enable.

In enable state, the external interrupt source will cause an external interrupt request to generate the interrupt to Microprocessor.

0: Disable.

23.1.2 External Interrupt Request 1/2/3 Register (EIREQ1/2/3) (Default Value: 0000_0000)

Bit7~0: External Interrupt Request

Read: 1: Requested, 0: Not Requested.

Write: 1: Clear Request, 0: No Change

23.1.3 External Interrupt Trigger Select 1 Register (EINTT1) (Default Value: 0000_0000)

Bit 7~0:INT17~10 Trigger Type

Indicate the trigger type of External Interrupt 17~10.

1: Rising Edge

0: Falling Edge.

23.1.4 External Interrupt Trigger Select 2 Register (EINTT2) (Default Value: 0000_0000)

Bit 7~0:INT27~20 Trigger Type

Indicate the trigger type of External Interrupt 27~20.

1: Rising Edge

0: Falling Edge.

23.1.5 External Interrupt Trigger Select 3 Register (EINTT3) (Default Value: 0000_0000)

Bit 7~6:INT33 Trigger Type

Indicate the trigger type of External Interrupt 33.

1x: Rising Edge& Falling Edge,

01: Rising Edge,

00: Falling Edge

Bit 5~4:INT32 Trigger Type

Indicate the trigger type of External Interrupt 32.

1x: Rising Edge& Falling Edge,

01: Rising Edge,

00: Falling Edge

Bit 3~2:INT31 Trigger Type

Indicate the trigger type of External Interrupt 31.

1x: Rising Edge& Falling Edge,

01: Rising Edge,

00: Falling Edge

Bit 1~0:INT30 Trigger Type

Indicate the trigger type of External Interrupt 30.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

23.1.6 External Interrupt Trigger Select 4 Register (EINTT4) (Default Value: 0000_0000)

Bit 7~6:INT37 Trigger Type

Indicate the trigger type of External Interrupt 37.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

Bit 5~4:INT36 Trigger Type

Indicate the trigger type of External Interrupt 36.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

Bit 3~2:INT35 Trigger Type

Indicate the trigger type of External Interrupt 35

01: Rising Edge

00: Falling Edge

Bit 1~0:INT34 Trigger Type

Indicate the trigger type of External Interrupt 34.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

24. FLASH MEMORY

The W83L951ADG has a 64KByte, 3.3-volt only CMOS flash memory. The byte-wide (×8) data appears on DQ7~DQ0. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is not required. The unique cell architecture of the Flash results in fast program/erase operations with extremely low current consumption (compared to other comparable 3.3-volt flash memory products). The device can also be programmed and erased by using standard EPROM programmers.

24.1 External Programming Mode

For programming the flash by external device, the Winbond Keyboard controller must enter the flash-programming mode by TEST# Pin connected to GND. RESET# Pin is connected to GND. FA [7:0] and FD [7:0] port is combined to GP07 to GP00. FA [7:0] is latched by the ALE (GP34).

In External Programming Mode, the W83L951ADG protects Internal Flash data, so the W83L951ADG will close “Read Command”. Under this condition, users must run “Erase Command” to use “Read Command”.

24.2 Internal Programming Mode

In the W83L951ADG, in addition to accessing the internal flash from outside, SFR can be accessed by Microprocessor. When Enable Memory Bit of Memory Mapping Control Register is high, and PC is F800~FFFFh, Microprocessor can access Internal Flash by SFR.

Table 24-1.Internal Programming Flash Register Definition

Internal Programming Flash									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F9	FCON	CEB	OEB	WEB	Reserved				EXCHANG_GP
FA	FADDH	A[15:8]							
FB	FADDL	A[7:0]							
FC	FDATA	DQ[7:0]							

24.2.1 Flash Control Register (FCON) (Default Value: 0000_0000)

Bit7: Flash Chip Select Enable (CEB)

Similar to CE# Pin. Refer to next section for further details.

Bit6: Flash Output Enable (OEB)

Similar to OE# Pin. Refer to next section for further details.

Bit5: Flash Write Enable (WEB)

Similar to WE# Pin. Refer to next section for further details.

Bit4~Bit1: Reserved

Bit0: Exchange GPIOA/B/C to GPIO1/0/3 Function (Reserved)

24.2.2 Flash Address High Byte Register (FADDH) (Default Value: 0000_0000)

Address [15:8] Input, Like A [15:8] Pin. Refer to next section for further details.

24.2.3 Flash Address Low Byte Register (FADDL) (Default Value: 0000_0000)

Address [7:0] Input, Like A [7:0] Pin. Refer to next section for further details.

24.2.4 Flash Data Register (FDATA) (Default Value: 0000_0000)

Write: Data Input

Read: Data Output

Similar to DQ [7:0] Pin. Refer to next section for further details.

24.3 Device Bus Operation

24.3.1 Read Mode

The read operation of Internal Flash is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

24.3.2 Write Mode

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is

written by bringing #WE to logic low state, while #CE is at logic low state and #OE is at logic high state. Addresses are latched on the falling edge of #WE or #CE, depending on which happens later; while data is latched on the rising edge of #WE or #CE, depending on which happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

24.3.3 Output Disable Mode

With the #OE input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

24.3.4 Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on #OE, #CE, or #WE will not initiate a write cycle.

24.4 Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. "Command Definitions" defines the valid register command sequences.

24.4.1 Read Command

The device will automatically power-up in the read state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. The device will automatically return to read state after completing an Embedded Program or Embedded Erase algorithm.

Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

24.4.2 Byte Program Command

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two "unlock" write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the embedded program algorithm. Addresses are latched on the falling edge of #CE or #WE, depending on which happens later and the data is latched on the rising edge of #CE or #WE, depending on which happens first. The rising edge of #CE or #WE (the

one happens first) begins programming using the Embedded Program Algorithm. Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as Data Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see "Hardware Sequence Flags"). Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for Data Polling operations. Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data in that particular location will be corrupted.

Programming is allowed in any sequence and across sector boundaries. Be aware that a data "0" cannot be programmed back to a "1". Attempting to program 0 back to 1, the toggle bit will stop toggling. Only erase operations can convert "0"s to "1"s.

Refer to the Programming Command Flow Chart using typical command strings and bus operations.

24.4.3 Chip Erase Command

Chip erase is a six-bus-cycle operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles are asserted, followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence, the device will automatically erase and verify the entire memory for an all one data pattern. The erase is performed sequentially on each sector at the same time (see "Feature"). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last #WE pulse in the command sequence and terminates when the data on DQ7 is "1" when the device returns to read the mode.

Refer to the Erase Command Flow Chart using typical command strings and bus operations.

24.5 Write Operation Status

24.5.1 DQ7: Data Polling

The W39L040 device features Data Polling as a method to indicate to the host that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7.

During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output.

Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce

a "1" at the DQ7 output. For chip erase, the Data Polling is valid after the rising edge of the sixth pulse in the six #WE write pulse sequences. For sector erase, the Data Polling is valid after the last rising edge of the sector erase #WE pulse. Data Polling must be performed at sector addresses within any of the sectors being erased. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable (#OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that bytes valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0~DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see "Command Definitions").

24.5.2 DQ6: Toggle Bit

The Flash also features the "Toggle Bit" as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (#OE toggling) data from the device at any address will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth #WE pulse in the four write pulse

sequences. For chip erase, the Toggle Bit is valid after the rising edge of the sixth #WE pulse in the six write pulse sequence. For sector/page erase, the Toggle Bit is valid after the last rising edge of the sector/page erase #WE pulse. The Toggle Bit is active during the sector/page erase time-out.

Either #CE or #OE toggling will cause DQ6 to toggle.

24.6 Table of Operating Modes

Table 24-2.Device Bus Operations

MODE	#CE	#OE	#WE	A0	A1	DQ0~DQ7
Read	VIL	VIL	VIH	A0	A1	Dout
Write	VIL	VIH	VIL	A0	A1	Din
Standby	VIH	X	X	X	X	High Z
Output Disable	VIL	VIH	VIH	X	X	High Z

Table 24-3.Command Definition

Command Description	No. of Cycle	1ST	2ND	3RD	4TH	5TH	6TH
		Addr,Data					
Read	1	Ain, Dout					
Byte Program	4	5555,AA	2AAA,55	5555,A0	Ain, Din		
Chip Erase	6	5555,AA	2AAA,55	5555,80	5555,AA	2AAA,55	5555,10
Page Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	PA 50
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit 1	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit 2	1	XXXX F0					

Notes:

1. Address Format: A14 ~ A0 (Hex); Data Format: DQ7 ~ DQ0 (Hex)

2. Either one of the two Product ID Exit commands can be used.

3. PA: Page Address = FXXXh to 0XXXh for page 15 to page 0.

24.7 Embedded Algorithm

24.7.1 Embedded Programming Algorithm

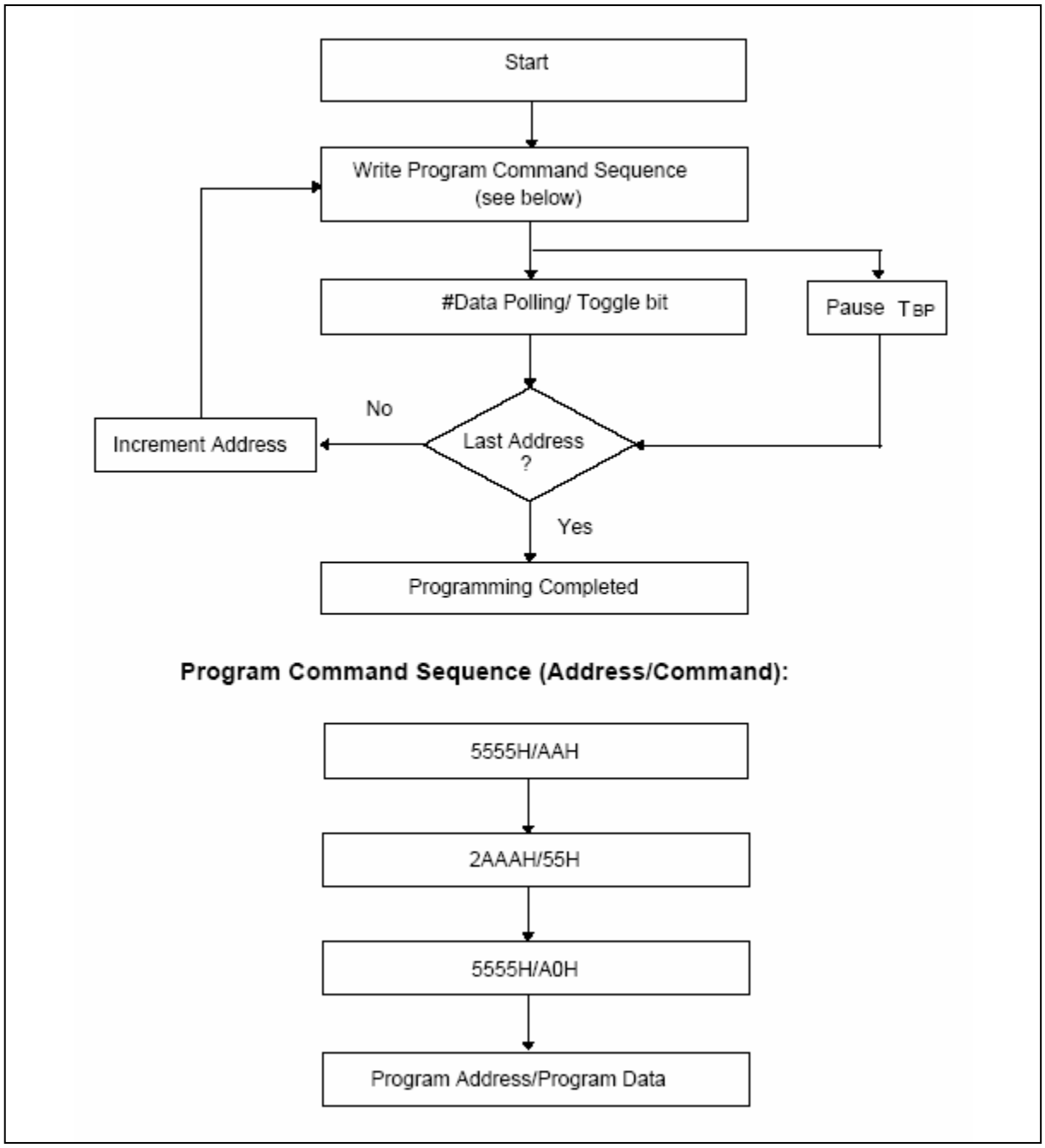


Figure 24-1.Embedded Programming Algorithm State Diagram

24.7.2 Embedded Erase Algorithm

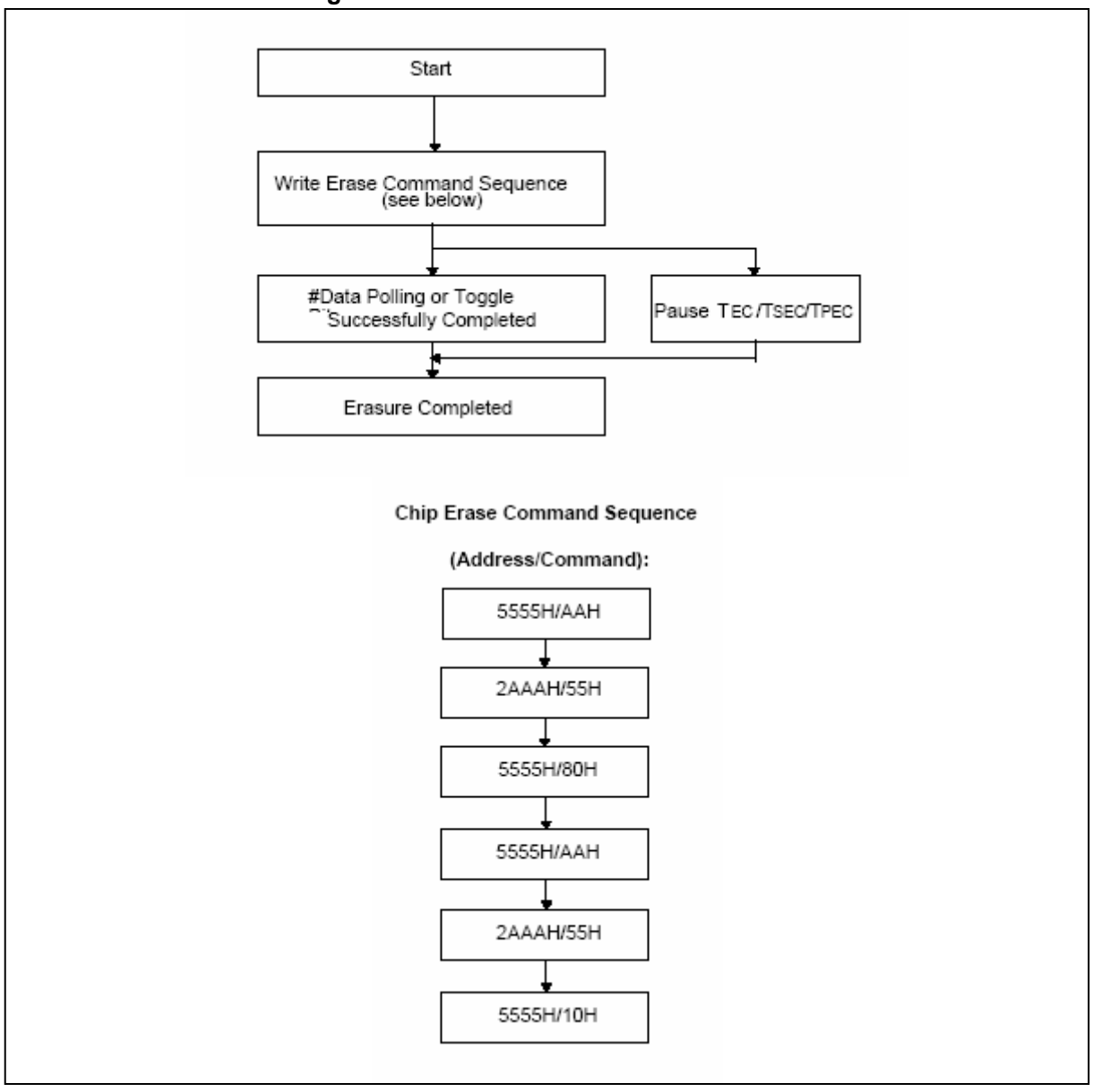


Figure 24-2.Embedded Erase Algorithm State Diagram

24.7.3 Embedded #Data Polling Algorithm

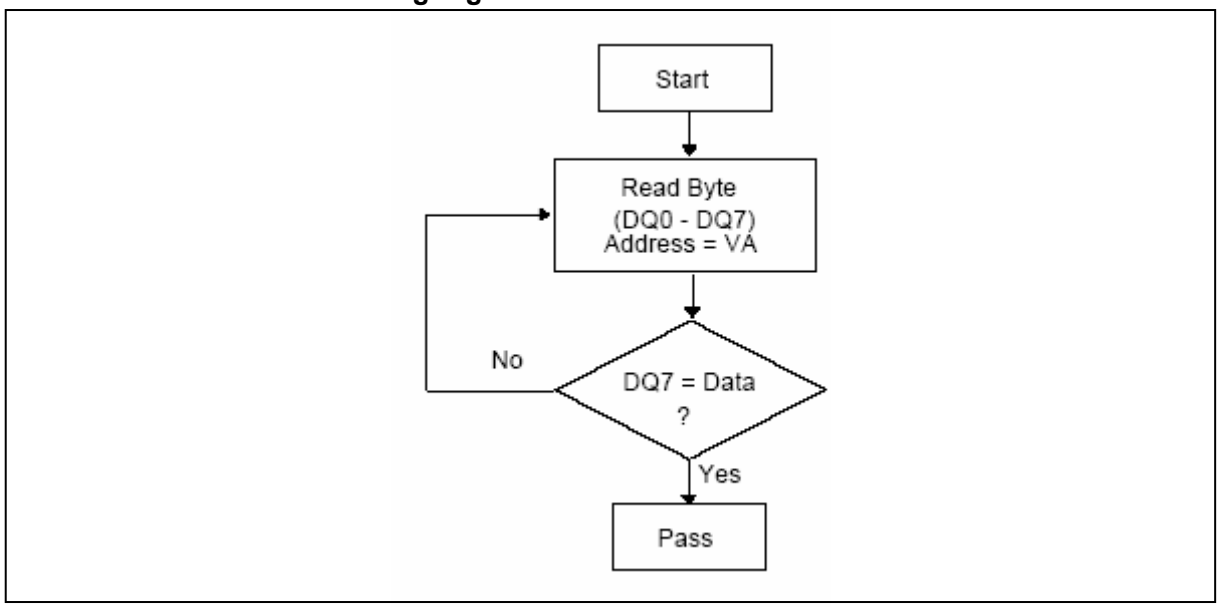


Figure 24-3.Embedded #Data Polling Algorithm State Diagram

Note: VA = Byte Address for programming

= Any Group Address during chip erase

24.7.4 Embedded Toggle Bit Algorithm

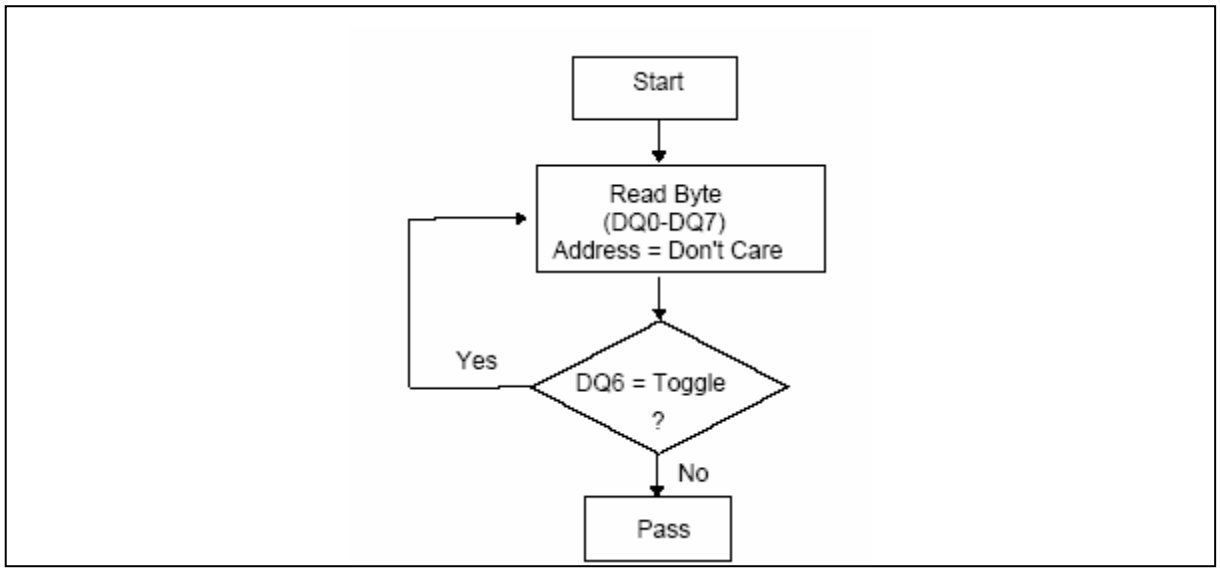


Figure 24-4.Embedded Toggle Bit Algorithm State Diagram

24.8 Timing Parameters

Table 24-4.Read Cycle Timing Parameters Table

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	TRC	90	-	ns
Chip Enable Access Time	TCE	-	90	ns
Address Access Time	TAA	-	90	ns
Output Enable Access Time	TOE	-	45	ns
#CE Low to Active Output	TCLZ	0	-	ns
#OE Low to Active Output	TOLZ	0	-	ns
#CE High to High-Z Output	TCHZ	-	25	ns
#OE High to High-Z Output	TOHZ	-	25	ns
Output Hold from Address Change	TOH	0	-	ns

Note: (VDD = 3.3V 0.3V, VSS = 0V, TA = 0 to 70 ° C or -40 to 85 ° C)

Table 24-5.Write Cycle Timing Parameters Table

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	40	-	-	nS
#WE and #CE Setup Time	TCS	0	-	-	nS
#WE and #CE Hold Time	TCH	0	-	-	nS
#OE High Setup Time	TOES	0	-	-	nS
#OE High Hold Time	TOEH	0	-	-	nS
#CE Pulse Width	TCP	100	-	-	nS
#WE Pulse Width	TWP	100	-	-	nS
#WE High Width	TWPH	100	-	-	nS
Data Setup Time	TDS	40	-	-	nS
Data Hold Time	TDH	10	-	-	nS
Byte Programming Time	TBP	-	35	50	S
Chip Erase Cycle Time	TEC	-	50	100	mS
Sector/Page Erase Cycle Time	TEP	-	12.5	25	mS

Table 24-6.Power-up Timing Parameters Table

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	S
Power-up to Write Operation	TPU. WRITE	5	mS

24.9 Timing Waveforms

The Timing Waveforms do not contain ALE (GP34 and TS (GP33). If using External Mode to access, TS pin must keep low. Use ALE (GP34) to do Low Address Byte (GP0) latch. ALE is high active and the pulse width is at least 50ns. Low Address Byte (GP0) must be stable before ALE changes the state from high to low.

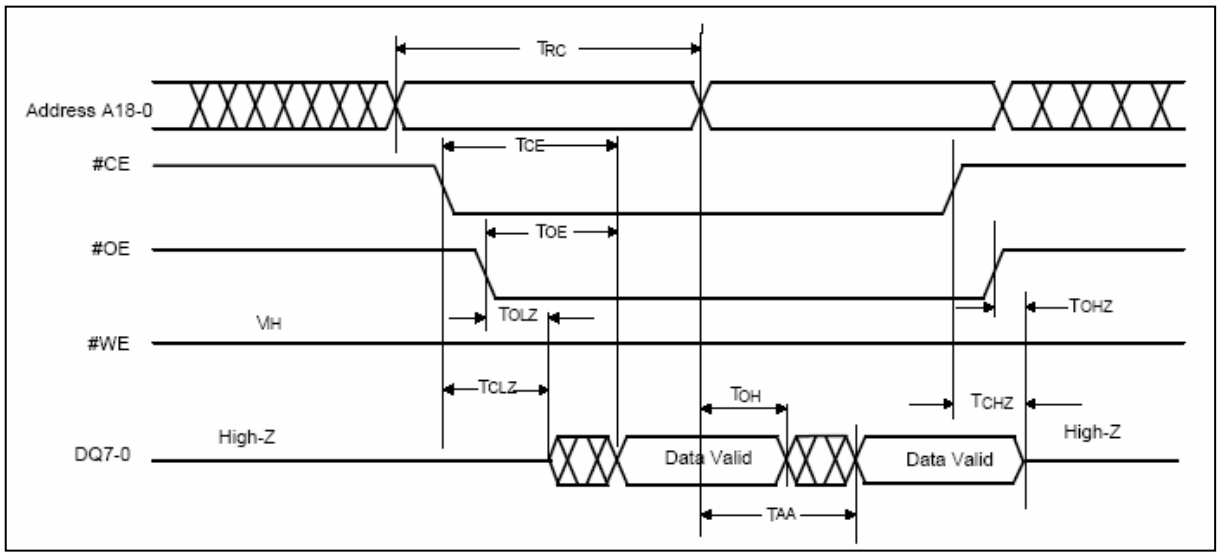


Figure 24-5.Read Cycle Timing Diagram

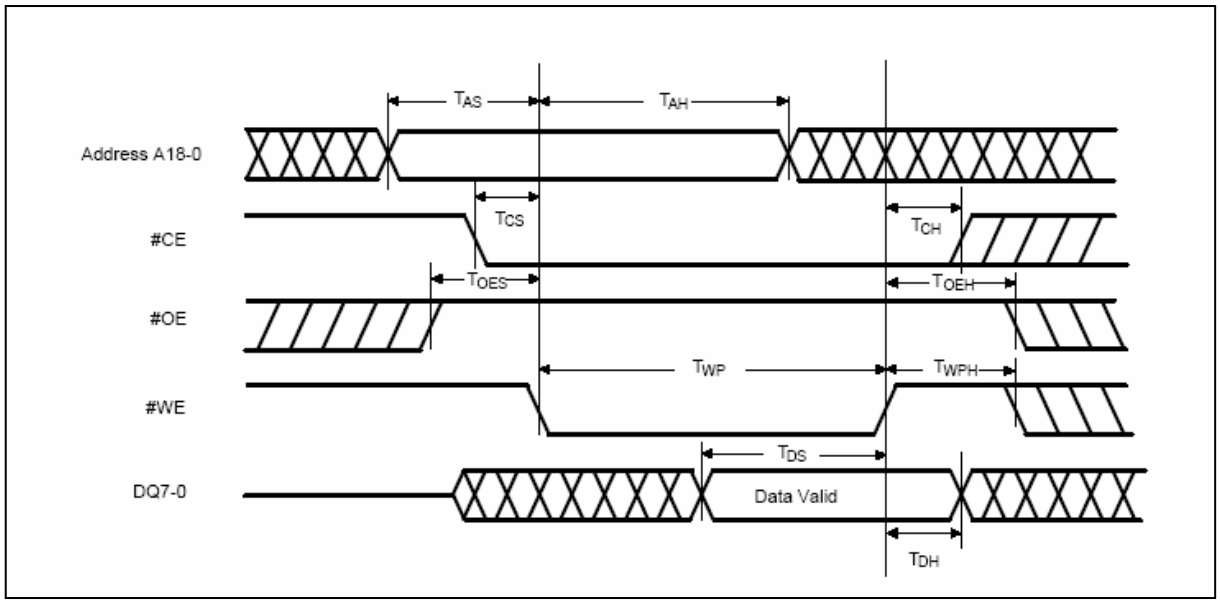


Figure 24-6.#WE Controlled Command Write Cycle Timing Diagram

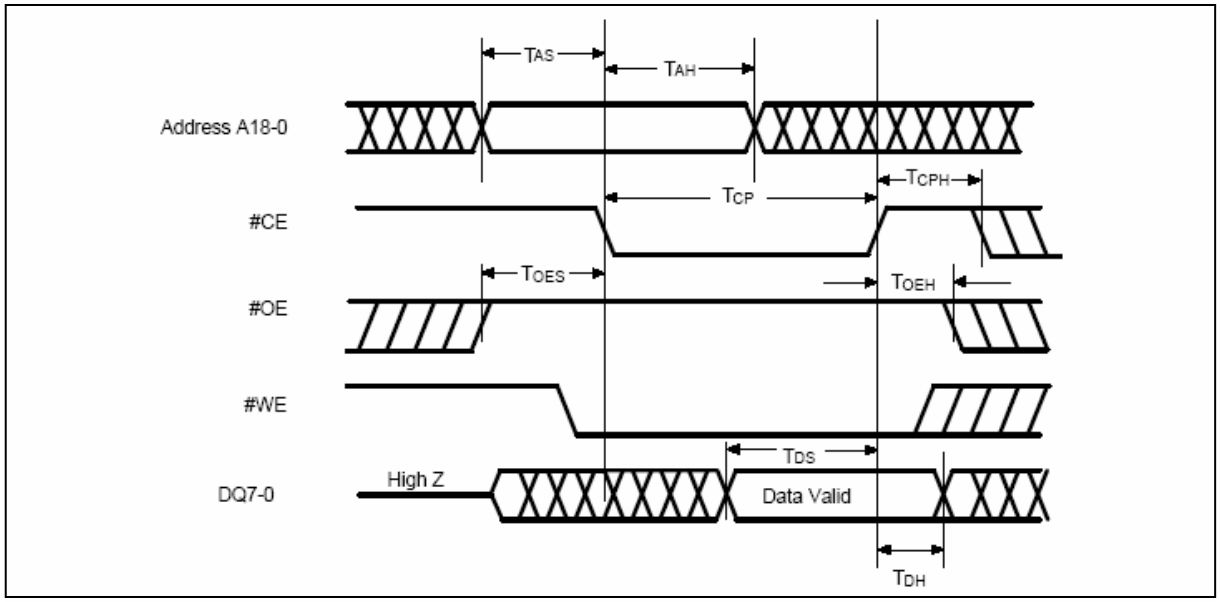


Figure 24-7.#CE Controlled Command Write Cycle Timing Diagram

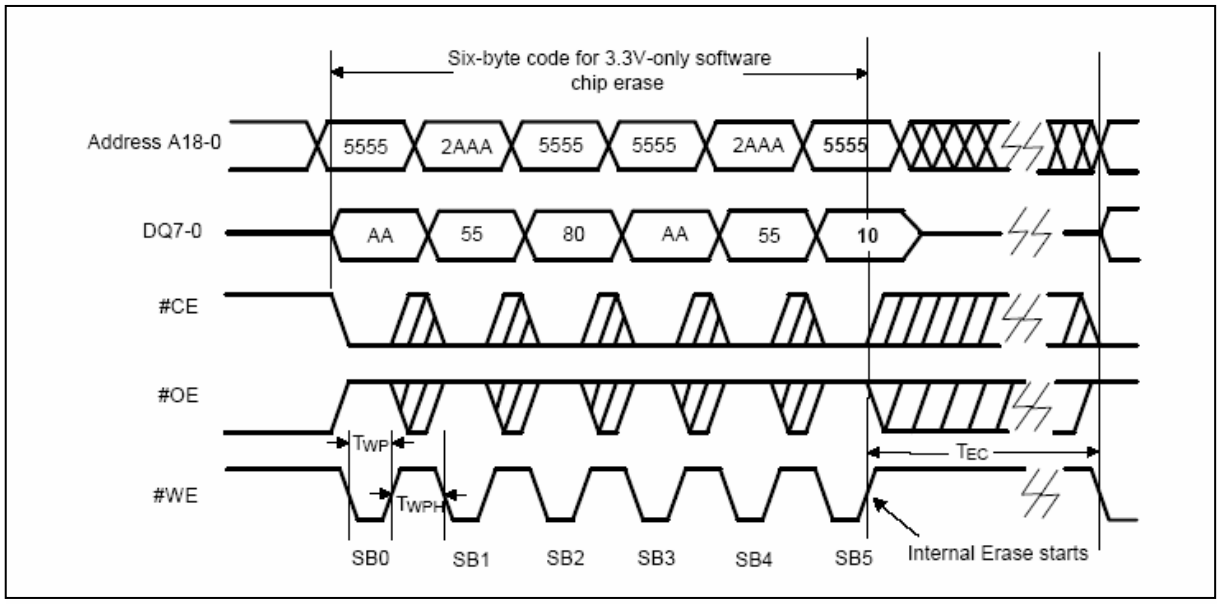


Figure 24-8.Chip Erase Timing Diagram

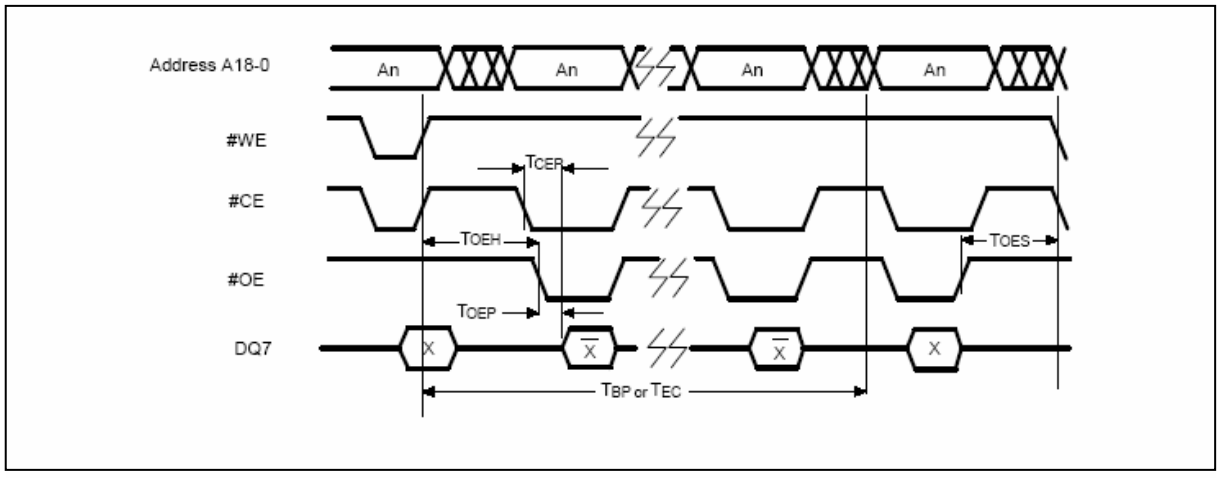


Figure 24-9.Data Polling Timing Diagram

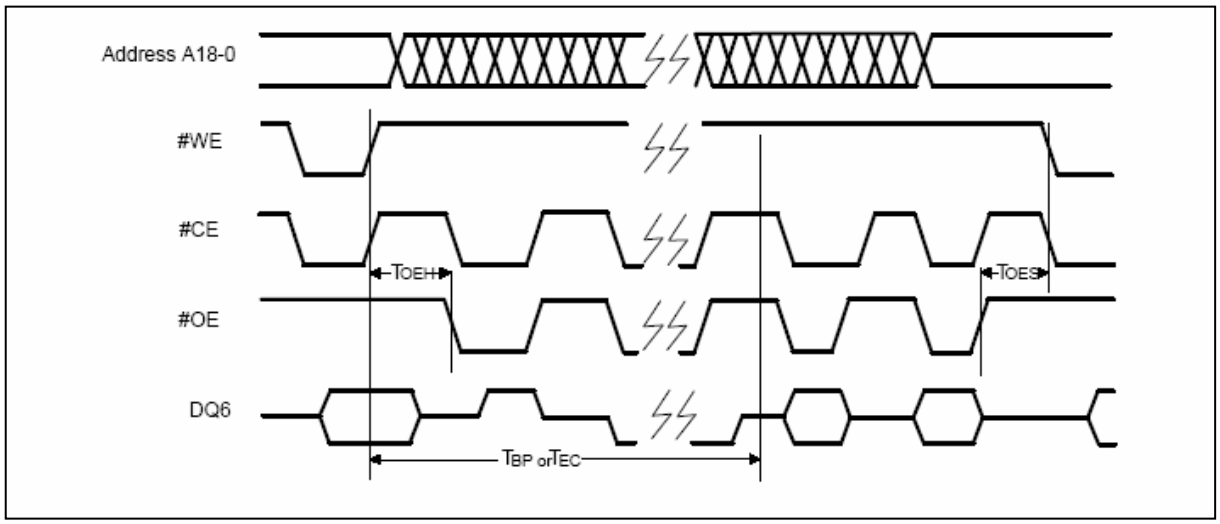


Figure 24-10.Toggle Bit Timing Diagram

25. ELECTRICAL CHARACTERISTIC

25.1 Absolute Maximum Ratings

Table 25-1 Absolute Maximum Rating Table

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to +4.6	V
Input Voltage	3.3 ± 10%	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +125	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

25.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{12tsm}—Bi-directional pin, TTL level, Schmitt-trigger input, selectable 250uA/12mA sink capability, 12mA source capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA / -250uA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{12tsai} — Bi-directional pin, TTL level, Schmitt-trigger input, Analog Input, 12mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{12tsao} — Bi-directional pin, TTL level, Schmitt-trigger input, Analog Output, 12mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{16tsh} — Bi-directional pin, TTL level, Schmitt-trigger input, 5V Tolerant, 16mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Output High Voltage	VOH	2.4			V	IOH = -16 mA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{24ts} — Bi-directional pin, TTL level, Schmitt-trigger input, 16mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = -24 mA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I_{ts} — Input pin, TTL level, Schmitt-trigger input						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V

26. HOW TO READ THE TOP MARKING

1st line: Winbond logo

2nd line: W83L951ADG, chip part number for Leadfree product

3rd line: Manufacture tracking code 22299460-N1

4th line: Tracking code 704 A A AB

704: Packages made in '07, week 04

A: Assembly house ID; A means ASE, O means OSE, G means GR…

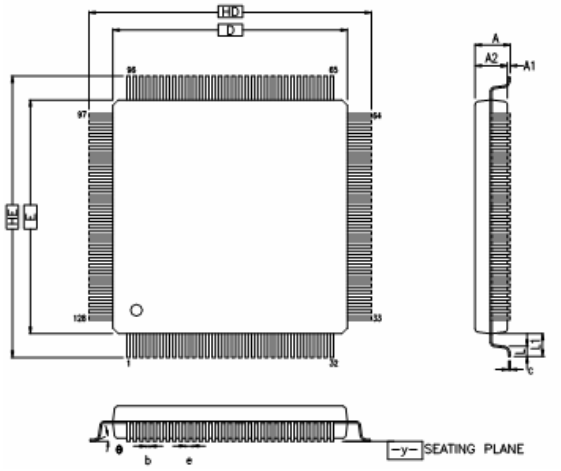
A: IC revision

AB: Internal version

27. PACKAGE DIMENSIONS

Winbond provides two packages for customers that contain 128- pin LQFP.

128-pin LQFP



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.