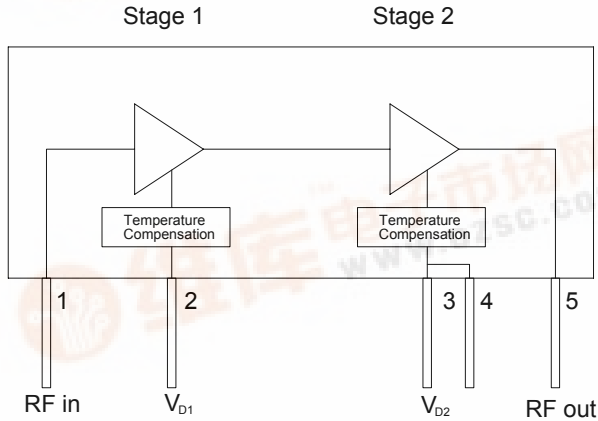




## Product Description

Sirenza Microdevices' **XD010-22S-D2F** 12W power module is a robust 2-stage Class A/AB amplifier module for use in the driver stages of GSM/EDGE RF power amplifiers for cellular base stations. The power transistors are fabricated using Sirenza's latest, high performance LDMOS process. This unit operates from a single voltage and has internal temperature compensation of the bias voltage to ensure stable performance over the full temperature range. It is a drop-in, no-tune solution for medium power applications requiring high efficiency, excellent linearity, and unit-to-unit repeatability. It is internally matched to 50 ohms.

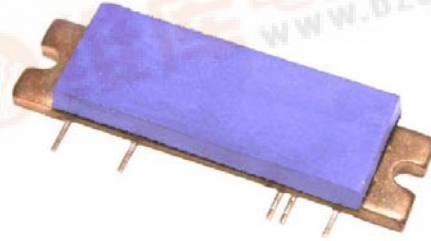
## Functional Block Diagram



Case Flange = Ground

## XD010-22S-D2F

1805-1880 MHz Class A/AB  
12W Power Amplifier Module



## Product Features

- 50  $\Omega$  RF impedance
- 12W Output  $P_{1dB}$
- Single Supply Operation : Nominally 28V
- High Gain: 31 dB at 1840 MHz
- High Efficiency: 25% at 1840 MHz
- Advanced, XeMOS II LDMOS FETS
- Temperature Compensation

## Applications

- Base Station PA driver
- Repeater
- GSM / EDGE

## Key Specifications

| Symbol          | Parameter  | Unit           | Min. | Typ. | Max. |
|-----------------|--|----------------|------|------|------|
| Frequency       | Frequency of Operation   | MHz            | 1805 |      | 1880 |
| $P_{1dB}$       | Output Power at 1dB Compression (single tone)                    | W              | 10   | 12   |      |
| Gain            | Gain at 5W Output Power (CW)                                     | dB             | 28.5 | 31   |      |
| Gain Flatness   | Peak to Peak Gain Variation                                      | dB             |      | 0.5  | 1.0  |
| IRL             | Input Return Loss 5W Output (CW)                                 | dB             | 10   | 14   |      |
| Efficiency      | Drain Efficiency at 10W CW                                       | %              | 20   | 25   |      |
| Linearity       | RMS EVM at 5W EDGE output  | %              |      | 1.5  |      |
|                 | Peak EVM at 5W EDGE output                                       | %              |      | 5    |      |
|                 | 3 <sup>rd</sup> Order IMD at 10W PEP (Two Tone; 1MHz $\Delta$ F) | dBc            | -26  | -32  |      |
| Delay           | Electrical Delay   | nS             |      | 2.5  |      |
| Phase Linearity | Deviation from Linear Phase (Peak to Peak)                       | Deg            |      | 0.5  |      |
| $R_{TH, j-1}$   | Thermal Resistance Stage 1 (Junction to Case)                    | $^{\circ}$ C/W |      | 11   |      |
| $R_{TH, j-2}$   | Thermal Resistance Stage 2 (Junction to Case)                    | $^{\circ}$ C/W |      | 4    |      |

Test Conditions  $Z_{in} = Z_{out} = 50\Omega$ ,  $V_{DD} = 28.0V$ ,  $I_{DQ1} = 230mA$ ,  $I_{DQ2} = 115mA$ ,  $T_{Flange} = 25^{\circ}C$

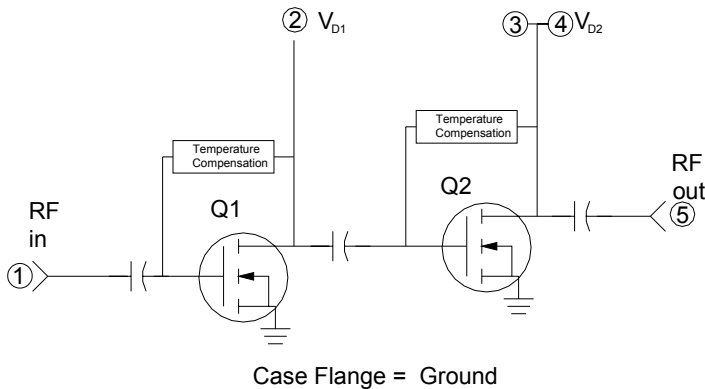
### Quality Specifications

| Parameter  |  | Unit  | Typical               |
|------------|--|-------|-----------------------|
| ESD Rating | Human Body Model, JEDEC Document - JESD22-A114-B | V     | 8000                  |
| MTTF       | 85°C Leadframe, 200°C Channel                    | Hours | 1.2 X 10 <sup>6</sup> |

### Pin Description

| Pin #  | Function        | Description   |
|--------|-----------------|---|
| 1      | RF Input        | Module RF input. Care must be taken to protect against video transients that may damage the active devices.   |
| 2      | V <sub>D1</sub> | This is the drain voltage for the first stage of the amplifier module. The first stage gate bias is temperature compensated to maintain constant quiescent drain current over the operating temperature range. Nominally +28Vdc See Note 1.                     |
| 3,4    | V <sub>D2</sub> | This is the drain voltage for the 2 <sup>nd</sup> stage of the amplifier module. The 2 <sup>nd</sup> stage gate bias is temperature compensated to maintain constant quiescent drain current over the operating temperature range. Nominally +28Vdc See Note 1. |
| 5      | RF Output       | Module RF output. Care must be taken to protect against video transients that may damage the active devices.  |
| Flange | Gnd             | Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions in application note AN-060 on Sirenza's web site.                           |

### Simplified Device Schematic



**Note 1:**

The internally generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be accomplished with AGC external to the module.

**Note 2:**

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

**Note 3:**

This module was designed to have its leads hand soldered to an adjacent PCB. The maximum soldering iron tip temperature should not exceed 700° C, and the soldering iron tip should not be in direct contact with the lead for longer than 10 seconds. Refer to app note AN060 ([www.sirenza.com](http://www.sirenza.com)) for further installation instructions.

### Absolute Maximum Ratings

| Parameters   | Value       | Unit |
|--|-------------|------|
| 1 <sup>st</sup> Stage Bias Voltage (V <sub>D1</sub> )  | 35          | V    |
| 2 <sup>nd</sup> Stage Bias Voltage (V <sub>D2</sub> )  | 35          | V    |
| RF Input Power   | +20         | dBm  |
| Load Impedance for Continuous Operation Without Damage | 5:1         | VSWR |
| Output Device Channel Temperature                      | +200        | °C   |
| Operating Temperature Range                            | -20 to +90  | °C   |
| Storage Temperature Range                              | -40 to +100 | °C   |

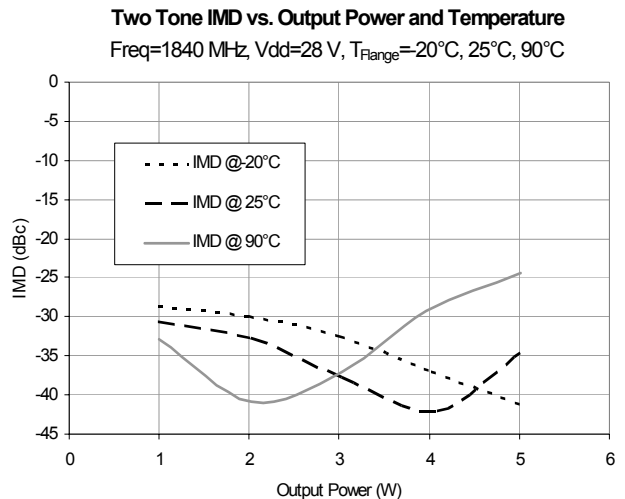
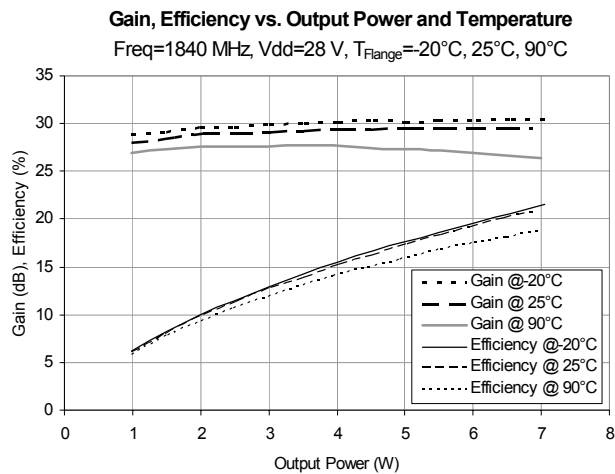
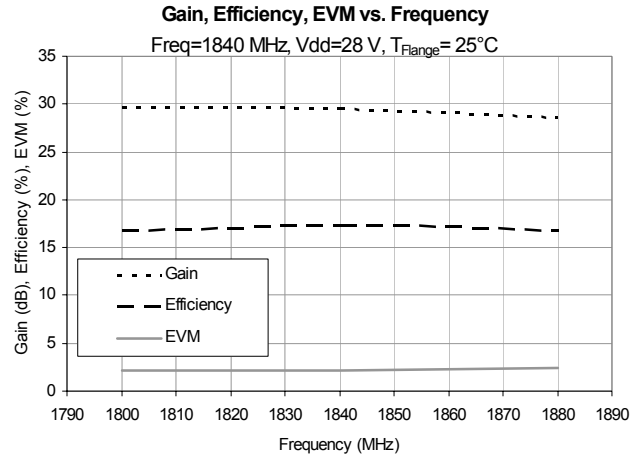
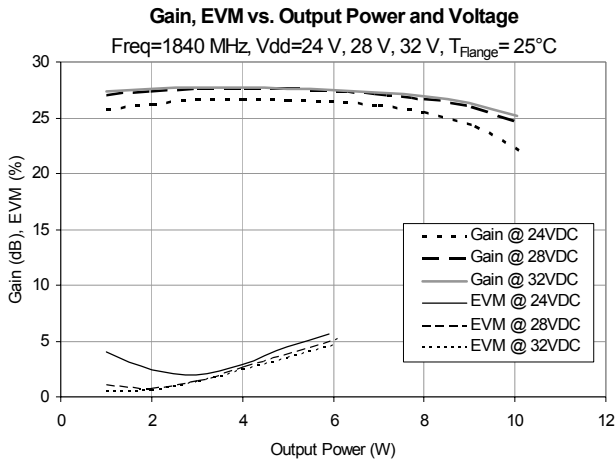
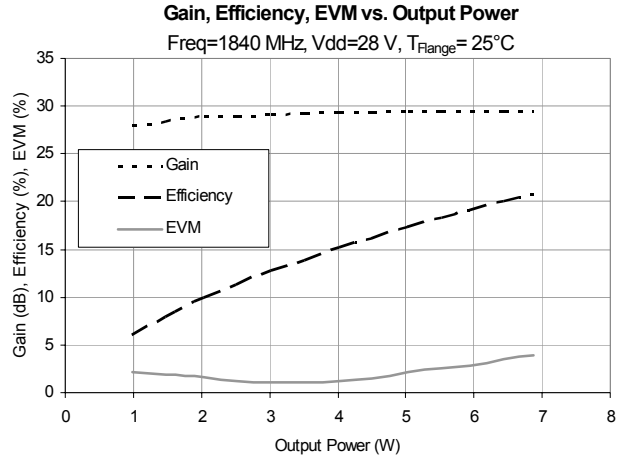
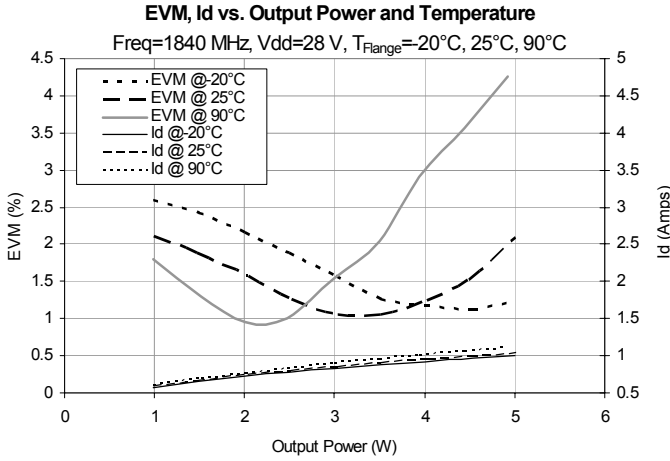
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.



**Caution: ESD Sensitive**

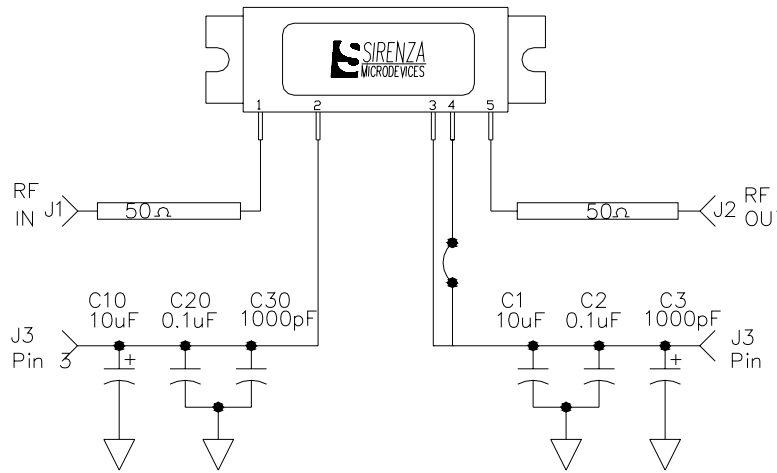
Appropriate precaution in handling, packaging and testing devices must be observed.

**Typical Performance Curves**



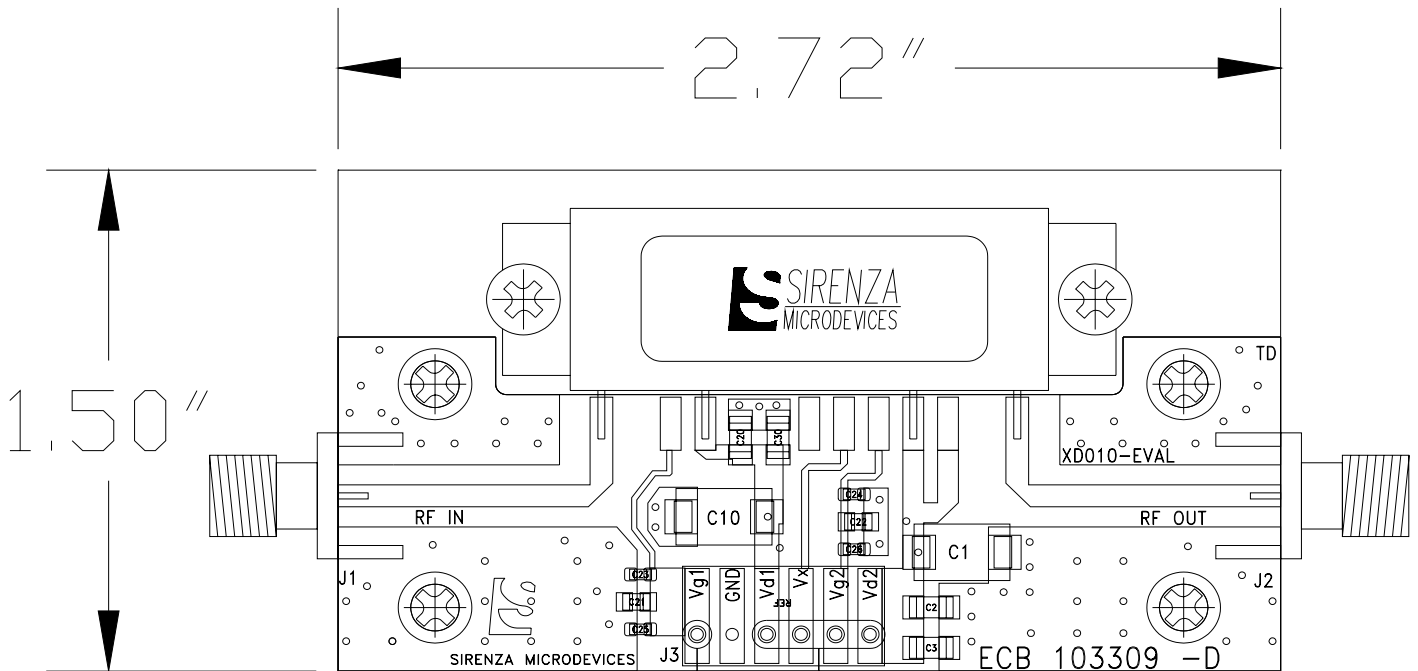
**Test Board Schematic with module attachments shown**

**Test Board Bill of Materials**



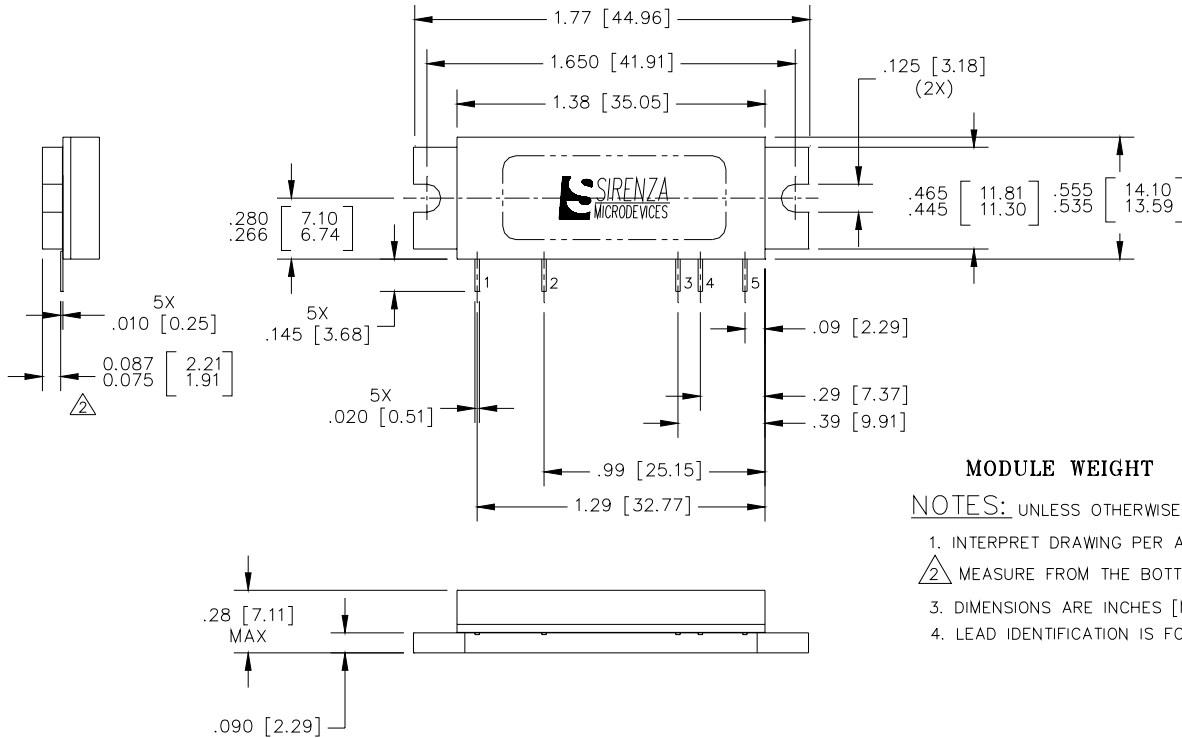
| Component          | Description   | Manufacturer |
|--------------------|---|--------------|
| PCB                | Rogers 4350, $\epsilon_r=3.5$<br>Thickness=30mils                   | Rogers       |
| J1, J2             | SMA, RF, Panel Mount Tab W/<br>Flange                               | Johnson      |
| J3                 | MTA Post Header, 6 Pin, Rect-<br>angle, Polarized, Surface<br>Mount | AMP          |
| C1, C10            | Cap, 10 $\mu$ F, 35V, 10%, Tant,<br>Elect, D                        | Kemet        |
| C2, C20            | Cap, 0.1 $\mu$ F, 100V, 10%, 1206                                   | Johanson     |
| C3, C30            | Cap, 1000pF, 100V, 10%, 1206  | Johanson     |
| C25, C26           | Cap, 68pF, 250V, 5%, 0603   | ATC          |
| C21, C22           | Cap, 0.1 $\mu$ F, 100V, 10%, 0805                                   | Panasonic    |
| C23, C24           | Cap, 1000pF, 100V, 10%, 0603  | AVX          |
| Mounting<br>Screws | 4-40 X 0.250"   | Various      |

**Test Board Layout**



To receive Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture, contact applications support at [support@sirenza.com](mailto:support@sirenza.com). Data sheet for evaluation circuit (XD010-EVAL) available from Sirenza website.

**Package Outline Drawing**



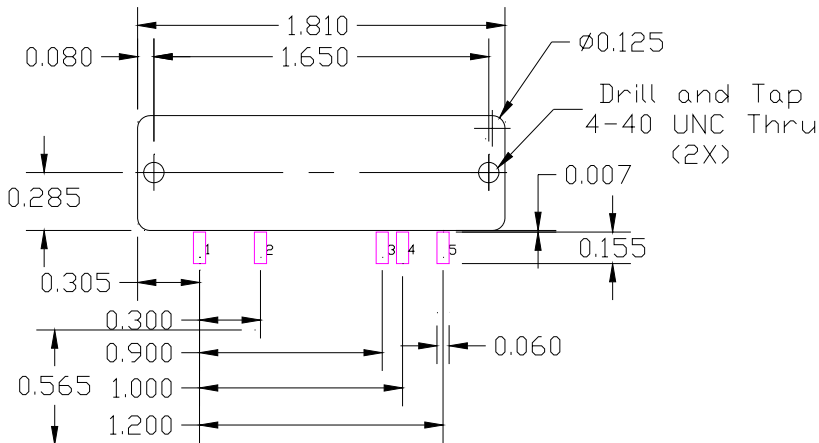
**MODULE WEIGHT = 12gm Nominal**

**NOTES:** UNLESS OTHERWISE SPECIFIED

1. INTERPRET DRAWING PER ANSI Y14.5.
2. MEASURE FROM THE BOTTOM OF THE LEADS.
3. DIMENSIONS ARE INCHES [MM].
4. LEAD IDENTIFICATION IS FOR REFERENCE ONLY.

**Recommended PCB Cutout and Landing Pads for the D2F Package**

**Note 3:** Dimensions are in inches



Refer to Application note AN-060 "Installation Instructions for XD Module Series" for additional mounting info. App note available at [www.sirenza.com](http://www.sirenza.com)