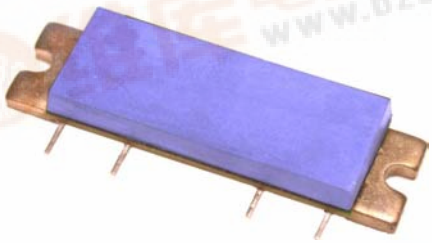
# XD010-42S-D4F

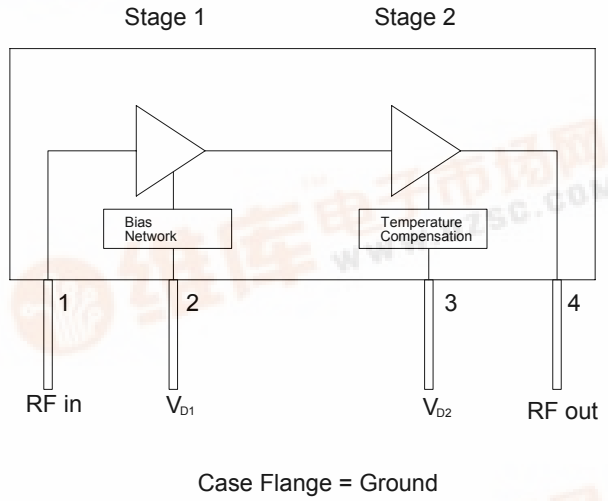
## 869-894 MHz Class A
## 8 W Power Amplifier Module



## Product Description

Sirenza Microdevices' **XD010-42S-D4F** 8W power module is a robust 2-stage Class A amplifier module for use in the driver stages of linear RF power amplifiers of cellular base stations. The power transistors are fabricated using Sirenza's latest, high performance LDMOS process. This unit operates from a single voltage and has internal temperature compensation of the bias voltage to ensure stable performance over the full temperature range. It is internally matched to 50 ohms.

## Functional Block Diagram




Case Flange = Ground

## Product Features

- **50 Ω RF impedance**
- **8W Output P1dB Typical**
- **Single Supply Operation : Nominally 28V**
- **High Gain: 30 dB at 880 MHz**
- **Advanced, XeMOS II LDMOS FETS**
- **Temperature Compensation**

## Applications

- **Base Station PA driver**
- **Repeater**
- **CDMA**
- **GSM / EDGE**

## Key Specifications

| Symbol | Parameter | Unit | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| Frequency | Frequency of Operation | MHz | 869 | | 894 |
| $P_{1dB}$ | Output Power at 1dB Compression, 880 MHz | W | 7 | 8 | |
| Gain | Gain at 1W Output Power (CW) | dB | 28 | 30 | |
| Gain Flatness | Over Frequency at 1W Output (CW) | dB | | 0.4 | 1 |
| IRL | Input Return Loss at 1W Output (CW) (50Ω Ref) | dB | 14 | 20 | |
| Efficiency | Drain Efficiency at 8W CW Output | % | 22 | 24 | |
| | Drain Efficiency at 1W CDMA (Single Carrier IS-95) | % | | 3.5 | |
| Linearity | ACPR at 1W CDMA Output (Single Carrier IS-95, 9 Ch Fwd, Offset=750KHz, ACPR Integrated Bandwidth) | dB | | -50 | |
| | ALT-1 at 1W CDMA (Single Carrier IS-95, 9 Ch Fwd, Offset=1980KHz, ACPR Integrated Bandwidth) | dB | | -75 | |
| | 3rd Order IMD at 8W PEP (Two Tone 1MHz Spacing) | dB | -28 | -32 | |
| | 3rd Order IMD at 1W PEP (Two Tone 1MHz Spacing) | dBc | -40 | -50 | |
| Delay | Signal Delay from Pin 1 to Pin 4 | nS | | 3.9 | |
| Phase Linearity | Deviation from Linear Phase (Peak to Peak) | Deg | | 0.5 | |
| $R_{TH, j-l}$ | Thermal Resistance Stage 1 (Junction to Case) | ºC/W | | 11 | |

**Test Conditions: $Z_{in} = Z_{out} = 50\Omega$, $V_{DD} = 28.0V$, $I_{DQ1} = 230mA$, $I_{DQ2} = 700mA$, $T_{Flange} = 25ºC$**

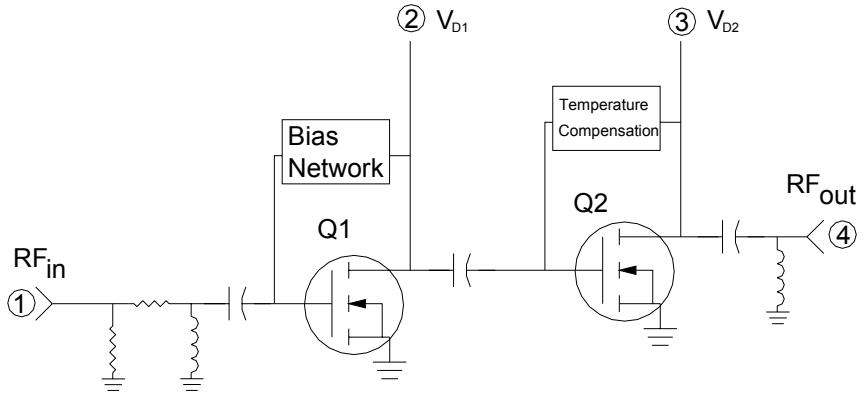
## Quality Specifications

| Parameter | | Unit | Typical |
|---|---|---|---|
| ESD Rating | Human Body Model, JEDEC Document - JESD22-A114-B | V | 8000 |
| MTTF | 85°C Leadframe, 200°C Channel | Hours | $1.2 \times 10^6$ |

## Pin Description

| Pin # | Function | Description |
|---|---|---|
| 1 | RF Input | Module RF input. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices. |
| 2 | $V_{D1}$ | This is the drain voltage for the first stage. Nominally +28Vdc |
| 3 | $V_{D2}$ | This is the drain voltage for the 2nd stage of the amplifier module. The 2nd stage gate bias is temperature compensated to maintain constant quiescent drain current over the operating temperature range. See Note 1. |
| 4 | RF Output | Module RF output. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices. |
| Flange | Gnd | Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions in application note AN-060 on Sirenza's web site. |

## Simplified Device Schematic




Case Flange = Ground

## Absolute Maximum Ratings

| Parameters | Value | Unit |
|---|---|---|
| 1st Stage Bias Voltage ($V_{D1}$) | 35 | V |
| 2nd Stage Bias Voltage ($V_{D2}$) | 35 | V |
| RF Input Power | +20 | dBm |
| Load Impedance for Continuous Operation Without Damage | 5:1 | VSWR |
| Output Device Channel Temperature | +200 | ºC |
| Base Plate Temperature: Operating with no RF Present | +90 | ºC |
| Operating Temperature Range | -20 to +90 | ºC |
| Storage Temperature Range | -40 to +100 | ºC |

**Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.**

**Caution: ESD Sensitive**
Appropriate precaution in handling, packaging and testing devices must be observed.

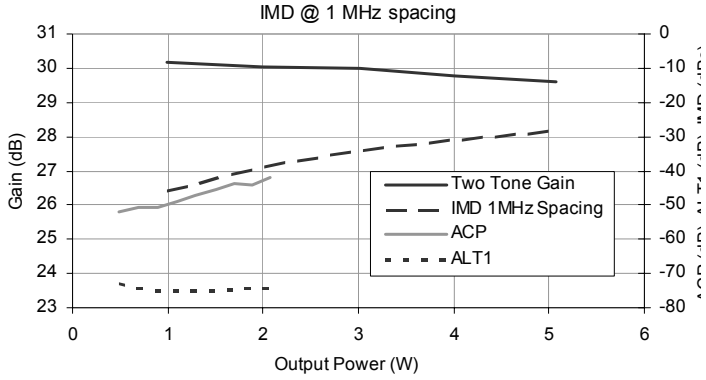
**Note 1:**
The internal generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be provided with AGC external to the module.

**Note 2:**
Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

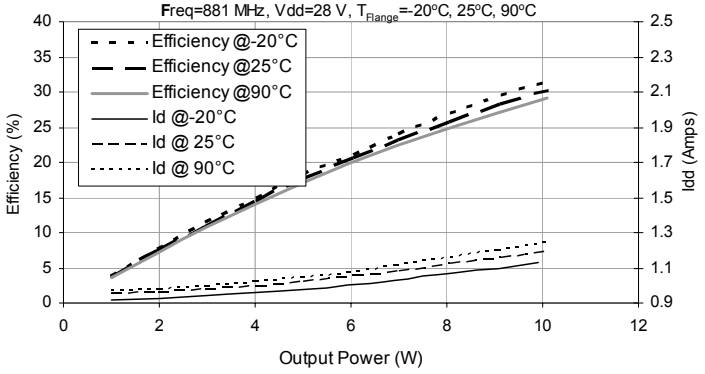
**Note 3:**
This module was designed to have it's leads hand soldered to an adjacent PCB. The maximum soldering iron tip temperature should not exceed 700° C, and the soldering iron tip should not be in direct contact with the lead for longer than 10 seconds. Refer to app note AN054 (www.sirenza.com) for further installation instructions.

## Typical Performance Curves

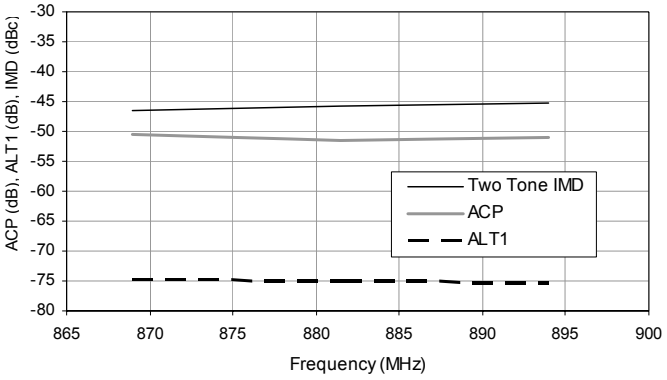
**Gain, IMD, ACP, ALT1 vs. Output Power**
Freq=881 MHz, Vdd=28V, $T_{Flange}$=25°C, IS-95
ADJ BW=30KHz @ 750 KHz spacing
ALT1 BW=30KHz @1980 KHz spacing
IMD @ 1 MHz spacing



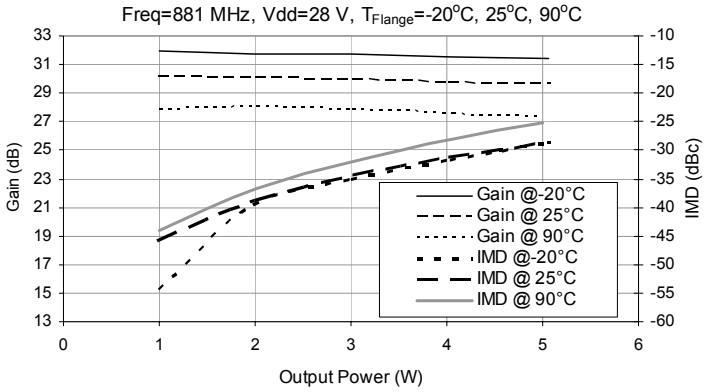

**Efficiency and Idd vs. Output Power and Temperature**
Freq=881 MHz, Vdd=28 V, $T_{Flange}$=-20°C, 25°C, 90°C



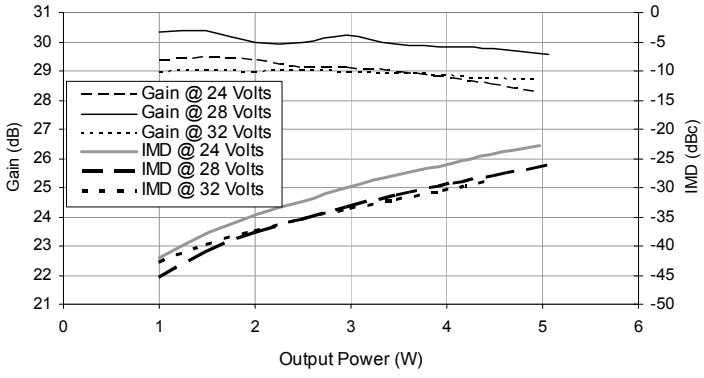

**Two Tone IMD, ACP, ALT1 vs. Frequency**
Output Power=1 Watt, Vdd=28 V, $T_{Flange}$=25°C IS95 standard,
channel BW= 1.23 MHz, ADJ BW= 30 KHz@ 750 KHz spacing.
ALT1 BW= 30 KHz@1980 KHz spacing. IMD@1 MHz spacing.



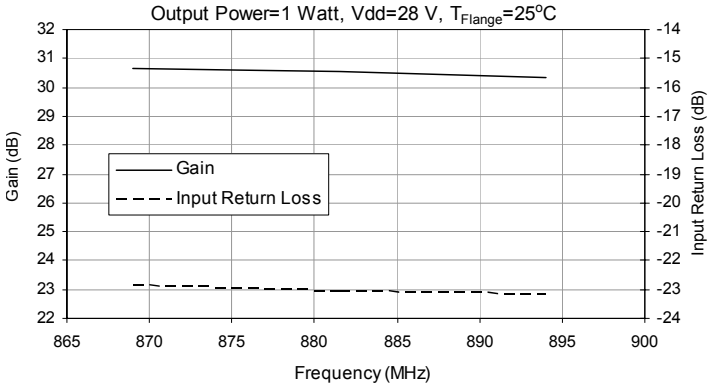

**Gain and IMD vs. Output Power and Temperature**
Freq=881 MHz, Vdd=28 V, $T_{Flange}$=-20°C, 25°C, 90°C



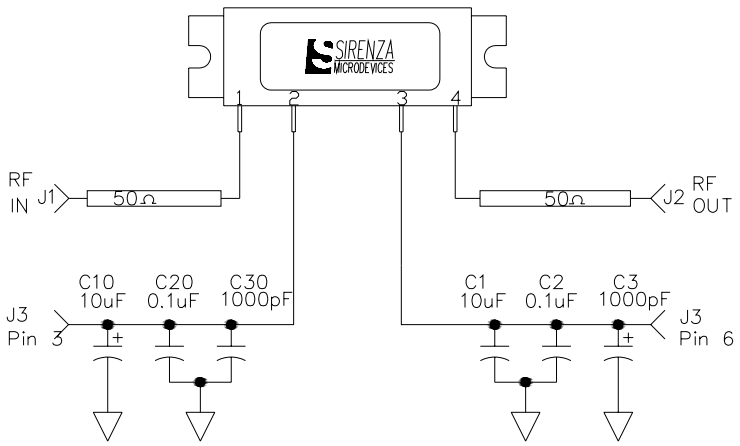

Gain and IMDs vs. Output Power and Voltage
Freq=881 and 882 MHz, Vdd=24 V, 28 V, 32 V
$T_{Flange}$=25°C




**Gain and Input Return Loss vs. Frequency**
Output Power=1 Watt, Vdd=28 V, $T_{Flange}$=25°C



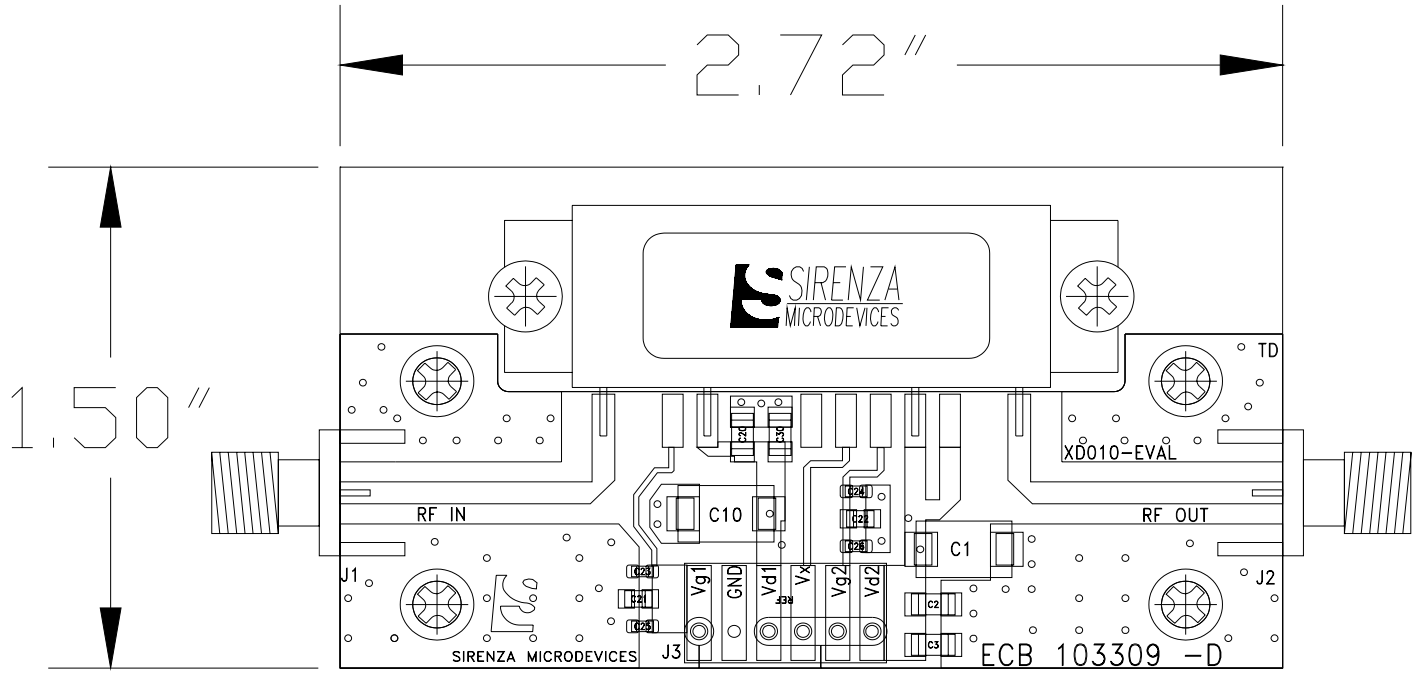
## Test Board Schematic with module connections shown




## Test Board Bill of Materials

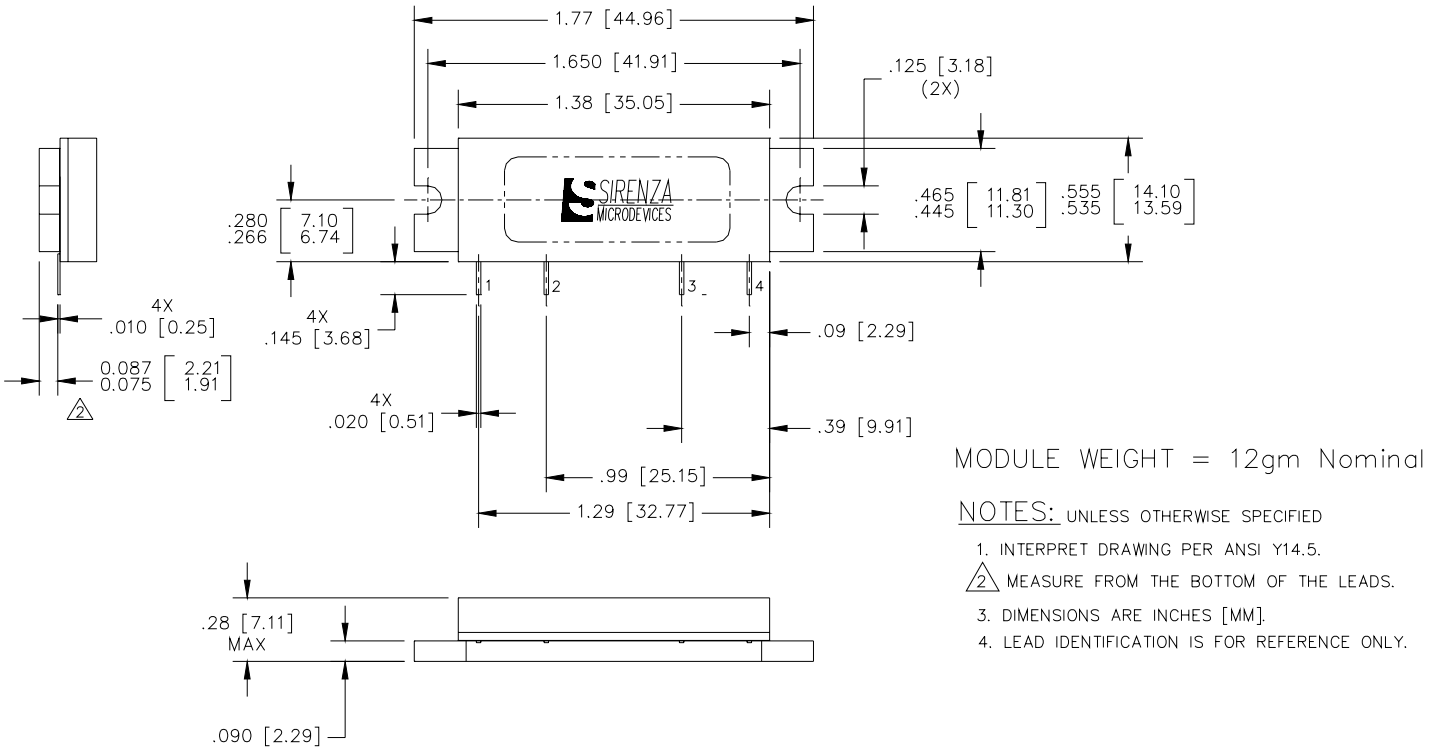
| Component | Description | Manufacturer |
|---|---|---|
| PCB | Rogers 4350, $\varepsilon_r$=3.5 Thickness=30mils | Rogers |
| J1, J2 | SMA, RF, Panel Mount Tab W / Flange | Johnson |
| J3 | MTA Post Header, 6 Pin, Rect-angle, Polarized, Surface Mount | AMP |
| C1, C10 | Cap, 10$\mu$F, 35V, 10%, Tant, Elect, D | Kemet |
| C2, C20 | Cap, 0.1$\mu$F, 100V, 10%, 1206 | Johanson |
| C3, C30 | Cap, 1000pF, 100V, 10%, 1206 | Johanson |
| C25, C26 | Cap, 68pF, 250V, 5%, 0603 | ATC |
| C21, C22 | Cap, 0.1$\mu$F, 100V, 10%, 0805 | Panasonic |
| C23, C24 | Cap, 1000pF, 100V, 10%, 0603 | AVX |
| Mounting Screws | 4-40 X 0.250” | Various |

## Test Board Layout

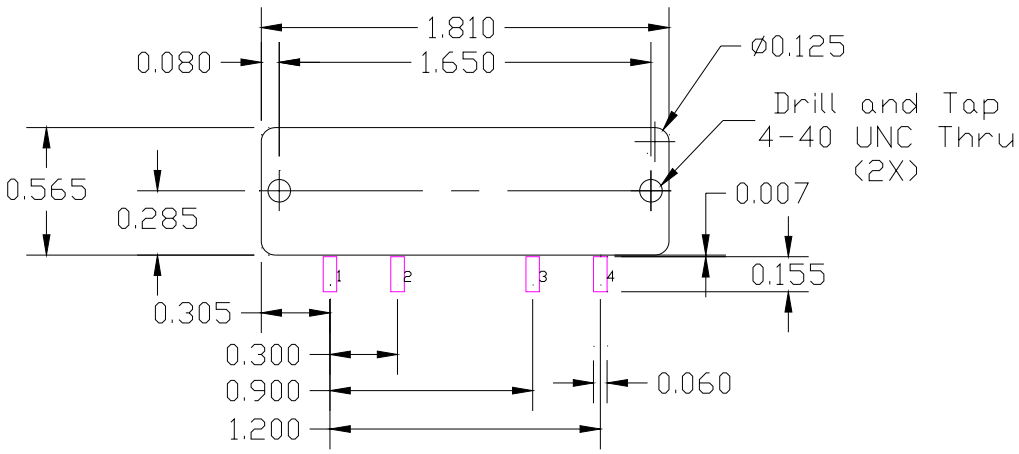



**To receive Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture, contact applications support at support@sirenza.com. Data sheet for evaluation circuit (XD010-EVAL) available from Sirenza website.**

## Package Outline Drawing




## Recommended PCB Cutout and Landing Pads for the D4F Package




**Note 3:** Dimensions are in inches

Refer to Application note AN-060 “Installation Instructions for XD Module Series” for additional mounting info. App note availbale at at www.sirenza.com