XIO2213A PCI Express to 1394b OHCI with 3-Port PHY

FEATURES

- **Full x1 PCI Express Throughput**
- **Fully Compliant with *PCI Express Base Specification*, Revision 1.1**
- **Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended Reference Clock**
- **Fully supports provisions of IEEE P1394b-2002**
- **Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000**
- **Fully Compliant with *1394 Open Host Controller Interface Specification*, Revision 1.1 and Revision 1.2 draft**
- **Three IEEE Std 1394b Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, 400M Bits/s, and 800M Bits/s**
- **Cable Ports Monitor Line Conditions for Active Connection To Remote Node**
- **Cable Power Presence Monitoring**
- **EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric**
- **Support for D1, D2, $D3_{hot}$**
- **Active State Link Power Management Saves Power When Packet Activity on the PCI Express™ Link is Idle, Using Both L0s and L1 States**
- **Eight 3.3-V, Multifunction, General-Purpose I/O Terminals**

DESCRIPTION

The Texas Instruments XIO2213A is a PCI Express to PCI translation bridge where the PCI bus interface is internally connected to a 1394b open host controller link-layer controller with a three-port 1394b PHY. The PCI-Express to PCI translation bridge is fully compatible with the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394b OHCI controller function is fully compatible with IEEE Standard 1394b and the latest *1394 Open Host Controller Interface (OHCI)* Specification.

The XIO2213A simultaneously supports up to four posted write transactions, four non-posted transactions, and four completion transactions pending in each direction at any time. Each posted write data queue and completion data queue can store up to 8K bytes of data. The non-posted data queues can store up to 128 bytes of data.

The PCI Express interface supports a x1 link operating at full 250 MB/s packet throughput in each direction simultaneously. Also, the bridge supports the advanced error reporting capability including ECRC as defined in the *PCI Express Base Specification*, Revision 1.1. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency. If parity errors are detected, then packet poisoning is supported for both upstream and downstream operations.

The PCIe Power management (PM) features include active state link PM, PME mechanisms, and all conventional PCI D-states. If the active state link PM is enabled, then the link automatically saves power when idle using the L0s and L1 states. PM active state NAK, PM PME, and PME-to-ACK messages are supported. The bridge is compliant with the latest PCI Bus Power Management Specification and provides several low-power modes, which enable the host power system to further reduce power consumption

Eight general-purpose inputs and outputs (GPIOs), configured through accesses to the PCI Express configuration space, allow for further system control and customization.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The device provides physical write posting and a highly tuned physical data path for SBP-2 performance. The device is capable of transferring data between the PCI Express bus and the 1394 bus at 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s. The device provides three 1394 ports that have separate cable bias (TPBIAS).

As required by the *1394 Open Host Controller Interface Specification*, internal control registers are memory-mapped and nonprefetchable. This configuration header is accessed through configuration cycles specified by PCI Express, and it provides plug-and-play (PnP) compatibility.

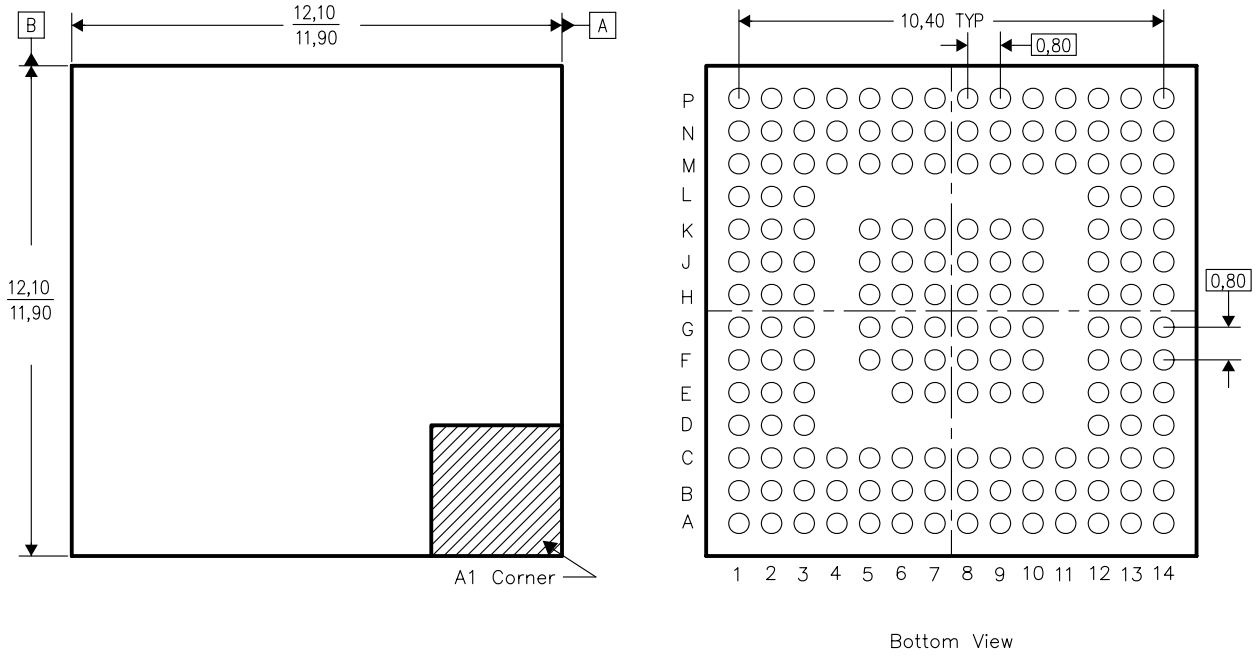
The PHY-layer provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. An optional external 2-wire serial EEPROM interface is provided to load the global unique ID for the 1394 fabric.

The XIO2213A requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. The power-down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL. Data bits to be transmitted through the cable ports are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbps (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

To ensure that the XIO2213A conforms to the IEEE Std 1394b-2002 standard, the BMODE terminal must be asserted. The BMODE terminal does not select the cable-interface mode of operation. The BMODE terminal selects the internal PHY section-LLC section interface mode of operation and affects the arbitration modes on the cable. BMODE must be pulled high during normal operation.

Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They can be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the XIO2213A, this bit can only be set by a write to the PHY register set. If a node is to be a contender for IRM or BM, the node software must set this bit in the PHY register set.

ZAY (S–PBGA–N167) PLASTIC BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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