8.5-11.0 GHz GaAs MMIC Power Amplifier

Mimix ASIA

August 2007 - Rev 03-Aug-07

XP1006-BD

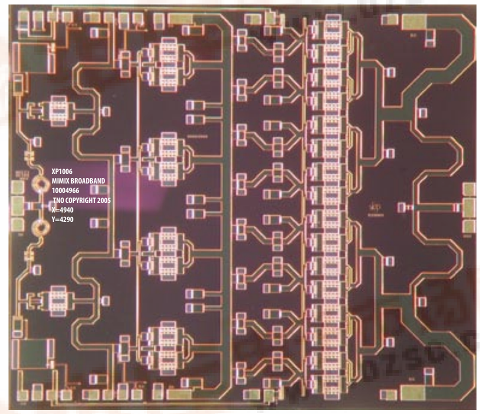
Features

- X-Band 10W Power Amplifier
- 21.0 dB Large Signal Gain
- +40.0 dBm Saturated Output Power
- 30% Power Added Efficiency
- On-chip Gate Bias Circuit
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010

General Description

Mimix Broadband's three stage 8.5-11.0 GHz GaAs MMIC power amplifier has a large signal gain of 21.0 dB with a +40.0 dBm saturated output power and also includes on-chip gate bias circuitry. This MMIC uses Mimix Broadband's 0.5µm GaAs PHEMT device model technology, and is based upon optical gate lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for radar applications.

Chip Device Layout



Absolute Maximum Ratings

Supply Voltage (Vd)	+9.0 VDC
Supply Current (Id)	4.5 A
Gate Bias Voltage (Vg)	+0.0 VDC
Input Power (Pin)	TBD
Storage Temperature (Tstg)	-65 to +165 ^{o}C
Operating Temperature (Ta)	-55 to MTTF Table[1]
Channel Temperature (Tch)	MTTF Table[1]

(1) Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.

Electrical Characteristics (Pulsed Mode F=10kHz, Duty Cycle=10%, T_A=25°C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	8.5	-	11.0
Input Return Loss (S11)	dB	-	15.0	-
Output Return Loss (S22)	dB	-	12.0	-
Large Signal Gain (S21)	dB	-	21.0	-
Gain Flatness (ΔS21)	dB	-	+/-0.5	-
Reverse Isolation (S12)	dB	-	60.0	-
Saturated Output Power (P_{SAT})	dBm	-	+40.0	-
Power Added Efficiency (PAE)	%	-	30	-
Drain Bias Voltage (Vd1,2,3)	VDC	-	+8.0	+9.0
Gate Bias Voltage (Vgg)	VDC	-6.0	-5.0	-4.0
Supply Current (Id) (Vd=8.0V, Vgg=-5.0V Typical)	A	-	4.2	4.5

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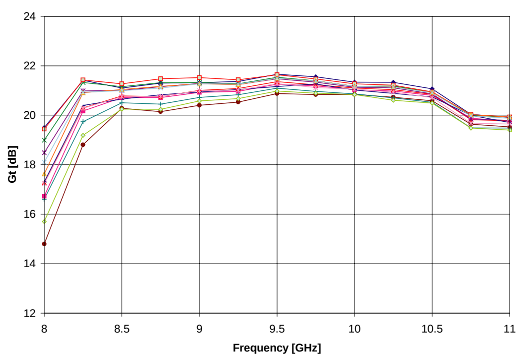
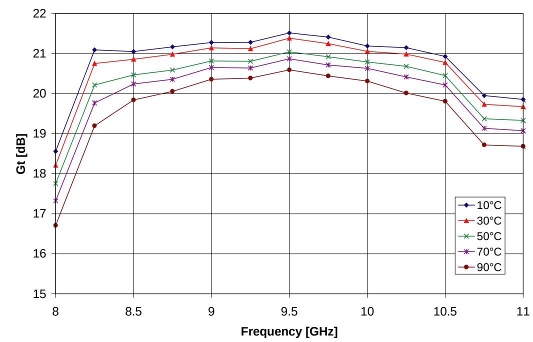
Power Amplifier Measurements (Pulsed Mode F=10kHz, Duty Cycle=10%, T_A=25°C)

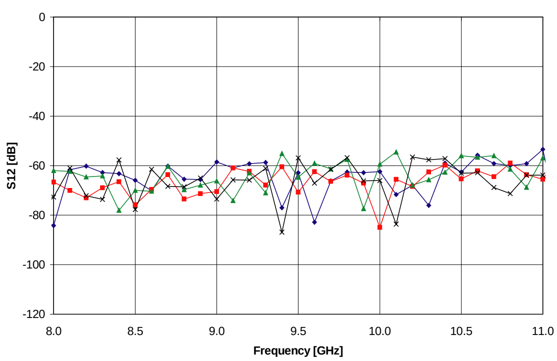
Large signal Gain (V_d=8V, V_{gg}=-5V, Ps=19dBm)



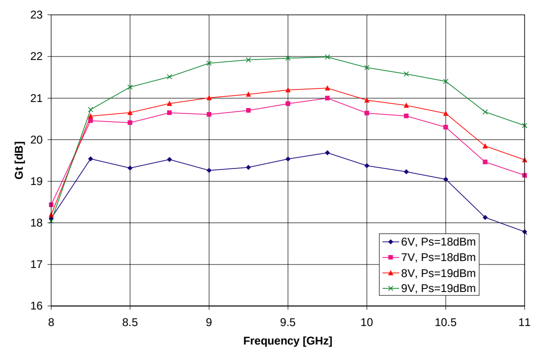
Large signal Gain



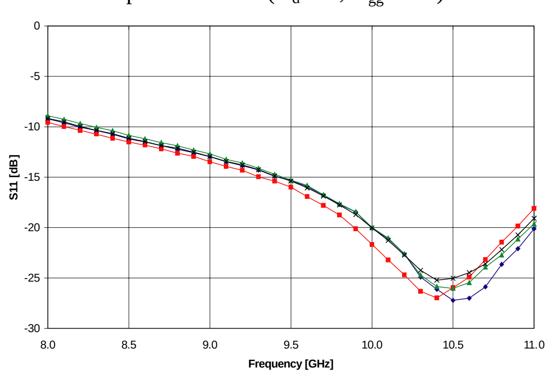
Reverse Isolation (V_d=8V, V_{gg}=-5V)



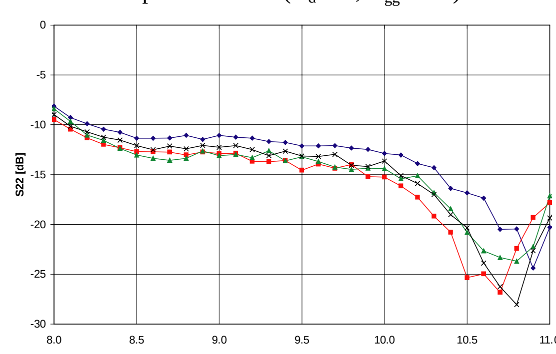
Large signal gain vs drain voltage (V_{gg}=-5V)



Input return loss (V_d=8V, V_{gg}=-5V)

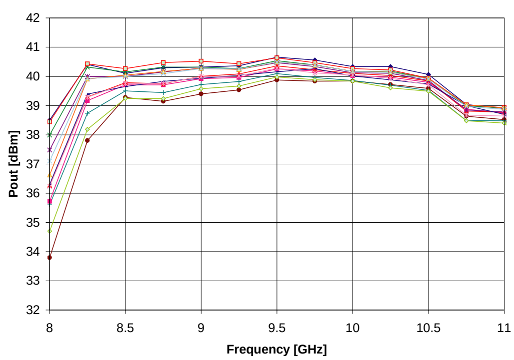


Output return loss (V_d=8V, V_{gg}=-5V)

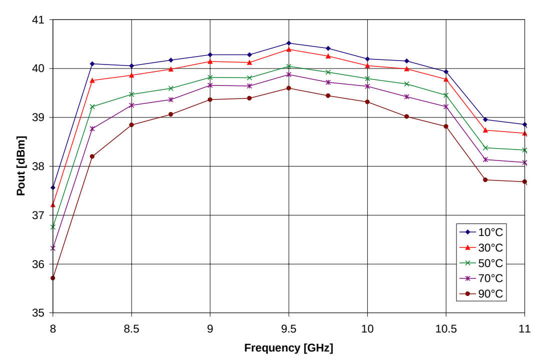


Power Amplifier Measurements (cont.)

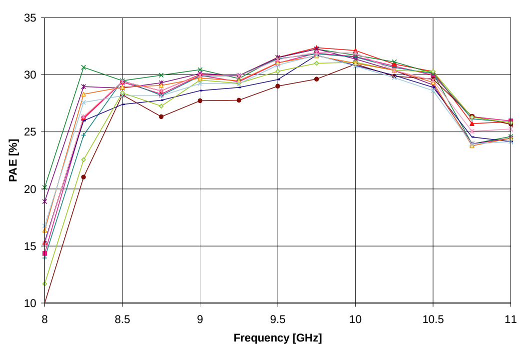
Output power (V_d=8V, V_{gg}=-5V, Ps=19dBm)



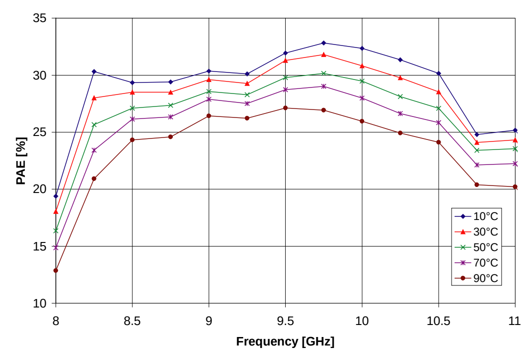
Output power



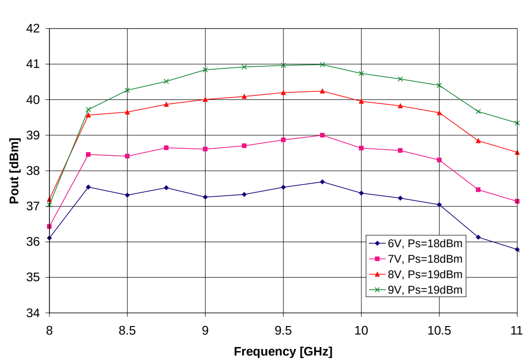
Power Added Efficiency (V_d=8V, V_{gg}=-5V, Ps=19dBm)



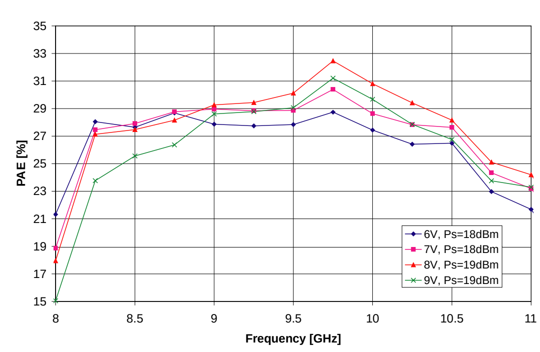
Power Added Efficiency



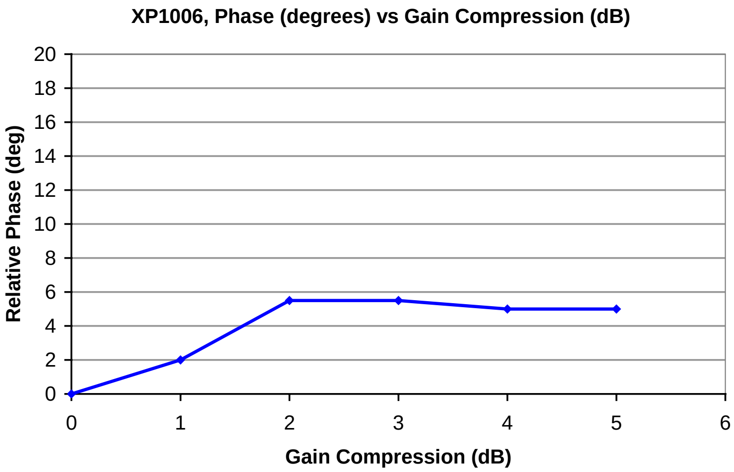
Output power vs drain voltage (V_{gg}=-5V)



Power added efficiency vs drain voltage (V_{gg}=-5V)



Power Amplifier Measurements (cont.)



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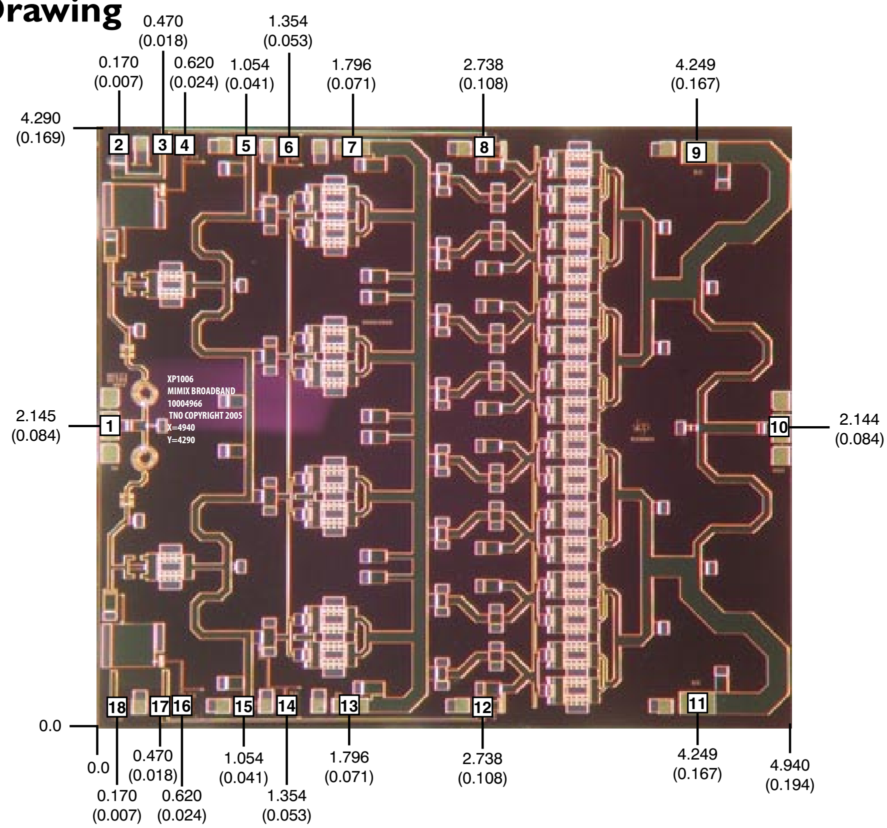
Mechanical Drawing



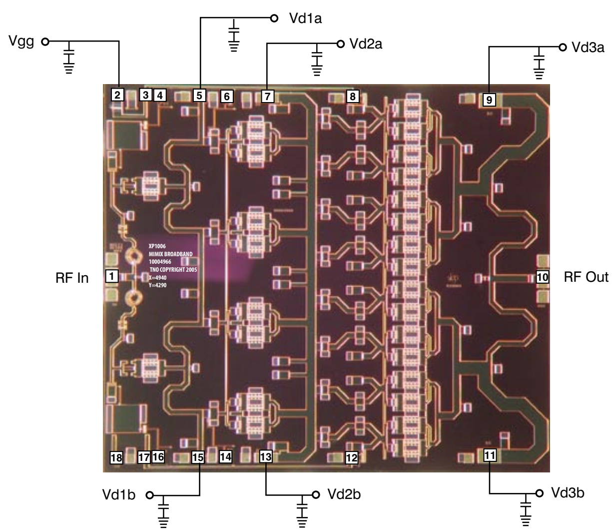
(Note: Engineering designator is I0004966)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 13.136 mg.

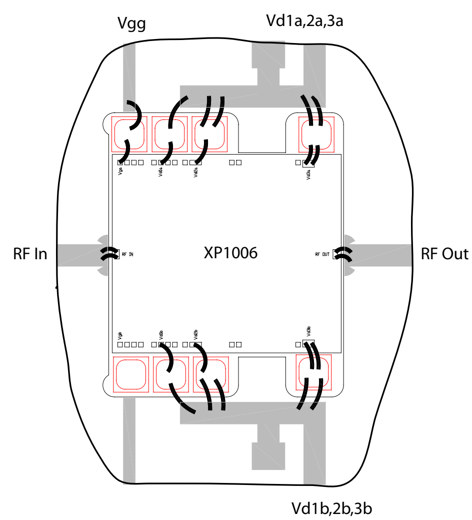
Bond Pad #1 (RF In)
Bond Pad #2 (Vgg)
Bond Pad #3 (Vg)
Bond Pad #4 (Vg1a)
Bond Pad #5 (Vd1a)
Bond Pad #6 (Vg2a)
Bond Pad #7 (Vd2a)
Bond Pad #8 (Vg3a)
Bond Pad #9 (Vd3a)
Bond Pad #10 (RF Out)
Bond Pad #11 Vd3b)
Bond Pad #12 (Vg3b)
Bond Pad #13 (Vd2b)
Bond Pad #14 (Vg2b)
Bond Pad #15 (Vd1b)
Bond Pad #16 (Vg1b)
Bond Pad #17 (Vg)
Bond Pad #18 (Vgr)

Pad Locations	**Size**	
RF/DC Pads	[mm]	[inches]
RF In/Out	0.120x0.200	0.005x0.008
Vgg, Vg, Vg1a, Vd1a, Vg2a, Vg3a, Vg1b, Vd1b, Vg2b, Vg3b	0.100x0.100	0.004x0.004
Vd2a, Vd2b	0.250x0.100	0.010x0.004
Vd3a, Vd3b	0.247x0.153	0.010x0.006

Bias Arrangement



Bypass Capacitors - See App Note [2]



App Note [1] Biasing - This device is biased by applying Vd(1,2,3) = 8.0V with a total drain current I(total)=4.2 A. The gate bias can be applied in one of three ways by using either Vgg (Pin #2), Vgr (pin #18) or Vg (pin #3 or #17).

1) Vgg (pin #2) applies a scaled gate voltage to all FETs through a FET / resistor divider (Vto compensated) bias network. Applying -5V to Vgg (pin #2) will typically draw 4.2A with no further adjustment necessary. Wafer lot variation may result in some devices experiencing higher or lower drain currents than the typical 4.2A.

2) Vgr (pin #18) applies a scaled gate bias to all FETs through a resistive divider network. Applying -5V to Vgr (pin #18) will typically draw 4.2A, however, the gate bias will need to be actively adjusted to regulate the desired drain current.

3) Vg (pin #3 or pin #17) provides a direct gate bias input to all the MMIC stages. This method of biasing allows the user to control the total drain current, without the scaling factor. The typically gate bias for operation is -0.9V.

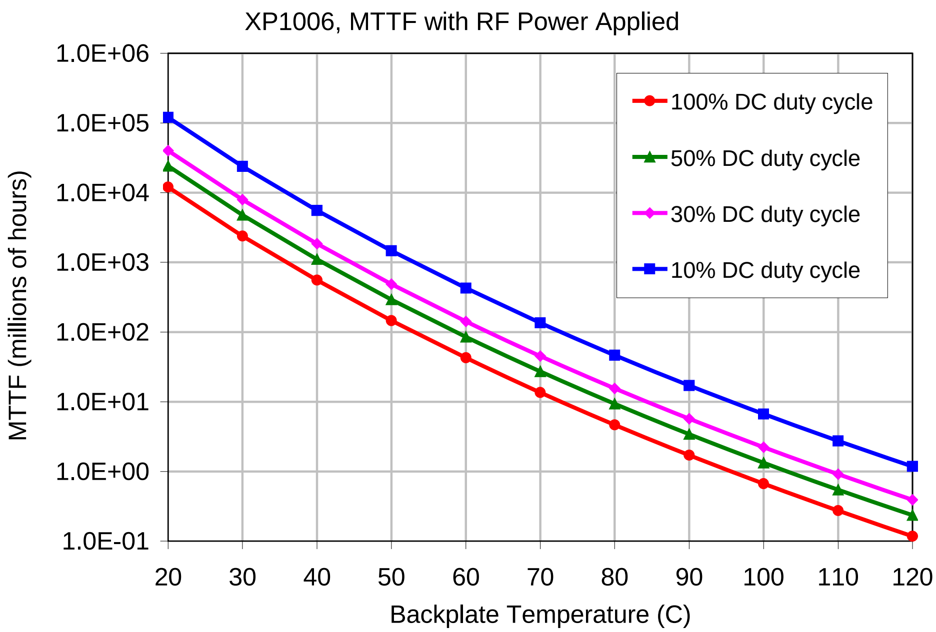
Make sure to sequence the applied voltage to ensure that negative gate bias is available before applying the positive drain supply.

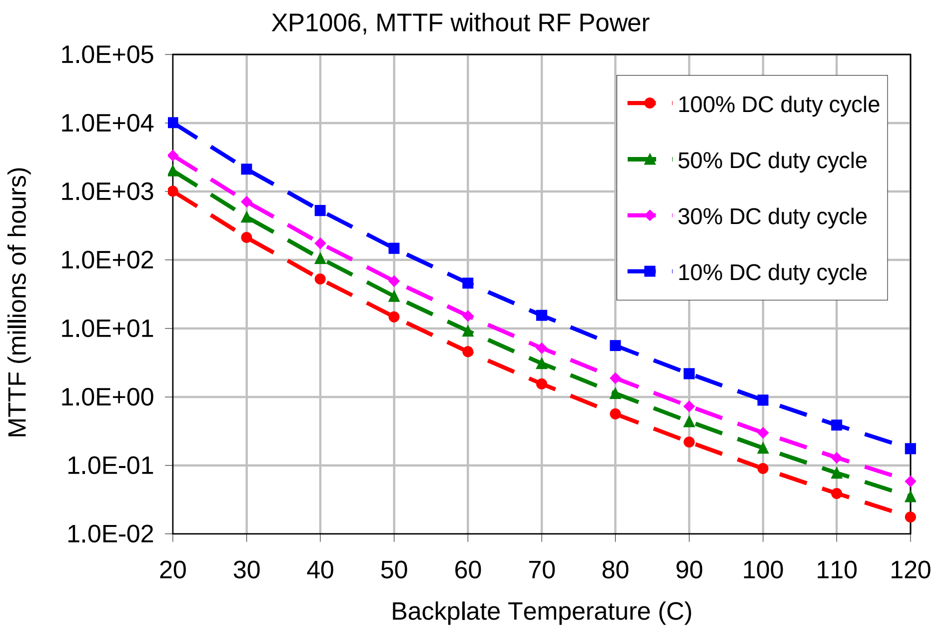
App Note [2] Bias Arrangement - Each DC pad (Vd1,2,3 and Vg1,2,3 or Vgg) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended.

App Note [3] Further Information - More application information is available on our website under Products -> Product Support -> Application Notes. Please refer to "Application of Mimix Broadband's X-Band, 10-Watt Power Amplifier MMIC" and "Epoxy Die Attach Considerations for HPA MMICs."

MTTF

MTTF is calculated from accelerated life-time data of single devices and assumes an isothermal back-plate.





Bias Conditions: Vd1=Vd2=Vd3=8.0V, Id(TOTAL)=4.2A

Handling and Assembly Information

CAUTION! - Mimix Broadband MMIC Products contain gallium arsenide (GaAs) which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- *Do not ingest.*
- *Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.*
- *Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.*

Life Support Policy - Mimix Broadband's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President and General Counsel of Mimix Broadband. As used herein: (1) Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. (2) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ESD - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

Die Attachment - GaAs Products from Mimix Broadband are 0.100 mm (0.004") thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the Mimix "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001[2] thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280 ºC (Note: Gold Germanium should be avoided). The work station temperature should be 310 ºC +/- 10 ºC. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

Ordering Information

Part Number for Ordering	**Description**
XP1006-BD-000V	"V" - vacuum release gel paks
XP1006-BD-EV1	XP1006 die evaluation module

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