



XRD6406

CMOS

6 MSPS, 10-Bit, High Speed
Analog-to-Digital Converter

FEATURES

- 10-Bit Resolution
- Sampling Rate to 6 MSPS
- DNL = ± 1 LSB, INL = ± 2 LSB
- Internal S/H Function
- Single 5V Power Supply
- V_{IN} DC Range: 0V to V_{DD}
- V_{REF} DC Range: 1V to V_{DD}
- Low Power: 65mW
- Three-State Digital Outputs
- Latch-Up Free
- Pin Compatible With: MP8784

APPLICATIONS

- Digital Color Copiers
- Precision CCDs and Scanners
- Digital Radio

June 1998-2

BENEFITS

- Simplified Analog Design
- Rugged
- Few External Components, no S/H Needed
- Reduced Board Space

GENERAL DESCRIPTION

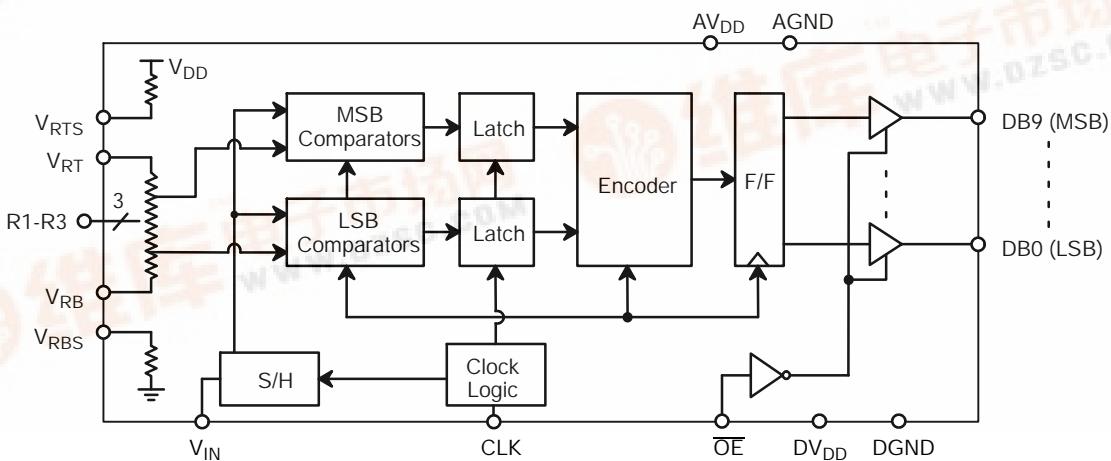
The XRD6406 is a 10-bit, 6 MSPS, Analog-to-Digital Converter for applications that require high speed and high accuracy. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The XRD6406 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the XRD6406 includes an on-chip S/H function that allows this part to digitize analog input signals between AGND and AV_{DD} .

The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 1.0V at V_{RB} and 4V at V_{RT} . Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD} . This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R3) can be used to externally trim any INL errors.

This device operates from a single 5V supply. Power consumption from a 5V supply is typically 65mW at $F_S=6MHz$.

SIMPLIFIED BLOCK DIAGRAM

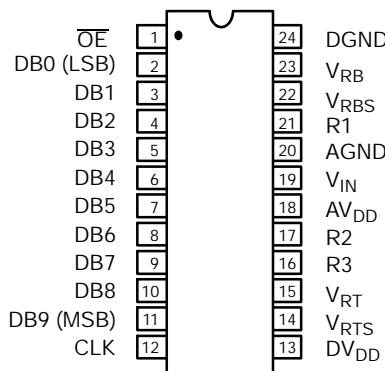


ORDERING INFORMATION

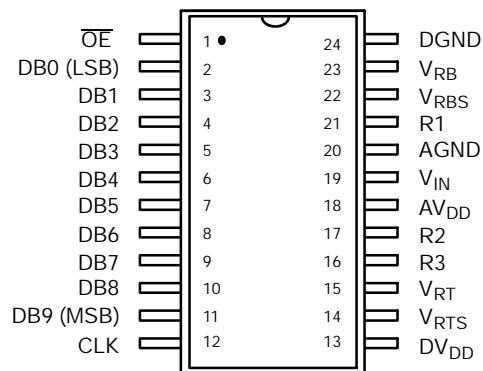
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	-40 to +85°C	XRD6406AIP	1	2
SOIC	-40 to +85°C	XRD6406AID	1	2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")



24 Pin SOIC (Jedec, 0.300")

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	OE	Output Enable
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	CLK	Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV _{DD}	Digital Power Supply
14	V _{RTS}	Top Internal Reference
15	V _{RT}	Top of Reference
16	R3	3/4 Reference Tap Point
17	R2	1/2 Reference Tap Point
18	AV _{DD}	Analog Power Supply
19	V _{IN}	Analog Input Voltage
20	AGND	Analog Ground
21	R1	1/4 Reference Tap Point
22	V _{RBS}	Bottom Internal Reference
23	V _{RB}	Bottom of Reference
24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5V$, $FS = 6MHz$ (50% Duty Cycle), $V_{RT} = 4.0$, $V_{RB} = 1.0$, $T_A = 25^\circ C$

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution Maximum Sampling Rate	FS	10 6			Bits MHz	
ACCURACY (A Grade)¹				± 1 ± 2	LSB LSB LSB LSB	
Differential Non-Linearity Integral Non-Linearity	DNL INL					Best Fit Line (Max INL – Min INL)/2
Zero Scale Error Gain Error	EZS EFS		10 6			
REFERENCE VOLTAGES						
Positive Ref. Voltage ^{2,3} Negative Ref. Voltage ^{2,3} Differential Ref. Voltage ^{2,3} Ladder Resistance Ladder Temp. Coefficient ² Top Internal Reference Bottom Internal Reference	V_{RT} V_{RB} V_{REF} R_L R_{TCO} V_{RTS} V_{RBS}	AGND 1.0	1400 2000 4 1	AV_{DD} AV_{DD}	V V V Ω ppm/°C V V	$V_{REF} = V_{RT} - V_{RB}$ V_{RT} connected to V_{RTS} & V_{RB} connected to V_{RBS}
ANALOG INPUT						
Input Bandwidth (-1 dB) ^{2,4} Input Voltage Range Input Capacitance (Sample) ^{2,5} Input Capacitance (Convert) ^{2,5} Aperture Delay ² Aperture Uncertainty ² (Jitter)	BW V_{IN} C_{IN} t_{AP} t_{AJ}	V_{RB}	25 25 7 25 50	V_{RT} 40 12 30	MHz V pF pF ns ps	
DIGITAL INPUTS						
Logical "1" Voltage Logical "0" Voltage DC Leakage Currents ^{2,6} CLK OE Input Capacitance ² Clock Timing (See Figure 1) Clock Period ² Rise & Fall Time ^{2,7} "High" Pulse Width ^{2,3} "Low" Pulse Width ^{2,3} Duty Cycle ^{2,3}	V_{IH} V_{IL} I_{IN} t_{R}, t_F t_{PWH} t_{PWL}	4	5 5 5 167 2 84 84 50	1	V V μA μA pF ns ns ns ns %	$V_{IN} = DGND$ to DV_{DD}
DIGITAL OUTPUTS						
Logical "1" Voltage Logical "0" Voltage 3-state Leakage Data Valid Delay Data Enable Delay Data 3-state Delay	V_{OH} V_{OL} I_{OZ} t_{DL} t_{DEN} t_{DHZ}	4.5	10 40 25 25	0.4	V V μA ns ns ns	$C_{OUT} = 15 pF$ $I_{LOAD} = 4mA$ $I_{SINK} = 4mA$ $V_{OUT} = DGND$ to DV_{DD}

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	Min	25°C Typ	Max	Units	Conditions
POWER SUPPLIES						
Operating Voltage (AV _{DD} , DV _{DD}) ^{8, 9} Current (AV _{DD} + DV _{DD})	V _{DD} I _{DD}	4.5	5 13	5.5 17	V mA	

Notes:

- 1 Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error (Figure 3.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 4.). Accuracy is a function of the sampling rate (FS).
- 2 Guaranteed. Not tested.
- 3 Specified values guarantee functionality, but INL & DNL specifications may not be met.
- 4 -1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
- 5 See V_{IN} equivalent circuit (Figure 8.). Switched capacitor analog input requires driver with low output resistance.
- 6 All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
- 7 Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.
- 8 The AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.
- 9 The AV_{DD} & DV_{DD} pins should be tied together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2, 3}

AV _{DD} to AGND	+7V	Storage Temperature	-65 to +150°C
V _{RT} & V _{RB}	V _{DD} +0.5 to GND -0.5V	Package Power Dissipation Rating to 75°C	
V _{IN}	V _{DD} +0.5 to GND -0.5V	PDIP, SOIC	1000mW
All Inputs	V _{DD} +0.5 to GND -0.5V	Derates above 75°C	14mW/°C
All Outputs	V _{DD} +0.5 to GND -0.5V	Lead Temperature (Soldering 10 seconds)	+300°C

Notes

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.
- 3 V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

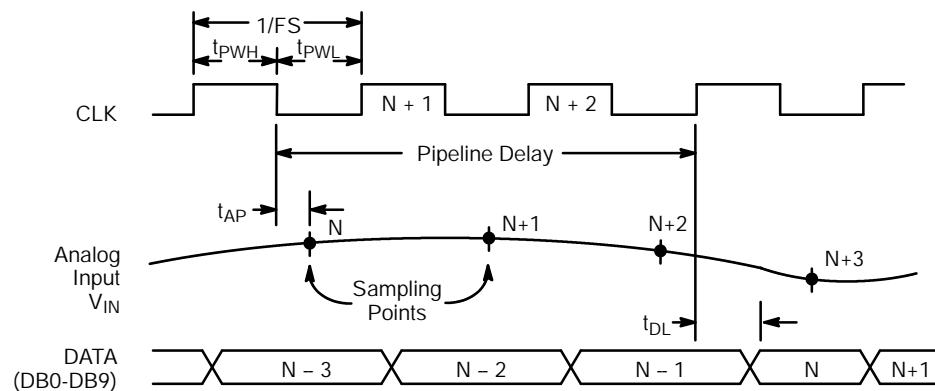


Figure 1. XRD6406 Timing Diagram

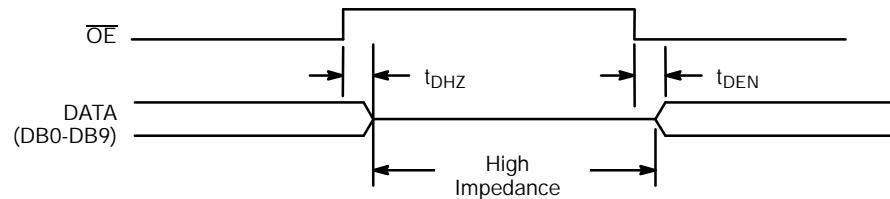
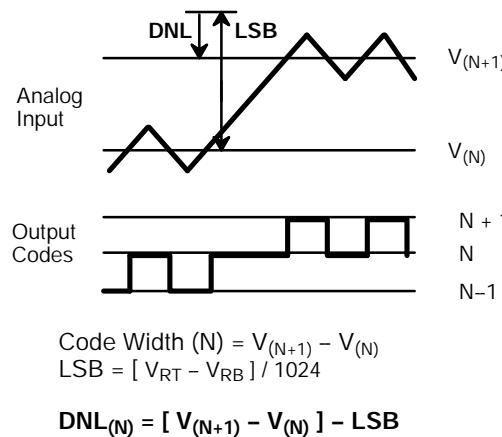


Figure 2. 3-State Timing Diagram

XRD6406

EXAR



$$\text{Code Width } N = V_{(N+1)} - V_{(N)}$$

$$\text{LSB} = [V_{RT} - V_{RB}] / 1024$$

$$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - \text{LSB}$$

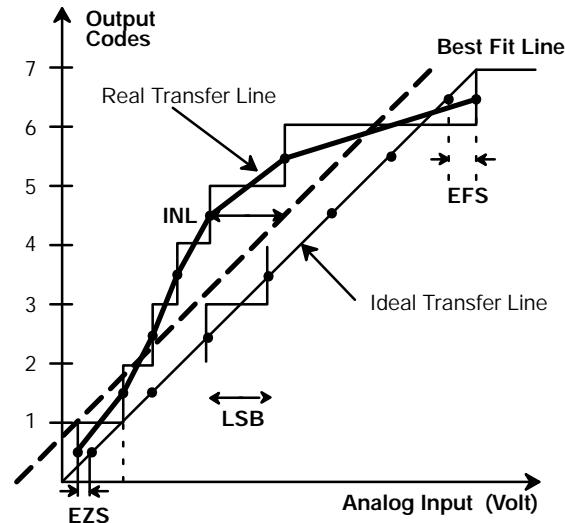


Figure 3. DNL Measurement

Figure 4. INL Error Calculation

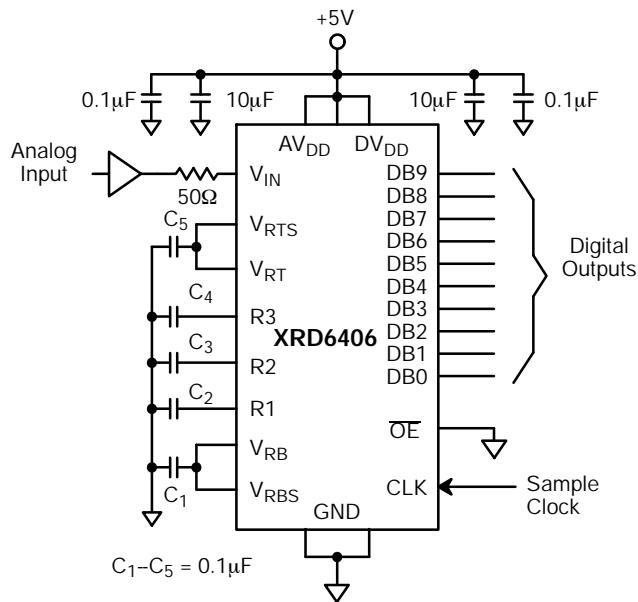


Figure 5. Typical Circuit Connections

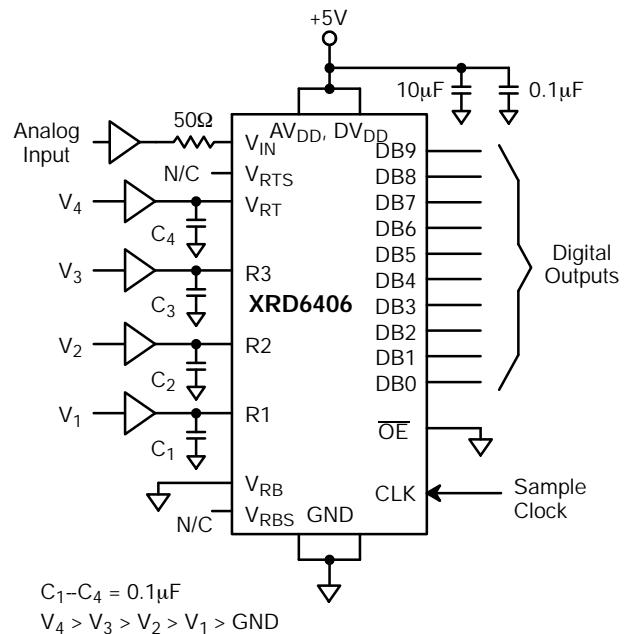


Figure 6. Creating a Piece Wise Linear Transfer Function

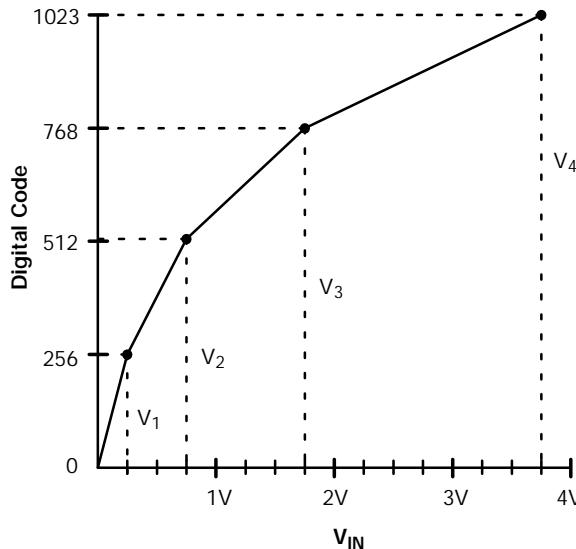


Figure 7. A Piece Wise Linear, Logarithmic Transfer Function

APPLICATION NOTES

Signals should not exceed AV_{DD} or DV_{DD} +0.5V or go below DGND or AGND -0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P-substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. Figure 8. shows an equivalent input circuit.

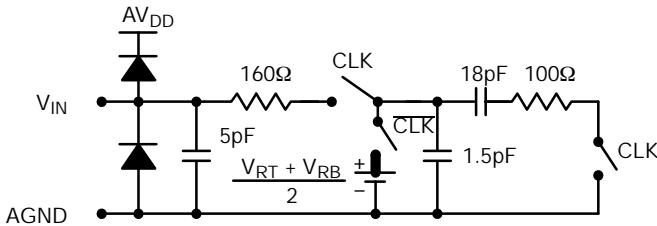


Figure 8. Equivalent Input Circuit

RTS & RBS Internal Bias Resistors

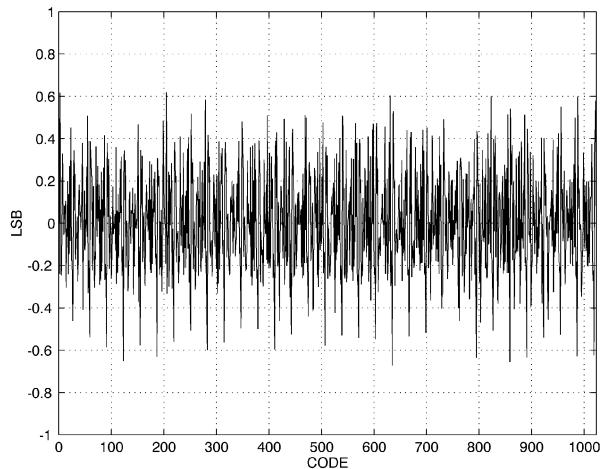
Two matched resistors are provided on the chip. These resistors can be used to generate on chip reference voltages. Each resistor has a value equal to 1/3 of the reference ladder resistor. By connecting RTS to V_{RT}, and connecting RBS to V_{RB}, the reference ladder will be biased to 1V at V_{RB} and 4V at V_{RT}.

If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

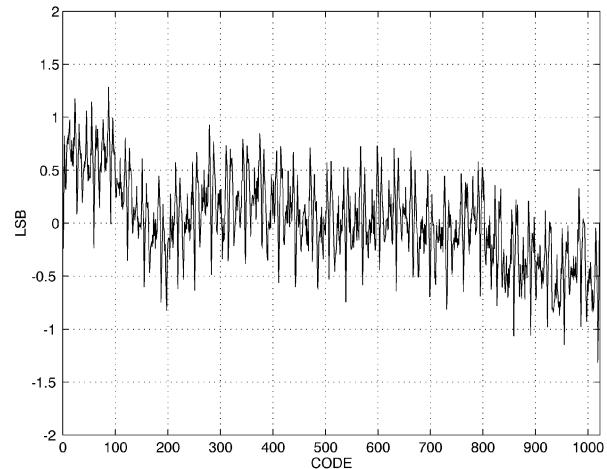
R1 thru R3 Reference Ladder Taps

These taps connect to every quarter point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to AGND; this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. A four segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins.

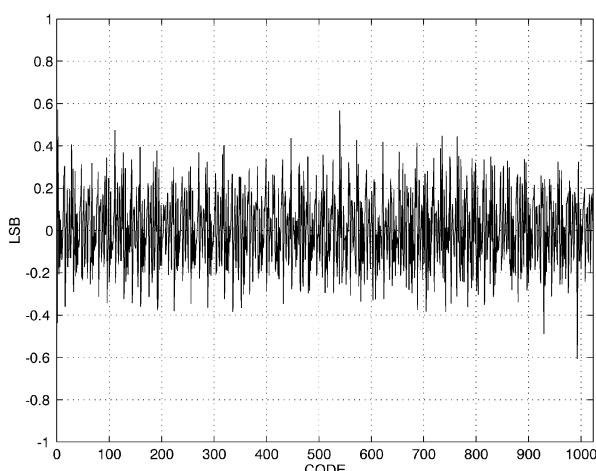
PERFORMANCE CHARACTERISTICS



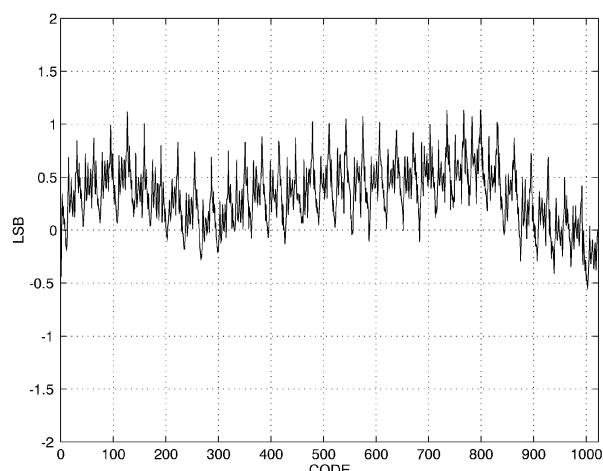
Graph 1. XRD6406, DNL @ 5MSPS
 $DV_{DD} = 5V$, $AV_{DD} = 5V$, $V_{RT} = 4V$, $V_{RB} = 1V$



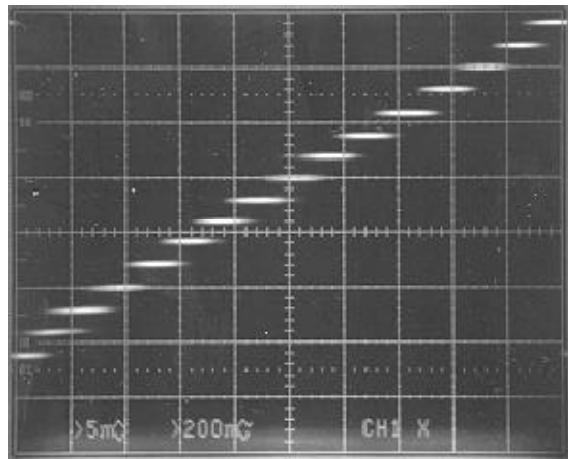
Graph 2. XRD6406, INL @ 5MSPS
 $DV_{DD} = 5V$, $AV_{DD} = 5V$, $V_{RT} = 4V$, $V_{RB} = 1V$



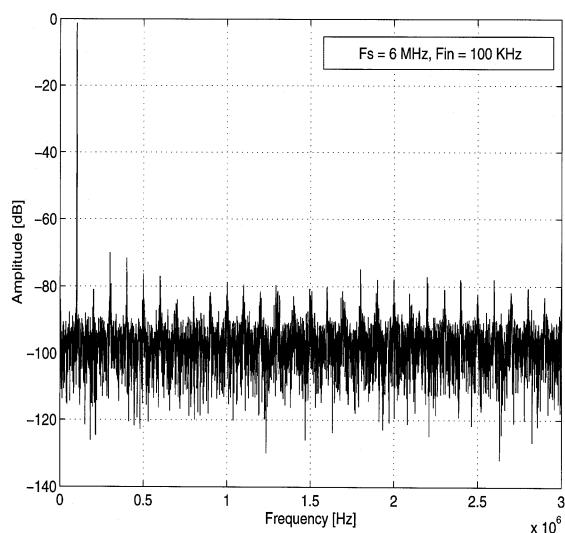
Graph 3. XRD6406, DNL @ 5MSPS
 $DV_{DD} = 3V$, $AV_{DD} = 5V$, $V_{RT} = 4.5V$, $V_{RB} = 0.5V$



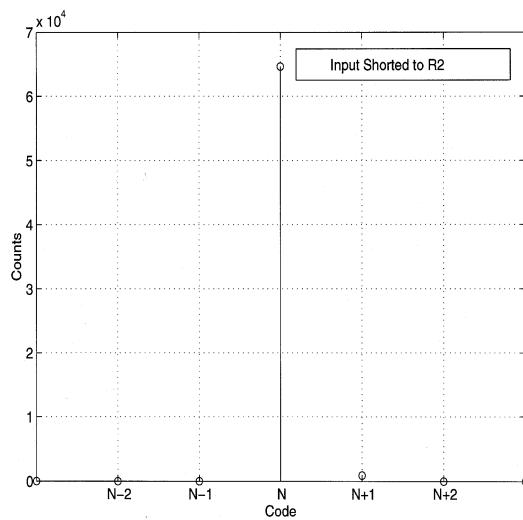
Graph 4. XRD6406, INL @ 5MSPS
 $DV_{DD} = 3V$, $AV_{DD} = 5V$, $V_{RT} = 4.5V$, $V_{RB} = 0.5V$



Graph 5. Crossplot Staircase Output
CLK = 6MSPS, V_{REF} = 4V



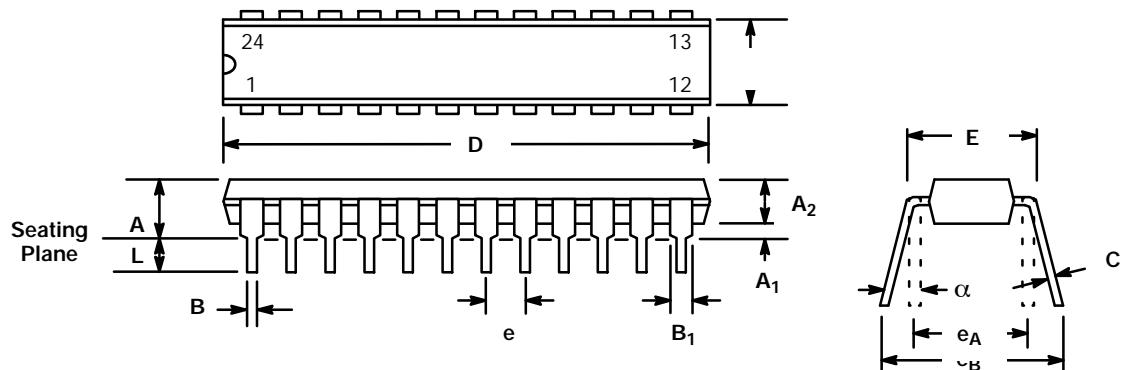
Graph 6. XRD6406 Spectral Performance



Graph 7. XRD6406 Output Noise Histogram

24 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

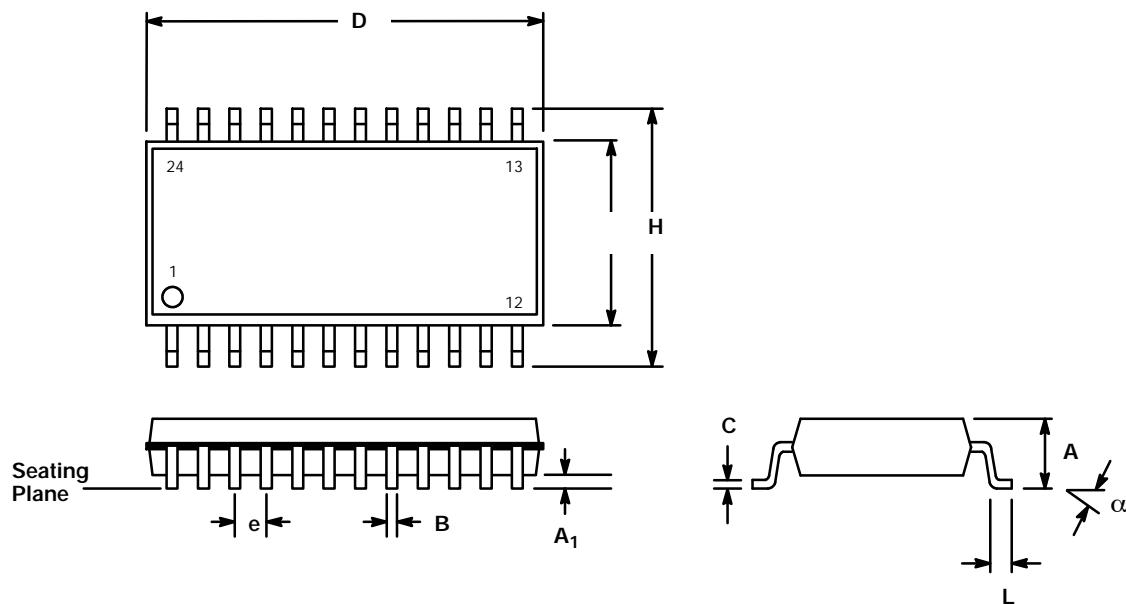


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.125	1.275	28.58	32.39
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)**

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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Datasheet June 1998

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