XRT94L31

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER

APRIL 2004 REV. P1.0.0

GENERAL DESCRIPTION

The XRT94L31 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L31 interfaces directly to the optical transceiver.

The XRT94L31 processes the section, line and path overhead in the SONET/SDH data stream. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L31 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L31 memory map or from external interface. A1, A2 framing pattern, C1 byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L31 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L31 provides 3 mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

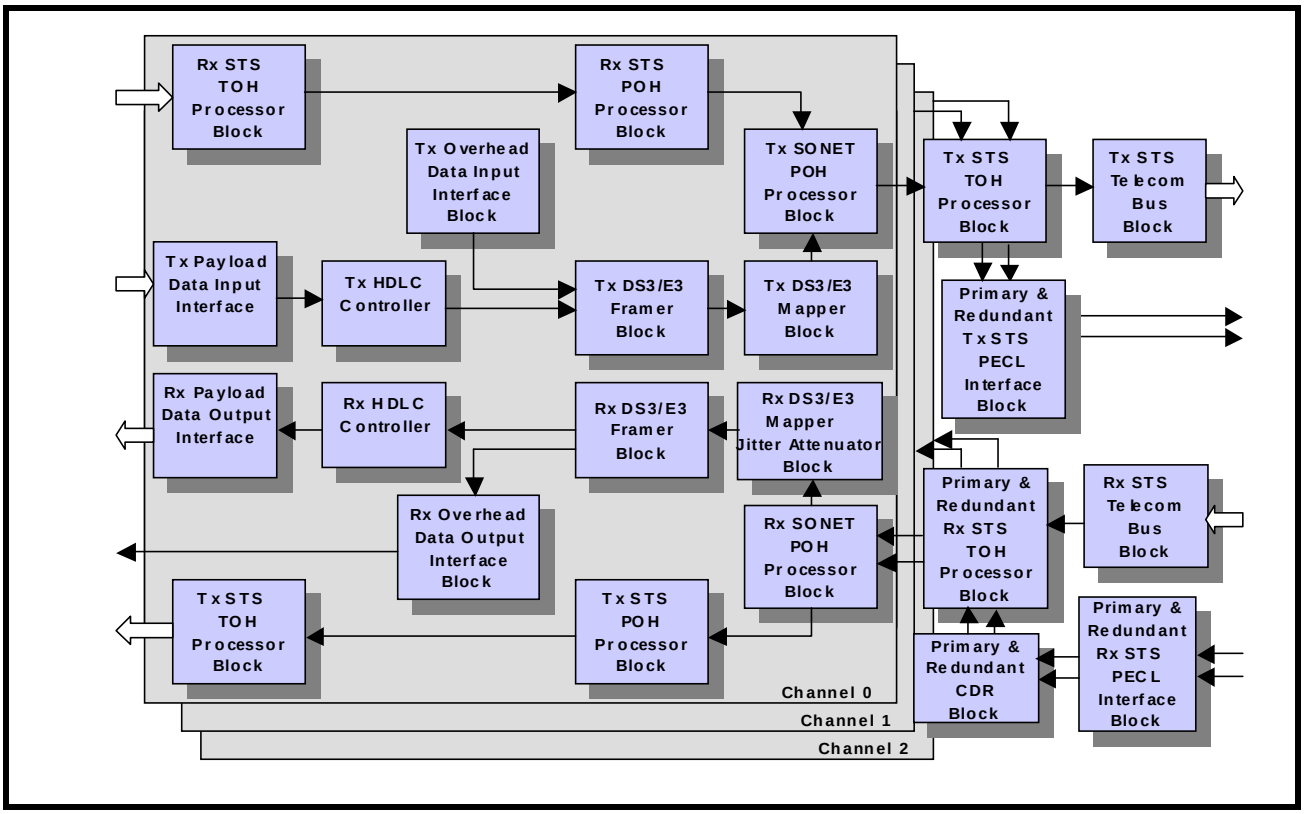
FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/ 19.44/77.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05UIpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149
- 8-bit microprocessor interface
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 504 Ball TBGA package

APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

BLOCK DIAGRAM OF THE XRT94L31



ORDERING INFORMATION

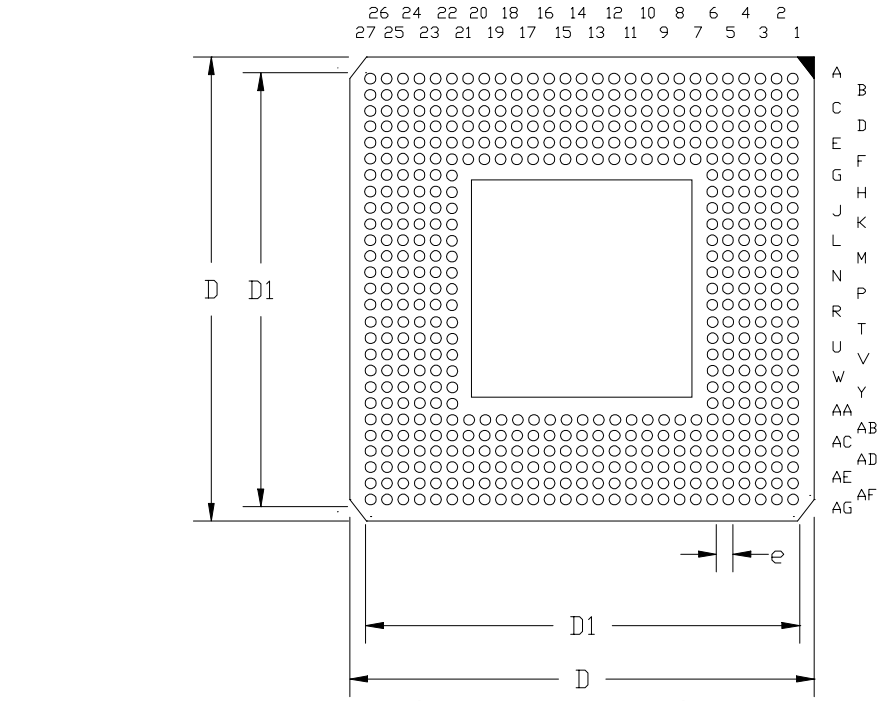
PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L31IB	35 x 35mm 504 Lead TBGA	-40°C to +85°C

PACKAGE OUTLINE DRAWING

504 TAPE BALL GRID ARRAY

(35 MM X 35 MM - TBGA)

BOTTOM VIEW



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.051	0.067	1.30	1.70
A1	0.020	0.028	0.50	0.70
A2	0.031	0.039	0.80	1.00
D	1.370	1.386	34.80	35.20
D1	1.300 BSC		33.02 BSC	
b	0.024	0.035	0.60	0.90
e	0.050 BSC		1.27 BSC	
P	0.006	0.012	0.15	0.30

NOTES

NOTICE

Datasheet April 2004.