



XR-L567

Micropower Tone Decoder

GENERAL DESCRIPTION

The XR-L567 is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the XR-L567 can replace the popular 567-type decoder with only minor component value changes. The XR-L567 offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4 mW at 5 volts. It operates over a wide frequency band of 0.01 Hz to 60 kHz and contains a logic compatible output which can sink up to 10 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

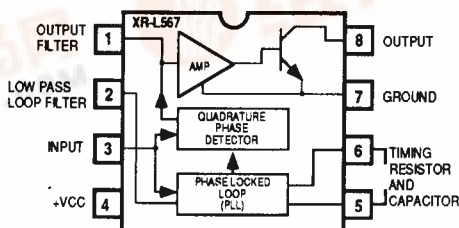
FEATURES

- Very Low Power Dissipation (≈ 4 mW at 5V).
- Bandwidth Adjustable from 0 to 14%.
- Logic Compatible Output with 10 mA Current Sinking Capability
- Highly Stable Center Frequency.
- Center Frequency Adjustable from 0.01 Hz to 60 kHz.
- Inherent Immunity to False Signals.
- High Rejection of Out-of-Band Signals and Noise.
- Frequency Range Adjustable Over 20:1 Range by External Resistor.

APPLICATIONS

Battery Operated Tone Detection
Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Storage Temperature	-65°C to + 150°C
Rev-A	

SYSTEM DESCRIPTION

The XR-L567 monolithic circuit consists of a phase detector low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependant upon the circuitry here. Pin 4 is + VCC (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

The XR-L567 is pin-for-pin compatible with the standard XR-567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load

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ELECTRICAL PERFORMANCE CHARACTERISTICS - XR-L567

TEST	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNIT	GROUP A SUBGROUP
				MIN	MAX		
Supply Current Quiescent	Icc	Vcc = +5V	TA = +25°C -55°C ≤ TA ≤ +125°C		1000 1000	μA μA	1 2,3
Supply Current Quiescent	Icc	Vcc = +8V	TA = +25°C		2000	μA	1
Supply Current Activated	Icc	Vcc = +5V	TA = +25°C -55°C ≤ TA ≤ +125°C		1400 2000	μA μA	1 2,3
Highest Center Frequency	Fc		TA = +25°C -55°C ≤ TA ≤ +125°C	10 10		KHz KHz	9 10,11
Center Frequency Drift with Supply	DRFT	4.75V ≤ Vcc ≤ 8V	TA = +25°C -55°C ≤ TA ≤ +125°C		2.0 3.0	%/V %/V	9 10,11
Output Saturation Voltage	VSAT	Ic = 2 mA Vin = 25 mVrms Vcc = +5V	TA = +25°C -55°C ≤ TA ≤ +125°C		0.4 0.4	V V	1 2,3
Output Saturation Voltage	VSAT	Ic = 10 mA Vin = 25 mVrms Vcc = +5V	TA = +25°C -55°C ≤ TA ≤ +125°C		0.6 0.6	V V	1 2,3
Output Leakage Current	IOL	Vin = 7.5 mVrms Vcc = 15V	TA = +25°C -55°C ≤ TA ≤ +125°C		25 25	μA μA	1 2,3
Largest No Output Input Voltage	VIL	Vcc = +5V	TA = +25°C -55°C ≤ TA ≤ +125°C	10 10		mVrms mVrms	4 5,6
Smallest Detectable Input Voltage	Vis		TA = +25°C -55°C ≤ TA ≤ +125°C		25 25	mVrms mVrms	4 5,6
Largest Detection Bandwidth	LDBW		TA = +25°C -55°C ≤ TA ≤ +125°C	10 10	18 20	% %	4 5,6
Largest Detection Bandwidth Skew	SKEW		TA = +25°C -55°C ≤ TA ≤ +125°C		3.0 3.0	% %	4 5,6