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YAMAHA

YDA138

D-3

STEREO 10W DIGITAL AUDIO POWER AMPLIFIER

■Overview

YDA138 (D-3) is a high efficient digital audio power amplifier IC that operates with a single 12V power supply.
An audio power amplifier with a maximum output of 10W (R_L=8Ω)×2ch or 20W (R_L=4Ω)×1ch can be configured with one chip.
YDA138 has a "Pure Pulse Direct Speaker Drive Circuit" which directly drives speakers while reducing distortion of pulse output signal and reducing noise on the signal, and realizes the highest standard low distortion rate characteristics and low noise characteristics as 10W-class of output digital amplifier IC.
In addition, circuit design with fewer external parts can be made depend on the condition of use because corresponds to filter less.
YDA138 has 50mW (R_L=32Ω)×2ch Class AB headphone amplifiers.
YDA138 provides Over-current protection function for speaker output terminals, IC thermal protection function, POP noise reduction function, and AM interference measures function as well as power-down function and output mute function.

■Features

Digital Amplifier

- Continuous maximum output
  10 W×2ch @V_{DDP}=12.0V, R_L=8Ω, THD+N=10%
  20 W×1ch @V_{DDP}=12.0V, R_L=4Ω, THD+N=10%
- Efficiency
  88 % @V_{DDP}=12.0V, R_L=8Ω, Po=10W
- Distortion Rate (THD+N)
  0.02 % @V_{DDP}=12.0V, R_L=8Ω, Po=1.0W
- S/N Ratio
  103dB @V_{DDP}=12.0V, R_L=8Ω, Po=10W, VOL[1:0]=H,H
- Channel Separation
  -70dB @V_{DDP}=12.0V, R_L=8Ω, VOL[1:0]=H,H

Class AB Headphone Amplifier

- Maximum output
  50mW×2ch @V_{DDP}=12.0V, R_L=32Ω, THD+N=10%
- Distortion Rate(THD+N)
  0.01 % @V_{DDP}=12.0V, R_L=32Ω, P_{ho}=30mW
- S/N Ratio
  95dB @V_{DDP}=12.0V, R_L=32Ω, P_{ho}=20mW, VOL[1:0]=H,H

Others

- Operating power supply range
  9.0V to 13.5V
- Multi-channel synchronizing operation by Master/Slave switching function
- Carrier frequency switching function
  524kHz/466kHz
- Sleep function with SLEEPN terminal
- Output muting function with MUTEN terminal
- Over-current protection function
- Thermal protection function
- Clock stop detection function
- Pop noise reduction function
- AM interference measures function
- Analog input/BTL (Bridge-Tied Load) output
- 42-pin plastic SSOP
  Pin lead plating with Pd free (YDA138-EZ)

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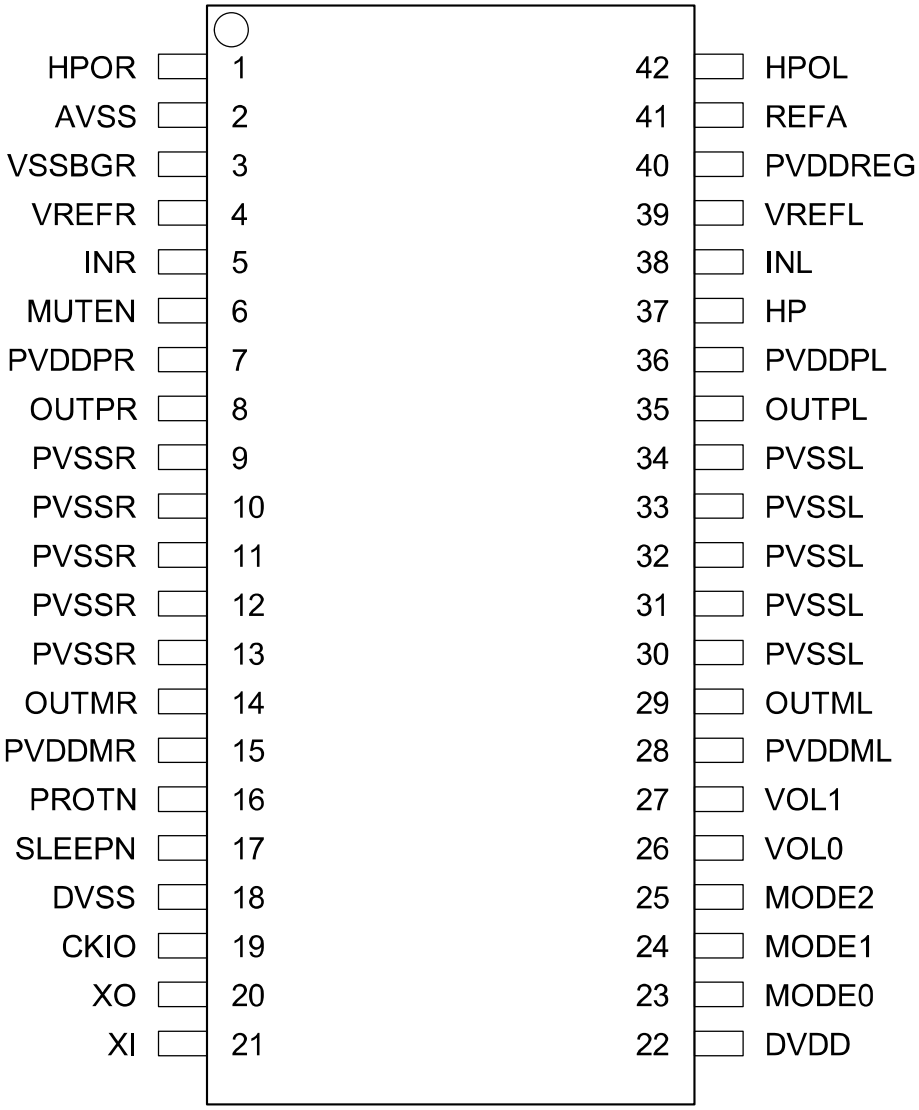
■Terminal configuration



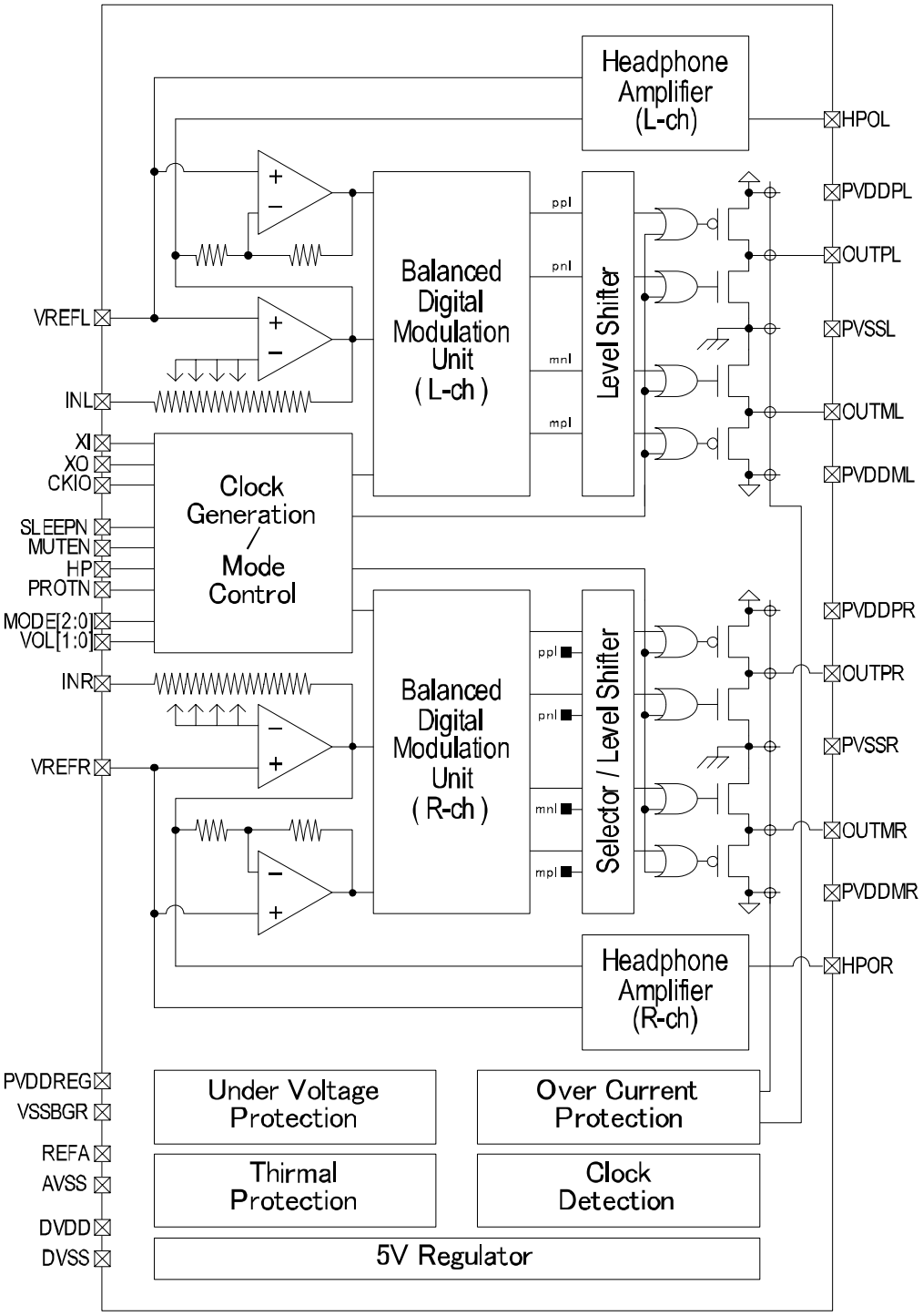
<42-pin SSOP Top View>

■Terminal function

No.	Name	I/O	Function	Voltage tolerance
1	HPOR	O	R-ch Headphone Output terminal	LV
2	AVSS	Pow	5V Analog Ground terminal	LV
3	VSSBGR	Pow	Ground terminal for Reference Voltage Supply	LV
4	VREFR	O	R-ch Reference Voltage terminal (with external capacitor)	LV
5	INR	I	R-ch Analog Signal Input terminal	LV
6	MUTEN	I	Mute Control terminal	LV
7	PVDDPR	Pow	R-ch 12V-line VDD terminal	HV
8	OUTPR	O	R-ch Positive Side Output terminal	HV
9	PVSSR	Pow	R-ch 12V-line VSS terminal	HV
10	PVSSR	Pow	R-ch 12V-line VSS terminal	HV
11	PVSSR	Pow	R-ch 12V-line VSS terminal	HV
12	PVSSR	Pow	R-ch 12V-line VSS terminal	HV
13	PVSSR	Pow	R-ch 12V-line VSS terminal	HV
14	OUTMR	O	R-ch Negative Side Output terminal	HV
15	PVDDMR	Pow	R-ch 12V-line VDD terminal	HV
16	PROTN	O	Warning Signal Output terminal (O/D)	HV
17	SLEEPN	I	Sleep Control terminal	HV
18	DVSS	Pow	Digital Ground terminal	LV
19	CKIO	I/O	Clock Input/Output terminal	LV
20	XO	O	CERALOCK connection terminal *1	LV
21	XI	I	CERALOCK connection terminal *1	LV
22	DVDD	I	Digital Power Supply terminal (Connect to REFA terminal outside the IC)	LV
23	MODE0	I	Operating Mode Selection terminal	LV
24	MODE1	I	Operating Mode Selection terminal	LV
25	MODE2	I	Operating Mode Selection terminal	LV
26	VOL0	I	Input Sensitivity Setting terminal	LV
27	VOL1	I	Input Sensitivity Setting terminal	LV
28	PVDDML	Pow	L-ch 12V-line VDD terminal	HV
29	OUTML	O	L-ch Negative Side Output terminal	HV
30	PVSSL	Pow	L-ch 12V-line VSS terminal	HV
31	PVSSL	Pow	L-ch 12V-line VSS terminal	HV
32	PVSSL	Pow	L-ch 12V-line VSS terminal	HV
33	PVSSL	Pow	L-ch 12V-line VSS terminal	HV
34	PVSSL	Pow	L-ch 12V-line VSS terminal	HV
35	OUTPL	O	L-ch Positive Side Output Terminal	HV
36	PVDDPL	Pow	L-ch 12V-line VDD terminal	HV
37	HP	I	Headphone Control terminal	LV
38	INL	I	L-ch Analog Signal Input terminal	LV
39	VREFL	O	L-ch Reference Voltage terminal (with external capacitor)	LV
40	PVDDREG	Pow	12V-line PVDD terminal for Regulator Circuit	HV
41	REFA	O	5V Regulator Output terminal (with external capacitor)	LV
42	HPOL	O	L-ch Headphone Output terminal	LV

(Note) I: Input terminal, O: Output terminal, I/O: Input/Output terminal, Pow: Power supply terminal
LV: Terminal for V_{REG} power supply voltage range as input voltage range.
HV: Terminal for V_{DDP} power supply voltage range as input voltage range.
*1: CERALOCK which was described above and will be described later is a registered trade mark of Murata Manufacturing Co.,Ltd.

■Block diagram



■Mode setting

・Operating Mode

SLEEPN	MUTEN	HP	MODE[2:0]	OUT*L	OUT*R	HPOL	HPOR	PROTN	CKIO	Outline
L	*	*	*	WL	WL	WL	WL	Z	Z	Sleep mode
H	L	L	*	WL	WL	WL	WL	Z	-	DA Mute mode *A)
H	L	H	*	WL	WL	RF	RF	Z	-	HA Mute mode *A)
H	H	L	LLL	P-H	P-H	WL	WL	Z	-	DA External Clock Slave mode *A)
H	H	L	LLH	P-L	P-L	WL	WL	Z	-	DA External Clock Slave mode *A)
H	H	L	LHL	P-H	P-H	WL	WL	Z	-	DA External Clock Master mode *A)
H	H	L	LHH	P-L	P-L	WL	WL	Z	-	DA External Clock Master mode *A)
H	H	L	HLL	PLS	PLS	WL	WL	Z	-	DA Internal Clock Slave mode *A)
H	H	L	HHL	PLS	PLS	WL	WL	Z	-	DA Internal Clock Master mode *A)
H	H	H	*	WL	WL	SIG	SIG	Z	-	HA mode *A)
H	*	*	LL*	-	-	-	-	-	CKIN	4.19MHz Clock Input
H	*	*	LH*	-	-	-	-	-	CKOUT	4.19MHz Clock Output
H	*	*	HLL	-	-	-	-	-	CKIN	≒500kHz Input (Internal Clock)
H	*	*	HHL	-	-	-	-	-	CKOUT	≒500KHz Output (Internal Clock)

Note:
1) "H" and "L" means logic level High and logic level Low, respectively.
2) "WL" means output disabled (weak pull-down output). "RF" means reference level output. "Z" means Hi-Z.
3) "P-H" means a carrier clock of 524kHz. "P-L" means a carrier clock of 466kHz. "PLS" means a carrier clock of approx. 500kHz (Internally generated clock).
4) "SIG" means an analog audio signal output.
5) "CKIN" means input of a clock with designated frequency. "CKOUT" means output of a designated clock.
6) "DA" means Digital Amplifier. "HA" means Headphone Amplifier.
7) Each output of OUT*L, OUT*R, HPOL, HPOR, PROTN, and CKIO becomes a state as shown in "Protection Mode", depending on the protection state, when entering protection state from a mode except sleep mode.
8) In monaural mode, OUT*R signal as shown in the above "Operating Mode" becomes the same as OUT*L signal. And, HPOR becomes "WL."
9) In operating modes indicated by *A), a state of the output signal becomes a state as shown in "Protection Mode" during a protection mode.
10) "HLH" and "HHH" of MODE[2:0] is reserved for system use.

・Protection Mode

SLEEPN	MUTEN	HP	MODE[2:0]	OUT*L	OUT*R	HPOL	HPOR	PROTN	CKIO	Outline
H	H	L	*	WL	WL	WL	WL	L	Z	Digital Amplifier Over-current Protection
H	*	*	*	WL	WL	WL	WL	L	Z	Over-Temperature Protection
H	*	*	*	WL	WL	-	-	-	-	Clock Stop Protection
H	*	*	*	WL	WL	WL	WL	Z	Z	Low Voltage Malfunction Prevention Protection
H	H	*	*	WL	WL	RF	RF	-	-	Power Supply Voltage Fluctuation Protection

Note:
1) Each protection function operates when input terminal is in the designated logic condition. Output terminal becomes a state as shown in the above during protection mode.

■Description of operating functions

●Digital Amplifier Function

YDA138 has digital amplifiers with analog input, PWM pulse output, Maximum output of 10W (R_L=8Ω)×2ch.
Distortion of PWM pulse output signal and noise of the signal is reduced by adopting "Pure Pulse Direct Speaker Drive Circuit"

First Stage Amplifier Gain Setting Function

YDA138 is composed of the first stage amplifier with gain setting control and 18dB fixed-gain digital amplifier. Gain of the first stage amplifier can be set by VOL[1:0] terminal.

Digital Amplifier Gain Setting

VOL[1:0]	L,L	L,H	H,L	H,H
Gain	36dB	30dB	24dB	18dB
Input Sensitivity	0.14V	0.28V	0.56V	1.12V
Input Impedance	12.1kΩ	22.0kΩ	37.1kΩ	56.5kΩ

Connect a 1μF or more capacitor to the audio signal input terminal (INL and INR) for the rejection of DC signal.
And, half voltage of REFA terminal voltage (V_{REG}) is output to the reference voltage terminals (VREFL and VREFR). Connect a 1μF or more capacitor to the terminals for voltage stabilization.

Carrier Clock Selection Function

YDA138 can select the followings by using MODE[2:0] terminal: selection of Internal clock/External clock, selection of Master mode/Slave mode, selection of carrier clock frequency.

MODE[2:0] setting and each operating mode

MODE[2:0]	Operating Mode	CKIO terminal	CERALOCK	Carrier Clock Frequency
L,L,L	External Clock Slave Mode	4.19MHz input	Unnecessary	524kHz
L,L,H				466kHz
L,H,L	External Clock Master Mode	4.19MHz output	Necessary	524kHz
L,H,H				466kHz
H,L,L	Internal Clock Slave Mode	500kHz input	Unnecessary	500kHz
H,L,H	Reserved			
H,H,L	Internal Clock Master Mode	500kHz output	Unnecessary	500kHz
H,H,H	Reserved			

When using in External Clock Mater Mode, connect a 4.19MHz resonator (CERALOCK) between XI terminal and XO terminal. No external element to XI terminal and XO terminal is necessary, when using in Internal Clock Master Mode.
When using in multi-channel, use one YDA138 (2ch) in Master Mode and use other YDA138 in Slave Mode. At this time, connect CKIO terminal of YDA138 used in Master Mode and that of YDA138 used in Slave Mode. In addition, select the same clock (either Internal Clock or External Clock) in all YDA138.
In an application with AM tuner, harmonic wave of carrier clock and interference of AM carrier frequency can be prevented by changing carrier clock frequency. The setting terminal for carrier clock frequency (MODE0) can be changed at any timing.
The setting terminal for clock mode (MODE2, MODE1) should be changed during power-off or sleep mode (SLEEPN=L).

●Headphone Amplifier Function

YDA138 has class AB single-ended push-pull headphone amplifier. Headphone amplifier mode can be set by setting HP terminal to H. Audio signal input terminal and voltage reference terminal is common to digital amplifier.
Connect DC-cut capacitor to headphone amplifier output terminal (HPOL and HPOR).
When a headphone amplifier is not used, HP terminal should be "L" and output terminal (HPOL, HPOR) should be "No Connection".

First stage Amplifier Gain Setting function

Headphone amplifier is composed of the first stage amplifier of which gain setting is possible, and 0dB fixed-gain amplifier. Gain of the first stage amplifier can be set by VOL[1:0] terminal.

Headphone Amplifier Gain Setting

VOL[1:0]	L,L	L,H	H,L	H,H
Gain	18dB	12dB	6dB	0dB
Input sensitivity	0.14V	0.28V	0.56V	1.12V
Input Impedance	12.1kΩ	22.0kΩ	37.1kΩ	56.5kΩ

●Control Function

Sleep Function

When SLEEPN terminal is L, YDA138 enters the Sleep Mode.
In Sleep mode, all the circuit functions including 5V regulator are stopped to minimize the consumption current. At this time, output stages of digital amplifier and headphone amplifier are disabled and PROTN and CKIO terminal output becomes “Hi-Z”.

Mute Function

When MUTEN terminal is set to L while HP terminal is L, YDA138 enters the Digital Amplifier Mute mode. In this mode, output stage of Digital Amplifier is disabled.
When MUTEN terminal is set to L while HP terminal is H, YDA138 enters the Headphone Amplifier Mute Mode. In this mode, output stage of Headphone Amplifier outputs the reference voltage.

Headphone Selection Function

When HP terminal is set to H, YDA138 enters the Headphone Amplifier mode. At this time, output stage of Digital Amplifier is disabled. On the contrary, when HP terminal is set to L, YDA138 enters Digital Amplifier mode. At this time, output of the Headphone Amplifier output is disabled.
When logic of HP terminal is changed, YDA138 restarts and as the result of it, all the protection states are cleared.

Monaural Selection Function

YDA138 enters the Monaural mode, when connecting VREFR terminal to REFA terminal and then connecting INR terminal to AVSS terminal.
In Digital Amplifier Monaural Mode, maximum continuous output 20W can be obtained by short-circuiting between OUTPL terminal and OUTPR terminal and between OUTML terminal and OUTMR terminal to drive 4Ω load resistor.
In Headphone Amplifier Monaural Mode, HPOUTL terminal outputs signals and HPOUTR terminal is disabled.

●Protection Function

YDA138 has Over-current Protection function and Clock Stop Protection function as protection functions for the digital amplifier. In addition, it has Output Current Limit function as a protection function for headphone amplifier. Moreover, YDA138 has Thermal Protection function, Low-voltage Malfunction Prevention function, and Power Supply Voltage Fluctuation Protection function commonly.

Over-current Protection Function

This is a function to make the Over-current Protection Mode (disables the output stage of digital amplifier in addition to the output of L signal to PROTN terminal) by detection of short-circuiting (Ground short/Power supply short/Speaker terminal short) in the output stage of digital amplifier.
The over-current protection function can be canceled by power off or setting L to SLEEPN terminal and can be automatically returned after the over-current detection by connection of PROTN terminal and SLEEPN terminal.

Thermal Protection Function

This is a function to make the Thermal Protection Mode (disables the output stage of digital amplifier and headphone amplifier in addition to the output of L signal to PROTN terminal) by detecting extraordinary high temperature of YDA138.
This Thermal Protection mode can be cancelled by lowering temperature of YDA138, power off, or setting L to SLEEPN terminal and can be automatically returned after the extraordinary high temperature detection by connection of PROTN terminal and SLEEPN terminal.

Clock Stop Protection Function

This is a function to make the Clock Stop Protection mode (disables the output stage of digital amplifier) when carrier clock frequency was extraordinarily lowered in digital amplifier mode.
The Clock Stop Protection mode can be cancelled by returning carrier clock frequency to the right value.

Low-voltage Malfunction Prevention Function

This is a function to make the Low-voltage Protection mode (disables the output stage of digital amplifier and headphone amplifier in addition to making “Hi-Z” of PROTN terminal) when voltage at 12V-line power terminal (PVDDREG) becomes lower than Low-voltage detection threshold voltage (V_{UVPL}) or voltage at 5V-line power terminal (REFA, DVDD) becomes lower than the voltage (V_{UVAL}).
In addition, when voltage at 12V-line power supply terminal becomes lower than $V_{UVPL,}$ 5V embedded regulator is also disabled.
The Low-voltage Protection mode is cancelled when voltage at each power supply terminal exceeded the low-voltage cancellation threshold voltage (V_{UVPH},V_{UVAH}).

Power Supply Voltage Detection Function

This is a function to make Mute mode when voltage at 5V Regulator output terminal (REFA) fluctuated (V_{MH},V_{ML}) with respect to twice of the voltage of reference terminals (VREFL,VREFR).

Headphone Amplifier Output Current Limit Function

YDA138 headphone amplifier has a Current-Limit-Circuit which limits output current so as not to exceed the limit current (I_{OCHP}).

●5V Regulator Function

YDA138 outputs 5V to REFA terminal when SLEEPN terminal is H. Connect a 1μF or more capacitor to REFA terminal for voltage stabilization.
Connect REFA terminal to DVDD terminal on a board. And, do not connect the REFA terminal to other terminals except for DVDD terminal and YDA138 control terminals.

●Pop Noise Reduction Function

The Pop Noise Reduction Function works in the following cases: Power-on, Power-off, Sleep ON/OFF, Mute ON/OFF, and switching time between headphone amplifier and digital amplifier.
Pop noise at the Power-on, Power-off, and Sleep ON/OFF depends on the value of DC-cut capacitor for audio input signal. The smaller the value, the greater the effect on the pop noise reduction; however, 1μF of capacitance is recommended in the consideration of the low frequency cutoff.

●Correspond to Filter less

Normally, when LC filter is not used, carrier signal of 50% modulation comes into speaker even in MUTE state and causes significant loss, and as the result the speaker is heated.
Generally, 10W speaker or so is considered to have inductance component of not less than 20μH.
In the modulation method of YDA138, duty ratio of the carrier signal is several % in the MUTE state, so the speaker inductance component can sufficiently inhibit speaker loss without LC filter; therefore, the speaker is not heated.

●Speaker Inductance

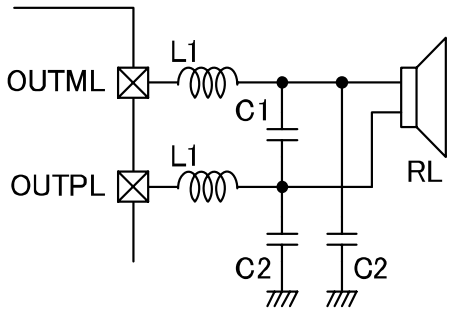
When YDA138 is used without LC filter, speaker inductance component reduces speaker loss in the MUTE state; therefore, use a speaker with inductance component of 20μH or more at the carrier clock frequency.

●LC Filter

When connecting LC filters to YDA138, make the following LC filter circuit. Use the following constant in accordance with speaker impedance. By using the following constant, low-pass filter with cutoff frequency=50kHz or so, Q=0.7 or so is configured.

LC Filter Constant

RL	L1	C1	C2
4Ω	10μH	0.47μF	0.01μF
8Ω	22μH	0.22μF	0.01μF
16Ω	47μH	0.11μF	0.01μF



LC Filter circuit

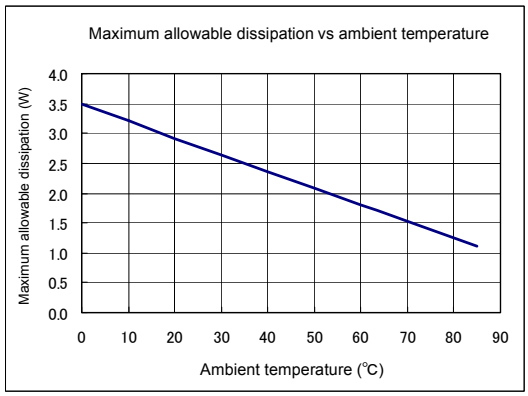
●Allowable Dissipation

The power dissipation of YDA138 is limited by the junction temperature rating (125℃) and package thermal resistance (35.9℃/W).
The power dissipation and junction temperature of YDA138 can be found by the following formula.
For the use of YDA138, take care not to exceed the power dissipation and junction temperature.

・Formula for the Power Dissipation

Ploss = (Pout ∗ Rpn / Rl) ∗ 2 + Idc ∗ Vdc

Ploss	: Allowable Dissipation (W)
Pout	: Output Power (W)
Rpn	: 0.66 (Constant)
Rl	: Load Resistor (Ω)
Idc	: 0.035(Constant / at V_{DDP}=12V)
	0.028(Constant / at V_{DDP}=9V)
	0.038(Constant / at V_{DDP}=13.5V)
Vdc	: Power supply voltage (V)



Maximum allowable dissipation of YDA138

・Formula for the junction temperature

Tj = Ploss ∗ θja + Ta

Ploss	: Allowable Dissipation (W)
θja	: 35.9 (Constant/ package thermal resistance (℃/W))
Ta	: Ambient Temperature (℃)

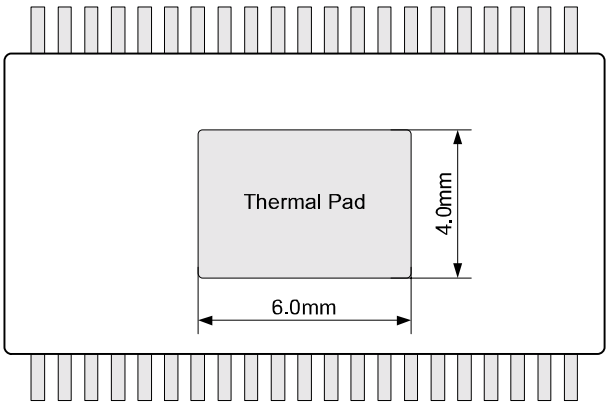
●Mounting

The package (42SSOP) for YDA138 has Thermal Pad for radiation on the bottom. This Thermal Pad does not need soldering on the board.

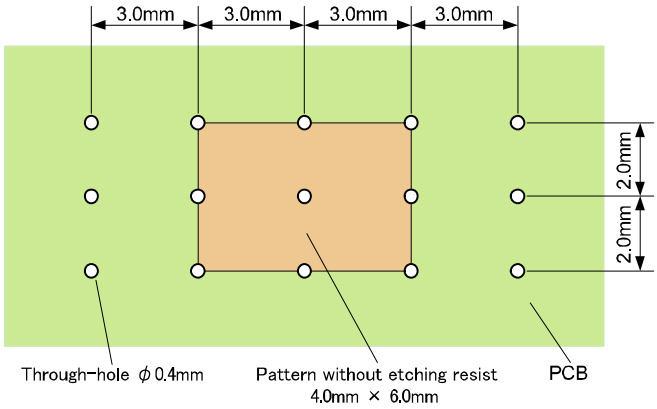
・Example of Pattern

Thermal resistance of the package is 35.9℃/W. This thermal resistance was measured under the following conditions: mounting board 136mm×85mm, copper leaf board density 154%, no wind. In addition, a part of the board that faces to Thermal Pad is a pattern (4mm*6mm) without etching resist, the pattern is connected to the opposite side by through-hole (φ0.4).

YDA138 Package bottom

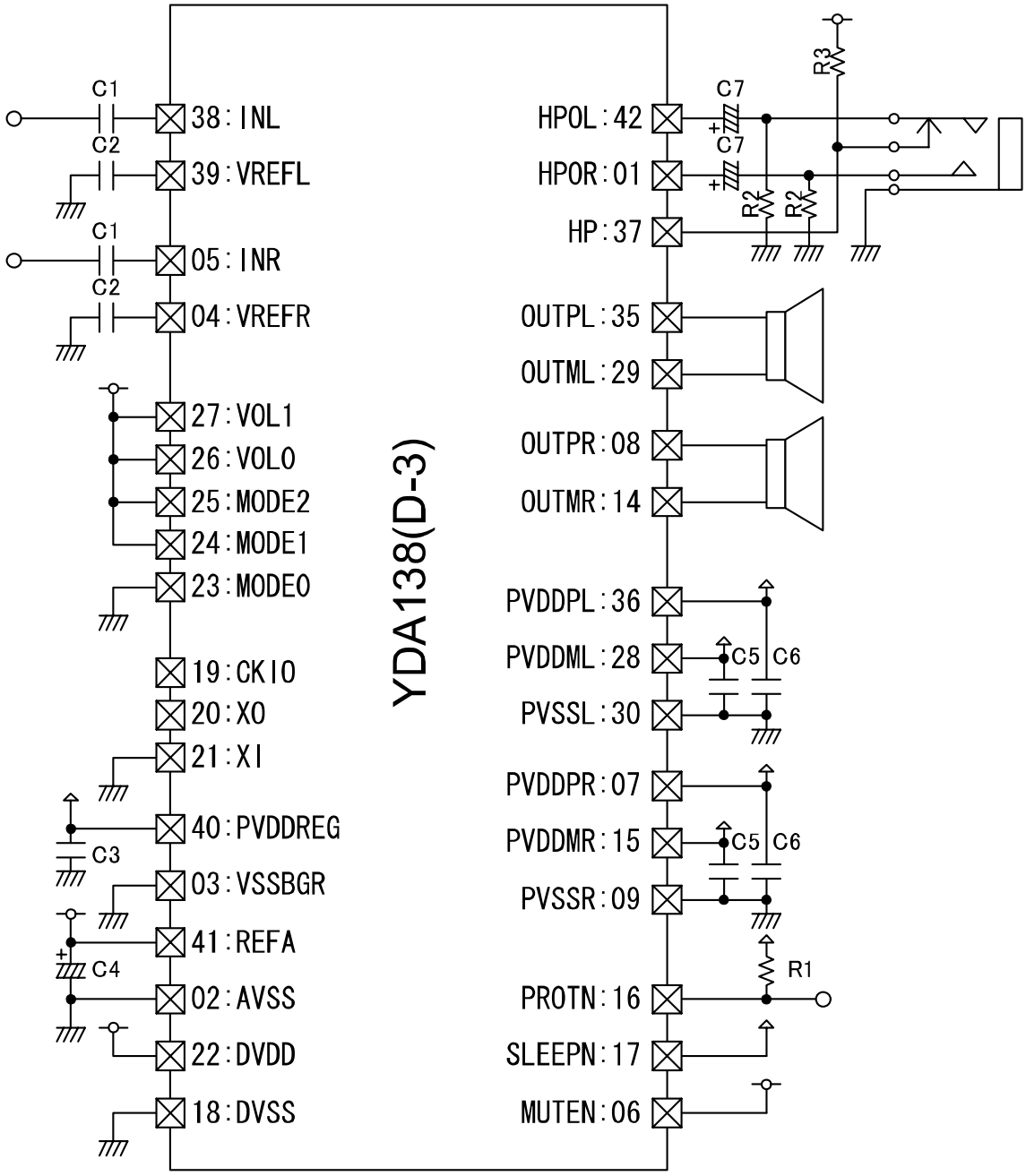


Example of pattern



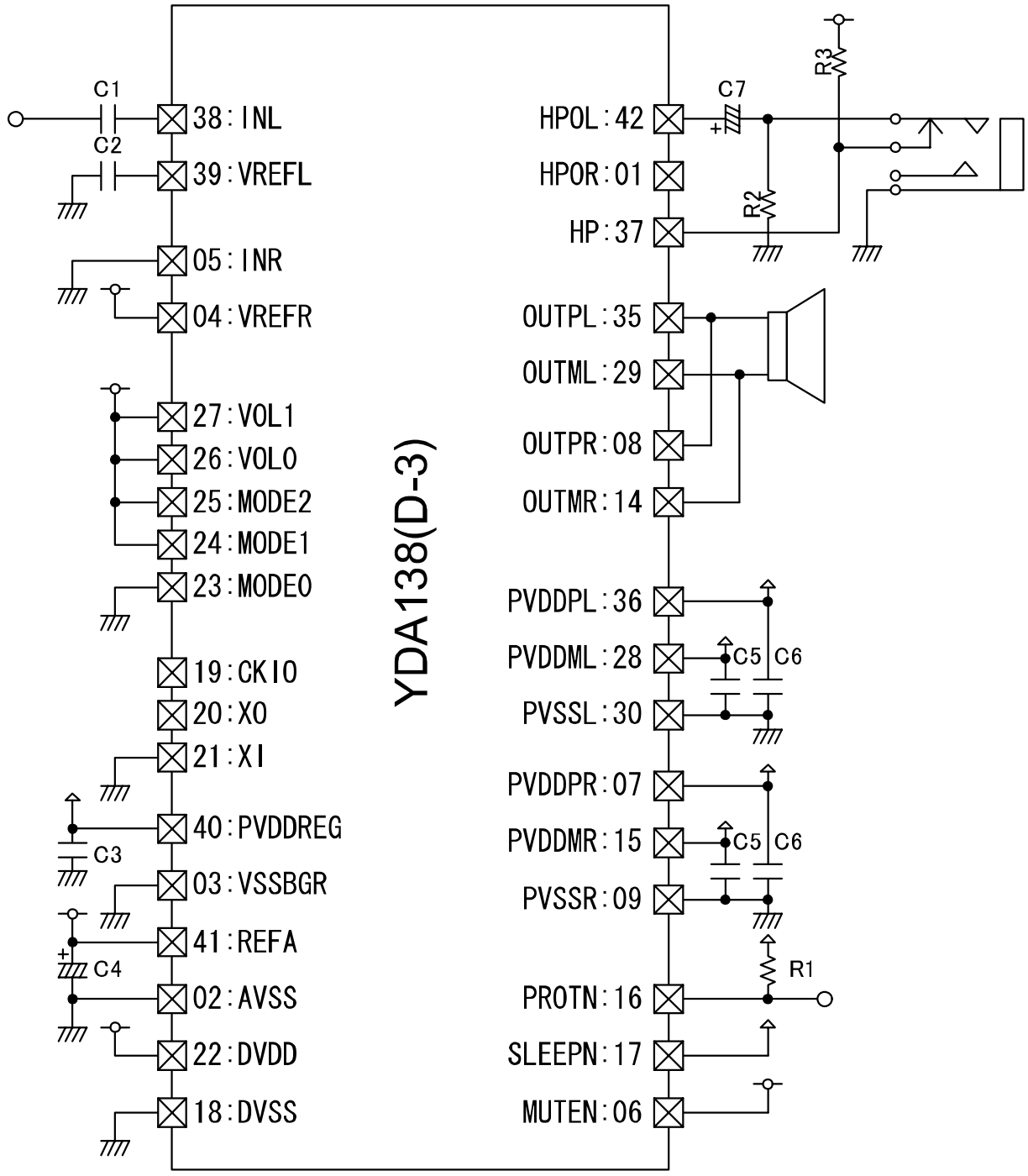
■Application circuit examples

●2-channel Operating Mode (Internal Clock Master Mode)

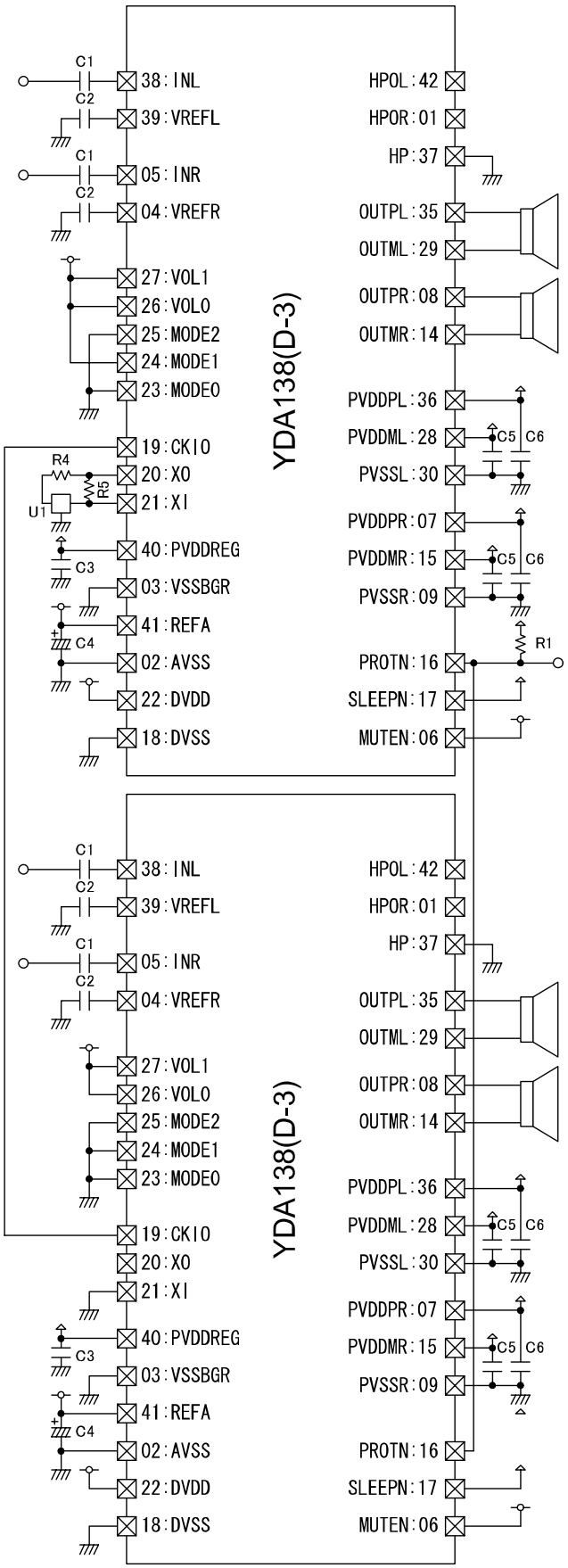


ID	Value	Element	ID	Value	Element
C1	1μF	Multilayer ceramic capacitor	R1	100kΩ	Chip Resistor
C2	1μF	Multilayer ceramic capacitor	R2	1kΩ	Chip Resistor
C3	0.1μF	Multilayer ceramic capacitor	R3	100kΩ	Chip Resistor
C4	10μF	Electrolytic capacitor (0.1μF Ceramic capacitor)	R4	680Ω	Chip Resistor
C5,C6	4.7μF	Multilayer ceramic capacitor	R5	1MΩ	Chip Resistor
C7	330μF	Electrolytic capacitor	U1	(CERALOCK) CSTCR4M19G53-B0	

●Monaural Operating Mode (Internal Clock Master Mode)



●Multi-channel Operating Mode



■Electrical characteristic

●Absolute Maximum Ratings Note 6)

Item	Symbol	Min.	Max.	Unit
Power supply terminal (VDDP) Voltage Range Note 1,2,3)	V_{DDP}	-0.3	14.0	V
SLEEPN, PROTN terminal Voltage Range	V_{IN1}	V_{SS}-0.3	V_{DDP}+0.3	V
CKIO Input/Output terminal Voltage Range	V_{IN2}	V_{SS}-0.3	V_{REG}+1.0	V
Voltage Range of terminals for control Note 4)	V_{IN3}	V_{SS}-0.3	V_{REG}+1.0	V
Voltage Range of Input/output terminals Note 5)	V_{IN4}	V_{SS}-0.3	V_{REG}+0.3	V
Allowable dissipation (Ta=25ºC)	P_{D25}		2.7	W
Allowable dissipation (Ta=70ºC)	P_{D70}		1.45	W
Junction temperature	T_{JMAX}		125	ºC
Storage Temperature	T_{STG}	-50	125	ºC

Note 1) VSS means AVSS, VSSBGR, DVSS, PVSSR and PVSSL. Place all VSS terminals in the same potential.
Note 2) All the voltages are measured with respect to V_{SS}=0V.
Note 3) Power supply terminal (VDDP) means PVDDREG, PVDDPR, PVDDMR, PVDDPL and PVDDML.
Note 4) Control Input/Output terminal means MUTEN, HP, VOL[1:0] and MODE[2:0].
Note 5) Input/output terminal means INL, VREFL, INR, VREFR, XI and XO.
Note 6) Absolute Maximum Ratings is values which must not be exceeded to guarantee device reliability and life, and when using a device in excess even a moment, it may immediately cause damage to device or may significantly deteriorate its reliability

●Recommended Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage Note 7)	V_{DDP}	9.0	12.0	13.5	V
Operating Ambient Temperature	T_a	-40	25	85	ºC
Speaker Impedance (Stereo)	R_{LS}	7.5	8		Ω
Speaker Impedance (Mono)	R_{LM}	3.75	4		Ω
Headphone Impedance	R_{LHP}	16	32		Ω

Note 7) All the voltages are measured with respect to V_{SS}=0V.

●DC Characteristics (V_{SS}=0V, V_{DDP}=12V±0.5V, Ta=0ºC to 85ºC, unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
REFA Output terminal voltage	V_{REG}	4.5	5	5.5	V
PROTN terminal Low level output voltage (I_{OL}=1.6mA)	V_{OLP}			0.4	V
CKIO terminal High level output voltage (I_{OH}=-80μA)	V_{OHC}	4.0			V
CKIO terminal Low level output voltage (I_{OL}=1.6mA)	V_{OLC}			0.5	V
SLEEPN, CKIO terminal High level input voltage	V_{IH1}	2.2			V
SLEEPN, CKIO terminal Low level input voltage	V_{IL1}			0.8	V
Input terminals for control High level input voltage	V_{IH2}	3.5			V
Input terminals for control Low level input voltage	V_{IL2}			1.5	V
REFA/DVDD terminal Start-up threshold voltage	V_{UVAH}		3.7		V
REFA/DVDD terminal Cutoff threshold voltage	V_{UVAL}		3.3		V
PVDDREG terminal start-up threshold voltage	V_{UVPH}		8.0		V
PVDDREG terminal Cutoff threshold voltage	V_{UVPL}		7.6		V
Power Supply Fluctuation Cutoff threshold voltage (lower limit)	V_{ML}		VREF*1.8		V
Power Supply Fluctuation Cutoff threshold voltage (upper limit)	V_{MH}		VREF*2.2		V
Headphone Amplifier limit current	I_{OCHP}		50		mA

●AC characteristics (V_{SS}=0V, V_{DDP}=12V±0.5V, Ta=0ºC to 85ºC, unless otherwise specified)

Item	Symbol	Min.	Typ.	Max.	Unit
Master Clock Frequency (internal clock mode)	F_{CK}		500		kHz
Clock Stop Detection Carrier Clock Frequency	F_{UFP}		150		kHz
Consumption Current (Sleep mode)	I_{SLEEP}		1		μA
Consumption Current (Mute mode)	I_{MUTE}		20		mA
Consumption Current (Digital amplifier output in no-signal input)	I_{DDD}		40		mA
Consumption Current (Headphone output in no-signal input)	I_{DDH}		10		mA

Note1) 8Ω resistor and 30μH coil are used as an output load in order to obtain various digital amplifier characteristics.

●Analog Characteristics (V_{SS}=0V, V_{DDP}=12V, Ta=25ºC, Frequency:1kHz, unless otherwise specified)

Digital Amplifier Section

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Maximum Output (stereo) (THD+N=10%)	R_L=8Ω	P_O		10.0		W
Maximum Output (mono) (THD+N=10%)	R_L=4Ω			20.0		W
Voltage Gain (at 1V input sensitivity)		A_V		18		dB
Total Harmonic Distortion Rate (stereo) (BW: 20kHz)	R_L=8Ω, P_O=1.0W	THD+N		0.02		%
Total Harmonic Distortion Rate (mono) (BW: 20kHz)	R_L=4Ω, P_O=10W			0.1		%
Signal /Noise Ratio (BW: 20kHz A-Filter)	R_L=8Ω, P_O=10W, VOL[1:0]=H,H	SNR		103		dB
Channel Separation Ratio	VOL[1:0]=H,H	CS		-70		dB
Maximum Efficiency	R_L=8Ω, P_O=10W	η		88		%
Output Offset Voltage		Vo		±20		mV

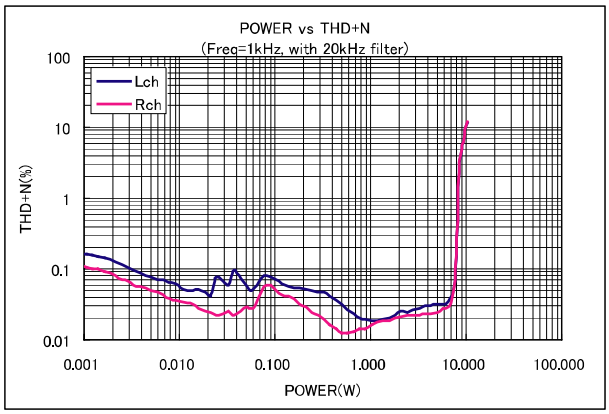
Note) All the values of analog characteristics were obtained by using our evaluation circumstance.
Depending upon parts and pattern layout to use, characteristics may be changed.
8Ω resistor and 30μH coil are used as an output load in order to obtain various digital amplifier characteristics.

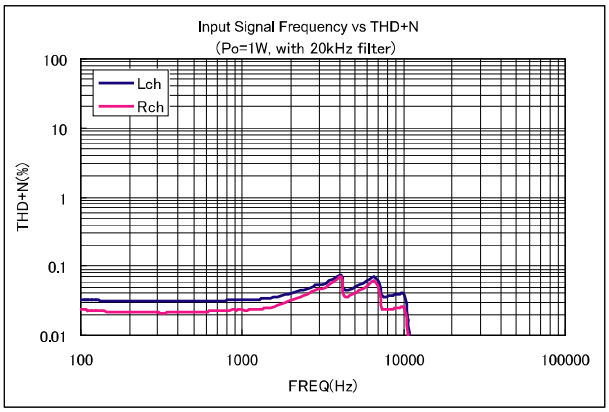
Headphone Amplifier Section

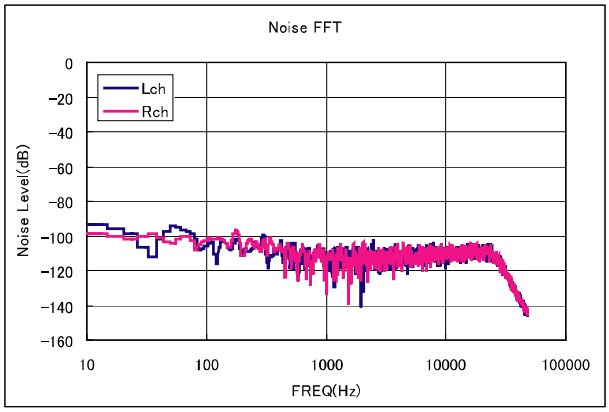
Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Maximum Output (THD+N=10%)	R_L=32Ω	P_{ho}		50.0		mW
Total Harmonic Distortion Rate (BW: 20kHz)	R_L=32Ω, P_{ho}=30mW	THD+N		0.01		%
Signal /Noise Ratio (BW: 20kHz A-Filter)	R_L=32Ω, P_{ho}=20mW, VOL[1:0]=H,H	SNR		95		dB
Channel Separation Ratio	R_L=32Ω, VOL[1:0]=H,H	CS		-75		dB

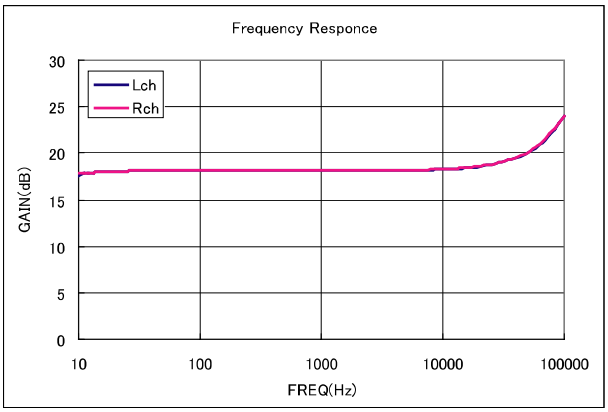
■Typical characteristics examples

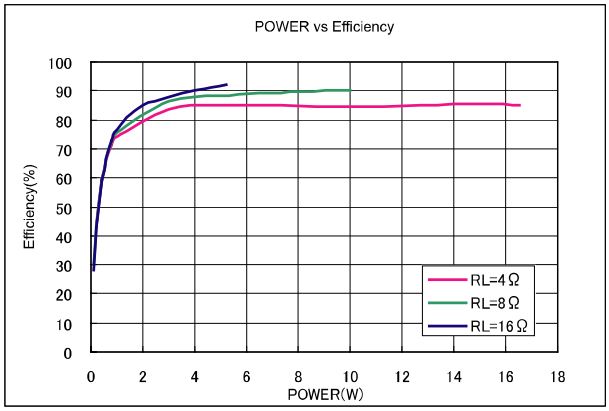
●Digital Amplifier Characteristics (V_{DDP}=12V, R_L=8Ω+30μH, Frequency=1kHz, VOL[1:0]=H,H, MODE[2:0]=L,H,L)

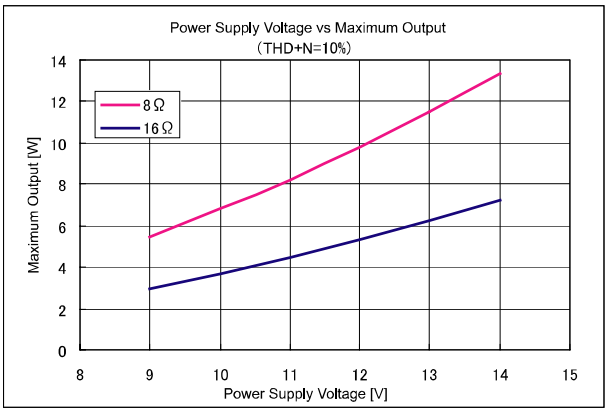


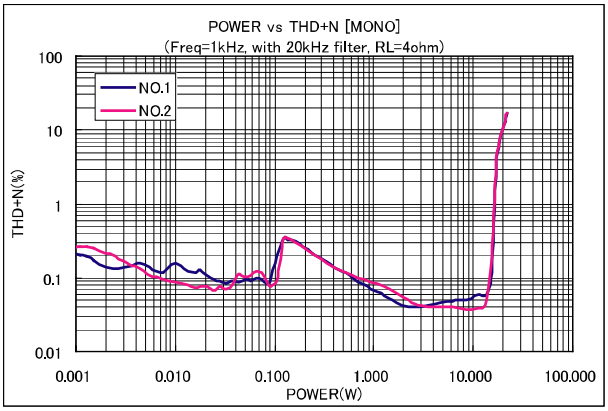


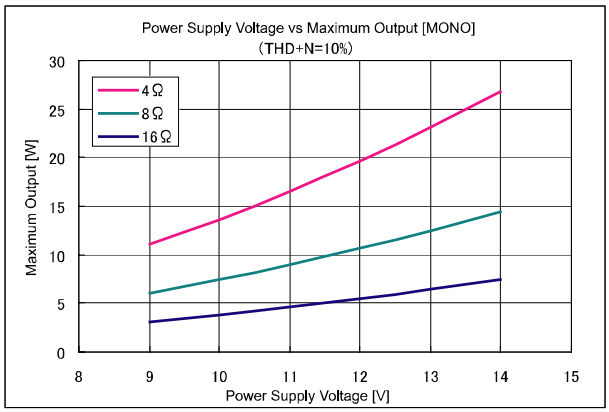




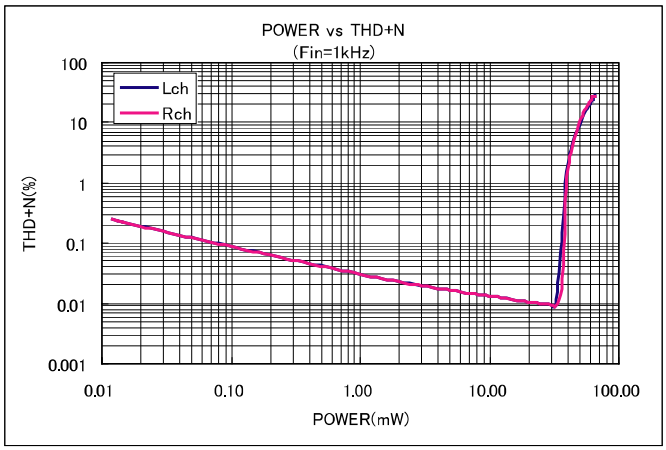


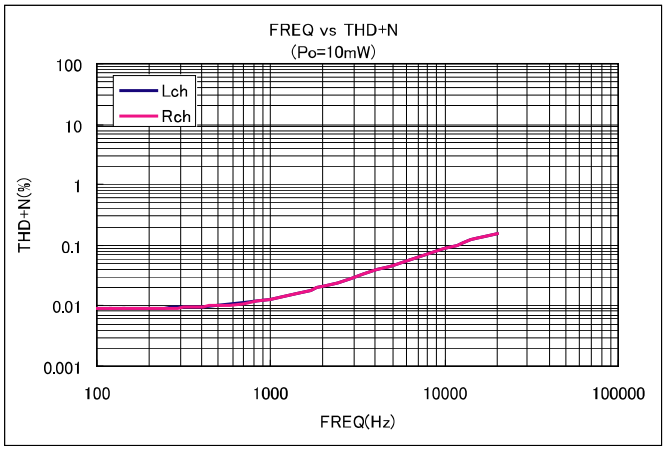


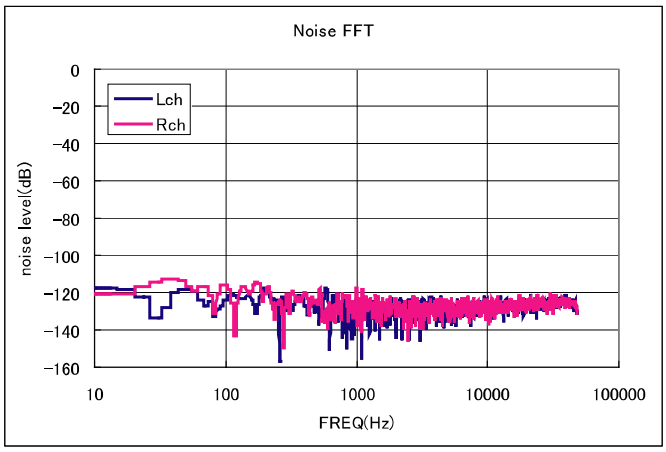


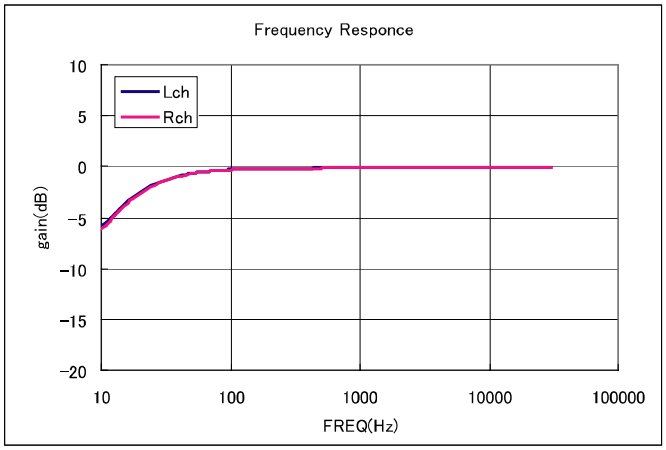


●Headphone Amplifier Characteristics (V_{DDP}=12V, R_L=32Ω, Frequency=1kHz, VOL[1:0]=H,H, MODE[2:0]=L,H,L)



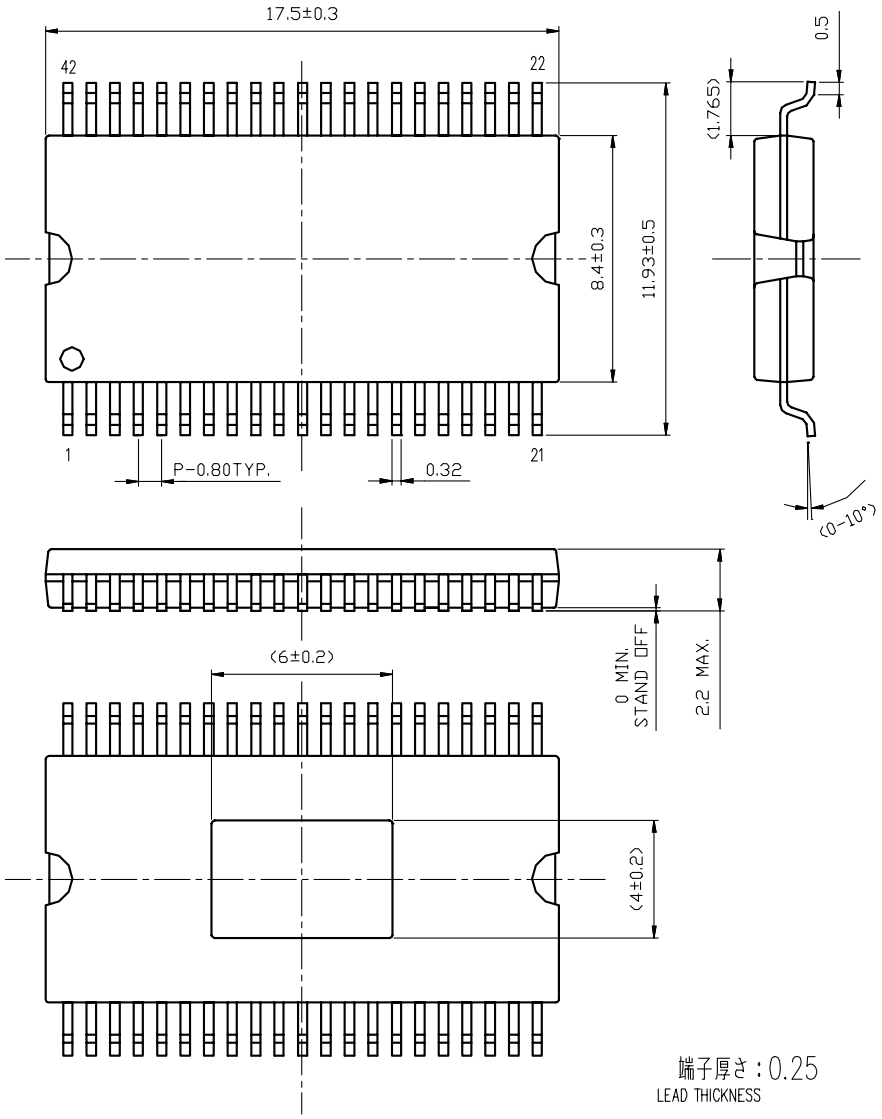






■Package outline

C-PK42EP-3



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

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YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

■ Head Office 203, Matsunokijima, Toyooka-mura
Iwata-gun, Shizuoka-ken, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office 3-12-12, Minami Senba, Chuo-ku,
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229

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