

Features

- Synchronizes to standard telecom or Ethernet backplane clocks and provides jitter filtered output clocks for SONET/SDH, PDH and Ethernet network interface cards
- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
- Two independent DPLLS provides timing for the transmit path (backplane to line rate) and the receive path (recovered line rate to backplane)
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Selectable loop bandwidth of 14 Hz, 28 Hz, 890 Hz, or 0.1 Hz
- Supports automatic hitless reference switching and short term holdover during loss of reference inputs
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g. 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Ethernet PHYs
- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any

Ordering Information

ZL30131GGG 100 Pin CABGA Trays

ZL30131GGG2 100 Pin CABGA* Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

multiple of 8 kHz up to 100 MHz (e.g., T1/E1, DS3/E3)

- Generates several styles of output frame pulses with selectable pulse width, polarity, and frequency
- Configurable input to output delay and output to output phase alignment
- Configurable through a serial interface (SPI or I²C)
- DPLLS can be configured to provide synchronous or asynchronous clock outputs

Applications

- ITU-T G.8262 Line Cards which support 1GbE and 10GbE interfaces
- SONET line cards up to OC-192
- SDH line cards up to STM-64

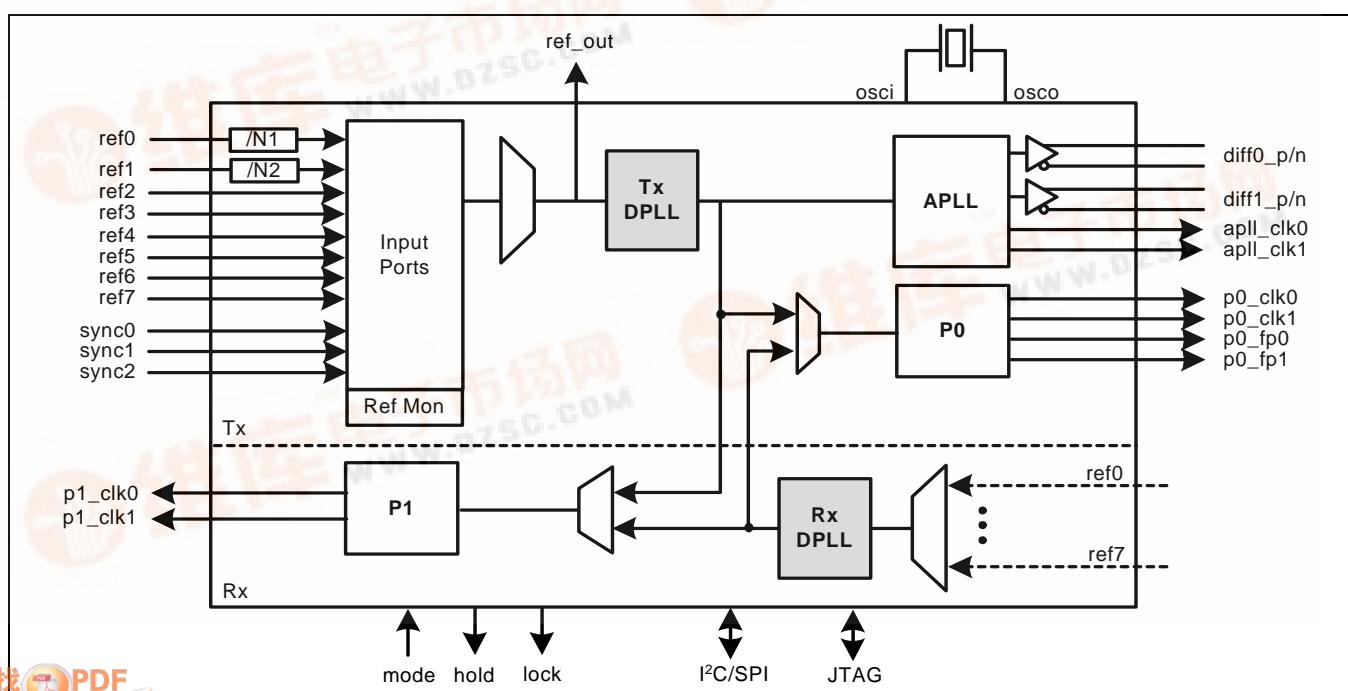


Figure 1 - Functional Block Diagram

Pin Description

Pin #	Name	I/O Type	Description
Input Reference			
C1 B2 A3 C3 B3 B4 C4 A4	ref0 ref1 ref2 ref3 ref4 ref5 ref6 ref7	I _u	Input References 7:0 (LVC MOS, Schmitt Trigger). These input references are available to both the Tx DPLL and the Rx DPLL for synchronizing output clocks. All eight input references can lock to any multiple of 8 kHz up to 77.76 MHz including 25 MHz and 50 MHz. Input ref0 and ref1 have additional configurable pre-dividers allowing input frequencies of 62.5 MHz, 125 MHz, and 155.52 MHz. These pins are internally pulled up to V _{dd} .
B1 A1 A2	sync0 sync1 sync2	I _u	Frame Pulse Synchronization References 2:0 (LVC MOS, Schmitt Trigger). These are optional frame pulse synchronization inputs associated with input references 0, 1 and 2. These inputs accept frame pulses in a clock format (50% duty cycle) or a basic frame pulse format with minimum pulse width of 5 ns. These pins are internally pulled up to V _{dd} .
Output Clocks and Frame Pulses			
A9 B10	diff0_p diff0_n	O	Differential Output Clock 0 (LVPECL). When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See “Output Clocks and Frame Pulses” section on page 22 more detail on clock frequency settings.
A10 B9	diff1_p diff1_n	O	Differential Output Clock 1 (LVPECL). When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See “Output Clocks and Frame Pulses” section on page 22 more detail on clock frequency settings.
D10	apll_clk0	O	APLL Output Clock 0 (LVC MOS). This output can be configured to provide any one of the SONET/SDH clock outputs up to 77.76 MHz or any of the Ethernet clock rates up to 125 MHz. The default frequency for this output is 77.76 MHz.
G10	apll_clk1	O	APLL Output Clock 1 (LVC MOS). This output can be configured to provide any one of the SONET/SDH clock outputs up to 77.76 MHz or any of the Ethernet clock rates up to 125 MHz. The default frequency for this output is 19.44 MHz.
K9	p0_clk0	O	Programmable Synthesizer 0 - Output Clock 0 (LVC MOS). This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz in addition to 2 kHz. The default frequency for this output is 2.048 MHz.
K7	p0_clk1	O	Programmable Synthesizer 0 - Output Clock 1 (LVC MOS). This is a programmable clock output configurable as a multiple or division of the p0_clk0 frequency within the range of 2 kHz to 100 MHz. The default frequency for this output is 8.192 MHz.
K8	p0_fp0	O	Programmable Synthesizer 0 - Output Frame Pulse 0 (LVC MOS). This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz.

Pin #	Name	I/O Type	Description
J7	p0_fp1	O	Programmable Synthesizer 0 - Output Frame Pulse 1 (LVC MOS). This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz
J10	p1_clk0	O	Programmable Synthesizer 1 - Output Clock 0 (LVC MOS). This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz in addition to 2 kHz. The default frequency for this output is 1.544 MHz (DS1).
K10	p1_clk1	O	Programmable Synthesizer1 - Output Clock 1 (LVC MOS). This is a programmable clock output configurable as a multiple or division of the p1_clk0 frequency within the range of 2 kHz to 100 MHz. The default frequency for this output is 3.088 MHz (2x DS1).
E1	ref_out	O	Rx DPLL Selected Output Reference (LVC MOS). This is a buffered copy of the output of the reference selector for the Rx DPLL. Switching between input reference clocks at this output is not hitless.
Control			
H5	rst_b	I	Reset (LVC MOS, Schmitt Trigger). A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
J5	hs_en	I _u	Tx DPLL Hitless Switching Enable (LVC MOS, Schmitt Trigger). A logic high at this input enables hitless reference switching. A logic low disables hitless reference switching and re-aligns the Tx DPLL's output phase to the phase of the selected reference input. This feature can also be controlled through software registers. This pin is internally pulled up to Vdd.
C2 D2	mode_0 mode_1	I _u	Tx DPLL Mode Select 1:0 (LVC MOS, Schmitt Trigger). During reset, the levels on these pins determine the default mode of operation for the Tx DPLL (Automatic, Normal, Holdover or Freerun). After reset, the mode of operation can be controlled directly with these pins, or by accessing the tx_dpll_modesel register (0x1F) through the serial interface. This pin is internally pulled up to Vdd.
K1	diff0_en	I _u	Differential Output 0 Enable (LVC MOS, Schmitt Trigger). When set high, the differential LVPECL output 0 driver is enabled. When set low, the differential driver is tristated reducing power consumption. This pin is internally pulled up to Vdd.
D3	diff1_en	I _u	Differential Output 1 Enable (LVC MOS, Schmitt Trigger). When set high, the differential LVPECL output 1 driver is enabled. When set low, the differential driver is tristated reducing power consumption. This pin is internally pulled up to Vdd.
Status			
H1	lock	O	Lock Indicator (LVC MOS). This is the lock indicator pin for the Tx DPLL. This output goes high when the Tx DPLL's output is frequency and phase locked to the input reference.
J1	hold	O	Holdover Indicator (LVC MOS). This pin goes high when the Tx DPLL enters the holdover mode.

Pin #	Name	I/O Type	Description
Serial Interface			
E2	sck_scl	I/B	Clock for Serial Interface (LVC MOS). Serial interface clock. When i2c_en = 0, this pin acts as the sck pin for the serial interface. When i2c_en = 1, this pin acts as the scl pin (bidirectional) for the I ² C interface.
F1	si_sda	I/B	Serial Interface Input (LVC MOS). Serial interface data pin. When i2c_en = 0, this pin acts as the si pin for the serial interface. When i2c_en = 1, this pin acts as the sda pin (bidirectional) for the I ² C interface.
G1	so	O	Serial Interface Output (LVC MOS). Serial interface data output. When i2c_en = 0, this pin acts as the so pin for the serial interface. When i2c_en = 1, this pin is unused and should be left unconnected.
E3	cs_b_asel0	I _u	Chip Select for SPI/Address Select 0 for I²C (LVC MOS). When i2c_en = 0, this pin acts as the chip select pin (active low) for the serial interface. When i2c_en = 1, this pin acts as the asel0 pin for the I ² C interface.
F3	asel1	I _u	Address Select 1 for I²C (LVC MOS). When i2c_en = 1, this pin acts as the asel1 pin for the I ² C interface. Internally pulled up to Vdd. Leave open when not in use.
F2	asel2	I _u	Address Select 2 for I²C (LVC MOS). When i2c_en = 1, this pin acts as the asel2 pin for the I ² C interface. Internally pulled up to Vdd. Leave open when not in use.
G2	int_b	O	Interrupt Pin (LVC MOS). Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled-up to Vdd.
J2	i2c_en	I _u	I²C Interface Enable (LVC MOS). If set high, the I ² C interface is enabled, if set low, the SPI interface is enabled. Internally pull-up to Vdd.
APLL Loop Filter			
A6	apll_filter	A	External Analog PLL Loop Filter terminal.
B6	filter_ref0	A	Analog PLL External Loop Filter Reference.
C6	filter_ref1	A	Analog PLL External Loop Filter Reference.
JTAG and Test			
J4	tdo	O	Test Serial Data Out (Output). JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
K2	tdi	I _u	Test Serial Data In (Input). JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.
H4	trst_b	I _u	Test Reset (LVC MOS). Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to Vdd. If this pin is not used then it should be connected to GND.
K3	tck	I	Test Clock (LVC MOS): Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.

Pin #	Name	I/O Type	Description
J3	tms	I _u	Test Mode Select (LVC MOS). JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V _{DD} . If this pin is not used then it should be left unconnected.
Master Clock			
K4	osci	I	Oscillator Master Clock Input (LVC MOS). This input accepts a 20 MHz reference from a clock oscillator (TCXO, OCXO). The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
K5	osco	O	Oscillator Master Clock Output (LVC MOS). This pin must be left unconnected when the osci pin is connected to a clock oscillator.
Miscellaneous			
J6	IC		Internal Connection. Connect to ground.
C5 B5 K6 H10	IC		Internal Connection. Leave unconnected.
H7 G3 E10 F10 D1	NC		No Connection. Leave Unconnected.
Power and Ground			
D9 E4 G8 G9 J8 J9 H6 H8	V _{DD}	P P P P P P P P	Positive Supply Voltage. +3.3V _{DC} nominal.
E8 F4	V _{CORE}	P P	Positive Supply Voltage. +1.8V _{DC} nominal.
A5 A8 C10	AV _{DD}	P P P	Positive Analog Supply Voltage. +3.3V _{DC} nominal.
B7 B8 H2	AV _{CORE}	P P P	Positive Analog Supply Voltage. +1.8V _{DC} nominal.

Pin #	Name	I/O Type	Description
D4		G	Ground. 0 Volts.
D5		G	
D6		G	
D7		G	
E5		G	
E6		G	
E7		G	
F5		G	
F6		G	
F7		G	
G4		G	
G5		G	
G6		G	
G7		G	
E9		G	
F8		G	
F9		G	
H9		G	
A7	AVss	G	Analog Ground. 0 Volts.
C7		G	
C8		G	
C9		G	
D8		G	
H3		G	

I - Input

I_d - Input, Internally pulled downI_u - Input, Internally pulled up

O - Output

A - Analog

P - Power

G - Ground

1.0 Pin Diagram

TOP VIEW

	1	2	3	4	5	6	7	8	9	10
A	○ sync1	○ sync2	○ ref2	○ ref7	○ AV _{DD}	○ apll_filter	○ AV _{SS}	○ AV _{DD}	○ diff0_p	○ diff1_p
B	○ sync0	○ ref1	○ ref4	○ ref5	○ IC	○ filter_ref0	○ AV _{CORE}	○ AV _{CORE}	○ diff1_n	○ diff0_n
C	○ ref0	○ mode_0	○ ref3	○ ref6	○ IC	○ filter_ref1	○ AV _{SS}	○ AV _{SS}	○ AV _{SS}	○ AV _{DD}
D	○ NC	○ mode_1	○ diff1_en	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ AV _{SS}	○ V _{DD}	○ apll_clk0
E	○ ref_out	○ sck/scl	○ cs_b/asel0	○ V _{DD}	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ V _{CORE}	○ V _{SS}	○ NC
F	○ si/sdh	○ asel2	○ asel1	○ V _{CORE}	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ NC
G	○ so	○ int_b	○ NC	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ V _{SS}	○ V _{DD}	○ V _{DD}	○ apll_clk1
H	○ lock	○ AV _{CORE}	○ AV _{SS}	○ trst_b	○ rst_b	○ V _{DD}	○ NC	○ V _{DD}	○ V _{SS}	○ IC
J	○ hold	○ i2c_en	○ tms	○ tdo	○ hs_en	○ IC	○ p0_fp1	○ V _{DD}	○ V _{DD}	○ p1_clk0
K	○ diff0_en	○ tdi	○ tck	○ osci	○ osc0	○ IC	○ p0_clk1	○ p0_fp0	○ p0_clk0	○ p1_clk1



1 - A1 corner is identified with a dot.

2.0 Functional Description

The ZL30131 OC-192/STM-64 PDH/SONET/SDH/10GbE Network Interface Synchronizer is a highly integrated device that provides timing for both PDH/SONET/SDH and Ethernet network interface cards. A functional block diagram is shown in Figure 1.

This device is ideally suited for designs that require both a transmit timing path (backplane to PHY) and a receive timing path (PHY to backplane). Each path is controlled with separate DPLLs (Tx DPLL, Rx DPLL) which are both independently configurable through the serial interface (SPI or I²C). A typical application of the ZL30131 is shown in Figure 2. In this application, the ZL30131 translates the 19.44 MHz clock from the telecom rate backplane (system timing bus), translates the frequency to 622.08 MHz or 156.25 MHz for the PHY Tx clock, and filters the jitter to ensure compliance with the related standards. A programmable synthesizer (P0) provides synchronous PDH clocks with multiples of 8 kHz for generating PDH interface clocks. On the receive path, the Rx DPLL and the P1 synthesizer translate the line recovered clock (8 kHz or 25 MHz) from the PHY to the 19.44 MHz telecom backplane (line recovered timing) for the central timing cards. The ZL30131 allows easy integration of Ethernet line rates with today's telecom backplanes.

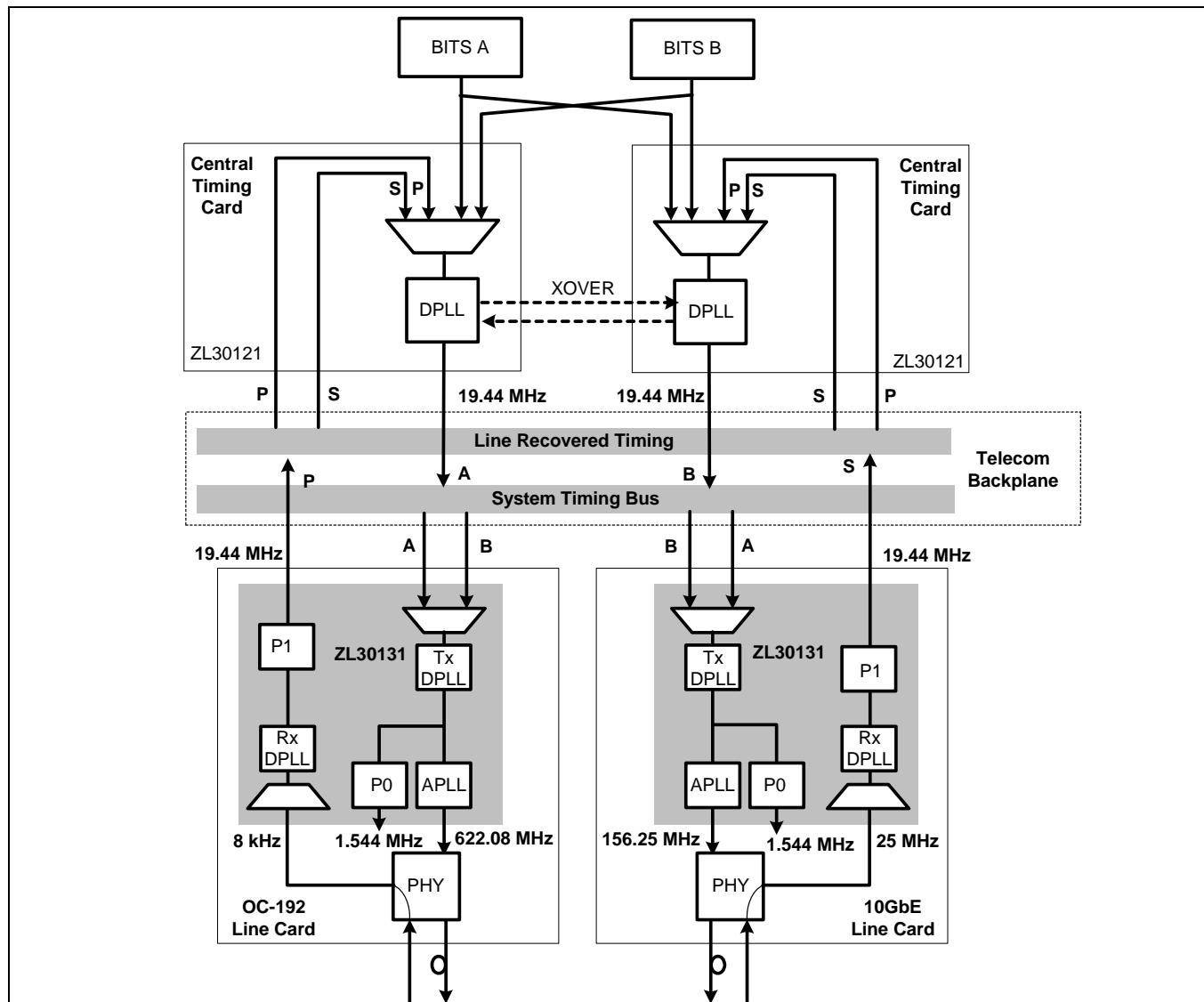
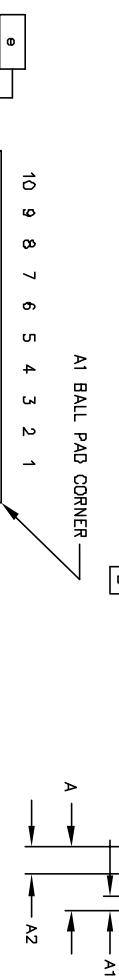
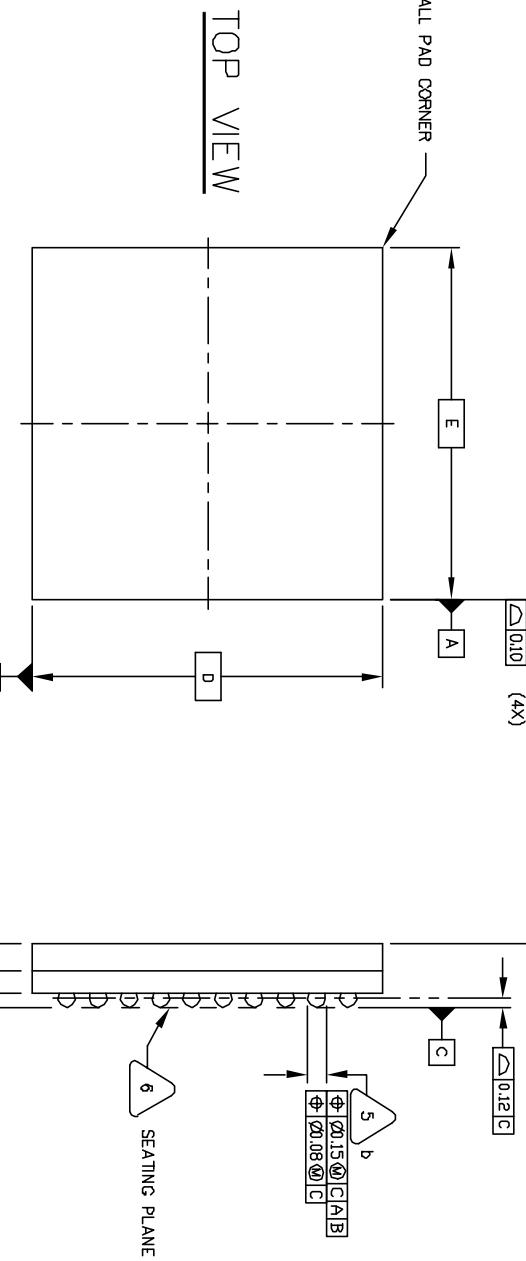


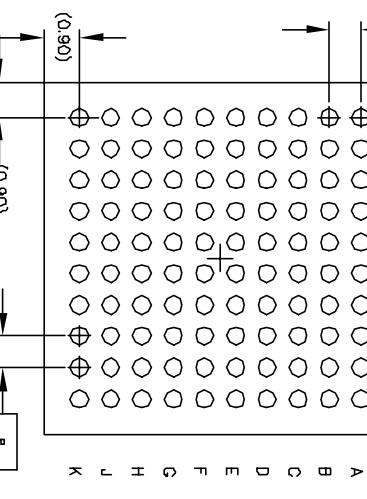
Figure 2 - Typical Application of the ZL30131

MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46	Typ.	
D	9.00	Ref.	
e	0.8	Ref	
n	100		



SIDE VIEW

BOTTOM VIEW



6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 100.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 0.8mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994

NOTES: UNLESS OTHERWISE SPECIFIED

© Zarlink Semiconductor 2005 All rights reserved.

ISSUE 1

ACN CDCA

DATE 15April05

APPRD.



ZARLINK
SEMICONDUCTOR

Package Code GG

Previous package codes N/A

Package Outline for 100ball 9x9mm, 0.8 mm Pitch, 4 layer, CABGA

111040



**For more information about all Zarlink products
visit our Web Site at**

www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE



**For more information about all Zarlink products
visit our Web Site at**

www.zarlink.com

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE