ZARLINK™ SEMICONDUCTOR

ZL50021
Enhanced 4 K Digital Switch with Stratum 3 DPLL

Data Sheet

Features

January 2006

- 4096-channel x 4096-channel non-blocking digital Time Division Multiplex (TDM) switch at 8.192 and 16.384 Mbps or using a combination of ports running at 2.048, 4.096, 8.192 and/or 16.384 Mbps
- 32 serial TDM input, 32 serial TDM output streams
- Integrated Digital Phase-Locked Loop (DPLL) exceeds Telcordia GR-1244-CORE Stratum 3 specifications
- Output clocks have less than 1 ns of jitter (except for the 1.544 MHz output)
- DPLL provides holdover, freerun and jitter attenuation features with four independent reference source inputs

Ordering Information

ZL50021GAC	256 Ball PBGA	Trays
ZL50021QCC	256 Lead LQFP	Trays
ZL50021GAG2	256 Ball PBGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

- Programmable key DPLL parameters (filter corner frequency, locking range, auto-holdover hysteresis range, phase slope, lock detector range)
- Exceptional input clock cycle to cycle variation tolerance (20 ns for all rates)
- Output streams can be configured as bi-directional for connection to backplanes

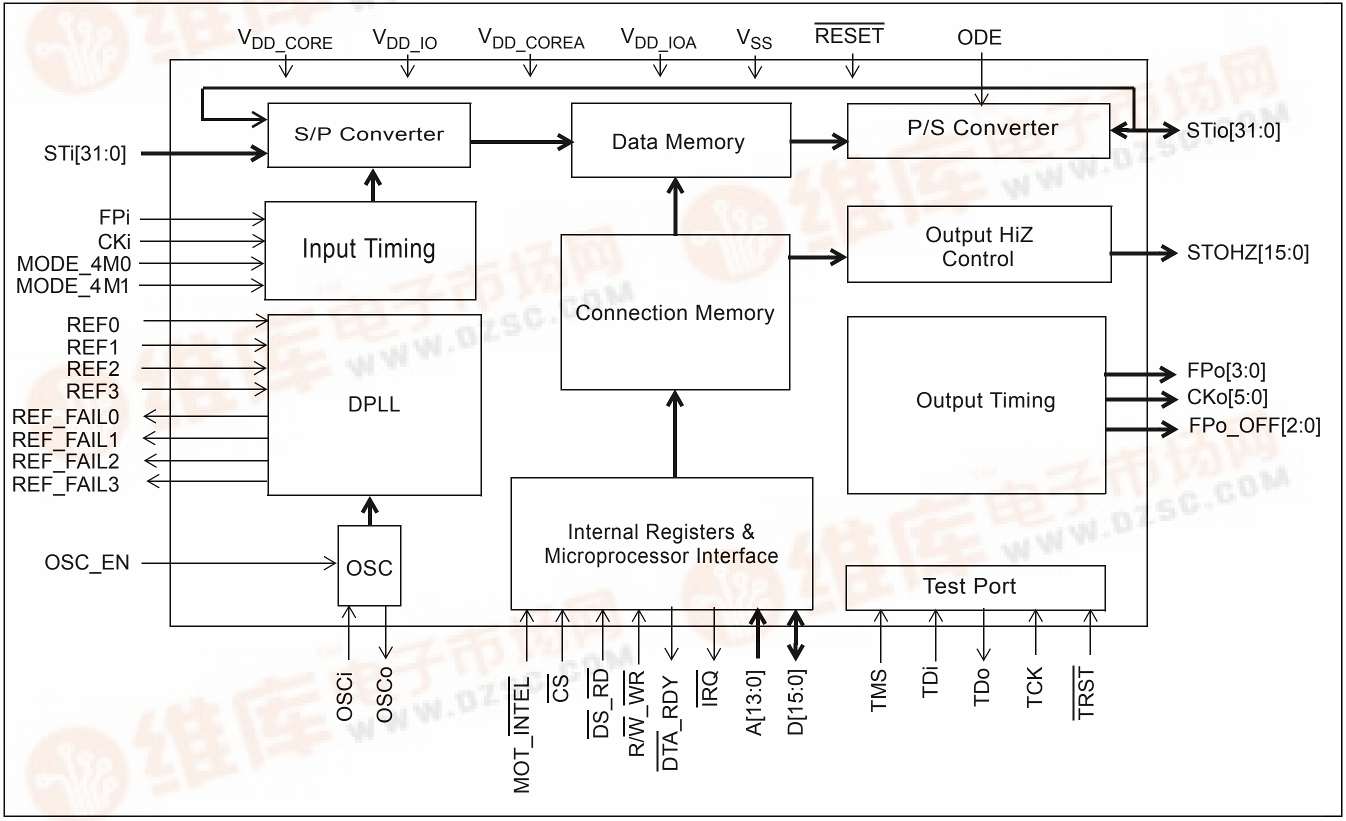

Figure 1 - ZL50021 Functional Block Diagram

Zarlink Semiconductor US Patent No. 5,602,884, UK Patent No. 0772912, France Brevete S.G.D.G. 0772912; Germany DBP No. 69502724.7-08

- Per-stream input and output data rate conversion selection at 2.048, 4.096, 8.192 or 16.384 Mbps. Input and output data rates can differ
- Per-stream high impedance control outputs (STOHZ) for up to 16 output streams
- Per-stream input bit delay with flexible sampling point selection
- Per-stream output bit and fractional bit advancement
- Per-channel ITU-T G.711 PCM A-Law/μ-Law Translation
- Multiple frame pulse and reference clock outputs
- Input clock: 4.096 MHz, 8.192 MHz, 16.384 MHz
- Input frame pulses: 61 ns, 122 ns, 244 ns
- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per Stream Bit Error Rate Test circuits
- Per-channel high impedance output control
- Per-channel message mode
- Control interface compatible with Intel and Motorola 16-bit non-multiplexed buses
- Connection memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE-1149.1 (JTAG) test port
- 3.3 V I/O with 5 V tolerant inputs; 1.8 V core voltage

Applications

- PBX and IP-PBX
- Small and medium digital switching platforms
- Wireless base stations and controllers
- Remote access servers and concentrators
- Multi service access platforms
- Digital Loop Carriers
- Computer Telephony Integration

Description

The ZL50021 is a maximum 4,096 x 4,096 channel non-blocking digital Time Division Multiplex (TDM) switch. It has thirty-two input streams (STi0 - 31) and thirty-two output streams (STio0 - 31). The device can switch 64 kbps and Nx64 kbps TDM channels from any input stream to any output stream. Each of the input and output streams can be independently programmed to operate at any of the following data rates: 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps. The ZL50021 provides up to sixteen high impedance control outputs (STOHZ0 - 15) to support the use of external tristate drivers for the first sixteen output streams (STio0 - 15). The output streams can be configured to operate in bi-directional mode, in which case STi0 - 31 will be ignored.

The device contains two types of internal memory - data memory and connection memory. There are four modes of operation - Connection Mode, Message Mode, BER Mode and High Impedance Mode. In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (the actual data to be output is stored in the data memory). In Message Mode, the connection memory is used for the storage of microprocessor data. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the data output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices. In BER mode the output channel data is replaced with a pseudorandom bit sequence (PRBS) from one of 32 PRBS generators that generates a 2^{15}-1 pattern. On the input side channels can be routed to one of 32 bit error detectors. In high impedance mode the selected output channel can be put into a high impedance state.

When the device is operating as a timing master, the internal digital PLL is in use. In this mode, an external 20.000 MHz crystal is required for the on-chip crystal oscillator. The DPLL is phase-locked to one of four input reference signals (which can be 8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz provided on REF0 - 3). The on-chip DPLL operates in normal, holdover or freerun mode and offers jitter attenuation. The jitter attenuation function exceeds the Stratum 3 specification.

The configurable non-multiplexed microprocessor port allows users to program various device operating modes and switching configurations. Users can employ the microprocessor port to perform register read/write, connection memory read/write, and data memory read operations. The port is configurable to interface with either Motorola or Intel-type microprocessors.

The device also supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

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Changes Summary

The following table captures the changes from the October 2004 issue.

Page	Item	Change
39, 77, 79	Section 12.1, "DPLL Timing Modes" on page 39 RCCR Register bits "FDM1 - 0" on page 77 RCSR Register bits "DPM1 - 0" on page 79	• The on-chip DPLL's normal, holdover, automatic, and freerun modes are now collectively referred to as DPLL timing modes instead of operation modes. This change is to avoid confusion with the two main device operating modes; the master and slave modes.
40, 41	Section 12.1.3.1, "Automatic Reference Switching Without Preferences" on page 40 and Section 12.1.3.2, "Automatic Reference Switching With Preference" on page 41	• Section 12.1.3.1 and Section 12.1.3.2 added to clarify the DPLL's automatic reference switching with and without preference operations in Automatic Timing Mode.
43, 46	Section 12.1.4, "Freerun Mode" on page 43, and Section 15.4, "Fast Locking Mode" on page 46	• Added description to specify that the device should not be in freerun and fast lock modes simultaneously. This is important in order to avoid incorrect output frame pulse generation.
73	Table 36, Lock Detector Threshold Register (LDTR) Bits	• Clarified threshold calculations.
75	Table 39, "Bandwidth Control Register (BWCR) Bits" Note 3.	• Added a table footnote to specify that the DPLL's fastlock and freerun modes should not be set simultaneously.
76	Table 40, "Reference Change Control Register (RCCR) Bits" Bits "PRS1 - 0" and Bits "PMS2 - 0"	• Added description to clarify that only two consecutive references can be used in automatic timing mode with a preferred reference.
77	Table 40, "Reference Change Control Register (RCCR) Bits", Bits "FDM1 - 0"	• Added description to specify that the DPLL's fastlock and freerun modes should not be set simultaneously.

1.0 Pinout Diagrams

1.1 BGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	STi29	STi28	STi27	STi25	STi26	STi24	NC	NC	STio22	STio23	STio21	STio20	NC	NC	V_{SS}	A
B	STi31	STi10	STi5	STi4	CKo2	STi0	CKo0	REF2	V_{DD_COREA}	FPi	CKi	IC_OPEN	IC_OPEN	OSCi	ODE	STio19	B
C	STi30	STi9	V_{SS}	STi7	STi6	STi1	CKo1	REF_FAIL2	V_{SS}	IC_OPEN	IC_OPEN	OSCo	IC_GND	V_{SS}	STio15	STio18	C
D	STi17	STi11	V_{DD_IO}	STi3	STi2	CKo4	REF3	REF1	REF_FAIL0	V_{SS}	FPo_OFF1	OSC_EN	STio13	V_{DD_IO}	STio14	STio16	D
E	STi16	STi14	STi8	V_{DD_IO}	V_{SS}	V_{DD_CORE}	REF_FAIL3	REF_FAIL1	REF0	NC	V_{DD_CORE}	V_{SS}	V_{DD_IO}	STio12	FPo2	STio17	E
F	STi19	STi15	STi12	STi13	V_{DD_IO}	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_IO}	IC_OPEN	FPo3	FPo_OFF2	STOHZ15	F
G	STi18	$\overline{\text{RESET}}$	IC_GND	IC_OPEN	TDo	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	A12	A13	FPo1	FPo0	STOHZ14	G
H	STi21	V_{SS}	V_{SS}	V_{DD_COREA}	CKo5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A7	A9	A10	FPo_OFF0	A11	STOHZ12	H
J	STi20	V_{DD_IOA}	V_{DD_IOA}	V_{SS}	V_{SS}	CKo3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A3	A4	A5	A8	A6	STOHZ13	J
K	STi22	V_{SS}	TMS	V_{SS}	V_{DD_COREA}	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	IC_OPEN	A0	A2	A1	STOHZ11	K
L	STi23	V_{DD_COREA}	$\overline{\text{TRST}}$	TCK	V_{DD_IO}	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_IO}	STio10	STio11	STio9	STOHZ10	L
M	STio25	NC	TDi	D0	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	D6	D10	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	$\overline{\text{MOT}}$_INTEL	MODE_4M0	STio8	STOHZ9	M
N	STio24	NC	V_{DD_IO}	STio0	STOHZ3	D1	D5	D7	D11	D13	R/$\overline{\text{W}}$_WR	$\overline{\text{DTA}}$_RDY	STio4	V_{DD_IO}	STOHZ5	STOHZ8	N
P	STio26	NC	V_{SS}	STio1	STio3	STOHZ1	D3	D8	D14	$\overline{\text{IRQ}}$	STio5	STOHZ4	STOHZ6	V_{SS}	STOHZ7	NC	P
R	STio27	NC	STOHZ0	STio2	STOHZ2	D2	D4	D9	D12	D15	$\overline{\text{CS}}$	$\overline{\text{DS}}$_$\overline{\text{RD}}$	MODE_4M1	STio6	STio7	NC	R
T	V_{SS}	STio28	STio29	STio31	STio30	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: A1 corner identified by metallized marking.

Note: Pinout is shown as viewed through top of package.

Figure 2 - ZL50021 256-Ball 17 mm x 17 mm PBGA (as viewed through top of package)

1.2 QFP Pinout

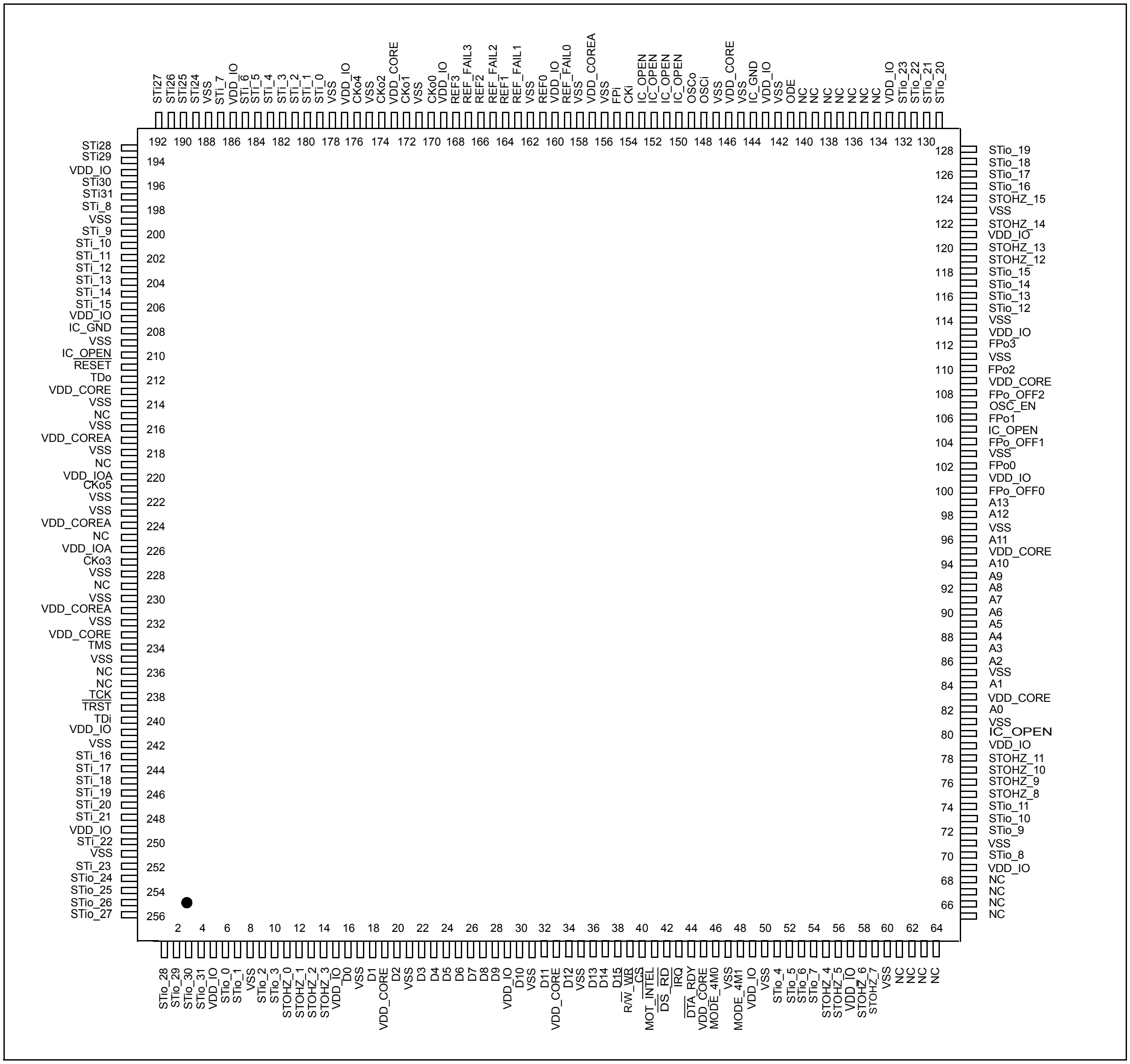


Figure 3 - ZL50021 256-Lead 28 mm x 28 mm LQFP (top view)

2.0 Pin Description

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
E6, E11, F6, F7, F10, F11, L6, L7, L10, L11, M6, M7, M10, M11	19, 33, 45, 83, 95, 109, 146, 173, 213, 233	V_{DD_CORE}	**Power Supply for the core logic:** +1.8 V
H4, K5, B9, L2	217, 231, 157, 224	V_{DD_COREA}	**Power Supply for analog circuitry:** +1.8V
D3, D14, E4, E13, F5, F12, G6, G11, K6, K11, L5, L12, N3, N14	5, 15, 29, 49, 57, 69, 79, 101, 113, 121, 133, 143, 160, 169, 177, 186, 195, 207, 241, 249	V_{DD_IO}	**Power Supply for I/O:** +3.3 V
J2, J3	220, 226	V_{DD_IOA}	**Power Supply for the CKo5 and CKo3 outputs:** +3.3V
A1, A16, C3, C9, C14, D10, E5, E12, F8, F9, G7, G8, G9, G10, H2, H3, H6, H7, H8, H9, H10, J4, J5, J7, J8, J9, J10, K2, K4, K7, K8, K9, K10, L8, L9, M5, M12, P3, P14, T1, T16	8, 17, 21, 31, 35, 47, 50, 60, 71, 81, 85, 97, 103, 111, 114, 123, 142, 145, 147, 156, 158, 162, 171, 175, 178, 188, 199, 209, 214, 216, 218, 222, 223, 228, 230, 232, 235, 242, 251	V_{SS}	**Ground**

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
K3	234	TMS	**Test Mode Select (5 V-Tolerant Input with Internal Pull-up):** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.
L4	238	TCK	**Test Clock (5 V-Tolerant Schmitt-Triggered Input with Internal Pull-up):** Provides the clock to the JTAG test logic.
L3	239	$\overline{\text{TRST}}$	**Test Reset (5 V-Tolerant Input with Internal Pull-up):** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation.
M3	240	TDi	**Test Serial Data In (5 V-Tolerant Input with Internal Pull-up):** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up resistor when it is not driven.
G5	212	TDo	**Test Serial Data Out (5 V-Tolerant Three-state Output):** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
B12, B13, C10, C11, F13, G4, K12	80, 105, 150, 151, 152, 153, 210	IC_OPEN	**Internal Test Mode (5V-Tolerant Input with Internal Pull-down):** These pins may be left unconnected.
C13, G3	144, 208	IC_GND	**Internal Test Mode Enable (5 V-Tolerant Input):** These pins **MUST** be low.
A8, A9, A14, A15, E10, M2, N2, P2, P16, R2, R16, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15	61, 62, 63, 64, 65, 66, 67, 68, 134, 135, 136, 137, 138, 139, 140, 215, 219, 225, 229, 236, 237	NC	**No Connect:** These pins **MUST** be left unconnected.
M14, R13	46, 48	MODE_4M0, MODE_4M1	**4M Input Clock Mode 0 to 1 (5V-Tolerant Input with internal pull-down)** These two pins should be tied together and are typically used to select CKi = 4.096MHz operation. See Table 7, “ZL50021 Operating Modes” on page 38 for a detailed explanation. See Table 18, “Control Register (CR) Bits” on page 56 for CKi and FPi selection using the CKIN1 - 0 bits.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
D12	107	OSC_EN	**Oscillator Enable (5 V-Tolerant Input with Internal Pull-down):** If tied high, this pin indicates that there is a 20 MHz external oscillator interfacing with the device. If tied low, there is no oscillator and CKi will be used for master clock generation. If the DPLL is activated, an external oscillator is required and this pin **MUST** be tied high.
C12	149	OSCo	**Oscillator Clock Output (3.3 V Output)** If OSC_EN = ‘1’, this pin should be connected to a 20 MHz crystal (see Figure 23 on page 105) or left unconnected if a clock oscillator is connected to OSCi pin under normal operation (see Figure 24 on page 106). If OSC_EN = 0, this pin **MUST** be left unconnected.
B14	148	OSCi	**Oscillator Clock Input (3.3 V Input)** If OSC_EN = ‘1’, this pin should be connected to a 20 MHz crystal (see Figure 23 on page 105) or to a clock oscillator under normal operation (see Figure 24 on page 106). If OSC_EN = 0, this pin **MUST** be driven high or low by connecting either to V_{DD_IO} or to ground.
E9, D8, B8, D7	161, 164, 166, 168	REF0 - 3	**DPLL Reference Inputs 0 to 3 (5 V-Tolerant Schmitt-Triggered Inputs)** If the device is in Master mode, these input pins accept 8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz timing references independently. One of these inputs is defined as the preferred or forced input reference for the DPLL. The Reference Change Control Register (RCCR) selects the control of the preferred reference. These pins are ignored if the device is in slave mode unless SLV_DPLLEN (bit 13) in the Control Register (CR) is set. When these input pins are not in use, they **MUST** be driven high or low by connecting either to V_{DD_IO} or to ground.
D9, E8, C8, E7	159, 163, 165, 167	REF_FAIL0 - 3	**Failure Indication for DPLL References 0 to 3 (5 V-Tolerant Three-state Outputs)** These output pins are used to indicate input reference failure when the device is in master mode. If REF0 fails, REF_FAIL0 will be driven high. If REF1 fails, REF_FAIL1 will be driven high. If REF2 fails, REF_FAIL2 will be driven high. If REF3 fails, REF_FAIL3 will be driven high. If the device is in slave mode, these pins are driven low, unless SLV_DPLLEN (bit 13) in the Control Register (CR) is set.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
G15, G14, E15, F14	102, 106, 110, 112	FPo0 - 3	**ST-BUS/GCI-Bus Frame Pulse Outputs 0 to 3 (5 V-Tolerant Three-state Outputs)** FPo0: 8 kHz frame pulse corresponding to the 4.096 MHz output clock of CKo0. FPo1: 8 kHz frame pulse corresponding to the 8.192 MHz output clock of CKo1. FPo2: 8 kHz frame pulse corresponding to 16.384 MHz output clock of CKo2. FPo3: Programmable 8 kHz frame pulse corresponding to 4.096 MHz, 8.192 MHz, 16.384 MHz, or 32.768 MHz output clock of CKo3. In Divided Slave modes, the frame pulse width of FPo0 - 3 cannot be narrower than the input frame pulse (FPi) width.
H14, D11	100, 104	FPo_OFF0 - 1	**Generated Offset Frame Pulse Outputs 0 to 1 (5 V-Tolerant Three-state Outputs)** Individually programmable 8 kHz frame pulses, offset from the output frame boundary by a programmable number of channels.
F15	108	FPo_OFF2 or FPo5	**Generated Offset Frame Pulse Output 2 or 19.44 MHz Frame Pulse Output (5 V-Tolerant Three-state Output)** As FPo_OFF2, this is an individually programmable 8 kHz width frame pulse, offset from the output frame boundary by a programmable number of channels. By programming the FP19EN (bit 10) of FPOFF2 register to high, this signal becomes FPo5, a non-offset frame pulse corresponding to the 19.44 MHz clock presented on CKo5. FPo5 is only available in Master mode or when the SLV_DPLLEN bit in the Control Register is set high while the device is in one of the slave modes.
B7, C7, B5, J6, D6, H5	170, 172, 174, 227, 176, 221	CKo0 - 5	**ST-BUS/GCI-Bus Clock Outputs 0 to 5 (5 V-Tolerant Three-state Outputs)** CKo0: 4.096 MHz output clock. CKo1: 8.192 MHz output clock. CKo2: 16.384 MHz output clock. CKo3: 4.096 MHz, 8.192 MHz, 16.384 MHz or 32.768 MHz programmable output clock CKo4: 1.544 MHz or 2.048 MHz programmable output clock CKo5: 19.44 MHz output clock See Section 6.0 on page 24 for details. In Divided Slave mode, the frequency of CKo0 - 3 cannot be higher than input clock (CKi). CKo4 and CKo5 are only available in Master mode or when the SLV_DPLLEN bit in the Control Register is set high while the device is in one of the slave modes.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
B10	155	FPi	**ST-BUS/GCI-Bus Frame Pulse Input (5 V-Tolerant Schmitt-Triggered Input)** This pin accepts the frame pulse which stays active for 61 ns, 122 ns or 244 ns at the frame boundary. The frame pulse frequency is 8 kHz. The frame pulse associated with the **highest input or output** data rate must be applied to this pin when the device is operating in Divided Slave mode or Master mode. The exception is if the device is operating in Master mode with loopback (i.e., CKi_LP is set in the Control Register). In that case, this input must be tied high or low externally. When the device is operating in Multiplied Slave mode, the frame pulse associated with the **highest input** data rate must be applied to this pin. For all modes (except Master mode with loopback), if the data rate is 16.384 Mbps, a 61 ns wide frame pulse must be used. By default, the device accepts a negative frame pulse in ST-BUS format, but it can accept a positive frame pulse instead if the FPINP bit is set high in the Control Register (CR). It can accept a GCI-formatted frame pulse by programming the FPINPOS bit in the Control Register (CR) to high.
B11	154	CKi	**ST-BUS/GCI-Bus Clock Input (5 V-Tolerant Schmitt Triggered Input)** This pin accepts a 4.096 MHz, 8.192 MHz or 16.384 MHz clock. The clock frequency associated with **twice the highest input or output** data rate must be applied to this pin when the device is operating in either Divided Slave mode or Master mode. The exception is if the device is operating in Master mode with loopback (i.e., CKi_LP is set in the Control Register). In that case, this input must be tied high or low externally. The clock frequency associated with **twice the highest input** data rate must be applied to this pin when the device is operating in Multiplied Slave mode. In all modes of operation (except Master mode with loopback), when data is running at 16.384 Mbps, a 16.384 MHz clock must be used. By default, the clock falling edge defines the input frame boundary, but the device allows the clock rising edge to define the frame boundary by programming the CKINP bit in the Control Register (CR).

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
B6, C6, D5, D4, B4, B3, C5, C4, E3, C2, B2, D2, F3, F4, E2, F2, E1, D1, G1, F1, J1, H1, K1, L1, A7, A5, A6, A4, A3, A2, C1, B1	179, 180, 181, 182, 183, 184, 185, 187, 198, 200, 201, 202, 203, 204, 205, 206, 243, 244, 245, 246, 247, 248, 250, 252, 189, 190, 191, 192, 193, 194, 196, 197	STi0 -31	**Serial Input Streams 0 to 31 (5 V-Tolerant Inputs with Enabled Internal Pull-downs)** The data rate of each input stream can be selected independently using the Stream Input Control Registers (SICR[n]). In the 2.048 Mbps mode, these pins accept serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins accept serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins accept serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins accept TDM data streams at 16.384 Mbps with 256 channels per frame.
N4, P4, R4, P5, N13, P11, R14, R15, M15, L15, L13, L14, E14, D13, D15, C15, D16, E16, C16, B16, A13, A12, A10, A11, N1, M1, P1, R1, T2, T3, T5, T4	6, 7, 9, 10, 51, 52, 53, 54, 70, 72, 73, 74, 115, 116, 117, 118, 125, 126, 127, 128, 129, 130, 131, 132, 253, 254, 255, 256, 1, 2, 3, 4	STio0 - 31	**Serial Output Streams 0 to 31 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os with Enabled Internal Pull-downs)** The data rate of each output stream can be selected independently using the Stream Output Control Registers (SOCR[n]). In the 2.048 Mbps mode, these pins output serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins output serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins output serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins output serial TDM data streams at 16.384 Mbps with 256 channels per frame. These output streams can be used as bi-directionals by programming BDH (bit 7) and BDL (bit 6) of Internal Mode Selection (IMS) register.
R3, P6, R5, N5, P12, N15, P13, P15, N16, M16, L16, K16, H16, J16, G16, F16	11, 12, 13, 14, 55, 56, 58, 59, 75, 76, 77, 78, 119, 120, 122, 124	STOHZ0 - 15	**Serial Output Streams High Impedance Control 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state Outputs)** These pins are used to enable (or disable) external three-state buffers. When an output channel is in the high impedance state, the STOHZ drives high for the duration of the corresponding output channel. When the STio channel is active, the STOHZ drives low for the duration of the corresponding output channel. STOHZ outputs are available for STio0 - 15 only.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
B15	141	ODE	**Output Drive Enable (5 V-Tolerant Input with Internal Pull-up)** This is the output enable control for STio0 - 31 and the output-driven-high control for STOHZ0 - 15. When it is high, STio0 - 31 and STOHZ0 - 15 are enabled. When it is low, STio0 - 31 are tristated and STOHZ0 - 15 are driven high.
M4, N6, R6, P7, R7, N7, M8, N8, P8, R8, M9, N9, R9, N10, P9, R10	16, 18, 20, 22, 23, 24, 25, 26, 27, 28, 30, 32, 34, 36, 37, 38	D0 - 15	**Data Bus 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os):** These pins form the 16-bit data bus of the microprocessor port.
N12	44	$\overline{\text{DTA}}$_RDY	**Data Transfer Acknowledgment_Ready (5 V-Tolerant Three-state Output)** This active low output indicates that a data bus transfer is complete for the Motorola interface. For the Intel interface, it indicates a transfer is completed when this pin goes from low to high. An external pull-up resistor **MUST** hold this pin at HIGH level for the Motorola mode. An external pull-down resistor **MUST** hold this pin at LOW level for the Intel mode.
R11	40	$\overline{\text{CS}}$	**Chip Select (5 V-Tolerant Input)** Active low input used by the Motorola or Intel microprocessor to enable the microprocessor port access.
N11	39	R/$\overline{\text{W}}$_$\overline{\text{WR}}$	**Read/Write_Write (5 V-Tolerant Input)** This input controls the direction of the data bus lines (D0 - 15) during a microprocessor access. For the Motorola interface, this pin is set high and low for the read and write access respectively. For the Intel interface, a write access is indicated when this pin goes low.
R12	42	$\overline{\text{DS}}$_$\overline{\text{RD}}$	**Data Strobe_Read (5 V-Tolerant Input):** This active low input works in conjunction with $\overline{\text{CS}}$ to enable the microprocessor port read and write operations for the Motorola interface. A read access is indicated when it goes low for the Intel interface.
K13, K15, K14, J11, J12, J13, J15, H11, J14, H12, H13, H15, G12, G13	82, 84, 86, 87, 88, 89, 90, 91, 92, 93, 94, 96, 98, 99	A0 - 13	**Address 0 to 13 (5 V-Tolerant Inputs):** These pins form the 14-bit address bus to the internal memories and registers.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
M13	41	MOT_$\overline{\text{INTEL}}$	**Motorola_Intel (5 V-Tolerant Input with Internal Pull-up)** This pin selects the Motorola or Intel microprocessor interface to be connected to the device. When this pin is unconnected or connected to high, Motorola interface is assumed. When this pin is connected to ground, Intel interface should be used.
P10	43	$\overline{\text{IRQ}}$	**Interrupt (5 V-Tolerant Three-state Output):** This programmable active low output indicates that the internal operating status of the DPLL has changed. An external pull-up resistor **MUST** hold this pin at HIGH level.
G2	211	$\overline{\text{RESET}}$	**Device Reset (5 V-Tolerant Input with Internal Pull-up)** This input (active LOW) puts the device in its reset state that disables the STio0 - 31 drivers and drives the STOHZ0 - 15 outputs to high. It also preloads registers with default values and clears all internal counters. To ensure proper reset action, the reset pin must be low for longer than 1 µs. Upon releasing the reset signal to the device, the first microprocessor access cannot take place for at least 600 µs due to the time required to stabilize the device and the crystal oscillator from the power-down state. Refer to Section Section 17.2 on page 49 for details.

3.0 Device Overview

The device has thirty-two ST-BUS/GCI-Bus inputs (STi0 - 31) and thirty-two ST-BUS/GCI-Bus outputs (STio0 - 31). STio0 - 31 can also be configured as bi-directional pins, in which case STi0 - 31 will be ignored. It is a non-blocking digital switch with 4096 64 kbps channels and is capable of performing rate conversion between ST-BUS/GCI-Bus inputs and ST-BUS/GCI-Bus outputs. The ST-BUS/GCI-Bus inputs accept serial input data streams with data rates of 2.048, 4.096, 8.192 and 16.384 Mbps on a per-stream basis. The ST-BUS/GCI-Bus outputs deliver serial data streams with data rates of 2.048, 4.096, 8.192 and 16.384 Mbps on a per-stream basis. The device also provides sixteen high impedance control outputs (STOHZ0 - 15) to support the use of external ST-BUS/GCI-Bus tristate drivers for the first sixteen ST-BUS/GCI-Bus outputs (STio0 -15).

By using Zarlink's message mode capability, microprocessor data stored in the connection memory can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The device uses the ST-BUS/GCI-Bus input frame pulse (FPi) and the ST-BUS/GCI-Bus input clock (CKi) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams with various data rates. The output data streams will be driven by and have their timing defined by FPi and CKi in Divided Slave mode. In Multiplied Slave mode, the output data streams will be driven by an internally generated clock, which is multiplied from CKi internally. In Master mode, the on-chip DPLL will drive the output data streams and provide output clocks and frame pulses. Refer to Application Note ZLAN-120 for further explanation of the different modes of operation.

When the device is in Master mode, the DPLL is phase-locked to one of four DPLL reference signals, REF0 - 3, which are sourced by an external 8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz reference signal. The on-chip DPLL also offers jitter attenuation, reference switching, reference monitoring, freerun and holdover functions. The jitter performance exceeds the Stratum 3 specification. The intrinsic jitter of all output clocks is less than 1 ns (except for the 1.544 MHz output).

There are two slave modes for this device:

The first is the Divided Slave mode. In this mode, output streams are clocked by input CKi. Therefore the output streams have exactly the same jitter as the input streams. The output data rate can be the same as or lower than the input data rate, but the output data rate cannot be higher than what CKi can drive. For example, if CKi is 4.096 MHz, the output data rate cannot be higher than 2.048 Mbps. The second slave mode is called Multiplied Slave mode. In this mode, CKi is used to generate a 16.384 MHz clock internally, and output streams are driven by this 16.384 MHz clock. In Multiplied Slave mode, the data rate of output streams can be any rate, but output jitter may not be exactly the same as input jitter.

A Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port has a 16-bit data bus, a 14-bit address bus and six control signals (MOT_$\overline{\text{INTEL}}$, $\overline{\text{CS}}$, $\overline{\text{DS}}$_$\overline{\text{RD}}$, R/$\overline{\text{W}}$_$\overline{\text{WR}}$, $\overline{\text{IRQ}}$ and $\overline{\text{DTA}}$_RDY).

The device supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

4.0 Data Rates and Timing

The ZL50021 has 32 serial data inputs and 32 serial data outputs. Each stream can be individually programmed to operate at 2.048, 4.096, 8.192 or 16.384 Mbps. Depending on the data rate there will be 32 channels, 64 channels, 128 channels or 256 channels, respectively, during a 125 μs frame.

The output streams can be programmed to operate as bi-directional streams. The output streams are divided into two groups to be programmed into bi-directional mode. By setting BDL (bit 6) in the Internal Mode Selection (IMS) register, input streams 0 - 15 (STi0 - 15) are internally tied low, and output streams 0 - 15 (STio0 - 15) are set to operate in a bi-directional mode. Similarly, when BDH (bit 7) in the Internal Mode Selection (IMS) register is set, input streams 16 - 31 (STi16 - 31) are internally tied low, and output streams 16 - 31 (STio16 - 31) are set to operate in bi-directional mode. The groups do not have to be set into the same mode. Therefore it is possible to have half of the streams operating in bi-directional mode while the other half is operating in normal input/output mode.

The input data rate is set on a per-stream basis by programming STIN[n]DR3 - 0 (bits 3 - 0) in the Stream Input Control Register 0 - 31 (SICR0 - 31). The output data rate is set on a per-stream basis by programming STO[n]DR3 - 0 (bits 3 - 0) in the Stream Output Control Register 0 - 31 (SOCR0 - 31). The output data rates do not have to match or follow the input data rates. The maximum number of channels switched is limited to 4096 channels. If all 32 input streams were operating at 16.384 Mbps (256 channels per stream), this would result in 8192 channels. Memory limitations prevent the device from operating at this capacity. A maximum capacity of 4096 channels will occur if half of the total streams are operating at 16.384 Mbps or all streams are operating at 8.192 Mbps. With all streams operating at 4.096 Mbps, the switching capacity is reduced to 2048 channels. And with all streams operating at 2.048 Mbps, the capacity will be further reduced to 1024 channels. However, as each stream can be programmed to a different data rate, any combination of data rates can be achieved, as long as the total channel count does not exceed 4096 channels. It should be noted that only full stream can be programmed for use. The device does not allow fractional streams.

4.1 External High Impedance Control, STOHZ0 - 15

There are 16 external high impedance control signals, STOHZ0 - 15, that are used to control the external drivers for per-channel high impedance operations. Only the first sixteen ST-BUS/GCI-Bus (STio0 - 15) outputs are provided with corresponding STOHZ signals. The STOHZ outputs deliver the appropriate number of control timeslot channels based on the output stream data rate. Each control timeslot lasts for one channel time. When the ODE pin is high and the OSB (bit 2) of the Control Register (CR) is also high, STOHZ0 - 15 are enabled. When the ODE pin, OSB (bit 2) of the Control Register (CR) or the $\overline{\text{RESET}}$ pin is low, STOHZ0 - 15 are driven high, together with all the ST-BUS/GCI-Bus outputs being tristated. Under normal operation, the corresponding STOHZ outputs of any unused ST-BUS/GCI-Bus channel (high impedance) are driven high. Refer to Figure 18 on page 34.

4.2 Input Clock (CKi) and Input Frame Pulse (FPi) Timing

The input clock for the ZL50021 can be arranged in one of three different ways. These different ways will be explained further in Section 11.1 to Section 11.3 on page 39. Depending on the mode of operation, the input clock, CKi, will be based on the highest data rate of either the input or both the input and output data rates. The user has to program the CKIN1 - 0 (bits 6 - 5) in the Control Register (CR) to indicate the width of the input frame pulse and the frequency of the input clock supplied to the device.

In Master mode and Divided Slave mode, the input clock, CKi, must be at least twice the highest input or output data rate. For example, if the highest input data rate is 4.096 Mbps and the highest output data rate is 8.192 Mbps, the input clock, CKi, must be 16.384 MHz, which is twice the highest overall data rate. The only exception to this is for 16.384 Mbps input or output data. In this case, the input clock, CKi, is equal to the data rate. The input frame pulse, FPi, must always follow CKi.

In Master mode, CKo2 and FPo2 can be programmed to be used as CKi and FPi by setting CKi_LP (bit 10) in the Control Register (CR). This will internally loop back the CKo2 and FPo2 timing. When this bit is set, CKi and FPi must be tied low or high externally.

Highest *Input or Output* Data Rate	**CKIN 1-0 Bits**	**Input Clock Rate (CKi)**	**Input Frame Pulse (FPi)**
16.384 Mbps or 8.192 Mbps	00	16.384 MHz	8 kHz (61 ns wide pulse)
4.096 Mbps	01	8.192 MHz	8 kHz (122 ns wide pulse)
2.048 Mbps	10	4.096 MHz	8 kHz (244 ns wide pulse)

Table 1 - CKi and FPi Configurations for Master and Divided Slave Modes

In Multiplied Slave mode, the input clock, CKi, must be at least twice the highest input data rate, regardless of the output data rate. Following the example above, if the highest input data rate is 4.096 Mbps, the input clock, CKi, must be 8.192 MHz, regardless of the output data rate. The only exception to this is for 16.384 Mbps input data. In this case, the input clock, CKi, is equal to the data rate. The input frame pulse, FPi, must always follow CKi.

Highest *Input* Data Rate	**CKIN 1-0 Bits**	**Input Clock Rate (CKi)**	**Input Frame Pulse (FPi)**
16.384 Mbps or 8.192 Mbps	00	16.384 MHz	8 kHz (61 ns wide pulse)
4.096 Mbps	01	8.192 MHz	8 kHz (122 ns wide pulse)
2.048 Mbps	10	4.096 MHz	8 kHz (244 ns wide pulse)

Table 2 - CKi and FPi Configurations for Multiplied Slave Mode

The ZL50021 accepts positive and negative ST-BUS/GCI-Bus input clock and input frame pulse formats via the programming of CKINP (bit 8) and FPINP (bit 7) in the Control Register (CR). By default, the device accepts the negative input clock format and ST-BUS format frame pulses. However, the switch can also accept a positive-going clock format by programming CKINP (bit 8) in the Control Register (CR). A GCI-Bus format frame pulse can be used by programming FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR).

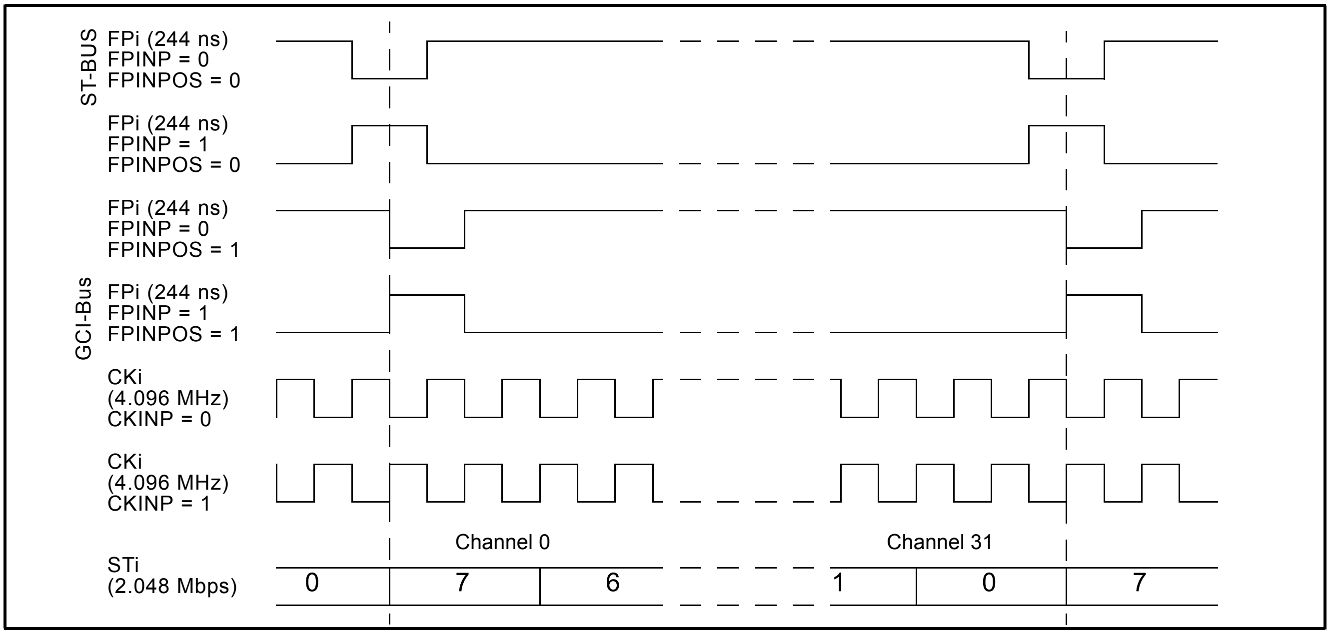


Figure 4 - Input Timing when CKIN1 - 0 bits = “10” in the CR

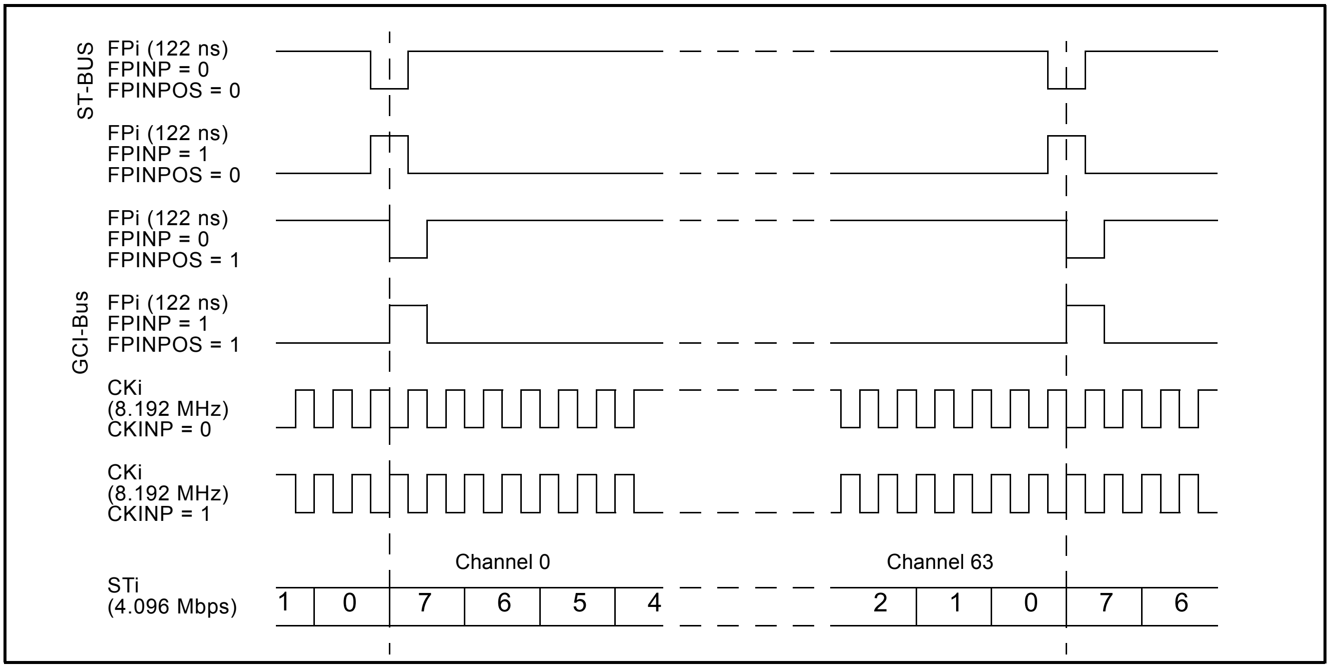


Figure 5 - Input Timing when CKIN1 - 0 bits = “01” in the CR

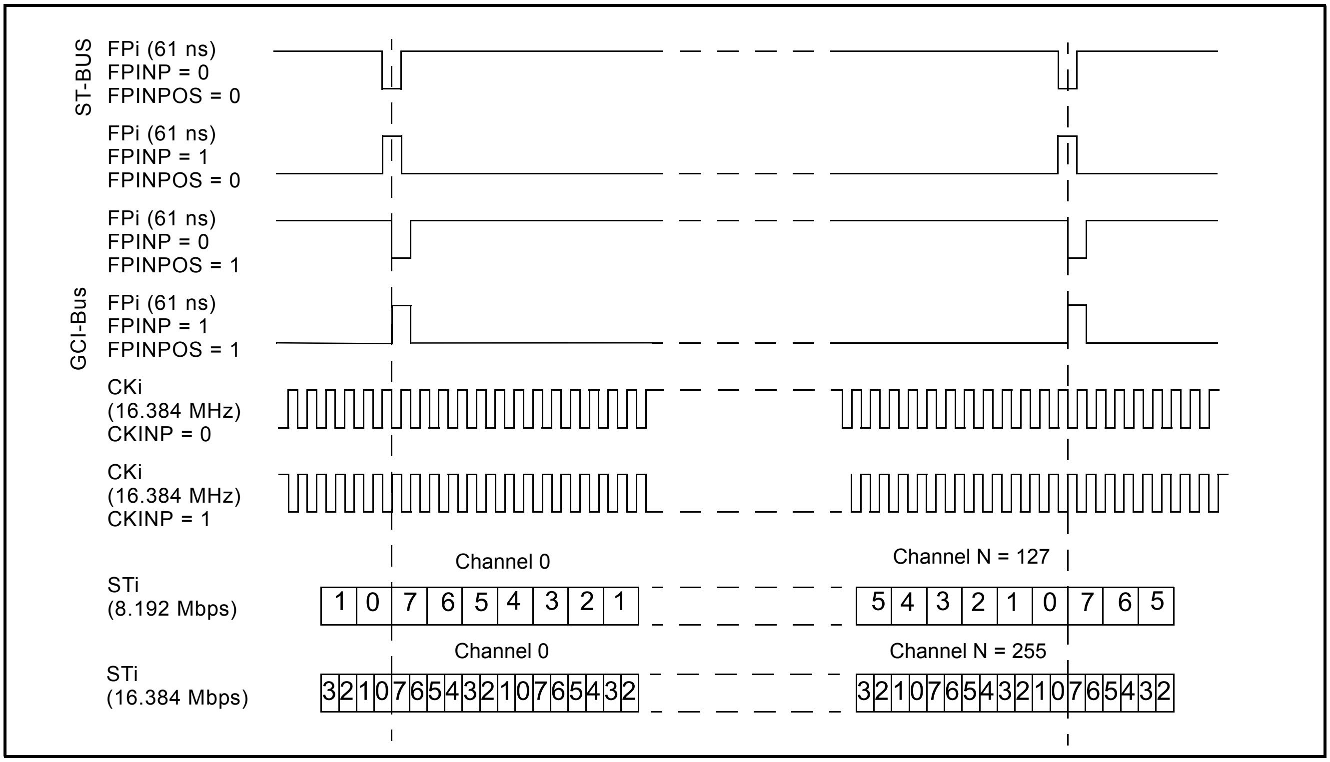


Figure 6 - Input Timing when CKIN1 - 0 = “00” in the CR

5.0 ST-BUS and GCI-Bus Timing

The ZL50021 is capable of operating using either the ST-BUS or GCI-Bus standards. The output timing that the device generates is defined by the bus standard. In the ST-BUS standard, the output frame boundary is defined by the falling edge of CKo while FPo is low. In the GCI-Bus standard, the frame boundary is defined by the rising edge of CKo while FPo goes high. The data rates define the number of channels that are available in a 125 μs frame pulse period.

By default, the ZL50021 is configured for ST-BUS input and output timing. To set the input timing to conform to the GCI-Bus standard, FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR) must be set. To set output timing to conform to the GCI-Bus standard, FPO[n]P and FPO[n]POS must be set in the Output Clock and Frame Pulse Selection Register (OCFSR). The CKO[n]P bits in the Output Clock and Frame Pulse Selection Register control the polarity (positive-going or negative-going) of the output clocks.

6.0 Output Timing Generation

The ZL50021 generates frame pulse and clock timing. There are five output frame pulse pins (FPo0 - 3, 5) and six output clock pins (CKo0 - 5). All output frame pulses are 8 kHz output signals. By default, the output frame boundary is defined by the falling edge of the CKo0, while FPo0 is low. At the output frame boundary, the CKo1, CKo2 and CKo3 output clocks will by default have a falling edge, while FPo1, FPo2 and FPo3 will be low. At the output frame boundary, CKo4 will by default have a falling edge while FPo0 is low (CKo4 has no corresponding output frame pulse). At the output frame boundary, CKo5 will by default have a rising edge while FPo5 (FPo_OFF2) will be low. The duration of the frame pulse low cycle and the frequency of the corresponding output clock are shown in Table 3 on page 25. Every frame pulse and clock output can be tristated by programming the enable bits in the Internal Mode Selection (IMS) register.

Pin Name	Output Timing Rate	Output Timing Unit
FPo0 pulse width	244	ns
CKo0	4.096	MHz
FPo1 pulse width	122	ns
CKo1	8.192	MHz
FPo2 pulse width	61	ns
CKo2	16.384	MHz
FPo3 pulse width	244, 122, 61 or 30	ns
CKo3	4.096, 8.192, 16.384 or 32.768	MHz
CKo4	1.544 or 2.048	MHz
FPo5 pulse width	51	ns
CKo5	19.44	MHz

Table 3 - Output Timing Generation

The output timing is dependent on the operation mode that is selected. When the device is in Divided Slave mode, the frequencies on CKo0 - 3 cannot be greater than the input clock, CKi. For example, if the input clock is 8.192 MHz, the CKo2 pin will not produce a valid output clock and the CKo3 pin can only be programmed to output a 4.096 MHz or 8.192 MHz clock signal. The output clocks CKo4 - 5 will not generate valid outputs unless the SLV_DPLLEN (bit 13) of the Control Register (CR) is set.

In Master mode there are programmable output frame pulse, FPo3, and clock pins, CKo3 and CKo4. The outputs from FPo3 and CKo3 are programmed by the CKOFPO3SEL1 - 0 (bits 13 - 12) in the Output Clock and Frame Pulse Selection (OCFSR) register. The output clock pin, CKo4, is controlled by setting the CKO4SEL (bit 14) in the OCFSR register.

In Multiplied Slave mode, CKo4 and CKo5 are not available unless SLV_DPLLEN is set in the Control Register. All other clocks and frame pulses correspond to the timing shown in Table 3 above.

The device also delivers positive or negative output frame pulse and ST-BUS/GCI-Bus output clock formats via the programming of various bits in the Output Clock and Frame Pulse Selection Register (OCFSR). By default, the device delivers the negative output clock format. The ZL50021 can also deliver GCI-Bus format output frame pulses by programming bits of the Output Clock and Frame Pulse Selection Register (OCFSR). As there is a separate bit setting for each frame pulse output, some of the outputs can be set to operate in ST-BUS mode and others in GCI-Bus mode.

The following figures describe the usage of the FPO0P, FPO1P, FPO2P, FPO3P, CKO0P, CKO1P, CKO2P, CKO3P, CKO4P and CKO5P bits to generate the FPo0 - 3 and CKo0 - 5 timing. FPo_OFF2 is configured to provide the non-offset frame pulse corresponding to the 19.44 MHz clock on CKo5 by setting the FP19EN (bit 10) in the FPOFF2 register. In this instance, FPo_OFF2 can be labeled as FPo5.

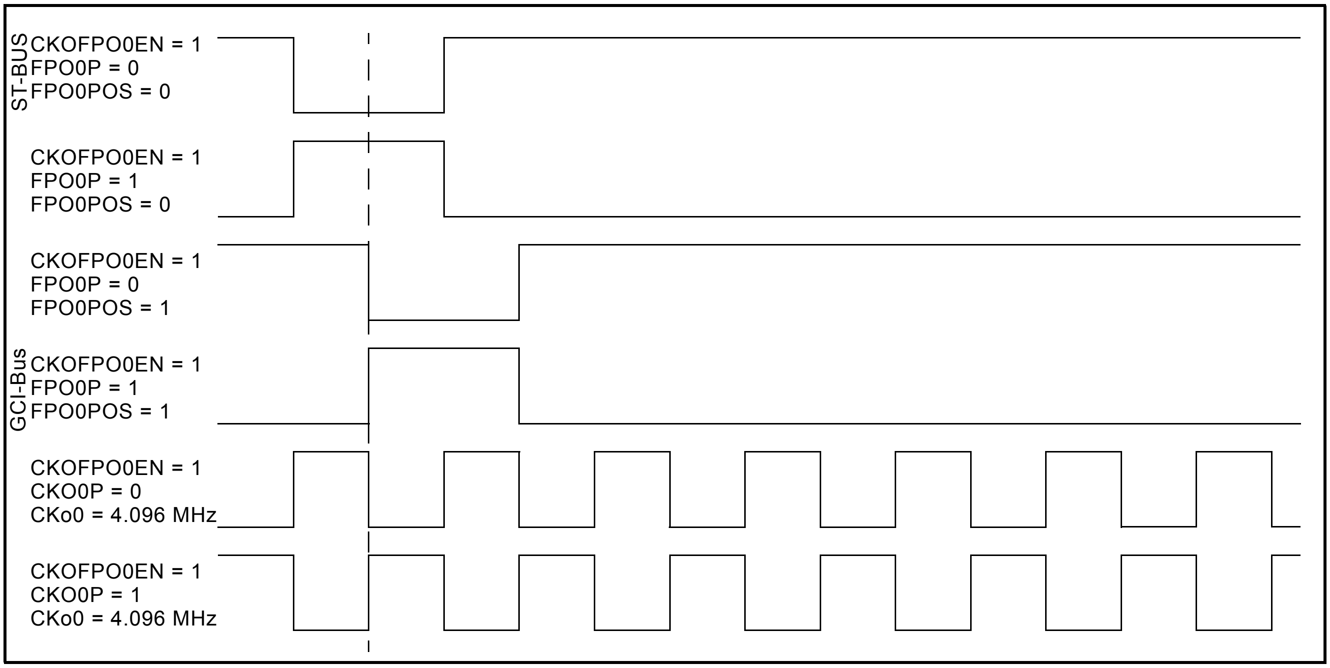


Figure 7 - Output Timing for CKo0 and FPo0

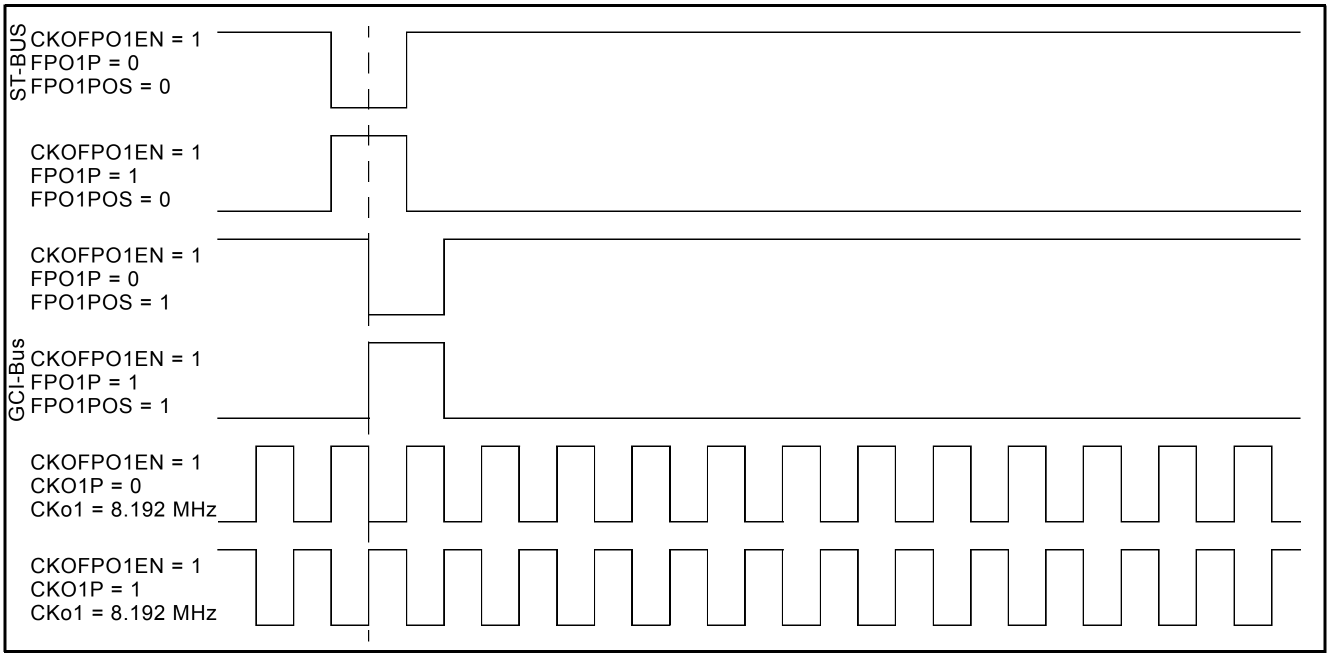


Figure 8 - Output Timing for CKo1 and FPo1

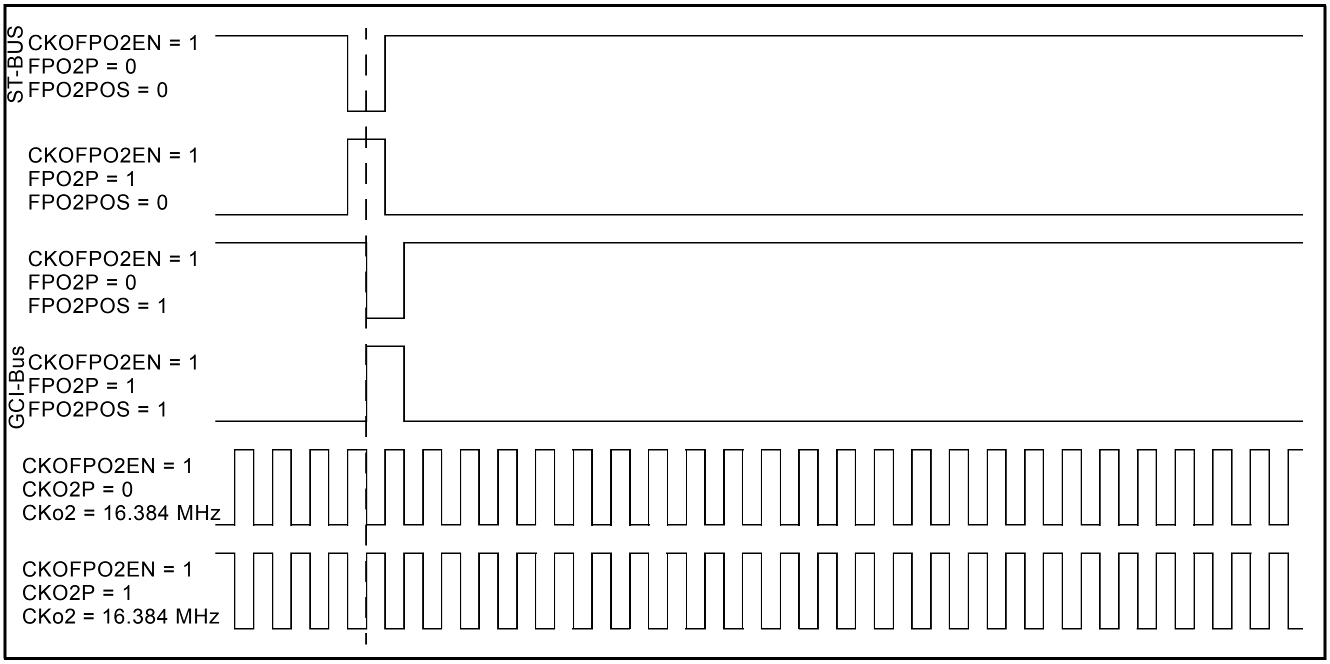
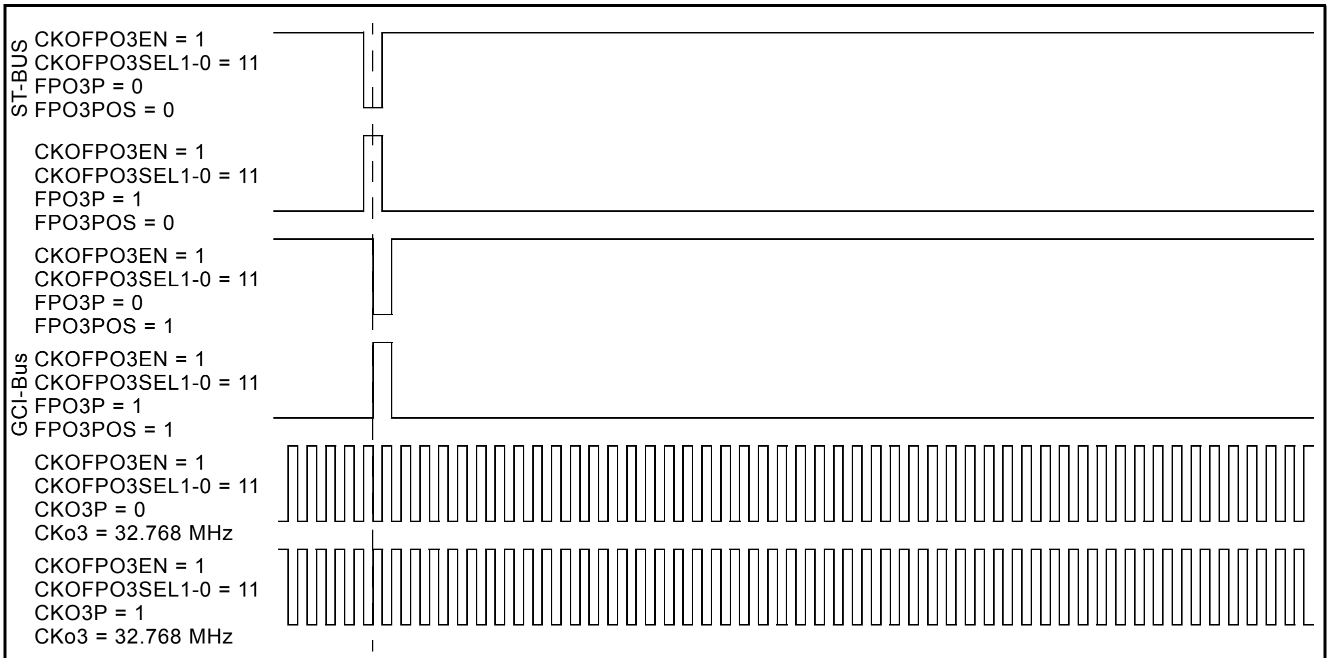
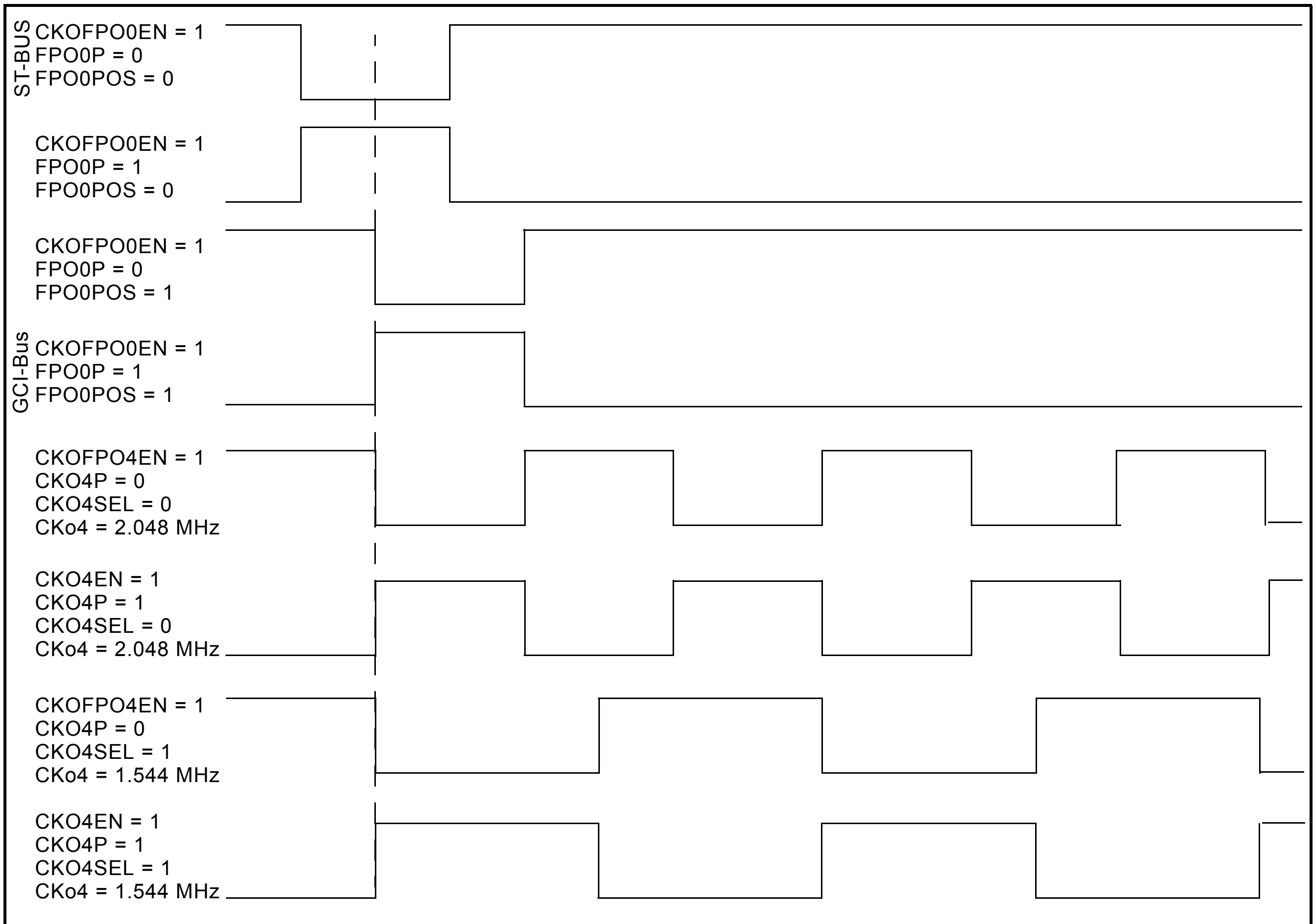


Figure 9 - Output Timing for CKo2 and FPo2



NOTE:
When CKOFPO3SEL1-0 = “00,” the output for FPo3 and CKo3 follow the same as Figure 7: Output Timing for CKo0 and FPo0
When CKOFPO3SEL1-0 = “01,” the output for FPo3 and CKo3 follow the same as Figure 8: Output Timing for CKo1 and FPo1
When CKOFPO3SEL1-0 = “10,” the output for FPo3 and CKo3 follow the same as Figure 9: Output Timing for CKo2 and FPo2

Figure 10 - Output Timing for CKo3 and FPo3 with CKoFPo3SEL1-0=”11”



NOTE:
While there is no frame pulse output directly tied to the CKo4, the output clocks are based on the frame pulse generated by FPo0.

Figure 11 - Output Timing for CKo4

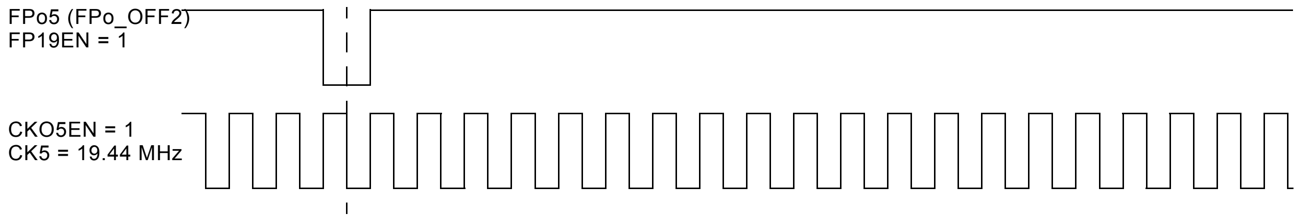


Figure 12 - Output Timing for CKo5 and FPo5 (FPo_OFF2)

7.0 Data Input Delay and Data Output Advancement

Various registers are provided to adjust the input delay and output advancement for each input and output data stream. The input bit delay and output bit advancement can vary from 0 to 7 bits for each individual stream.

If input delay of less than a bit is desired, different sampling points can be used to handle the adjustments. The sampling point can vary from 1/4 to 4/4 with a 1/4-bit increment for all input streams, unless the stream is operating at 16.384 Mbps, in which case the fractional bit delay has a 1/2-bit increment. By default, the sampling point is set to the 3/4-bit location for non-16.384 Mbps data rates and the 1/2-bit location for the 16.384 Mbps data rate.

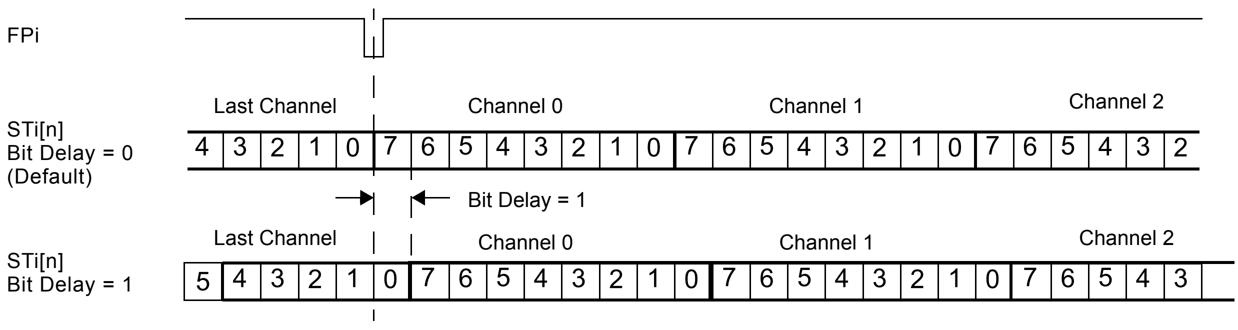
The fractional output bit advancement can vary from 0 to 3/4 bits, again with a 1/4-bit increment unless the output stream is operating at 16.38 Mbps, in which case the output fractional bit advancement has a 1/2-bit increment from 0 to 1/2 bit. By default, there is 0 output bit advancement.

Although input delay or output advancement features are available on streams which are operating in bi-directional mode it is not recommended, as it can easily cause bus contention. If users require this function, special attention must be given to the timing to ensure contention is minimized.

7.1 Input Bit Delay Programming

The input bit delay programming feature provides users with the flexibility of handling different wire delays when designing with source streams for different devices.

By default, all input streams have zero bit delay, such that bit 7 is the first bit that appears after the input frame boundary (assuming ST-BUS formatting). The input delay is enabled by STIN[n]BD2-0 (bits 8 - 6) in the Stream Input Control Register 0 - 31 (SICR0 - 31) as described in Table 61 on page 94. The input bit delay can range from 0 to 7 bits.

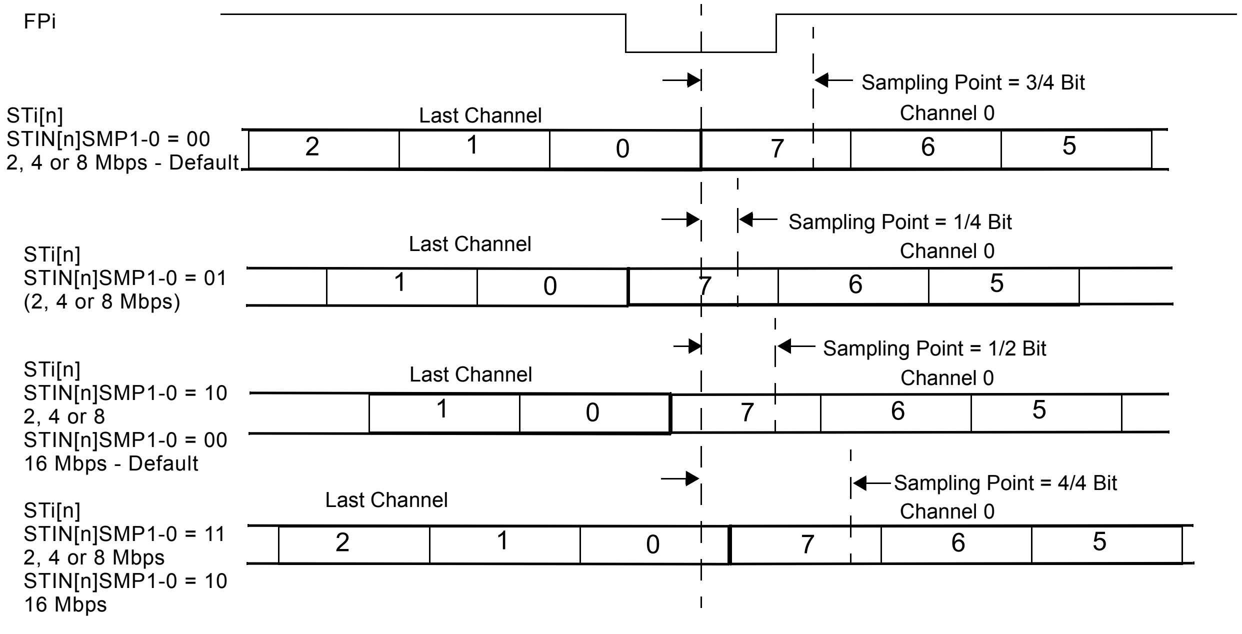


Note: Last Channel = 31, 63, 127 and 255 for 2.048, 4.096, 8.192 and 16.384 Mbps modes respectively.

Figure 13 - Input Bit Delay Timing Diagram (ST-BUS)

7.2 Input Bit Sampling Point Programming

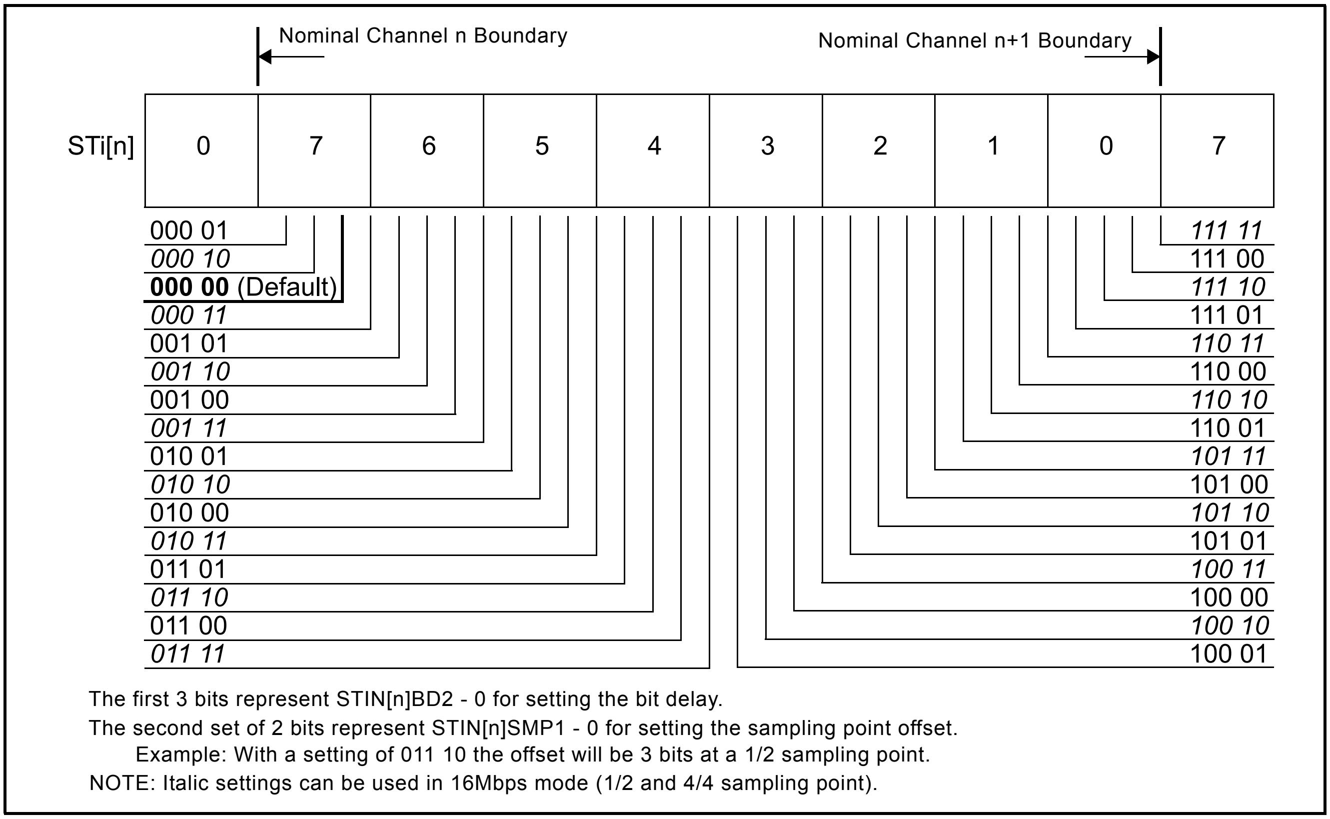
In addition to the input bit delay feature, the ZL50021 allows users to change the sampling point of the input bit by programming STIN[n]SMP 1-0 (bits 5 - 4) in the Stream Input Control Register 0 - 31 (SICR0 - 31). For input streams operating at any rate except 16.384 Mbps, the default sampling point is at 3/4 bit and users can change the sampling point to 1/4, 1/2, 3/4 or 4/4 bit position. When the stream is operating at 16.384 Mbps, the default sampling point is 1/2 bit and can be adjusted to a 4/4 bit position.



Note: Last Channel = 31, 63, 127 and 255 for 2.048, 4.096, 8.192 and 16.384 Mbps mode respectively.

Figure 14 - Input Bit Sampling Point Programming

The input delay is controlled by STIN[n]BD2-0 (bits 8 - 6) to control the bit shift and STIN[n]SMP1 - 0 (bits 5 - 4) to control the sampling point in the Stream Input Control Register 0 - 31 (SICR0 - 31).



The first 3 bits represent STIN[n]BD2 - 0 for setting the bit delay.
The second set of 2 bits represent STIN[n]SMP1 - 0 for setting the sampling point offset.
Example: With a setting of 011 10 the offset will be 3 bits at a 1/2 sampling point.
NOTE: Italic settings can be used in 16Mbps mode (1/2 and 4/4 sampling point).

Figure 15 - Input Bit Delay and Factional Sampling Point

7.3 Output Advancement Programming

This feature is used to advance the output data of individual output streams with respect to the output frame boundary. Each output stream has its own bit advancement value which can be programmed in the Stream Output Control Register 0 - 31 (SOCR0 - 31).

By default, all output streams have zero bit advancement such that bit 7 is the first bit that appears after the output frame boundary (assuming ST-BUS formatting). The output advancement is enabled by STO[n]AD 2 - 0 (bits 6 - 4) of the Stream Output Control Register 0 - 31 (SOCR0 - 31) as described in Table 63 on page 98. The output bit advancement can vary from 0 to 7 bits.

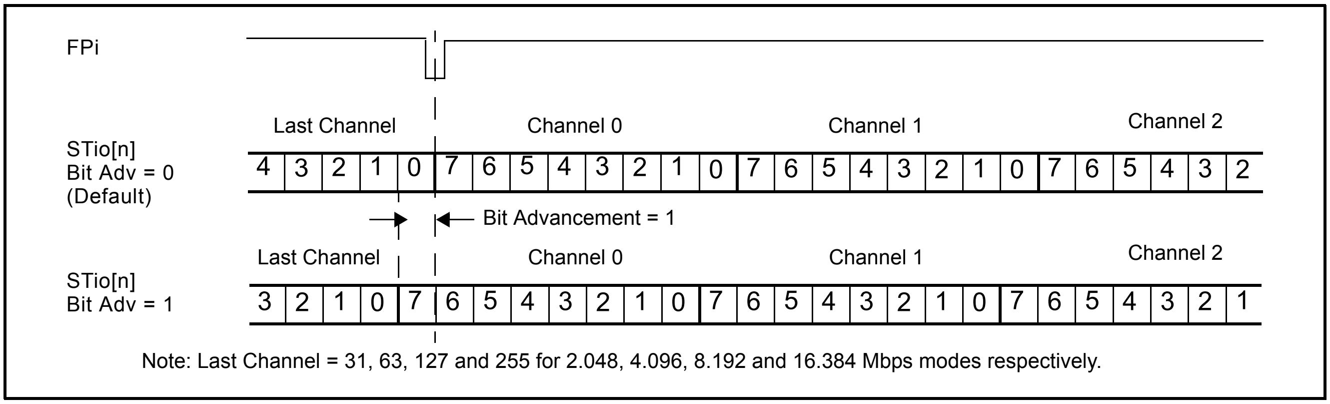
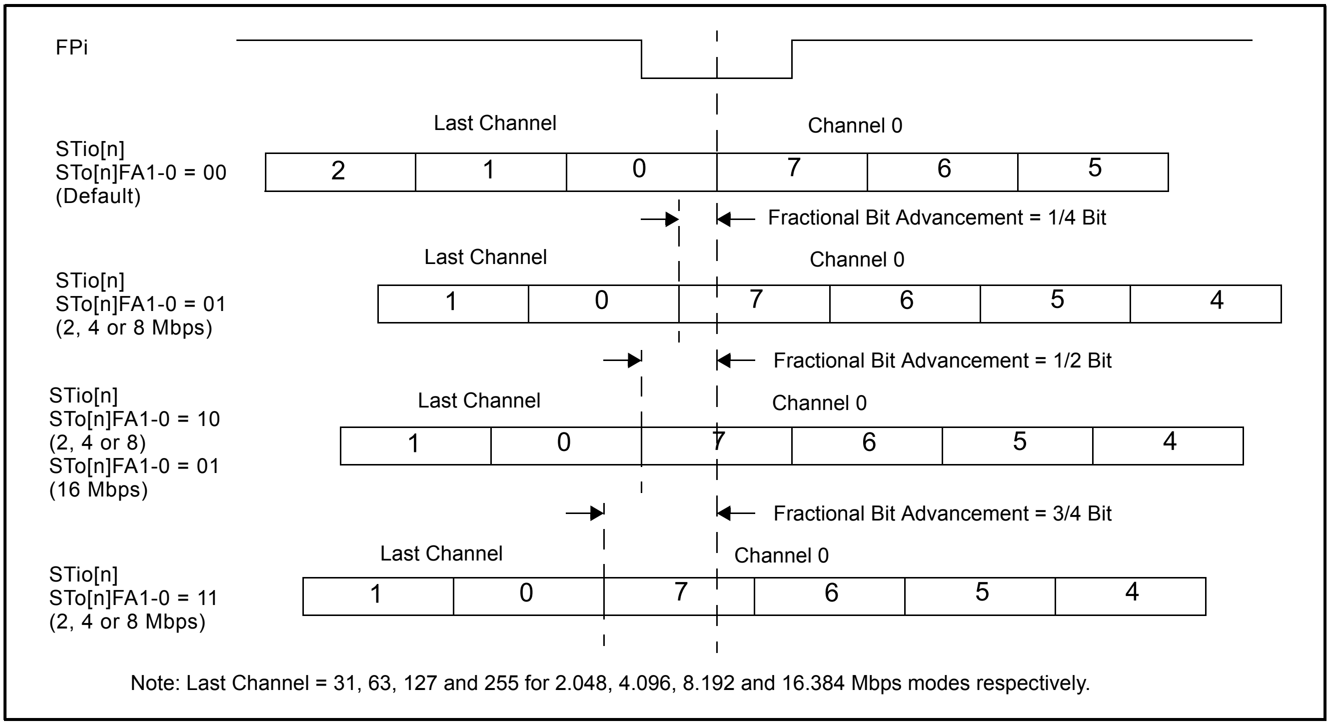


Figure 16 - Output Bit Advancement Timing Diagram (ST-BUS)

7.4 Fractional Output Bit Advancement Programming

In addition to the output bit advancement, the device has a fractional output bit advancement feature that offers better resolution. The fractional output bit advancement is useful in compensating for varying parasitic load on the serial data output pins.

By default all of the streams have zero fractional bit advancement such that bit 7 is the first bit that appears after the output frame boundary. The fractional output bit advancement is enabled by STO[n]FA 1 - 0 (bits 8 - 7) in the Stream Output Control Register 0 - 31 (SOCR0 - 31). For all streams running at any data rate except 16.384 Mbps the fractional bit advancement can vary from 0, 1/4, 1/2 to 3/4 bits. For streams operating at 16.384 Mbps, the fractional bit advancement can be set to either 0 or 1/2 bit.

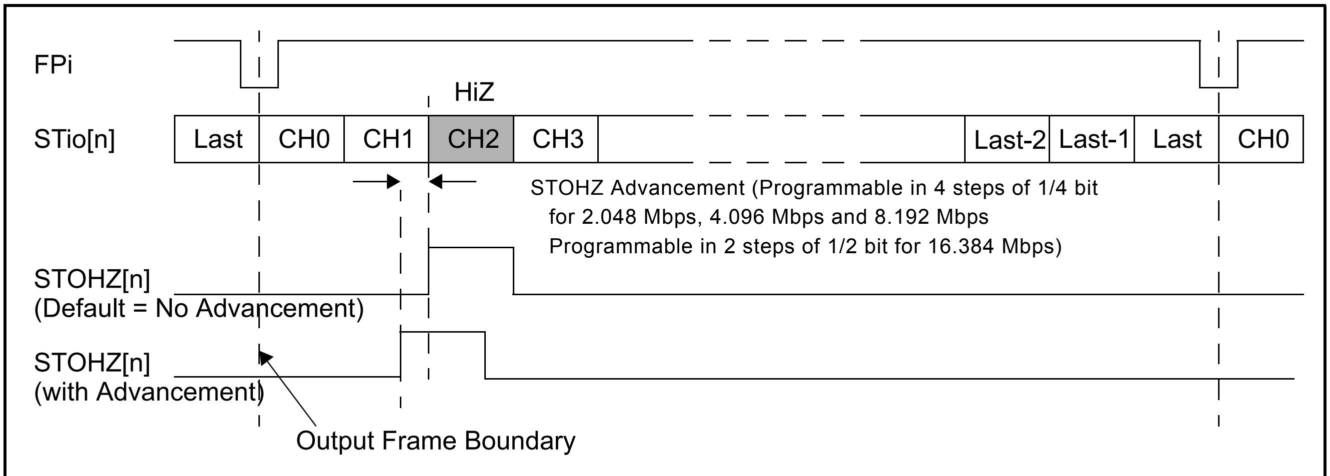


Note: Last Channel = 31, 63, 127 and 255 for 2.048, 4.096, 8.192 and 16.384 Mbps modes respectively.

Figure 17 - Output Fractional Bit Advancement Timing Diagram (ST-BUS)

7.5 External High Impedance Control Advancement

The external high impedance signals can be programmed to better match the timing required by the external buffers. By default, the output timing of the STOHZ signals follows the programmed channel delay and bit offset of their corresponding ST-BUS/GCI-Bus output streams. In addition, for all high impedance streams operating at any data rate except 16.384 Mbps, the user can advance the STOHZ signals a further 0, 1/4, 1/2, 3/4 or 4/4 bits by programming STOHZ[n]A 2 - 0 (bit 11 - 9) in the Stream Output Control Register. When the stream is operating at 16.384 Mbps, the additional STOHZ advancement can be set to 0, 1/2 or 4/4 bits by programming the same register.



NOTE: n = 0 to 15

NOTE: Last = Last Channel of 31, 63, 127 and 255 for 2.048 Mbps, 4.096 Mbps. 8.192 Mbps and 16.384 Mbps modes respectively.

Figure 18 - Channel Switching External High Impedance Control Timing

8.0 Data Delay Through the Switching Paths

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications, select constant delay to maintain the frame integrity of the information through the switch. The delay through the device varies according to the type of throughput delay selected by the $V/\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0.

8.1 Variable Delay Mode

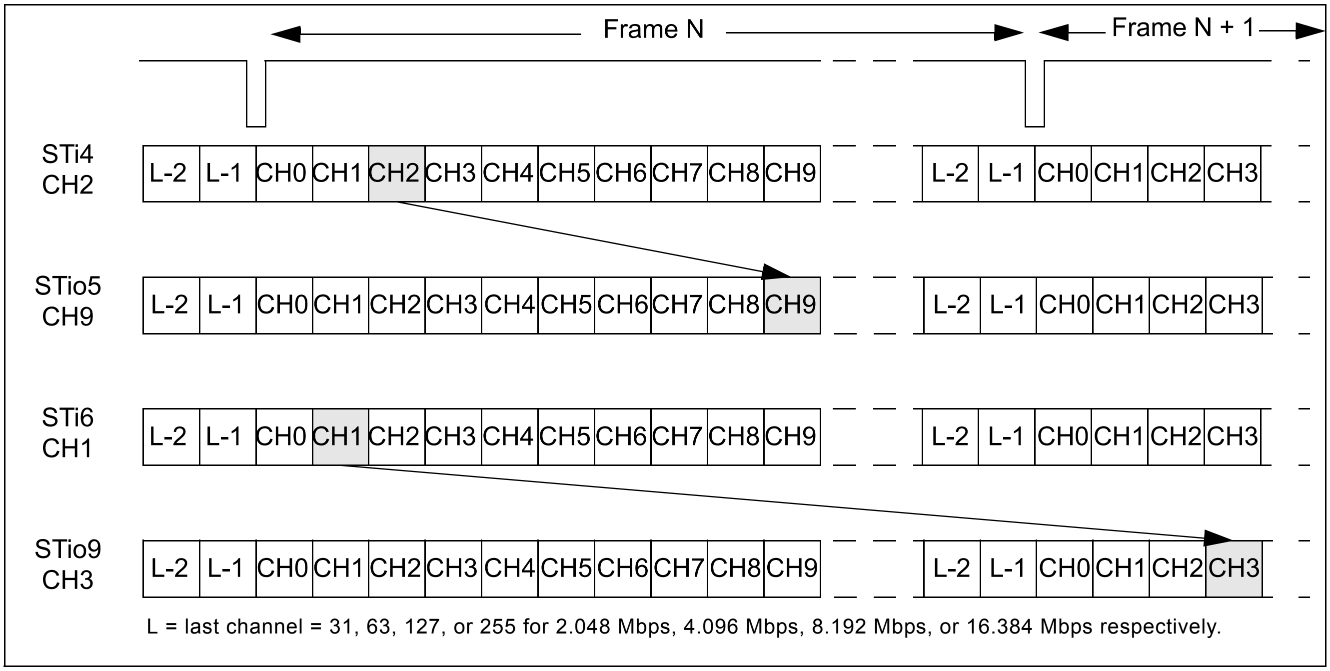
Variable delay mode causes the output channel to be transmitted as soon as possible. This is a useful mode for voice applications where the minimum throughput delay is more important than frame integrity. The delay through the switch can vary from 7 channels to 1 frame + 7 channels. To set the device into variable delay mode, VAREN (bit 4) in the Control Register (CR) must be set before $V/\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0. If the VAREN bit is not set and the device is programmed for variable delay mode, the information read on the output stream will not be valid.

In variable delay mode, the delay depends on the combination of the source and destination channels of the input and output streams.

m = input channel number n = output channel number	n-m <= 0	0 < n-m < 7	n-m = 7		n-m > 7
			STio < STi	STio >= STi	
T = Delay between input and output	1 frame - (m-n)	1 frame + (n-m)		n-m	

Table 4 - Delay for Variable Delay Mode

For example, if Stream 4 Channel 2 is switched to Stream 5 Channel 9 with variable delay, the data will be output in the same 125 µs frame. Contrarily, if Stream 6 Channel 1 is switched to Stream 9 Channel 3, the information will appear in the following frame.



L = last channel = 31, 63, 127, or 255 for 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, or 16.384 Mbps respectively.

Figure 19 - Data Throughput Delay for Variable Delay

8.2 Constant Delay Mode

In this mode, frame integrity is maintained in all switching configurations. The delay though the switch is 2 frames - Input Channel + Output Channel. This can result in a minimum of 1 frame + 1 channel delay if the last channel on a stream is switched to the first channel of a stream. The maximum delay is 3 frames - 1 channel. This occurs when the first channel of a stream is switched to the last channel of a stream. The constant delay mode is available for all output channels.

The data throughput delay is expressed as a function of ST-BUS/GCI-Bus frames, input channel number (m) and output channel number (n). The data throughput delay (T) is:

T = 2 frames + (n - m)

The constant delay mode is controlled by $V/\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0. When this bit is set low, the channel is in constant delay mode. If VAREN (bit 4) in the Control Register (CR) is set (to enable variable throughput delay on a chip-wide basis), the device can still be programmed to operate in constant delay mode.

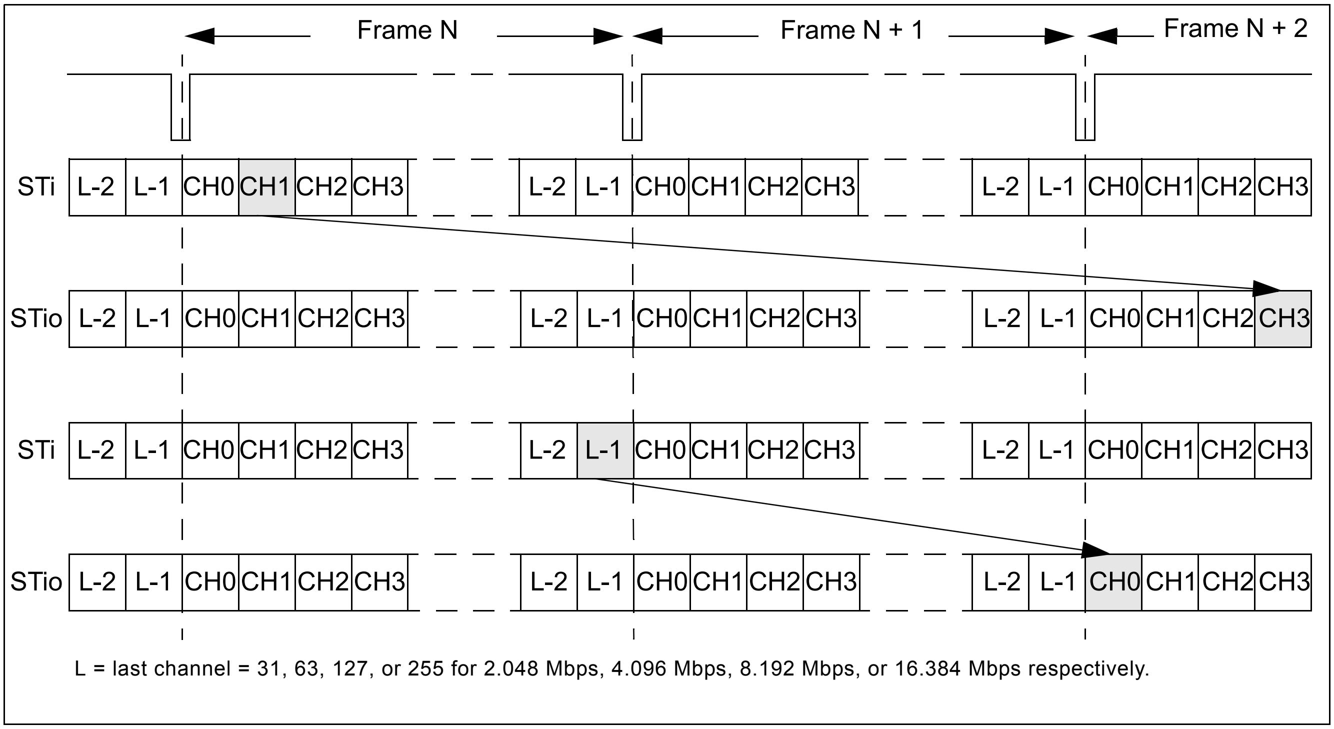


Figure 20 - Data Throughput Delay for Constant Delay

9.0 Connection Memory Description

The connection memory consists of two blocks, Connection Memory Low (CM_L) and Connection Memory High (CM_H). The CM_L is 16 bits wide and is used for channel switching and other special modes. The CM_H is 5 bits wide and is used for the voice coding function. When UAEN (bit 15) of the Connection Memory Low (CM_L) is low, μ-law/A-law conversion will be turned off and the contents of CM_H will be ignored. Each connection memory location of the CM_L or CM_H can be read or written via the 16 bit microprocessor port within one microprocessor access cycle. See Table 68 on page 101 for the address mapping of the connection memory. Any unused bits will be reset to zero on the 16-bit data bus.

For the normal channel switching operation, CMM (bit 0) of the Connection Memory Low (CM_L) is programmed low. SCA7 - 0 (bits 8 - 1) indicate the source (input) channel address and SSA4 - 0 (bits 13 - 9) indicate the source (input) stream address. The 5-bit contents of the CM_H will be ignored during the normal channel switching mode without the μ-law/A-law conversion when UAEN (bit 15) of the Connection Memory Low (CM_L) is set to zero. If μ-law/A-law conversion is required, the CM_H bits must be programmed first to provide the voice/data information, the input coding law and the output coding law before the assertion of UAEN (bit 15) in the Connection Memory Low.

When CMM (bit 0) of the Connection Memory Low (CM_L) is programmed high, the ZL50021 will operate in one of the special modes described in Table 70 on page 103. When the per-channel message mode is enabled, MSG7 - 0 (bit 10 - 3) in the Connection Memory Low (CM_L) will be output via the serial data stream as message output data. When the per-channel message mode is enabled, the μ-law/A-law conversion can also be enabled as required.

10.0 Connection Memory Block Programming

This feature allows for fast initialization of the connection memory after power up.

10.1 Memory Block Programming Procedure

1. Set MBPE (bit 3) in the Control Register (CR) from low to high.
2. Configure BPD2 - 0 (bits 3 - 1) in the Internal Mode Selection (IMS) register to the desired values to be loaded into CM_L.
3. Start the block programming by setting MBPS (bit 0) in the Internal Mode Selection Register (IMS) high. The values stored in BPD2 - 0 will be loaded into bits 2 - 0 of all CM_L positions. The remaining CM_L locations (bits 15 - 3) and the programmable values in the CM_H (bits 4 - 0) will be loaded with zero values.

The following tables show the resulting values that are in the CM_L and CM_H connection memory locations.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	BPD2	BPD1	BPD0

Table 5 - Connection Memory Low After Block Programming

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6 - Connection Memory High After Block Programming

Note: Bits 15 to 5 are reserved in Connection Memory High and should always be 0.

It takes at least two frame periods (250 μs) to complete a block program cycle.

MBPS (bit 0) in the Control Register (CR) will automatically reset to a low position after the block programming process has completed.

MBPE (bit 3) in the Internal Mode Selection (IMS) register must be cleared from high to low to terminate the block programming process. This is not an automatic action taken by the device and must be performed manually.

Note: Once the block program has been initiated, it can be terminated at any time prior to completion by setting MBPS (bit 0) in the Control Register (CR) or MBPE (bit 3) in the Internal Mode Selection (IMS) register to low. If the MBPE bit was used to terminate the block programming, the MBPS bit will have to be set low before enabling other device operations.

11.0 Device Operation in Master Mode and Slave Modes

This device has two main operating modes - Master mode and Slave mode. Each operating mode has different input/output clock and frame pulse setup requirements and usage.

If the device is programmed to work in Master mode, it is expected that the input clock and frame pulse will be supplied from the embedded DPLL, either directly using the internal loopback mode or indirectly through external loopback path. Sources and destinations of the device's serial input and output data, respectively, have to be synchronized with the device's output clock and frame pulse. In Master mode, output clocks and frame pulses are driven by the DPLL and they are always available with any of the specified frequencies.

The device can also operate in two different Slave modes: Divided Slave mode and Multiplied Slave mode. In either Slave modes, output clocks and frame pulses are generated based on CKi and FPi. The difference is that, in Divided Slave mode, the output clocks and frame pulses are directly divided from CKi/FPi, while in Multiplied Slave mode, the output clocks and frame pulses are generated from an internal high-speed clock synchronized to CKi and FPi. Therefore, in Divided Slave mode, the output clock rates cannot exceed the CKi rate (the output data rates are also limited as per Table 1), but in Multiplied Slave mode, all specified output clock rates and data rates are available on CKo0-3 and STio0-31. The input data rate cannot exceed the CKi rate in either Slave modes, because input data are always sampled directly by CKi.

By default, CKo4, CKo5 and FPo5 are not available in Slave mode, as the embedded DPLL is disabled. However, the DPLL can be activated even in Slave mode by programming the SLV DPLLEN bit in the Control Register. When the DPLL is enabled in Slave mode, CKo4, CKo5 and FPo5 are generated from the DPLL synchronized to one of the REF0-3 inputs, while the other clocks, frame pulses, and input/output data are synchronized to CKi/FPi. It basically creates two separate timing domains - one for the DPLL, and one for data switch logic. The two can be totally asynchronous to each other. In this case the DPLL will be fully functional, including its capability of reference monitoring.

Note that an external oscillator is required whenever the DPLL is used.

Table 7, “ZL50021 Operating Modes” on page 38 summarizes the different modes of operation available within the ZL50021. Each Major mode has various associated Minor modes that are determined by setting the relevant Input Control pins and Control Register bits (Table 18, “Control Register (CR) Bits” on page 56) indicated in the table.

Device		**Input Pins**				**CR Register**			**Output Clock Pins**				**Data Pins**	
Operating Mode		**Control**		**Signal**		**Bits**			**Reference Lock**		**Enabled**		**Clock Source**	
Major	Minor	OSC_EN	MODE_4M [1:0]	OSCi	CKi	OPM [1:0]	SLV_DPLLEN	CKi_LP	CKo0-3	CKo4-5	CKo0-3	CKo4-5	STi	STo
Master	CKi	1	00	20 MHz	4/8/16 M	00	X	0	Freerun, Holdover or REF0-3		Yes	Yes	CKi*	Cko2 (DPLL)
	Loopback				X			1					Cko2	
Divided Slave	4 M	1	11	20 MHz	4 M	01	1	X	CKi	REF0-3		Yes	CKi	CKo0-3 (CKi)
	8/16 M		00		8/16 M									
	4 M	0	11	X	4 M	X0	0			X		No		
	8/16 M		00		8/16 M									
Multiplied Slave	4 M	1	11	20 MHz	4 M	11	1		CKi MULT	REF0-3		Yes		CKo0-3 (CKi MULT)
	8/16 M		00		8/16 M									
	4 M	0	11	X	4 M	X1	0			X		No		
	8/16 M		00		8/16 M									

Legend:

X - Don’t care or not applicable.

Reference Lock - Refers to what signal the output pins are locked to:
REF0-3 = Normal Mode
Cki = Bypass. Cki is passed directly through to CKo0-3.
Cki MULT = Cki is passed through clock multiplier to CKo0-3.
* CKi must be phase aligned (edge synchronous) to CKo0-3.
Clock Source - Refers to which clock samples STi and which clock outputs STo; STi applies when STi or STio is input; STo applies when STio is output.

Table 7 - ZL50021 Operating Modes

11.1 Master Mode Operation

When the device is in Master mode, the DPLL is phase-locked to the one of four DPLL reference signals, REF0 to REF3, which are sourced by an external 8 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz signal. The on-chip DPLL also offers reference switching and monitoring, jitter attenuation, freerun and holdover functions. In this mode, STio0 - 31 are driven by a clock generated by the DPLL, which also provides all the output clocks (CKo0 - 5) and frame pulses (FPo0 - 3 and FPo_OFF0 - 2). One of the output clocks and frame pulses should be looped back to CKi/FPi as reference for the input data, either by internal loopback (by setting the CKi_LP bit high in the Control Register) or through some external loopback paths. If external loopback is used, it is recommended that CKo2 (16.384MHz) and FPo2 (61ns pulse) are used so that all input data rates are available.

11.2 Divided Slave Mode Operation

When the device is in Divided Slave mode, STio0 - 31 are driven by CKi. In this mode, the output streams and clocks have the same jitter characteristics as the input clock (CKi), but the input and output data rates cannot exceed the limit defined by CKi (as per Table 1). For example, if CKi is 4.096 MHz, the input and output data rate cannot be higher than 2.048 Mbps, and the generated output clock rates cannot exceed 4.096 MHz. If the DPLL is not enabled, an external oscillator is optional in Divided Slave mode.

11.3 Multiplied Slave Mode Operation

When the device is in Multiplied Slave mode, device hardware is used to multiply CKi internally. STio0 - 31 are driven by this internally generated clock. In this mode, the output clocks and data can run at any of the specified rates, but they may have different jitter characteristics from the input clock (CKi). The input data rates are still limited by the CKi rate (as per Table 1), as input data are always sampled directly by CKi. If the DPLL is not enabled, an external oscillator is not required in Multiplied Slave mode.

12.0 Overall Operation of the DPLL

The DPLL accepts four input references and delivers six output clocks and five output frame pulses. The DPLL meets or exceeds all of the requirements of the Telcordia GR-1244-CORE standard for a Stratum 3 compliant PLL. This includes the freerun, reference switching and monitoring, jitter/wander attenuation and holdover functions. The intrinsic output jitter of the DPLL does not exceed 1 ns (except for the 1.544 MHz output).

The input locking range of the DPLL is programmable, such that it can be larger than the strict Stratum 3 requirements.

The DPLL is able to lock to an input reference presented on the REF0 - 3 inputs. It is possible to force the DPLL module to lock to a selected reference, to prefer one reference, to enter holdover mode or to freerun.

While in freerun mode, the DPLL is able to work in software mode which allows the user to program an output frequency offset value through the microport of the device. Depending on the selected software mode, the DPLL outputs can:

a. gradually meet the given frequency offset (following pre-programmed phase alignment speed (phase slope) and internal filter response), or

b. immediately, upon finishing the microport write, reach the given frequency offset, allowing an external filter to be used.

12.1 DPLL Timing Modes

There are four timing modes for the DPLL: normal, holdover, automatic and freerun modes. In addition to these four functional timing modes, the DPLL can also be programmed to internal reset mode.

12.1.1 Normal Mode

In normal mode, the DPLL generates clocks and frame pulses that are phase locked to the active input reference. Jitter on the input clock is attenuated by the DPLL.

12.1.2 Holdover Mode

In holdover mode, the DPLL no longer synchronizes the output clock to any input reference. It maintains the frequency that it was at prior to entering holdover mode. The holdover mode typically happens when the input clock becomes unreliable or is lost altogether. It takes some time for the system to realize that the input clock is unreliable. Meanwhile, the DPLL tracks an unreliable clock. Therefore the DPLL could hold to an invalid frequency when it enters holdover mode. In order to prevent this situation, the DPLL stores the current frequency at regular intervals in holdover memory so that it can restore the frequency of the input clock just after the input clock became unreliable.

The accuracy of the output clock with respect to the last valid input clock is subject to certain standards referred to as Stratum levels where each level requires a certain accuracy. The standards ANSI T1.101 and Telcordia GR-1244-CORE specify the Stratum level requirements. Where ANSI just gives one total number, Telcordia splits it into three components, thereby creating a more stringent requirement than ANSI.

In order to meet Stratum 3, the holdover accuracy of the DPLL is better than 0.05 ppm. Note that in order for the system to meet Stratum 3, the system clock provided by the external oscillator must meet the requirements for the temperature dependence and drift. If Stratum 3 accuracy is not required, a less stable and cheaper system clock can be used instead.

12.1.3 Automatic Mode

In this mode, the state machine controls the DPLL based on the settings in the registers and the quality of the reference input clocks. The DPLL is internally either in normal or holdover mode. In the following two sections, the reference selection and state machine operation in automatic mode will be explained in more details.

12.1.3.1 Automatic Reference Switching Without Preferences

When the DPLL is programmed to operate in Automatic mode without Preference (RCCR Register, PMS2-0 bits = 000), all references, REF0-3, will have equal importance. A circulating *Round Robin* selection sequence determines the reference to be used as shown in Figure 21. The state machine basically searches for valid reference in a circular order of REF0 -> REF1 -> REF2 -> REF3 -> REF0, etc.

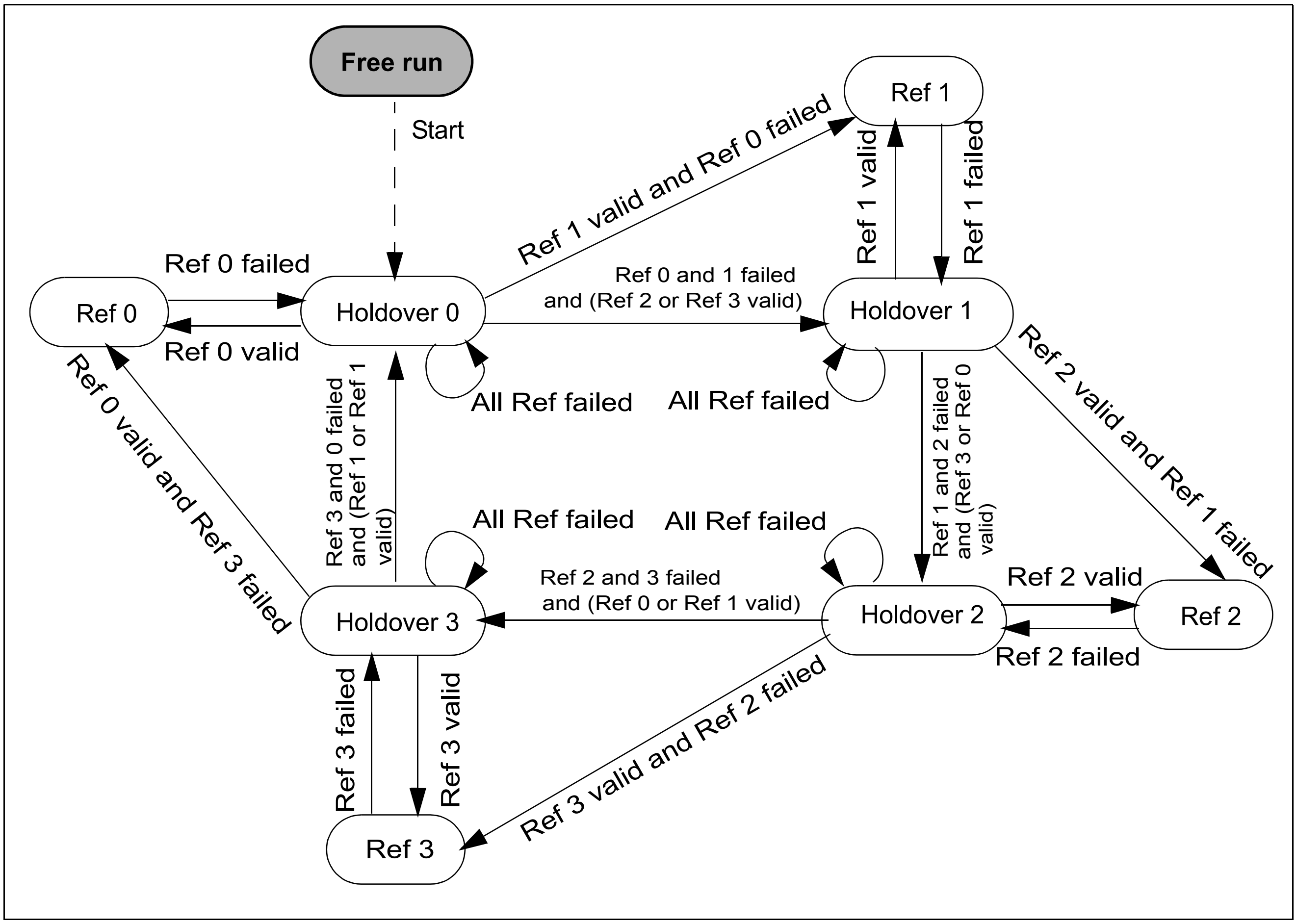


Figure 21 - Automatic Reference Switching State Diagram with No Preferred Reference

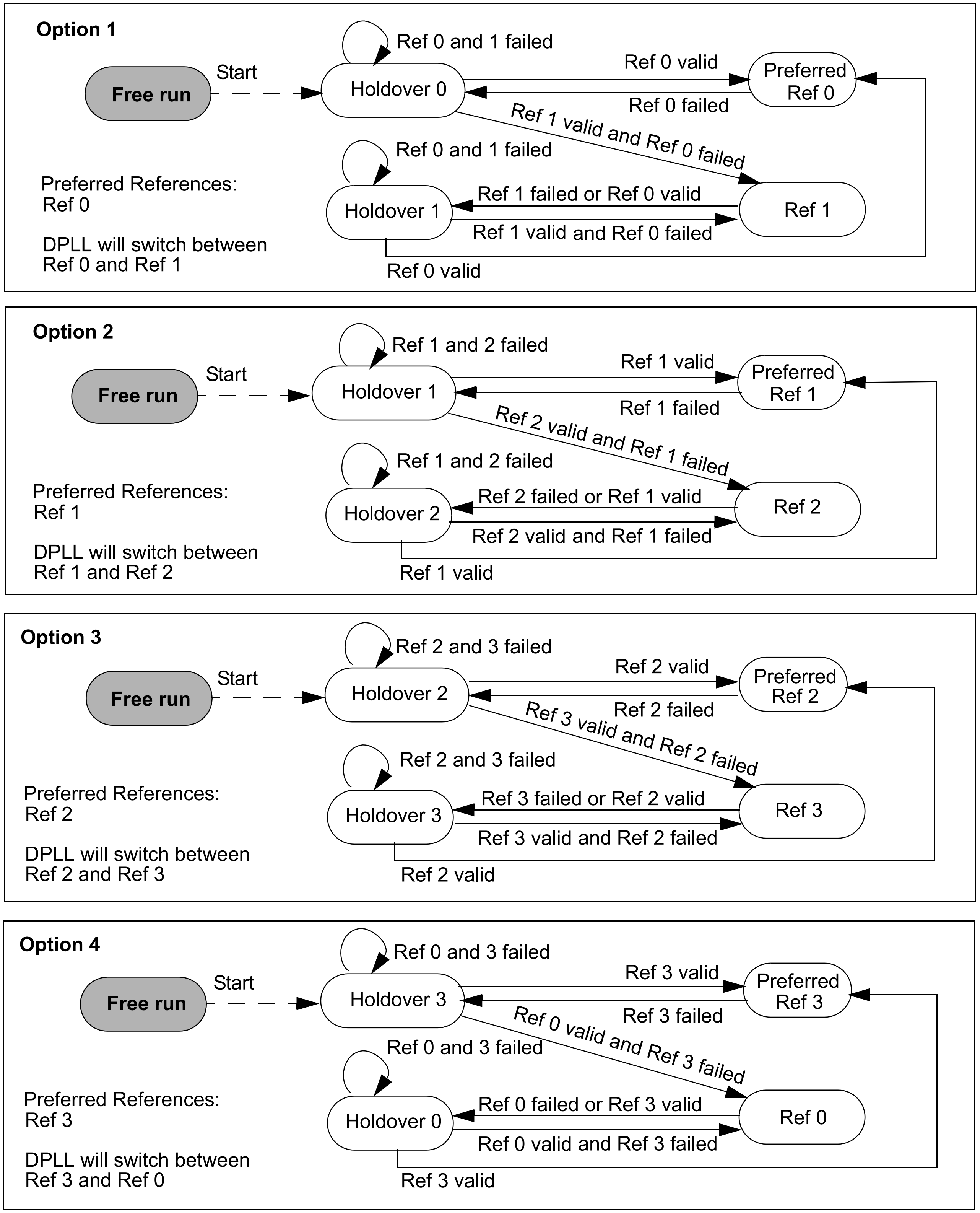
12.1.3.2 Automatic Reference Switching With Preference

If a particular reference needs to have higher priority than the others, the device can be programmed in Automatic mode with a preferred reference (RCCR Register, PMS2-0 bits = 001). When a preferred reference is selected, the device can only switch automatically between two references, as shown in Table 8. The preferred reference will be used as the primary reference and, by default, only its next consecutive reference will be used as the secondary reference. No more than two references can be used in Automatic mode when a preferred reference is selected.

	Primary Reference (Preferred)	Secondary Reference
Option 1	Ref 0	Ref 1
Option 2	Ref 1	Ref 2
Option 3	Ref 2	Ref 3
Option 4	Ref 3	Ref 0

Table 8 - Preferred Reference Selection Options

Figure 22 shows the state diagram for the four valid options of automatic reference switching with a preferred reference.



Note: other combinations not shown here are invalid settings and should not be used

Figure 22 - Automatic Reference Switching State Diagrams with Preferred Reference

With a preferred reference, if more than two references are required, or the two references are not in consecutive order, or the roles of the two references need to be interchanged, then external software is required to manually control the reference switching of the DPLL (by monitoring the reference failure status and reprogramming the device accordingly).

12.1.4 Freerun Mode

In freerun mode, the DPLL generates a fixed output frequency based on the crystal oscillator and a programmed centre frequency. To meet Stratum 3, the accuracy of the circuitry for the freerunning output clock must be 4.6 ppm or better. The circuit’s freerun accuracy is better than 0.003 ppm.

In freerun mode, the DPLL does not lock to any reference. It is important that the device is not simultaneously in freerun mode (see the RCCR Register) and fast lock mode (see the BWCR Register). Otherwise, the output frame pulse may not be generated correctly.

12.1.4.1 Software Controlled Mode

When the DPLL is in the freerun mode, it can be put into software controlled mode by enabling the SWE (bit 3) in the DPLL Control Register (DPLLCR). The Software Delta Frequency Register (SWDFR) contains the frequency offset to which the DPLL outputs will move. If SWF (bit 4) in the DPLL Control Register (DPLLCR) is low, the DPLL outputs will gradually move to the given frequency offset, with the speed defined by the DPLL internal filter and phase alignment speed (phase slope) limiter. If SWF (bit 4) is high, the DPLL outputs will reach the Software Delta Frequency Register (SWDFR) frequency offset immediately after it is written, allowing an external software-based filter and phase alignment speed (phase slope) limiter to be used. When SWE (bit 3) is low or the DPLL is not in the freerun mode, the value of Software Delta Frequency Register (SWDFR) will be ignored. For detailed description of the DPLL Control Register (DPLLCR) bits and the Software Delta Frequency Register (SWDFR) bits see Table 29 on page 66, and Table 33 on page 71, respectively.

12.1.5 DPLL Internal Reset Mode

DPLL_IRM (bit 0) in the DPLL Control Register (DPLLCR) enables the internal reset mode. In the internal reset mode, the DPLL module is disabled to save power. The circuit will be reset continuously and no output clocks will be generated. When the internal DPLL module is in the internal reset mode, all registers remain accessible. Note that applying the DPLL reset does not reset the DPLL registers: they preserve the values that they had prior to entering reset.

13.0 DPLL Frequency Behaviour

13.1 Input Frequencies

The DPLL is capable of synchronizing to one of the following input frequencies:

8 kHz
1.544 MHz (DS1)
2.048 MHz (E1)
4.096 MHz
8.192 MHz
16.384 MHz
19.44 MHz

Table 9 - DPLL Input Reference Frequencies

13.2 Input Frequencies Selection

The input frequencies of REF 0 - 3 can be automatically detected or programmed independently by the Reference Frequency Register (RFR) if RFRE (bit 1) in the DPLL Control Register (DPLLCR) is set. The detected frequency of the selected reference is indicated in the Reference Change Status Register (RCSR). In addition, the detected frequencies of all four references are indicated in the Reference Frequency Status Register (RFSR). See Table 29 on page 66, Table 30 on page 68, Table 41 on page 78 and Table 59 on page 92 for the detailed bit description of the DPLL Control Register (DPLLCR), Reference Frequency Register (RFR), Reference Change Status Register (RCSR) and Reference Frequency Status Register (RFSR), respectively.

13.3 Output Frequencies

The DPLL generates a limited number of output signals. All signals are synchronous to each other and in the normal operating mode, are locked to the selected input reference. The DPLL provides outputs with the following frequencies:

CKo0	4.096 MHz
CKo1	8.192 MHz
CKo2	16.384 MHz
CKo3	4.096 MHz, 8.192 MHz, 16.384 MHz or 32.768 MHz
CKo4	1.544 MHz or 2.048 MHz
CKo5	19.44 MHz
FPo0	8 kHz (244 ns wide pulse)
FPo1	8 kHz (122 ns wide pulse)
FPo2	8 kHz (61 ns wide pulse)
FPo3	8 kHz (122 ns, 61 ns or 30 ns wide pulse)
FPo5	8 kHz (51 ns wide pulse)

Table 10 - Generated Output Frequencies

13.4 Pull-In/Hold-In Range (also called Locking Range)

The widest tolerance required for any of the given input clock frequencies is ±130 ppm for the T1 clock (1.544 MHz). If the system clock (crystal/oscillator) accuracy is ±30 ppm, it requires a minimum pull-in range of ±160 ppm. Users who do not require the ±30 ppm freerun accuracy of the DPLL can use a ±100 ppm system clock. Therefore the pull-in range is a minimal ±230 ppm. The pull-in range is programmable through the Frequency Locking Range Register (FLRR) as described in Table 35 on page 72. Since the width of the register is 14 bits, the maximum programmable pull-in range can be as high as ±372 ppm. The minimum pull-in/hold-in range required for Stratum 3 clocks is ±4.6 ppm. The default pull-in range of this device is ±20 ppm.

14.0 Jitter Performance

14.1 Input Clock Cycle to Cycle Timing Variation Tolerance

The ZL50021 has an exceptional cycle to cycle timing variation tolerance of 20 ns. This allows the ZL50021 to synchronize off a low cost DPLL when it is in either Divided Slave mode or Multiplied Slave mode.

14.2 Input Jitter Acceptance

The input jitter acceptance is specified in standards as the minimum amount of jitter of a certain frequency on the input clock that the DPLL must accept without making cycle slips or losing lock. The lower the jitter frequency, the larger the jitter acceptance. For jitter frequencies below a tenth of the cut-off frequency of the DPLL's jitter transfer function, it safely can be said that any provided input jitter will be followed by the DPLL. The maximum value of jitter tolerance for the DPLL is ±1023 UI_{p-p}.

14.3 Jitter Transfer Function

The corner frequency (-3 dB) of the DPLL is programmable through LPF (bits 3 - 0) in the Bandwidth Control Register (BWCR) from 0.475 Hz to 15.5 kHz, in 16 steps. Stratum 3 requires a corner frequency of maximally 3 Hz. The default corner frequency is 1.9 Hz.

15.0 DPLL Specific Functions and Requirements

15.1 Lock Detector

To determine if the DPLL is locked to the input clock, a lock detector monitors the phase value output of the phase detector, which represents the difference between input reference and output feedback clock. If the phase value is below a certain threshold for a certain interval, the DPLL is pronounced locked to the input clock. The monitoring is done in intervals of 4 ms. The lock detector threshold and the interval are programmable by the user through the Lock Detector Threshold Register (LDTR) and the Lock Detector Interval Register (LDIR) respectively. See Table 36 on page 73 and Table 37 on page 73 for the bit descriptions of the Lock Detector Threshold Register (LDTR) and Lock Detector Interval Register (LDIR) registers respectively. The value of the Lock Detector Threshold Register (LDTR) should be programmed with respect to the maximum expected jitter frequency and amplitude on the selected input references.

The lock status can be monitored through the Reference Change Status Register (RCSR). See Table 41 on page 78 for the bit description of the Reference Change Status Register (RCSR).

15.2 Maximum Time Interval Error (MTIE)

Several standards require that the output clock of the DPLL may not move in phase more than a certain amount. In order to meet those standards, a special circuit maintains the phase of the DPLL output clock during reference and mode rearrangements. The total output phase change or Maximum Timing Interval Error (MTIE) during rearrangements is less than 31 ns per rearrangement, exceeding Stratum 3 requirements. After a large number of reference switches, the accumulated phase error can become significant, so it is recommended to use MTIE reset in such situations, to realign outputs to the nearest edge of the selected reference. The MTIE reset can be programmed by setting MTR (bit 7) in the Reference Change Control Register (RCCR), as described in Table 40 on page 76.

15.3 Phase Alignment Speed (Phase Slope)

Besides total phase change, standards also require a certain rate of the phase change of the output clock. The phase alignment speed is programmable by the user through a value in the Slew Rate Limit Register (SRLR) as described in Table 38 on page 74. Stratum 3 requires that the phase alignment speed not exceed 81 ns per 1.326 ms (61ppm). The width of the register and the limiter circuitry, if not bypassed, provide a maximum phase change alignment speed of 186 ppm.

The limiter circuitry can be bypassed by programming BLM (bit 13) in the Bandwidth Control Register (BWCR). Bypassing limiter (combined with choice of other parameters in the BWCR register) can achieve very fast lock of the output clock to the selected input reference. A side effect of the bypassing limiter is manifested through much higher intrinsic jitter. Once the bypassing is stopped, the jitter characteristics are guaranteed. The phase alignment speed default value is 56 ppm.

15.4 Fast Locking Mode

If very fast locking feature (e.g., locking time in order of 1 s) is desirable, the Bandwidth Control Register (BWCR) can be programmed to accommodate the feature for any selected corner frequency. In this mode, the DPLL's phase alignment speed limiter is bypassed. See Table 39, "Bandwidth Control Register (BWCR) Bits" on page 74.

Semi-fast locking mode does not bypass the internal phase alignment speed limiter, thereby maintaining phase alignment speed. This mode can be achieved by programming the SM_FST bit in the DPLL Control Register.

In freerun mode, the DPLL does not lock to any reference. It is important that the device is not simultaneously in freerun mode (see the RCCR Register) and fast lock mode (see the BWCR Register). Otherwise, the output frame pulse may not be generated correctly.

15.5 Reference Monitoring

The quality of the four input reference clocks is continuously monitored by the reference monitors. There are separate reference monitor circuits for the four DPLL references. References are checked for short phase (single period) deviations as well as for frequency (multi-period) deviations with hysteresis.

The Reference Status Register (RSR) reports the status of the reference monitors. The register bits are described in Table 57 on page 89. The Reference Mask Register (RMR) allows users to ignore the monitoring features of the reference monitors. See Table 58 on page 90 for details.

15.6 Single Period Reference Monitoring

Values for short phase deviations (upper and lower limit) are programmable through registers. The unit of the binary values of these numbers is 100 MHz clock period (10ns). Single period deviation limits are more relaxed than multi period limits, and are used for early detection of the reference loss, or huge phase jumps.

Registers containing the lower and upper limits of the acceptance range for the single input reference period measurement are: Reference Lower Limit Registers: R0LLR, R1LLR, R2LLR and R3LLR and the Reference Upper Limit Registers: R0ULR, R1ULR, R2ULR and R3ULR.

The default values for the upper and lower limits are shown in the following table:

Reference Frequency	Comment
8 kHz	10 UIp-p
1.544 MHz	0.3 UIp-p
2.048 MHz	0.2 UIp-p
4.096 MHz	0.2 UIp-p
8.192 MHz	0.2 UIp-p
16.384 MHz	0.2 UIp-p
19.44 MHz	0.2 UIp-p

Table 11 - Values for Single Period Limits

Reference Frequency	Upper Limit (in 10 ns units)	Lower Limit (in 10 ns units)	Comment
8 kHz	‘h2E4A	‘h335C	6.4 us (10 UIp-p of 1.544 MHz)
1.544 MHz	‘h002B	‘h0055	0.3 UIp-p
2.048 MHz	‘h0025	‘h003B	0.2 UIp-p
4.096 MHz	‘h0011	‘h001E	0.2 UIp-p
8.192 MHz	‘h0007	‘h000F	0.2 UIp-p
16.384 MHz	‘h0002	‘h0008	0.2 UIp-p
19.44 MHz	‘h0002	‘h0007	0.2 UIp-p

Table 12 - Default Values for Single Period Limits

15.7 Multiple Period Reference Monitoring

To monitor reference failure based on frequency offset, multi period checking is performed. Reference validation time is prescribed by Telcordia GR-1244-CORE and is between 10 and 30 seconds. To meet the criteria for reference validation time, the time base for multi period monitoring has to be big enough and is programmable. To implement hysteresis, the upper limits are split into near upper and far upper limits and the lower limits are split into near lower and far lower limits. The reference failure is detectable only when the reference passes far limits, but passing is not detected until the reference is within near limits. The zone between near and far limits, called the “grey zone”, is required by standards and prevents unnecessary reference switching when the selected reference is close to the boundary of failure.

The monitor makes a decision about reference validity after two consecutive measurements with respect to its time base. The time base for multi-period monitoring, by default, is 10 seconds. The time base is defined in the number of reference clock cycles and is programmable.

Assuming that the evaluation time is chosen to be the same regardless of reference frequency (10 seconds), the parameters that allow hysteresis functionality also have the same values, regardless of the reference frequency. These parameters (near lower, far lower, near upper and far upper limits) are programmable.

Registers containing the multi period count are: Reference Multi-Period Counter Registers: R0MPCRL, R0MPCRU, R1MPCRL, R1MPCRU, R2MPCRL, R2MPCRU, R3MPCRL and R3MPCRU.

For the measurement length of multiple clock periods, the period count is set by the Reference Multi-Period Count Registers - Lower 16 Bits: R0MPCRL, R1MPCRL, R2MPCRL and R3MPCRL and the Reference Multi-Period Count Registers - Upper 16 Bits: R0MPCRU, R1MPCRU, R2MPCRU, and R3MPCRU.

The near upper measurement limits are set by the Multi-Period Near Upper Limit Registers, MPNULRL and MPNULRU.

The far upper measurement limits are set by the Multi-Period Far Upper Limit Registers, MPFULRL and MPFULRU.

The near lower measurement limits are set by the Multi-Period Near Lower Limit Registers, MPNLLRL and MPNLLRU.

The far lower measurement limits are set by the Multi-Period Far Lower Limit Registers, MPFLLRL and MPFLLRU.

The registers’ default values upon the device reset comply to Stratum 3 when reference frequencies are 8 kHz. If MRLE (bit 2) of the DPLL Control Register (DPLLCR) is not set, all above mentioned registers for limits and counter values will be ignored and the Stratum 3 default values will be used. The values that comply to Stratum 3 for each detected input reference frequency are used. In order to use programmed values for the monitor registers, MRLE (bit 2) has to be set, in the eventuality that values other than Stratum 3 compliant values are desired.

	Stratum 3 Default Values (in 10 ns units)
Far Upper Limit	-11.287 ppm ’h3B9A9DE8
Near Upper Limit	-9.913 ppm ’h3B9AA346
Nominal Value	0 ppm ’h3B9AC9FF
Near Lower Limit	9.913ppm ’h3B9AF0B8
Far Lower Limit	11.287 ppm ‘h3B9AF616

Table 13 - Multi-period Hysteresis Limits

16.0 Microprocessor Port

The device provides access to the internal registers, connection memories and data memories via the microprocessor port. The microprocessor port is capable of supporting both Motorola and Intel non-multiplexed microprocessors. The microprocessor port consists of a 16-bit parallel data bus (D15 - 0), 14 bit address bus (A13 - 0) and six control signals (MOT_$\overline{\text{INTEL}}$, $\overline{\text{CS}}$, $\overline{\text{DS}}$_$\overline{\text{RD}}$, R/$\overline{\text{W}}$_$\overline{\text{WR}}$, $\overline{\text{IRQ}}$ and $\overline{\text{DTA}}$_RDY).

The data memory can only be read from the microprocessor port. For a data memory read operation, D7 - 0 will be used and D15 - 8 will output zeros.

For a CM_L read or write operation, all bits (D15 - 0) of the data bus will be used. For a CM_H write operation, D4 - 0 of the data bus must be configured and D15 - 5 are ignored. D15 - 5 must be driven either high or low. For a CM_H read operation, D4 - 0 will be used and D15 - 5 will output zeros.

Refer to Figure 26 on page 109, Figure 27 on page 110, Figure 28 on page 111 and Figure 29 on page 112 for the microprocessor timing.

17.0 Device Reset and Initialization

The $\overline{\text{RESET}}$ pin is used to reset the ZL50021. When this pin is low, the following functions are performed:

- synchronously puts the microprocessor port in a reset state
- tristates the STio0 - 31 outputs
- drives the STOHZ0 - 15 outputs to high
- preloads all internal registers with their default values (refer to the individual registers for default values)
- clears all internal counters

17.1 Power-up Sequence

The recommended power-up sequence is for the V_{DD_IO} supply (normally +3.3 V) to be established before the power-up of the V_{DD_CORE} supply (normally +1.8 V). The V_{DD_CORE} supply may be powered up at the same time as V_{DD_IO}, but should not “lead” the V_{DD_IO} supply by more than 0.3 V.

17.2 Device Initialization on Reset

Upon power up, the should be initialized as follows:

- Set the ODE pin to low to disable the STio0 - 31 outputs and to drive STOHZ0 - 15 to high
- Set the $\overline{\text{TRST}}$ pin to low to disable the JTAG TAP controller
- Reset the device by pulsing the $\overline{\text{RESET}}$ pin to zero for longer than 1 μs
- After releasing the $\overline{\text{RESET}}$ pin from low to high, wait for a certain period of time (see Note below) for the device to stabilize from the power down state before the first microprocessor port access can occur
- Program CKIN1 - 0 (bit 6 -5) in the Control Register (CR) to define the frequency of the CKi and FPi inputs
- Wait at least 500 μs prior to the next microport access (see Note below)
- Use the block programming mode to initialize the connection memory
- Release the ODE pin from low to high after the connection memory is programmed

NOTE: If an external oscillator is used, the waiting time is 500 μs. Without the external oscillator, if CKi is 16.384 MHz, the waiting time is 500 μs; if CKi is 8.192 MHz, the waiting time is 1ms; if CKi is 4.096 MHz, the waiting time is 2 ms.

17.3 Software Reset

In addition to the hardware reset from the $\overline{\text{RESET}}$ pin, the device can also be reset by using software reset. There are two software reset bits in the Software Reset Register (SRR). SRSTDPLL (bit 0) is used to reset the DPLL while SRSTSW (bit 1) resets the rest of the switch.

18.0 Pseudorandom Bit Generation and Error Detection

The ZL50021 has one Bit Error Rate (BER) transmitter and one BER receiver for each pair of input and output streams, resulting in 32 transmitters connected to the output streams and 32 receivers associated with the input streams. Each transmitter can generate a BER sequence with a pattern of 2^{15}-1 pseudorandom code (ITU O.151). Each transmitter can start at any location on the stream and will last for a minimum of 1 channel to a maximum of 1 frame time (125 μs). The BER receivers and transmitters are enabled by programming the RBEREN (bit 5) and TBEREN (bit 4) in the IMS register. In order to save power, the 32 transmitters and/or receivers can be disabled. (This is the default state.)

Multiple connection memory locations can be programmed for BER tests such that the BER patterns can be transmitted for multiple consecutive output channels. If consecutive input channels are not selected, the BER receiver will not compare the bit patterns correctly. The number of output channels which the BER pattern occupies has to be the same as the number of channels defined in the BER Length Register (BRLR) which defines how many BER channels are to be monitored by the BER receiver.

For each input stream, there is a set of registers for the BER test. The registers are as follows:

- BER Receiver Control Register (**BRCR**) - ST[n]CBER (bit 1) is used to clear the Bit Receiver Error Register (BRER). ST[n]SBER (bit 0) is used to enable the per-stream BER receiver.
- BER Receiver Start Register (**BRSR**) - ST[n]BRS7 - 0 (bit 7 - 0) defines the input channel from which the BER sequence will start to be compared.
- BER Receiver Length Register (**BRLR**) - ST[n]BL8 - 0 (bit 8 - 0) define how many channels the sequence will last. Depending on the data rate being used, the BER test can last for a maximum of 32, 64, 128 or 256 channels at the data rates of 2.048, 4.096, 8.192 or 16.384 Mbps, respectively. The minimum length of the BER test is a single channel. The user must take care to program the correct channel length for the BER test so that the channel length does not exceed the total number of channels available in the stream.

- BER Receiver Error Register (**BRER**) - This read-only register contains the number of counted errors. When the error count reaches 0xFFFF, the BER counter will stop updating so that it will not overflow. ST[n]CBER (bit 1) in the BER Receiver Control Register is used to reset the BRER register.

For normal BER operation, CMM (bit 0) must be 1 in the Connection Memory Low (CM_L). PCC1 - 0 (bits 2 - 1) in the Connection Memory Low must be programmed to “10” to enable the per-stream based BER transmitters. For each stream, the length (or total number of channels) of BER testing can be as long as one whole frame, but the channels MUST be consecutive. Upon completion of programming the connection memory, the corresponding BER receiver can be started by setting ST[n]SBER (bit 0) in the BRCR to high. There must be at least 2 frames (250 μs) between completion of connection memory programming and starting the BER receiver before the BER receiver can correctly identify BER errors. A 16 bit BER counter is used to count the number of bit errors.

19.0 PCM A-law/μ-law Translation

The ZL50021 provides per-channel code translation to be used to adapt pulse code modulation (PCM) voice or data traffic between networks which use different encoding laws. Code translation is valid in both Connection Mode and Message Mode.

In order to use this feature, the Connection Memory High (CM_H) entry for the output channel must be programmed. $\overline{\text{V}}$/D (bit 4) defines if the traffic in the channel is voice or data. Setting ICL1 - 0 (bits 3 - 2) programs the input coding law and OCL1 - 0 (bits 1- 0) programs the output coding law as shown in Table 14.

The different code options are:

Input Coding (ICL1- 0)	**Output Coding (OCL1 - 0)**	**Voice Coding ($\overline{\text{V}}$/D bit = 0)**	**Data Coding ($\overline{\text{V}}$/D bit = 1)**
00	00	ITU-T G.711 A-law	No code
01	01	ITU-T G.711 μ-law	Alternate Bit Inversion (ABI)
10	10	A-law without Alternate Bit Inversion (ABI)	Inverted Alternate Bit Inversion (ABI)
11	11	μ-law without Magnitude Inversion (MI)	All bits inverted

Table 14 - Input and Output Voice and Data Coding

For voice coding options, the ITU-T G.711 A-law and ITU-T G.711 μ-law are the standard rules for encoding. A-law without Alternate Bit Inversion (ABI) is an alternative code that does not invert the even bits (6, 4, 2, 0). μ-law without Magnitude Inversion (MI) is an alternative code that does not perform inversion of magnitude bits (6, 5, 4, 3, 2, 1, 0).

When transferring data code, the option “no code” does not invert the bits. The Alternate Bit Inversion (ABI) option inverts the even bits (6, 4, 2, 0) while the Inverted Alternate Bit Inversion (ABI) inverts the odd bits (7, 5, 3, 1). When the “All bits inverted” option is selected, all of the bits (7, 6, 5, 4, 3, 2, 1, 0) are inverted.

The input channel and output channel encoding law are configured independently. If the output channel coding is set to be different from the input channel, the ZL50021 performs translation between the two standards. If the input and output encoding laws are set to the same standard, no translation occurs. As the $\overline{\text{V}}$/D (bit 4) of the Connection Memory High (CM_H) must be set on a per-channel basis, it is not possible to translate between voice and data encoding laws.

20.0 Quadrant Frame Programming

By programming the Stream Input Quadrant Frame Registers (SIQFR0 - 31), users can divide one frame of input data into four quadrant frames and can force the LSB or MSB of every input channel in these quadrants to one or zero for robbed-bit signaling. The four quadrant frames are defined as follows:

Data Rate	Quadrant 0	Quadrant 1	Quadrant 2	Quadrant 3
2.048 Mbps	Channel 0 - 7	Channel 8 - 15	Channel 16 - 23	Channel 24 - 31
4.096 Mbps	Channel 0 - 15	Channel 16 - 31	Channel 32 - 47	Channel 48 - 63
8.192 Mbps	Channel 0 - 31	Channel 32 - 63	Channel 64 - 95	Channel 96 - 127
16.384 Mbps	Channel 0 - 63	Channel 64 - 127	Channel 128 - 191	Channel 192 - 255

Table 15 - Definition of the Four Quadrant Frames

When the quadrant frame control bits, STIN[n]Q3C2 - 0 (bit 11 - 9), STIN[n]Q2C2 - 0 (bit 8 - 6), STIN[n]Q1C2 - 0 (bit 5 - 3) or STIN[n]Q1C2 - 0 (bit 2 - 0), are set, the LSB or MSB of every input channel in the quadrant is forced to “1” or “0” as shown by the following table:

STIN[n]Q[y]C[2:0]	Action
0xx	Normal Operation
100	Replaces LSB of every channel in Quadrant y with ‘0’
101	Replaces LSB of every channel in Quadrant y with ‘1’
110	Replaces MSB of every channel in Quadrant y with ‘0’
111	Replaces MSB of every channel in Quadrant y with ‘1’
Note: y = 0, 1, 2, 3	

Table 16 - Quadrant Frame Bit Replacement

Note that Quadrant Frame Programming and BER reception cannot be used simultaneously on the same input stream.

21.0 JTAG Port

The JTAG test port is implemented to meet the mandatory requirements of the IEEE-1149.1 (JTAG) standard. The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller.

21.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the ZL50021 test functions. It consists of three input pins and one output pin as follows:

- **Test Clock Input (TCK)** - TCK provides the clock for the test logic. TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Selection Inputs (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to high when it is not driven from an external source.
- **Test Data Input (TDi)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. The registers are

described in a subsequent section. The received input data is sampled at the rising edge of the TCK pulse. This pin is internally pulled to high when it is not driven from an external source.

- **Test Data Output (TDo)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or test data register are serially shifted out towards TDo. The data from TDo is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDo driver is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)** - Resets the JTAG scan structure. This pin is internally pulled to high when it is not driven from an external source.

21.2 Instruction Register

The ZL50021 uses the public instructions defined in the IEEE-1149.1 standard. The JTAG interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDi when the TAP Controller is in its shifted-OR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDi and TDo during data register scanning.

21.3 Test Data Registers

As specified in the IEEE-1149.1 standard, the ZL50021 JTAG interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of boundary-scan cells arranged to form a scan path around the boundary of the ZL50021 core logic.
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDi to TDo.
- **The Device Identification Register** - The JTAG device ID for the ZL50021 is 0C36514B$_H$

Version	<31:28>	0000
Part Number	<27:12>	1100 0011 0110 0101
Manufacturer ID	<11:1>	0001 0100 101
LSB	<0>	1

21.4 BSDL

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE-1149.1 test interface.

22.0 Register Address Mapping

Address A13 - A0	CPU Access	Register Name	Abbreviation	Reset By
0000_H	R/W	Control Register	CR	Switch/Hardware
0001_H	R/W	Internal Mode Selection Register	IMS	Switch/Hardware
0002_H	R/W	Software Reset Register	SRR	Hardware Only
0003_H	R/W	Output Clock and Frame Pulse Control Register	OCFCR	DPLL/Hardware
0004_H	R/W	Output Clock and Frame Pulse Selection Register	OCFSR	DPLL/Hardware
0005_H	R/W	FPo_OFF0 Register	FPOFF0	DPLL/Hardware
0006_H	R/W	FPo_OFF1 Register	FPOFF1	DPLL/Hardware
0007_H	R/W	FPo_OFF2 Register	FPOFF2	DPLL/Hardware
0010_H	R Only	Internal Flag Register	IFR	Switch/Hardware
0011_H	R Only	BER Error Flag Register 0	BERFR0	Switch/Hardware
0012_H	R Only	BER Error Flag Register 1	BERFR1	Switch/Hardware
0013_H	R Only	BER Receiver Lock Register 0	BERLR0	Switch/Hardware
0014_H	R Only	BER Receiver Lock Register 1	BERLR1	Switch/Hardware
0040_H	R/W	DPLL Control Register	DPLLCR	DPLL/Hardware
0041_H	R/W	Reference Frequency Register	RFR	DPLL/Hardware
0042_H	R/W	Centre Frequency Register - Lower 16 Bits	CFRL	DPLL/Hardware
0043_H	R/W	Centre Frequency Register - Upper 10 Bits	CFRU	DPLL/Hardware
0044_H	R/W	Software Delta Frequency Register	SWDFR	DPLL/Hardware
0045_H	R Only	Frequency Offset Register	FOR	DPLL/Hardware
0046_H	R/W	Frequency Locking Range Register	FLRR	DPLL/Hardware
0047_H	R/W	Lock Detector Threshold Register	LDTR	DPLL/Hardware
0048_H	R/W	Lock Detector Interval Register	LDIR	DPLL/Hardware
0049_H	R/W	Slew Rate Limit Register	SRLR	DPLL/Hardware
$004A_H$	R/W	Bandwidth Control Register	BWCR	DPLL/Hardware
$004B_H$	R/W	Reference Change Control Register	RCCR	DPLL/Hardware
$004C_H$	R Only	Reference Change Status Register	RCSR	DPLL/Hardware
$004E_H$	R/W	Multi-period Near Upper Limit Register - Lower 16 Bits	MPNULRL	DPLL/Hardware

Table 17 - Address Map for Registers (A13 = 0)

$004F_H$	R/W	Multi-period Near Upper Limit Register - Upper 16 Bits	MPNULRU	DPLL/Hardware
0050_H	R/W	Multi-period Far Upper Limit Register - Lower 16 Bits	MPFULRL	DPLL/Hardware
0051_H	R/W	Multi-period Far Upper Limit Register - Upper 16 Bits	MPFULRU	DPLL/Hardware
0052_H	R/W	Multi-period Near Lower Limit Register - Lower 16 Bits	MPNLLRL	DPLL/Hardware
0053_H	R/W	Multi-period Near Lower Limit Register - Upper 16 Bits	MPNLLRU	DPLL/Hardware
0054_H	R/W	Multi-period Far Lower Limit Register - Lower 16 Bits	MPFLLRL	DPLL/Hardware
0055_H	R/W	Multi-period Far Lower Limit Register - Upper 16 Bits	MPFLLRU	DPLL/Hardware
0056_H	R/W	Reference 0 Multi-period Count Register - Lower 16 Bits	R0MPCRL	DPLL/Hardware
0057_H	R/W	Reference 0 Multi-period Count Register - Upper 16 Bits	R0MPCRU	DPLL/Hardware
0058_H	R/W	Reference 0 Upper Limit Register	R0ULR	DPLL/Hardware
0059_H	R/W	Reference 0 Lower Limit Register	R0LLR	DPLL/Hardware
$005A_H$	R/W	Reference 1 Multi-period Count Register - Lower 16 Bits	R1MPCRL	DPLL/Hardware
$005B_H$	R/W	Reference 1 Multi-period Count Register - Upper 16 Bits	R1MPCRU	DPLL/Hardware
$005C_H$	R/W	Reference 1 Upper Limit Register	R1ULR	DPLL/Hardware
$005D_H$	R/W	Reference 1 Lower Limit Register	R1LLR	DPLL/Hardware
$005E_H$	R/W	Reference 2 Multi-period Count Register - Lower 16 Bits	R2MPCRL	DPLL/Hardware
$005F_H$	R/W	Reference 2 Multi-period Count Register - Upper 16 Bits	R2MPCRU	DPLL/Hardware
0060_H	R/W	Reference 2 Upper Limit Register	R2ULR	DPLL/Hardware
0061_H	R/W	Reference 2 Lower Limit Register	R2LLR	DPLL/Hardware
0062_H	R/W	Reference 3 Multi-period Count Register - Lower 16 Bits	R3MPCRL	DPLL/Hardware
0063_H	R/W	Reference 3 Multi-period Count Register - Upper 16 Bits	R3MPCRU	DPLL/Hardware
0064_H	R/W	Reference 3 Upper Limit Register	R3ULR	DPLL/Hardware
0065_H	R/W	Reference 3 Lower Limit Register	R3LLR	DPLL/Hardware
0066_H	R Only	Interrupt Register	IR	DPLL/Hardware
0067_H	R/W	Interrupt Mask Register	IMR	DPLL/Hardware
0068_H	R/W	Interrupt Clear Register	ICR	DPLL/Hardware
0069_H	R Only	Reference Status Register	RSR	DPLL/Hardware
$006A_H$	R/W	Reference Mask Register	RMR	DPLL/Hardware
$006B_H$	R Only	Reference Frequency Status Register	RFSR	DPLL/Hardware
$006C_H$	R/W	Output Jitter Control Register	OJCR	DPLL/Hardware
0100_H - $011F_H$	R/W	Stream Input Control Registers 0 - 31	SICR0 - 31	Switch/Hardware

Table 17 - Address Map for Registers (A13 = 0) (continued)

0120_H - $013F_H$	R/W	Stream Input Quadrant Frame Registers 0 - 31	SIQFR0 - 31	Switch/Hardware
0200_H - $021F_H$	R/W	Stream Output Control Registers 0 - 31	SOCR0 - 31	Switch/Hardware
0300_H - $031F_H$	R/W	BER Receiver Start Registers 0 - 31	BRSR0 - 31	Switch/Hardware
0320_H - $033F_H$	R/W	BER Receiver Length Registers 0 - 31	BRLR0 - 31	Switch/Hardware
0340_H - $035F_H$	R/W	BER Receiver Control Registers 0 - 31	BRCR0 - 31	Switch/Hardware
0360_H - $037F_H$	R Only	BER Receiver Error Registers 0 - 31	BRER0 - 31	Switch/Hardware

Table 17 - Address Map for Registers (A13 = 0) (continued)

23.0 Detailed Register Description

External Read/Write Address: 0000$_H$
Reset Value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SLV_ DPLLEN	OPM 1	OPM 0	CKi_ LP	FPIN POS	CKINP	FPINP	CKIN 1	CKIN 0	VAR EN	MBPE	OSB	MS1	MS0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 14</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>13</td><td>SLV_ DPLLEN</td><td>DPLL Enable in Slave Mode (Ignored in Master Mode).
When this bit is low, DPLL is disabled in Slave mode.
When this bit is high and OSC_EN = 1, the DPLL is enabled in Slave mode.
When SLV_DPLLEN is set in Slave mode, CKo[3:0] and FPo[3:0] are generated from CKi and FPi. CKo[5:4] and FPo[5] are locked to the selected input reference (one of REF[3:0]). In this mode of operation, the DPLL retains its functionality, including the generation of the REF_FAIL[3:0] output signals. See Table 7, “ZL50021 Operating Modes” on page 38 for more details.</td></tr>
<tr><td>12 - 11</td><td>OPM1 - 0</td><td>Operation Mode
These bits are used to set the device in Master/Slave operation. Refer to Table 7, “ZL50021 Operating Modes” on page 38 for more details.</td></tr>
<tr><td>10</td><td>CKi_LP</td><td>CKi and FPi Loopback (Ignored in Slave mode)
When this bit is low, CKi and FPi are used as input pins.
When this bit is high, CKi and FPi are internally looped back from CKo2 (16.384 MHz) and FPo2 respectively, and CKi pin and FPi pin should be tied low or high externally; CKIN1 - 0 (bits 6 - 5) of this register should be programmed to be 00. See Table 7, “ZL50021 Operating Modes” on page 38 for more details.</td></tr>
<tr><td>9</td><td>FPINPOS</td><td>Input Frame Pulse (FPi) Position
When this bit is low, FPi straddles frame boundary (as defined by ST-BUS).
When this bit is high, FPi starts from frame boundary (as defined by GCI-Bus)</td></tr>
<tr><td>8</td><td>CKINP</td><td>Clock Input (CKi) Polarity
When this bit is low, the CKi falling edge aligns with the frame boundary.
When this bit is high, the CKi rising edge aligns with the frame boundary.</td></tr>
<tr><td>7</td><td>FPINP</td><td>Frame Pulse Input (FPi) Polarity
When this bit is low, the input frame pulse FPi has the negative frame pulse format.
When this bit is high, the input frame pulse FPi has the positive frame pulse format.</td></tr>
<tr><td>6 - 5</td><td>CKIN1 - 0</td><td>Input Clock (CKi) and Frame Pulse (FPi) Selection
<table>
<tr><td>CKIN1 - 0</td><td>FPi Active Period</td><td>CKi</td></tr>
<tr><td>00</td><td>61 ns</td><td>16.384 MHz</td></tr>
<tr><td>01</td><td>122 ns</td><td>8.192 MHz</td></tr>
<tr><td>10</td><td>244 ns</td><td>4.096 MHz</td></tr>
<tr><td>11</td><td colspan="2">Reserved</td></tr>
</table>
The MODE_4M0 and MODE_4M1 pins, as described in “Pin Description” on page 13, should also be set to define the input clock mode.</td></tr>
</table>

Table 18 - Control Register (CR) Bits

External Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SLV_ DPLLEN	OPM 1	OPM 0	CKi_ LP	FPIN POS	CKINP	FPINP	CKIN 1	CKIN 0	VAR EN	MBPE	OSB	MS1	MS0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>4</td><td>VAREN</td><td>Variable Delay Mode Enable
When this bit is low, the variable delay mode is disabled on a device-wide basis.
When this bit is high, the variable delay mode is enabled on a device-wide basis.</td></tr>
<tr><td>3</td><td>MBPE</td><td>Memory Block Programming Enable
When this bit is high, the connection memory block programming mode is enabled to program the connection memory. When it is low, the memory block programming mode is disabled.</td></tr>
<tr><td>2</td><td>OSB</td><td>Output Stand By Bit
This bit enables the STio0 - 31 and the STOHZ0 -15 serial outputs. The following table describes the HiZ control of the serial data outputs:
<table>
<tr><th>$\overline{\text{RESET}}$ Pin</th><th>SRSTSW (in SRR)</th><th>ODE Pin</th><th>OSB Bit</th><th>STio0 - 31</th><th>STOHZ0 - 15</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>X</td><td>HiZ</td><td>Driven High</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>X</td><td>HiZ</td><td>Driven High</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>X</td><td>HiZ</td><td>Driven High</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>HiZ</td><td>Driven High</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Active (Controlled by CM)</td><td>Active (Controlled by CM)</td></tr>
</table>
Note: Unused output streams are tristated (STio = HiZ, STOHZ = Driven High). Refer to SOCR0 - 31 (bit2 - 0).</td></tr>
<tr><td>1 - 0</td><td>MS1 - 0</td><td>Memory Select Bits These two bits are used to select connection memory low, connection high or data memory for access by CPU:
<table>
<tr><th>MS1 - 0</th><th>Memory Selection</th></tr>
<tr><td>00</td><td>Connection Memory Low Read/Write</td></tr>
<tr><td>01</td><td>Connection Memory High Read/Write</td></tr>
<tr><td>10</td><td>Data Memory Read</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Table 18 - Control Register (CR) Bits (continued)

External Read/Write Address: 0001_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIO_ PD_EN	BDH	BDL	RBER EN	TBER EN	BPD 2	BPD 1	BPD 0	MBPS

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 9</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>8</td><td>STIO_PD_ EN</td><td>STio Pull-down Enable
When this bit is low, the pull-down resistors on all STio pads will be disabled.
When this bit is high, the pull-down resistors on all STio pads will be enabled.</td></tr>
<tr><td>7</td><td>BDH</td><td>Bi-directional Control for Streams 16-31
<table>
<tr><th>BDH</th><th>STio16 - 31 Operation</th></tr>
<tr><td>0</td><td>normal operation:
STi16-31 are inputs
STio16-31 are outputs</td></tr>
<tr><td>1</td><td>bi-directional operation:
STi16-31 tied low internally
STio16-31 are bi-directional</td></tr>
</table></td></tr>
<tr><td>6</td><td>BDL</td><td>Bi-directional Control for Streams 0-15
<table>
<tr><th>BDL</th><th>STio0 - 15 Operation</th></tr>
<tr><td>0</td><td>normal operation:
STi0-15 are inputs
STio0-15 are outputs</td></tr>
<tr><td>1</td><td>bi-directional operation:
STi0-15 tied low internally
STio0-15 are bi-directional</td></tr>
</table></td></tr>
<tr><td>5</td><td>RBEREN</td><td>PRBS Receiver Enable: When this bit is low, all the BER receivers are disabled. To enable any BER receivers, this bit MUST be high.</td></tr>
<tr><td>4</td><td>TBEREN</td><td>PRBS Transmitter Enable: When this bit is low, all the BER transmitters are disabled. To enable any BER transmitters, this bit MUST be high.</td></tr>
<tr><td>3 - 1</td><td>BPD2 - 0</td><td>Block Programming Data: These bits refer to the value to be loaded into the connection memory, whenever the memory block programming feature is activated. After the MBPE bit in the Control Register is set to high and the MBPS bit in this register is set to high, the contents of the bits BPD2 - 0 are loaded into bits 2 - 0 of the Connection Memory Low. Bits 15 - 3 of the Connection Memory Low and bits 15 - 0 of Connection Memory High are zeroed.</td></tr>
</table>

Table 19 - Internal Mode Selection Register (IMS) Bits

External Read/Write Address: 0001_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIO_ PD_EN	BDH	BDL	RBER EN	TBER EN	BPD 2	BPD 1	BPD 0	MBPS

Bit	Name	Description
0	MBPS	**Memory Block Programming Start:** A zero to one transition of this bit starts the memory block programming function. The MBPS and BPD2 - 0 bits in this register must be defined in the same write operation. Once the MBPE bit in the Control Register is set to high, the device requires two frames to complete the block programming. After the programming function has finished, the MBPS bit returns to low, indicating the operation is completed. When MBPS is high, MBPS or MBPE can be set to low to abort the programming operation. Whenever the microprocessor writes a one to the MBPS bit, the block programming function is started. As long as this bit is high, the user must maintain the same logical value to the other bits in this register to avoid any change in the device setting.

Table 19 - Internal Mode Selection Register (IMS) Bits (continued)

External Read/Write Address: 0002_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST SW	SRST DPLL

Bit	Name	Description
15 - 2	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
1	SRSTSW	**Software Reset Bit for Switch:** When this bit is low, data switching blocks are in normal operation. When this bit is high, data switching blocks are in software reset state. Refer to Table 17, “Address Map for Registers (A13 = 0)” on page 53 for details regarding which registers are affected.
0	SRSTDPLL	**Software Reset Bit for DPLL:** When this bit is low, the DPLL block is in normal operation. When this bit is high, the DPLL block is in software reset state. Refer to Table 17, “Address Map for Registers (A13 = 0)” on page 53 for details regarding which registers are affected.

Table 20 - Software Reset Register (SRR) Bits

External Read/Write Address: 0003_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FPOF2 EN	FPOF1 EN	FPOF0 EN	CKO5 EN	CKO4 EN	CKO FPO3 EN	CKO FPO2 EN	CKO FPO1 EN	CKO FPO0 EN

Bit	Name	Description
15 - 9	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
8	FPOF2EN	**FPo_OFF2/FPo5 Enable** When this bit is high, output frame pulse FPo_OFF2/FPo5 is enabled. When this bit is low, output frame pulse FPo_OFF2/FPo5 is in high impedance state.
7	FPOF1EN	**FPo_OFF1 Enable** When this bit is high, output frame pulse FPo_OFF1 is enabled. When this bit is low, output frame pulse FPo_OFF1 is in high impedance state.
6	FPOF0EN	**FPo_OFF0 Enable** When this bit is high, output frame pulse FPo_OFF0 is enabled. When this bit is low, output frame pulse FPo_OFF0 is in high impedance state.
5	CKO5EN	**CKo5 Enable** When this bit is high, output clock CKo5 is enabled. When this bit is low, output clock CKo5 is in high impedance state. CKo5 is available in Master mode or in Slave mode with SLV_DPLLEN set.
4	CKO4EN	**CKo4 Enable** When this bit is high, output clock CKo4 is enabled. When this bit is low, output clock CKo4 is in high impedance state. CKo4 is available in Master mode or in Slave mode with SLV_DPLLEN set.
3	CKOFPO3 EN	**CKo3 and FPo3 Enable** When this bit is high, output clock CKo3 and output frame pulse FPo3 are enabled. When this bit is low, CKo3 and FPo3 are in high impedance state.
2	CKOFPO2 EN	**CKo2 and FPo2 Enable** When this bit is high, output clock CKo2 and output frame pulse FPo2 are enabled. When this bit is low, CKo2 and FPo2 are in high impedance state.
1	CKOFPO1 EN	**CKo1 and FPo1 Enable** When this bit is high, output clock CKo1 and output frame pulse FPo1 are enabled. When this bit is low, CKo1 and FPo1 are in high impedance state.
0	CKOFPO0 EN	**CKo0 and FPo0 Enable** When this bit is high, output clock CKo0 and output frame pulse FPo0 are enabled. When this bit is low, CKo0 and FPo0 are in high impedance state.

Table 21 - Output Clock and Frame Pulse Control Register (OCFCR) Bits

External Read/Write Address: 0004_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKO4 P	CKO4 SEL	CKO FPO3 SEL1	CKO FPO3 SEL0	CKO3 P	FPO3 P	FPO3 POS	CKO2 P	FPO2 P	FPO2 POS	CKO1 P	FPO1 P	FPO1 POS	CKO0 P	FPO0 P	FPO0 POS

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15</td><td>CKO4P</td><td>Output Clock (CKo4) Polarity Selection
When this bit is low, the output clock CKo4 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo4 rising edge aligns with the frame boundary.
CKo4 is available in Master mode or in Slave mode with SLV_DPLLEN set.</td></tr>
<tr><td>14</td><td>CKO4SEL</td><td>Output Clock (CKo4) Frequency Selection
When this bit is low, the output clock CKo4 is 2.048 MHz.
When this bit is high, the output clock CKo4 is 1.544 MHz.
CKo4 is available in Master mode or in Slave mode with SLV_DPLLEN set.</td></tr>
<tr><td>13 - 12</td><td>CKOFPO3 SEL1 - 0</td><td>Output Clock (CKo3) Frequency and Output Frame Pulse (FPo3) Pulse Cycle Selection
<table>
<tr><th>CKOFPO3 SEL1 - 0</th><th>FPo3</th><th>CKo3</th></tr>
<tr><td>00</td><td>244 ns</td><td>4.096 MHz</td></tr>
<tr><td>01</td><td>122 ns</td><td>8.192 MHz</td></tr>
<tr><td>10</td><td>61 ns</td><td>16.384 MHz</td></tr>
<tr><td>11</td><td>30 ns</td><td>32.768 MHz</td></tr>
</table>
</td></tr>
<tr><td>11</td><td>CKO3P</td><td>Output Clock (CKo3) Polarity Selection
When this bit is low, the output clock CKo3 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo3 rising edge aligns with the frame boundary.</td></tr>
<tr><td>10</td><td>FPO3P</td><td>Output Frame Pulse (FPo3) Polarity Selection
When this bit is low, the output frame pulse FPo3 has the negative frame pulse format.
When this bit is high, the output frame pulse FPo3 has the positive frame pulse format.</td></tr>
<tr><td>9</td><td>FPO3POS</td><td>Output Frame Pulse (FPo3) Position
When this bit is low, FPo3 straddles frame boundary (as defined by ST-BUS).
When this bit is high, FPo3 starts from frame boundary (as defined by GCI-Bus).</td></tr>
<tr><td>8</td><td>CKO2P</td><td>Output Clock (CKo2) Polarity Selection
When this bit is low, the output clock CKo2 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo2 rising edge aligns with the frame boundary.</td></tr>
<tr><td>7</td><td>FPO2P</td><td>Output Frame Pulse (FPo2) Polarity Selection
When this bit is low, the output frame pulse FPo2 has the negative frame pulse format.
When this bit is high, the output frame pulse FPo2 has the positive frame pulse format.</td></tr>
</table>

Table 22 - Output Clock and Frame Pulse Selection Register (OCFSR) Bits

External Read/Write Address: 0004_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKO4 P	CKO4 SEL	CKO FPO3 SEL1	CKO FPO3 SEL0	CKO3 P	FPO3 P	FPO3 POS	CKO2 P	FPO2 P	FPO2 POS	CKO1 P	FPO1 P	FPO1 POS	CKO0 P	FPO0 P	FPO0 POS

Bit	Name	Description
6	FPO2POS	**Output Frame Pulse (FPo2) Position** When this bit is low, FPo2 straddles frame boundary (as defined by ST-BUS). When this bit is high, FPo2 starts from frame boundary (as defined by GCI-Bus).
5	CKO1P	**Output Clock (CKo1) Polarity Selection** When this bit is low, the output clock CKo1 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo1 rising edge aligns with the frame boundary.
4	FPO1P	**Output Frame Pulse (FPo1) Polarity Selection** When this bit is low, the output frame pulse FPo1 has the negative frame pulse format. When this bit is high, the output frame pulse FPo1 has the positive frame pulse format.
3	FPO1POS	**Output Frame Pulse (FPo1) Position** When this bit is low, FPo1 straddles frame boundary (as defined by ST-BUS). When this bit is high, FPo1 starts from frame boundary (as defined by GCI-Bus).
2	CKO0P	**Output Clock (CKo0) Polarity Selection** When this bit is low, the output clock CKo0 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo0 rising edge aligns with the frame boundary.
1	FPO0P	**Output Frame Pulse (FPo0) Polarity Selection** When this bit is low, the output frame pulse FPo0 has the negative frame pulse format. When this bit is high, the output frame pulse FPo0 has the positive frame pulse format.
0	FPO0POS	**Output Frame Pulse (FPo0) Position** When this bit is low, FPo0 straddles frame boundary (as defined by ST-BUS). When this bit is high, FPo0 starts from frame boundary (as defined by GCI-Bus).

Note: In Divided Slave modes, CKo3 - 1 cannot exceed frequency of CKi.
Note: CKo[5:4] are available in Master mode or in Slave mode with SLV_DPLLEN set.

Table 22 - Output Clock and Frame Pulse Selection Register (OCFSR) Bits (continued)

External Read/Write Address: 0005_H - 0007_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	FP19 EN	FOF[n] OFF7	FOF[n] OFF6	FOF[n] OFF5	FOF[n] OFF4	FOF[n] OFF3	FOF[n] OFF2	FOF[n] OFF1	FOF[n] OFF0	FOF[n] C1	FOF[n] C0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 11</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>10</td><td>FP19EN</td><td>19.44 MHz Frame Pulse Output Enable. (For FPo_OFF2 only)
This bit is a reserved bit for FPo_OFF0 and FPo_OFF1, and MUST be set to zero.
When this bit is high, FPo_OFF2 is negative frame pulse output corresponding to 19.44 MHz without channel offset.
When this bit is low, FPo_OFF2 is output frame pulse with channel offset.</td></tr>
<tr><td>9 - 2</td><td>FOF[n]OFF7 - 0</td><td>FPo_OFF[n] Channel Offset
The binary value of these bits refers to the channel offset from original frame boundary. Permitted channel offset values depend on bits 1-0 of this register.</td></tr>
<tr><td>1 - 0</td><td>FOF[n]C1 - 0</td><td>FPo_OFF[n] Control bits
<table>
<tr><th>FOF[n]C 1-0</th><th>Data Rate (Mbps)</th><th>FPo_OFF[n] Pulse Cycle Width</th><th>FOF[n]OFF7 - 0 Permitted Channel Offset</th><th>Polarity Control</th><th>Position Control</th></tr>
<tr><td>00</td><td>2.048</td><td>one 4.096 MHz clock</td><td>0 - 31</td><td>FPO0P</td><td>FPO0POS</td></tr>
<tr><td>01</td><td>4.096</td><td>one 8.192 MHz clock</td><td>0 - 63</td><td>FPO1P</td><td>FPO1POS</td></tr>
<tr><td>10</td><td>8.192</td><td>one 16.384 MHz clock</td><td>0 - 127</td><td>FPO2P</td><td>FPO2POS</td></tr>
<tr><td>11</td><td>16.384</td><td>one 16.384 MHz clock</td><td>0 - 255</td><td>FPO2P</td><td>FPO2POS</td></tr>
</table></td></tr>
<tr><td colspan="3">Note: [n] denotes output offset frame pulse from 0 to 2.</td></tr>
</table>

Table 23 - FPo_OFF[n] Register (FPo_OFF[n]) Bits

External Read Address: 0010_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	OUT ERR	IN ERR

Bit	Name	Description
15 - 2	Unused	**Reserved** In normal functional mode, these bits are zero.
1	OUTERR	**Output Error (Read Only)** This bit is set high when the total number of output channels is programmed to be more than the maximum capacity of 4096, in which case the output channels beyond the maximum capacity should be disabled. This bit will be cleared automatically after programming is corrected.
0	INERR	**Input Error (Read Only)** This bit is set high when the total number of input channels is programmed to be more than the maximum capacity of 4096, in which case the input channels beyond the maximum capacity should be disabled.This bit will be cleared automatically after programming is corrected.

Table 24 - Internal Flag Register (IFR) Bits - Read Only

External Read Address: 00011_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER F15	BER F14	BER F13	BER F12	BER F11	BER F10	BER F9	BER F8	BER F7	BER F6	BER F5	BER F4	BER F3	BER F2	BER F1	BER F0

Bit	Name	Description
15 - 0	BERF[n]	**BER Error Flag[n]** If BERF[n] is high, it indicates that BER Receiver Error Register [n] (BRER[n]) is not zero. If BERF[n] is low, it indicates that BER Receiver Error Register [n] (BRER[n]) is zero.
Note: [n] denotes input stream from 0 - 15.		

Table 25 - BER Error Flag Register 0 (BERFR0) Bits - Read Only

External Read/Write Address: 00012_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER F31	BER F30	BER F29	BER F28	BER F27	BER F26	BER F25	BER F24	BER F23	BER F22	BER F21	BER F20	BER F19	BER F18	BER F17	BER F16

Bit	Name	Description
15 - 0	BERF[n]	**BER Error Flag[n]** If BERF[n] is high, it indicates that BER Receiver Error Register [n] (BRER[n]) is not zero. If BERF[n] is low, it indicates that BER Receiver Error Register [n] (BRER[n]) is zero.
Note: [n] denotes input stream from 16 - 31.		

Table 26 - BER Error Flag Register 1 (BERFR1) Bits - Read Only

External Read Address: 00013_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER L15	BER L14	BER L13	BER L12	BER L11	BER L10	BER L9	BER L8	BER L7	BER L6	BER L5	BER L4	BER L3	BER L2	BER L1	BER L0

Bit	Name	Description
15 - 0	BERL[n]	**BER Receiver Lock[n]** If BERL[n] is high, it indicates that BER Receiver of STi[n] is locked. If BERL[n] is low, it indicates that BER Receiver of STi[n] is not locked.
Note: [n] denotes input stream from 0 - 15.		

Table 27 - BER Receiver Lock Register 0 (BERLR0) Bits - Read Only

External Read Address: 00014_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER L31	BER L30	BER L29	BER L28	BER L27	BER L26	BER L25	BER L24	BER L23	BER L22	BER L21	BER L20	BER L19	BER L18	BER L17	BER L16

Bit	Name	Description
15 - 0	BERL[n]	**BER Receiver Lock[n]** If BERL[n] is high, it indicates that BER Receiver of STi[n] is locked. If BERL[n] is low, it indicates that BER Receiver of STi[n] is not locked.

Note: [n] denotes input stream from 16 - 31.

Table 28 - BER Receiver Lock Register 1 (BERLR1) Bits - Read Only

External Read/Write Address: 0040_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	LIN_ RES	SM_ FST	0	SWF	SWE	MRLE	RFRE	DPLL _IRM

Bit	Name	Description
15-8	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
7	LIN_RES	**Linear Response of DPLL Phase Multiplier.** When this bit is high, linear phase multiplication will be used to determine the jitter transfer characteristics. (Follow the jitter transfer as per BWCR register for small and large jitter amplitude). When this bit is low, non-linear phase multiplication will be used to determine the jitter transfer characteristics. (Only high jitter amplitudes follow the jitter transfer as per BWCR register). When 0, DPLL has better holdover stability and output jitter.
6	SM_FST	**Semi-Fast Locking Control Bit.** When this bit is high, the semi-fast locking mode is enabled, allowing the Fast Frequency Lock (FFL3 - 0) bits in the BWCR register to be used even if the DPLL slew rate limiter is not bypassed. When this bit is low, the FFL3 - 0 bits in the BWCR register are ignored if the Bypass Limiter bit (BLM) in the BWCR register is not set.
5	Unused	**Reserved.** In normal functional mode, this bit **MUST** be set to zero.

Table 29 - DPLL Control Register (DPLLCR) Bits

External Read/Write Address: 0040_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	LIN_ RES	SM_ FST	0	SWF	SWE	MRLE	RFRE	DPLL _IRM

Bit	Name	Description
4	SWF	**Software Mode Fast Control Bit.** When this bit is low, the SWE bit is high, and the DPLL is in freerun mode (the FDM1 - 0 bits of the RCCR register are ='11'), the software slow control mode is enabled. The DPLL outputs will stabilize to delta frequency contents of Software Delta Frequency Register (SWDFR), after programmed internal DPLL filter response and phase alignment speed (phase slope) time. When this bit is high, the SWE bit is high, and the DPLL is in freerun mode, the software fast control mode is enabled. The DPLL outputs will reach the delta frequency contents of Software Delta Frequency Register (SWDFR), immediately after writing to the Software Delta Frequency Register, therefore allowing external software filters and phase alignment speed (phase slope) limiters to be used. This case will usually require very frequent updating of the SWDFR register. When the SWE bit is low or the DPLL is not in freerun mode, this bit is ignored.
3	SWE	**Software Mode Enable Bit.** When this bit is low, the Software Delta Frequency Register (SWDFR) content is ignored and the software mode of the DPLL is disabled. When this bit is high and the DPLL is in freerun mode, the DPLL software mode is enabled, meaning that the Software Delta Frequency Register content is used to control the DPLL output frequency, depending on the value of SWF bit of this register. When the DPLL is not in freerun mode, this bit is ignored.
2	MRLE	**Monitor Register Limits Enable Bit.** When this bit is low, the monitor register content is ignored and the Stratum 3 default value for each detected reference frequency is used to set up the DPLL's reference monitoring functions. When this bit is high, the monitor registers contents are used to control the monitoring functionality of the DPLL. The following registers are affected: RnULR, RnLLR, RnMPCRL, RnMPCRU, MPNULRL, MPNULRU, MPFULRL, MPFULRU, MPNLLRL, MPNLLRU, MPFLLRL, MPFLLRU.
1	RFRE	**Reference Frequency Register Enable:** When this bit is low, the reference frequency value used in the DPLL comes from appropriate reference frequency detector. When this bit is high, the reference frequency value comes from Reference Frequency Register (RFR).
0	DPLL_ IRM	**DPLL Internal Reset Mode:** When this bit is low, the DPLL module is in the operational state. When this bit is high, the DPLL module is in the power saving mode. Registers are not reset and are still accessible in the power saving mode.

Table 29 - DPLL Control Register (DPLLCR) Bits (continued)

External Read/Write Address: 0041_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	R3F2	R3F1	R3F0	R2F2	R2F1	R2F0	R1F2	R1F1	R1F0	R0F2	R0F1	R0F0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15-12</td><td>Unused</td><td>Reserved
In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>11 - 9</td><td>R3F2 - 0</td><td>Reference 3 Frequency Bits
When the RFRE bit of the DPLLCR register is high, these bits are used to select the REF3 input frequency. When the RFRE bit is low, these bits are ignored.
<table>
<tr><th>R3F2</th><th>R3F1</th><th>R3F0</th><th>REF 3 Input Frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.544 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2.048 MHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4.096 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8.192 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16.384 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>19.44 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>8 - 6</td><td>R2F2 - 0</td><td>Reference 2 Frequency Bits: When the RFRE bit of the DPLLCR register is high, these bits are used to select the REF2 input frequency. When the RFRE bit is low, these bits are ignored.
<table>
<tr><th>R2F2</th><th>R2F1</th><th>R2F0</th><th>REF 2 Input Frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.544 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2.048 MHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4.096 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8.192 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16.384 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>19.44 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Table 30 - Reference Frequency Register (RFR) Bits

External Read/Write Address: 0041$_H$
Reset Value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	R3F2	R3F1	R3F0	R2F2	R2F1	R2F0	R1F2	R1F1	R1F0	R0F2	R0F1	R0F0

Bit	Name	Description
5 - 3	R1F2 - 0	**Reference 1 Frequency Bits** When the RFRE bit of the DPLLCR register is high, these bits are used to select the REF1 input frequency. When the RFRE bit is low, these bits are ignored.
2 - 0	R0F2 - 0	**Reference 0 Frequency Bits** When the RFRE bit of the DPLLCR register is high, these bits are used to select the REF0 input frequency. When the RFRE bit is low, these bits are ignored.

R1F2	R1F1	R1F0	REF 1 Input Frequency
0	0	0	8 kHz
0	0	1	1.544 MHz
0	1	0	2.048 MHz
0	1	1	4.096 MHz
1	0	0	8.192 MHz
1	0	1	16.384 MHz
1	1	0	19.44 MHz
1	1	1	Reserved

R0F2	R0F1	R0F0	REF 0 Input Frequency
0	0	0	8 kHz
0	0	1	1.544 MHz
0	1	0	2.048 MHz
0	1	1	4.096 MHz
1	0	0	8.192 MHz
1	0	1	16.384 MHz
1	1	0	19.44 MHz
1	1	1	Reserved

Table 30 - Reference Frequency Register (RFR) Bits (continued)

External Read/Write Address: 0042_H
Reset Value: $16B1_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFN 15	CFN 14	CFN 13	CFN 12	CFN 11	CFN 10	CFN 9	CFN 8	CFN 7	CFN 6	CFN 5	CFN 4	CFN 3	CFN 2	CFN 1	CFN 0

Bit	Name	Description
15 - 0	CFN15 - 0	**Center Frequency Number (CFN) Lower 16 Bits:** The total binary value of these bits and the CFRU register bits defines the output center frequency number according to the following formula: $f_{OUT} = \frac{CFN}{2^{26}} \times f_{MCLK}$ where, f_{OUT} is desired output center frequency, while f_{MCLK} is frequency of DPLL master clock. For given master clock frequency of 100 MHz, and desired output center frequency of 65.536 MHz, the CFN has the value of: $CFN = 2^{26} \times \frac{65.536MHz}{100MHz} = 2^{26} \times 0.65536 = 43980465 = 29F16B1_H$ The register contents should be changed only if compensation for input oscillator (or crystal) frequency offset is required. e.g., if master clock frequency is off by +20 ppm (100.002 MHz -> 5 times multiplied c20i of 20.0004 MHz), the CFN should be programmed to be: $CFN = 2^{26} \times \frac{65.536MHz}{100.002MHz} = 2^{26} \times 0.65534689 = 43979585 = 29F1341_H$ The default value of this register **SHOULD NOT** be changed in any other circumstances.

Table 31 - Centre Frequency Register - Lower 16 Bits (CFRL)

External Read/Write Address: 0043_H
Reset Value: $029F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	CFN 25	CFN 24	CFN 23	CFN 22	CFN 21	CFN 20	CFN 19	CFN 18	CFN 17	CFN 16

Bit	Name	Description
15 - 10	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
9 - 0	CFN25 - 16	**Center Frequency Number (CFN) Upper 10 Bits:** The total binary value of these bits and the CFRL register bits represents the center frequency number (CFN) explained under CFRL register bits explanation. The default value of this register should be changed only if compensation for input oscillator (or crystal) frequency offset is required, and **SHOULD NOT** be changed in any other circumstances.

Table 32 - Centre Frequency Register - Upper 10 Bits (CFRU)

External Read/Write Address: 0044_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SDF 14	SDF 13	SDF 12	SDF 11	SDF 10	SDF 9	SDF 8	SDF 7	SDF 6	SDF 5	SDF 4	SDF 3	SDF 2	SDF 1	SDF 0

Bit	Name	Description
15	Unused	**Reserved.** In normal functional mode, this bit **MUST** be set to zero.
14 - 0	SDF14 - 0	**Software Delta Frequency Bits:** When the SWE bit in the DPLLCR register is high and the DPLL is in freerun mode (the FDM1-0 bits of the RCCR register are ='11'), the binary value of these bits represents the targeted deviation of the DPLL output from its center frequency (delta frequency). Depending on the SWF bit in the DPLLCR register, the deviation will be met immediately or after programmed filter response and phase alignment speed (phase slope) time. When the SWE bit in the DPLLCR register is low or the DPLL is not in freerun mode, these bits are ignored. Defined in same units as CFN in the 2's complement format.

Note: examples of programming:
if +10 ppm is desired output frequency, the SDF14-0 should be: CFN x 0.00001 = 440 = $01B8_H$
if -10 ppm is desired output frequency, the SDF14-0 should be: CFN x (-0.00001) = -440 = $7E48_H$

Table 33 - Software Delta Frequency Register (SWDFR) Bits

External Read Only Address: 0045_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FOF 14	FOF 13	FOF 12	FOF 11	FOF 10	FOF 9	FOF 8	FOF 7	FOF 6	FOF 5	FOF 4	FOF 3	FOF 2	FOF 1	FOF 0

Bit	Name	Description
15	Unused	**Reserved.** In normal functional mode, this bit is zero.
14 - 0	FOF14 - 0	**Frequency Offset Bits:** The binary value of these bits represents the current deviation of the DPLL output from its center frequency. Defined in same units as CFN in the 2's complement format. In the software fast mode these bits do not represent frequency offset since the internal filter and phase alignment speed (phase slope) limiter are not used.

Note 1: Output frequency offset, relative to master clock, will be represented as the following:
+10 ppm: CFN x 0.00001 = 440 = $01B8_H$
-10 ppm: CFN x (-0.00001) = -440 = $7E48_H$

Table 34 - Frequency Offset Register (FOR) Bits - Read Only

External Read/Write Address: 0046_H
Reset Value: 0370_H (see Note)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	FLR 13	FLR 12	FLR 11	FLR 10	FLR 9	FLR 8	FLR 7	FLR 6	FLR 5	FLR 4	FLR 3	FLR 2	FLR 1	FLR 0

Bit	Name	Description
15 - 14	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
13 - 0	FLR13 - 0	**Frequency Lock Range Bits:** If not in limiter bypass mode, the binary value of these bits defines the maximum allowed deviation of the DPLL output from its center frequency. If the DPLL limiter bypass is set in the Bandwidth Control Register, the DPLL output frequency can exceed the value specified by these bits, since the proportional value of reference-to-feedback difference is predominant to the integration value in that case. Defined in same units as CFN (unsigned).

Note: The default value is ±20 ppm ('h0370/CFN = 20 ppm).

Table 35 - Frequency Locking Range Register (FLRR) Bits

External Read/Write Address: 0047_H
Reset Value: $000F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LDT 15	LDT 14	LDT 13	LDT 12	LDT 11	LDT 10	LDT 9	LDT 8	LDT 7	LDT 6	LDT 5	LDT 4	LDT 3	LDT 2	LDT 1	LDT 0

Bit	Name	Description
15 - 0	LDT15 - 0	**Lock Detect Threshold Bits:** The binary value of these bits defines the upper limit of the absolute phase from the phase detector output for lock detection. When the value of the absolute phase is less than or equal to LDT for duration of time defined by the LDIR register, the DPLL locks. When the value of the absolute phase is greater than LDT for duration of time defined by the LDIR register divided by 256, the DPLL does not lock.

Note: LDT should be calculated as per the maximum expected amplitude of jitter on the active input reference using the following formula:

$$LDT = \frac{\underline{MAX\_EXP\_JITTER\ (ns)}}{15.2\ (ns)} \times 2$$

Example: If maximum expected jitter amplitude on 2.048 MHz reference is 10UI (i.e., 10 x 488.2 ns = 4882 ns) (assuming the jitter frequency where DPLL attenuation is big), the LDT should be programmed to be (4882/15.2) x 2 = 642 = 0282_H

Table 36 - Lock Detector Threshold Register (LDTR) Bits

External Read/Write Address: 0048_H
Reset Value: $2C00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LDI 15	LDI 14	LDI 13	LDI 12	LDI 11	LDI 10	LDI 9	LDI 8	LDI 7	LDI 6	LDI 5	LDI 4	LDI 3	LDI 2	LDI 1	LDI 0

Bit	Name	Description
15 - 0	LDI15 - 0	**Lock Detector Interval Bits:** The binary value of these bits defines the time interval that the output phase detector must be below the lock detect threshold to declare lock. Unsigned representation of the LDI bits is defined in 4ms intervals.

Table 37 - Lock Detector Interval Register (LDIR) Bits

External Read/Write Address: 0049_H
Reset Value: $099F_H$ (see Note)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	SRL 12	SRL 11	SRL 10	SRL 9	SRL 8	SRL 7	SRL 6	SRL 5	SRL 4	SRL 3	SRL 2	SRL 1	SRL 0

Bit	Name	Description
15 - 13	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
12 - 0	SRL12 - 0	**Slew Rate Limit Bits:** The binary value of these bits defines the maximum rate of DPLL phase change (phase slope), where the phase represents difference between the input reference and output feedback clock. Defined in same units as CFN (unsigned).

Note: The default value is ±56 ppm (’h099F/CFN = 56 ppm).

Table 38 - Slew Rate Limit Register (SRLR) Bits

External Read/Write Address: $004A_H$
Reset Value: 0002_H (see Note)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	BLM	FLF_ QS	FLC 3	FLC 2	FLC 1	FLC 0	FFL 3	FFL 2	FFL 1	FFL 0	LPF 3	LPF 2	LPF 1	LPF 0

Bit	Name	Description
15 - 14	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
13	BLM	**Bypass Limiter Bit:** When this bit is high, the DPLL slew rate limiter is bypassed (ignored). In combination with FLF_QS, FLC3 - 0, FFL3 - 0 and LPF3 - 0 bits, causes fast locking of the DPLL output clocks to the selected reference. When this bit is low, the DPLL performs normal lock following the slew rate limit defined in the slew rate limit register (SRLR).
12	FLF_QS	**Fast Lock Frequency Quick Stabilization Bit:** This bit is used to control speed of internal frequency stabilization. When this bit is high, the DPLL internal frequency will quickly stabilize to the appropriate value, allowing very fast storage of holdover frequency value. When this bit is low, the internal frequency value will be reached over normal locking time (i.e. <100 seconds), and some extra jitter on output clocks can be expected. It is recommended to set this bit if fast locking functionality is desired. When the BLM bit is low, this bit is ignored.
11 - 8	FLC3 - 0	**Fast Lock Control Bits:** Value of these bits (unsigned) control stability of frequency when FFL3 - 0 bits of this register are used. Larger values result in faster locking and are recommended for reference clocks with small jitter, while smaller values are recommended for references with presence of significant jitter.

Table 39 - Bandwidth Control Register (BWCR) Bits

External Read/Write Address: 004A$_H$
Reset Value: 0002$_H$ (see Note)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	BLM	FLF_QS	FLC 3	FLC 2	FLC 1	FLC 0	FFL 3	FFL 2	FFL 1	FFL 0	LPF 3	LPF 2	LPF 1	LPF 0

Bit	Name	Description
7 - 4	FFL3 - 0	**Fast Frequency Lock Bits:** When the BLM bit in this register is high or when SM_FST bit in the DPLLCR register is high, value of these bits (unsigned) represents fast locking speed of the DPLL output clocks to the active input reference. The value also represents speed grade that internal frequency value, used in holdover mode, reaches the DPLL output frequency. The bigger the value, the faster the locking. When both the BLM and the SM_FST bits are low, these bits are ignored.
3 - 0	LPF3 - 0	**Low Pass Filter Control Bits:** Define the DPLL low pass filter corner frequency.

LPF3	LPF2	LPF1	LPF0	CORNER FREQUENCY OF DPLL FILTER
0	0	0	0	0.47 Hz
0	0	0	1	0.95 Hz
0	0	1	0	1.9 Hz
0	0	1	1	3.8 Hz
0	1	0	0	7.6 Hz
0	1	0	1	15.2 Hz
0	1	1	0	30.4 Hz
0	1	1	1	60.7 Hz
1	0	0	0	121 Hz
1	0	0	1	243 Hz
1	0	1	0	486 Hz
1	0	1	1	971Hz
1	1	0	0	1.94 kHz
1	1	0	1	3.88 kHz
1	1	1	0	7.77 kHz
1	1	1	1	15.54 kHz

Note 1: The default corner frequency (-3 dB point) of the low pass filter is 1.9 Hz.

Note 2: To set fast lock mode, it is recommended to program the register bits as follows:
LPF3-0 ->’h8, unless a specific filter response (low pass filter characteristic) is required
FFL3-0 ->’hF
FLC3-0 ->’hF, if significant amount of jitter is not present on the active reference input
FLF_QS -> 1
BLM -> 1

Note 3: In fast lock mode, it is important that the device is not also in freerun mode (see the RCCR Register). Otherwise, the output frame pulse may not be generated correctly.

Note 4: If the selected reference is 8 kHz, LPF3 - 0 should not be chosen to have corner frequency higher than 1/10 of the carrier frequency, or 800Hz (i.e. bits LPF3 - 0 should have a value equal to or smaller than 1010).

Note 5: When the FFL3 - 0 bits are used in normal locking mode (when the BLM bit is not set and the SM_FST bit in the DPLLCR register is set), the DPLL locking time increases as the unsigned binary representation of FFL3 - 0 value increases, maintaining given phase alignment speed (phase slope). The DPLL peaking, which is limited by some standards, increases as well, so the FFL3 - 0 must be chosen with respect to given standard requirements.

Table 39 - Bandwidth Control Register (BWCR) Bits (continued)

External Read/Write Address: $004B_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	MTR	PRS 1	PRS 0	PMS 2	PMS 1	PMS 0	FDM 1	FDM 0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 8</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>7</td><td>MTR</td><td>MTIE Reset: When this bit is low, the MTIE circuit applies a phase offset between the reference input clock and the DPLL output clock and the phase offset value is maintained. When this bit is high, MTIE circuit is in its reset state and the phase offset value is reset to zero, causing alignment of the DPLL output clocks to nearest edge of the selected input reference.</td></tr>
<tr><td>6 - 5</td><td>PRS1 - 0</td><td>Preferred Reference Selection Bits: These bits select the preferred reference from one of the input references They are used only if the PMS2-0 bits are set to 001. Otherwise, these bits are ignored.
<table>
<tr><th>PRS1</th><th>PRS0</th><th>PREFERRED REFERENCE SELECTION</th></tr>
<tr><td>0</td><td>0</td><td>REF0</td></tr>
<tr><td>0</td><td>1</td><td>REF1</td></tr>
<tr><td>1</td><td>0</td><td>REF2</td></tr>
<tr><td>1</td><td>1</td><td>REF3</td></tr>
</table></td></tr>
<tr><td>4 - 2</td><td>PMS2 - 0</td><td>Preference Mode Selection Bits: These bits select one of the preference modes:
<table>
<tr><th>PMS2</th><th>PMS1</th><th>PMS0</th><th>PREFERENCE MODE</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No Preference</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Preference as per the setting of the PRS1 - 0 bits</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Force REF0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Force REF1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Force REF2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Force REF3</td></tr>
<tr><td colspan="3">110 - 111</td><td>Reserved</td></tr>
</table>
If in automatic mode with a preferred reference (PMS2-0 = 001 and FDM1-0 = 00), the automatic state machine will only switch between two references (as per Table 8). Please see Section 12.1.3.2, “Automatic Reference Switching With Preference“ on page 41 for more details.</td></tr>
</table>

Table 40 - Reference Change Control Register (RCCR) Bits

External Read/Write Address: $004B_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	MTR	PRS 1	PRS 0	PMS 2	PMS 1	PMS 0	FDM 1	FDM 0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>1 - 0</td><td>FDM1 - 0</td><td>Force DPLL Timing Mode: These bits force the DPLL into one of the valid timing modes.
In freerun mode, it is important that the DPLL is not also in fast lock mode (see the BWCR register). Otherwise, the output frame pulses may not be generated correctly.
<table>
<tr><th>FDM1</th><th>FDM0</th><th>DPLL TIMING MODE</th></tr>
<tr><td>0</td><td>0</td><td>Automatic</td></tr>
<tr><td>0</td><td>1</td><td>Normal</td></tr>
<tr><td>1</td><td>0</td><td>Holdover</td></tr>
<tr><td>1</td><td>1</td><td>Freerun</td></tr>
</table>
</td></tr>
</table>

Table 40 - Reference Change Control Register (RCCR) Bits (continued)

External Read Only Address: 004C$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SLM	LST	RFR2	RFR1	RFR0	RES1	RES0	DPM1	DPM0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 9</td><td>Unused</td><td>Reserved. In normal functional mode, these bits are zero.</td></tr>
<tr><td>8</td><td>SLM</td><td>Slew Rate Limiter Status Bit: If the device sets this bit to high, the DPLL phase difference between the input and output clocks is changing at the slew rate limit defined in the Slew Rate Limit Register (SRLR).</td></tr>
<tr><td>7</td><td>LST</td><td>Lock Status Bit: If the device sets this bit to high, while the LDTR and LDIR registers are programmed properly, the DPLL output clocks are locked to the selected input reference. If this bit is low, the DPLL output clocks are not yet locked to the selected input reference.</td></tr>
<tr><td>6 - 4</td><td>RFR2 - 0</td><td>Reference Frequency Indicator Bits: These bits represent the frequency of the selected reference indicated by the reference bits (RES1 - 0) in this register.
<table>
<tr><th>RFR2</th><th>RFR1</th><th>RFR0</th><th>Frequency of the Selected Reference</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.544 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2.048 MHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4.096 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8.192 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16.384 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>19.44 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3 - 2</td><td>RES1 - 0</td><td>Reference Select Indicator Bits: These bits indicate which one of the four reference inputs (REF0 - 3 pins) is being selected by the device.
<table>
<tr><th>RES1</th><th>RES0</th><th>Input Reference in use</th></tr>
<tr><td>0</td><td>0</td><td>REF 0</td></tr>
<tr><td>0</td><td>1</td><td>REF 1</td></tr>
<tr><td>1</td><td>0</td><td>REF 2</td></tr>
<tr><td>1</td><td>1</td><td>REF 3</td></tr>
</table></td></tr>
</table>

Table 41 - Reference Change Status Register (RCSR) Bits - Read Only

External Read Only Address: 004C$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SLM	LST	RFR2	RFR1	RFR0	RES1	RES0	DPM1	DPM0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>1 - 0</td><td>DPM1 - 0</td><td>DPLL Timing Mode Status Bits: These bits indicate the DPLL’s timing mode status.
<table>
<tr><td>DPM1</td><td>DPM0</td><td>DPLL Timing Mode State</td></tr>
<tr><td>0</td><td>0</td><td>MTIE</td></tr>
<tr><td>0</td><td>1</td><td>Normal</td></tr>
<tr><td>1</td><td>0</td><td>Holdover</td></tr>
<tr><td>1</td><td>1</td><td>Freerun</td></tr>
</table>
</td></tr>
</table>

Table 41 - Reference Change Status Register (RCSR) Bits - Read Only (continued)

External Read/Write Address: 004E$_H$
Reset Value: A346$_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MNU 15	MNU 14	MNU 13	MNU 12	MNU 11	MNU 10	MNU 9	MNU 8	MNU 7	MNU 6	MNU 5	MNU 4	MNU 3	MNU 2	MNU 1	MNU 0

Bit	Name	Description
15 - 0	MNU15 - 0	**Multiple-Period Near Upper Limit Bits:** Total binary value of these bits and the MPNULRU register bits defines the near upper limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents near upper limit for all reference frequencies, which is +9.913 ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’upper’ is based on frequency.

Table 42 - Multi-period Near Upper Limit Register - Lower 16 Bits (MPNULRL)

External Read/Write Address: $004F_H$
Reset Value: $3B9A_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MNU 31	MNU 30	MNU 29	MNU 28	MNU 27	MNU 26	MNU 25	MNU 24	MNU 23	MNU 22	MNU 21	MNU 20	MNU 19	MNU 18	MNU 17	MNU 16

Bit	Name	Description
15 - 0	MNU31 - 16	**Multiple-Period Near Upper Limit Bits:** Total binary value of these bits and the MPNULRL register bits defines the near upper limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents near upper limit for all reference frequencies, which is +9.913 ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’upper’ is based on frequency.

Table 43 - Multi-period Near Upper Limit Register - Upper 16 Bits (MPNULRU)

External Read/Write Address: 0050_H
Reset Value: $9DE8_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFU 15	MFU 14	MFU 13	MFU 12	MFU 11	MFU 10	MFU 9	MFU 8	MFU 7	MFU 6	MFU 5	MFU 4	MFU 3	MFU 2	MFU 1	MFU 0

Bit	Name	Description
15 - 0	MFU15 - 0	**Multiple-Period Far Upper Limit Bits:** Total binary value of these bits and the MPFULRU register bits defines the far upper limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents far upper limit for all reference frequencies, which is +11.287 ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’upper’ is based on frequency.

Table 44 - Multi-period Far Upper Limit Register - Lower 16 Bits (MPFULRL)

External Read/Write Address: 0051_H
Reset Value: $3B9A_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFU 31	MFU 30	MFU 29	MFU 28	MFU 27	MFU 26	MFU 25	MFU 24	MFU 23	MFU 22	MFU 21	MFU 20	MFU 19	MFU 18	MFU 17	MFU 16

Bit	Name	Description
15 - 0	MFU31 - 16	**Multiple-Period Far Upper Limit Bits:** Total binary value of these bits and the MPFULRL register bits defines the far upper limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents far upper limit for all reference frequencies, which is +11.287 ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’upper’ is based on frequency.

Table 45 - Multi-period Far Upper Limit Register - Upper 16 Bits (MPFULRU)

External Read/Write Address: 0052_H
Reset Value:$F0B8_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MNL 15	MNL 14	MNL 13	MNL 12	MNL 11	MNL 10	MNL 9	MNL 8	MNL 7	MNL 6	MNL 5	MNL 4	MNL 3	MNL 2	MNL 1	MNL 0

Bit	Name	Description
15 - 0	MNL15 - 0	**Multiple-Period Near Lower Limit Bits:** Total binary value of these bits and the MPNLLRU register bits defines the near lower limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents near lower limit for all reference frequencies, which is -9.913ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’lower’ is based on frequency.

Table 46 - Multi-period Near Lower Limit Register - Lower 16 Bits (MPNLLRL)

External Read/Write Address: 0053_H
Reset Value: $3B9A_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MNL 31	MNL 30	MNL 29	MNL 28	MNL 27	MNL 26	MNL 25	MNL 24	MNL 23	MNL 22	MNL 21	MNL 20	MNL 19	MNL 18	MNL 17	MNL 16

Bit	Name	Description
15 - 0	MNL31 - 16	**Multiple-Period Near Lower Limit Bits:** Total binary value of these bits and the MPNLLRL register bits defines the near lower limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents near lower limit for all reference frequencies, which is -9.913ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’lower’ is based on frequency.

Table 47 - Multi-period Near Lower Limit Register - Upper 16 Bits (MPNLLRU)

External Read/Write Address: 0054_H
Reset Value: $F616_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFL 15	MFL 14	MFL 13	MFL 12	MFL 11	MFL 10	MFL 9	MFL 8	MFL 7	MFL 6	MFL 5	MFL 4	MFL 3	MFL 2	MFL 1	MFL 0

Bit	Name	Description
15 - 0	MFL15 - 0	**Multiple-Period Far Lower Limit Bits:** Total binary value of these bits and the MPFLLRU register bits defines the far lower limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents far lower limit for all reference frequencies, which is -11.287ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’lower’ is based on frequency.

Table 48 - Multi-period Far Lower Limit Register - Lower 16 Bits (MPFLLRL)

External Read/Write Address: 0055_H
Reset Value: $3B9A_H$ (Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFL 31	MFL 30	MFL 29	MFL 28	MFL 27	MFL 26	MFL 25	MFL 24	MFL 23	MFL 22	MFL 21	MFL 20	MFL 19	MFL 18	MFL 17	MFL 16

Bit	Name	Description
15 - 0	MFL31 - 16	**Multiple-Period Far Lower Limit Bits:** Total binary value of these bits and the MPFLLRL register bits defines the far lower limit for the multiple period count of any reference input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents far lower limit for all reference frequencies, which is -11.287ppm (Stratum 3 compliant value), regardless of the reference frequency.

Note 2: The name ’lower’ is based on frequency.

Table 49 - Multi-period Far Lower Limit Register - Upper 16 Bits (MPFLLRU)

External Read/Write Addresses: 0056_H, $005A_H$, $005E_H$, 0062_H
Reset Value: $387F_H$ (see Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC[n] 15	MC[n] 14	MC[n] 13	MC[n] 12	MC[n] 11	MC[n] 10	MC[n] 9	MC[n] 8	MC[n] 7	MC[n] 6	MC[n] 5	MC[n] 4	MC[n] 3	MC[n] 2	MC[n] 1	MC[n] 0

Bit	Name	Description
15 - 0	MC[n]15 - 0 (n = 0 - 3)	**Reference n Multi-period Count Bits:** Total binary value of these bits and the RnMPCRU register bits defines the number of reference clock periods to be measured for the multi-period frequency check for the REFn input monitoring, **minus 1**.

Note 1: The default value represents lower bits of multi-period count for 8 kHz input frequency, calculated to have 10 seconds observation time.

Note 2: When the MRLE bit of DPLLCR register is low, these registers are ignored. Depending on reference frequency (detected or programmed through the Reference Frequency Register), the following values are used instead:
’h387F - if reference frequency is 8 kHz
’h987F - if reference frequency is 1.544 MHz
’h7FFF - if reference frequency is 2.048 MHz
’hFFFF - if reference frequency is 4.096 MHz, 8.192 MHz or16.384 MHz
’h4EFF - if reference frequency is 19.44 MHz

Table 50 - Multi-period Count Register - Lower 16 Bits (RnMPCRL) Bits, (n = 0 - 3)

External Read/Write Addresses: 0057$_H$, 005B$_H$, 005F$_H$, 0063$_H$
Reset Value: 0001$_H$ (see Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC[n] 31	MC[n] 30	MC[n] 29	MC[n] 28	MC[n] 27	MC[n] 26	MC[n] 25	MC[n] 24	MC[n] 23	MC[n] 22	MC[n] 21	MC[n] 20	MC[n] 19	MC[n] 18	MC[n] 17	MC[n] 16

Bit	Name	Description
15 - 0	MC[n]31 - 16 (n = 0 - 3)	**Reference n Multi-period Count Bits:** Total binary value of these bits and the RnMPCRL register bits defines the number of reference clock periods to be measured for the multi-period frequency check for the REFn input monitoring, **minus 1**.

Note 1: The default value represents lower bits of multi-period count for 8 kHz input frequency, calculated to have 10 seconds observation time.

Note 2: When the MRLE bit of DPLLCR register is low, these registers are ignored. Depending on reference frequency (detected or programmed through the Reference Frequency Register), the following values are used instead:
’h0001 - if reference frequency is 8 kHz
’h00EB - if reference frequency is 1.544 MHz
’h0138 - if reference frequency is 2.048 MHz
’h0270 - if reference frequency is 4.096 MHz
’h04E1 - if reference frequency is 8.192 MHz
’h09C3 - if reference frequency is 16.384 MHz
’h0B96 - if reference frequency is 19.44 MHz

Table 51 - Multi-period Count Register - Upper 16 Bits (RnMPCRU) Bits, (n = 0 - 3)

External Read/Write Addresses: 0058_H, $005C_H$, 0060_H, 0064_H
Reset Value: $2E4A_H$ (see Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UL[n] 15	UL[n] 14	UL[n] 13	UL[n] 12	UL[n] 11	UL[n] 10	UL[n] 9	UL[n] 8	UL[n] 7	UL[n] 6	UL[n] 5	UL[n] 4	UL[n] 3	UL[n] 2	UL[n] 1	UL[n] 0

Bit	Name	Description
15 - 0	UL[n]15 - 0 (n = 0 - 3)	**Reference n Single Period Upper Limit Bits:** The binary value of these bits defines the upper limit for the period of the REFn input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents limit for 8 kHz input frequency, which is +6.4 µs (+10UI_{p-p} of 1.544 MHz).

Note 2: When the MRLE bit of DPLLCR register is low, these registers are ignored. Depending on reference frequency (detected or programmed through the Reference Frequency Register), the following values are used instead:
’h2E4A (10UIp-p of 1.544 MHz i.e. 6.4 µs) - if reference frequency is 8 kHz
’h002B (0.3UIp-p) - if reference frequency is 1.544 MHz
’h0025 (0.2UIp-p) - if reference frequency is 2.048 MHz
’h0011 (0.2UIp-p) - if reference frequency is 4.096 MHz
’h0007 (0.2UIp-p) - if reference frequency is 8.192 MHz
’h0002 (0.2UIp-p) - if reference frequency is 16.384 MHz
’h0002 (0.2UIp-p) - if reference frequency is 19.44 MHz

Note 3: The name ‘upper’ is based on frequency.

Table 52 - Upper Limit Register (RnULR) Bits, (n = 0 - 3)

External Read/Write Addresses: 0059$_H$, 005D$_H$, 0061$_H$, 0065$_H$
Reset Value: 335C$_H$ (see Note 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LL[n] 15	LL[n] 14	LL[n] 13	LL[n] 12	LL[n] 11	LL[n] 10	LL[n] 9	LL[n] 8	LL[n] 7	LL[n] 6	LL[n] 5	LL[n] 4	LL[n] 3	LL[n] 2	LL[n] 1	LL[n] 0

Bit	Name	Description
15 - 0	LL[n]15 - 0 (n = 0 to 3)	**Reference n Single Period Lower Limit Bits:** The binary value of these bits defines the lower limit for the period of the REFn input, **minus 1**. The unit of the binary value is measured in 100 MHz clock periods.

Note 1: The default value represents limit for 8 kHz input frequency, which is -6.4 µs (-10UI$_{p-p}$ of 1.544 MHz).

Note 2: When the MRLE bit of DPLLCR register is low, these registers are ignored. Depending on reference frequency (detected or programmed through the Reference Frequency Register), the following values are used instead:
’h335C (10UIp-p of 1.544 MHz i.e. 6.4 µs) - if reference frequency is 8 kHz
’h0055 (0.3UIp-p) - if reference frequency is 1.544 MHz
’h003B (0.2UIp-p) - if reference frequency is 2.048 MHz
’h001E (0.2UIp-p) - if reference frequency is 4.096 MHz
’h000F (0.2UIp-p) - if reference frequency is 8.192 MHz
’h0008 (0.2UIp-p) - if reference frequency is 16.384 MHz
’h0007 (0.2UIp-p) - if reference frequency is 19.44 MHz

Note 3: The name ‘lower’ is based on frequency.

Table 53 - Lower Limit Register (RnLLR) Bits, (n = 0 - 3)

External Read Only Address: 0066_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	LCI	RCI	HOI	SLI

Bit	Name	Description
15 - 4	Unused	**Reserved.** In normal functional mode, these bits is zero.
3	LCI	**Lock Change Interrupt Bit:** If the device sets this bit to high, the device lock status has changed.
2	RCI	**Reference Change Interrupt Bit:** If the device sets this bit to high, the selected reference has changed.
1	HOI	**Holdover Interrupt Bit:** If the device sets this bit to high, the device has entered or recovered from the holdover/MTIE mode.
0	SLI	**Slew Rate Limit Interrupt Bit:** If the device sets this bit to high, the device phase status has changed from perspective of changing at the slew rate limit.

Note 1: If any of these bits are set, the interrupt output will become active unless the Interrupt Mask Register (IMR) has a high value for that particular bit.

Note 2: Any of these bits can be cleared by setting the appropriate bit in the Interrupt Clear Register.

Table 54 - Interrupt Register (IR) Bits - Read Only

External Read/Write Address: 0067_H
Reset Value: $000F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	LIM	RIM	HIM	SIM

Bit	Name	Description
15 - 4	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
3	LIM	**Lock Interrupt Mask Bit:** When this bit is high, it masks the lock status change interrupt.
2	RIM	**Reference Change Interrupt Mask Bit:** When this bit is high, it masks the reference change interrupt.
1	HIM	**Holdover Interrupt Mask Bit:** When this bit is high, it masks the holdover entry/exit interrupt.
0	SIM	**Slew Rate Limiter Interrupt Mask Bit:** When this bit is high, it masks the slew rate interrupt.

Table 55 - Interrupt Mask Register (IMR) Bits

External Read/Write Address: 0068_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	ICB 3	ICB 2	ICB 1	ICB 0

Bit	Name	Description
15 - 4	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
3 - 0	ICB3 - 0	**Interrupt Clear Bits:** Writing a “1” to any bit in this register will clear the corresponding bit in the Interrupt Register (IR). The Interrupt Clear Register is self-clearing, i.e. once it has completed its action, the ICR register bit returns to 0.

Table 56 - Interrupt Clear Register (ICR) Bits

External Read Only Address: 0069_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3 FML	R3 FMU	R3 FL	R3 FU	R2 FML	R2 FMU	R2 FL	R2 FU	R1 FML	R1 FMU	R1 FL	R1 FU	R0 FML	R0 FMU	R0 FL	R0 FU

Bit	Name	Description
15	R3FML	**Reference 3 Multi-period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF3 fails the multi-period lower limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
14	R3FMU	**Reference 3 Multi-period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF3 fails the multi-period upper limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
13	R3FL	**Reference 3 Single Period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF3 fails the single-period lower limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
12	R3FU	**Reference 3 Single Period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF3 fails the single-period upper limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
11	R2FML	**Reference 2 Multi-period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF2 fails the multi-period lower limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
10	R2FMU	**Reference 2 Multi-period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF2 fails the multi-period upper limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
9	R2FL	**Reference 2 Single Period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF2 fails the single-period lower limit check. (see Table 11, “Values for Single Period Limits” on page 46)
8	R2FU	**Reference 2 Single Period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF2 fails the single-period upper limit check. (see Table 11, “Values for Single Period Limits” on page 46)
7	R1FML	**Reference 1 Multi-period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF1 fails the multi-period lower limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)

Table 57 - Reference Failure Status Register (RSR) Bits - Read Only

External Read Only Address: 0069$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3 FML	R3 FMU	R3 FL	R3 FU	R2 FML	R2 FMU	R2 FL	R2 FU	R1 FML	R1 FMU	R1 FL	R1 FU	R0 FML	R0 FMU	R0 FL	R0 FU

Bit	Name	Description
6	R1FMU	**Reference 1 Multi-period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF1 fails the multi-period upper limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
5	R1FL	**Reference 1 Single Period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF1 fails the single-period lower limit check. (see Table 11, “Values for Single Period Limits” on page 46)
4	R1FU	**Reference 1 Single Period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF1 fails the single-period upper limit check. (see Table 11, “Values for Single Period Limits” on page 46)
3	R0FML	**Reference 0 Multi-period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF0 fails the multi-period lower limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
2	R0FMU	**Reference 0 Multi-period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF0 fails the multi-period upper limit check. (see Table 13, “Multi-period Hysteresis Limits” on page 48)
1	R0FL	**Reference 0 Single Period Lower Limit Fail Bit:** If the device sets this bit to high, the input REF0 fails the single-period lower limit check. (see Table 11, “Values for Single Period Limits” on page 46)
0	R0FU	**Reference 0 Single Period Upper Limit Fail Bit:** If the device sets this bit to high, the input REF0 fails the single-period upper limit check. (see Table 11, “Values for Single Period Limits” on page 46)

Table 57 - Reference Failure Status Register (RSR) Bits - Read Only (continued)

External Read/Write Address: 006A$_H$
Reset Value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3 MML	R3 MMU	R3 ML	R3 MU	R2 MML	R2 MMU	R2 ML	R2 MU	R1 MML	R1 MMU	R1 ML	R1 MU	R0 MML	R0 MMU	R0 ML	R0 MU

Bit	Name	Description
15	R3MML	**Reference 3 Multi-period Lower Limit Mask Bit:** When this bit is high, it masks the multi-period lower limit check (or forces pass) for REF3.

Table 58 - Reference Mask Register (RMR) Bits

External Read/Write Address: 006A$_H$
Reset Value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3 MML	R3 MMU	R3 ML	R3 MU	R2 MML	R2 MMU	R2 ML	R2 MU	R1 MML	R1 MMU	R1 ML	R1 MU	R0 MML	R0 MMU	R0 ML	R0 MU

Bit	Name	Description
14	R3MMU	**Reference 3 Multi-period Upper Limit Mask Bit:** When this bit is high, it masks the multi-period upper limit check (or forces pass) for REF3.
13	R3ML	**Reference 3 Single-period Lower Limit Mask Bit:** When this bit is high, it masks the single-period lower limit check (or forces pass) for REF3.
12	R3MU	**Reference 3 Single-period Upper Limit Mask Bit:** When this bit is high, it masks the single-period upper limit check (or forces pass) for REF3.
11	R2MML	**Reference 2 Multi-period Lower Limit Mask Bit:** When this bit is high, it masks the multi-period lower limit check (or forces pass) for REF2.
10	R2MMU	**Reference 2 Multi-period Upper Limit Mask Bit:** When this bit is high, it masks the multi-period upper limit check (or forces pass) for REF2.
9	R2ML	**Reference 2 Single-period Lower Limit Mask Bit:** When this bit is high, it masks the single-period lower limit check (or forces pass) for REF2.
8	R2MU	**Reference 2 Single-period Upper Limit Mask Bit:** When this bit is high, it masks the single-period upper limit check (or forces pass) for REF2.
7	R1MML	**Reference 1 Multi-period Lower Limit Mask Bit:** When this bit is high, it masks the multi-period lower limit check (or forces pass) for REF1.
6	R1MMU	**Reference 1 Multi-period Upper Limit Mask Bit:** When this bit is high, it masks the multi-period upper limit check (or forces pass) for REF1.
5	R1ML	**Reference 1 Single-period Lower Limit Mask Bit:** When this bit is high, it masks the single-period lower limit check (or forces pass) for REF1.
4	R1MU	**Reference 1 Single-period Upper Limit Mask Bit:** When this bit is high, it masks the single-period upper limit check (or forces pass) for REF1.
3	R0MML	**Reference 0 Multi-period Lower Limit Mask Bit:** When this bit is high, it masks the multi-period lower limit check (or forces pass) for REF0.
2	R0MMU	**Reference 0 Multi-period Upper Limit Mask Bit:** When this bit is high, it masks the multi-period upper limit check (or forces pass) for REF0.
1	R0ML	**Reference 0 Single-period Lower Limit Mask Bit:** When this bit is high, it masks the single-period lower limit check (or forces pass) for REF0.
0	R0MU	**Reference 0 Single-period Upper Limit Mask Bit:** When this bit is high, it masks the single-period upper limit check (or forces pass) for REF0.

Table 58 - Reference Mask Register (RMR) Bits (continued)

<table>
<tr><td colspan="3">External Read Only Address: 006B_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	R3FS2	R3FS1	R3FS0	R2FS2	R2FS1	R2FS0	R1FS2	R1FS1	R1FS0	R0FS2	R0FS1	R0FS0
</td></tr>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 12</td><td>Unused</td><td>Reserved. In normal functional mode, these bits are zero.</td></tr>
<tr><td>11 - 9</td><td>R3FS2 - 0</td><td>Reference 3 Frequency Status Bits: These bits report detected frequency of REF3.
<table>
<tr><th>R3FS2</th><th>R3FS1</th><th>R3FS0</th><th>REF3 Frequency Measurement</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.544 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2.048 MHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4.096 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8.192 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16.384 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>19.44 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>8 - 6</td><td>R2FS2 - 0</td><td>Reference 2 Frequency Status Bits: These bits report detected frequency of REF2.
<table>
<tr><th>R2FS2</th><th>R2FS1</th><th>R2FS0</th><th>REF 2 Frequency Measurement</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.544 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2.048 MHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4.096 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>8.192 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16.384 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>19.44 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

Table 59 - Reference Frequency Status Register (RFSR) Bits - Read only

External Read Only Address: $006B_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	R3FS 2	R3FS 1	R3FS 0	R2FS 2	R2FS 1	R2FS 0	R1FS 2	R1FS 1	R1FS 0	R0FS 2	R0FS 1	R0FS 0

Bit	Name	Description
5 - 3	R1FS2 - 0	**Reference 1 Frequency Status Bits:** These bits report detected frequency of REF1.
2 - 0	R0FS2 - 0	**Reference 0 Frequency Status Bits:** These bits report detected frequency of REF0.

R1FS2	R1FS1	R1FS0	REF1 Frequency Measurement
0	0	0	8 kHz
0	0	1	1.544 MHz
0	1	0	2.048 MHz
0	1	1	4.096 MHz
1	0	0	8.192 MHz
1	0	1	16.384 MHz
1	1	0	19.44 MHz
1	1	1	Reserved

R0FS2	R0FS1	R0FS0	REF0 Frequency Measurement
0	0	0	8 kHz
0	0	1	1.544 MHz
0	1	0	2.048 MHz
0	1	1	4.096 MHz
1	0	0	8.192 MHz
1	0	1	16.384 MHz
1	1	0	19.44 MHz
1	1	1	Reserved

Table 59 - Reference Frequency Status Register (RFSR) Bits - Read only (continued)

External Read/Write Address: $006C_H$
Reset Value: 0002_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	OJP2	OJP1	OJP0

Bit	Name	Description
15 - 3	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
2 - 0	OJP2 - 0	**Output Jitter Performance Bits:** These bits are used to control the DPLL output jitter performance with respect to the noise received through the output pins. The higher value (unsigned) means more filtering, while zero means filter bypass. The default value of 2_H gives the best performance for most circumstances.

Table 60 - Output Jitter Control Register (OJCR) Bits

External Read/Write Address: 0100_H - $011F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIN[n] BD2	STIN[n] BD1	STIN[n] BD0	STIN[n] SMP1	STIN[n] SMP0	STIN[n] DR3	STIN[n] DR2	STIN[n] DR1	STIN[n] DR0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 9</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>8 - 6</td><td>STIN[n]BD2 - 0</td><td>Input Stream[n] Bit Delay Bits.
The binary value of these bits refers to the number of bits that the input stream will be delayed relative to FPi. The maximum value is 7. Zero means no delay.</td></tr>
<tr><td>5 - 4</td><td>STIN[n]SMP1 - 0</td><td>Input Data Sampling Point Selection Bits:
<table>
<tr><th>STIN[n]SMP1-0</th><th>Sampling Point (2.048 Mbps, 4.096 Mbps, 8.192 Mbps streams)</th><th>Sampling Point (16.384 Mbps streams)</th></tr>
<tr><td>00</td><td>3/4 point</td><td rowspan="2">2/4 point</td></tr>
<tr><td>01</td><td>1/4 point</td></tr>
<tr><td>10</td><td>2/4 point</td><td rowspan="2">4/4 point</td></tr>
<tr><td>11</td><td>4/4 point</td></tr>
</table>
</td></tr>
</table>

Table 61 - Stream Input Control Register 0 - 31 (SICR0 - 31) BIts

External Read/Write Address: 0100$_H$ - 011F$_H$
Reset Value: 0000$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIN[n] BD2	STIN[n] BD1	STIN[n] BD0	STIN[n] SMP1	STIN[n] SMP0	STIN[n] DR3	STIN[n] DR2	STIN[n] DR1	STIN[n] DR0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>3 - 0</td><td>STIN[n]DR3 - 0</td><td>Input Data Rate Selection Bits:
<table>
<tr><th>STIN[n]DR3-0</th><th>Data Rate</th></tr>
<tr><td>0000</td><td>Stream Unused</td></tr>
<tr><td>0001</td><td>2.048 Mbps</td></tr>
<tr><td>0010</td><td>4.096 Mbps</td></tr>
<tr><td>0011</td><td>8.192 Mbps</td></tr>
<tr><td>0100</td><td>16.384 Mbps</td></tr>
<tr><td>0101 - 1111</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td colspan="3">Note: [n] denotes input stream from 0 - 31.</td></tr>
</table>

Table 61 - Stream Input Control Register 0 - 31 (SICR0 - 31) BIts (continued)

External Read/Write Address: 0120_H - $013F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	STIN[n] Q3C2	STIN[n] Q3C1	STIN[n] Q3C0	STIN[n] Q2C2	STIN[n] Q2C1	STIN[n] Q2C0	STIN[n] Q1C2	STIN[n] Q1C1	STIN[n] Q1C0	STIN[n] Q0C2	STIN[n] Q0C1	STIN[n] Q0C0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 12</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>11 - 9</td><td>STIN[n]Q3C2 - 0</td><td>Quadrant Frame 3 Control Bits. These three bits are used to control STi[n]’s quadrant frame 3, which is defined as Ch24 to 31, Ch48 to 63, Ch96 to 127 and Ch192 to 255 for the 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, and 16.384 Mbps modes respectively.
<table>
<tr><th>STIN[n]Q3C 2-0</th><th>Operation</th></tr>
<tr><td>0xx</td><td>normal operation</td></tr>
<tr><td>100</td><td>LSB of each channel is replaced by “0”</td></tr>
<tr><td>101</td><td>LSB of each channel is replaced by “1”</td></tr>
<tr><td>110</td><td>MSB of each channel is replaced by “0”</td></tr>
<tr><td>111</td><td>MSB of each channel is replaced by “1”</td></tr>
</table></td></tr>
<tr><td>8 - 6</td><td>STIN[n]Q2C2 - 0</td><td>Quadrant Frame 2 Control Bits. These three bits are used to control STi[n]’s quadrant frame 2, which is defined as Ch16 to 23, Ch32 to 47, Ch64 to 95 and Ch128 to 191 for the 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, and 16.384 Mbps modes respectively.
<table>
<tr><th>STIN[n]Q2C 2-0</th><th>Operation</th></tr>
<tr><td>0xx</td><td>normal operation</td></tr>
<tr><td>100</td><td>LSB of each channel is replaced by “0”</td></tr>
<tr><td>101</td><td>LSB of each channel is replaced by “1”</td></tr>
<tr><td>110</td><td>MSB of each channel is replaced by “0”</td></tr>
<tr><td>111</td><td>MSB of each channel is replaced by “1”</td></tr>
</table></td></tr>
</table>

Table 62 - Stream Input Quadrant Frame Register 0 - 31 (SIQFR0 - 31) Bits

External Read/Write Address: 0120_H - $013F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	STIN[n] Q3C2	STIN[n] Q3C1	STIN[n] Q3C0	STIN[n] Q2C2	STIN[n] Q2C1	STIN[n] Q2C0	STIN[n] Q1C2	STIN[n] Q1C1	STIN[n] Q1C0	STIN[n] Q0C2	STIN[n] Q0C1	STIN[n] Q0C0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>5 - 3</td><td>STIN[n]Q1C2 - 0</td><td>Quadrant Frame 1 Control Bits. These three bits are used to control STi[n]’s quadrant frame 1, which is defined as Ch8 to 15, Ch16 to 31, Ch32 to 63 and Ch64 to 127 for the 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, and 16.384 Mbps modes respectively.
<table>
<tr><th>STIN[n]Q1C 2-0</th><th>Operation</th></tr>
<tr><td>0xx</td><td>normal operation</td></tr>
<tr><td>100</td><td>LSB of each channel is replaced by “0”</td></tr>
<tr><td>101</td><td>LSB of each channel is replaced by “1”</td></tr>
<tr><td>110</td><td>MSB of each channel is replaced by “0”</td></tr>
<tr><td>111</td><td>MSB of each channel is replaced by “1”</td></tr>
</table></td></tr>
<tr><td>2 - 0</td><td>STIN[n]Q0C2 - 0</td><td>Quadrant Frame 0 Control Bits. These three bits are used to control STi[n]’s quadrant frame 0, which is defined as Ch0 to 7, Ch0 to 15, Ch0 to 31 and Ch0 to 63 for the 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, and 16.384 Mbps modes respectively.
<table>
<tr><th>STIN[n]Q0C2-0</th><th>Operation</th></tr>
<tr><td>0xx</td><td>normal operation</td></tr>
<tr><td>100</td><td>LSB of each channel is replaced by “0”</td></tr>
<tr><td>101</td><td>LSB of each channel is replaced by “1”</td></tr>
<tr><td>110</td><td>MSB of each channel is replaced by “0”</td></tr>
<tr><td>111</td><td>MSB of each channel is replaced by “1”</td></tr>
</table></td></tr>
<tr><td colspan="3">Note: [n] denotes input stream from 0 - 31.</td></tr>
</table>

Table 62 - Stream Input Quadrant Frame Register 0 - 31 (SIQFR0 - 31) Bits (continued)

External Read/Write Address: 0200_H - $021F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	STOHZ [n]A2	STOHZ [n]A1	STOHZ [n]A0	STO[n] FA1	STO[n] FA0	STO[n] AD2	STO[n] AD1	STO[n] AD0	STO[n] DR3	STO[n] DR2	STO[n] DR1	STO[n] DR0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 12</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>11 - 9</td><td>STOHZ[n]A2 - 0
(Valid only for STio0-15)</td><td>STOHZ Additional Advancement Bits:
<table>
<tr><th>STOHZ[n]A2-0</th><th>Additional Advancement (2.048 Mbps, 4.096 Mbps, 8.192 Mbps)</th><th>Additional Advancement (16.384 Mbps)</th></tr>
<tr><td>000</td><td>0 bit</td><td>0 bit</td></tr>
<tr><td>001</td><td>1/4 bit</td><td>2/4 bit</td></tr>
<tr><td>010</td><td>2/4 bit</td><td>4/4 bit</td></tr>
<tr><td>011</td><td>3/4 bit</td><td rowspan="3">Reserved</td></tr>
<tr><td>100</td><td>4/4 bit</td></tr>
<tr><td>101-111</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>8 - 7</td><td>STO[n]FA1 - 0</td><td>Output Stream[n] Fractional Advancement Bits:
<table>
<tr><th>STO[n]FA1-0</th><th>Advancement (2.048 Mbps, 4.096 Mbps, 8.192 Mbps streams)</th><th>Advancement (16.384 Mbps streams)</th></tr>
<tr><td>00</td><td>0</td><td>0</td></tr>
<tr><td>01</td><td>1/4 bit</td><td>2/4</td></tr>
<tr><td>10</td><td>2/4 bit</td><td rowspan="2">Reserved</td></tr>
<tr><td>11</td><td>3/4 bit</td></tr>
</table></td></tr>
<tr><td>6 - 4</td><td>STO[n]AD2 - 0</td><td>Output Stream[n] Bit Advancement Selection Bits:
The binary value of these bits refers to the number of bits that the output stream is to be advanced relative to FPo. The maximum value is 7. Zero means no advancement.</td></tr>
<tr><td>3 - 0</td><td>STO[n]DR3 - 0</td><td>Output Data Rate Selection Bits:
<table>
<tr><th>STIN[n]DR3 - 0</th><th>Data Rate</th></tr>
<tr><td>0000</td><td>disabled: STio HiZ (STOHZ driven high)</td></tr>
<tr><td>0001</td><td>2.048 Mbps</td></tr>
<tr><td>0010</td><td>4.096 Mbps</td></tr>
<tr><td>0011</td><td>8.192 Mbps</td></tr>
<tr><td>0100</td><td>16.384 Mbps</td></tr>
<tr><td>0101 - 1111</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td colspan="3">Note: [n] denotes output stream from 0 - 31.</td></tr>
</table>

Table 63 - Stream Output Control Register 0 - 31 (SOCR0 - 31) Bits

External Read/Write Address: 0300_H - $031F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ST[n] BRS7	ST[n] BRS6	ST[n] BRS5	ST[n] BRS4	ST[n] BRS3	ST[n] BRS2	ST[n] BRS1	ST[n] BRS0

Bit	Name	Description
15 - 8	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
7 - 0	ST[n] BRS7 - 0	**Stream[n] BER Receive Start Bits:** The binary value of these bits refers to the input channel in which the BER data starts to be compared.

Note: [n] denotes input stream from 0 - 31

Table 64 - BER Receiver Start Register [n] (BRSR[n]) Bits

External Read/Write Address: 0320_H - $033F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ST[n] BL8	ST[n] BL7	ST[n] BL6	ST[n] BL5	ST[n] BL4	ST[n] BL3	ST[n] BL2	ST[n] BL1	ST[n] BL0

Bit	Name	Description
15 - 9	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
8 - 0	ST[n] BL8 - 0	**Stream[n] BER Length Bits:** The binary value of these bits refers to the number of consecutive channels expected to receive the BER pattern. The maximum number of BER channels is 32, 64, 128 and 256 for the data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps and 16.384 Mbps respectively. The minimum number of BER channels is 1. If these bits are set to zero, no BER test will be performed.

Note: [n] denotes input stream from 0 - 31

Table 65 - BER Receiver Length Register [n] (BRLR[n]) Bits

External Read/Write Address: 0340_H - $035F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	ST[n] CBER	ST[n] SBER

Bit	Name	Description
15 - 2	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
1	ST[n] CBER	**Stream[n] Bit Error Rate Counter Clear:** When this bit is high, it resets the internal bit error counter and the stream BER Receiver Error Register to zero.
0	ST[n] SBER	**Stream[n] Bit Error Rate Test Start:** When this bit is high, it enables the BER receiver; starts the bit error rate test. The bit error test result is kept in the BER Receiver Error (BRER[n]) register. Upon the completion of the BER test, set this bit to zero. Note that the RBEREB bit must be set in the IMS Register first.

Note: [n] denotes input stream from 0 - 31

Table 66 - BER Receiver Control Register [n] (BRCR[n]) Bits

External Read Address: 0360_H - $037F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST[n] BC15	ST[n] BC14	ST[n] BC13	ST[n] BC12	ST[n] BC11	ST[n] BC10	ST[n] BC9	ST[n] BC8	ST[n] BC7	ST[n] BC6	ST[n] BC5	ST[n] BC4	ST[n] BC3	ST[n] BC2	ST[n] BC1	ST[n] BC0

Bit	Name	Description
15 - 0	ST[n] BC15 - 0	**Stream[n] BER Count Bits (Read Only):** The binary value of these bits refers to the bit error counts. When it reaches its maximum value of 0xFFFF, the value will be held and will not rollover.

Note: [n] denotes input stream from 0 - 31

Table 67 - BER Receiver Error Register [n] (BRER[n]) Bits - Read Only

24.0 Memory

24.1 Memory Address Mappings

When A13 is high, the data or connection memory can be accessed by the microprocessor port. Bit 1 - 0 in the Control Register determine the access to the data or connection memory (CM_L or CM_H).

MSB (Note 1)	Stream Address (St0 - 31)						Channel Address (Ch0 - 255)								
A13	**A12**	**A11**	**A10**	**A9**	**A8**	**Stream [n]**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**Channel [n]**
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.		.	.		.	.
.	.	.	.	.	.	.	.	.	.		.			.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	Ch 63 (Note 3)
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	0	1	1	1	0	Stream 14	.	.	.	.	.	.	.	.	.
1	0	1	1	1	1	Stream 15	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	1	1	1	1	1	1	0	Ch126
.	.	.	.	.	.	.	0	1	1	1	1	1	1	1	Ch 127 (Note 4)
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	Stream 30	1	1	1	1	1	1	1	0	Ch 254
1	1	1	1	1	1	Stream 31	1	1	1	1	1	1	1	1	Ch 255 (Note 5)

Note 1: A13 must be high for access to data and connection memory positions. A13 must be low to access internal registers.

Note 2: Channels 0 to 31 are used when serial stream is at 2.048 Mbps.

Note 3: Channels 0 to 63 are used when serial stream is at 4.096 Mbps.

Note 4: Channels 0 to 127 are used when serial stream is at 8.192 Mbps.

Note 5: Channels 0 to 255 are used when serial stream is at 16.384 Mbps.

Table 68 - Address Map for Memory Locations (A13 = 1)

24.2 Connection Memory Low (CM_L) Bit Assignment

When the CMM bit (bit 0) in the connection memory low is zero, the per-channel transmission is set to the normal channel-switching. The connection memory low bit assignment for the channel transmission mode is shown in Table 69 on page 102.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UA EN	V/$\overline{C}$	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	SCA 7	SCA 6	SCA 5	SCA 4	SCA 3	SCA 2	SCA 1	SCA 0	**CMM =0**

Bit	Name	Description
15	UAEN	**Conversion between μ-law and A-law Enable** When this bit is low, normal switch without μ-law/A-law conversion. Connection memory high will be ignored. When this bit is high, switch with μ-law/A-law conversion, and connection memory high controls the conversion method.
14	V/$\overline{C}$	**Variable/Constant Delay Control.** When this bit is low, the output data for this channel will be taken from constant delay memory. When this bit is set to high, the output data for this channel will be taken from variable delay memory. Note that VAREN must be set in Control Register first.
13 - 9	SSA4 - 0	**Source Stream Address.** The binary value of these 5 bits represents the input stream number.
8 - 1	SCA7 - 0	**Source Channel Address.** The binary value of these 8 bits represents the input channel number.
0	CMM = 0	**Connection Memory Mode = 0.** If this is low, the connection memory is in the normal switching mode. Bit13 - 1 are the source stream number and channel number.

Note: For proper μ-law/A-law conversion, the CM_H bits should be set before Bit 15 (UAEN bit) is set to high.

Table 69 - Connection Memory Low (CM_L) Bit Assignment when CMM = 0

When CMM is one, the device is programmed to perform one of the special per-channel transmission modes. Bits PCC0 and PCC1 from connection memory are used to select the per-channel tristate, message or BER test mode as shown in Table 70 on page 103.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UA EN	0	0	0	0	MSG 7	MSG 6	MSG 5	MSG 4	MSG 3	MSG 2	MSG 1	MSG 0	PCC 1	PCC 0	**CMM =1**

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15</td><td>UAEN</td><td>Conversion between μ-law and A-law Enable (Message mode only)
When this bit is low, message mode has no μ-law/A-law conversion. Connection memory high will be ignored.
When this bit is high, message mode has μ-law/A-law conversion, and connection memory high controls the conversion method.</td></tr>
<tr><td>14 - 11</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>10 - 3</td><td>MSG7 - 0</td><td>Message Data Bits: 8-bit data for the message mode. Not used in the per-channel tristate and BER test modes.</td></tr>
<tr><td>2 - 1</td><td>PCC1 - 0</td><td>Per-Channel Control Bits: These two bits control the corresponding entry's value on the STio stream.
<table>
<tr><th>PCC1</th><th>PCC0</th><th>Channel Output Mode</th></tr>
<tr><td>0</td><td>0</td><td>Per Channel Tristate</td></tr>
<tr><td>0</td><td>1</td><td>Message Mode</td></tr>
<tr><td>1</td><td>0</td><td>BER Test Mode</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>0</td><td>CMM = 1</td><td>Connection Memory Mode = 1. If this is high, the connection memory is in the per-channel control mode which is per-channel tristate, per-channel message mode or per-channel BER mode.</td></tr>
<tr><td colspan="3">Note: For proper μ-law/A-law conversion, the CM_H bits should be set before Bit 15 (UAEN bit) is set to high.</td></tr>
</table>

Table 70 - Connection Memory Low (CM_L) Bit Assignment when CMM = 1

24.3 Connection Memory High (CM_H) Bit Assignment

Connection memory high provides the detailed information required for µ-law and A-law conversion. ICL and OCL bits describe the Input Coding Law and the Output Coding Law, respectively. They are used to select the expected PCM coding laws for the connection, on the TDM inputs, and on the TDM outputs. The $\overline{\text{V}}$/D bit is used to select the class of coding law. If the $\overline{\text{V}}$/D bit is cleared (to select a voice connection), the ICL and OCL bits select between A-law and µ-law specifications related to G.711 voice coding. If the $\overline{\text{V}}$/D bit is set (to select a data connection), the ICL and OCL bits select between various bit inverting protocols. These coding laws are illustrated in the following table. If the ICL is different than the OCL, all data bytes passing through the switch on that particular connection are translated between the indicated laws. If the ICL and the OCL are the same, no coding law translation is performed. The ICL, the OCL bits and $\overline{\text{V}}$/D bit only have an effect on PCM code translations for constant delay connections, variable delay connections and per-channel message mode.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	$\overline{\text{V}}$/D	ICL 1	ICL 0	OCL 1	OCL 0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15 - 5</td><td>Unused</td><td>Reserved. In normal functional mode, these bits MUST be set to zero.</td></tr>
<tr><td>4</td><td>$\overline{\text{V}}$/D</td><td>Voice/Data Control.
When this bit is low, the corresponding channel is for voice.
When this bit is high, the corresponding channel is for data.</td></tr>
<tr><td>3 - 2</td><td>ICL1 - 0</td><td>Input Coding Law.
<table>
<tr><th rowspan="2">ICL1-0</th><th colspan="2">Input Coding Law</th></tr>
<tr><th>For Voice ($\overline{\text{V}}$/D bit = 0)</th><th>For Data ($\overline{\text{V}}$/D bit = 1)</th></tr>
<tr><td>00</td><td>CCITT.ITU A-law</td><td>No code</td></tr>
<tr><td>01</td><td>CCITT.ITU µ-law</td><td>ABI</td></tr>
<tr><td>10</td><td>A-law w/o ABI</td><td>Inverted ABI</td></tr>
<tr><td>11</td><td>µ-law w/o Magnitude Inversion</td><td>All Bits Inverted</td></tr>
</table>
</td></tr>
<tr><td>1 - 0</td><td>OCL1 - 0</td><td>Output Coding Law.
<table>
<tr><th rowspan="2">OCL1-0</th><th colspan="2">Output Coding Law</th></tr>
<tr><th>For Voice ($\overline{\text{V}}$/D bit = 0)</th><th>For Data ($\overline{\text{V}}$/D bit = 1)</th></tr>
<tr><td>00</td><td>CCITT.ITU A-law</td><td>No code</td></tr>
<tr><td>01</td><td>CCITT.ITU µ-law</td><td>ABI</td></tr>
<tr><td>10</td><td>A-law w/o ABI</td><td>Inverted ABI</td></tr>
<tr><td>11</td><td>µ-law w/o Magnitude Inversion</td><td>All Bits Inverted</td></tr>
</table>
</td></tr>
</table>

Note 1: For proper µ-law/A-law conversion, the CM_H bits should be set before Bit 15 of CM_L is set to high.

Note 2: Refer to G.711 standard for detail information of different laws.

Table 71 - Connection Memory High (CM_H) Bit Assignment

25.0 Applications

This section contains application-specific details for clock and crystal operation and power supply decoupling.

25.1 OSCi Master Clock Requirement

The device requires a 20 MHz master clock source at the OSCi pin when operating in Master mode or in Divided Slave with OSC mode. The clock source may be either an external clock oscillator connected to the OSCi pin, or an external crystal connected between the OSCi and OSCo pins. If an external clock source is present, OSC_EN must be tied high.

Note that using a crystal is only suitable for wider tolerance applications (i.e. ±100 ppm). Stratum 4E applications (i.e. ±32 ppm) should use a clock oscillator while Stratum 3 applications (i.e. ±4.6 ppm) should use a temperature-compensated clock module. See Application Note ZLAN-68 for a list of Oscillators and Crystals that can be used with Zarlink PLL's and Digital Switches with embedded PLL's.

25.1.1 External Crystal Oscillator

When an external crystal oscillator is used, a complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 23 on page 105. XC is a buffered version of the 20 MHz input clock connected to the internal circuitry.

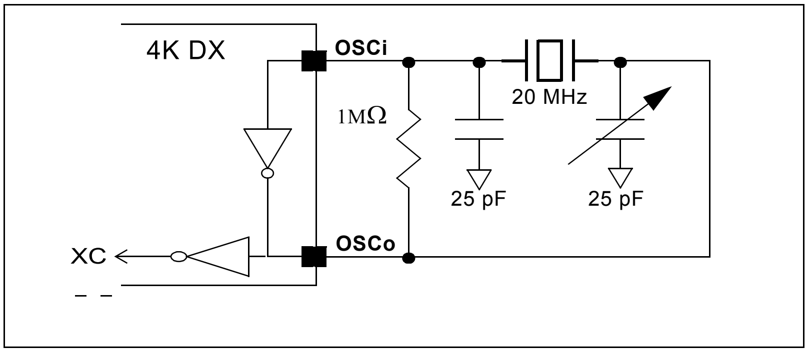


Figure 23 - Crystal Oscillator Circuit

The accuracy of a crystal oscillator circuit depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances and stray capacitances have a major effect on the accuracy of the oscillator frequency. The trimmer capacitor shown in Figure 23 on page 105 may be used to compensate for capacitive effects.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal accuracy only affects the output clock accuracy in the freerun or the holdover mode. The crystal specification is as follows:

Frequency	20 MHz
Tolerance	As required
Oscillation Mode	Fundamental
Resonance Mode	Parallel
Load Capacitance	20 pF - 32 pF
Maximum Series Resistance	35 Ω
Approximate Drive Level	1 mW

25.1.2 External Clock Oscillator

When an external clock oscillator is used, numerous parameters must be considered. They include absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle.

The output clock should be connected directly (not AC coupled) to the OSCi input of the device, and the OSCo output should be left open as shown in Figure 24 on page 106. XC is a buffered version of the 20 MHz input clock connected to the internal circuitry.

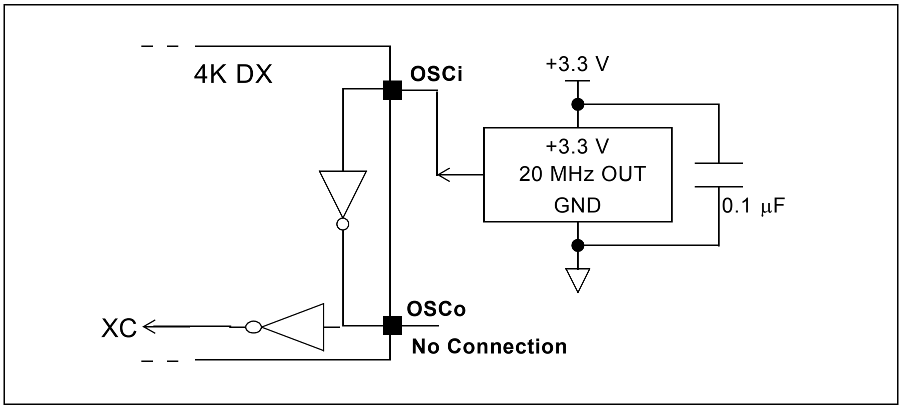


Figure 24 - Clock Oscillator Circuit

For applications requiring ±32 ppm clock accuracy, the following requirements should be met:

Frequency	20.000 MHz
Tolerance	±32 ppm
Rise and Fall Time	10 ns
Duty Cycle	40% to 60%

For applications requiring Stratum 3 compliance (±4.6 ppm clock accuracy), the following temperature compensated clock oscillator module may be used.

Frequency	20.000 MHz
Tolerance	±4.6 ppm
Rise and Fall Time	10 ns
Duty Cycle	40% to 60%

26.0 DC Parameters

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
2	Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
3	Input Voltage	V_{I_3V}	-0.5	V_{DD} + 0.5	V
4	Input Voltage (5V-tolerant inputs)	V_{I_5V}	-0.5	7.0	V
5	Continuous Current at Digital Outputs	I_o		15	mA
6	Package Power Dissipation	P_D		1.5	W
7	Storage Temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD_IO}	3.0	3.3	3.6	V
3	Positive Supply	V_{DD_CORE}	1.71	1.8	1.89	V
4	Input Voltage	V_I	0	3.3	V_{DD_IO}	V
5	Input Voltage on 5V-Tolerant Inputs	V_{I_5V}	0	5.0	5.5	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current - V_{DD_CORE}	I_{DD_CORE}			175	mA	
2	Supply Current - V_{DD_IO}	I_{DD_IO}			75	mA	C_L = 30 pF
3	Input High Voltage	V_{IH}	2.0			V	
4	Input Low Voltage	V_{IL}			0.8	V	
5	Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			5 5	µA µA	$0 \le < V_{IN} \le V_{DD\_IO}$ See Note 1
6	Weak Pullup Current	I_{PU}		-33		µA	Input at 0V
7	Weak Pulldown Current	I_{PD}		33		µA	Input at V_{DD_IO}
8	Input Pin Capacitance	C_I		3		pF	
9	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 8 mA
10	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
11	Output High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD}$
12	Output Pin Capacitance	C_O		5	10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).

27.0 AC Parameters

AC Electrical Characteristics[†] - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	$0.5V_{DD\_IO}$	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD\_IO}$	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD\_IO}$	V	

† Characteristics are over recommended operating conditions unless otherwise stated.

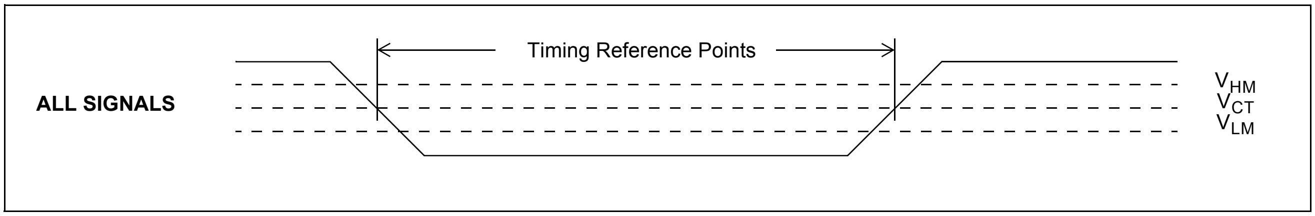


Figure 25 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode - Read Access

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions[2]
1	$\overline{\text{CS}}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{\text{DS}}$ de-asserted time	t_{DSD}	15			ns	
3	$\overline{\text{CS}}$ setup to $\overline{\text{DS}}$ falling	t_{CSS}	0			ns	
4	R/$\overline{\text{W}}$ setup to $\overline{\text{DS}}$ falling	t_{RWS}	10			ns	
5	Address setup to $\overline{\text{DS}}$ falling	t_{AS}	5			ns	
6	$\overline{\text{CS}}$ hold after $\overline{\text{DS}}$ rising	t_{CSH}	0			ns	
7	R/$\overline{\text{W}}$ hold after $\overline{\text{DS}}$ rising	t_{RWH}	0			ns	
8	Address hold after $\overline{\text{DS}}$ rising	t_{AH}	0			ns	
9	Data setup to $\overline{\text{DTA}}$ Low	t_{DS}	8			ns	C_L = 50 pF
10	Data hold after $\overline{\text{DS}}$ rising	t_{DH}	7			ns	C_L = 50 pF, R_L = 1 K (Note 1)
11	Acknowledgement delay time. From $\overline{\text{DS}}$ low to $\overline{\text{DTA}}$ low: Registers Memory	t_{AKD}			 75 185	 ns ns	 C_L = 50 pF C_L = 50 pF
12	Acknowledgement hold time. From $\overline{\text{DS}}$ high to $\overline{\text{DTA}}$ high	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
13	$\overline{\text{DTA}}$ drive high to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (see Section 17.2 on page 49) must be applied before the first microprocessor access is performed after the $\overline{\text{RESET}}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

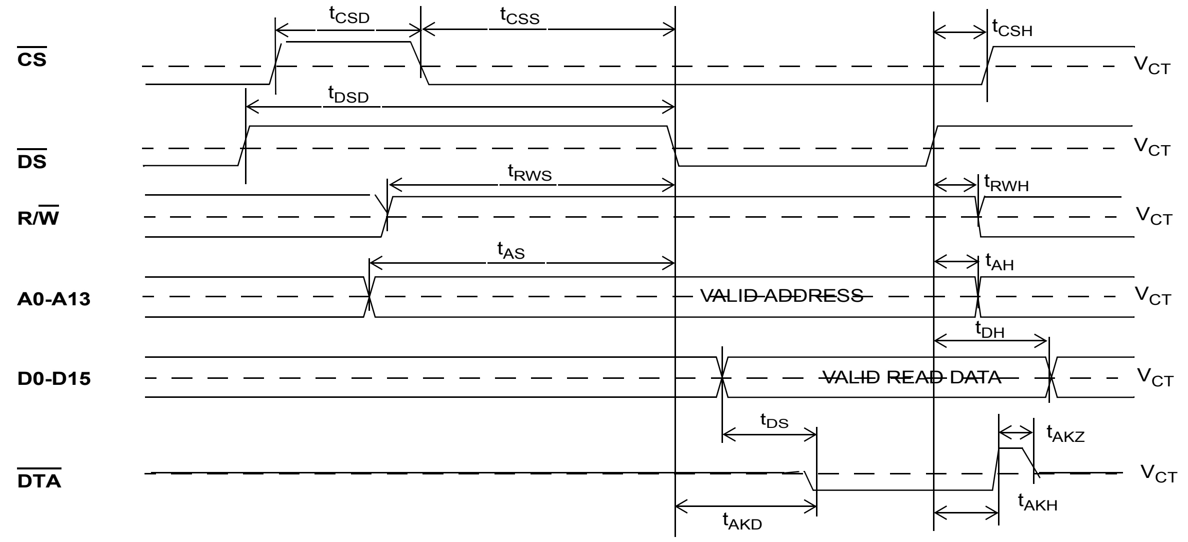


Figure 26 - Motorola Non-Multiplexed Bus Timing - Read Access

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode - Write Access

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions²
14	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
15	$\overline{DS}$ de-asserted time	t_{DSD}	15			ns	
16	$\overline{CS}$ setup to $\overline{DS}$ falling	t_{CSS}	0			ns	
17	R/$\overline{W}$ setup to $\overline{DS}$ falling	t_{RWS}	10			ns	
18	Address setup to $\overline{DS}$ falling	t_{AS}	5			ns	
19	Data setup to $\overline{DS}$ falling	t_{DS}	0			ns	C_L = 50 pF
20	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
21	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	0			ns	
22	Address hold after $\overline{DS}$ rising	t_{AH}	0			ns	
23	Data hold from $\overline{DS}$ rising	t_{DH}	5			ns	C_L = 50 pF, R_L = 1 K (Note 1)
24	Acknowledgement delay time. From $\overline{DS}$ low to $\overline{DTA}$ low: Registers Memory	t_{AKD}			55 150	ns ns	C_L = 50 pF C_L = 50 pF
25	Acknowledgement hold time. From $\overline{DS}$ high to $\overline{DTA}$ high	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
26	$\overline{DTA}$ drive high to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs (see Section 17.2 on page 49) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

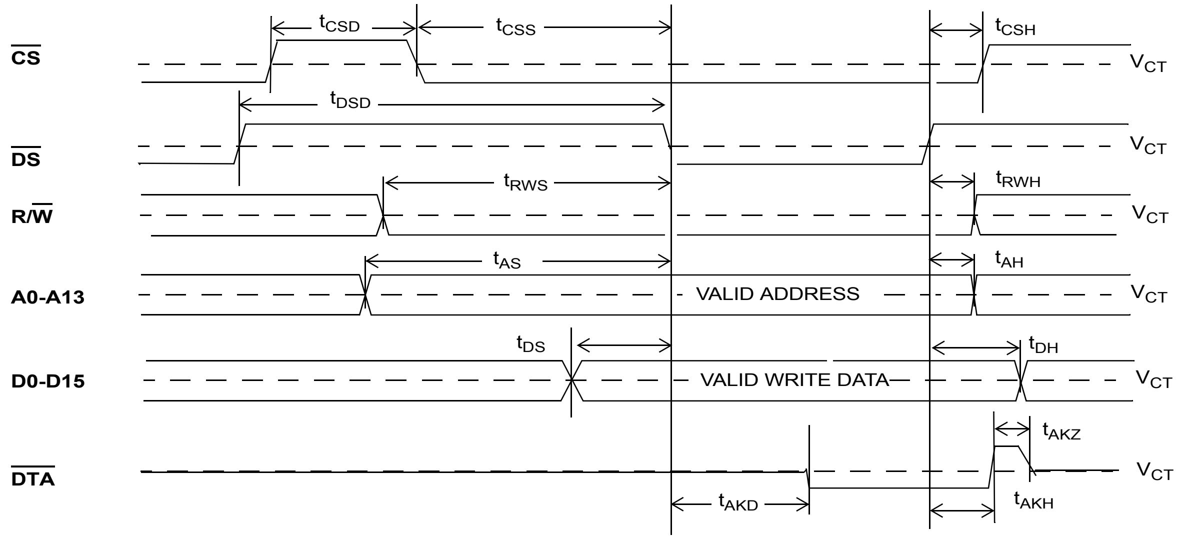


Figure 27 - Motorola Non-Multiplexed Bus Timing - Write Access

AC Electrical Characteristics† - Intel Non-Multiplexed Bus Mode - Read Access

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions[2]
27	$\overline{\text{CS}}$ de-asserted time	t_{CSD}	15			ns	
28	$\overline{\text{RD}}$ setup to $\overline{\text{CS}}$ falling	t_{RS}	10			ns	
29	$\overline{\text{WR}}$ setup to $\overline{\text{CS}}$ falling	t_{WS}	10			ns	
30	Address setup to $\overline{\text{CS}}$ falling	t_{AS}	5			ns	
31	$\overline{\text{RD}}$ hold after $\overline{\text{CS}}$ rising	t_{RH}	0			ns	
32	$\overline{\text{WR}}$ hold after $\overline{\text{CS}}$ rising	t_{WH}	0			ns	
33	Address hold after $\overline{\text{CS}}$ rising	t_{AH}	0			ns	
34	Data setup to RDY high	t_{DS}	8			ns	C_L = 50 pF
35	Data hold after $\overline{\text{CS}}$ rising	t_{DH}	7			ns	C_L = 50 pF, R_L = 1 K (Note 1)
36	Acknowledgement delay time. From $\overline{\text{CS}}$ low to RDY high: Registers Memory	t_{AKD}			175 185	ns ns	C_L = 50 pF C_L = 50 pF
37	Acknowledgement hold time. From $\overline{\text{CS}}$ high to RDY low	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
38	RDY drive low to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2ms (see Section 17.2 on page 49) must be applied before the first microprocessor access is performed after the $\overline{\text{RESET}}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

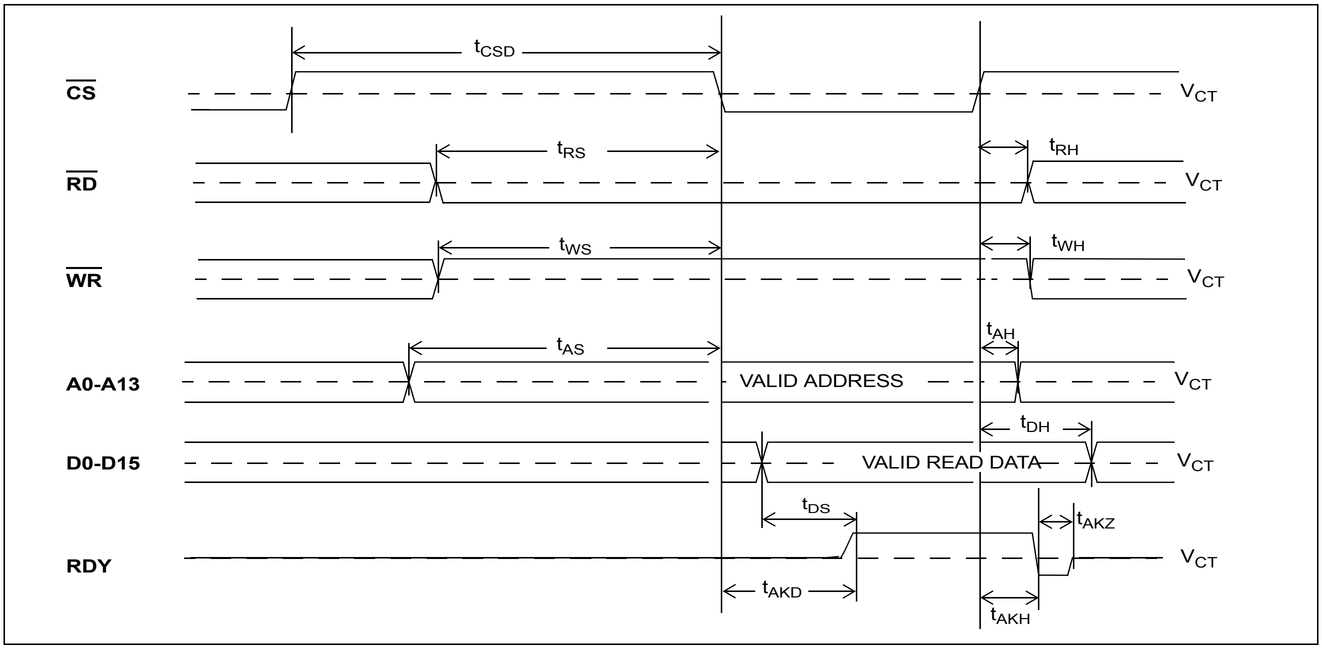


Figure 28 - Intel Non-Multiplexed Bus Timing - Read Access

AC Electrical Characteristics† - Intel Non-Multiplexed Bus Mode - Write Access

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions[2]
39	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
40	$\overline{WR}$ setup to $\overline{CS}$ falling	t_{WS}	10			ns	
41	$\overline{RD}$ setup to $\overline{CS}$ falling	t_{RS}	10			ns	
42	Address setup to $\overline{CS}$ falling	t_{AS}	5			ns	
43	Data setup to $\overline{CS}$ falling	t_{DS}	0			ns	C_L = 50 pF
44	$\overline{WR}$ hold after $\overline{CS}$ rising	t_{WH}	0			ns	
45	$\overline{RD}$ hold after $\overline{CS}$ rising	t_{RH}	0			ns	
46	Address hold after $\overline{CS}$ rising	t_{AH}	10			ns	
47	Data hold after $\overline{CS}$ rising	t_{DH}	5			ns	C_L = 50 pF, R_L = 1 K (Note 1)
48	Acknowledgement delay time. From $\overline{CS}$ low to RDY high: Registers Memory	t_{AKD}			 55 150	 ns ns	 C_L = 50 pF C_L = 50 pF
49	Acknowledgement hold time. From $\overline{CS}$ high to RDY low	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
50	RDY drive low to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2ms (Section 17.2 on page 49) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

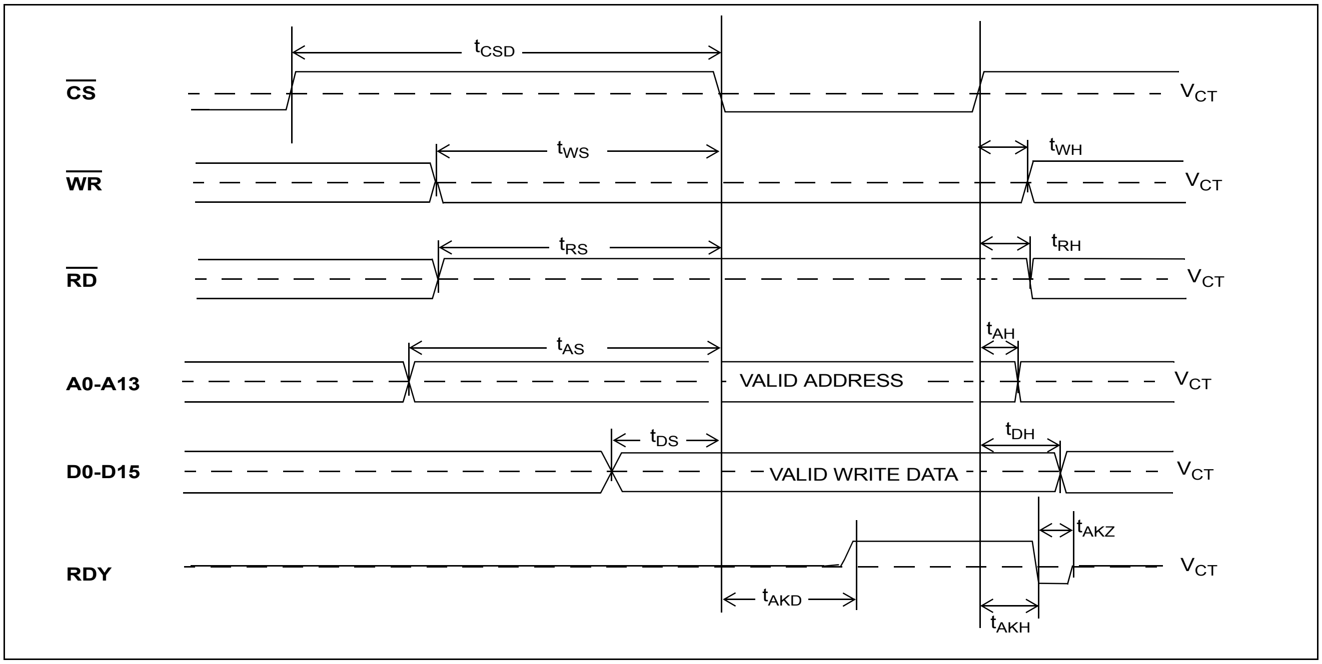


Figure 29 - Intel Non-Multiplexed Bus Timing - Write Access

AC Electrical Characteristics† - JTAG Test Port Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	100			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	20			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	20			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	60			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L = 30 pF
9	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	200			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

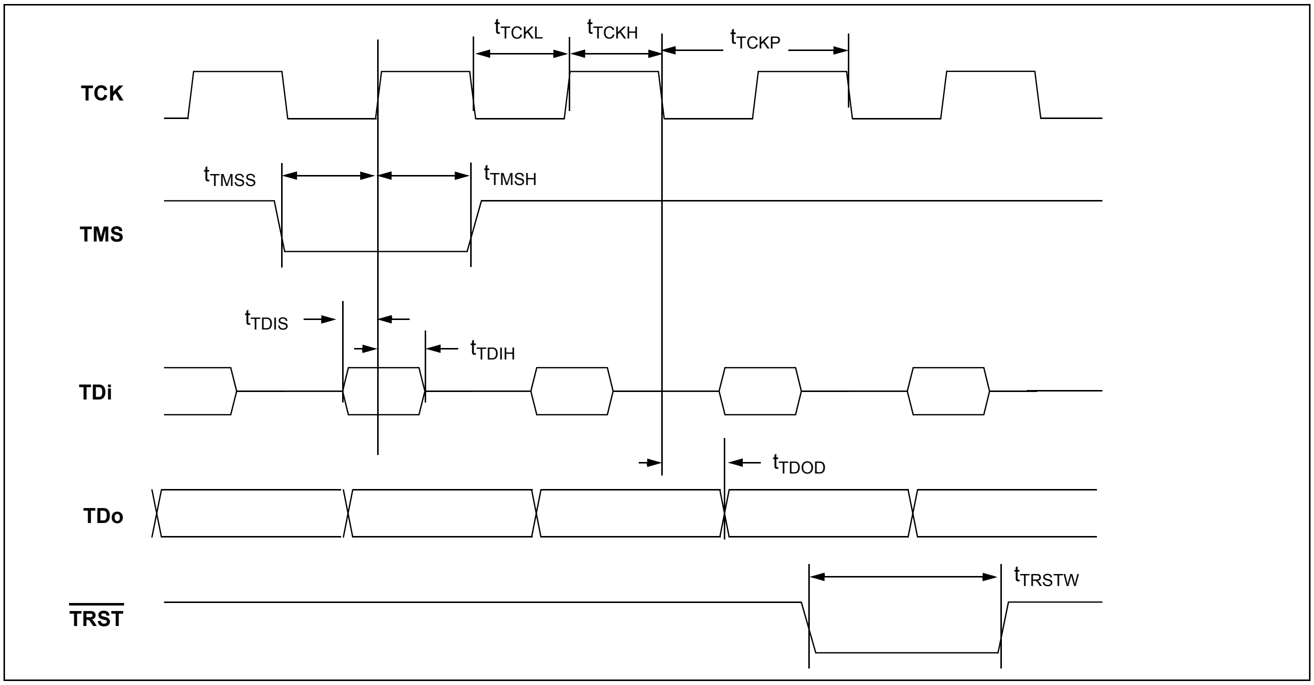


Figure 30 - JTAG Test Port Timing Diagram

AC Electrical Characteristics† - OSCi 20 MHz Input Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes‡
1	Input frequency accuracy		-4.6		4.6	ppm	1
2	Duty cycle		40		60	%	
3	Input rise or fall time	t_{IR}, t_{IF}			3	ns	17

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ See "Performance Characteristics Notes" on page 133.

AC Electrical Characteristics[†] - FPi and CKi Timing when CKIN1-0 bits = 00 (16.384 MHz)

	Characteristic	Sym.	Min.	Typ.[‡]	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	40	61	115	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	20			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	20			ns	
4	CKi Input Clock Period	t_{CKIP}	55	61	67	ns	
5	CKi Input Clock High Time	t_{CKIH}	27		34	ns	
6	CKi Input Clock Low Time	t_{CKIL}	27		34	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics[†] - FPi and CKi Timing when CKIN1-0 bits = 01 (8.192 MHz)

	Characteristic	Sym.	Min.	Typ.[‡]	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	90	122	220	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	45			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	45			ns	
4	CKi Input Clock Period	t_{CKIP}	110	122	135	ns	
5	CKi Input Clock High Time	t_{CKIH}	55		69	ns	
6	CKi Input Clock Low Time	t_{CKIL}	55		69	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics[†] - FPi and CKi Timing when CKIN1-0 bits = 10 (4.096 MHz)

	Characteristic	Sym.	Min.	Typ.[‡]	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	90	244	420	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	110			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	110			ns	
4	CKi Input Clock Period	t_{CKIP}	220	244	270	ns	
5	CKi Input Clock High Time	t_{CKIH}	110		135	ns	
6	CKi Input Clock Low Time	t_{CKIL}	110		135	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

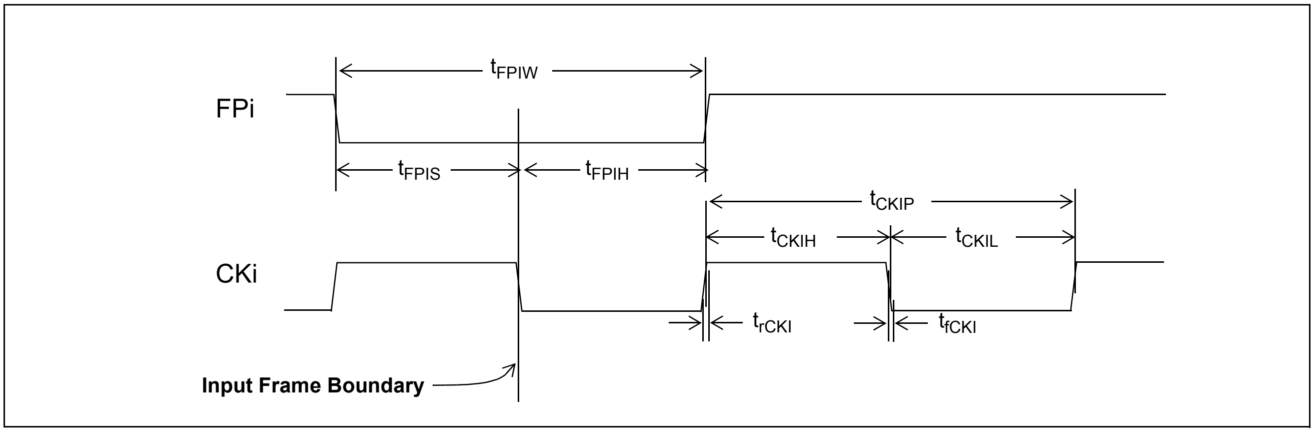


Figure 31 - Frame Pulse Input and Clock Input Timing Diagram (ST-BUS)

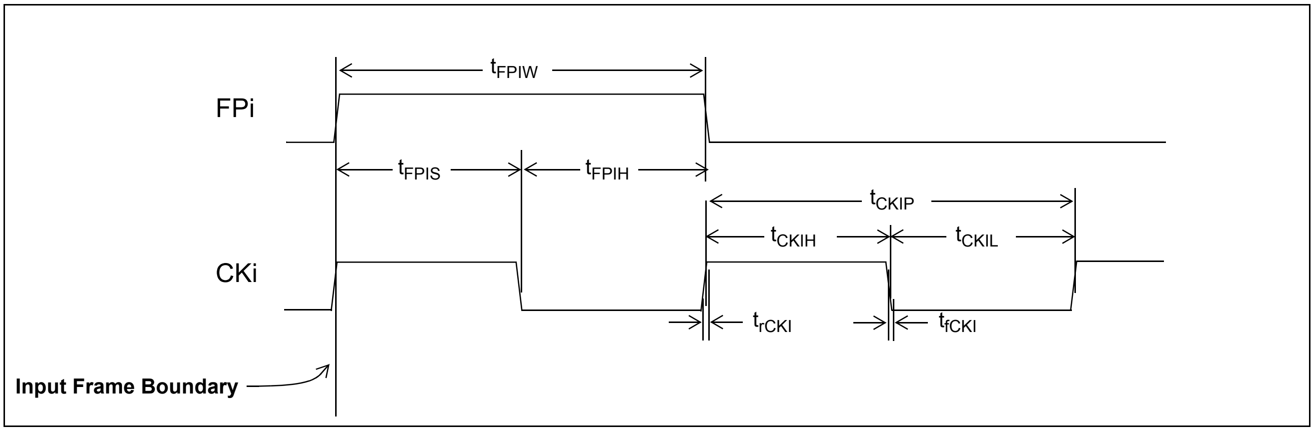


Figure 32 - Frame Pulse Input and Clock Input Timing Diagram (GCI-Bus)

AC Electrical Characteristics† - ST-BUS/GCI-Bus Input Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	STi Setup Time						
	2.048 Mbps	t_{SIS2}	5			ns	
	4.096 Mbps	t_{SIS4}	5			ns	
	8.192 Mbps	t_{SIS8}	5			ns	
	16.384 Mbps	t_{SIS16}	8			ns	
2	STi Hold Time						
	2.048 Mbps	t_{SIH2}	8			ns	
	4.096 Mbps	t_{SIH4}	8			ns	
	8.192 Mbps	t_{SIH8}	8			ns	
	16.384 Mbps	t_{SIH16}	8			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

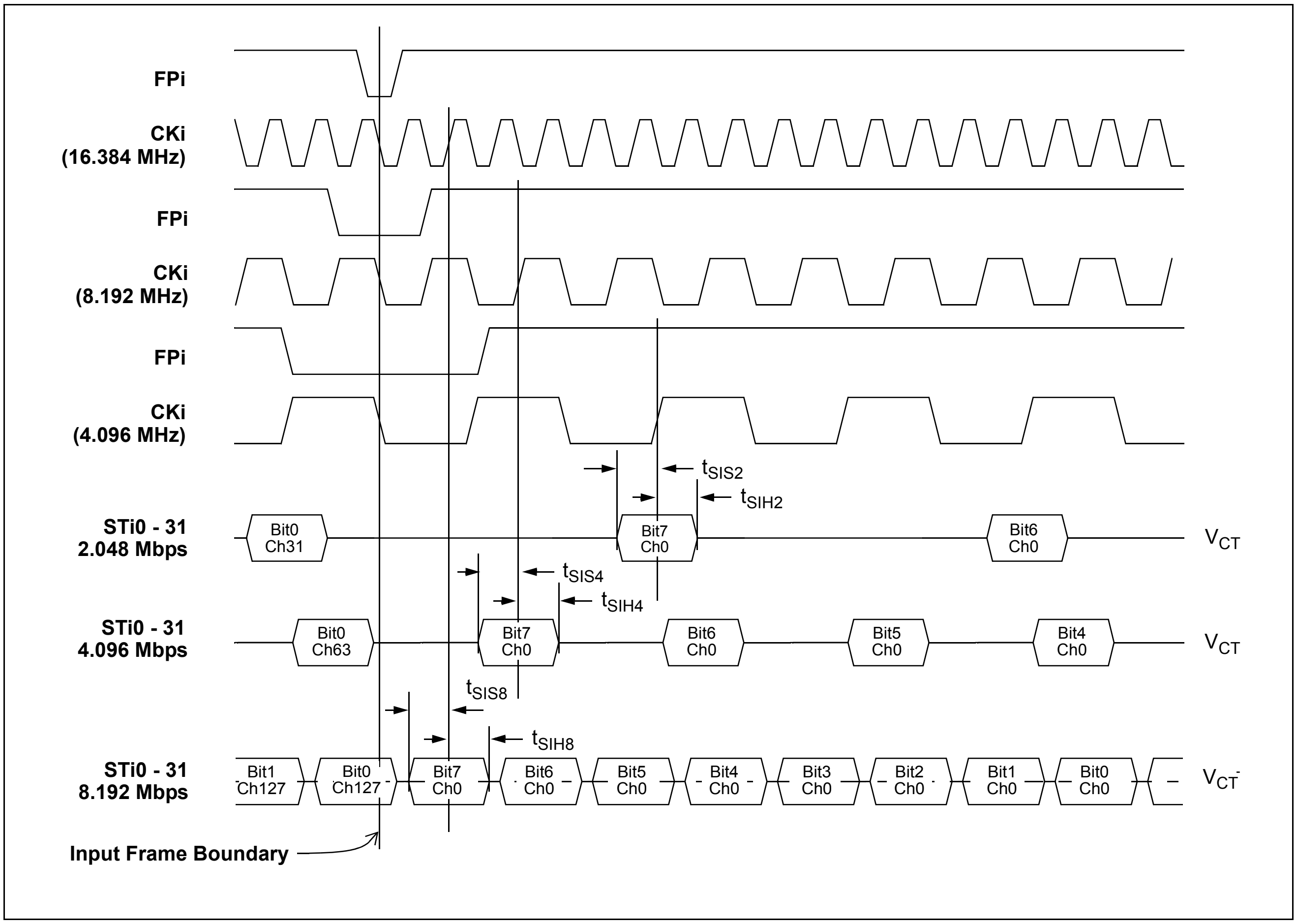


Figure 33 - ST-BUS Input Timing Diagram when Operated at 2 Mbps, 4 Mbps, 8 Mbps

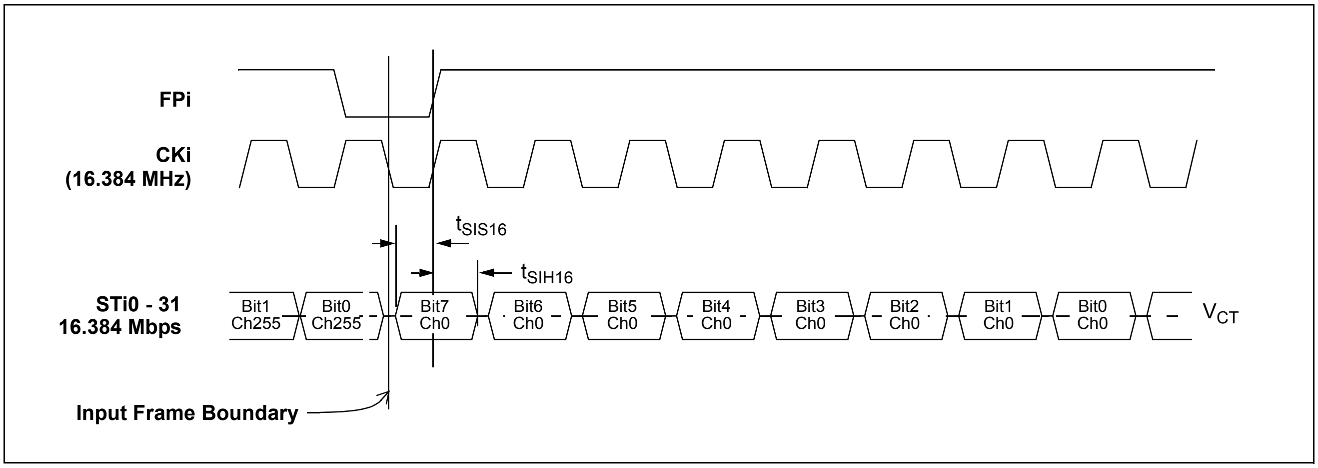


Figure 34 - ST-BUS Input Timing Diagram when Operated at 16 Mbps

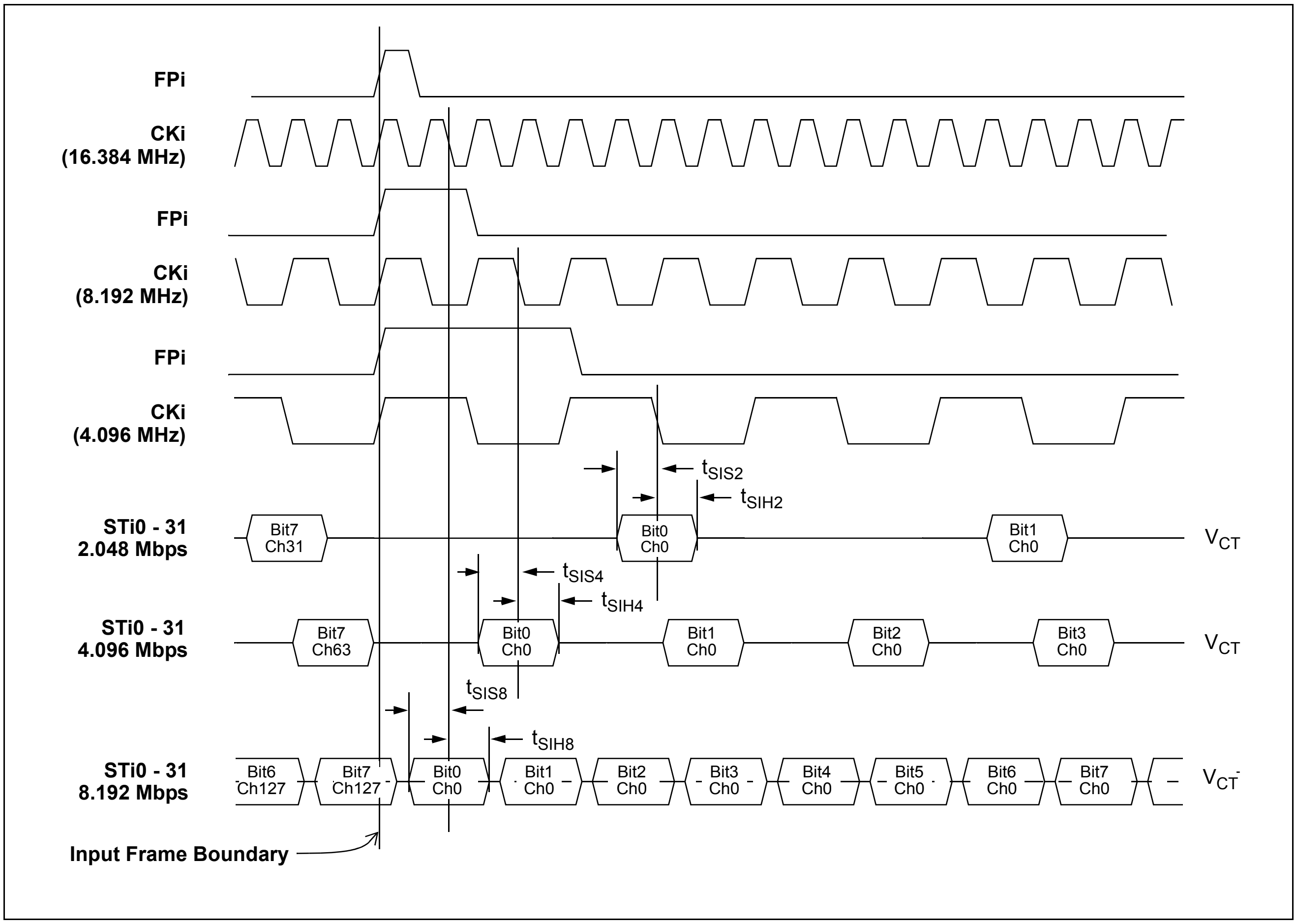


Figure 35 - GCI-Bus Input Timing Diagram when Operated at 2 Mbps, 4 Mbps, 8 Mbps

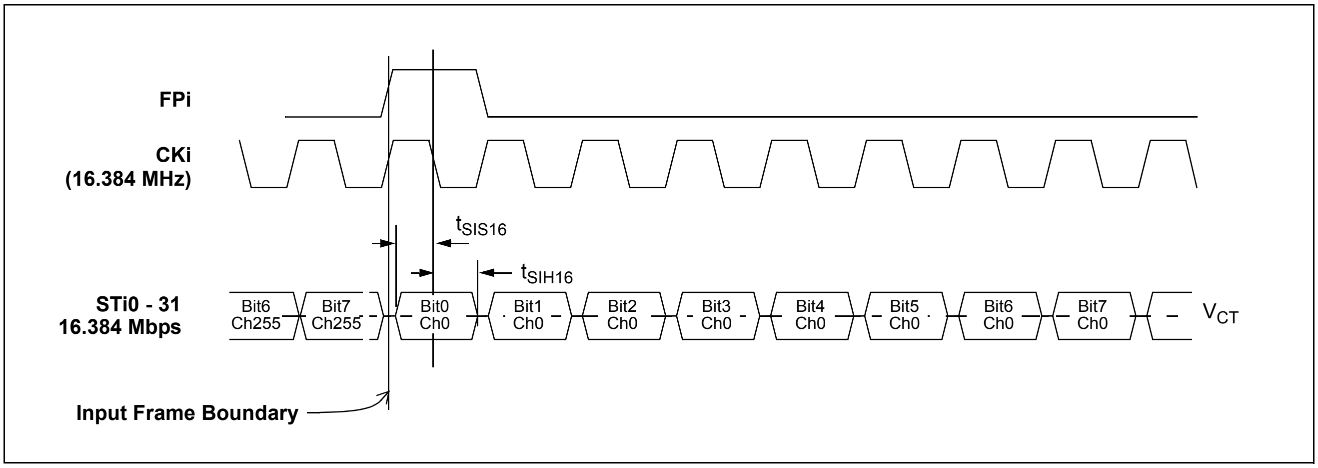


Figure 36 - GCI-Bus Input Timing Diagram when Operated at 16 Mbps

AC Electrical Characteristics† - ST-BUS/GCI-Bus Master Mode Output Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	STio Delay - Active to Active						C_L = 30 pF
	at 2.048 Mbps	t_{SOD2}	1		8	ns	
	at 4.096 Mbps	t_{SOD4}	1		8	ns	
	at 8.192 Mbps	t_{SOD8}	1		8	ns	
	at 16.384 Mbps	t_{SOD16}	1		8	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - ST-BUS/GCI-Bus Multiplied Slave Mode Output Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	STio Delay - Active to Active						C_L = 30 pF
	at 2.048 Mbps	t_{SOD2}	0		6	ns	
	at 4.096 Mbps	t_{SOD4}	0		6	ns	
	at 8.192 Mbps	t_{SOD8}	0		6	ns	
	at 16.384 Mbps	t_{SOD16}	0		6	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - ST-BUS/GCI-Bus Divided Slave Mode Output Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	STio Delay - Active to Active						C_L = 30 pF
	at 2.048 Mbps	t_{SOD2}	-6		0	ns	
	at 4.096 Mbps	t_{SOD4}	-6		0	ns	
	at 8.192 Mbps	t_{SOD8}	-6		0	ns	
	at 16.384 Mbps	t_{SOD16}	-6		0	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

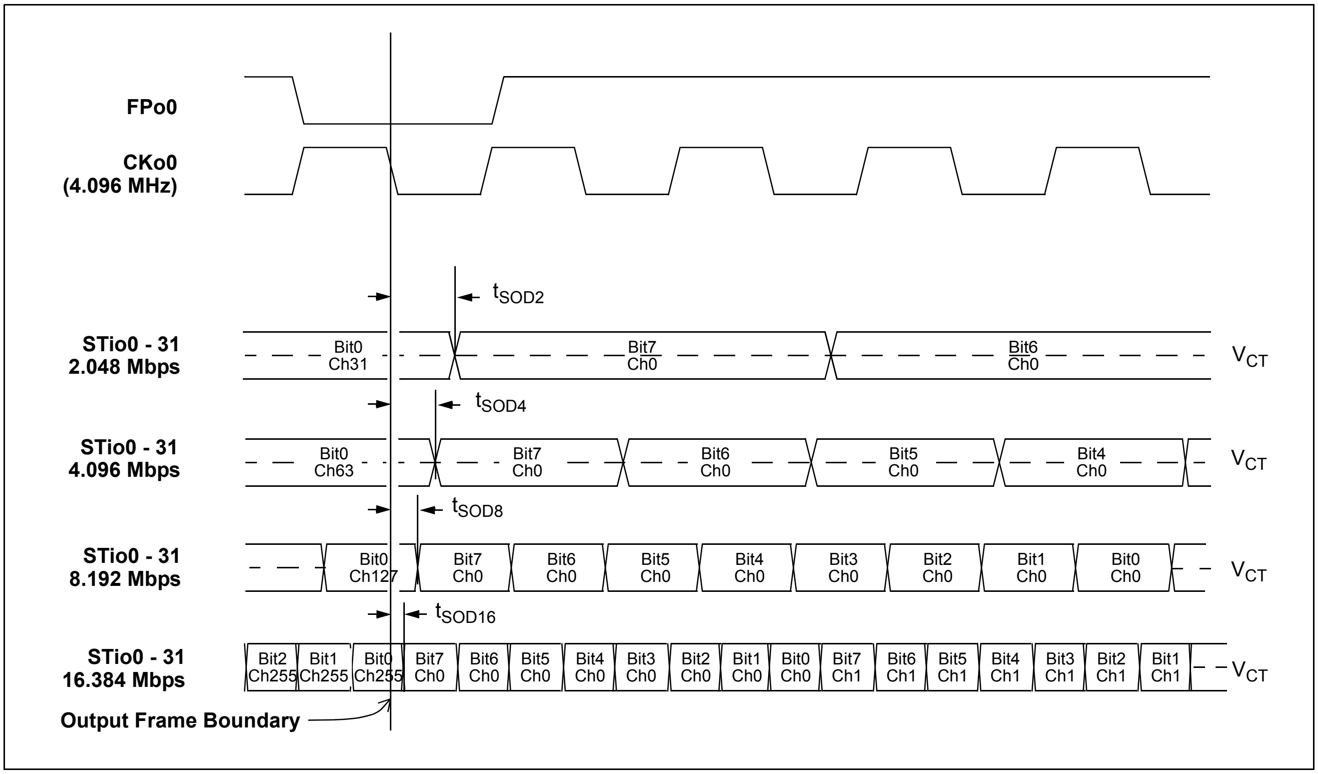


Figure 37 - ST-BUS Output Timing Diagram when Operated at 2, 4, 8 or 16 Mbps

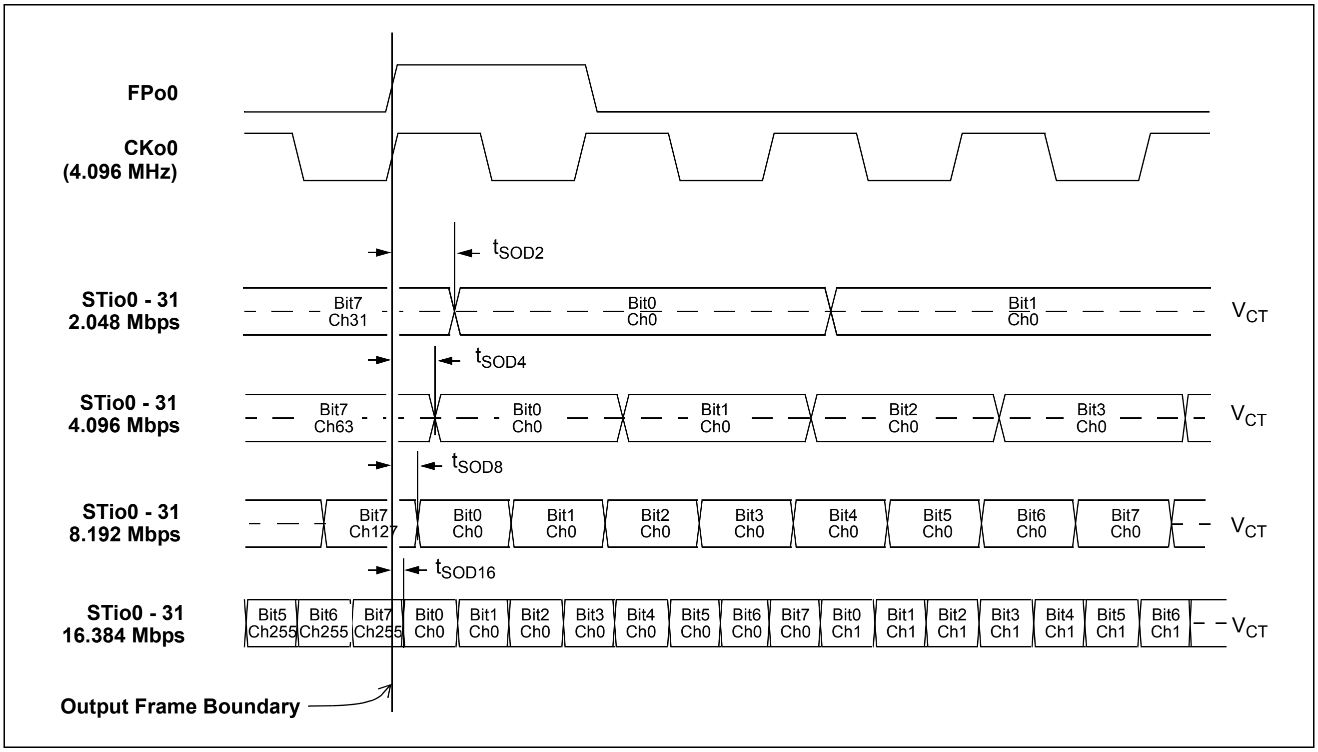


Figure 38 - GCI-Bus Output Timing Diagram when Operated at 2, 4, 8 or 16 Mbps

AC Electrical Characteristics† - ST-BUS/GCI-Bus Output Tristate Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions*
1	STio Delay - Active to High-Z	t_{DZ}	-2 -3 -8		8 7 0	ns ns ns	Master Mode Multiplied Slave Mode Divided Slave Mode
2	STio Delay - High-Z to Active	t_{ZD}	-2 -3 -8		8 7 0	ns ns ns	Master Mode Multiplied Slave Mode Divided Slave Mode
3	Output Drive Enable (ODE) Delay - High-Z to Active	t_{ZD_ODE}			77	ns	Master or Multiplied Slave Mode
	CKi @ 4.096 MHz CKi @ 8.192 MHz CKi @ 16.384 MHz				260 138 77	ns ns ns	Divided Slave Mode
4	Output Drive Enable (ODE) Delay - Active to High-Z	t_{DZ_ODE}			77	ns ns	Master or Multiplied Slave Mode
	CKi @ 4.096 MHz CKi @ 8.192 MHz CKi @ 16.384 MHz				260 138 77	ns	Divided Slave Mode

† Characteristics are over recommended operating conditions unless otherwise stated.

* Test condition is R_L = 1 k, C_L = 30 pF; high impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

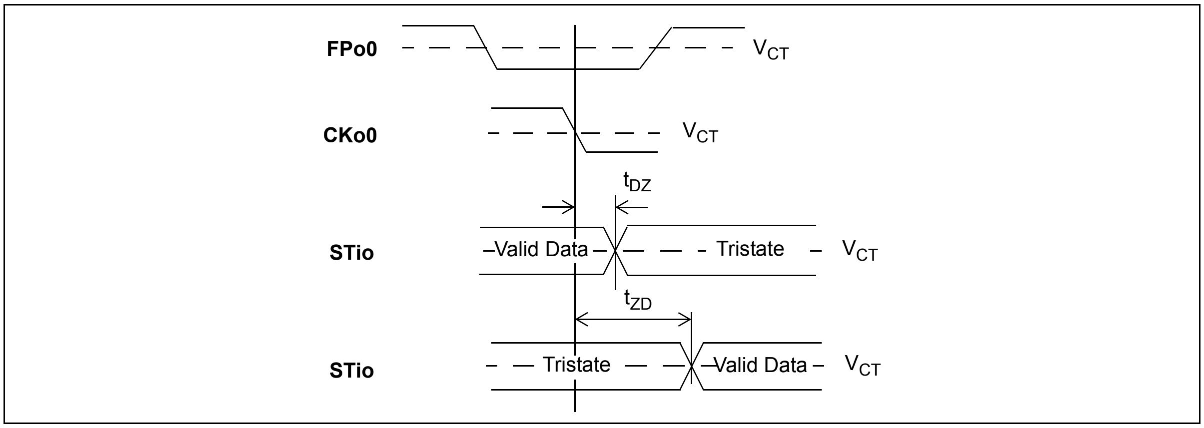


Figure 39 - Serial Output and External Control

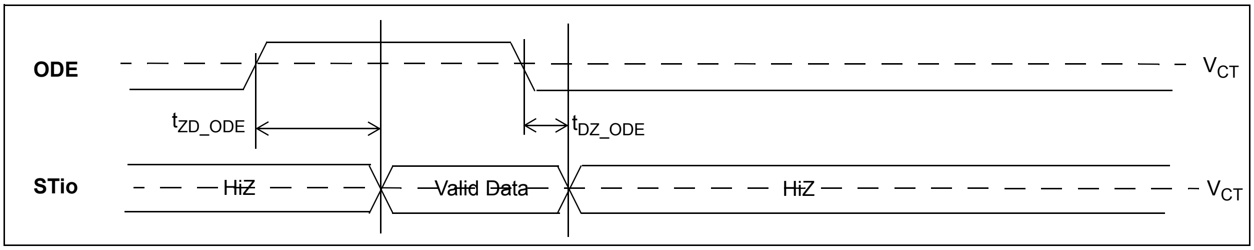


Figure 40 - Output Drive Enable (ODE)

AC Electrical Characteristics† - Slave Mode Input/Output Frame Boundary Alignment

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Input and Output Frame Offset in Divided Slave with CKi mode	t_{FBOS}	5		13	ns	
2	Input and Output Frame Offset in Multiplied Slave	t_{FBOS}	2		10	ns	Input reference jitter is equal to zero.

† Characteristics are over recommended operating conditions unless otherwise stated.

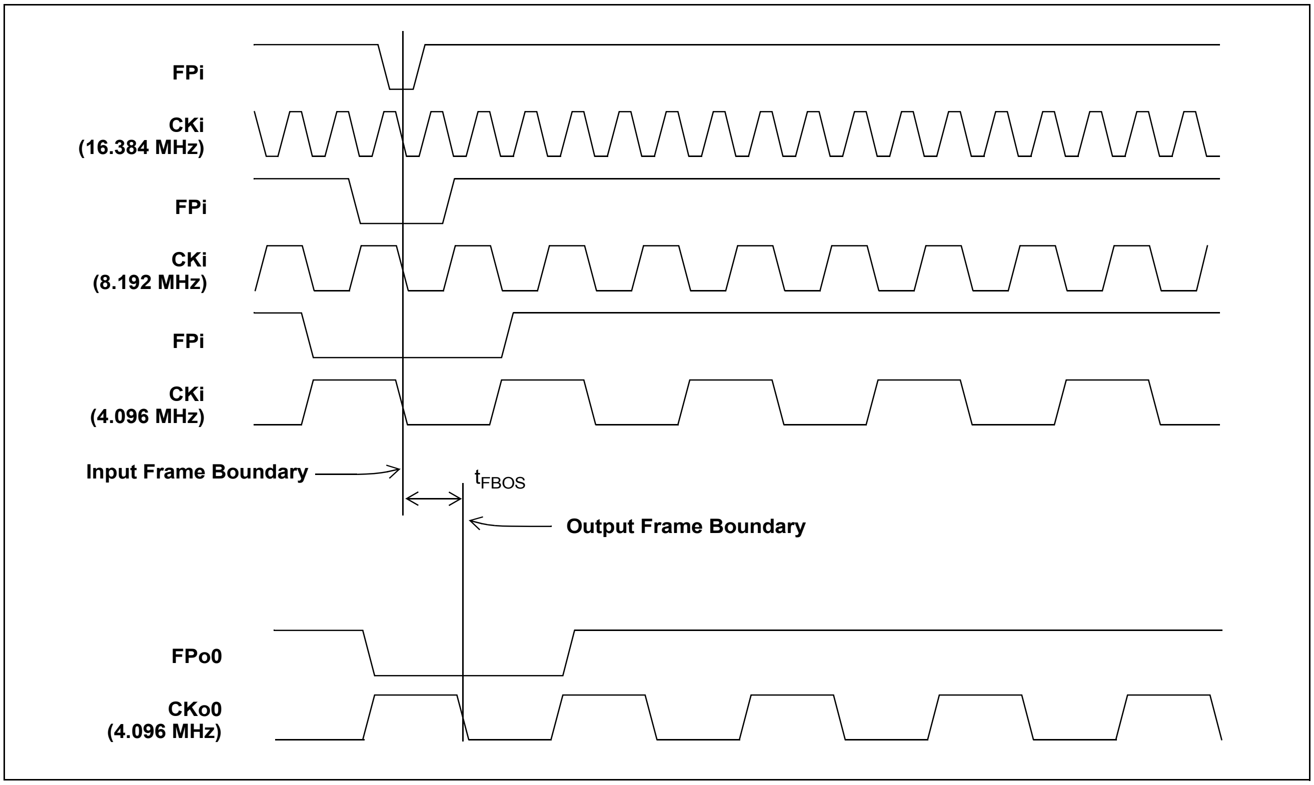


Figure 41 - Input and Output Frame Boundary Offset

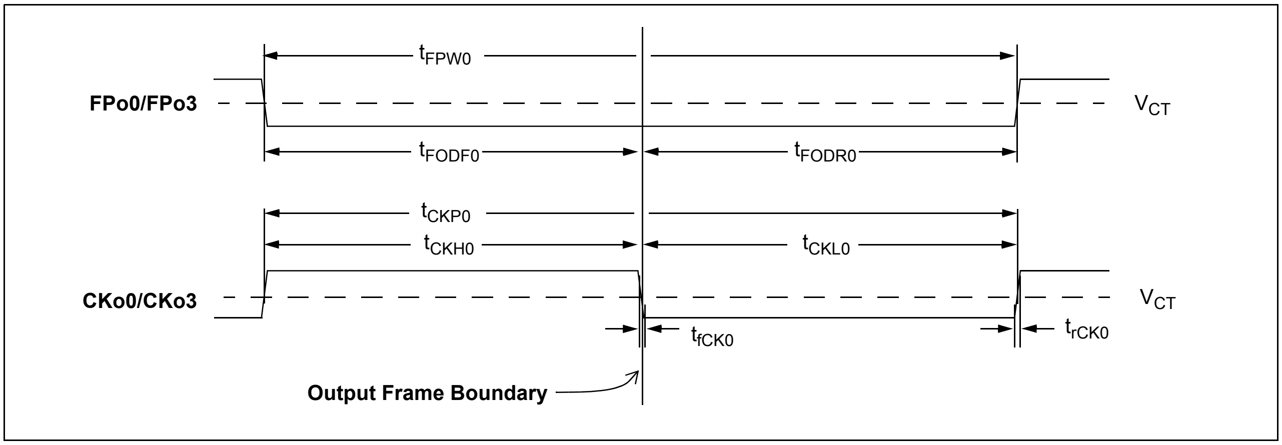


Figure 42 - FPo0 and CKo0 or FPo3 and CKo3 (4.096 MHz) Timing Diagram

AC Electrical Characteristics† - FPo0 and CKo0 or FPo3 and CKo3 (4.096 MHz) Timing (Master Mode, Divided Slave Mode, or Multiplied Slave Mode with less than 10 ns of jitter on CKi)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo0 Output Pulse Width	t_{FPW0}	239	244	249	ns	C_L = 30 pF
2	FPo0 Output Delay from the FPo0 falling edge to the output frame boundary	t_{FODF0}	117		127	ns	
3	FPo0 Output Delay from the output frame boundary to the FPo0 rising edge	t_{FODR0}	117		127	ns	
4	CKo0 Output Clock Period	t_{CKP0}	239	244	249	ns	C_L = 30 pF
5	CKo0 Output High Time	t_{CKH0}	117		127	ns	
6	CKo0 Output Low Time	t_{CKL0}	117		127	ns	
7	CKo0 Output Rise/Fall Time	t_{rCK0}, t_{fCK0}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo0 and CKo0 or FPo3 and CKo3 (4.096 MHz) Timing (Multiplied Slave Mode with more than 10 ns of jitter on CKi)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo0 Output Pulse Width	t_{FPW0}	218	244	270	ns	C_L = 30 pF
2	FPo0 Output Delay from the FPo0 falling edge to the output frame boundary	t_{FODF0}	117		127	ns	
3	FPo0 Output Delay from the output frame boundary to the FPo0 rising edge	t_{FODR0}	97		146	ns	
4	CKo0 Output Clock Period	t_{CKP0}	218	244	270	ns	C_L = 30 pF
5	CKo0 Output High Time	t_{CKH0}	117		127	ns	
6	CKo0 Output Low Time	t_{CKL0}	97		146	ns	
7	CKo0 Output Rise/Fall Time	t_{rCK0}, t_{fCK0}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

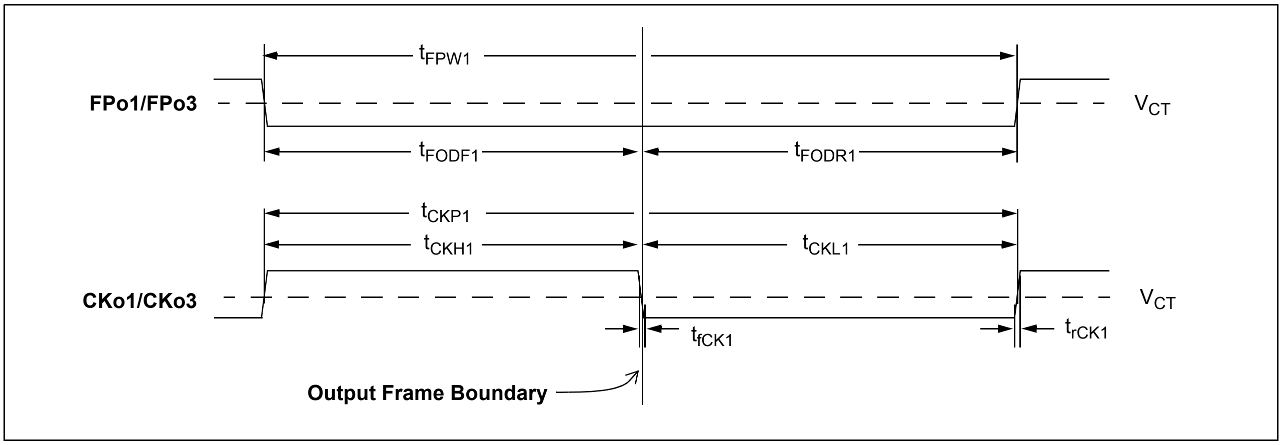


Figure 43 - FPo1 and CKo1 or FPo3 and CKo3 (8.192 MHz) Timing Diagram

AC Electrical Characteristics† - FPo1 and CKo1 or FPo3 and CKo3 (8.192 MHz) Timing (Master Mode, Divided Slave Mode, or Multiplied Slave Mode with less than 10 ns of jitter on CKi)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo1 Output Pulse Width	t_{FPW1}	117	122	127	ns	C_L = 30 pF
2	FPo1 Output Delay from the FPo1 falling edge to the output frame boundary	t_{FODF1}	56		66	ns	
3	FPo1 Output Delay from the output frame boundary to the FPo1 rising edge	t_{FODR1}	56		66	ns	
4	CKo1 Output Clock Period	t_{CKP1}	117	122	127	ns	C_L = 30 pF
5	CKo1 Output High Time	t_{CKH1}	56		66	ns	
6	CKo1 Output Low Time	t_{CKL1}	56		66	ns	
7	CKo1 Output Rise/Fall Time	t_{rCK1}, t_{fCK1}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo1 and CKo1 or FPo3 and CKo3 (8.192 MHz) Timing (Multiplied Slave Mode with more than 10 ns of jitter on CKi)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo1 Output Pulse Width	t_{FPW1}	106	122	127	ns	C_L = 30 pF
2	FPo1 Output Delay from the FPo1 falling edge to the output frame boundary	t_{FODF1}	56		66	ns	
3	FPo1 Output Delay from the output frame boundary to the FPo1 rising edge	t_{FODR1}	46		66	ns	
4	CKo1 Output Clock Period	t_{CKP1}	106	122	148	ns	C_L = 30 pF
5	CKo1 Output High Time	t_{CKH1}	46		87	ns	
6	CKo1 Output Low Time	t_{CKL1}	46		87	ns	
7	CKo1 Output Rise/Fall Time	t_{rCK1}, t_{fCK1}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

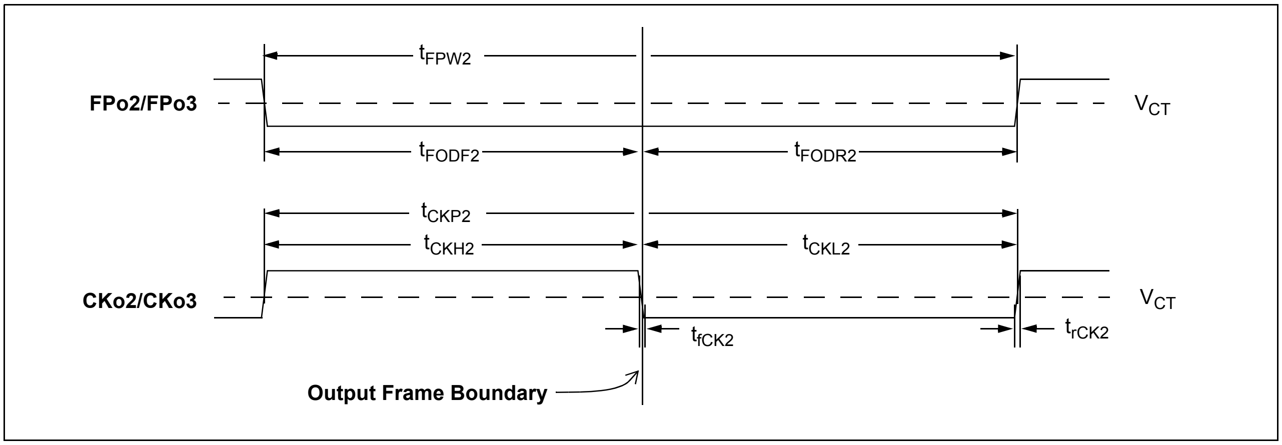


Figure 44 - FPo2 and CKo2 or FPo3 and CKo3 (16.384 MHz) Timing Diagram

AC Electrical Characteristics† - FPo2 and CKo2 or FPo3 and CKo3 (16.384 MHz) Timing (Master Mode, Divided Slave Mode, or Multiplied Slave Mode with less than 10 ns of jitter on CKi)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo2 Output Pulse Width	t_{FPW2}	56	61	66	ns	C_L = 30 pF
2	FPo2 Output Delay from the FPo2 falling edge to the output frame boundary	t_{FODF2}	25		36	ns	
3	FPo2 Output Delay from the output frame boundary to the FPo2 rising edge	t_{FODR2}	25		36	ns	
4	CKo2 Output Clock Period	t_{CKP2}	56	61	66	ns	C_L = 30 pF
5	CKo2 Output High Time	t_{CKH2}	25		36	ns	
6	CKo2 Output Low Time	t_{CKL2}	25		36	ns	
7	CKo2 Output Rise/Fall Time	t_{rCK2}, t_{fCK2}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo2 and CKo2 or FPo3 and CKo3 (16.384 MHz) Timing (Multiplied Slave Mode with more than 10 ns of jitter on CKi)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo2 Output Pulse Width	t_{FPW2}	56	61	66	ns	C_L = 30 pF
2	FPo2 Output Delay from the FPo2 falling edge to the output frame boundary	t_{FODF2}	25		36	ns	
3	FPo2 Output Delay from the output frame boundary to the FPo2 rising edge	t_{FODR2}	25		36	ns	
4	CKo2 Output Clock Period	t_{CKP2}	47	61	76	ns	C_L = 30 pF
5	CKo2 Output High Time	t_{CKH2}	17		43	ns	
6	CKo2 Output Low Time	t_{CKL2}	17		43	ns	
7	CKo2 Output Rise/Fall Time	t_{rCK2}, t_{fCK2}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

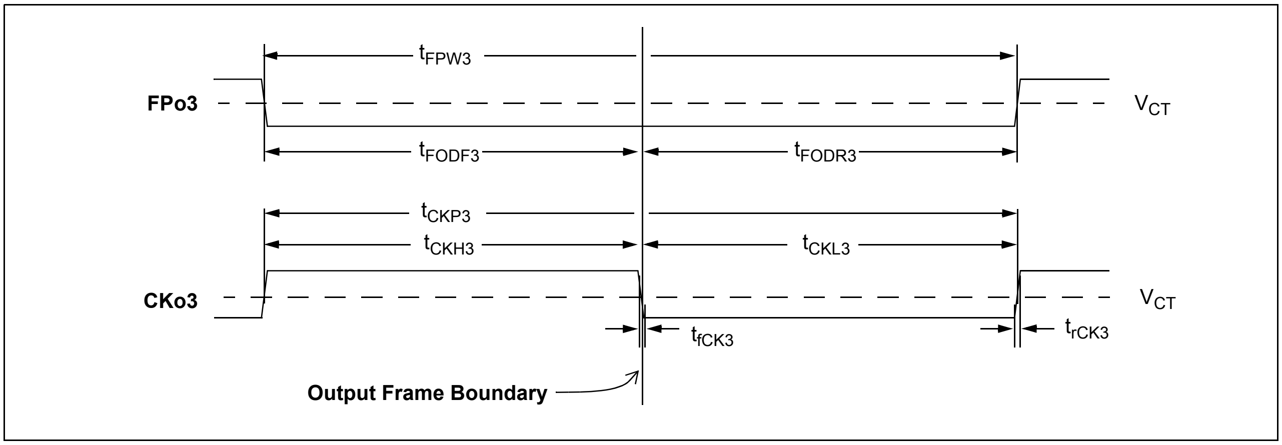


Figure 45 - FPo3 and CKo3 (32.768 MHz) Timing Diagram

AC Electrical Characteristics† - FPo3 and CKo3 (32.768 MHz) Timing (Master Mode, Divided Slave Mode, or Multiplied Slave Mode with less than 10 ns of jitter on CKi)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo3 Output Pulse Width	t_{FPW3}	27	30.5	34	ns	C_L = 30 pF
2	FPo3 Output Delay from the FPo3 falling edge to the output frame boundary	t_{FODF3}	10		18	ns	
3	FPo3 Output Delay from the output frame boundary to the FPo3 rising edge	t_{FODR3}	12		21	ns	
4	CKo3 Output Clock Period	t_{CKP3}	27	30.5	34	ns	C_L = 30 pF
5	CKo3 Output High Time	t_{CKH3}	12		19	ns	
6	CKo3 Output Low Time	t_{CKL3}	12		19	ns	
7	CKo3 Output Rise/Fall Time	t_{rCK3}, t_{fCK3}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo3 and CKo3 (32.768 MHz) Timing (Multiplied Slave Mode with more than 10 ns of jitter on CKi

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo3 Output Pulse Width	t_{FPW3}	27	30.5	34	ns	C_L = 30 pF
2	FPo3 Output Delay from the FPo3 falling edge to the output frame boundary	t_{FODF3}	12		19	ns	
3	FPo3 Output Delay from the output frame boundary to the FPo3 rising edge	t_{FODR3}	12		19	ns	
4	CKo3 Output Clock Period	t_{CKP3}	17	30.5	44	ns	C_L = 30 pF
5	CKo3 Output High Time	t_{CKH3}	5		29	ns	
6	CKo3 Output Low Time	t_{CKL3}	12		18	ns	
7	CKo3 Output Rise/Fall Time	t_{rCK3}, t_{fCK3}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

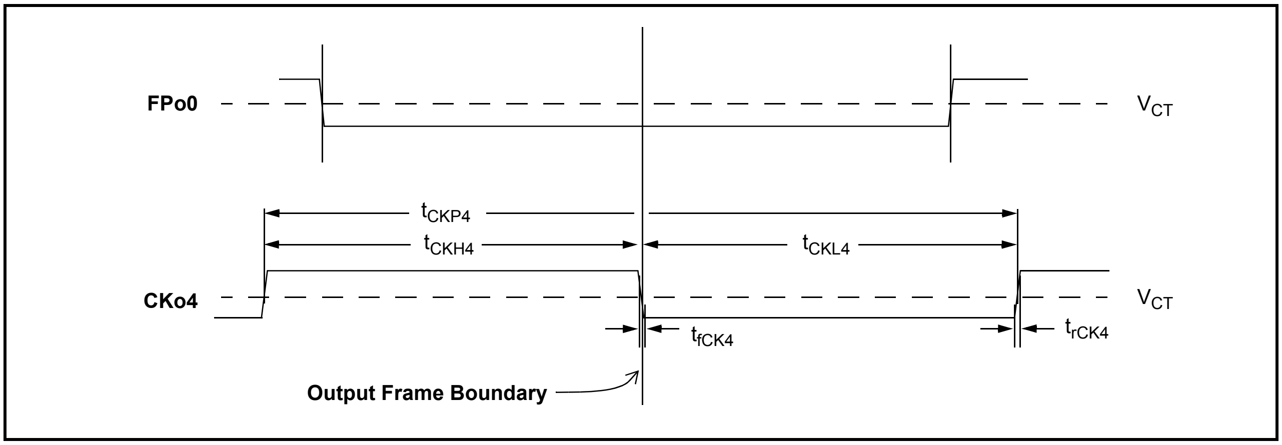


Figure 46 - FPo4 and CKo4 Timing Diagram (1.544/2.048 MHz)

AC Electrical Characteristics† - CKo4 (1.544 MHz) Timing (Only when DPLL is active)

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	CKo4 Output Clock Period	t_{CKP4}	645		650	ns	C_L = 30 pF
2	CKo4 Output High Time	t_{CKH4}	320		327	ns	
3	CKo4 Output Low Time	t_{CKL4}	320		327	ns	
4	CKo4 Output Rise/Fall Time	t_{rCK4}, t_{fCK4}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - CKo4 (2.048 MHz) Timing (Only when DPLL is active)

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	CKo4 Output Clock Period	t_{CKP4}	485		492	ns	C_L = 30 pF
2	CKo4 Output High Time	t_{CKH4}	241		247	ns	
3	CKo4 Output Low Time	t_{CKL4}	241		247	ns	
4	CKo4 Output Rise/Fall Time	t_{rCK4}, t_{fCK4}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

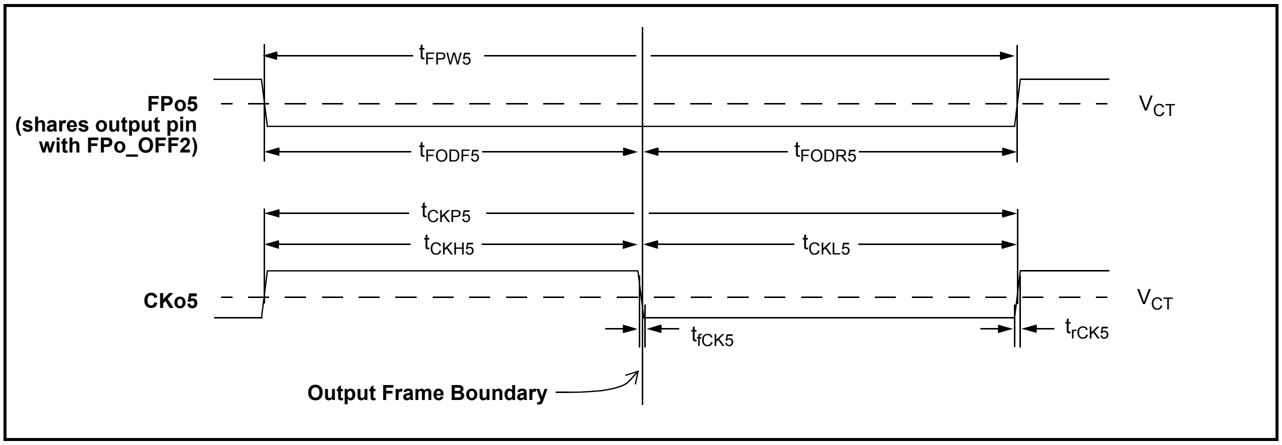


Figure 47 - CKo5 Timing Diagram

AC Electrical Characteristics† - CKo5 (19.44 MHz) Timing (Only when DPLL is active)

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	FPo5 Output Pulse Width	t_{FPW5}	49		55	ns	C_L = 30 pF
2	FPo5 Output Delay from the FPo5 falling edge to the output frame boundary	t_{FODF5}	22		28	ns	
3	FPo5 Output Delay from the output frame boundary to the FPo5 rising edge	t_{FODR5}	21		32	ns	
4	CKo5 Output Clock Period	t_{CKP5}	50		53	ns	
5	CKo5 Output High Time	t_{CKH5}	23		27	ns	
6	CKo5 Output Low Time	t_{CKL5}	24		28	ns	
7	CKo5 Output Rise/Fall Time	t_{rCK5}, t_{fCK5}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - REF0-3 Reference Input to CKo Output Timing

	Characteristic	Sym.	Min.	Max.	Units	Notes‡
1	Minimum input pulse width high or low	t_{RPMIN}	16		ns	1,2,3,16
2	Input rise or fall time	$t_{IR,(or}$ $t_{IF)}$		5	ns	
3	Input to CKo0 output delay (no input jitter) with reference	t_{RD}			ns	
	8k, 2M, 4M, 8M and 16 MHz		-7	0		
	1.544 MHz		6	15		
	19.44 MHz		-10	-2		

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ See “Performance Characteristics Notes” on page 133

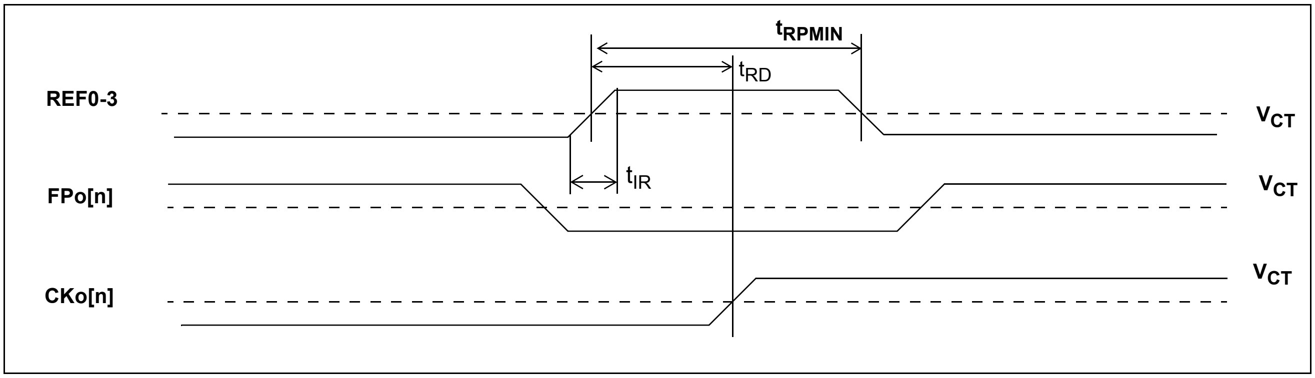


Figure 48 - REF0 - 3 Reference Input/Output Timing

AC Electrical Characteristics† - Master Mode Output Timing

	Characteristic	Sym.	Min.	Max.	Units	Notes‡
1	CKo0 to CKo1 (8.192 MHz) delay	t_{C1D}	-1	2	ns	1-5,16
2	CKo0 to CKo2 (16.384 MHz) delay	t_{C2D}	-1	3	ns	
3	CKo0 to CKo3 (32.768 MHz/16.384 MHz/8.192 MHz/4.096 MHz) delay	t_{C3D}	-4	0	ns	
4	CKo0 to CKo4 delay 2.048 MHz 1.544 MHz	t_{C4D}	 -2 -12	 3 7	ns	
5	CKo0 to CKo5 (19.44 MHz) delay	t_{C5D}	6	12	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ See “Performance Characteristics Notes” on page 133

AC Electrical Characteristics† - Divided Slave Mode Output Timing

	Characteristic	Sym.	Min.	Max.	Units	Notes‡
1	CKo0 to CKo1 (8.192 MHz) delay	t_{C1D}	-1	2	ns	1-5,16
2	CKo0 to CKo2 (16.384 MHz) delay	t_{C2D}	-1	3	ns	
3	CKo0 to CKo3 (32.768 MHz/16.384 MHz/8.192 MHz/4.096 MHz) delay	t_{C3D}	-2	2	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ See “Performance Characteristics Notes” on page 133

AC Electrical Characteristics† - Multiplied Slave Mode Output Timing

	Characteristic	Sym.	Min.	Max.	Units	Notes‡
1	CKo0 to CKo1 (8.192 MHz) delay	t_{C1D}	-1	2	ns	1-5,16
2	CKo0 to CKo2 (16.384 MHz) delay	t_{C2D}	-1	3	ns	
3	CKo0 to CKo3 (32.768 MHz/16.384 MHz/8.192 MHz/4.096 MHz) delay	t_{C3D}	-1	3	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ See “Performance Characteristics Notes” on page 133

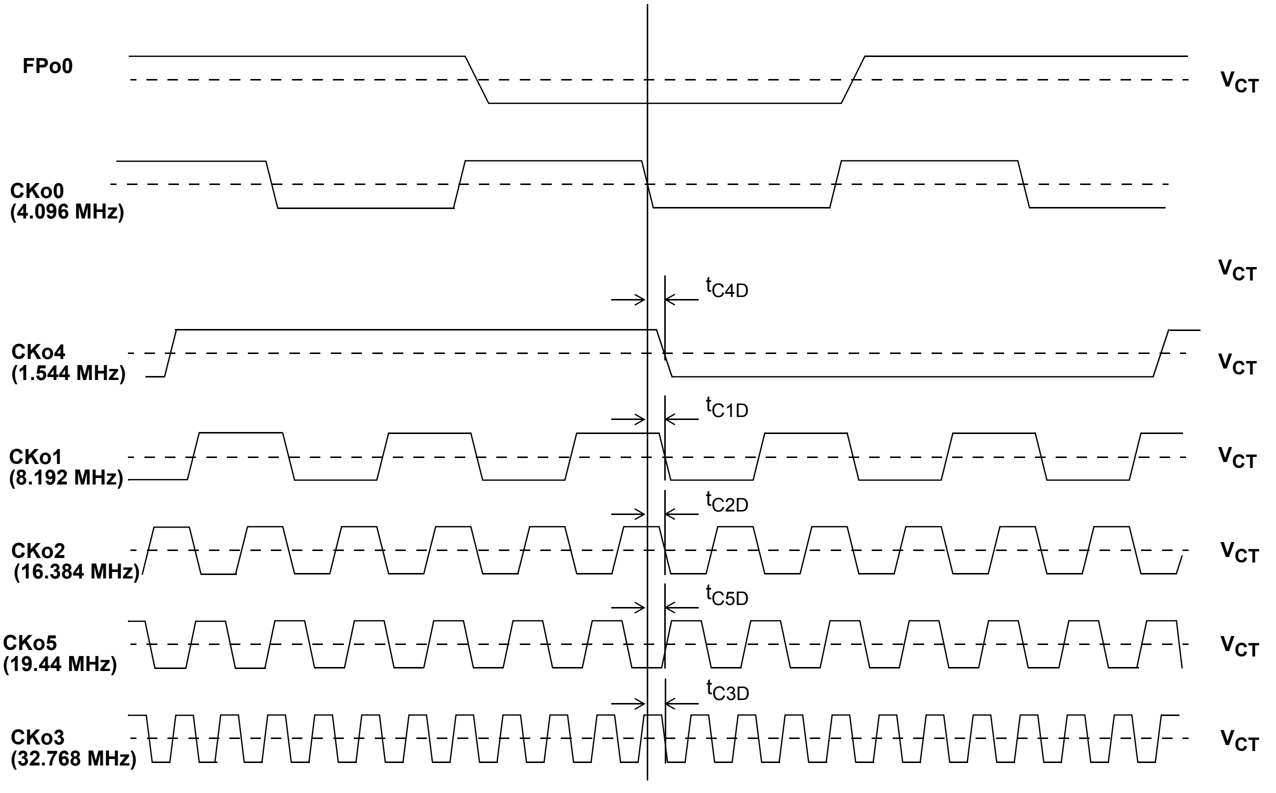


Figure 49 - Output Timing (ST-BUS Format)

DPLL Performance Characteristics† - Accuracy & Switching

	Characteristics	Min.	Max.	Units	Conditions/Notes‡
1	Freerun Mode accuracy	-0.003	0	ppm	1,5,7
2	Initial Holdover Frequency Stability	-0.03	0.03	ppm	1,4,8
3	Pull-in/Hold-in range (Stratum 3)	-20	20	ppm	1,3,7,9
4	Reference Far Hysteresis Limit (Stratum 3)	-11.4	11.4	ppm	1,3,7,9,15
5	Reference Near Hysteresis Limit (Stratum 3)	-9.8	9.8	ppm	
6	Output phase continuity for reference switch[1]		31	ns	14
7	Normal output phase alignment speed (phase slope)		56	µs/s	10
8	Normal Phase lock time[2]		60	s	1,3,7,9,10,12
9	Fast phase lock time		1	s	1,3,7,9,10,11,12

1. Reference switching to normal, holdover, or freerun mode
2. -4.6 to +4.6 ppm locking

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ See “Performance Characteristics Notes” on page 133

DPLL Performance Characteristics† - Output Jitter Generation (Unfiltered except for CKo5)

	Characteristics	Typ.‡	Units	Conditions/Notes*
1	Jitter at CKo0 and CKo3 (4.096 MHz)	810	ps-pp	1-6,16
2	Jitter at CKo1 and CKo3 (8.192 MHz)	800	ps-pp	
3	Jitter at CKo2 and CKo3 (16.384 MHz)	710	ps-pp	
4	Jitter at CKo3 (4.096, 8.192, 16.384, or 32.768 MHz)	670	ps-pp	
5	Jitter at CKo4 (1.544 MHz or 2.048 MHz) 1.544 MHz 2.048 MHz	 1060 630	 ps-pp ps-pp	
6	Jitter at CKo5 (19.44 MHz) unfiltered jitter 500 Hz - 1.3 MHz jitter 65 kHz - 1.3 MHz jitter 12 kHz - 1.3 MHz jitter	 770 540 460 510	 ps-pp ps-pp ps-pp ps-pp	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* See “Performance Characteristics Notes” on page 133.

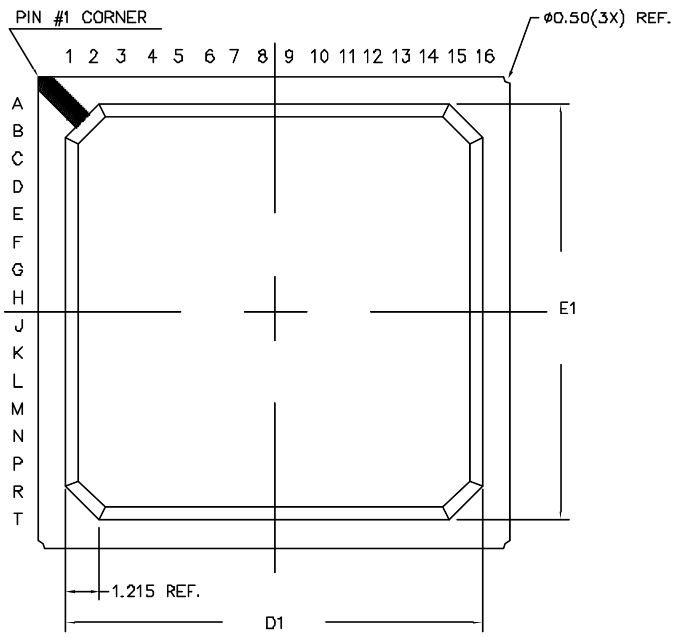
Performance Characteristics Notes

† Characteristics are over recommended operating conditions unless otherwise stated.

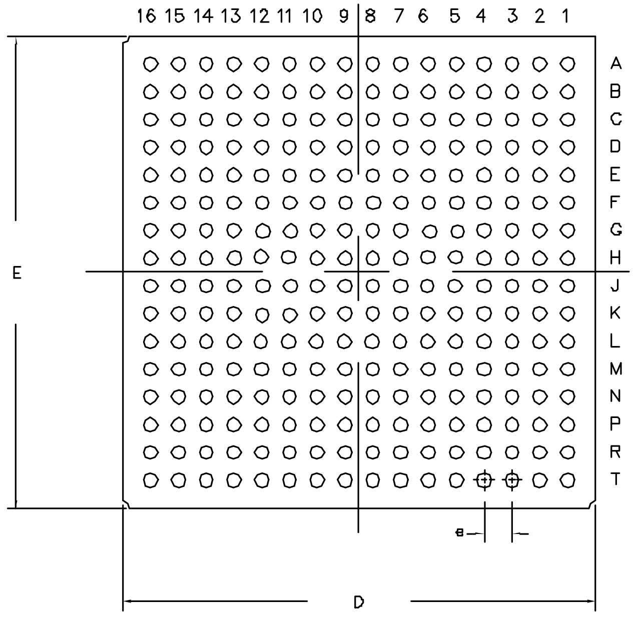
‡ Typical figures are at 25°C, V_{DD_CORE} at 1. 8 V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

1. Jitter on master clock input (XIN) is 100 ps pp or less.
2. Jitter on reference input (REF0-3) is 2 ns pp or less.
3. Normal Mode selected.
4. Holdover Mode selected.
5. Freerun Mode selected.
6. Jitter is measured without an output filter.
7. Accuracy of master clock input (XIN) is 0 ppm.
8. Accuracy of master clock input (XIN) is 100 ppm.
9. Capture range is programmed to +/-20 ppm; inaccuracy of XIN shifts this range.
10. Phase alignment speed (phase slope) is programmed to 7 ns/125 µs.
11. Fast lock is enabled.
12. Low pass filter is programmed to 1.9 Hz.
13. Applies to all programmable low pass filter selections of 1.9 Hz and above.
14. Any input reference switch or state switch (e.g.; REF0 to REF3, Normal to Holdover, etc.).
15. Multi-period near limits and far limits are programmed to 9.913 ppm & 11.287 ppm respectively.
16. 30 pF load on output pin.

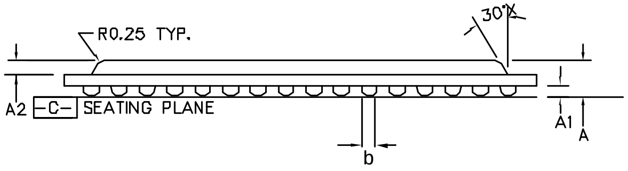
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	1.42	1.80
A1	0.30	0.50
A2	0.85 REF	
D	16.80	17.20
D1	14.80	15.20
E	16.80	17.20
E1	14.80	15.20
b	0.40	0.60
e	1.00	
N	256	
Conforms to JEDEC MS-034		



SIDE VIEW

NOTES:-

1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crov
   of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.

ISSUE	1			
ACN	214440			
DATE	26June03			
APPRD.				

ZARLINK SEMICONDUCTOR

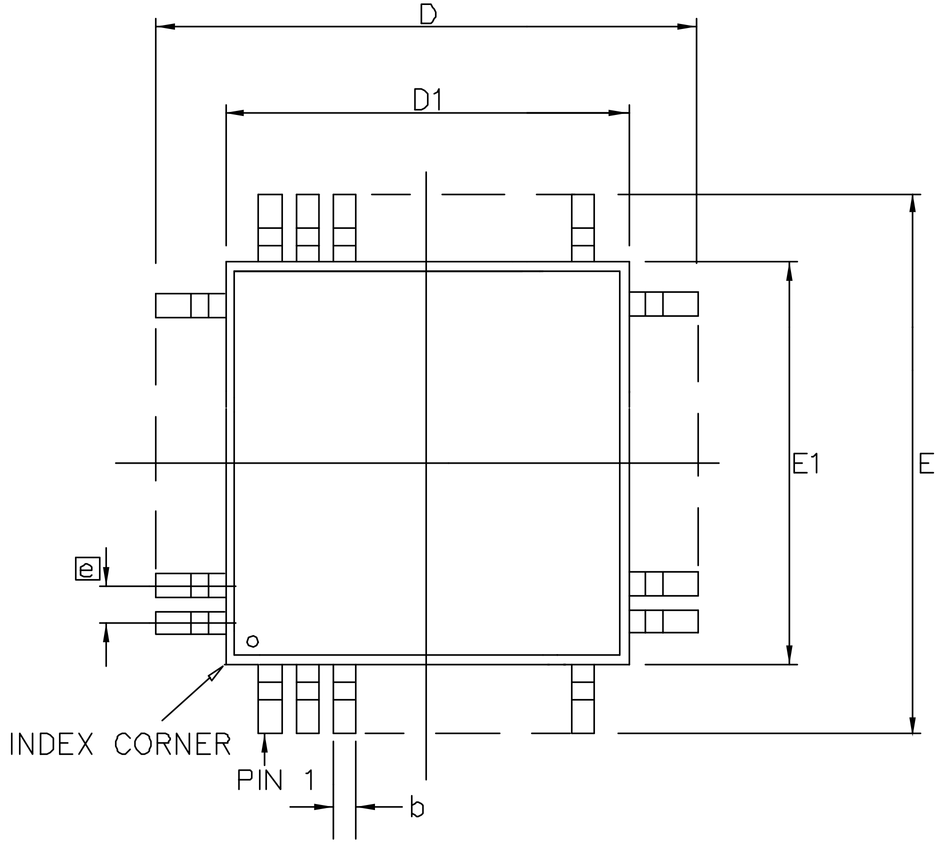
Previous package codes

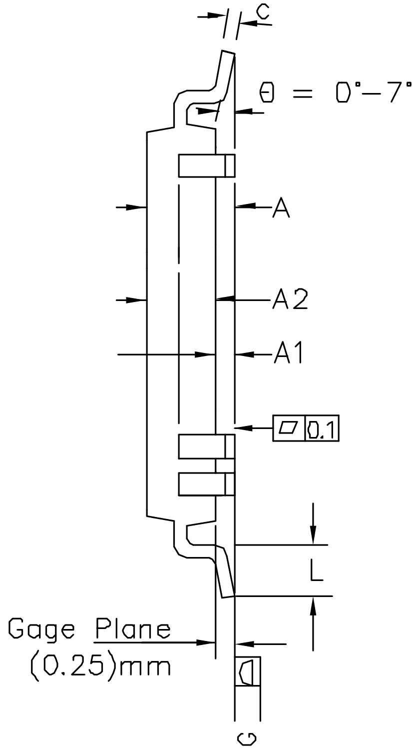
BP/G

Package Code GA

Package Outline for
256ball BGA
17x17x1.61mm

GPD00842





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	—	1.60		—	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	30.00 BSC			1.181 BSC	
D1	28.00 BSC			1.102 BSC	
E	30.00 BSC			1.181 BSC	
E1	28.00 BSC			1.102 BSC	
L	0.45	0.75		0.018	0.029
e	0.40 BSC			0.016 BSC	
b	0.13	0.23		0.005	0.009
c	0.09	0.20		0.003	0.008
	Pin features				
N	256				
ND	64				
NE	64				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BJC Iss. D

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both, located within a zone of dimension E1/4 x D1/4 from the index corner
2. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
3. Dimensions D1 and E1 do not include mold protrusion – allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
4. "N" is the total number of terminals
5. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package
6. Dimension b does not include Dambar protrusion.
7. Controlling Dimensions are in Millimeter
8. A1 is defined as the distance from the seating plane to the lowest point of the package body

ISSUE	1	2	3	4
ACN	214172	214382		
DATE	27Mar03	12June03		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

GP

Package Code QC

Package Outline for 256 lead
LQFP (28 x 28 x 1.4mm)
2.0mm Footprint

GPD00837

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