

# **ZXMN2088DE6** 20V Dual SOT23-6 N-channel enhancement mode MOSFET with low gate drive capability

## Summary

V <sub>(BR)DSS</sub>	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A)
	0.200 @ V <sub>GS</sub> = 4.5V	2.1
20	0.240 @ V <sub>GS</sub> = 2.5V	1.9
18 74 11	0.310 @ V <sub>GS</sub> = 1.8V	1.7



## **Description**

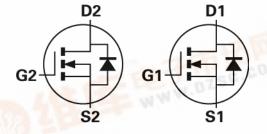
This new generation dual n-channel trench MOSFET from Zetex features low on-resistance achievable with low gate drive.

## **Features**

- Low on-resistance
- Low gate drive capability
- SOT23-6 (dual) package

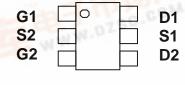
## **Applications**

- **Power Management functions**
- Disconnect switches
- Relay driving and load switching



## **Ordering information**

Device	Reel size	Tape width	Quantity
	(inches)	(mm)	per reel
ZXMN2088DE6TA	7	8	3,000



Pinout - top view

# **Device marking**

2088



**Absolute maximum ratings** 

Parameter	Symbol	Limit	Unit
Drain-Source voltage	V <sub>DSS</sub>	20	V
Gate-Source voltage	$V_{GS}$	± 8	V
Continuous Drain current @ V <sub>GS</sub> = 4.5V; T <sub>A</sub> =25°C (b) (d)	I <sub>D</sub>	2.1	Α
@ V <sub>GS</sub> = 4.5V; T <sub>A</sub> =70°C <sup>(b) (d)</sup>		1.7	
@ $V_{GS}$ = 4.5V; $T_A$ =25°C <sup>(a) (d)</sup>		1.7	
Pulsed Drain current (c)	I <sub>DM</sub>	8	А
Power dissipation at T <sub>A</sub> =25°C (a) (d)	P <sub>D</sub>	0.9	W
Linear derating factor		7.2	mW/°C
Power dissipation at T <sub>A</sub> =25°C <sup>(a) (e)</sup>	P <sub>D</sub>	1.1	W
Linear derating factor		8.8	mW/°C
Power dissipation at T <sub>A</sub> =25°C (b) (d)	P <sub>D</sub>	1.3	W
Linear derating factor		10.4	mW/°C
Operating and storage temperature range	$T_j$ , $T_{stg}$	-55 to +150	°C

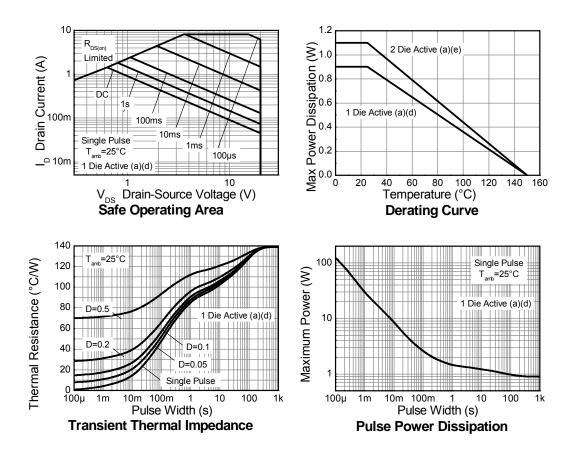
## Thermal resistance

Parameter	Symbol	Value	Unit
Junction to Ambient (a) (d)	$R_{\theta JA}$	139	°C/W
Junction to Ambient (a) (e)	$R_{\theta JA}$	113	°C/W
Junction to Ambient (b) (d)	$R_{\theta JA}$	96	°C/W

## **NOTES:**

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) As above measured at  $t \le 5$  sec.
- (c) Repetitive rating 25mm x 25mm FR4 PCB, D=0.02, pulse width 300us pulse width limited by maximum junction temperature.
- (d) For device with one active die
- (e) For device with two active die running at equal power.

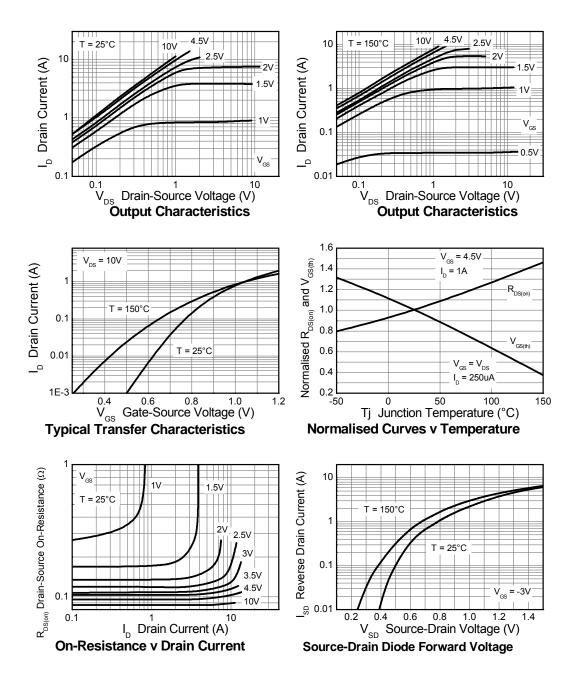
# **Thermal Characteristics**

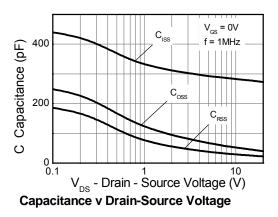


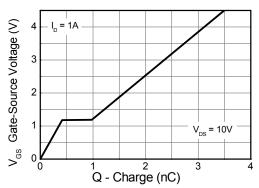
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	V <sub>(BR)DSS</sub>	20			V	I <sub>D</sub> = 250μA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>			100	nA	V <sub>DS</sub> = 3V, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>			1	μΑ	V <sub>DS</sub> = 20V, V <sub>GS</sub> =0V
Gate-Body leakage	I <sub>GSS</sub>			100	nA	V <sub>GS</sub> =±8V, V <sub>DS</sub> =0V
Gate-Source threshold voltage	$V_{GS(th)}$	0.4		1.0	V	I <sub>D</sub> = 250μA, V <sub>DS</sub> =V <sub>GS</sub>
Static Drain-Source on-state	R <sub>DS(on)</sub>		112	0.200	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 1.0A
resistance (*)			137	0.240	Ω	V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 0.6A
			165	0.310	Ω	V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 0.3A
Forward transconductance (*)(‡)	9 <sub>fs</sub>		4.6		S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1.0A
Dynamic (‡)	•		•			•
Input capacitance	C <sub>iss</sub>		279		pF	V <sub>DS</sub> = 10V, V <sub>GS</sub> =0V
Output capacitance	C <sub>oss</sub>		52		pF	f=1MHz
Reverse transfer capacitance	C <sub>rss</sub>		29		pF	
Switching (†)(‡)						
Turn-on-delay time	t <sub>d(on)</sub>		2		ns	V <sub>DD</sub> = 10V,V <sub>GS</sub> =4.5V
Rise time	t <sub>r</sub>		3.2		ns	I <sub>D</sub> = 1A
Turn-off delay time	$t_{d(off)}$		12.7		ns	$R_G \approx 6.0\Omega$
Fall time	t <sub>f</sub>		6.2		ns	
Gate Charge						
Total Gate charge	$Q_g$		3.8		nC	V <sub>DS</sub> = 10V,
Gate-Source charge	$Q_{gs}$		0.41		nC	V <sub>GS</sub> = 4.5V
Gate Drain charge	$Q_{gd}$		0.56		nC	I <sub>D</sub> = 2.4A
Source-drain diode						
Diode forward voltage (‡)	V <sub>SD</sub>		0.75	0.95	٧	T <sub>j</sub> =25°C, I <sub>S</sub> = 1.0A, V <sub>GS</sub> =0V
Reverse recovery time	t <sub>rr</sub>		6.6		ns	T <sub>j</sub> = 25°C,
Reverse recovery charge	Q <sub>rr</sub>		1.6		nC	I <sub>F</sub> = 1.24A
						di/dt = 100A/µs

**NOTES:** (\*) Measured under pulsed conditions. Pulse width  $\leq 300 \mu s$ ; duty cycle  $\leq 2\%$ . (†) Switching characteristics are independent of operating junction temperature. (‡) For design aid only, not subject to production testing.

## **Typical Characteristics**

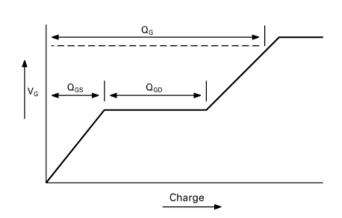






Gate-Source Voltage v Gate Charge

## **Test Circuits**



Current regulator

12V 0.2μF 50k Same as D.U.T

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V<sub>DS</sub>

V<sub>DS</sub>

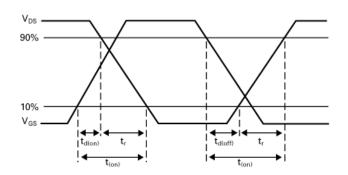
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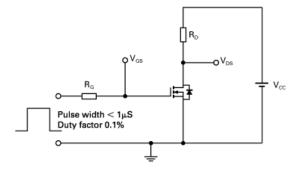
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Basic gate charge waveform

Gate charge test circuit



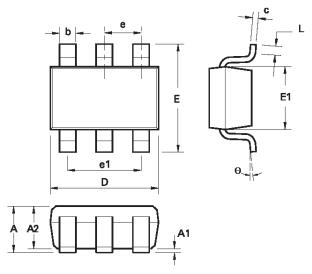


Switching time waveforms

Switching time test circuit

# Packaging details – SOT236

# Package outline



DIM	Millimeters		Inc	hes
	Min.	Max.	Min.	Max.
Α	0.90	1.45	0.354	0.0570
A1	0.00	0.15	0.00	0.0059
A2	0.90	1.30	0.0354	0.0511
b	0.35	0.50	0.0078	0.0196
С	0.09	0.26	0.0035	0.0102
D	2.70	3.10	0.1062	0.1220
E	2.20	3.20	0.0866	0.1181
E1	1.30	1.80	0.0511	0.0708
L	0.10	0.60	0.0039	0.0236
е	0.95 REF		0.037	4 REF
e1	1.90 REF		0.074	8 REF
L	0°	30°	0°	30°

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

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Production has been discontinued "Obsolete"

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