

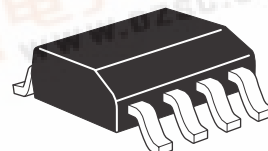


ZXMN6A11DN8

60V SO8 Dual N-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
60	0.120 @ $V_{GS} = 10V$	3.2
	0.180 @ $V_{GS} = 4.5V$	2.6



Description

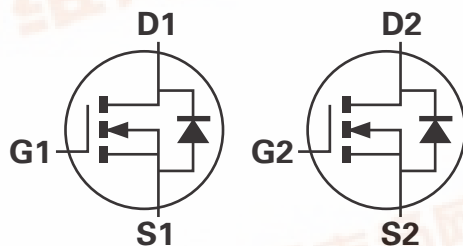
This new generation trench MOSFET from Zetex features a unique structure combining the benefits of low on-resistance and fast switching, making it ideal for high efficiency power management applications.

Features

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- Low profile SOIC package

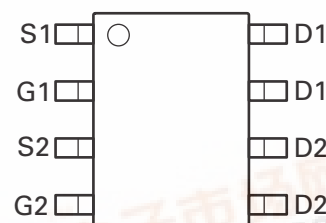
Applications

- DC-DC converters
- Power management functions
- Motor control



Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN6A11DN8TA	7	12	500



Pin out - top view

Device marking

ZXMN
6A11D

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Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current @ $V_{GS} = 10V$; $T_{amb}=25^{\circ}C^{(b)}$ @ $V_{GS} = 10V$; $T_{amb}=70^{\circ}C^{(b)}$ @ $V_{GS} = 10V$; $T_{amb}=25^{\circ}C^{(a)}$	I_D	3.2 2.6 2.5	A
Pulsed drain current ^(c)	I_{DM}	13.7	A
Continuous source current (body diode) ^(b)	I_S	3.1	A
Pulsed source current (body diode) ^(c)	I_{SM}	13.7	A
Power dissipation at $T_{amb} = 25^{\circ}C^{(a)(d)}$	P_D	1.25	W
Linear derating factor		10	mW/ $^{\circ}C$
Power dissipation at $T_{amb} = 25^{\circ}C^{(a)(e)}$	P_D	1.8	W
Linear derating factor		14	mW/ $^{\circ}C$
Power dissipation at $T_{amb} = 25^{\circ}C^{(b)(d)}$	P_D	2.1	W
Linear derating factor		17	mW/ $^{\circ}C$
Operating and storage temperature range	T_j, T_{stg}	-55 to +150	$^{\circ}C$

Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient ^{(a)(d)}	$R_{\theta JA}$	100	$^{\circ}C/W$
Junction to ambient ^{(a)(e)}	$R_{\theta JA}$	70	$^{\circ}C/W$
Junction to ambient ^{(b)(d)}	$R_{\theta JA}$	60	$^{\circ}C/W$

NOTES:

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

(b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.

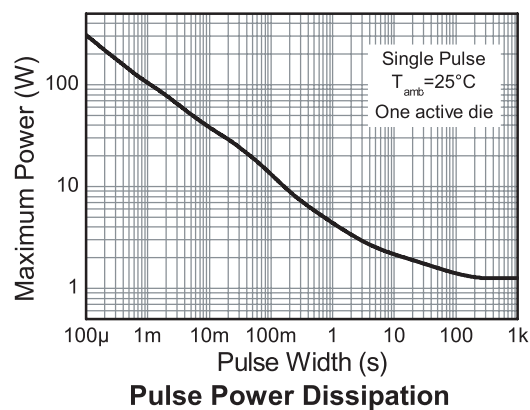
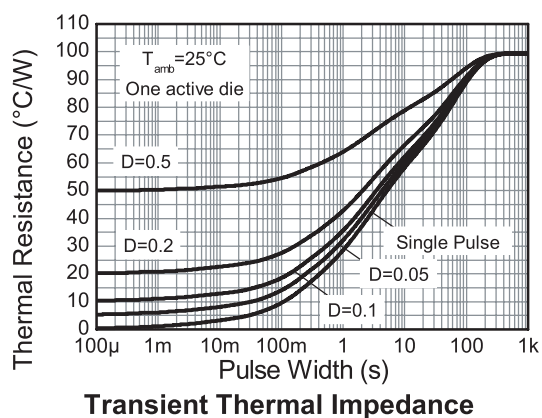
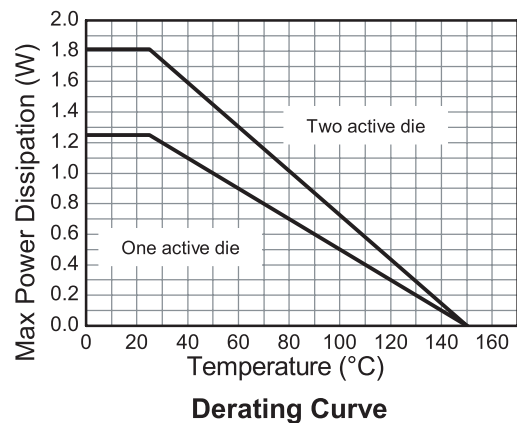
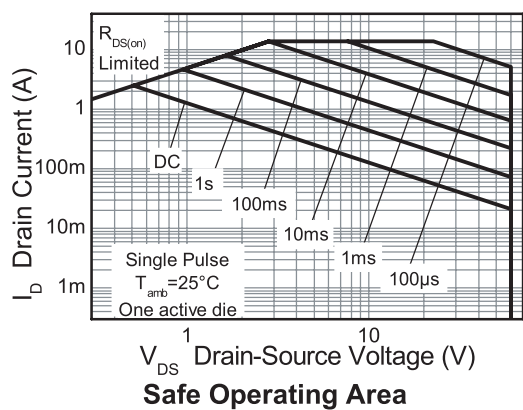
(c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300 μs - pulse width limited by maximum junction temperature.

(d) For a dual device with one active die.

(e) For a device with two active die running at equal power.

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Typical characteristics



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Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-source breakdown voltage	V _{(BR)DSS}	60			V	I _D = 250μA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}			1.0	μA	V _{DS} = 60V, V _{GS} =0V
Gate-body leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-source threshold voltage	V _{GS(th)}	1.0			V	I _D = 250μA, V _{DS} =V _{GS}
Static drain-source on-state resistance (*)	R _{DS(on)}			0.120	Ω	V _{GS} = 10V, I _D = 2.5A
				0.180	Ω	V _{GS} = 4.5V, I _D = 2A
Forward transconductance(*) (‡)	g _{fs}		4.9		S	V _{DS} = 15V, I _D = 2.5A
Dynamic(‡)						
Input capacitance	C _{iss}		330		pF	V _{DS} = 40V, V _{GS} =0V f=1MHz
Output capacitance	C _{oss}		35.2		pF	
Reverse transfer capacitance	C _{rss}		17.1		pF	
Switching (†) (‡)						
Turn-on-delay time	t _{d(on)}		1.95		ns	V _{DD} = 30V, I _D = 2.5A R _G ≈6.0Ω, V _{GS} = 10V
Rise time	t _r		3.5		ns	
Turn-off delay time	t _{d(off)}		8.2		ns	
Fall time	t _f		4.6		ns	
Gate charge	Q _g		3.0		nC	V _{DS} = 15V, V _{GS} = 5V I _D = 2.5A
Total gate charge	Q _g		5.7		nC	V _{DS} = 15V, V _{GS} = 10V I _D = 2.5A
Gate-source charge	Q _{gs}		1.25		nC	
Gate drain charge	Q _{gd}		0.86		nC	
Source-drain diode						
Diode forward voltage(*)	V _{SD}		0.85	0.95	V	T _j =25°C, I _S = 2.8A, V _{GS} =0V
Reverse recovery time(‡)	t _{rr}		21.5		ns	T _j =25°C, I _S = 2.5A, di/dt=100A/μs
Reverse recovery charge(‡)	Q _{rr}		20.5		nC	

NOTES:

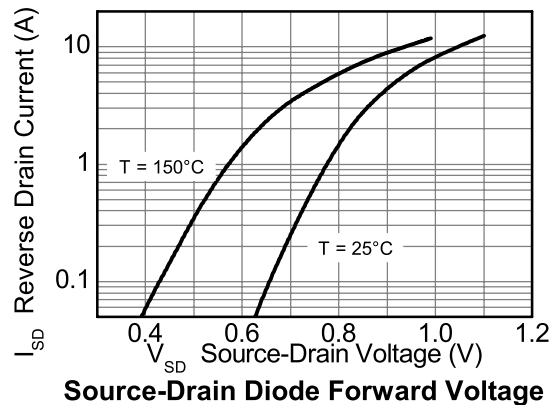
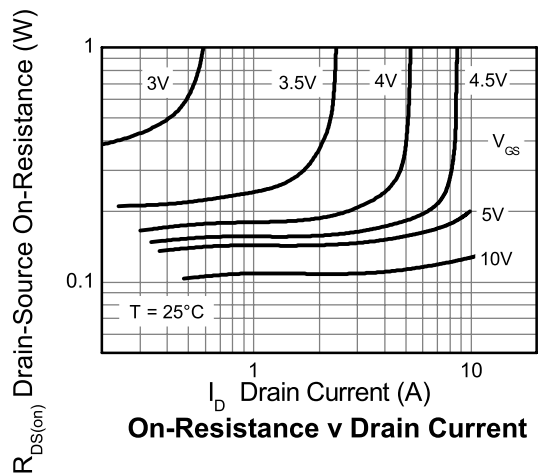
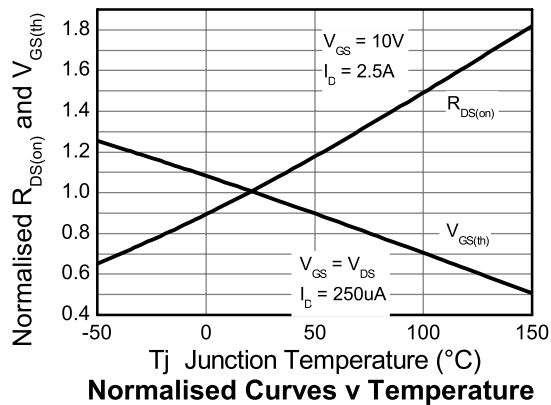
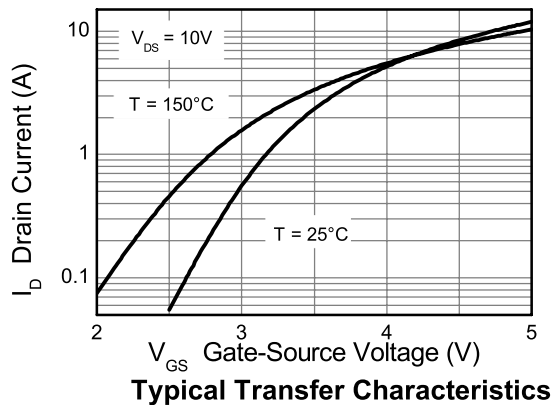
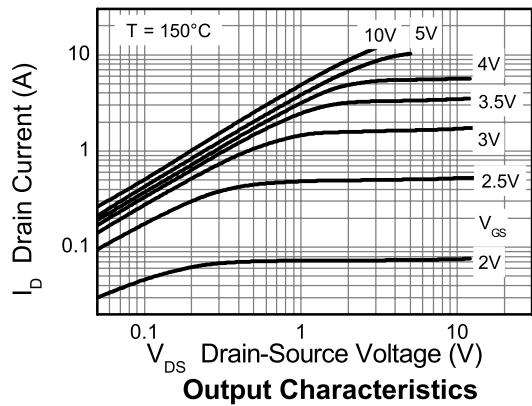
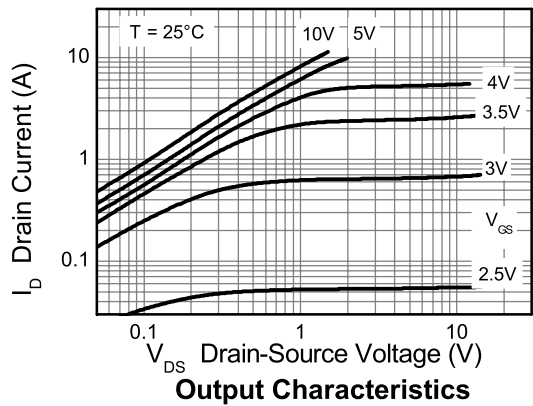
(*) Measured under pulsed conditions. Pulse width = $300\mu\text{s}$. Duty cycle $\leq 2\%$.

(†) Switching characteristics are independent of operating junction temperature.

(‡) For design aid only, not subject to production testing.

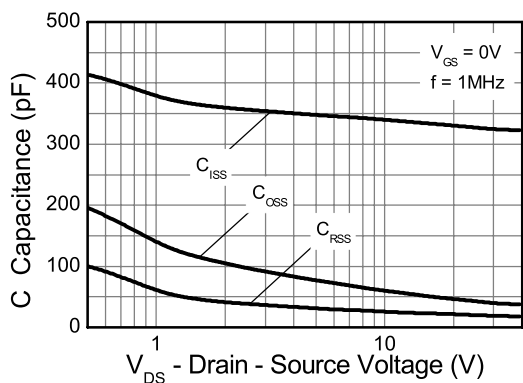
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Typical characteristics

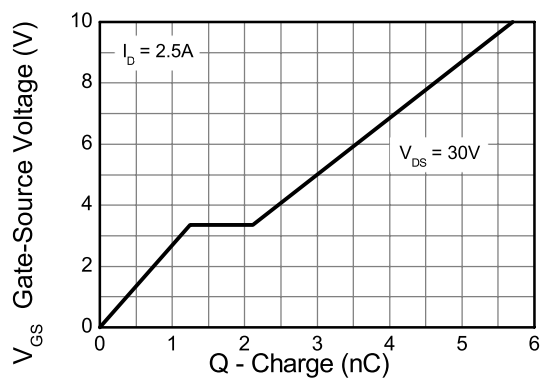


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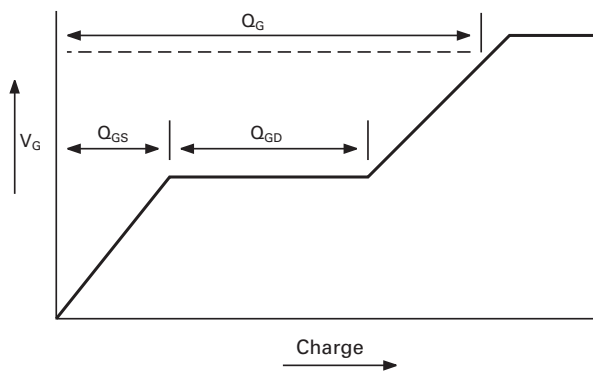
Typical characteristics



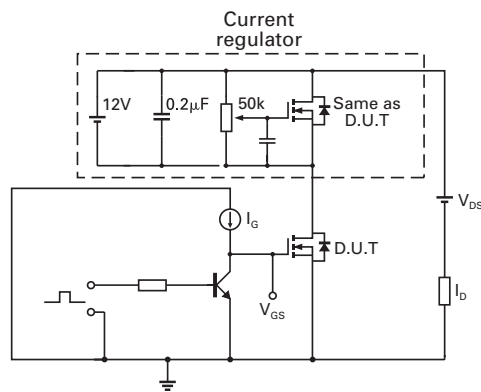
Capacitance v Drain-Source Voltage



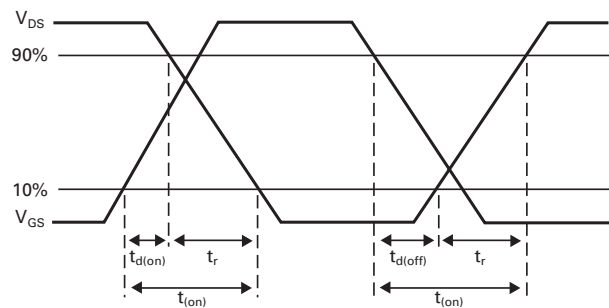
Gate-Source Voltage v Gate Charge



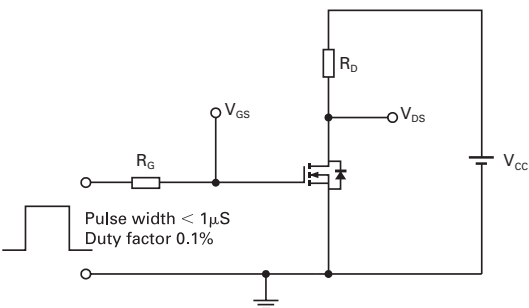
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



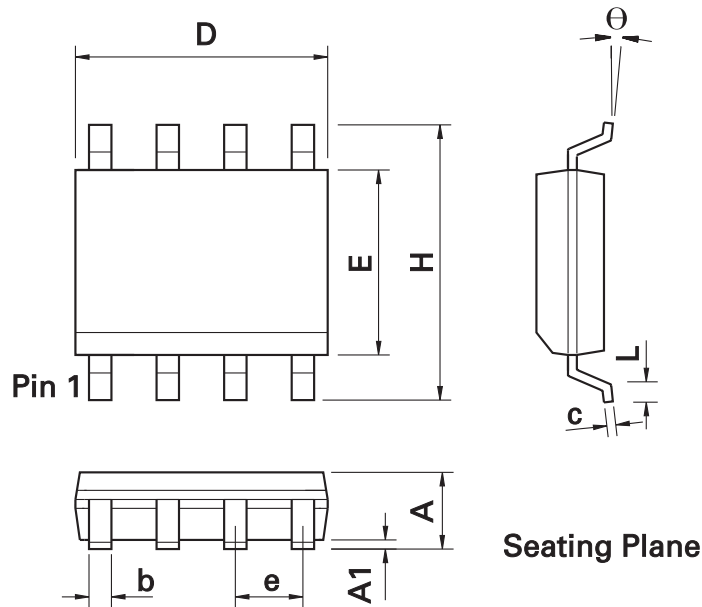
Switching time test circuit

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Package outline - S08



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	Θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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