

**Z84C13/Z84C15****Z80® CMOS EIPC ENHANCED  
INTELLIGENT PERIPHERAL CONTROLLER****GENERAL DESCRIPTION**

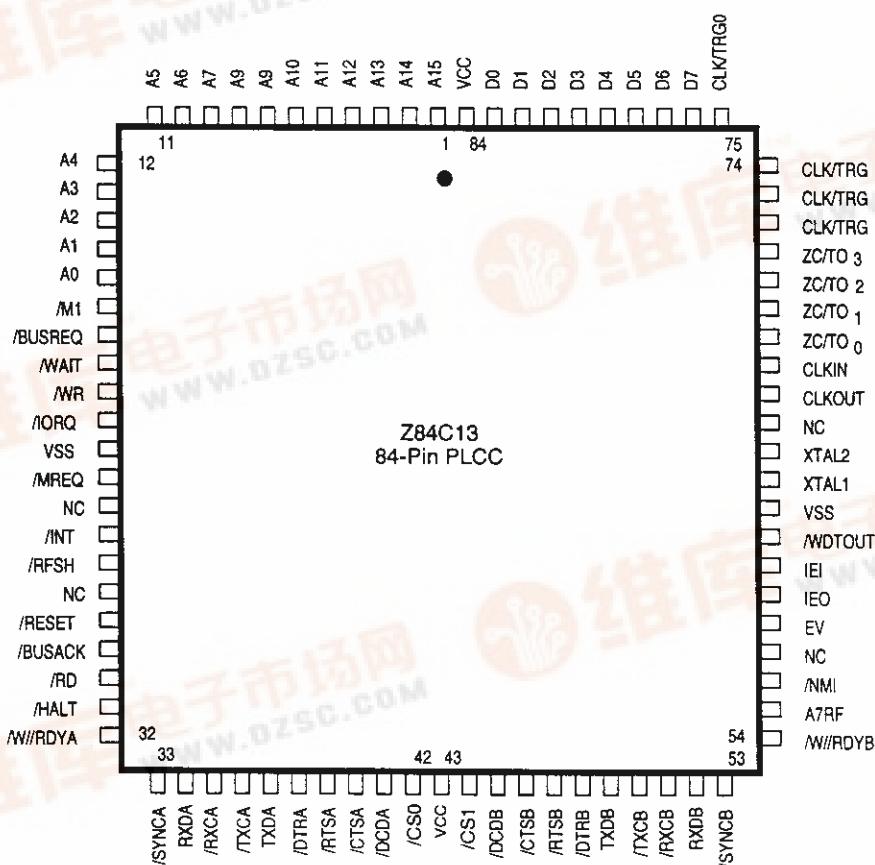
The Enhanced Intelligent Peripheral Controller (EIPC) is a series of highly superintegrated devices. The Z84C15 is a CMOS 8-bit microprocessor integrated with the CTC, SIO, CGC, WDT and the PIO into a single 100-pin Quad Flat Pack (QFP), or 100-pin Very Small Quad Flat Pack (VQFP) package. The Z84C13 is the Z84C15 without PIO, and is housed in a 84-pin PLCC package. These high-end superintegrated intelligent peripheral controllers are targeted for a broad range of applications ranging from error correcting modems to enhancement/cost reductions of existing hardware using Z80® MCU-based discrete peripherals.

**Notes:**

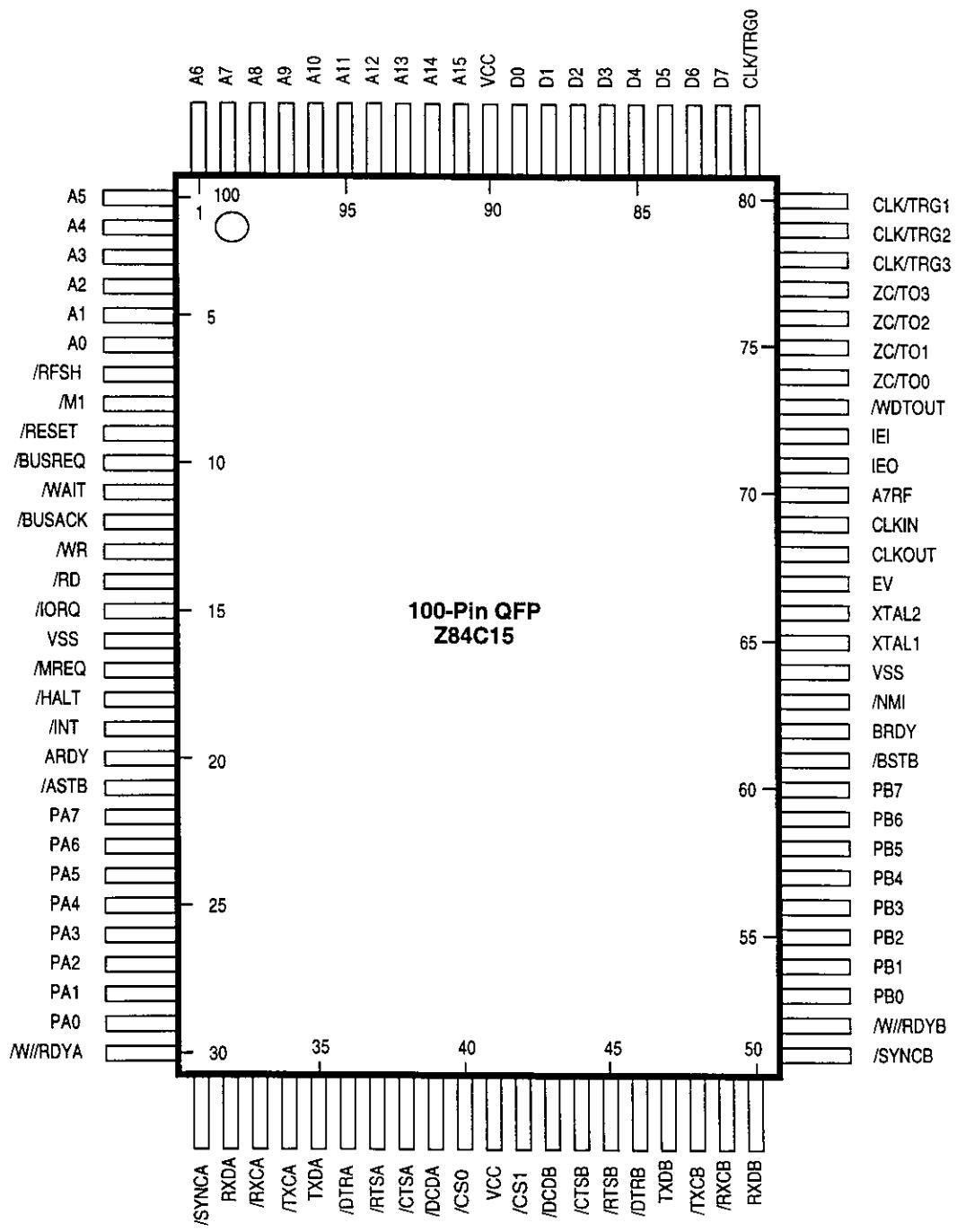
All Signals with a preceding front slash, "/", are active Low, e.g.: /B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

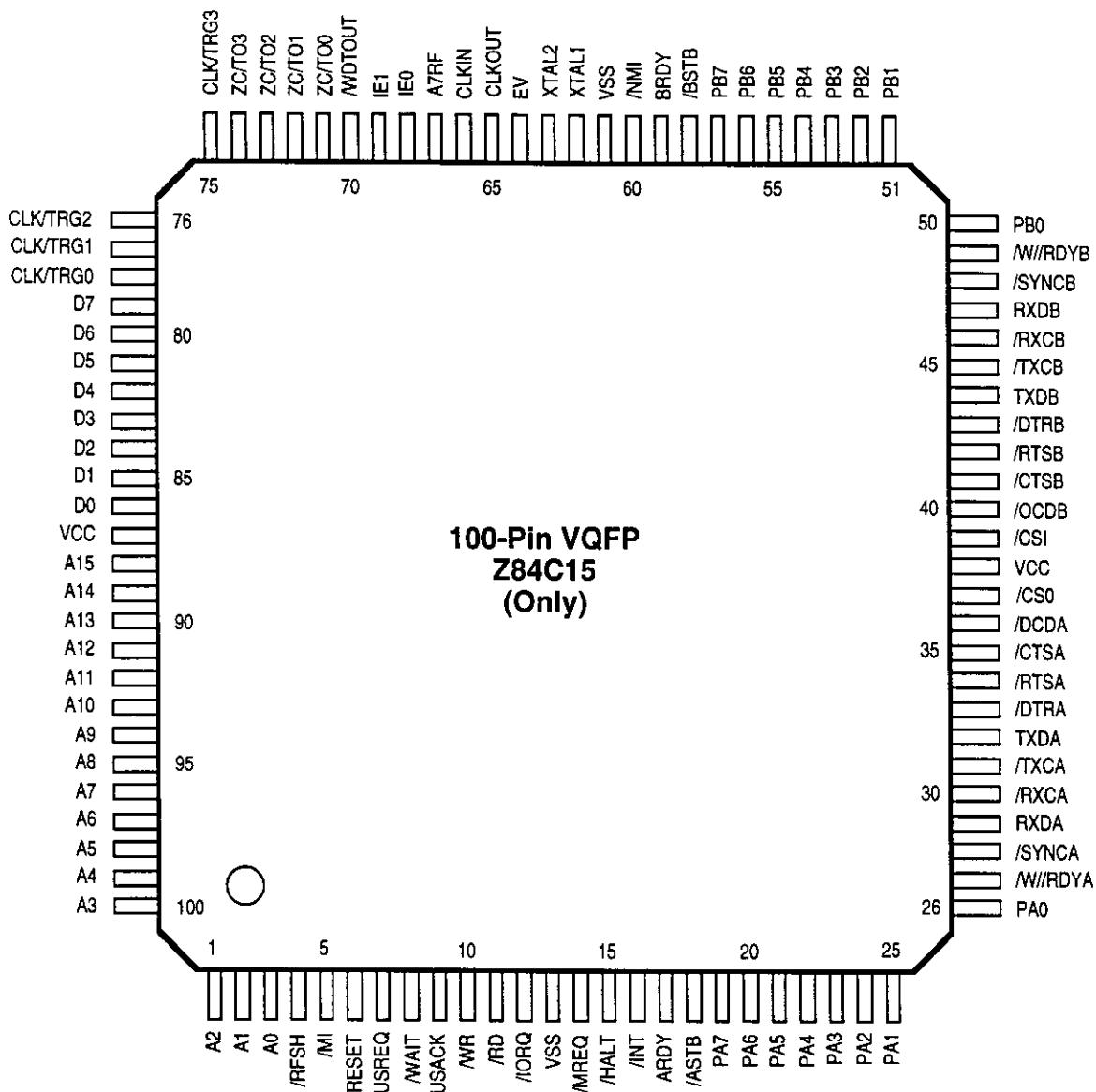
Connection	Circuit	Device
Power Ground	V <sub>cc</sub> GND	V <sub>pp</sub> V <sub>ss</sub>

**Z84C13 Pin Assignments**

## GENERAL DESCRIPTION (Continued)



Z84C15 Pin Assignments



Z84C15 Pin Assignments

## ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V <sub>CC</sub>	Supply Voltage (*)	-0.3	+7.0	V
T <sub>STG</sub>	Storage Temp	-65°	+150°	C
T <sub>A</sub>	Oper Ambient Temp	†		C

**Notes:**

\* Voltage on all pins with respect to GND.

† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Standard Test Load).

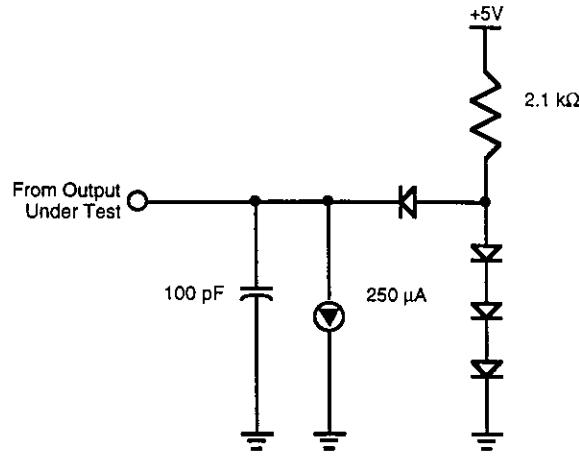
Available operating temperature ranges are:

S = 0°C to 70°C

E = -40°C to +100°C

Voltage Supply Range:  $+4.50V \leq V_{CC} \leq +5.50V$

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.



## CAPACITANCE

Guaranteed by design and characterization

Symbol	Parameter	Min	Max	Unit
C <sub>CLOCK</sub>	Clock Capacitance	35	pF	
C <sub>IN</sub>	Input Capacitance	5	pF	
C <sub>OUT</sub>	Output Capacitance	15	pF	

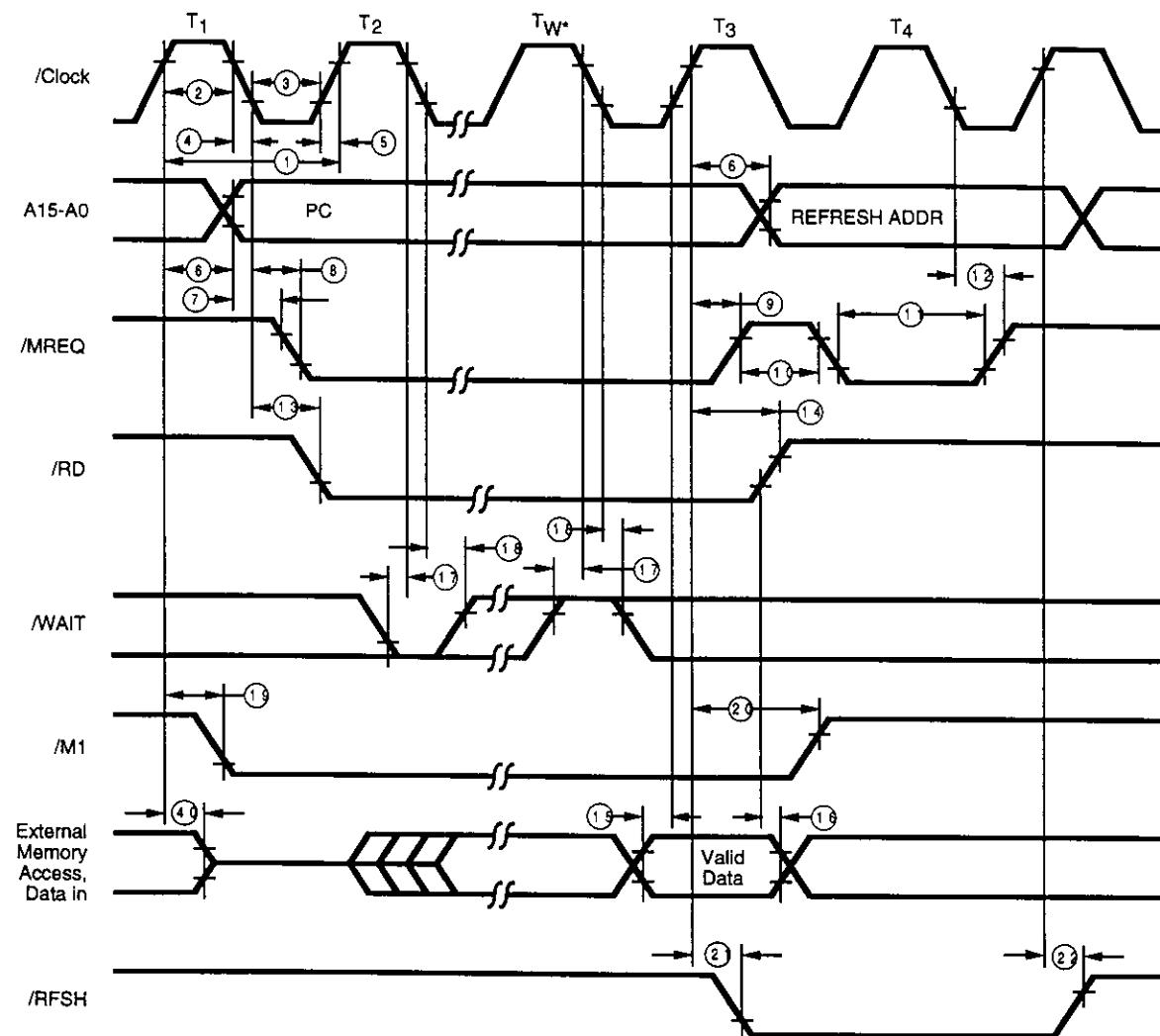
**DC CHARACTERISTICS**
 $V_{cc} = 5.0V \pm 10\%$ , unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Condition
$V_{OHC}$	Clock Output High Voltage	$V_{cc}-0.6$		V	-2.0 mA
$V_{OLC}$	Clock Output Low Voltage		0.4	V	+2.0 mA
$V_{IHC}$	Clock Input High Voltage	$V_{cc}-0.6$		V	
$V_{ILC}$	Clock Input Low Voltage		0.4	V	
$V_{IH}$	Input High Voltage	2.2	$V_{cc}$	V	
$V_{IL}$	Input Low Voltage	-0.3	0.8	V	
$V_{OL}$	Output Low Voltage		0.4 [5]	V	$I_{LO}=2.0$ mA
$V_{OH1}$	Output High Voltage	2.4		V	$I_{OH}=-1.6$ mA
$V_{OH2}$	Output High Voltage	$V_{cc}-0.8$ [5]		V	$I_{OH}=-250$ $\mu$ A
$I_{CC1}$	Power Supply Current		TBD		$V_{cc}=5V$
	XTALIN = 16 MHz				
	XTALIN = 10 MHz	50		mA	$V_{IH}=V_{cc}-0.2V$
	XTALIN = 6 MHz	30		mA	$V_{IL}=0.2V$
$I_{CC2}$	Power Supply Current (STOP Mode)	50		$\mu$ A	$V_{cc}=5V$
	Power Supply Current (IDLE1 Mode)		TBD		$V_{cc}=5V$
	XTALIN = 16 MHz				
	XTALIN = 10 MHz	6		mA	$V_{IH}=V_{cc}-0.2V$
$I_{CC3}$	XTALIN = 6 MHz	4		mA	$V_{IL}=0.2V$
	Power Supply Current (IDLE2 Mode)		TBD		$V_{cc}=5V$
	XTALIN = 16 MHz		TBD [1]	mA	$V_{IH}=V_{cc}-0.2V$
	XTALIN = 10 MHz		TBD [1]	mA	$V_{IL}=0.2V$
$I_L$	XTALIN = 6 MHz				
	Input Leakage Current	-10	10 [4]	$\mu$ A	$V_{IN}=0.4V$ to $V_{cc}$
$I_{L(SY)}$	SYNC Pin Leakage Current	-40	10	$\mu$ A	$V_{OUT}=0.4V$ to $V_{cc}$
$I_{LO}$	Tri-state Output Leakage Current in Float	-10	10 [2]	$\mu$ A	$V_{OUT}=0.4V$ to $V_{cc}$
$I_{ODD}$	Darlington Drive Current (Port B and CTC ZC/TO)	-1.5		mA	$V_{OH}=1.5V$ $REXT = 390$ Ohms

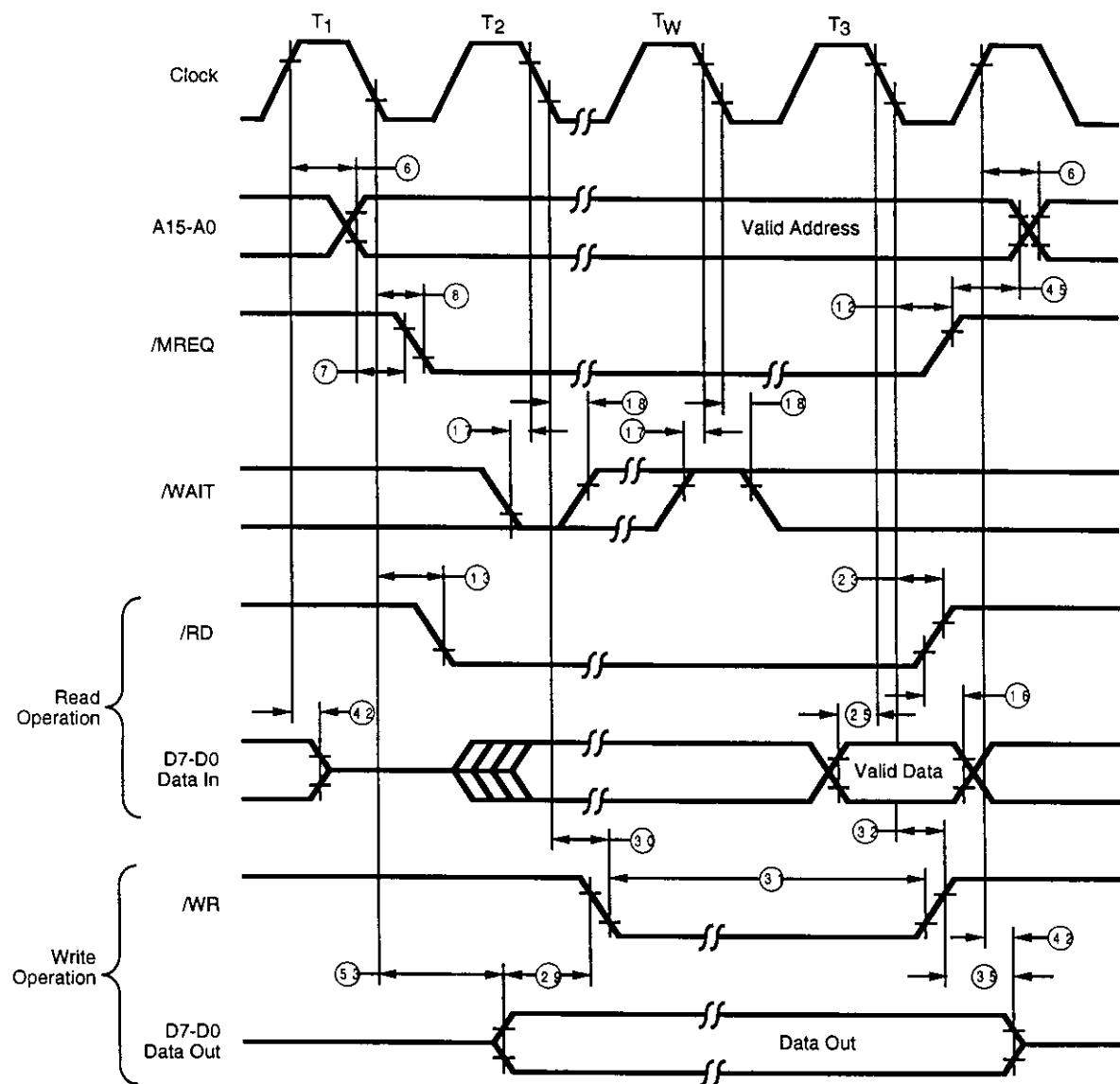
**Notes:**

- [1] Measurements made with outputs floating.
- [2] A15-A0, D7-D0, /MREQ, /IORQ, /RD and /WR.
- [3]  $I_{CC2}$  Standby current is guaranteed when the /HALT pin is Low in STOP mode.
- [4] All pins except XTAL1, where  $I_L = \pm 25$   $\mu$ A.
- [5] A15-A0, D7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /BUSACK.

## TIMING DIAGRAMS

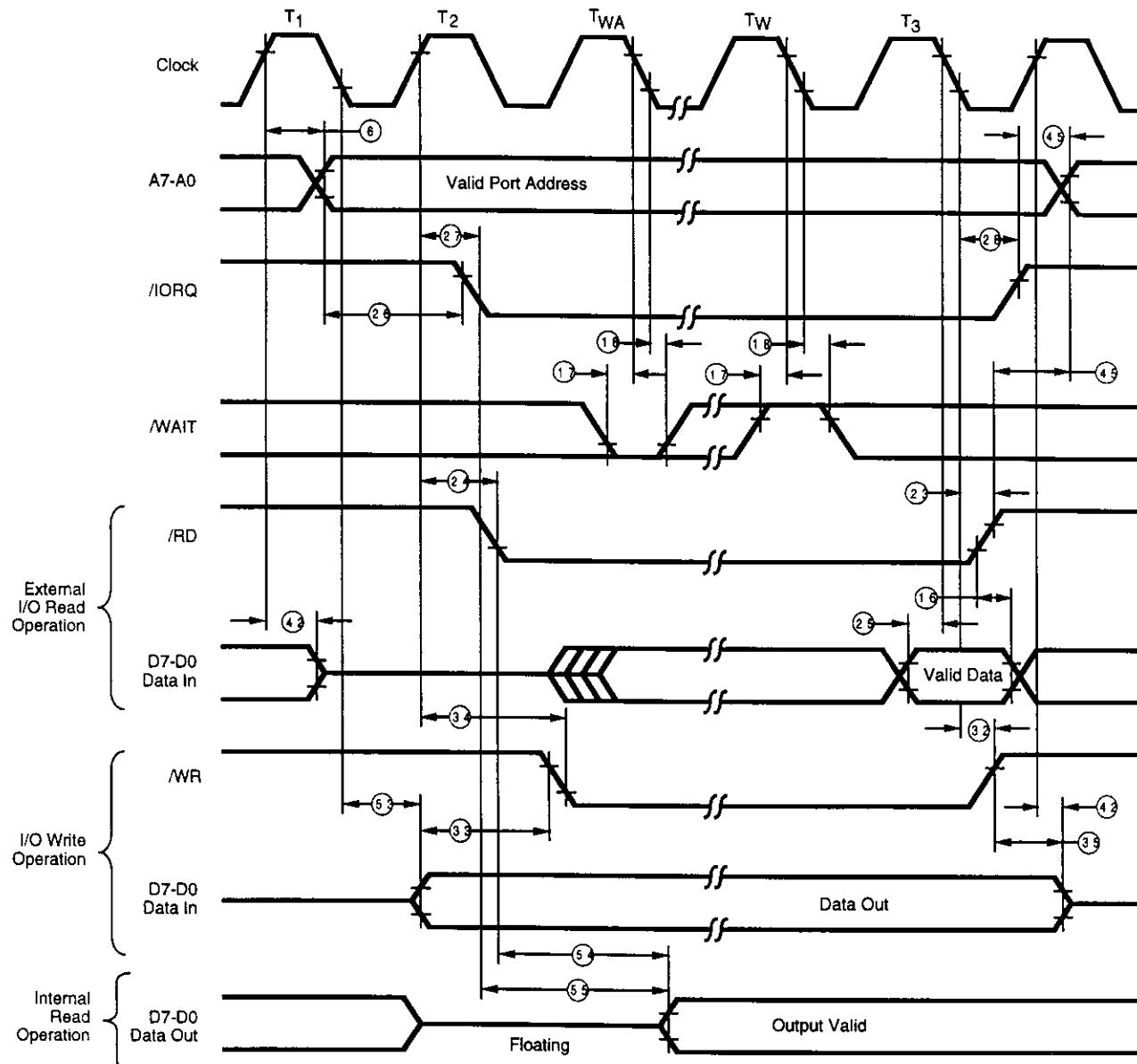


Instruction Opcode Fetch  
 (See Table A)



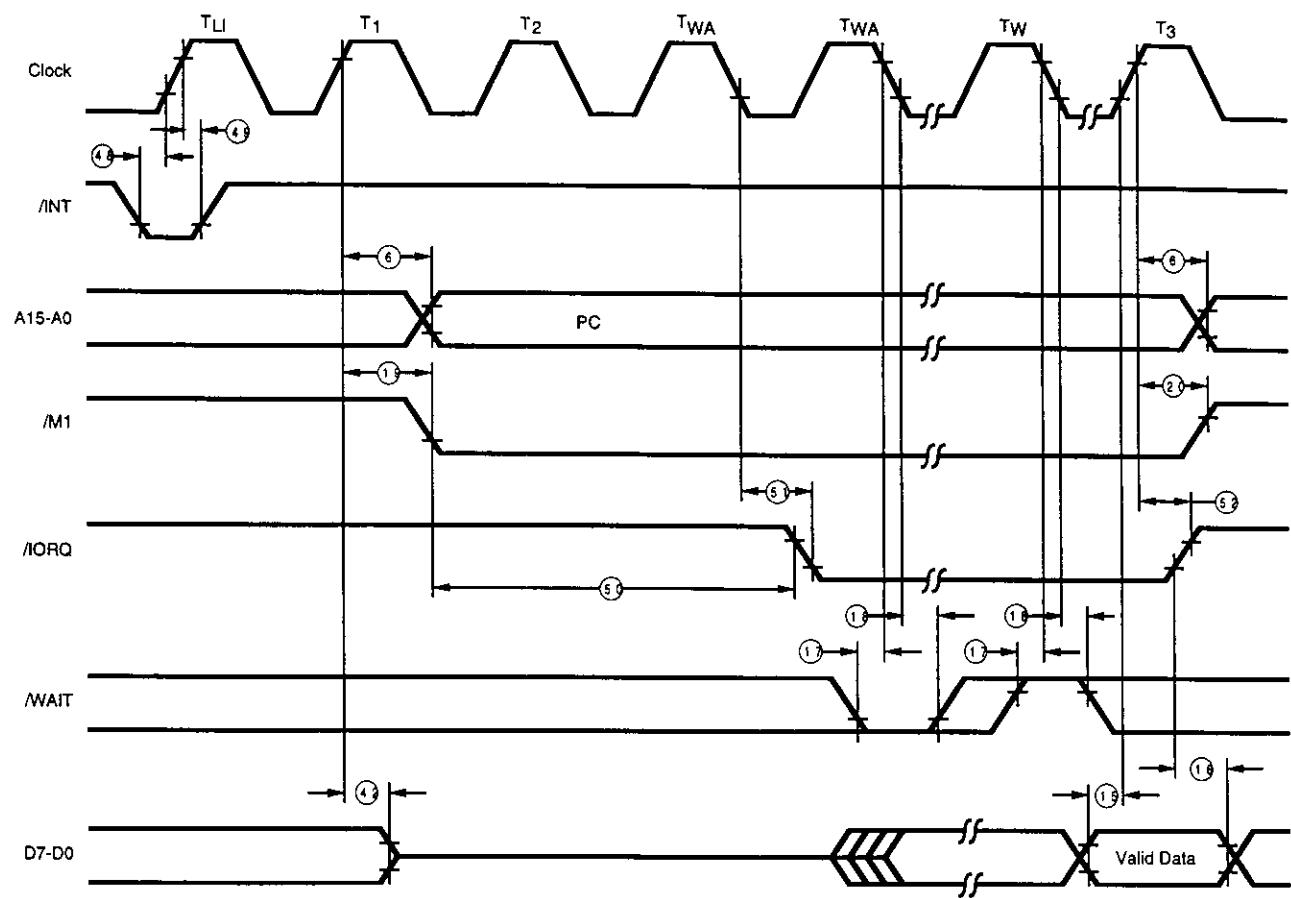
Memory Read or Write Cycle  
(See Table A)

## TIMING DIAGRAMS



Note:  $T_{WA}$  = One wait cycle automatically inserted by CPU

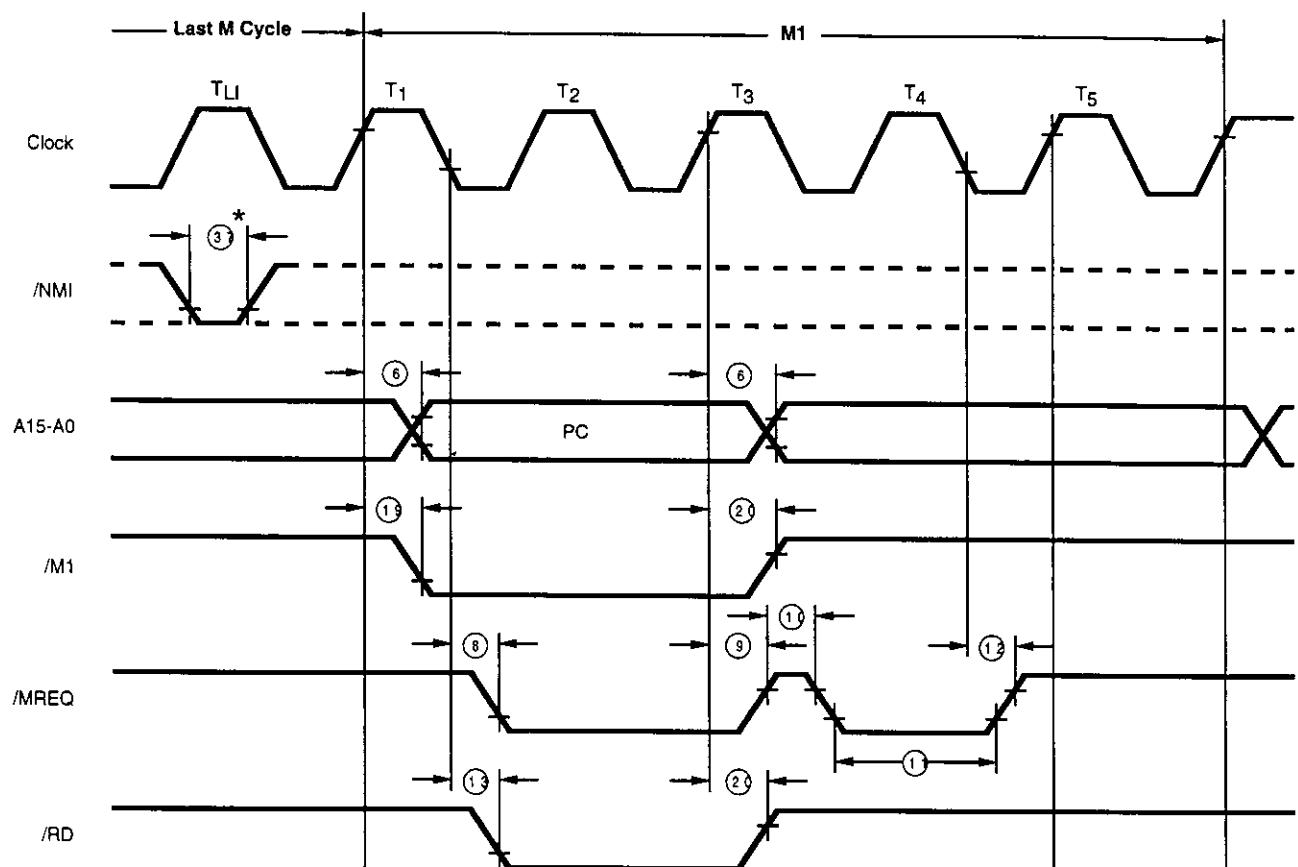
Input or Output Cycle  
 (See Table A)



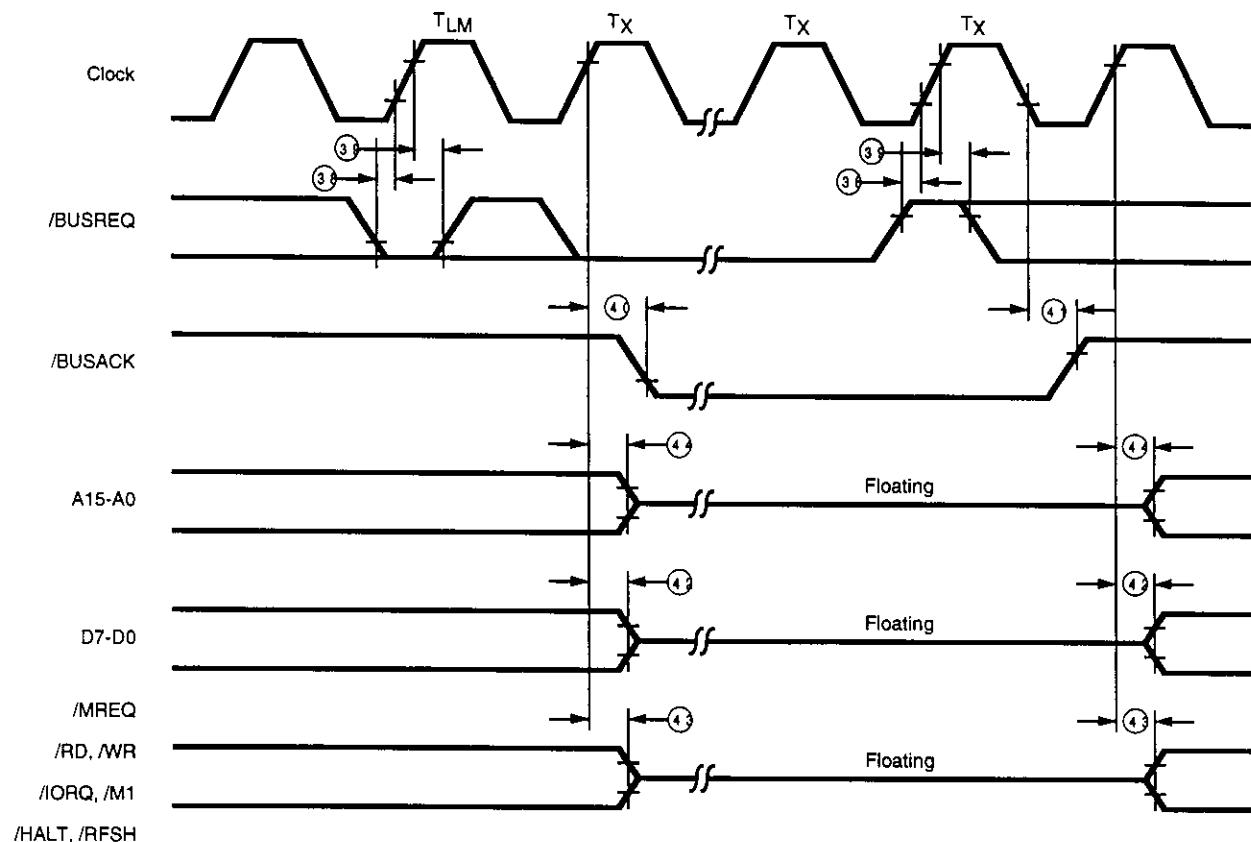
NOTE: 1)  $T_{LI}$  = Last state of any instruction cycle

2)  $T_{WA}$  = Wait cycle automatically inserted by CPU

### Interrupt Request/Acknowledge Cycle (See Table A)

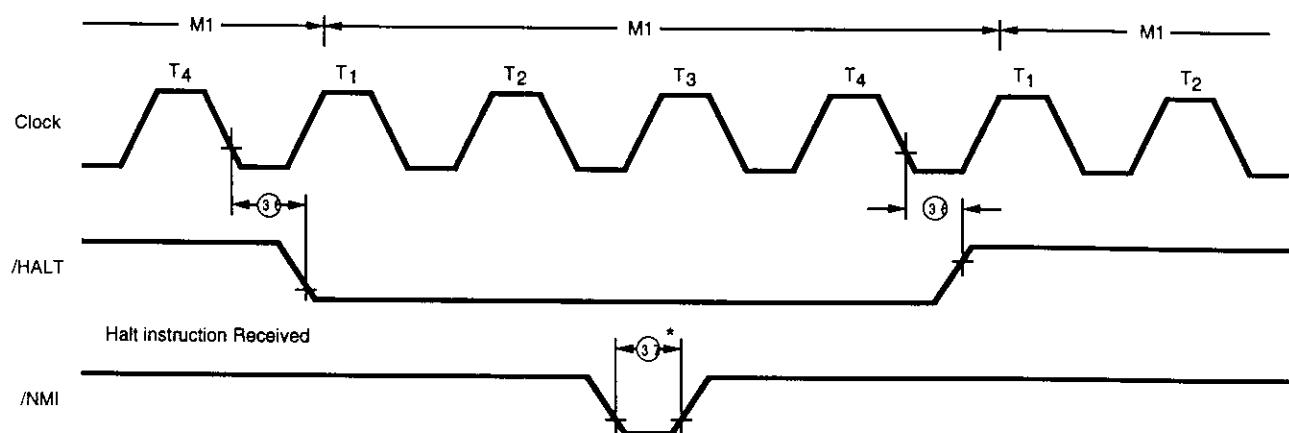
**TIMING DIAGRAMS**


**Input or Output Cycle**  
 (See Table A)



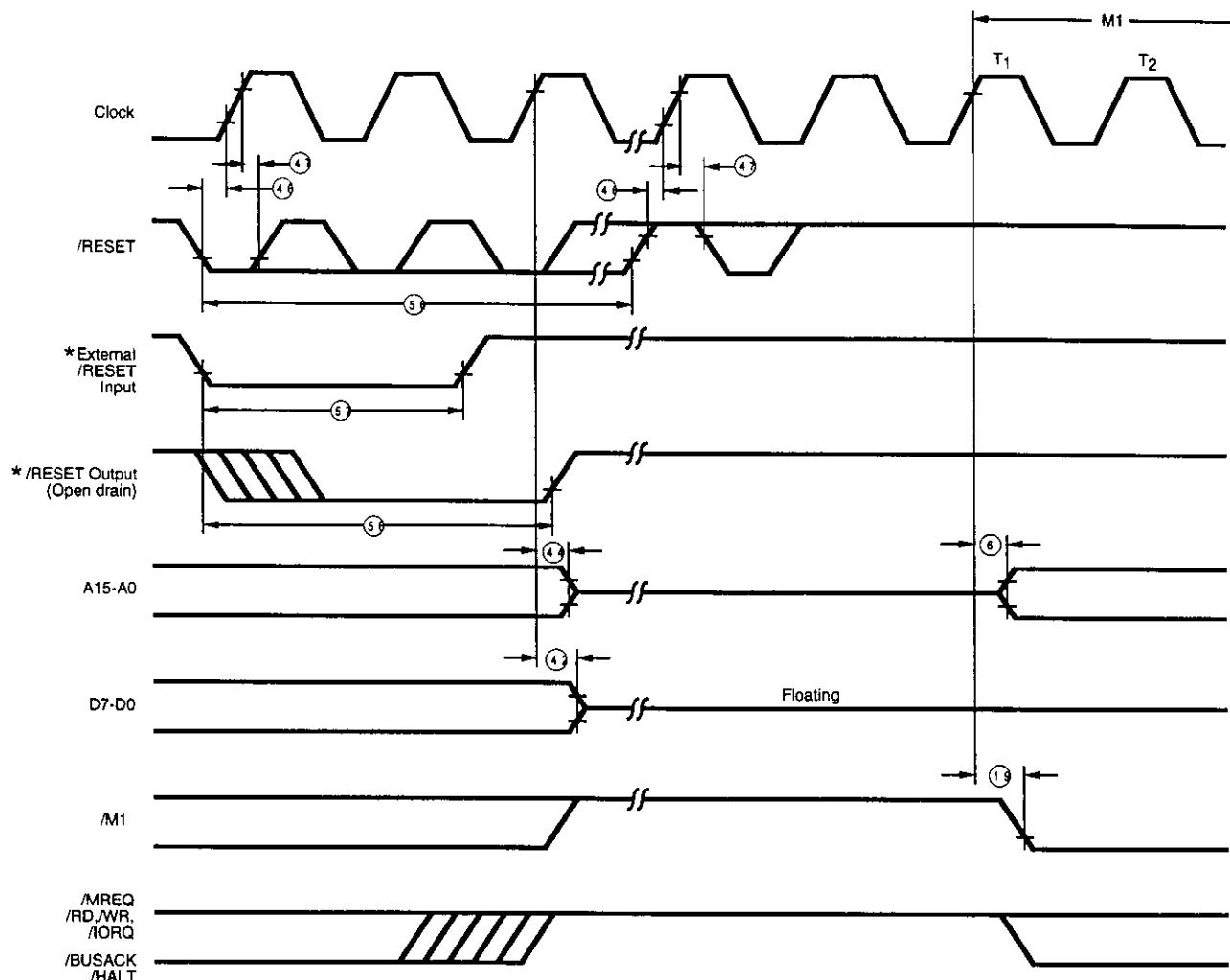
Notes: 1)  $T_{LM}$  = Last state of any M cycle  
 2)  $T_X$  = An arbitrary clock cycle used by requesting device

**Interrupt Request/Acknowledge Cycle**  
 (See Table A)

**TIMING DIAGRAMS (Continued)**

\* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMIs falling edge must occur no later than the rising edge of the clock preceding the last state of any instruction cycle (T<sub>L1</sub>).

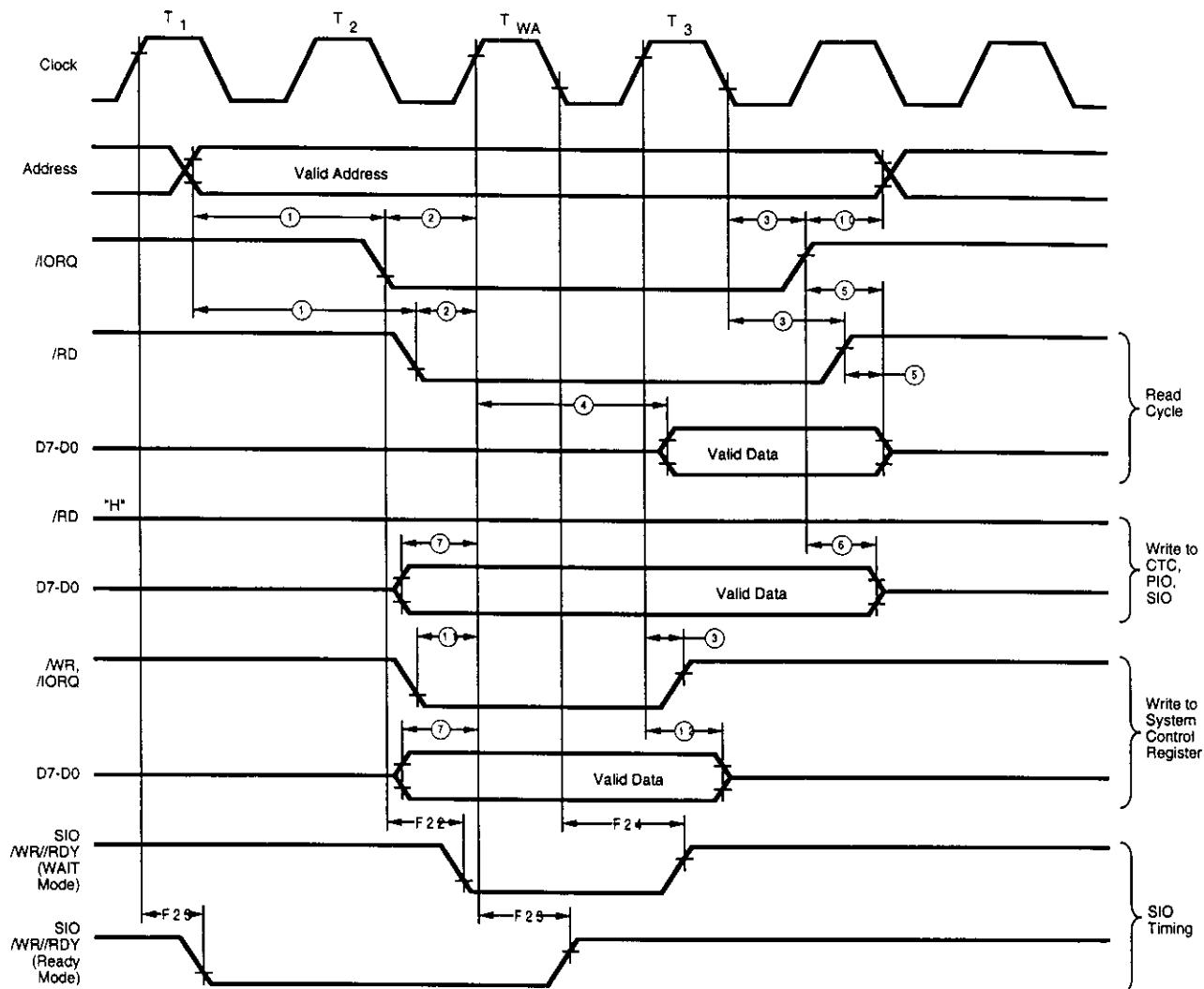
**Halt Acknowledge  
(See Table A)**

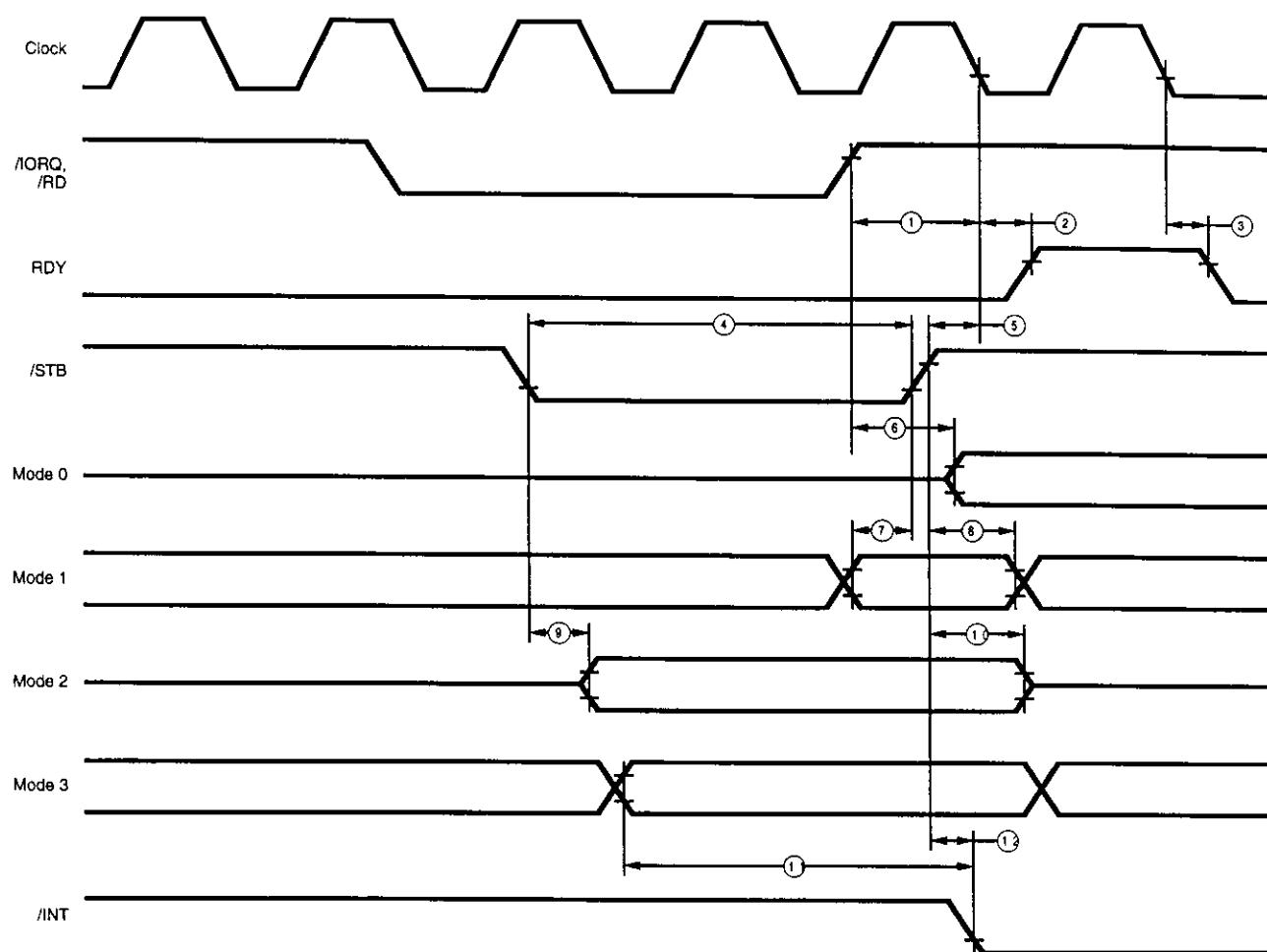


\* 84C13/C15 Only Reset Output is Enabled

### Reset Cycle (See Table A)

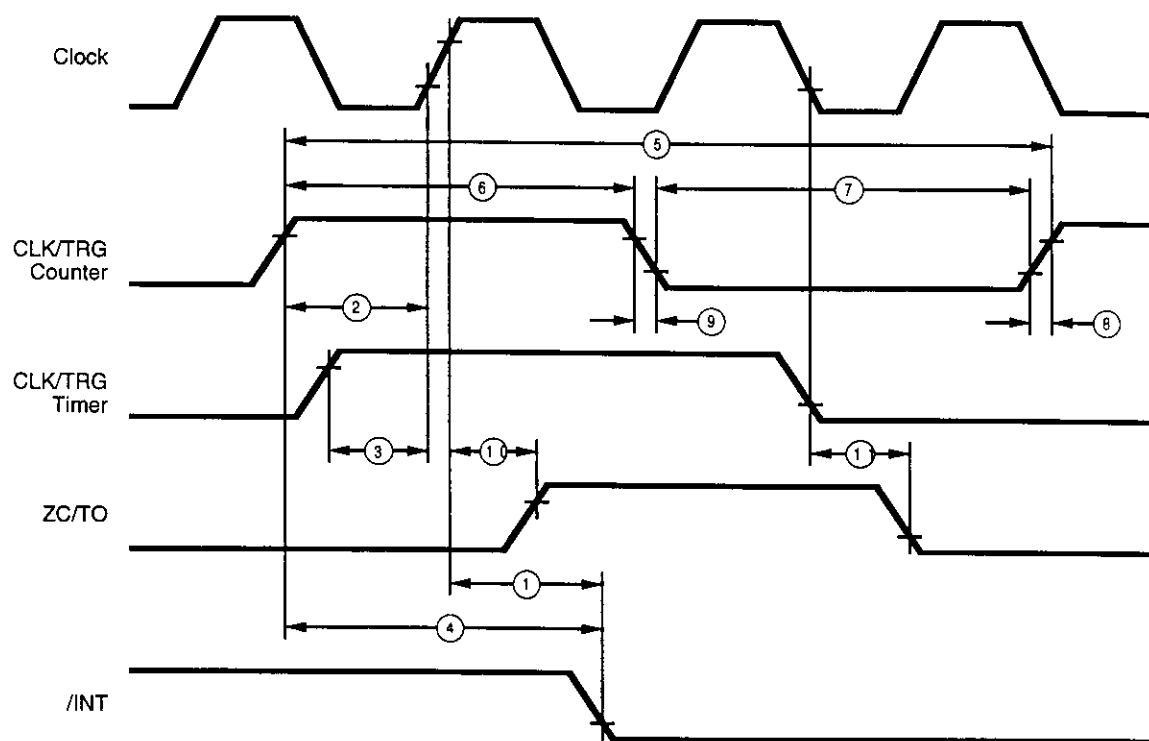
## TIMING DIAGRAMS (Continued)


 On-chip Peripheral I/O Access  
 from External Bus master

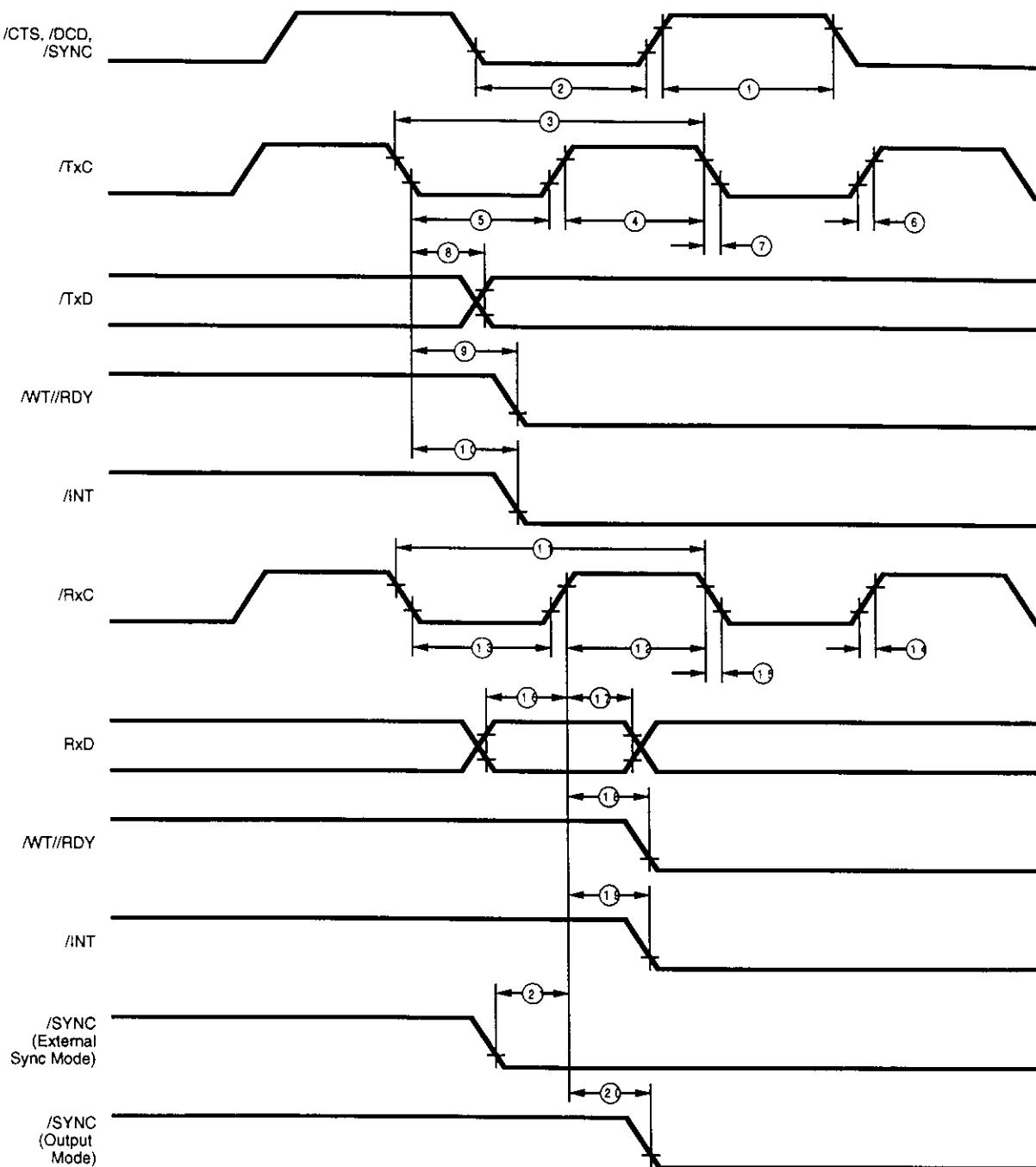


PIO Timing  
(See Table D)

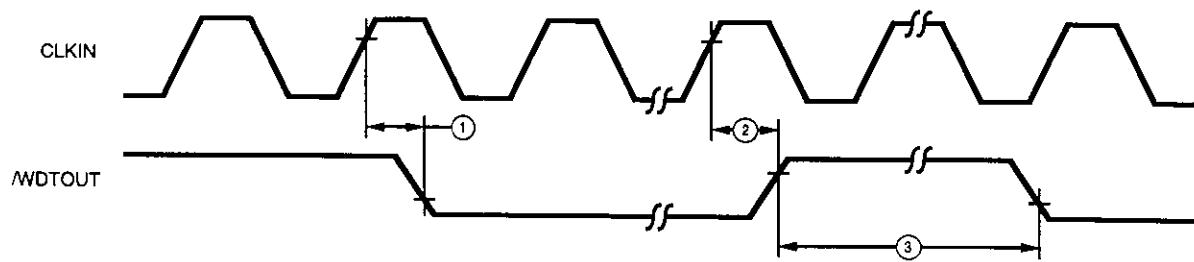
## TIMING DIAGRAMS (Continued)



Counter/Timer Timing  
(See Table E)



SIO Timing  
 (See Table F)

**TIMING DIAGRAMS (Continued)**

**Watch-Dog Timer Timing**  
(See Table H)

## AC CHARACTERISTICS

Table A. CPU Timing

No	Symbol	Parameter	Z84C1306		Z84C1310		Z84C1316 †		Unit	Note		
			Z84C1506		Z84C1510		Z84C1516					
			Min	Max	Min	Max	Min	Max				
1	TcC	Clock Cycle time	162**	DC	100**	DC	61	DC	ns	[A1]		
2	TwCh	Clock Pulse Width (High)	65	DC	40	DC	20	DC	ns	[A1]		
3	TwCl	Clock Pulse Width (Low)	65	DC	40	DC	20	DC	ns	[A1]		
4	TfC	Clock Fall time		20		10		6	ns	[A1]		
5	TrC	Clock Rise time		20		10		6	ns	[A1]		
6	TdCr(A)	Address Valid from Clock Rise		90		65		55	ns			
7	TdA(MREQf)	Address Valid to /MREQ Fall	35**		0**		-15		ns			
8	TdCl(MREQf)	Clock Fall to /MREQ Fall Delay		70		55		40	ns			
9	TdCr(MREQr)	Clock Rise to /MREQ Rise Delay		70		55		40	ns			
10	TwMREQh	/MREQ Pulse Width (High)	65**		30**		10		ns	[A2]		
11	TwMREQl	/MREQ Pulse Width (Low)	132**		75**		25		ns	[A2]		
12	TdCl(MERQr)	Clock Fall to /MREQ Rise Delay		70		55		40	ns			
13	TdCl(RDf)	Clock Fall to /RD Fall Delay		80		65		40	ns			
14	TdCr(RDr)	Clock Rise to /RD Rise Delay		70		55		40	ns			
15	TsD(Cr)	Data Setup Time to Clock Rise	30		25		10		ns			
16	ThD(RDr)	Data Hold Time After /RD Rise	0		0		0		ns			
17	TsWAIT(Cf)	/WAIT Setup Time to Clock Fall	60		20		12		ns			
18	ThWAIT(Cf)	/WAIT Hold Time After Clock Fall	10		10		10		ns			
19	TdCr(M1f)	Clock Rise to /M1 Fall Delay		80		65		40	ns			
20	TdCr(M1r)	Clock Rise to /M1 Rise Delay		80		65		40	ns			
21	TdCr(RFSHf)	Clock Rise to /RFSH Fall Delay		110		80		60	ns			
22	TdCr(RFSHr)	Clock Rise to /RFSH Rise Delay		100		80		60	ns			
23	TdCl(RDr)	Clock Fall to /RD Rise Delay		70		55		40	ns			
24	TdCr(RDf)	Clock Rise to /RD Fall Delay		70		55		40	ns			
25	TsD(Cf)	Data Setup to Clock Fall During M2, M3, M4 or M5 Cycles	40		25		12		ns			
26	TdA(IORQf)	Address Stable Prior to /IORQ Fall	107**		50**		0		ns			
27	TdCr(IORQf)	Clock Rise to /IORQ Fall Delay		65		50		40	ns			
28	TdCl(IORQr)	Clock Fall to /IORQ Rise Delay		70		55		40	ns			
29	TdD(WRf)	Data Stable Prior to /WR Fall	22**		40**		-10		ns			
30	TdCl(WRf)	Clock Fall to /WR Fall Delay		70		55		40	ns			
31	TwWR	/WR Pulse Width	132**		75**		25		ns			
32	TdCl(WRr)	Clock Fall to /WR Rise Delay		70		55		40	ns			
33	TdD(WRf)IO	Data Stable Prior to /WR Fall	-55**		-10**		-30		ns			
34	TdCr(WRf)	Clock Rise to /WR Fall Delay		60		50		40	ns			
35	TdWRr(D)	Data Stable from /WR Fall	30**		10**		0	0	ns			
36	TdCl(HALT)	Clock Fall to /HALT 0 or 1		260		90		70	ns			
37	TwNMI	/NMI pulse Width	60		60		60		ns			
38	TsBUSREQ(Cr)	/BUSREQ Setup Time to Clock Rise	50		30		15		ns			
39	ThBUSREQ(Cr)	/BUSREQ Hold Time after Clock Rise	10		10		10		ns			
40	TdCr(BUSACKf)	Clock Rise to /BUSACK Fall Delay		90		75		40	ns			

**AC CHARACTERISTICS** (Continued)

**Table A. CPU Timing** (Continued)

No	Symbol	Parameter	Z84C1306		Z84C1310		Z84C1316 †		Unit	Note
			Z84C1506	Z84C1510	Min	Max	Min	Max		
41	TdCf(BUSACKr)	Clock Fall to /BASACK Rise Delay			90		75		40	ns
42	TdCr(Dz)	Clock Rise to Data Float Delay			80		65		40	ns
43	TdCr(CTz)	Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR)			70		65		40	ns
44	TdCr(Az)	Clock Rise to Address Float Delay			80		75		40	ns
45	TdCTr(A)	Address Hold Time from /MREQ, /IORQ, /RD or /WR	35**		20**			0		ns
46	TsRESET(Cr)	/RESET to Clock Rise Setup Time	60		40		15			ns
47	ThRESET(Cr)	/RESET to Clock Rise Hold Time	10		10		10			ns
48	TsINTt(Cr)	/INT Fall to Clock Rise Setup Time	70		50		15			ns
49	ThINTr(Cr)	/INT Rise to Clock Rise Hold Time	10		10		10			ns
50	TdM1f(IORQf)	/M1 Fall to /IORQ Fall Delay	359**		220**		100			ns
51	TdCf(IORQf)	Clock Fall to /IORQ Fall Delay			70		55		45	ns
52	TdCf(IORQR)	Clock Rise to /IORQ Rise Delay			70		55		45	ns
53	TdCf(D)	Clock Fall to Data Valid Delay			130		110		75	ns
54	TRDf(D)	/RD Fall to Output Data Valid		TBD		60		40		ns
55	TdIORQ(D)	/IORQ Fall to Output Data Valid		TBD		70		45		ns
56	TwRESET	/RESET Pulse Width 013/015, or C13/C15 with RESET Output Disabled		3TcC		3TcC		3TcC		ns
57	TwRESEToe	/RESET Pulse Width RESET Output Enabled		2TcC		2TcC		2TcC		ns
58	TwRESETdo	/RESET Drive Duration RESET Output Enabled		16TcC		16TcC		16TcC		ns
59	TwRESETpor	/RESET drive duration on Power-On Sequence	10	75	10	75	10	75	ms	
				25		20		15		ns
60	TdCs(A)	Address Valid to Chip Select Valid								

**Notes:**

† 16 MHz parts are only available in Standard Temperature range.

\*\* For clock period other than the minimum shown, calculate parameters using the formula on Table H.

[A1] These parameters apply to the external Clock input on CLKIN pin. For the cases where external Clock is fed from XTAL1, please refer to Table B.

[A2] For loading &gt;= 50 pF, decrease width by 10 ns for each additional 50 pF.

Table H. Footnote to Table A.

No	Symbol	Parameter	Z84C1306 Z84C1506	Z84C1310 Z84C1510	Z84C1316 Z84C1516
1	TcC	TwCh + TwCl + TrC + TfC			
7	TdA(MREQf)	TwCh + TfC	-50	-50	-45
10	TwMREQh	TwCh + TfC	-20	-20	-20
11	TwMREQI	TcC	-0	-25	-25
26	TdA(IORQf)	TcC	-55	-50	-50
29	TdD(WRf)	TcC	-140	-60	-60
31	TwWR	TcC	-30	-25	-25
33	TdD(WRf)	TwCl + TrC	-140	-60	-60
35	TdWRr(D)	TwCl + TrC	-55	-40	-25
45	TdCTr(A)	TwCl + TrC	-50	-30	-30
50	TdM1f(IORQf)	2TcC + TwCh + TfC	-50	-30	-30

**AC CHARACTERISTICS** (Continued)

**Table B. CGC Timing**

No	Symbol	Parameter	Z84C1306		Z84C1310		Z84C1316 †		Unit	Note
			Z84C1506	Z84C1510	Min	Max	Min	Max		
1	TRST(INT)S	Clock Restart Time by /INT (STOP Mode)			(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC	ns
2	TRST(NMI)S	Clock Restart Time by /NMI (STOP Mode)			(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC		(Typ)2 <sup>14</sup> +2.5TcC	ns
3	TRST(INT)I	Clock Restart Time by /INT (IDLE Mode)			2.5TcT		2.5TcT		2.5TcT	ns
4	TRST(NMI)I	Clock Restart Time by /NMI (IDLE Mode)			2.5TcT		2.5TcT		2.5TcT	ns
5	TRST(RESET)I	Clock Restart Time by /RESET (IDLE Mode)			1TcC		1TcC		1TcC	ns
6	TfCLKOUT	CLKOUT Rise Time			15		10		6	ns
7	TrCLKOUT	CLKOUT Fall time			15		10		6	ns
8	TcX1	XTAL1 Cycle Time (for External Clock Input on XTAL1)								
		Divide-by-Two Mode	81			50			31	ns
		Divide-by-One Mode	162			100			61	ns
9	TwX1	XTAL1 Low Pulse Width (for External Clock Input on XTAL1)								
		Divide-by-Two Mode	35			15			10	ns
		Divide-by-One Mode	65			40			25	ns
10	TwhX1	XTAL1 High Pulse Width (for External Clock input on XTAL1)								
		Divide-by-Two mode	35			15			10	ns
		Divide-by-One mode	65			40			25	ns
11	TrX1	XTAL1 Rise Time (for External Clock Input on XTAL1)			25		25		15	ns [B1]
12	Tfx1	XTAL1 Fall Time (for External Clock Input on XTAL1)			25		25		15	ns [B1]

**Note:**

[B1] If parameters 8 and 9 are not met, adjust parameters 11 and 12 to satisfy parameters 8 and 9.

† 16 MHz parts are only available in Standard Temperature range.

**Table C. Timing for on-chip peripheral access from external bus master  
and daisy-chain timing**

No	Symbol	Parameter	Z84C1306		Z84C1310		Z84C1316 †		Unit	Note
			Z84C1506	Min	Max	Z84C1510	Min	Max	Z84C1516	
1	TsA(Rif)	Address Setup Time to /RD, /IORQ Fall		50		40		30		ns
2	TsRf(Cr)	/RD, /IORQ Rise to Clock Rise Setup		60		50		40		ns
3	Th	Hold time for Specified Setup		15		15		10		ns
4	TdCr(DO)	Clock Rise to Data out delay			100		80	60		ns
5	TdRIf(DOz)	/RD, /IORQ Rise to Data Out Float Delay			75		60	50		ns
6	ThRDr(D)	/M1, /RD, /IORQ Rise to Data Hold		15	40	15	30		20	ns [C1]
7	TsD(Cr)	Data In to Clock Rise Setup Time		30		25		15		ns
8	TdIOf(DOI)	/IORQ Fall to Data Out Delay (INTACK cycle)			95		95	70		ns
9	ThIOr(D)	/IORQ Rise to Data Hold		15		15		10		ns
10	ThIOr(A)	/IORQ Rise to Address Hold		15		15		10		ns
11	TsWIf(Cr)	/IORQ, /WR setup time to Clock Rise New parameter		20		20		15		ns [C2]
12	ThWRr(Cr)	Clock Rise to /IORQ, /WR Rise hold time		0		0		0		ns [C2]
13	TsM1f(Cr)	/M1 Fall to Clock Rise Setup Time		40		40		15		ns
14	TsM1r(Cf)	/M1 Rise to Clock Rise Setup Time (/M1 cycle)		-15		-15		-10		ns
15	TdM1f(IEOf)	/M1 Fall to IEO Fall delay (Interrupt Immediately Preceding /M1 Fall)			140		80	60		ns
20	TdCf(IEOr)	Clock Fall to IEO Rise Delay		50		40		30		ns
21	TdCf(IEOf)	Clock Fall to IEO Rise Delay			90		75	75		ns

**Notes:**

[C1] For I/O write to PIO, CTC and SIO.

[C2] For I/O Write to system control registers.

[C3] For daisy-chain timing, please refer to the note on Page 24.

† 16 MHz parts are only available in Standard Temperature range.

**AC CHARACTERISTICS (Continued)**
**Table D. PIO Timing (Z84x15 only)**

No	Symbol	Parameter	Z84C1506		Z84C1510		Z84C1516 †		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	TsIOr(Cr)	/IORQ Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		100		ns	
2	TdCf(RDYr)	Clock Fall to RDY Rise Delay		100		115		40	ns	[D2]
3	TdCf(RDYf)	Clock Fall to RDY Fall Delay		100		115		45	ns	[D2]
4	TwSTB	/STB Pulse Width	100		80		50		ns	[D1]
5	TsSTBr(Cr)	/STB Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		70		ns	[D2]
6	TdIOr(PD)	/IORQ Rise to Port Data Stable Delay (Mode 0)		140		120		100	ns	[D2]
7	TsPD(STBr)	Port Data to /STB Rise Setup Time (Mode 1)	140		75		30		ns	
8	ThPD(STBr)	Port Data to /STB Rise Hold Time (Mode 1)	15		15		15		ns	
9	TdSTBf(PD)	/STB Fall to Port Data Stable (Mode 2)	150		120		35		ns	[D2]
10	TdSTBr(PDz)	/STB Rise to Port Data Float Delay (Mode 2)	140		120		55		ns	
11	TdPD(INTf)	Port Data Match to /INT Fall Delay (Mode 3)	250		200		40		ns	
12	TdSTBr(INTf)	/STB Rise to /INT Fall Delay	290		220		90		ns	

**Notes:**

[D1] For Mode 2: TwSTB &gt; TsPD(STB).

[D2] Increase these values by 2 ns for 10 pF increase in loading up to 100 pF Max.

† 16 MHz parts are only available in Standard Temperature range.

**Table E. CTC Timing**

No	Symbol	Parameter	Z84C1306		Z84C1310		Z84C1316 †		Unit	Note
			Z84C1506	Min	Max	Z84C1510	Min	Max		
1	TdCr(INT1)	Clock Rise to /INT Fall Delay		(TcC+100)			(TcC+80)			[E1]
2	TsCTR(Cc)	CLK/TRG to Clock Rise								
		Setup Time for Immediate Count	90			90		40	ns	[E2]
3	TsCTR(Ct)	CLK/TRG to Clock Rise								
		Setup Time for Enabling of Prescaler on Following Clock Rise	90			90		40	ns	[E1]
4	TdCTR(INTf)	CLK/TRG to /INT Fall Delay								
		TsCTR(C) Satisfied		(1)+(3)			(1)+(3)			[E2]
		TsCTR(C) not Satisfied		TcC+(1)+(3)			TcC+(1)+(3)			[E2]
5	TcCTR	CLK/TRG Cycle time	(2TcC)	DC		(2TcC)	DC		ns	[E3]
6	TwCTRrh	CLK/TRG Width (Low)	90	DC		90	DC	25	DC	ns
7	TwCTRI	CLK/TRG Width (High)	90	DC		90	DC	25	DC	ns
8	TrCTR	CLK/TRG Rise Time	30			30		15		ns
9	TfCTR	CLK/TRG Fall Time	30			30		15		ns
10	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay	80			80		25		ns
11	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay	80			80		25		ns

**Notes:**

[E1] Timer Mode.

[E2] Counter Mode.

[E3] Counter Mode only; when using a cycle time less than 3TcC, parameter #2 must be met.

† 16 MHz parts are only available in Standard Temperature range.

**Table F. SIO Timing**

No	Symbol	Parameter	Z84C1306		Z84C1310		Z84C1316 †		Unit	Note
			Z84C1506	Min	Max	Z84C1510	Min	Max		
1	TwPh	Pulse Width (High)		150		120		80		ns
2	TwPl	Pulse Width (Low)		150		120		80		ns
3	TcTxC	/TxC Cycle Time		250		200		120		ns [F1]
4	TwTxCh	/TxC Width (High)		85		80		55		ns
5	TwTxCl	/TxC Width (Low)		85		80		80		ns
6	TrTxC	/TxC Rise Time			60		60		60	ns
7	TfTxC	/TxC Fall Time			60		60		60	ns
8	TdTxCf(TxD)	/TxC Fall to TxD Delay			160		120		95	ns
9	TdTxCf(W/RRf) (Ready Mode)	/TxC Fall to W//RDY Fall Delay	5	9	5	9	5	8		TcC
10	TdTxCf(INTf)	/TxC Fall to /INT Fall Delay	5	9	5	9	5	9		TcC
11	TcRxC	/RxC Cycle Time		250		200		120		ns [F1]
12	TwRxCh	/RxC Width (High)		85		80		55		ns
13	TwRxCl	/RxC Width (Low)		85		80		70		ns
14	TrRxC	/RxC Rise Time			60		60		60	ns
15	TfRxC	/RxC Fall Time			60		60		60	ns
16	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (X1 Mode)	0		0		5			ns
17	ThRxCr(RxD)	/RxC Rise to RxD Hold Time (X1 Mode)		80		60		40		ns
18	TdRxCr(W/RRf)	/RxC Rise to W//RDY Fall Delay (Ready Mode)	10	13	10	13	10	13		TcC
19	TdRxCr(INTf)	/RxC Rise to /INT Fall Delay	10	13	10	13	10	13		TcC
20	TdRxCr(SYNCf)	/RxC Rise to /SYNC Fall Delay (Output Modes)	4	7	4	7	4	7		TcC
21	TsSYNCf(RxCr)	/SYNC Fall to /RxC Rise Setup (External Sync Modes)		-100		-100		-100		ns [F2]
22	TdIOf(W/RRf)	/IORQ Fall or Valid Address to W//RDY Delay (Wait Mode)		130		110		40		[F2]
23	TdCr(W/RRf)	Clock Rise to W//RDY Delay (Ready Mode)		85		85		40		[F2]
24	TdCf(W/Rz)	Clock Fall to W//RDY Float Delay (Wait Mode)		90		80		40		[F2]

**Notes:**

[F1] In all modes, the System Clock rate must be at least five times the maximum data rate.

[F2] Parameters 22 to 24 are on page 14.

† 16 MHz parts are only available in Standard Temperature range.

**AC CHARACTERISTICS (Continued)**
**Table G. Watch-Dog Timer Timing**

No	Symbol	Parameter	Z84C1306 Z84C1506		Z84C1310 Z84C1510		Z84C1316 † Z84C1516		
			Min	Max	Min	Max	Min	Max	Units
1	TdC(WDTf)	Clock Rise to /WDTOUT Fall Delay		160		160		160	ns
2	TdCr(WbTc)	Clock Rise to /WDTOUT Rise Delay		165		165		160	ns
3	TcWDT	/WDTOUT Cycle Time							
		WDTP = 00	(Typ)2 <sup>16</sup> TcC		(Typ)2 <sup>16</sup> TcC		(Typ)2 <sup>16</sup> TcC		ns
		WDTP = 01	(Typ)2 <sup>18</sup> TcC		(Typ)2 <sup>18</sup> TcC		(Typ)2 <sup>18</sup> TcC		ns
		WDTP = 10	(Typ)2 <sup>20</sup> TcC		(Typ)2 <sup>20</sup> TcC		(Typ)2 <sup>20</sup> TcC		ns
		WDTP = 11	(Typ)2 <sup>22</sup> TcC		(Typ)2 <sup>22</sup> TcC		(Typ)2 <sup>22</sup> TcC		ns

**Notes:**

\* In all modes, the System Clock rate must be at least five times the maximum data rate.

RESET must be active a minimum of one complete clock cycle.

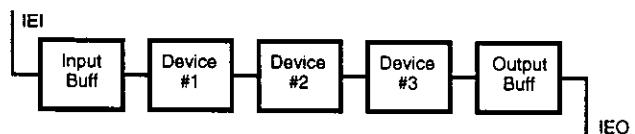
[1] Units equal to System Clock Periods.

[2] Units in nanoseconds (ns).

† 16 MHz parts are only available in Standard Temperature range.

**Additional information for note [C3]**

Parameter #15, 16, 17 and 18 of Table C. These parameters are daisy-chain timing and calculated values, and vary depending on the inside daisy-chain configuration, which is specified in the Interrupt Priority Register. Inside the IPC, the daisy-chain can be figured as follows:


**Internal Daisy-Chain Configuration**

No	Parameter	6 MHz		10 MHz		16 MHz*		Units
		Min	Max	Min	Max	Min	Max	
15	TdM1(IEO)		160		100		80	ns
16	TsIEI(IO) (PIO at #3) (CTC at #3) (SIO at #3)	230		140		100		ns
		280		160		120		ns
		290		160		120		ns
17	TdIEI(IEOf)		120		70		70	ns
18	TdIEI(IEOr)		290		150		120	ns

To calculate IPC daisy-chain timing, it can be treated as if there are Z80 PIO, CTC and SIO with Input buffer and look ahead circuit on the chain. Following are the calculation formulas:

Parameter Table C, #15, /M1 falling to IEO delay  
 $TsM1(IEO) = \text{Max}[TdM1(IO)\#1, TdM1(IO)\#2, TdM1(IO)\#3] + (\text{look-ahead gate Delay})$

Parameter Table C, #16, IEI to /IORQ falling setup time  
 $TsIEI(IEO) = TdIEI(IEO)\#1 + TdIEI(IEO)\#2 + TsIEI(IEO)\#3 + (\text{Input Buffer delay})$

Parameter Table C, #17, IEI falling to IEO falling delay  
 $TdIEI(IEOf) = \text{Max}[TdIEI(IEOf)PIO, TdIEI(IEOf)CTC, TdIEI(IEOf)SIO] + (\text{Input Buffer delay}) + (\text{look-ahead gate Delay})$

Parameter Table C, #18, IEI rising to IEO rising delay (After ED decode)  
 $TdIEI(IEOr) = TdIEI(IEOr)PIO + TdIEI(IEOr)CTC + TdIEI(IEOr)SIO + (\text{Input Buffer delay}) + (\text{look-ahead gate Delay})$

\* Where TdIEI(IEO) is worse number between TdIEI(IEOr) and TdIEI(IEOf)

## ERRATA

1. One of the operational modes is STOP mode. All operation of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, SIO, and the watch-dog timer are stopped at 0 level of the T4 state in the HALT instruction operation code fetch cycle. In STOP mode of operation, the chip will not restart by inputting /RESET.

Workaround:

Use either /NMI or any other /INT, or power-down and power-up to restart again.

2. RFSH by definition should go into High Z state when the EV pin is active. This is not happening and RFSH is not going into High Z state. This could cause a problem with the emulator boards. A device emulator is driving RFSH at the same time the Z84C15 is driving a 1 level. This will cause an extra 30 mA+ current in the RFSH buffer.

Workaround:

If the customer does not use the RFSH pin, then the emulator will still work but will measure an extra 30 mA ICC current. If the customer application uses the RFSH pin, then a 3 level signal could cause the emulator board fail. This can be fixed by adding a jumper to the board on the RFSH pin, when using an emulator open the RFSH pin to the Z84C15. When not using an emulator jumper, RFSH to the output from the emulator board.

3. PIO Port A has inconsistent output drive. Bits 0, 1, 2, 6, and 7 have standard drive current, while bits 3, 4, and 5 have STD + 50%.

Workaround:

This should not cause any problems.

4. The Z84C15 will sometimes lock up in power cycling. This is because the Power-on Reset implementation requires complete discharge to logic 0 to trigger.

Workaround:

Make sure the device is powered-down completely before it is powered-up again.

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