Z08030/8530

Serial Communications Controller

Customer Procurement Specification

PS011301-0601

ZiLOG Worldwide Headquarters • 910 E. Hamilton Avenue • Campbell, CA 95008
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

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ZiLOG Worldwide Headquarters
910 E. Hamilton Avenue
Campbell, CA 95008
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0[a]	V_{CC}+0.3[c]	V	
V_{IL}	Input Low Voltage	-0.3[c]	0.8[a]	V	
V_{OH}	Output High Voltage	2.4[a]		V	I_{OH} = -250 µA
V_{OL}	Output Low Voltage		0.4[a]	V	I_{OL} = +2.0 mA
I_{IL}	Input Leakage		±10.0[a]	µA	0.4 ≤ V_{IN} ≤ +2.4V
I_{OL}	Output Leakage		±10.0[a]	µA	0.4 ≤ V_{OUT} ≤ +2.4V
I_{CC}	V_{CC} Supply Current		250	mA	

V_{CC} = 5V ± 5% unless otherwise specified, over specified temperature range.

a Tested
b Guaranteed by Design
c Guaranteed by Characterization

Absolute Maximum Ratings

Voltages on all pins with respect to GND ..... −0.3V to +7.0V
Operating Ambient Temperature ..... See Ordering Information
Storage Temperature ..... −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

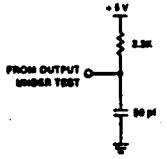
Standard Test Conditions

The DC characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

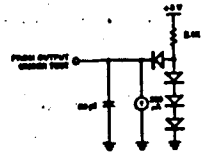
Standard conditions are as follows:

- +4.75 V ≤ V_{CC} ≤ +5.25 V
- GND = 0 V
- T_A as specified in Ordering Information

All ac parameters assume a load capacitance of 50 pF max.

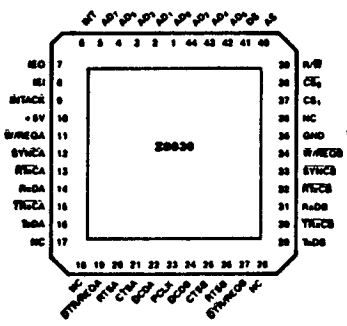


Open-Drain Test Load

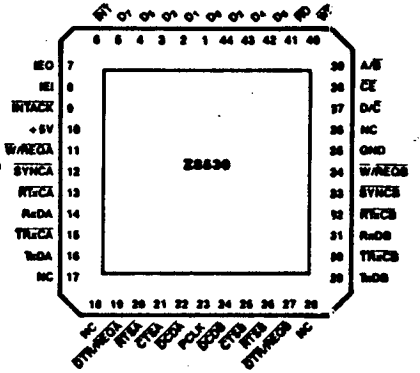


Standard Test Load

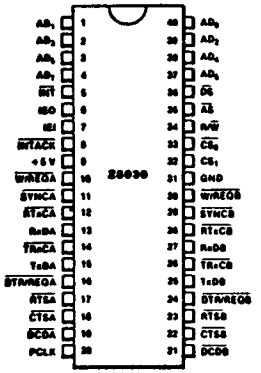
Zilog, Inc. 210 Hacienda Ave., Campbell, CA 95008-6600
Telephone (408) 370-8000 TWX 910-338-7621



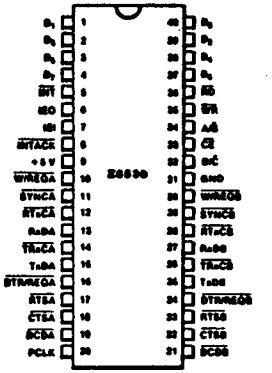
Chip Carrier Pin Assignments, Z8030



Chip Carrier Pin Assignments, Z8530



DIP Pin Assignments, Z8030



DIP Pin Assignments, Z8530

00-2837-02

Zilog

Z80030/8530 Customer Procurement Spec (CPS)

General Description

The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses and the Zilog Z-BUS.® The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, Digital PhaseLocked Loops, and crystal oscillators that dramatically reduce the need for external logic.

The SCC handles asynchronous formats, Synchronous byte-oriented protocols such as IBM Bisync, and Synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The daisy-chain interrupt hierarchy is also supported—as is standard for Zilog peripheral components.

Maximum data rate:
1/4 PCLOCK using external phase lock loop.

Minimum data rate:
50 baud for any PCLK period.

Z8030 AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	Notes*†
1	TwAS	$\overline{AS}$ Low Width	70[a]		50[a]		35[a]		
2	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50[c]		25[c]		15[c]		
3	TsCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time	0[a]		0[a]		0[a]		1
4	ThCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time	60[a]		40[a]		30[a]		1
5	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time	100[a]		80[a]		65[a]		1
6	ThCS1(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time	55[c]		40[c]		30[c]		1
7	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	10[c]		10[c]		10[c]		
8	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250[a]		200[a]		150[a]		
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100[a]		80[a]		65[a]		
10	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55[a]		40[a]		35[a]		
11	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0[c]		0[c]		0[c]		
12	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	60[c]		40[c]		30[c]		
13	TwDSI	$\overline{DS}$ Low Width	240[a]		200[a]		150[a]		
14	TrC	Valid Access Recovery Time	4TcPC[a]		4TcPC[a]		4TcPC[a]		2
15	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30[a]		10[a]		10[a]		1
16	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50[a]		30[a]		25[a]		1
17	TsDW(DS)	Write Data to $\overline{DS}$ ↓ Setup Time	30[a]		20[a]		15[a]		
18	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30[a]		20[a]		20[a]		
19	TdDS(DA)	$\overline{DS}$ ↓ to Data Active Delay	0[c]		0[c]		0[c]		
20	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0[a]		0[a]		0[a]		
21	TdDS(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250[a]		180[a]		140[a]	
22	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Valid Delay		520[a]		300[a]		250[a]	

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the SCC.
*Timings are preliminary and subject to change.
†Units in nanoseconds (ns).
a Tested
b Guaranteed by Design
c Guaranteed by Characterization

Z8030 AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	Notes*†
23	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70[c]		45[c]		40[c]	3
24	TdA(DR)	Address Required Valid to Read Data Valid Delay		570[a]		310[a]		260[a]	
25	TdDS(W)	$\overline{DS}$ ↓ to Wait Valid Delay		240[a]		200[a]		170[a]	4
26	TdDS(REQ)	$\overline{DS}$ ↓ to W/$\overline{REQ}$ Not Valid Delay		240[a]		200[a]		170[a]	
27	TdDS(REQ)	$\overline{DS}$ ↓ to DTR/$\overline{REQ}$ Not Valid Delay		5TcPC[a] +300[a]		5TcPC[a] +250[a]		5TcPC[a] +200[a]	
28	TdAS(INT)	$\overline{AS}$ ↑ to $\overline{INT}$ Valid Delay		600[a]		600[a]		600[a]	4
29	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay	250[a]		250[a]		250[a]		5
30	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	380[a]		300[a]		150[a]		
31	TdDSA(DR)	$\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay		250[a]		180[a]		140[a]	
32	TsIE(DSA)	IEI to $\overline{DS}$ ↓ (Acknowledge) Setup Time	120[a]		100[a]		80[a]		
33	ThIE(DSA)	IEI to $\overline{DS}$ ↑ (Acknowledge) Hold Time	0[c]		0[c]		0[c]		
34	TdIE(IEO)	IEI to IEO Delay		120[a]		100[a]		80[a]	
35	TdAS(IEO)	$\overline{AS}$ ↑ to IEO Delay		250[a]		250[a]		200[a]	6
36	TdDSA(INT)	$\overline{DS}$ ↓ (Acknowledge) to $\overline{INT}$ Inactive Delay		500[a]		500[a]		450[a]	4
37	TdDS(ASQ)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay for No Reset	30[a]		15[a]		15[a]		
38	TdASQ(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay for No Reset	30[a]		30[a]		30[a]		
39	TwRES	$\overline{AS}$ and $\overline{DS}$ Coincident Low for Reset	250[a]		200[a]		150[a]		7
40	TwPCl	PCLK Low Width	105[a]	2000[a]	70[a]	1000[a]	50[a]		
41	TwPCh	PCLK High Width	105[a]	2000[a]	70[a]	1000[a]	50[a]		
42	TcPC	PCLK Cycle Time	250[a]	4000[a]	165[a]	2000[a]	120[a]		
43	TrPC	PCLK Rise Time		30[a]		10[a]		10[a]	
44	TfPC	PCLK Fall Time		30[a]		10[a]		10[a]	

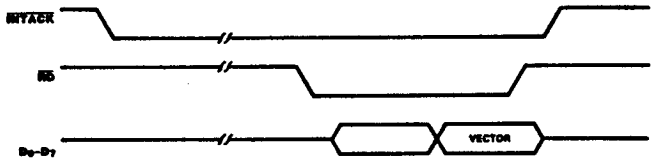
NOTES
3. Float delay is defined as the time required for a ±0.5V change in the output with a maximum dc load and a minimum ac load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any Z-SCC in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIE(DSA) for the Z-SCC, and TdIE(IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a Z-SCC pulling INT Low at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z-SCC.
*Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0".
†Units in nanoseconds (ns).

Z8030/Z8530 SYSTEM TIMING AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	Notes*†‡
1	TdRXC(REQ)	$\overline{RxC}$ ↑ to $\overline{W/REQ}$ Valid Delay	8	12	8	12	8	12	2
2	TdRXC(W)	$\overline{RxC}$ ↑ to Wait Inactive Delay	8	14	8	14	8	14	1,2
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay	4	7	4	7	4	7	2
4a.	TdRXC(INT), Z8530	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay	10	16	10	16	10	16	1,2
4b.	TdRXC(INT), Z8030		8	12	8	12	8	12	1,2
			+2	+3	+2	+3	+2	+3	4
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay	5	8	5	8	5	8	3
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay	5	11	5	11	5	11	1,3
7	TdTXC(DRQ)	$\overline{TxC}$ ↓ $\overline{DTR/REQ}$ Valid Delay	4	7	4	7	4	7	3
8a.	TdTXC(INT), Z8530	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay	6	10	6	10	6	10	1,3
8b.	TdTXC(INT), Z8030		4	6	4	6	4	6	1,3
			+2	+3	+2	+3	+2	+3	4
9a.	TdSY(INT), Z8530	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay	2	6	2	6	2	6	1
9b.	TdSY(INT), Z8030		2	3	2	3	2	3	1,4
10a.	TdEXT(INT), Z8530	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay	2	6	2	6	2	6	1
10b.	TdEXT(INT), Z8030		2	3	2	3	2	3	1,4

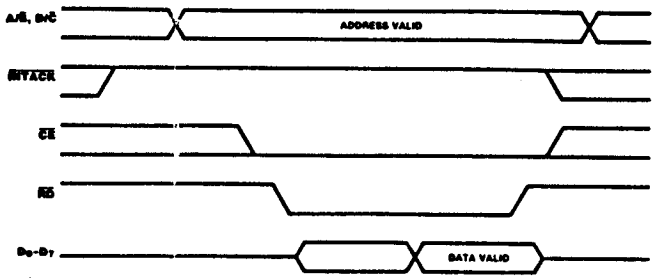
NOTES:
1. Open-drain output, measured with open-drain test load.
2. RxC is RTxC or TRxC, whichever is supplying the receive clock.
3. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
4. Units equal to $\overline{AS}$.

*Timings are preliminary and subject to change.
†Units equal to TcPC.

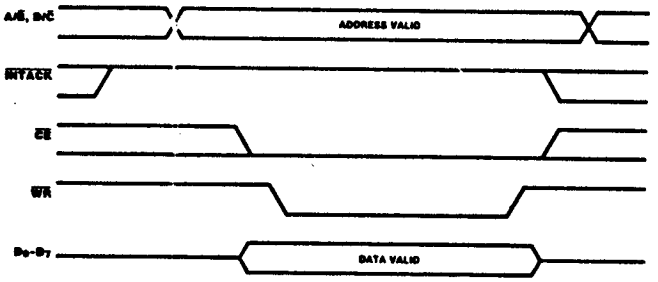


Interrupt Acknowledge Cycle Timing

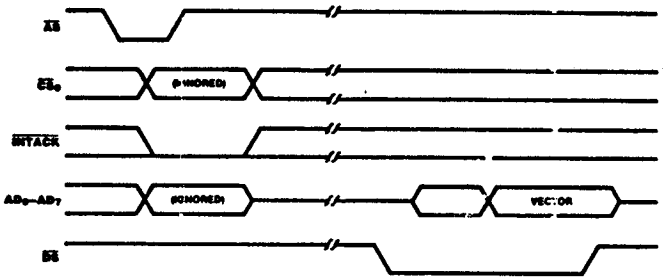
Z8530 Timing



Read Cycle Timing

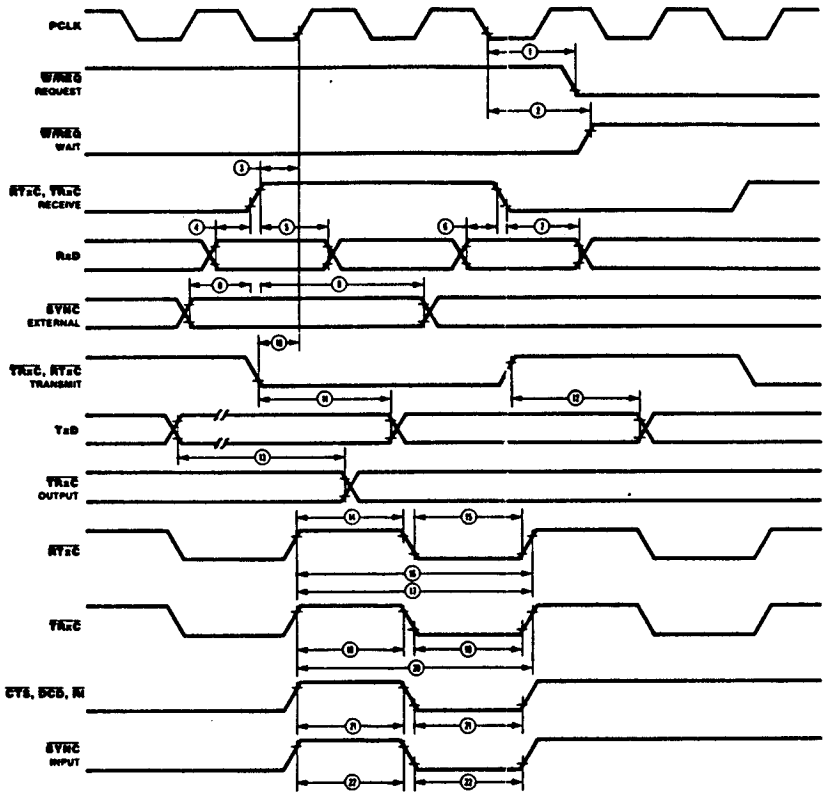


Write Cycle Timing

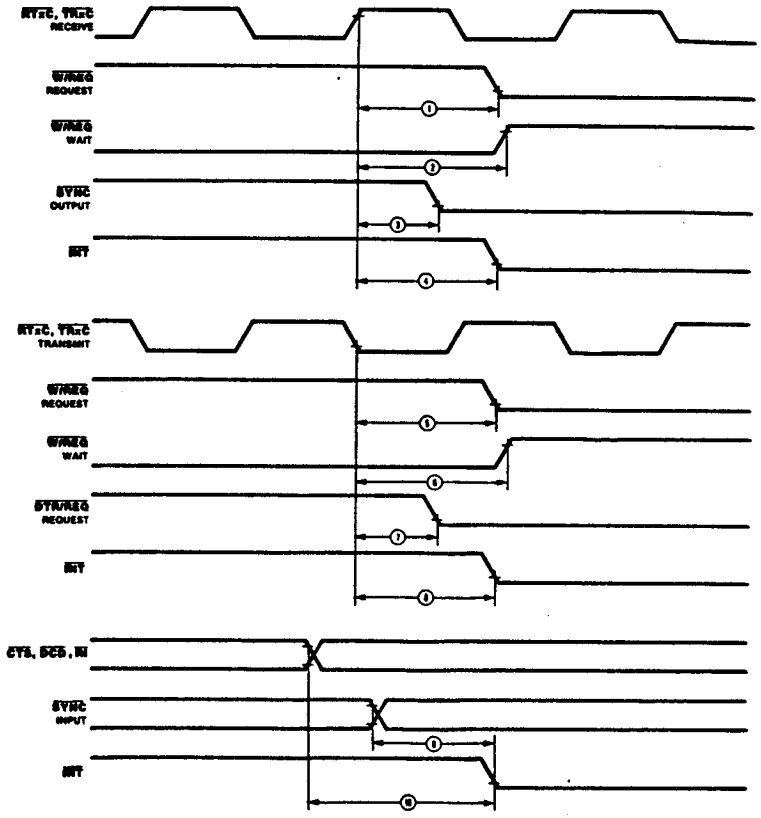


Interrupt Acknowledge Cycle Timing

General Timing

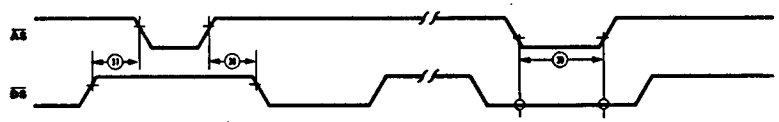


System Timing



Reset Timing

Z8030



Z8530 AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	Notes*†
1	TwPCl	PCLK Low Width	105[a]	2000[a]	70[a]	1000[a]	50[a]	1000[a]	
2	TwPCh	PCLK High Width	105[a]	2000[a]	70[a]	1000[a]	50[c]	1000[a]	
3	TfPC	PCLK Fall Time		20[a]		10[a]		10[a]	
4	TrPC	PCLK Rise Time		20[a]		10[a]		10[a]	
5	TcPC	PCLK Cycle Time	250[a]	4000[a]	165[a]	2000[a]	125[a]	2000[a]	
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80[a]		80[a]		70[a]		
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0[c]		0[c]		0[c]		
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80[a]		80[a]		70[a]		
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0[c]		0[c]		0[c]		
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	10[a]		10[a]		10[a]		
11	TsIAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time	200[a]		160[a]		145[a]		1
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0[c]		0[c]		0[c]		
13	TsIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time	200[a]		160[a]		145[a]		1
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0[a]		0[a]		0[a]		
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	100[a]		100[a]		85[a]		
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0[a]		0[a]		0[a]		
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0[a]		0[a]		0[a]		
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100[a]		70[a]		60[a]		
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time	0[a]		0[a]		0[a]		1
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time	0[a]		0[a]		0[a]		1
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time	100[a]		70[a]		60[a]		1
22	TwRDl	$\overline{RD}$ Low Width	390[a]		200[a]		150[a]		1
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0[c]		0[c]		0[c]		
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0[a]		0[a]		0[a]		
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		250[a]		180[a]		140[a]	
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay		70[a]		45[a]		40[a]	2

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ±0.5V change at the output with a maximum dc load and minimum ac load.

*Timings are preliminary and subject to change.
†Units in nanoseconds (ns).

Z8530 AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	Notes*†
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		300[a]		280[a]		220[a]	
28	TwWRl	$\overline{WR}$ Low Width	240[a]		200[a]		150[a]		
29	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Setup Time	10[a]		10[a]		10[a]		
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0[c]		0[c]		0[c]		
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay		240[a]		200[a]		170[a]	4
32	TdRD(W)	$\overline{RD}$ ↓ Wait Valid Delay		240[a]		200[a]		170[a]	4
33	TdWRl(REQ)	$\overline{WR}$ ↓ to W/$\overline{REQ}$ Not Valid Delay		240[a]		200[a]		170[a]	
34	TdRDl(REQ)	$\overline{RD}$ ↓ to W/$\overline{REQ}$ Not Valid Delay		240[a]		200[a]		170[a]	
35	TdWRr(REQ)	$\overline{WR}$ ↓ DTR/$\overline{REQ}$ Not Valid Delay		5TcPC[a] +300[a]		5TcPC[a] +250[a]		5TcPC[a] +225[a]	
36	TdRDr(REQ)	$\overline{RD}$ ↑ to DTR/$\overline{REQ}$ Not Valid Delay		5TcPC[a] +300[a]		5TcPC[a] +250[a]		5TcPC[a] +200[a]	
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay		500[a]		500[a]		500[a]	4
38	TdIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay	250[a]		200[a]		150[a]		5
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	250[a]		200[a]		150[a]		
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		250[a]		180[a]		140[a]	
41	TslEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	120[c]		100[c]		95[c]		
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0[a]		0[a]		0[a]		
43	TdIEI(IEO)	IEI to IEO Delay Time		120[c]		100[c]		95[c]	
44	TdPC(IEO)	PCLK ↑ to IEO Delay		250[a]		250[a]		200[a]	
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay		500[c]		500[c]		450[a]	4
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	30[c]		15[c]		15[c]		
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	30[c]		30[c]		20[c]		
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250[a]		200[a]		150[a]		
49	Trc	Valid Access Recovery Time	4TcPC[a]		4TcPC[a]		4TcPC[a]		3

NOTES:
3. Parameter applies only between transactions involving the SCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEI(IEO) for each device separating them in the daisy chain.

*Timings are preliminary and subject to change.
†Units in nanoseconds (ns).

a Tested
b Guaranteed by Design
c Guaranteed by Characterization

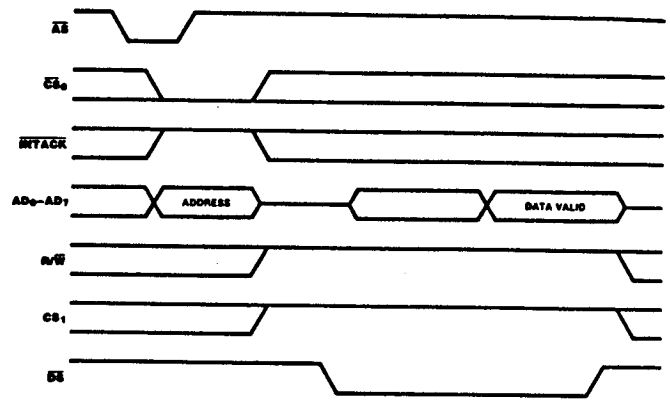
Z8030/Z8530 GENERAL TIMING AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	Notes*†
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid Delay		250[a]		250[a]		250[a]	
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350[a]		350[a]		350[a]	
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (PCLK ÷ 4 case only)	80	TwPCL[c]	70	TwPCL[c]	60	TwPCL[c]	1,4
4	TsRXD(RXCr)	RxD to RxC ↑ Setup Time (X1 Mode)	0[a]		0[a]		0[a]		1
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (X1 Mode)	150[a]		150[a]		150[a]		1
6	TsRXD(RXCf)	RxD to RxC ↓ Setup Time (X1 Mode)	0[a]		0[a]		0[a]		1,5
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (X1 Mode)	150[c]		150[c]		150[a]		1,5
8	TsSY(RXC)	SYNC to RxC ↑ Setup Time	−200[a]		−200[a]		−200[a]		1
9	ThSY(RXC)	SYNC to RxC ↑ Hold Time	3TcPC[c] +400		3TcPC[c] +320		3TcPC[c] +250		1
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time	0[a]		0[a]		0[a]		2,4
11	TdTXCf(TXD)	TxC ↓ to TxD Delay (X1 Mode)		300[a]		230[a]		200[a]	2
12	TdTxCr(TXD)	TxC ↑ to TxD Delay (X1 Mode)		300[a]		230[a]		200[a]	2,5
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)		200[a]		200[a]		200[a]	
14	TwRTXh	RTxC High Width	180[a]		180[a]		150[a]		6
15	TwRTXl	RTxC Low Width	180[a]		180[a]		150[a]		6
16	TcRTX	RTxC Cycle Time (RxD, TxD)	1000[a]		640[a]		500[a]		6,7
17	TcRTXX	Crystal Oscillator Period	250[c]	1000[c]	165[c]	1000[c]	125[c]	1000[c]	3
18	TwTRXh	TRxC High Width	180[a]		180[a]		150[a]		6
19	TwTRXl	TRxC Low Width	180[a]		180[a]		150[a]		6
20	TcTRX	TRxC Cycle Time	1000[a]		640[a]		500[a]		6,7
21	TwEXT	DCD or CTS Pulse Width	200[a]		200[a]		200[a]		
22	TwSY	SYNC Pulse Width	200[a]		200[a]		200[a]		

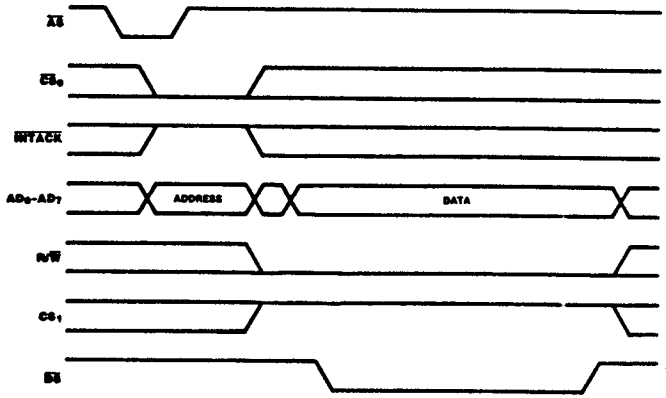
NOTES:
1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30 pf capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
7. The maximum receive or transmit data is ¼ PCLK.

*Timings are preliminary and subject to change.
†Units in nanoseconds (ns).

Z8030 Timing



Read Cycle Timing

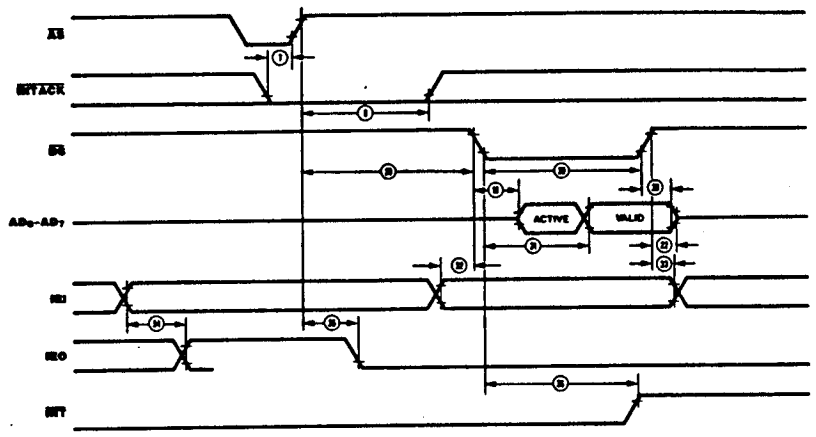


Write Cycle Timing

a Tested
b Guaranteed by Design
c Guaranteed by Characterization

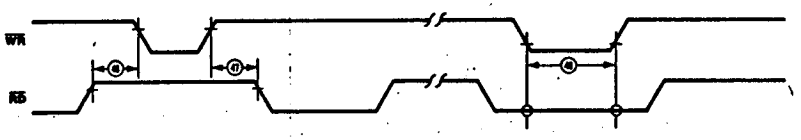
Interrupt Acknowledge Timing

Z8030



Reset Timing

Z8530



Cycle Timing

Z8530