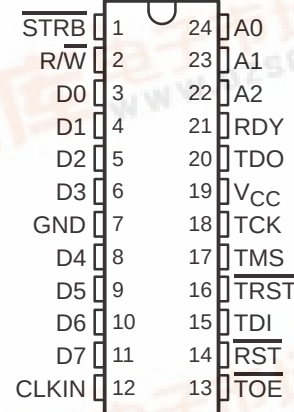


IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

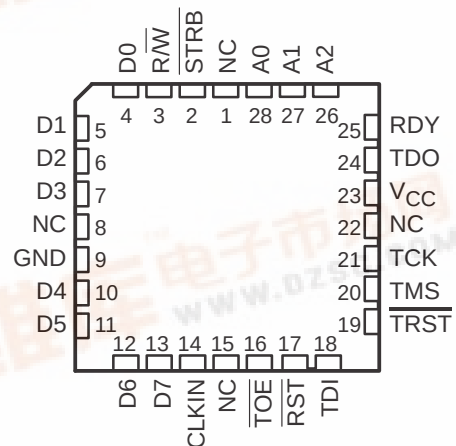
SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

- Members of Texas Instruments (TI) Broad Family of Testability Products Supporting IEEE Std 1149.1-1990 (JTAG) Test Access Port (TAP) and Boundary-Scan Architecture
- Provide Built-In Access to IEEE Std 1149.1 Scan-Accessible Test/Maintenance Facilities at Board and System Levels
- While Powered at 3.3 V, the TAP Interface Is Fully 5-V Tolerant for Mastering Both 5-V and/or 3.3-V IEEE Std 1149.1 Targets
- Simple Interface to Low-Cost 3.3-V Microprocessors/Microcontrollers Via 8-Bit Asynchronous Read/Write Data Bus
- Easy Programming Via Scan-Level Command Set and Smart TAP Control
- Transparently Generate Protocols to Support Multidrop TAP Configurations Using TI's Addressable Scan Port
- Flexible TCK Generator Provides Programmable Division, Gated-TCK, and Free-Running-TCK Modes
- Discrete TAP Control Mode Supports Arbitrary TMS/TDI Sequences for Noncompliant Targets
- Programmable 32-Bit Test Cycle Counter Allows Virtually Unlimited Scan/Test Length
- Accommodate Target Retiming (Pipeline) Delays of Up To 15 TCK Cycles
- Test Output Enable ($\overline{\text{TOE}}$) Allows for External Control of TAP Signals
- High-Drive Outputs ($\sim 32\text{-mA } I_{\text{OH}}$, $64\text{-mA } I_{\text{OL}}$) at TAP Support Backplane Interface and/or High Fanout
- Package Options Include Plastic Small-Outline (DW) Package, Ceramic Chip Carriers (FK), and Ceramic 300-mil DIPs (JT)

SN54LVT8980 . . . JT PACKAGE
SN74LVT8980 . . . DW PACKAGE
(TOP VIEW)



SN54LVT8980 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'LVT8980 embedded test-bus controllers (eTBC) are members of the TI broad family of testability integrated circuits. This family of devices supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit assemblies. Unlike most other devices of this family, the eTBC is not a boundary-scannable device; rather, its function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller. Thus, the eTBC enables the practical and effective use of the IEEE Std 1149.1 test-access infrastructure to support embedded/built-in test, emulation, and configuration/maintenance facilities at board and system levels.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

description (continued)

The eTBC masters all TAP signals required to support one 4- or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset ($\overline{\text{TRST}}$). All such signals can be connected directly to the associated target IEEE Std 1149.1 devices without need for additional logic or buffering. However, as well as being directly connected, the TMS, TDI, and TDO signals can be connected to distant target IEEE Std 1149.1 devices via a pipeline, with a retiming delay of up to 15 TCK cycles; the eTBC automatically handles all associated serial-data justification.

Conceptually, the eTBC operates as a simple 8-bit memory- or I/O- mapped peripheral to a microprocessor/microcontroller (host). High-level commands and parallel data are passed to/from the eTBC via its generic host interface, which includes an 8-bit data bus (D7–D0) and a 3-bit address bus (A2–A0). Read/write select ($\overline{\text{RW}}$) and strobe ($\overline{\text{STRB}}$) signals are implemented so that the critical host-interface timing is independent of the CLKIN period. An asynchronous ready (RDY) indicator is provided to hold off, or insert wait states into, a host read/write cycle when the eTBC cannot respond immediately to the requested read/write operation.

High-level commands are issued by the host to cause the eTBC to generate the TMS sequences necessary to move the test bus from any stable TAP-controller state to any other such stable state, to scan instruction or data through test registers in target devices, and/or to execute instructions in the Run-Test/Idle TAP state. A 32-bit counter can be programmed to allow a predetermined number of scan or execute cycles.

During scan operations, serial data that appears at the TDI input is transferred into a serial-to-4 × 8-bit-parallel first-in/first-out (FIFO) read buffer, which can then be read by the host to obtain the return serial-data stream up to eight bits at a time. Serial data that is to be transmitted from the TDO output is written by the host, up to eight bits at a time, to a 4 × 8-bit-parallel-to-serial FIFO write buffer.

In addition to such simple state-movement, scan, and run-test operations, the eTBC supports several additional commands that provide for input-only scans, output-only scans, recirculate scans (in which TDI is mirrored back to TDO), and a scan mode that generates the protocols used to support multidrop TAP configurations using TI's addressable scan port. Two loopback modes also are supported that allow the microprocessor/microcontroller host to monitor the TDO or TMS data streams output by the eTBC.

The eTBC's flexible clocking architecture allows the user to choose between free-running (in which the TCK always follows CLKIN) and gated modes (in which the TCK output is held static except during state-move, run-test, or scan cycles) as well as to divide down TCK from CLKIN. A discrete mode is also available in which the TAP is driven strictly by read/write cycles under full control of the microprocessor/microcontroller host. These features ensure that virtually any IEEE Std 1149.1 target device or device chain – even where such may not fully comply to IEEE Std 1149.1 – can be serviced by the eTBC.

While most operations of the eTBC are synchronous to CLKIN, a test-output enable ($\overline{\text{TOE}}$) is provided for output control of the TAP outputs, and a reset ($\overline{\text{RST}}$) input is provided for hardware reset of the eTBC. The former can be used to disable the eTBC so that an external controller can master the associated IEEE Std 1149.1 test bus.

The SN54LVT8980 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT8980 is characterized for operation from –40°C to 85°C.

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

Terminal Functions

TERMINAL NAME	DESCRIPTION
A2–A0	Address inputs. A2–A0 form the 3-bit address bus that interfaces the eTBC to its microprocessor/microcontroller host. These inputs directly index the eTBC register to be accessed (read from or written to).
CLKIN	Clock input. CLKIN is the system clock input for the eTBC. Most operations of the eTBC are synchronous to CLKIN. Internally, the CLKIN signal is divided by a programmable divisor to generate TCK.
D7–D0	Data inputs/outputs. D7–D0 form the 8-bit bidirectional data bus that interfaces the eTBC to its microprocessor/microcontroller host. Data in the eTBC registers is accessed (read or written) using this data bus. D7 is considered the most-significant bit, while D0 is considered the least-significant bit.
GND	Ground
RDY	Ready output. RDY is used to indicate to the microprocessor/microcontroller host whether or not the eTBC is ready to service the access (read or write) operation that currently is being requested. If RDY remains high following the initiation of an access cycle (STRB negative edge), then the eTBC is ready. Otherwise, if RDY goes low following the initiation of an access cycle (STRB negative edge), then the eTBC is not ready. In cases where the eTBC is not ready, subsequent processing in the eTBC may clear the not-ready state, which allows RDY to return high before the end of the access cycle. In any event, the RDY output returns high upon the termination of any access cycle (STRB positive edge).
$\overline{\text{RST}}$	Reset input. $\overline{\text{RST}}$ is used to initiate asynchronous reset of the eTBC. Assertion (low) of $\overline{\text{RST}}$ places the eTBC in a reset state from which it does not exit until $\overline{\text{RST}}$ is released (high). While $\overline{\text{RST}}$ is low, the eTBC ignores host writes, the RDY, TDO, TMS, and TRST outputs are high, while TCK outputs CLKIN/16. An internal pullup forces $\overline{\text{RST}}$ to a high level if it has no external connection.
$\overline{\text{R/W}}$	Read/write select. $\overline{\text{R/W}}$ is used by the microprocessor/microcontroller host to instruct the eTBC as to whether it is to perform read access ($\overline{\text{R/W}}$ high) or write access ($\overline{\text{R/W}}$ low). While $\overline{\text{R/W}}$ is high and $\overline{\text{STRB}}$ is low, the D7–D0 outputs are enabled to drive low and/or high logic levels onto the host data bus. Otherwise, while $\overline{\text{R/W}}$ is low, the D7–D0 outputs are disabled to a high-impedance state so that the host data bus can drive to the eTBC.
$\overline{\text{STRB}}$	Read/write strobe. $\overline{\text{STRB}}$ is used by the microprocessor/microcontroller host to instruct the eTBC to initiate ($\overline{\text{STRB}}$ negative edge) or terminate/conclude ($\overline{\text{STRB}}$ positive edge) an access (read or write) operation. An internal pullup forces $\overline{\text{STRB}}$ to a high level if it has no external connection.
TCK	Test clock. TCK transmits the TCK signal required by the eTBC's IEEE Std 1149.1 target(s). All operations of the TAP are synchronous to TCK. Generally, the TCK signal is generated internally by the eTBC by division of CLKIN by a programmable divisor. Alternatively, when the eTBC is in its discrete-control mode, a rising edge of TCK is generated on a read to the discrete-control register, while a falling edge is generated on a write to the discrete-control register.
TDI	Test data input. TDI receives the TDI signal output by the eTBC's IEEE Std 1149.1 target(s). It is the serial input for shifting test data from the target(s); it is sampled on the rising edge of TCK and is expected to be transferred from the target(s) on the falling edge of TCK. An internal pullup forces TDI to a high level if it has no external connection.
TDO	Test data output. TDO transmits the TDO signal required by the eTBC's IEEE Std 1149.1 target(s). It is the serial output for shifting test data to the target(s); it is transferred on the falling edge of TCK and is sampled in the target on the rising edge of TCK.
TMS	Test mode select. TMS transmits the TMS signal required by the eTBC's IEEE Std 1149.1 target(s). It is the one control signal that directs the next TAP-controller state of the target(s). It is transferred from the eTBC on the falling edge of TCK and is sampled in the target(s) on the rising edge of TCK.
$\overline{\text{TOE}}$	Test-output enable. $\overline{\text{TOE}}$ is the active-low output enable for the eTBC TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$). When $\overline{\text{TOE}}$ is inactive (high) the TAP outputs are disabled to a high-impedance state. Otherwise, when $\overline{\text{TOE}}$ is active (low), the TAP outputs are enabled to drive low and/or high logic levels according to other eTBC functions. An internal pullup forces $\overline{\text{TOE}}$ to a high level if it has no external connection.
$\overline{\text{TRST}}$	Test reset. $\overline{\text{TRST}}$ transmits the $\overline{\text{TRST}}$ signal that may be required by some of the eTBC's IEEE Std 1149.1 target(s). A low signal at $\overline{\text{TRST}}$ is intended to initiate asynchronous test reset of the connected target(s). Such a low signal at $\overline{\text{TRST}}$ is generated only when the microprocessor/microcontroller host writes an appropriate value into the eTBC command register or, while the eTBC is in discrete-control mode, into the discrete-control register.
VCC	Supply voltage

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

application information

In application, the eTBC is used to master a single IEEE Std 1149.1 TAP under the control of a microprocessor/microcontroller host. A typical implementation is shown in Figure 1.

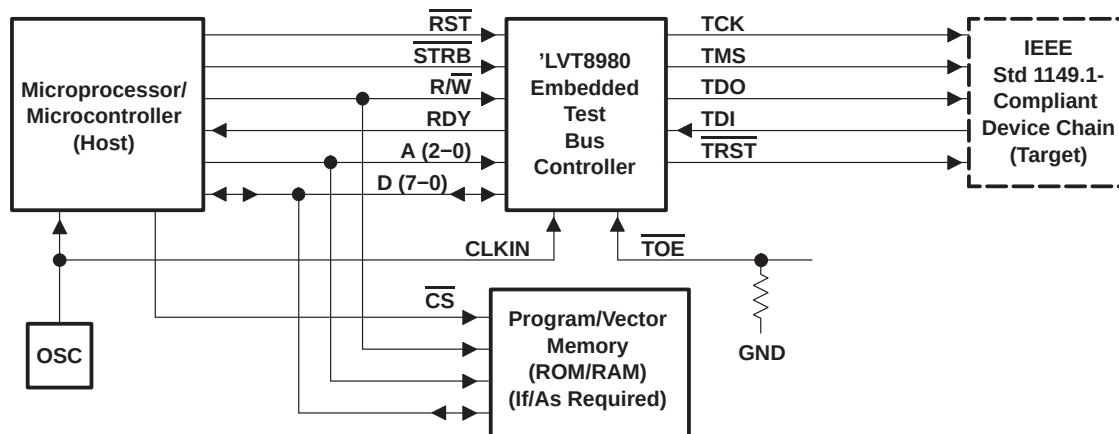


Figure 1. eTBC Application

All signals required to master IEEE Std 1149.1-compliant devices – TCK, TMS, TDO, TDI – are sourced/received by the eTBC. The eTBC also can source the optional TRST signal. Additionally, the eTBC implements high-drive output buffers, allowing it to interface directly to on- or off-board targets without need for buffering or other additional logic.

The eTBC's generic host interface allows it to act as a simple 8-bit memory- or I/O-mapped peripheral. As shown in Figure 1, for many choices of host microprocessor/microcontroller, this interface can be accomplished without additional logic. While the eTBC requires a clock input (CLKIN), in many cases it can be driven from the same source that provides a clock signal to the host.

Thus, in combination with the host microprocessor/microcontroller, the eTBC can be used to implement a two-chip embedded test-control function supporting board- and system-level built-in test, based on structured IEEE Std 1149.1 test access. In some cases, for additional program and/or test vector storage, an external ROM/RAM may be required.

By use of the eTBC in such an embedded test control function, the host microprocessor/microcontroller is freed from the burden of generating the TAP-state sequences, serializing the outgoing bit stream, and deserializing the incoming bit stream. All such tasks are implemented in the eTBC, allowing the host to operate at full 8-bit parallel efficiency, host software to operate at the level of discrete scan operations versus the level of TAP manipulation, and test throughput to be maximized. The eTBC's full suite of data-scan and instruction-scan commands ensure that the host software operates efficiently.

Host efficiency and flexibility also is maximized through the eTBC's fully visible status and implementation of the ready output (RDY). RDY goes inactive during a read or write access if the host-requested access cannot be performed immediately. Thus, it can be used to insert hold or wait states back to the host. When the condition blocking the access clears, the requested access completes. Additionally, all conditions that can cause such a blocking condition are updated continuously in the eTBC status and command registers. Thus, the host software can poll the eTBC status, rather than implement RDY in hardware.

SN54LVT8980, SN74LVT8980 EMBEDDED TEST-BUS CONTROLLERS IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

application information (continued)

The eTBC also provides several capabilities that support special target application requirements. The eTBC's test-output enable allows its master function to be disabled so that another device (an external tester, for example) can control the target TAP. Where required, due to target noncompliance or sensitivity to state sequencing, discrete-control mode provides the host software with arbitrary control of TMS and TDO sequences. Also, where targets may be sensitive to leaving Shift-DR state during scan operation, gated-TCK mode allows the TCK output to be stopped, rather than cycling the target TAP state to Pause-DR state, when service to TDI buffer or TDO buffer is required.

Where target devices are extremely distant (due to cabling, etc.), pipelining may be implemented at intervals along the incoming or outgoing paths to retime (deskew) the TDI, TDO, and TMS signals. An example is shown in Figure 2. In such applications, the eTBC automatically can adjust the incoming test-data bit stream to account for cycle delays introduced by the pipeline.

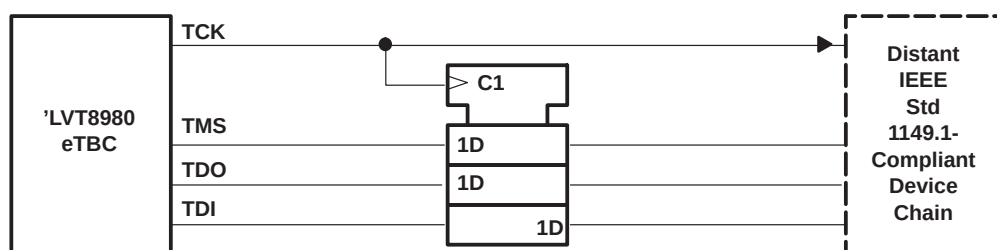


Figure 2. Retimed Interface to Target

Also, in gated-TCK mode, special scan commands provide transparent support for addressable shadow protocols. Thus, in conjunction with its high-drive outputs, the eTBC can fully support multidrop backplane TAP configurations implemented with TI's addressable scan ports (ASP). Figure 3 shows a multidrop TAP configuration in a passive-backplane application implemented with a centralized (one eTBC per chassis/rack) test-control architecture, while Figure 4 shows a passive-backplane application implemented with a distributed (eTBC per module) test-control architecture. Figure 5 shows a multidrop TAP configuration in an active-backplane (motherboard) application.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

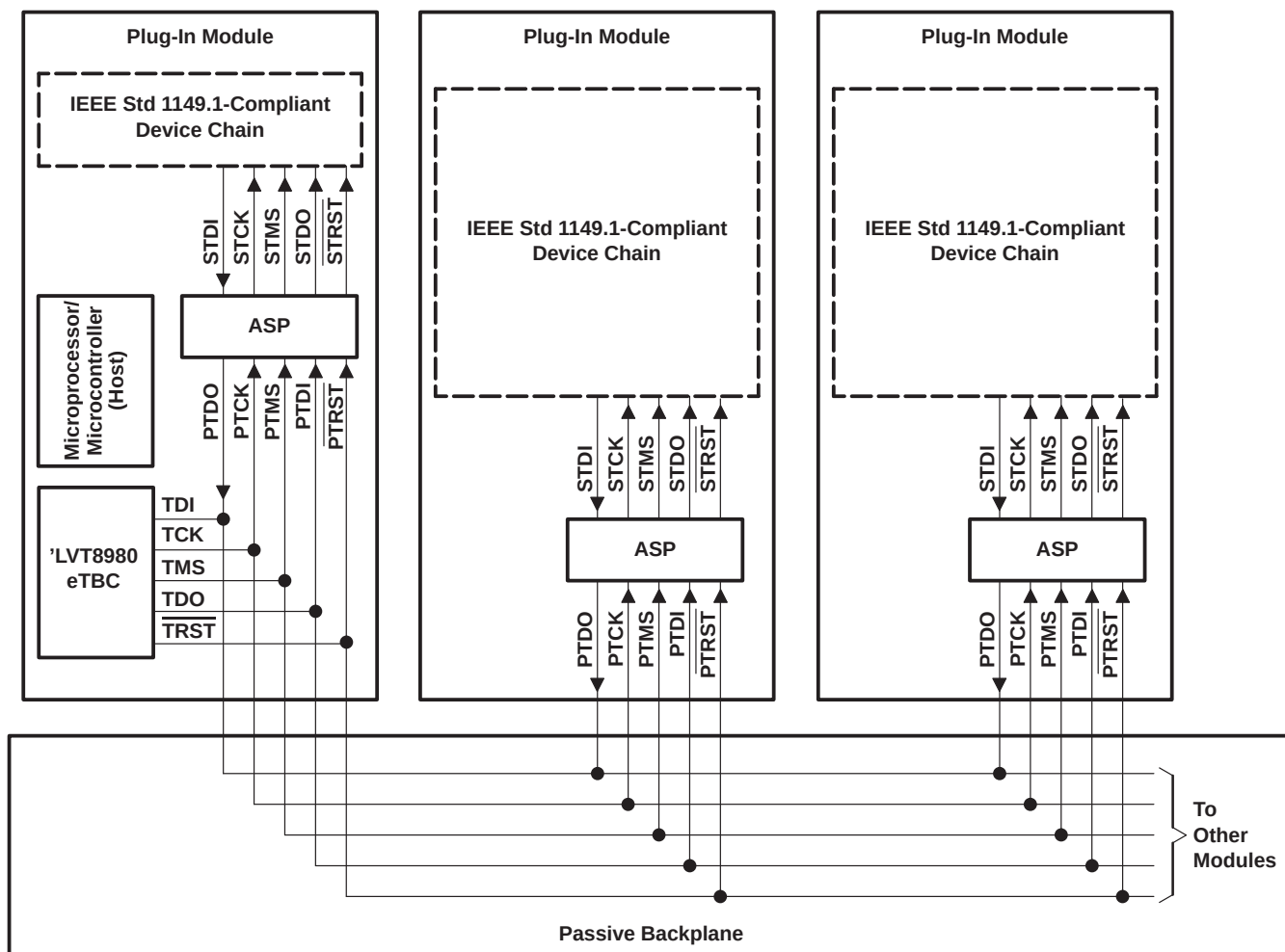


Figure 3. Passive-Backplane Application With Centralized (eTBC Per Chassis) Test-Control Architecture

SN54LVT8980, SN74LVT8980 EMBEDDED TEST-BUS CONTROLLERS IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

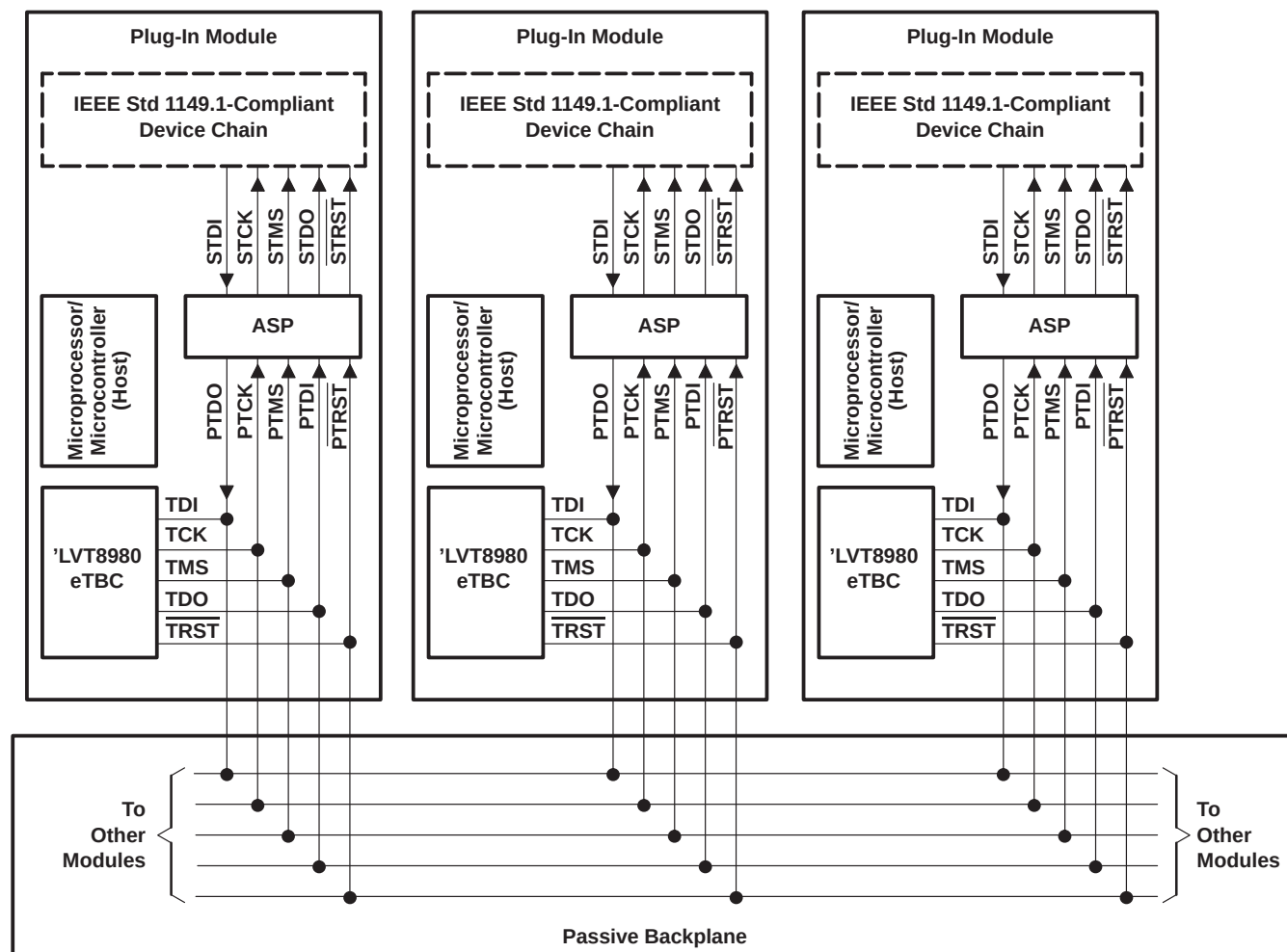


Figure 4. Passive-Backplane Application With Distributed Test-Control (eTBC Per Card) Architecture

SN54LVT8980, SN74LVT8980 EMBEDDED TEST-BUS CONTROLLERS IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

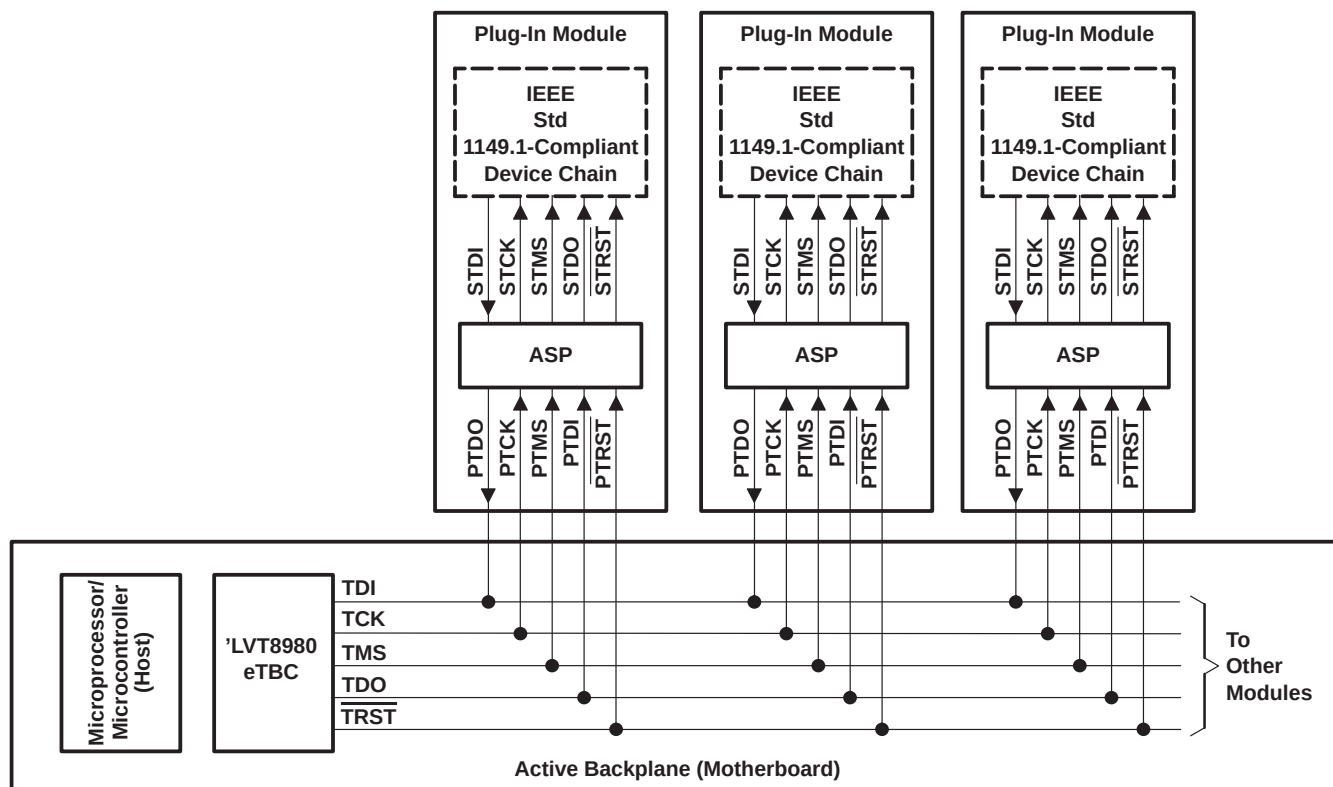


Figure 5. Active-Backplane (Motherboard) Application

architecture

Conceptually, the eTBC can be viewed as an IEEE Std 1149.1 coprocessor/accelerator that operates in conjunction with (and under the control of) a host microprocessor/microcontroller. The eTBC implements this function using an 8-bit generic host interface and a scan-test-based command/control architecture. As shown in the functional block diagram, beyond these fundamental elements and another central block supporting discrete-control mode, the eTBC functions are accomplished in four additional blocks – one for each of the required TAP signals – a TCK generator, a TAP-state (TMS) generator, a TDO buffer, and a TDI buffer.

host interface

The eTBC host interface is implemented generically on an 8-bit read/write data bus (D7–D0). Three address pins (A2–A0) directly index the eTBC's eight read/write registers: configurationA, configurationB, status, command, TDO buffer, TDI buffer, counter, and discrete control. The register address map is given in Table 1.

host access timing

Host access timing is asynchronous to the clock input (CLKIN) and is fully controlled by the read/write strobe ($\overline{\text{STRB}}$). The read/write select ($\text{R}/\overline{\text{W}}$) serves to control the direction of data flow on the bidirectional data bus. Figure 6 shows the read access timing, while Figure 7 shows the write access timing. As shown, for either read or write access, $\text{R}/\overline{\text{W}}$ and address signals should be held while $\overline{\text{STRB}}$ is low.

For read access ($\text{R}/\overline{\text{W}}$ high), the eTBC data bus outputs are made active on the falling edge of $\overline{\text{STRB}}$, to drive the data contained in the selected eTBC register. Otherwise, when $\overline{\text{STRB}}$ is high, the eTBC data outputs are at high impedance. Therefore, in many applications, the $\text{R}/\overline{\text{W}}$ signal can be shared in common with other host peripherals (ROM or RAM, for example), while the $\overline{\text{STRB}}$ signal is generated separately (by discrete chip-select signals available from the host or a decode logic) for each required peripheral.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

host access timing (continued)

For write access ($\overline{R/\overline{W}}$ low), the eTBC data outputs remain at high impedance independent of $\overline{STRB}$. The address of the register to be written is latched from the address pins on the falling edge of $\overline{STRB}$, while the data to be written is latched from the data bus on the rising edge of $\overline{STRB}$.

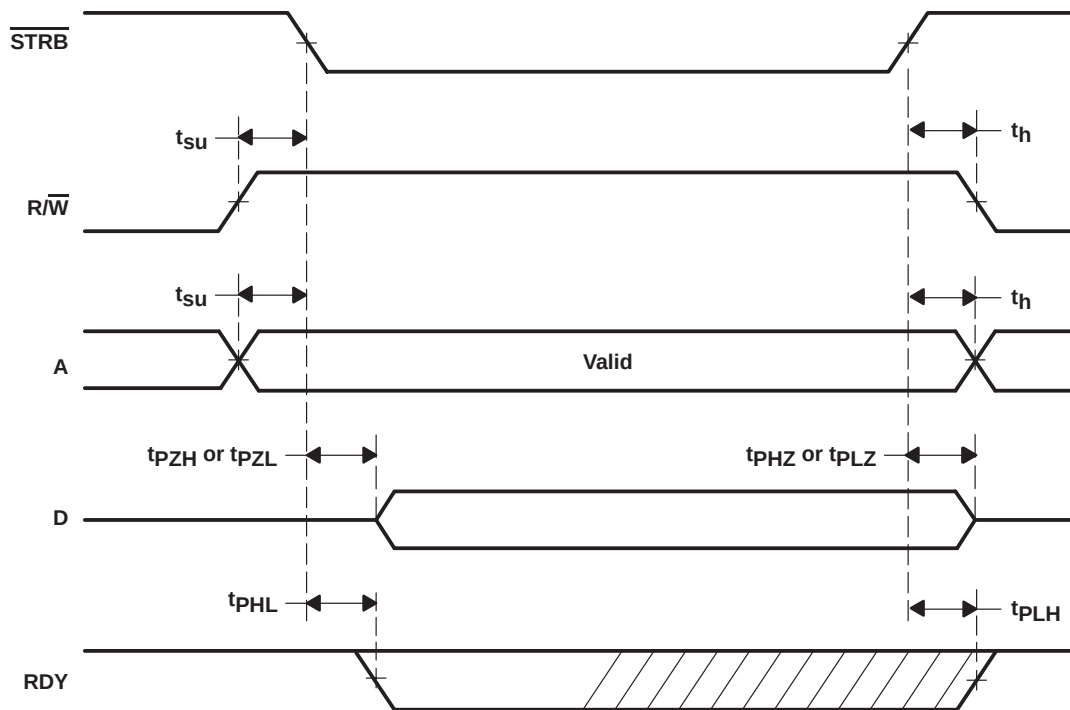


Figure 6. Read Access Timing

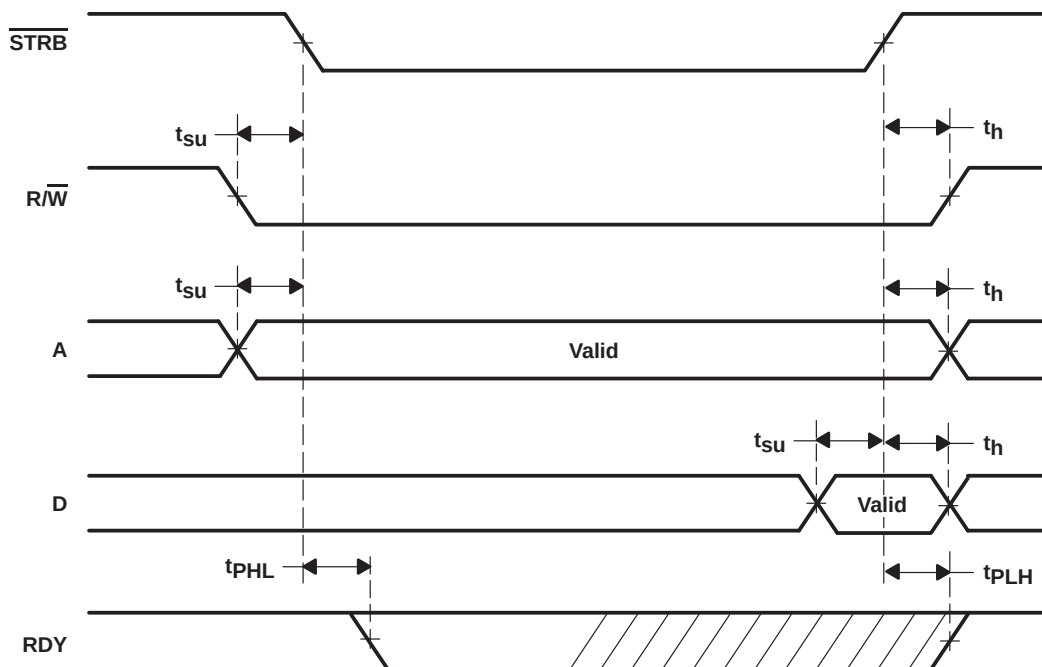


Figure 7. Write Access Timing

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

ready output

The ready output (RDY) from the host interface can be used, where the selected microprocessor/microcontroller supports it, to insert wait or hold states back to the host. If a host-requested access cannot be performed immediately, RDY goes inactive (low) during that given access. When the condition blocking the access clears, RDY goes active (high) and the eTBC grants the requested access. Alternatively, where such hardware-generated hold or wait states are not supported in the selected microprocessor/microcontroller host, the eTBC status and/or command registers can be polled to determine its readiness to grant a given read or write access.

Conditions that cause a host access to be blocked (and RDY to become inactive) are limited to the following:

- While the TDI buffer is empty, as indicated in status register (bit 7, TDIS), a requested read to TDI-buffer register generates RDY inactive; this condition clears, RDY goes active, and the requested access completes, when the TDI buffer is no longer empty.
- While the TDO buffer is full or is being reset upon initiation of a scan command, as indicated in status register (bit 6, TDOS), a requested write to TDO-buffer register generates RDY inactive; this condition clears, RDY goes active, and the requested access completes, when the TDO buffer is no longer full or the TDO-buffer reset completes, as applicable.
- While a command is in progress, as indicated by a non-zero value in the opcode field (bits 3–0, OPCOD) of the command register, a requested write to command, configurationA, configurationB, or counter registers generates RDY inactive. This condition clears, RDY goes active, and the requested access is complete, when the previously specified command finishes. The sole exception is the writing of a logic 1 into the software reset (bit 7, SWRST) bit of the command register, which is never blocked.
- While a full-duplex scan command is in progress, and the number of retiming-delay bits is other than zero, the number of writes to TDO-buffer register may not exceed, by more than 5, the number of reads to TDI-buffer register. A write to TDO-buffer register that does exceed this limit is blocked, and generates RDY inactive, indefinitely; the TDI-buffer register must be read before another write to, the TDO-buffer register.

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

register descriptions

A summary of the eTBC registers, their address mappings, bit assignments, reset values, and host accessibility (read/write or read-only) is provided in Table 1. All registers are fully readable by the host. All registers are fully writeable by the host, with the exception of the status and TDI-buffer registers. Also, with the exception of TDO-buffer and command registers, writes to any register while a command is in progress are held off (RDY inactive) or ignored. Bits designated as reserved should be written to logic 0; read-only bits designated as reserved always read logic 0.

Table 1. Register Summary

ADDRESS A2–A0	REGISTER	REGISTER DETAIL (BIT ASSIGNMENTS)								RESET VALUE	HOST ACCESS
		BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)		
000	ConfigurationA	Reserved		NTOE	LPBK		MODE			0x00	R/W
001	ConfigurationB	CDIV			Reserved	RDLY				0x80	R/W
010	Status	TDIS	TDOS	CTRS	Reserved	TAPST				0x00	R
011	Command	SWRST	NTRST	ENDST		OPCOD				0x00	R/W
100	TDO buffer									0x00	R/W
101	TDI buffer									0x00	R
110	Counter									0x00	R/W
111	Discrete control	Reserved				DNTR	DTMS	DTDl	DTDO	0x00	R/W

configuration registers

All eTBC test commands operate under the influence of the configurationA and configurationB registers. The decodes of the various bit groups assigned to these registers are given in Table 2 and Table 3, respectively. These registers are fully readable at all times and are fully writeable, except when an eTBC command is in progress. Bit group values designated as reserved should not be written.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

Table 2. ConfigurationA Register Decode

CONFIGURATIONA		VALUE	RESULT
BIT GROUP	BIT NO.		
NTOE	5	0	TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$) are enabled.
		1	TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$) are disabled (high impedance).
LPBK	4–3	00	No loopback – TDI pin inputs to TDI buffer.
		01	TMS loopback – TAP-state generator inputs to TDI buffer. TMS and TDO pins are fixed high.
		10	TDO loopback – TDO buffer inputs to TDI buffer. TMS and TDO pins are fixed high.
		11	Reserved
MODE	2–0	000	Automatic/free-running-TCK mode – all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output runs continuously. While operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state is cycled to Pause-DR or Pause-IR, as appropriate, until the host performs the required buffer service.
		001	Automatic/gated-TCK mode – all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output is run only when required to move TAP state or to progress run-test or scan operations, otherwise, it is gated off (low). While operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state remains in Shift-IR or Shift-DR, as appropriate, but the TCK output is gated off until the host performs the required buffer service.
		010	Discrete-control mode – all TAP outputs are determined by contents of the discrete-control register under control of host software.
		011–111	Reserved

Table 3. ConfigurationB Register Decode

CONFIGURATIONB		VALUE	RESULT
BIT GROUP	BIT NO.		
CDIV	7–5	000–111	$\text{TCK} = (\text{CLKIN}) / (2^{\text{CDIV}})$; reset value $\text{TCK} = (\text{CLKIN}) / (2^4) = \text{CLKIN} / 16$
RDLY	3–0	0000–1111	Number of retiming delays to accommodate = RDLY; while operating a scan command, TDI sampling is delayed by a number of TCK cycles, equal to RDLY, following the generation of Shift-DR or Shift-IR state, as appropriate.

The negated test-output-enable (NTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware $\overline{\text{TOE}}$. The loopback (LPBK) bit group allows the selection of the source of data to be input to the TDI buffer – from the TDI pin for normal eTBC operations or, for eTBC verification purpose, from TAP-state (TMS) generator or TDO buffer. The test mode (MODE) bit group provides a choice of automatic/free-running-TCK, automatic/gated-TCK, or discrete-control modes.

The clock-divisor (CDIV) bit group allows software control of the TCK output frequency, based on a division of the CLKIN input. Divisors from 2^0 (1) to 2^7 (128) are provided. The clock divisor defaults to 2^4 (16) on eTBC reset (power up, hardware initiated, or software initiated). The retiming-delay (RDLY) bit group provides for the automatic accommodation of retiming (pipeline) delays, which can be used to deskew the TAP signals to target scan chains that are electrically distant (due to cabling delays, etc).

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

status register

The status of the eTBC is fully reported and continuously updated in the status register. The decode of the various bit groups assigned to the status register is given in Table 4.

Table 4. Status Register Decode

STATUS		VALUE	RESULT
BIT GROUP	BIT NO.		
TDIS	7	0	The TDI buffer is empty – no TDI data is available for host read.
		1	The TDI buffer is not empty – at least one byte of TDI data is available for host read.
TDOS	6	0	The TDO buffer is not full – at least one byte in TDO buffer is available for host write.
		1	The TDO buffer is full – no bytes in TDO buffer are available for host write.
CTRS	5	0	The counter is not loaded with a complete 32-bit value – command operation cannot begin until counter load completes.
		1	The counter is loaded with a complete 32-bit value – command operation can begin.
TAPST	3–0	0000	The current target TAP state (as sent by eTBC) is Test-Logic-Reset.
		0001	The current target TAP state (as sent by eTBC) is Select-DR-Scan.
		0010	The current target TAP state (as sent by eTBC) is Capture-DR.
		0011	The current target TAP state (as sent by eTBC) is Shift-DR.
		0100	The current target TAP state (as sent by eTBC) is Exit1-DR.
		0101	The current target TAP state (as sent by eTBC) is Pause-DR.
		0110	The current target TAP state (as sent by eTBC) is Exit2-DR.
		0111	The current target TAP state (as sent by eTBC) is Update-DR.
		1000	The current target TAP state (as sent by eTBC) is Run-Test/Idle.
		1001	The current target TAP state (as sent by eTBC) is Select-IR-Scan.
		1010	The current target TAP state (as sent by eTBC) is Capture-IR.
		1011	The current target TAP state (as sent by eTBC) is Shift-IR.
		1100	The current target TAP state (as sent by eTBC) is Exit1-IR.
		1101	The current target TAP state (as sent by eTBC) is Pause-IR.
		1110	The current target TAP state (as sent by eTBC) is Exit2-IR.
		1111	The current target TAP state (as sent by eTBC) is Update-IR.

The TDI-buffer-status (TDIS) bit reports the readiness of the TDI buffer to respond to a host read. The TDO-buffer-status (TDOS) bit reports the readiness of the TDO buffer to respond to a host write. The counter-status (CTRS) bit reports the readiness of the counter to support a command that uses the counter. The current-TAP-state (TAPST) bit group continuously reports the target TAP state as monitored by the eTBC.

command register

The command register is used to perform software reset of the eTBC, to discretely control the state of the TRST output when not in discrete-control mode, and to initiate test operations in the target(s). The decode of the various bits assigned to the command register is given in Table 5.

Any read to the command register while a command is in progress returns the value written to the command register upon initiation of the command. Once a command finishes, the operation-code (OPCOD) bit group in the command register is reset to null. In this way, the status of a requested command can be monitored/pollled by the host.

With the exception of the software-reset (SWRST) bit, which can be written at any time, writes to the command register, while a command is in progress, causes RDY inactive and is ignored if the write cycle is terminated before the previously requested command finishes.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

Table 5. Command Register Decode

COMMAND		VALUE	RESULT	TEST OPERATION COMMENTS			
BIT GROUP	BIT NO.			WORKING TAP STATE	USES COUNTER	USES TDI BUFFER	USES TDO BUFFER
SWRST	7	0	Normal operation				
		1	Full reset				
TRST	6	0	If not in discrete-control mode, output high to $\overline{\text{TRST}}$ pin				
		1	If not in discrete-control mode, output low to $\overline{\text{TRST}}$ pin				
ENDST	5–4	00	Finish command in TAP state Test-Logic-Reset				
		01	Finish command in TAP state Run-Test/Idle				
		10	Finish command in TAP state Pause-DR				
		11	Finish command in TAP state Pause-IR				
OPCOD	3–0	0000	Null				
		0001	Reserved				
		0010	Execute run test	Run-Test/Idle	Yes	No	No
		0011	Execute input-only ASP scan	N/A	Yes	Yes	No
		0100	Execute ASP scan	N/A	Yes	Yes	Yes
		0101	Execute output-only ASP scan	N/A	Yes	No	Yes
		0110	Execute state move	N/A	No	No	No
		0111	Execute state jump	N/A	No	No	No
		1000	Execute instruction-register scan	Shift-IR	Yes	Yes	Yes
		1001	Execute data-register scan	Shift-DR	Yes	Yes	Yes
		1010	Execute input-only instruction-register scan	Shift-IR	Yes	Yes	No
		1011	Execute input-only data-register scan	Shift-DR	Yes	Yes	No
		1100	Execute output-only instruction-register scan	Shift-IR	Yes	No	Yes
		1101	Execute output-only data-register scan	Shift-DR	Yes	No	Yes
		1110	Execute recirculate instruction-register scan	Shift-IR	Yes	Yes	No
		1111	Execute recirculate data-register scan	Shift-DR	Yes	Yes	No

The software-reset (SWRST) bit is provided to allow software initiation of full eTBC reset. This bit of the command register can be written at any time, regardless of the configuration or command in progress. The test-reset (TRST) bit allows direct software control of the state of $\overline{\text{TRST}}$ output in modes other than discrete control.

The end-TAP-state (ENDST) bit group determines the TAP state in which the target scan chain is left when the requested command finishes. The operation-code (OPCOD) bit group determines the test operation to be executed in the target.

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

counter register

The counter register, while only 8 bits wide like any other eTBC register, provides read/write access to the full 32-bit eTBC counter. Writes to the counter register are accomplished by four complete host access cycles, otherwise, the counter is considered unloaded (CTRS = 0). Reads to the counter register likewise are accomplished by four complete host access cycles. However, reads do not affect the counter-loaded status (CTRS). The counter access (both read and write) is in least-significant-byte-first order. Any writes to the counter register while a command is in progress are ignored. The 32-bit value present in the counter at initiation of a command is used to determine the number of TCK cycles or scan bits for which the command is operated.

TDO-buffer register

The TDO-buffer register, while only 8 bits wide like any other eTBC register, provides write access to the full 4×8 (32-bit) FIFO that comprises the TDO buffer. The TDO-buffer register can be written as long as the TDO buffer does not become full. When the TDO buffer becomes full, further writes to the TDO-buffer register cause RDY inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the write to be ignored if the write cycle is terminated before the TDO-buffer-full status is cleared.

TDI-buffer register

The TDI-buffer register, while only 8 bits wide like any other eTBC register, provides read access to the full 4×8 (32-bit) FIFO that comprises the TDI buffer. The TDI-buffer register can be read as long as the TDI buffer does not become empty. When the TDI buffer becomes empty, further reads to the TDI-buffer register cause RDY inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the read data to be invalid if the read cycle is terminated before the TDI-buffer-empty status is cleared.

discrete-control register

The discrete-control register is used to program the state of the TAP outputs (TCK, TDO, TMS, $\overline{\text{TRST}}$) and to poll the state of the TAP input (TDI) when the eTBC is in its discrete-control mode. The contents of the discrete-control register determine values output to TDO, TMS, and $\overline{\text{TRST}}$ according to the decode in Table 6. The TCK output is generated on each read and write to the discrete-control register; writes generate TCK falling edge, while reads generate TCK rising edge. In modes other than the discrete-control mode, this register is fully writeable and readable, but writes and reads have no effect on eTBC or target operation.

Table 6. Discrete-Control Register Decode

DISCRETE CONTROL		VALUE	RESULT
BIT GROUP	BIT NO.		
DNTR	3	0	If in discrete-control mode, output low to $\overline{\text{TRST}}$ pin, otherwise nothing
		1	If in discrete-control mode, output high to $\overline{\text{TRST}}$ pin, otherwise nothing
DTMS	2	0	If in discrete-control mode, output low to TMS pin, otherwise nothing
		1	If in discrete-control mode, output high to TMS pin, otherwise nothing
DTD I	1	0	The TDI data received is a logic 0.
		1	The TDI data received is a logic 1.
DTDO	0	0	If in discrete-control mode, output low to TDO pin, otherwise nothing
		1	If in discrete-control mode, output high to TDO pin, otherwise nothing

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

command/control

The eTBC's command-based architecture is structured around a set of comprehensive IEEE Std 1149.1 (JTAG) test objectives, which include TAP state movement, scan operations, and run test (operation of test logic in Run-Test/Idle state). The set of test operations, as decoded from the command register (bits 3–0, OPCOD) is given in Table 5. Commands are initiated by writing the eTBC command register; upon command initiation, the test-control logic is initialized and the TDO and TDI buffers are cleared. Command completion is indicated when the operation code (OPCOD) field of the command register returns to the value of the null command.

The eTBC command operation is modified by the configurationA and configurationB registers, which should be written prior to writing the command register, as the values in these registers cannot be modified while a command is in progress. Also, commands are operated only in automatic test modes, as specified in the configurationA register (bits 2–0, MODE) – while in the discrete-control mode, commands are ignored.

All eTBC commands operate similarly to accomplish IEEE Std 1149.1 test objectives. First, the eTBC generates a TMS sequence to move the target scan chain from its current TAP state to a working state that depends on the test objective. Second, the command is operated (test run, bits scanned) in the working state for a number of TCK cycles (or scan bits) determined by the value of the counter upon command initiation. Third, the eTBC generates a TMS sequence to move the target scan chain from the working state to the end state specified in the command register (bits 5–4, ENDST). For some commands, one or more of these steps are omitted.

TAP-state-movement commands

Two eTBC commands are provided to accomplish TAP state movement. The state-move command operates to generate a TMS sequence to move the target scan chain directly from its current TAP state to the end state specified in the command register. The state-jump command moves the eTBC's stored value of the target TAP state without generating any changes to the TMS output. The state-jump command can therefore be used to switch between targets that share the same test bus, such as those in a multidrop backplane configuration implemented with TI addressable scan ports, but that may be left in different TAP states.

run-test command

The run-test command allows the test logic of the target scan chain to execute autonomously in the Run-Test/Idle TAP state. Such test logic is commonly used to implement chip- or board-level built-in self-test. The run-test command generates TMS sequences to move the target scan chain from its current TAP state to the Run-Test/Idle TAP state, where it remains for a number of TCK cycles determined by the value of the counter upon command initiation. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

scan commands

Eleven eTBC commands are provided to perform scan operations to target scan chains. These can be classified by the destination of scan data in the target – addressable scan port (ASP), IEEE Std 1149.1 instruction register, or IEEE Std 1149.1 data register – and by the nature/direction of the data transfer – full-duplex (default), input-only, output-only, or recirculate. The only combination of these two factors that is not implemented is recirculate ASP scan.

addressable scan port (ASP) scan commands

The ASP scan commands scan data to and/or from an addressable scan port target. Since ASP devices require that TMS remain fixed throughout their select and acknowledge protocols, the eTBC does not generate TMS sequences or change its stored value of the target's TAP state. Also, for the same reason, ASP scan commands that target ASP devices should be operated in gated-TCK mode. The ASP scan commands do allow data written to the TDO buffer to be driven serially onto the TDO pin and bits received serially at the TDI pin to be stored into the TDI buffer for reading by the host. However, the ASP scan commands do not perform any bit-pair encoding of ASP select protocols or decoding of ASP acknowledge protocols. Such encoding/decoding must be performed in the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation.

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

instruction-register scan commands

The instruction-register scan commands scan bits to and/or from the concatenation of instruction registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-IR TAP state. Data written to the TDO buffer can be driven serially onto the TDO pin and bits received serially at the TDI pin can be stored in the TDI buffer for reading by the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation. If, during the operation of an instruction register scan command, the TDO buffer becomes empty or the TDI buffer becomes full, the TAP state is sequenced to Pause-IR (if in free-running-TCK mode) or the TCK output is gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

data-register scan commands

The data-register scan commands operate to scan bits to and/or from the concatenation of data registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-DR TAP state. Data written to the TDO buffer can be driven serially onto the TDO pin and bits received serially at the TDI pin can be stored in the TDI buffer for reading by the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation. If, during the operation of a data-register scan command, the TDO buffer becomes empty or the TDI buffer becomes full, the TAP state is sequenced to Pause-DR (if in free-running-TCK mode) or the TCK output is gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

other scan-command variations

As noted before, the nature/direction of the data transfer for any scan command can vary, along with the destination of scan data in the target, as follows:

- For scan commands of the full-duplex (default) class, both TDO buffer and TDI buffer are used to scan data to and from the target scan chain, respectively.
- For scan commands of the input-only class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is fixed at a high level throughout the scan operation.
- For scan commands of the output-only class, only the TDO buffer is used to scan data to the target scan chain; incoming TDI data is simply ignored.
- For scan commands of the recirculate class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is generated by recirculating the incoming TDI data back into the target scan chain.

counter

As described above, the value loaded in the eTBC's 32-bit counter at initiation of a command is used to specify the number of TCK cycles or scan bits to remain in the command's working state. As each TCK cycle or scan bit is processed for a run-test or scan command, respectively, the counter value is decremented. When the counter value reaches zero, the command leaves its working state to finish in the end state specified in the command register.

Before a command that uses the counter can be initiated, a full 32-bit value should be loaded by four consecutive writes to the counter register. As well, the full 32-bit current value of the counter can be observed by four consecutive reads to the counter register. The counter status (unloaded/loaded) is maintained and observable in the status register (bit 5, CTRS).

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the counter is cleared and assumes its unloaded state.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

TCK generator

The TCK generator sources the test clock (TCK) signal required by the IEEE Std 1149.1 target(s) and the eTBC internal test-control logic. The fundamental TCK frequency is produced by division of CLKIN. The divisor is programmable within a range of 1 to 128 in the configurationB register (bits 7–5, CDIV). The TCK output to the target(s) operate in free-running or gated modes. The free-running mode toggles TCK continuously, based on CLKIN, while the gated mode operates the TCK only when required to move the target TAP state or to perform a run-test or scan operation.

While the eTBC is in discrete-control mode, the TCK generator is not used; instead, the state of TCK is toggled on each alternating read and write to the discrete-control register. A falling edge of TCK is produced by write, while a rising edge of TCK is produced by read.

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the TCK generator assumes its free-running mode with a clock divisor of 16 ($TCK = CLKIN/16$).

TAP-state generator

The TAP-state generator sources the TMS signal, which sequences the TAP controllers of connected IEEE Std 1149.1-compliant target devices. The TAP controller specified by IEEE Std 1149.1 is a synchronous finite-state machine that provides test control signals throughout each target device; its state diagram is shown in Figure 8. This diagram and the TAP-controller states are discussed subsequently.

The TAP-state generator operates under the control of an executing command to generate the TMS sequences required to move connected target devices from one stable state to another, to capture and scan test data into/out of target devices, and to operate built-in test modes of target devices in the Run-Test/Idle state.

The TAP state currently being generated always is maintained by the TAP-state generator and is constantly available in the eTBC status register (bits 3–0, TAPST) for host read. Based on the TAP state that is current upon command initiation, the TAP-state generator sources a defined sequence of TMS values to reach the TAP state in which the command is progressed (e.g., Shift-IR, Shift-DR, Run-Test/Idle), and ultimately to reach the specified end TAP state. These sequences are detailed in Tables 7–12.

While the eTBC is in free-running-TCK mode, if a currently operating scan command empties or fills a required test data buffer, then the TAP-state generator sources the TMS sequences required to move the connected target devices to their Pause-IR or Pause-DR states. In such case, the TAP-state generator maintains target devices in their Pause-IR or Pause-DR states until the required test data buffer is serviced appropriately. However, if such a buffer condition occurs while the eTBC is in gated-TCK mode, the TAP-state generator maintains the target devices in their Shift-IR or Shift-DR states while the TCK is gated off.

While the eTBC is in discrete-control mode, the TAP-state generator is not used; instead, the state of the TMS pin is determined by the contents of the discrete-control register. Thus, TMS sequences that cannot be generated automatically still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

The TAP-state generator also is not used during the operation of the special addressable shadow protocol (ASP) scan commands. Since, by definition, ASPs operate only while the TAP is idling (maintaining one of the TAP states Test-Logic-Reset, Run-Test/Idle, Pause-IR, or Pause-DR), the TMS pin must be maintained at the value it held upon initiation of the ASP scan command.

For eTBC verification/debugging, in addition to continuous update of the current target TAP state in the eTBC status register, the output of the TAP-state (TMS) generator can be selected for loopback into the TDI buffer. When this TMS-loopback mode is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TAP-state generator assumes the Test-Logic-Reset TAP state.

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

Table 7. TMS Sequencing From TAP State Test-Logic-Reset

FROM TEST-LOGIC-RESET (TMS = H) TO:											
TEST-LOGIC-RESET		RUN-TEST-IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	T-L-R	L	R-T/I	L	R-T/I	L	R-T/I	L	R-T/I	L	R-T/I
				H	S-DR-S	H	S-DR-S	H	S-DR-S	H	S-DR-S
				L	Capture-DR	L	Capture-DR	H	S-IR-S	H	S-IR-S
				L	Shift-DR	H	Exit1-DR	L	Capture-IR	L	Capture-IR
						L	Pause-DR	L	Shift-IR	H	Exit1-IR
										L	Pause-IR

Table 8. TMS Sequencing From TAP State Run-Test/Idle

FROM RUN-TEST/IDLE (TMS = L) TO:											
TEST-LOGIC-RESET		RUN-TEST-IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	S-DR-S	L	R-T/I	H	S-DR-S	H	S-DR-S	H	S-DR-S	H	S-DR-S
H	S-IR-S			L	Capture-DR	L	Capture-DR	H	S-IR-S	H	S-IR-S
H	T-L-R			L	Shift-DR	H	Exit1-DR	L	Capture-IR	L	Capture-IR
						L	Pause-DR	L	Shift-IR	H	Exit1-IR
										L	Pause-IR

Table 9. TMS Sequencing From TAP State Pause-DR

FROM PAUSE-DR (TMS = L) TO:											
TEST-LOGIC-RESET		RUN-TEST-IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit2-DR	H	Exit2-DR	H	Exit2-DR	H	Exit2-DR	H	Exit2-DR	H	Exit2-DR
H	Update-DR	H	Update-DR	L	Shift-DR	H	Update-DR	H	Update-DR	H	Update-DR
H	S-DR-S	L	R-T/I			H	S-DR-S	H	S-DR-S	H	S-DR-S
H	S-IR-S					L	Capture-DR	H	S-IR-S	H	S-IR-S
H	T-L-R					H	Exit1-DR	L	Capture-IR	L	Capture-IR
						L	Pause-DR	L	Shift-IR	H	Exit1-IR
										L	Pause-IR

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

Table 10. TMS Sequencing From TAP State Pause-IR

FROM PAUSE-IR (TMS = L) TO:											
TEST-LOGIC-RESET		RUN-TEST-IDLE		SHIFT-DR		PAUSE-DR		SHIFT-IR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit2-IR	H	Exit2-IR	H	Exit2-IR	H	Exit2-IR	H	Exit2-IR	H	Exit2-IR
H	Update-IR	H	Update-IR	H	Update-IR	H	Update-IR	L	Shift-IR	H	Update-IR
H	S-DR-S	L	R-T/I	H	S-DR-S	H	S-DR-S			H	S-DR-S
H	S-IR-S			L	Capture-DR	L	Capture-DR			H	S-IR-S
H	T-L-R			L	Shift-DR	H	Exit1-DR			L	Capture-IR
						L	Pause-DR			H	Exit1-IR
										L	Pause-IR

Table 11. TMS Sequencing From TAP State Shift-DR

FROM SHIFT-DR (TMS = L) TO:							
TEST-LOGIC-RESET		RUN-TEST-IDLE		PAUSE-DR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit1-DR	H	Exit1-DR	H	Exit1-DR	H	Exit1-DR
H	Update-DR	H	Update-DR	L	Pause-DR	H	Update-DR
H	S-DR-S	L	R-T/I			H	S-DR-S
H	S-IR-S					H	S-IR-S
H	T-L-R					L	Capture-IR
						H	Exit1-IR
						L	Pause-IR

Table 12. TMS Sequencing From TAP State Shift-IR

FROM SHIFT-IR (TMS = L) TO:							
TEST-LOGIC-RESET		RUN-TEST-IDLE		PAUSE-DR		PAUSE-IR	
NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE	NEXT TMS	NEXT TAP STATE
H	Exit1-IR	H	Exit1-IR	H	Exit1-IR	H	Exit1-IR
H	Update-IR	H	Update-IR	H	Update-IR	L	Pause-IR
H	S-DR-S	L	R-T/I	H	S-DR-S		
H	S-IR-S			L	Capture-DR		
H	T-L-R			H	Exit1-DR		
				L	Pause-DR		

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
 SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

state diagram description

The state diagram shown in Figure 8 is in accordance with IEEE Std 1149.1-1990. The TAP controller proceeds through its states, based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at any given time.

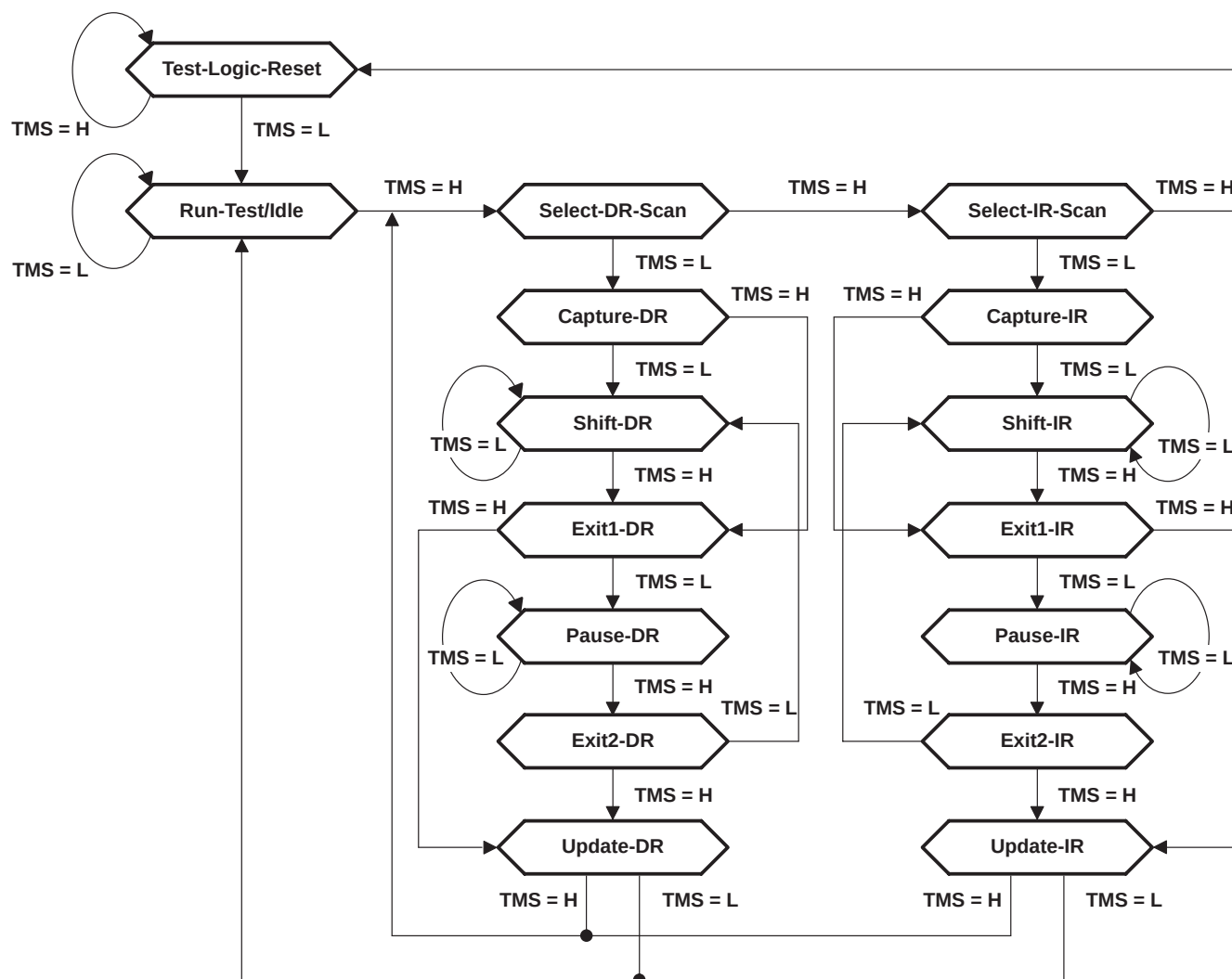


Figure 8. TAP-Controller State Diagram

Test-Logic-Reset

The eTBC TAP-state generator powers up in the Test-Logic-Reset state. Alternatively, the eTBC can be forced to this state asynchronously by assertion of its $\overline{\text{RST}}$ input or synchronously by writing the eTBC command register (bit 7-SWRST).

For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

Run-Test/Idle

For a target device, Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

Select-DR-Scan, Select-IR-Scan

For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

Capture-DR

For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the Capture-DR state is exited.

Shift-DR

For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is shifted serially through the selected data register on each TCK cycle.

Exit1-DR, Exit2-DR

For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

For target devices, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

Update-DR

For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

Capture-IR

For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the Capture-IR state is exited.

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

Shift-IR

For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is shifted serially through the instruction register on each TCK cycle.

Exit1-IR, Exit2-IR

For target devices, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

For target devices, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

Update-IR

For target devices, the current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

TDO buffer

The TDO buffer is the 4×8 -bit parallel-to-serial FIFO that accepts scan data from the host in 8-bit-parallel format and serializes it onto the TDO pin during scan operations. Scan data is expected to be transferred from the host in least-significant-byte-first order to meet IEEE Std 1149.1 requirements for least-significant-bit-first scan order. Any partial byte to be written should be justified to D0. The TDO buffer is cleared upon command initiation, so no scan data should be written to the TDO buffer before writing a scan command to the command register.

The TDO-buffer status (not full/full) is maintained in the status register (bit 6, TDOS). When the TDO-buffer status is full, writes to the TDO buffer is held off by RDY inactive and if the write cycle is aborted prior to RDY active, the write data is ignored.

For the convenience and efficiency of operating scans to the target for which outgoing data is not required, the eTBC supports special classes of input-only and recirculate scan commands that do not require nor operate the TDO buffer and so, the host need not perform any write access to it. While the input-only scan commands are operating, the TDO pin outputs a fixed high level. While the recirculate scan commands are operating, the TDO pin recirculates to the target the data that is received at TDI.

While the eTBC is in discrete-control mode, the TDO buffer is not used; instead, the state of the TDO pin is determined by the contents of the discrete-control register. Thus, TMS/TDO sequences that cannot be generated automatically still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the TDO-buffer output can be selected for loopback into the TDI buffer. When this TDO-loopback mode is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TDO buffer is cleared and assumes its not-full state.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

TDI buffer

The TDI buffer is the serial-to-4 × 8-bit parallel FIFO that serially receives data at the TDI pin and makes it available in 8-bit parallel format for reading by the host. Scan data is expected to be transferred from the IEEE Std 1149.1 targets in least-significant-bit-first order and is made available for host read in least-significant-byte-first order. The last data available for host read during a scan command may be a partial byte, in which case it is justified to D0.

The TDI-buffer status (empty/not empty) is maintained in the status register (bit 7, TDIS). When the TDI-buffer status is empty, reads to the TDI buffer is held off by RDY inactive and, if the read cycle is aborted prior to RDY active, the read data is invalid.

The TDI buffer is able to automatically accommodate retiming (pipeline) delays to the target. While operating a scan command, TDI sampling is delayed by a number of TCK cycles, equal to a value given in the configurationB register (bits 3–0, RDLY), following the generation of Shift-DR or Shift-IR state, as appropriate.

For the convenience and efficiency of operating scans to the target for which incoming data is not required, the eTBC supports a special class of output-only scan commands that neither require nor operate the TDI buffer. While the output-only scan commands are operating, the data received at TDI is ignored and the host need not perform any read access to the TDI buffer.

While the eTBC is in discrete-control mode, the TDI buffer is not used; instead, the state of the TDO pin is observed in the discrete-control register. Thus, TMS/TDO sequences that cannot be generated automatically still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the input to the TDI buffer can be selected for loopback from either TDO buffer or TAP-state (TMS) generator. When either of these loopback modes is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TDI buffer is cleared and assumes its empty state.

discrete control

The discrete-control block provides the multiplexing and control logic required to support the eTBC's discrete-control mode, in addition to its automatic modes. While the eTBC is in discrete-control mode, the TAP signals are fully controllable/accessible to the host via reads/writes to the discrete-control register. No commands can be initiated/operated while the eTBC is in the discrete-control mode.

Upon eTBC reset (power up, hardware initiated, or software initiated), the discrete-control mode is inactive.

reset

The eTBC provides three mechanisms for comprehensive and equivalent reset – power-up reset, hardware-initiated reset ($\overline{\text{RST}}$), and software-initiated reset (SWRST, bit 7 of command register) to the following effect:

- All eTBC registers are reset to default values as given in Table 1.
- The command/control logic is fully reset.
- The counter is cleared/unloaded. The TDO buffer and TDI buffer are cleared/emptied.
- The TAP-state generator is reset to the Test-Logic-Reset TAP state.
- TDO, TMS, and $\overline{\text{TRST}}$ output high levels; TCK outputs CLKIN/16.

As a consequence, the IEEE Std 1149.1 targets can be expected to be driven synchronously to the Test-Logic-Reset state no later than the fifth rising edge of TCK (72 CLKIN cycles).

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): D, RDY	–0.5 V to $V_{CC} + 0.5$ V
TCK, TDO, TMS, $\overline{TRST}$	–0.5 V to 7 V
Current into any output in the low state, I_{OL} : SN54LVT8980 (D, RDY)	12 mA
SN54LVT8980 (TCK, TDO, TMS, $\overline{TRST}$)	96 mA
SN74LVT8980 (D, RDY)	12 mA
SN74LVT8980 (TCK, TDO, TMS, $\overline{TRST}$)	128 mA
Current into any output in the high state, I_{OH} (see Note 2): SN54LVT8980 (D, RDY)	16 mA
SN54LVT8980 (TCK, TDO, TMS, $\overline{TRST}$)	48 mA
SN74LVT8980 (D, RDY)	16 mA
SN74LVT8980 (TCK, TDO, TMS, $\overline{TRST}$)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O > V_{CC}$): D, RDY	50 mA
Package thermal impedance, θ_{JA} (see Note 3) DW package (low K):	81°C/W
(high K):	46°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51 for low K, and JESD 51-7 for high K.

recommended operating conditions (see Note 4)

			SN54LVT8980		SN74LVT8980		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage			5.5		5.5	V
I _{OH}	High-level output current	D, RDY		−8		−8	mA
		TCK, TDO, TMS, $\overline{\text{TRST}}$		−24		−32	
I _{OL}	Low-level output current	D, RDY		6		6	mA
		TCK, TDO, TMS, $\overline{\text{TRST}}$		48		64	
Δt/Δv	Input transition rise or fall rate			10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused control inputs (A, CLKIN, R/W) must be held high or low to prevent them from floating.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVT8980			SN74LVT8980			UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA	-1.2			-1.2			V	
V _{OH}	D, RDY	V _{CC} = MIN to MAX‡, I _{OH} = -100 μA	V _{CC} -0.2			V _{CC} -0.2			V	
		V _{CC} = 2.7 V, I _{OH} = -4 mA	2.3			2.3				
		V _{CC} = 3 V	I _{OH} = -4 mA	2.6			2.6			
			I _{OH} = - 8 mA	2.4			2.4			
	TCK, TDO, TMS, $\overline{\text{TRST}}$	V _{CC} = MIN to MAX‡, I _{OH} = -100 μA	V _{CC} -0.2			V _{CC} -0.2				
		V _{CC} = 2.7 V, I _{OH} = -8 mA	2.4			2.4				
		V _{CC} = 3 V	I _{OH} = -24 mA	2						
			I _{OH} = -32 mA				2			
V _{OL}	D, RDY	V _{CC} = MIN to MAX‡, I _{OL} = 100 μA	0.2			0.2			V	
		V _{CC} = 2.7 V	I _{OL} = 4 mA	0.55			0.55			
			I _{OL} = 6 mA	0.8			0.8			
		V _{CC} = 3 V	I _{OL} = 4 mA	0.55			0.55			
			I _{OL} = 6 mA	0.8			0.8			
	TCK, TDO, TMS, $\overline{\text{TRST}}$	V _{CC} = MIN to MAX‡, I _{OL} = 100 μA	0.2			0.2				
		V _{CC} = 2.7 V	I _{OL} = 24 mA	0.5			0.5			
		V _{CC} = 3 V	I _{OL} = 16 mA	0.4			0.4			
			I _{OL} = 32 mA	0.5			0.5			
			I _{OL} = 48 mA	0.55						
			I _{OL} = 64 mA				0.55			
I _I	A, CLKIN, $\overline{\text{RST}}$, R/W, $\overline{\text{STRB}}$, TDI, $\overline{\text{TOE}}$	V _{CC} = 0 or MAX‡, V _I = 5.5 V	10			10			μA	
	A, CLKIN, R/W	V _{CC} = 3.6 V, V _I = V _{CC} or GND	±1			±1				
	$\overline{\text{RST}}$, $\overline{\text{STRB}}$, TDI, $\overline{\text{TOE}}$	V _{CC} = 3.6 V, V _I = V _{CC}	1			1				
		V _{CC} = 3.6 V, V _I = 0	-40	-100	-40	-100				
I _{off}	TCK, TDO, TMS, $\overline{\text{TRST}}$	V _{CC} = 0, V _I or V _O = 0 to 4.5 V	±100			±100			μA	
I _{OZH}	D, TCK, TDO, TMS, $\overline{\text{TRST}}$	V _{CC} = 3.6 V, V _O = 3 V	5			5			μA	
I _{OZL}	D, TCK, TDO, TMS, $\overline{\text{TRST}}$	V _{CC} = 3.6 V, V _O = 0.5 V	-5			-5			μA	
I _{OZPU} §	TCK, TDO, TMS, $\overline{\text{TRST}}$	$\frac{V_{CC}}{\text{TOE}}$ = 0 to 1.5 V, V _O = 0.5 V to 3 V, $\overline{\text{TOE}}$ = 0	±100			±100			μA	
I _{OZPD} §	TCK, TDO, TMS, $\overline{\text{TRST}}$	$\frac{V_{CC}}{\text{TOE}}$ = 1.5 V to 0, V _O = 0.5 V to 3 V, $\overline{\text{TOE}}$ = 0	±100			±100			μA	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This parameter is characterized, but not tested.

SN54LVT8980, SN74LVT8980

EMBEDDED TEST-BUS CONTROLLERS

IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	SN54LVT8980			SN74LVT8980			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
I _{CC}	Outputs high	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	0.5			0.5			mA
	Outputs low		7			7			
	Outputs disabled		0.5			0.5			
ΔI _{CC} [¶]		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	0.2			0.2			mA
C _i		V _I = 3 V or 0	4			4			pF
C _{io}		V _O = 3 V or 0	5			5			pF
C _O		V _O = 3 V or 0	7			7			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 9 and 10)

			SN54LVT8980				SN74LVT8980				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency, CLKIN		TCK = CLKIN (CDIV = 0)	0	20	0	16	0	20	0	16	MHz
			TCK = CLKIN/2 (CDIV = 1)	0	40	0	32	0	40	0	32	
			TCK ≤ CLKIN/4 (CDIV ≥ 2)	0	70	0	64	0	70	0	64	
t _w	Pulse duration	CLKIN high or low	TCK = CLKIN (CDIV = 0)	25		31		25		31		ns
			TCK = CLKIN/2 (CDIV = 1)	12.5		15.5		12.5		15.6		
			TCK ≤ CLKIN/4 (CDIV ≥ 2)	7.1		7.8		7.1		7.8		
		RST low		10		10		10		10		
		STRB low		8		8		8		8		
t _{su}	Setup time	A before STRB↓ Read or write (R/W high or low)	10		10		10		10		ns	
		D before STRB↑ Write (R/W low)	5		5		5		5			
		R/W before STRB↓	5		5		5		5			
		TDI before CLKIN↑	5		5		5		5			
t _h	Hold time	A after STRB↑ Read or write (R/W high or low)	5		5		5		5		ns	
		D after STRB↑ Write (R/W low)	15		15		15		15			
		R/W after STRB↑		6		6		6		6		
		TDI after CLKIN↑		10		10		10		10		

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

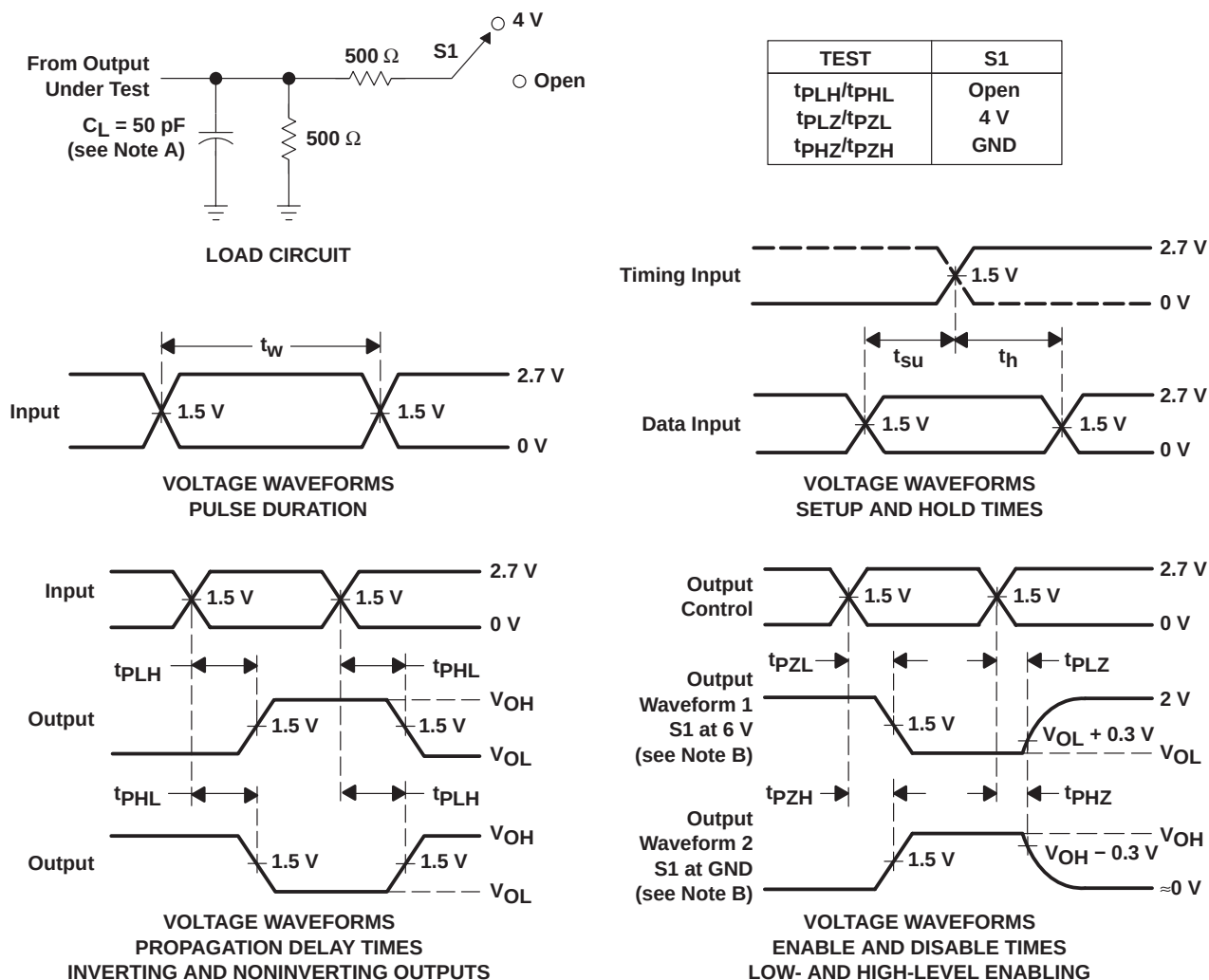
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 9 and 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT8980				SN74LVT8980				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
tPLH	CLKIN	TCK	6	20	25		6	10	17	20		ns
tPHL			6	20	25		6	10	17	20		
tPLH	CLKIN	TDO, TMS	8	35	40		8	18	30	35		ns
tPHL			8	35	40		8	18	30	35		
tPLH	$\overline{\text{RST}}\downarrow$	D	3	35	40		3	17	30	35		ns
tPHL			3	35	40		3	17	30	35		
tPLH	$\overline{\text{RST}}\downarrow$	RDY	3	35	40		3	17	30	35		ns
tPHL			3	35	40		3	17	30	35		
tPLH	$\overline{\text{RST}}\downarrow$	TDO, TMS, TRST	5	30	35		5	15	25	30		ns
tPHL		TCK	5	30	35		5	15	25	30		
tPLH	$\overline{\text{STRB}}\uparrow$	RDY	3	22	28		3	10	18	22		ns
tPHL	$\overline{\text{STRB}}\downarrow$		3	22	28		3	10	18	22		
tPLH	$\overline{\text{STRB}}\uparrow$	TCK, TDO, TMS, TRST discrete mode	3	28	35		3	14	22	28		ns
tPHL		3	28	35		3	14	22	28			
tPLH	$\overline{\text{STRB}}\uparrow$	TCK, TDO, TMS, TRST other modes	6	40	45		6	20	35	40		ns
tPHL		6	40	45		6	20	35	40			
tPZH	$\overline{\text{STRB}}\downarrow$	D	3	20	25		3	8	15	18		ns
tPZL			3	20	25		3	8	15	18		
tPZH	$\overline{\text{STRB}}\uparrow$	TCK, TDO, TMS, TRST	5	30	35		5	15	25	30		ns
tPZL		5	30	35		5	15	25	30			
tPZH	$\overline{\text{TOE}}\downarrow$	TCK, TDO, TMS, TRST	2	15	18		2	6	12	15		ns
tPZL		2	15	18		2	6	12	15			
tPHZ	$\overline{\text{STRB}}\uparrow$	D	3	20	25		3	8	15	18		ns
tPLZ			3	20	25		3	8	15	18		
tPHZ	$\overline{\text{STRB}}\uparrow$	TCK, TDO, TMS, TRST	5	30	35		5	15	25	30		ns
tPLZ		5	30	35		5	15	25	30			
tPHZ	$\overline{\text{TOE}}\uparrow$	TCK, TDO, TMS, TRST	2	15	18		2	6	12	15		ns
tPLZ		2	15	18		2	6	12	15			

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
 SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

PARAMETER MEASUREMENT INFORMATION

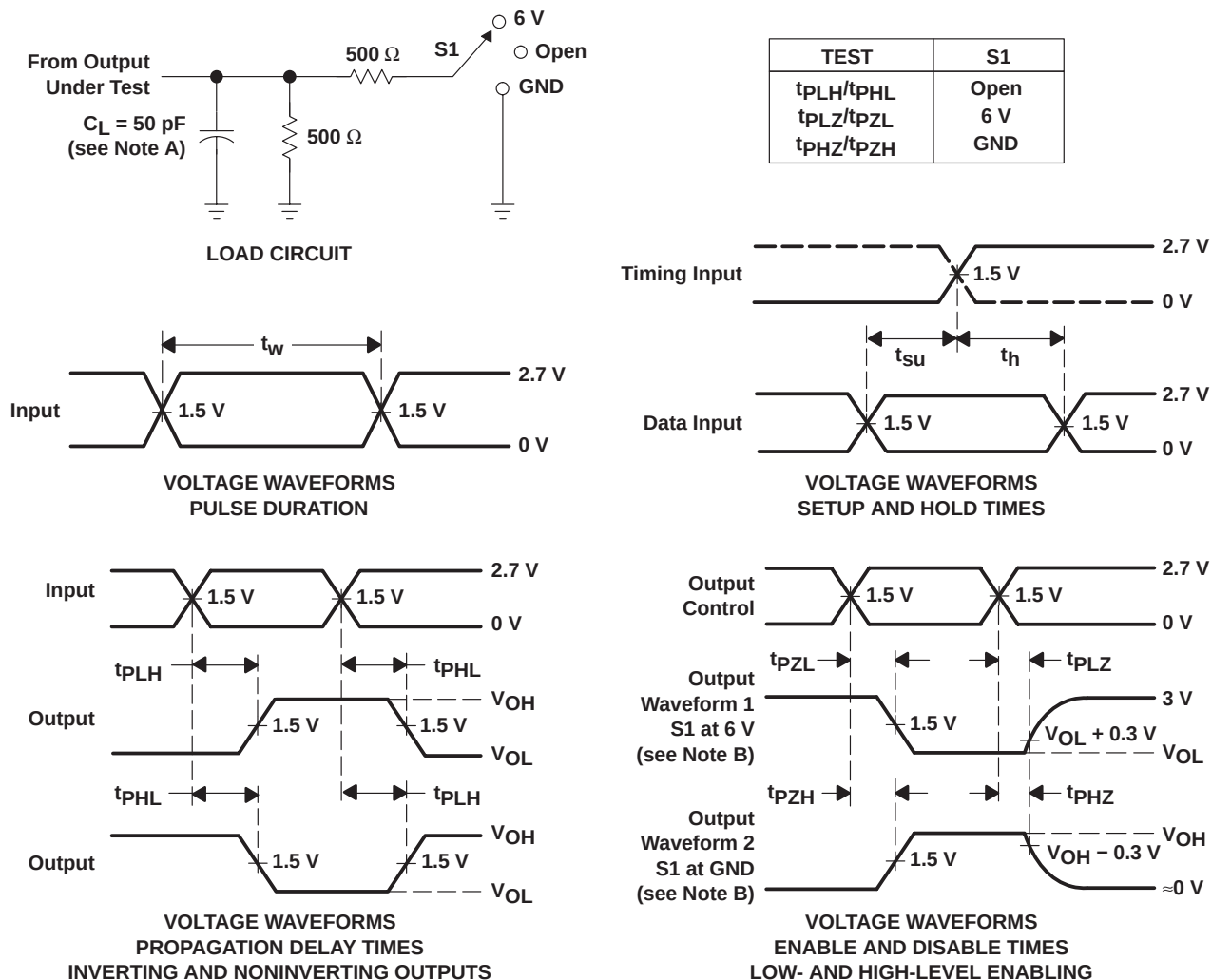


- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 9. Load Circuit and Voltage Waveforms (D and RDY Outputs)

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

PARAMETER MEASUREMENT INFORMATION



- NOTES: E. C_L includes probe and jig capacitance.
 F. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 G. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 H. The outputs are measured one at a time, with one transition per measurement.

Figure 10. Load Circuit and Voltage Waveforms (TCK, TDO, TMS, $\overline{TRST}$ Outputs)

SN54LVT8980, SN74LVT8980 EMBEDDED TEST-BUS CONTROLLERS IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

silicon errata

The descriptions and specifications included in this data sheet represent the intended performance of the 'LVT8990 device. In most cases, these descriptions and specifications also represent the actual performance of silicon of a given revision. Specific exceptions are noted here. **In all cases listed here, subsequent release of the 'LVT8980 "A" correctly specifies or fixes these problems.**

item 1 – operation of host interface ($\overline{\text{STRB}}$) asynchronous to CLKIN

The host interface, which is timed by $\overline{\text{STRB}}$, is intended to be, and properly should be, fully asynchronous relative to CLKIN. In short, the device should function as described in this data sheet, regardless of the timing relationship between applied $\overline{\text{STRB}}$ and CLKIN.

The 'LVT8990 "X" die, however, fails to function properly when $\overline{\text{STRB}}$ is not synchronous to CLKIN. Specifically, $\overline{\text{STRB}}$ must be applied, considering adequate setup time requirements, as follows:

	SN74LVT8980				UNIT
	$V_{CC} = 3.3 \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		
	MIN	MAX	MIN	MAX	
t_{SU} $\overline{\text{STRB}}$ high before CLKIN↑	25		25		ns

Subsequent release of the 'LVT8980 "A" corrects the host interface synchronous problem described here.

workaround

For an 'LVT8980 "X" die design, always operate the host interface (specifically, $\overline{\text{STRB}}$) synchronously to CLKIN, maintaining setup time requirements as given above. In most applications, this means that the eTBC CLKIN is driven from the same original clock source as the host CPU.

item 2 – read of TDI buffer while it is empty (not ready)

When a read is made to the TDI buffer while it is empty (not ready), the RDY pin signal is specified to go low, indicating that the eTBC presently is not ready to service the requested access. If, while $\overline{\text{STRB}}$ is held low, subsequent processing of a scan command fills a byte in the TDI buffer, the RDY pin signal is specified to return high, indicating that the eTBC is ready to complete the access. Correspondingly, the available byte of data from the TDI buffer should be latched onto the data bus such that the host can access this data.

The 'LVT8990 "X" die, however, does not function properly with respect to the actual data latched to the data bus. That is, if a read is made to TDI buffer while it is empty (not ready), the RDY pin signal will go low as specified; also, if the $\overline{\text{STRB}}$ pin signal is held low, and further processing of a scan command fills a byte in the TDI buffer, the RDY pin signal will return high, as specified. However, at the same time that RDY returns high, the TDI data byte should be latched onto the data bus. If this does not occur, the data that does appear on the data bus is not valid.

Subsequent release of the 'LVT8980 "A" corrects the read of the TDI buffer, while empty, as described here.

workaround

For an LVT8990 "X" design, always poll the TDI buffer (read status register, bit 7, TDIS) to ensure that it is ready prior to a desired read to TDI buffer. Of course, such a software-pollled mode versus the hardware-inserted wait-states (RDY) mode (as originally specified, and as proposed to be fixed in 'LVT8980 "A" device revision) will place more overhead on the CPU and likely reduce throughput as well.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

item 3 – incorrect operation when using retiming (pipeline) delays

When setting bits 3-0 of the ConfigurationB register to any non-zero value, the eTBC intends to delay TDI sampling by a number of TCK cycles. The feature would be used to accommodate retiming (pipeline) delays from the target scan chains that are electrically distant from the eTBC. This delay is equal to the value set in the RDLY bit group and has a maximum value of 15.

The 'LVT8980 "X" die, however, does not function properly with respect to the use of retiming delays in gated-TCK mode. Specifically, when operating in these modes, the eTBC may drop bits. When using retiming delays and free-running-TCK mode, the eTBC does not know when to jump to PAUSE or properly set the TDI buffer status in the Status register. In either TCK mode described here, the status register does not properly indicate when the TDO buffer is full.

Subsequent release of the 'LVT8980 "A" corrects the operation of retiming delays as described here. When using retiming delays, the 'LVT8980 "A" allows the maximum number of TDO writes minus TDI reads to be four, compared to five, as proposed in the 'LVT8980 "X".

workaround

For an 'LVT8980 "X" design, retiming delays should not be used. Any required retiming must be handled with additional logic that interfaces to the eTBC.

item 4 – when in discrete mode, reads and writes to any register will cause TCK to toggle

When in discrete mode, the eTBC is specified to poll the TDI input and post values on the TDO, TMS, and $\overline{\text{TRST}}$ outputs based on contents of the Discrete-Control register. The TCK output is specified to toggle during reads and writes to the Discrete-Control register. Reads generate TCK rising edge, and writes generate TCK falling edge.

The 'LVT8980 "X" die functions correctly when reading and writing to the Discrete-Control register. However, when in discrete mode and reading or writing to any register, the eTBC generates TCK rising edges and falling edges, respectively. The intended operation is to toggle TCK only when reading or writing to the Discrete-Control register.

Subsequent release of the 'LVT8980 "A" corrects the discrete mode problem as described here.

workaround

For an 'LVT8980 "X" design, when in discrete mode, reading or writing to registers other than the Discrete-Control register should be avoided.

item 5 – output pulse glitch on RDY output

When attempting to write to or read any of the eTBC registers, if any condition exists to prevent that operation, RDY will be asserted low in response to the low transition on $\overline{\text{STRB}}$. If RDY remains high when $\overline{\text{STRB}}$ goes low, it should remain high for the duration of the low state of $\overline{\text{STRB}}$.

The 'LVT8980 "X" die, however, does not function properly with respect to RDY remaining high throughout the duration of the low state of $\overline{\text{STRB}}$. In certain cases, while performing writes to the TDO register, RDY may glitch low for several nanoseconds, then return high. This glitch always follows a high transition on the internal TCK, which always follows a high transition on CLKIN.

Subsequent release of 'LVT8980 "A" die corrects the problem as described here. If RDY does not go low, following a low transition on $\overline{\text{STRB}}$, then it will stay high for the duration of the low state of $\overline{\text{STRB}}$.

workaround

For an 'LVT8980 "X" design, the user should not use transitions on RDY to trigger logic events. Also, while $\overline{\text{STRB}}$ is held low during TDO writes, the user should not rely on the accuracy of the state of RDY until approximately 15 ns, following a high transition of CLKIN.

SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES

SCBS676E – DECEMBER 1996 – REVISED MARCH 2004

item 6 – command register internal reset can cause subsequent command writes to be ignored

When the command register is empty, the eTBC should allow for subsequent commands to be written and accepted as long as an internal reset is complete. The internal reset lasts for a small number of TCK cycles, and the eTBC should block subsequent writes to the command register via the RDY output until the internal reset is complete.

The 'LVT8980 "X" die, however, does not function properly with respect to blocking subsequent command writes with the RDY pin. The command register can be empty, and a new command can be written prior to internal reset completion. In this case, a subsequent command write could be ignored.

Subsequent release of 'LVT8980 "A" die corrects the problem as described here. Once the command register is empty, a new command can be written and will be accepted immediately.

workaround

For an 'LVT8980 "X" design, the user should wait at least one full TCK cycle before writing a subsequent command to the empty command register. The TCK cycle length will depend on the CLKIN frequency and clock divisor (CDIV) selected. These values should be known, even if the eTBC is operating in gated-TCK mode.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
1L8980DWRG4	NRND	SOIC	DW	24		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT8980DW	OBSOLETE	SOIC	DW	24		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT8980DWR	OBSOLETE	SOIC	DW	24		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

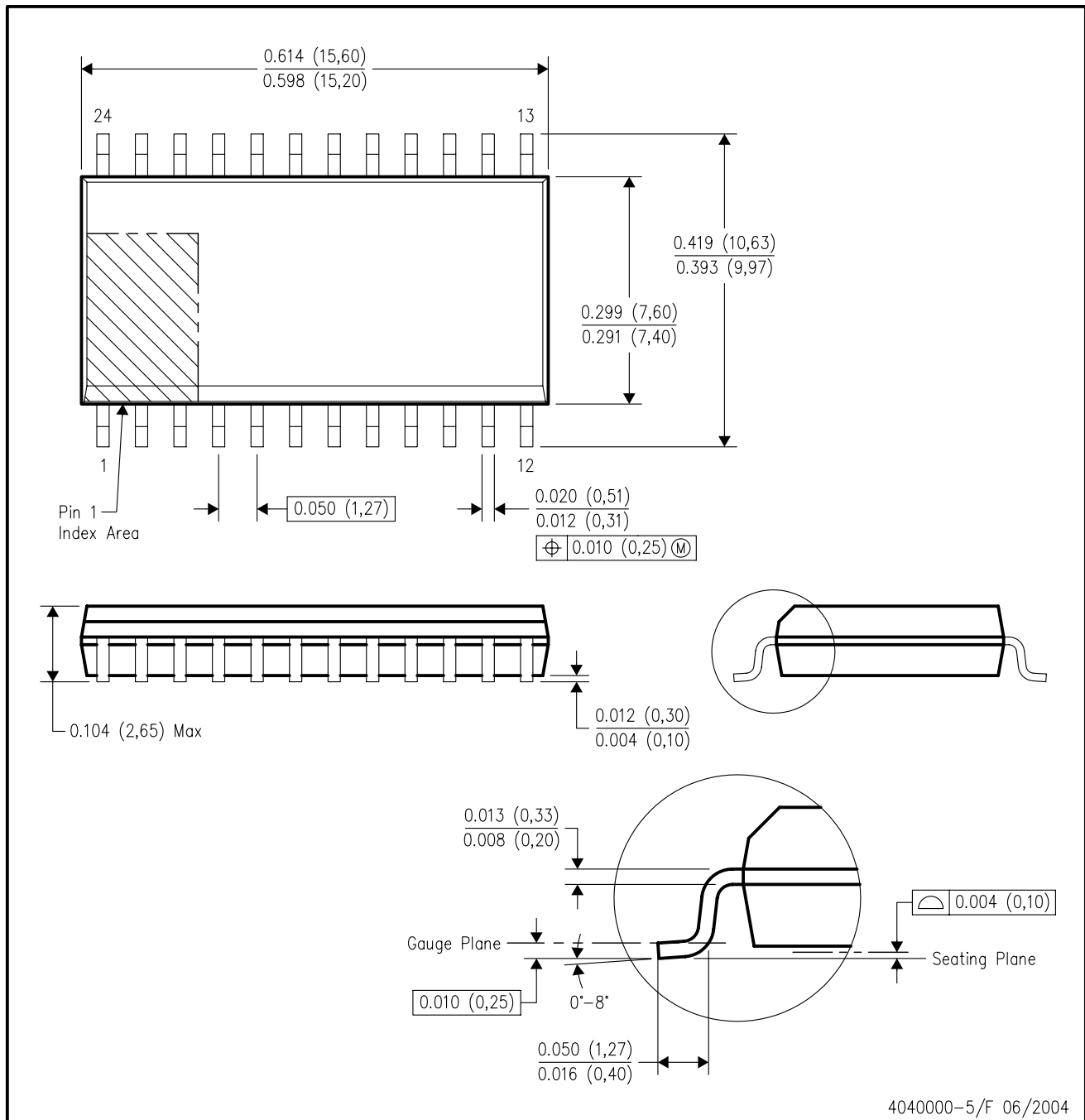
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265