SANYO

No.2458

2SA1572/2SC4067

PNP/ NPN Epitaxial Planar Silicon Transistors

Switching Applications (with Bias Resistance)

Applications

. Switching circuit, inverter circuit, interface circuit, driver circuit

Features

. On-chip bias resistance: R1=0, R2=47kΩ
. Small-sized package: SPA

( ): PNP

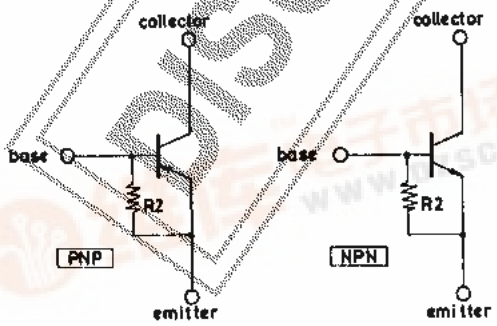
Absolute Maximum Ratings at Ta=25°C

			unit
Collector to Base Voltage	V_{CBO}	(-)50	V
Collector to Emitter Voltage	V_{CEO}	(-)50	V
Emitter to Base Voltage	V_{EBO}	(-)5	V
Collector Current	I_C	(-)100	mA
Collector Current(Pulse)	I_{CP}	(-)200	mA
Collector Dissipation	P_C	300	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55 to +150	°C

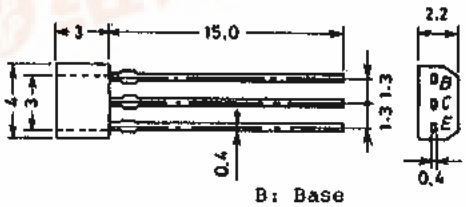
Electrical Characteristics at Ta=25°C

			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	V_{CB}=(-)40V, I_E=0			(-)0.1	μA
	I_{CEO}	V_{CE}=(-)40V, I_B=0			(-)0.5	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(-)5V, I_C=0	(-)81	(-)106	(-)151	μA
DC Current Gain	h_{FE}	V_{CE}=(-)5V, I_C=(-)10mA	80			
Gain-Bandwidth Product	f_T	V_{CE}=(-)10V, I_C=(-)5mA		250 (200)		MHz
Output Capacitance	C_{ob}	V_{CB}=(-)10V, f=1MHz		3.7 (5.5)		pF
C-E Saturation Voltage	$V_{CE(sat)}$	I_C=(-)10mA, I_B=(-)0.5mA		(-)0.1	(-)0.3	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	I_C=(-)10μA, I_E=0	(-)50			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	I_C=(-)100μA, R_{BE}=∞	(-)50			V
Resistance	R2		33	47	61	kΩ

Electrical Connection



Case Outline 2033
(unit:mm)



B: Base
C: Collector
E: Emitter

SANYO: SPA

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