



2SJ505(L), 2SJ505(S)

Silicon P Channel MOS FET

REJ03G0872-0500

Rev.5.00

Jun 05, 2006

Description

High speed power switching

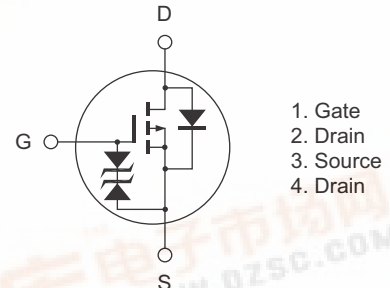
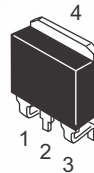
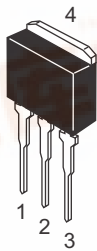
Features

- Low on-resistance
 $R_{DS(on)} = 0.017 \Omega$ typ.
- Low drive current.
- 4 V gate drive devices.
- High speed switching.

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDPAK (L))

RENESAS Package code: PRSS0004AE-B
(Package name: LDPAK (S)-(1))



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-50	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-200	A
Body to drain diode reverse drain current	I_{DR}	-50	A
Avalanche current	I_{AP} ^{Note 3}	-50	A
Avalanche energy	E_{AR} ^{Note 3}	214	mJ
Channel dissipation	P_{ch} ^{Note 2}	75	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. Value at $T_a = 25^\circ C$, $R_g \geq 50 \Omega$

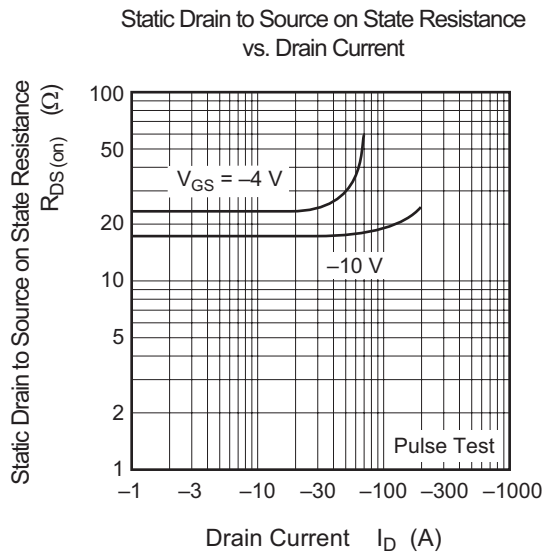
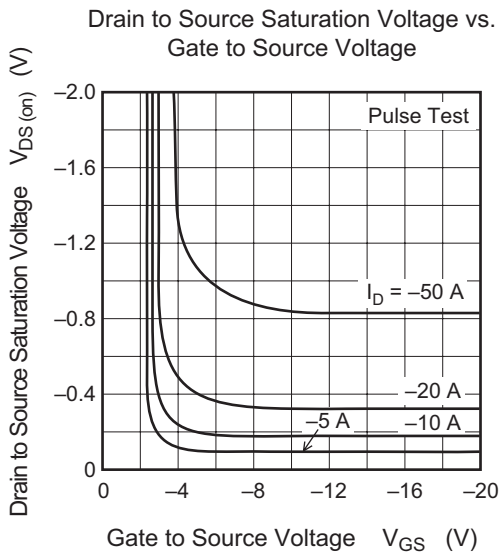
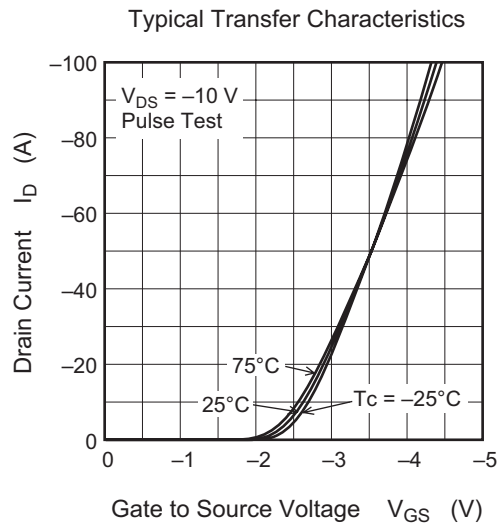
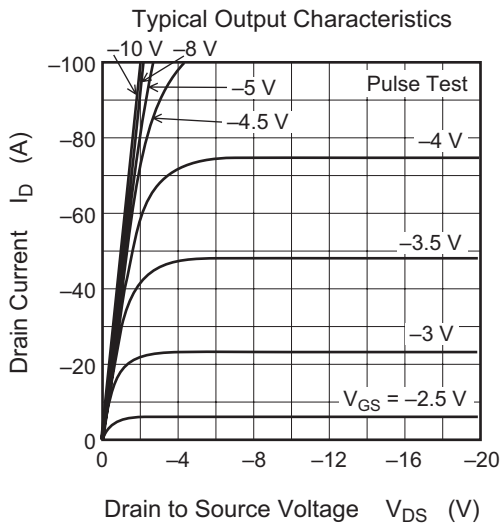
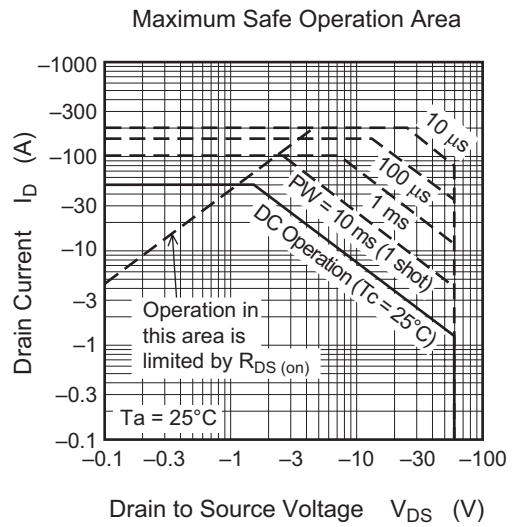
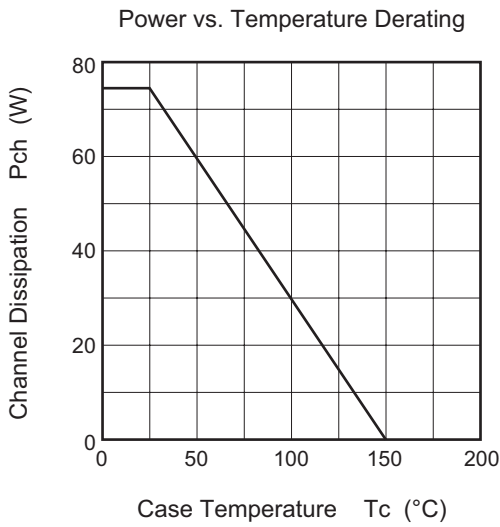
Electrical Characteristics

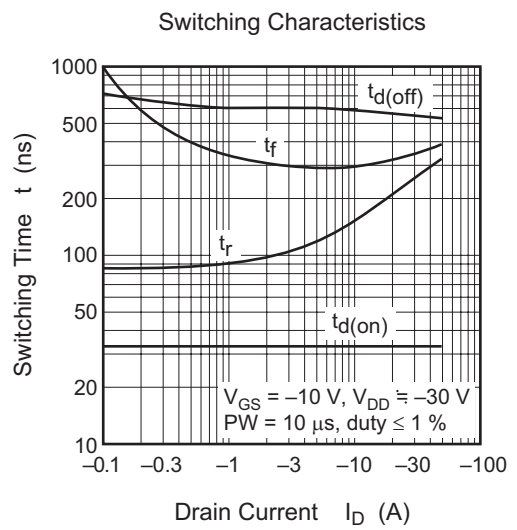
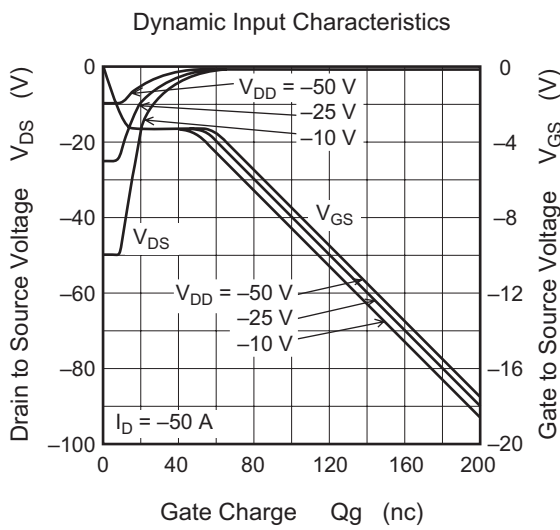
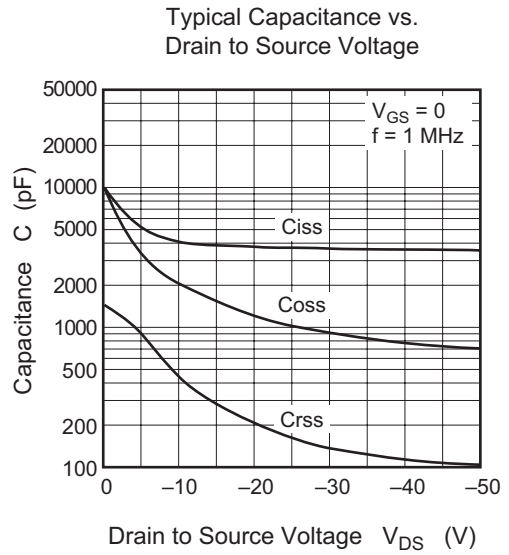
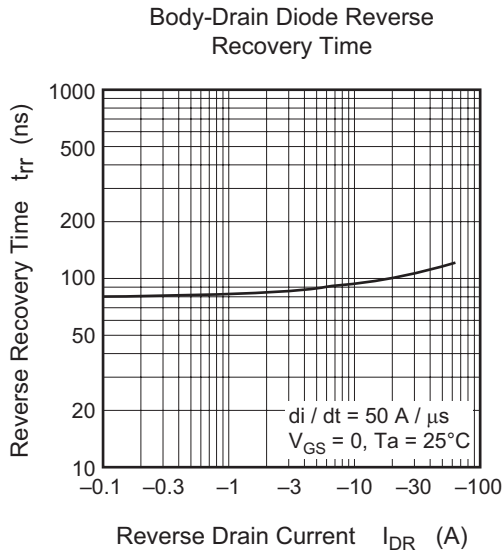
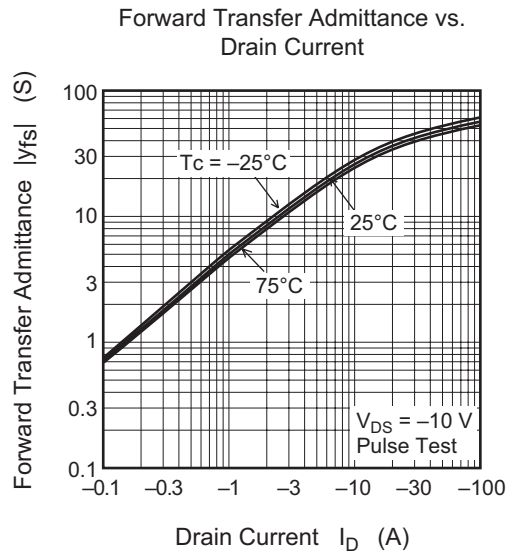
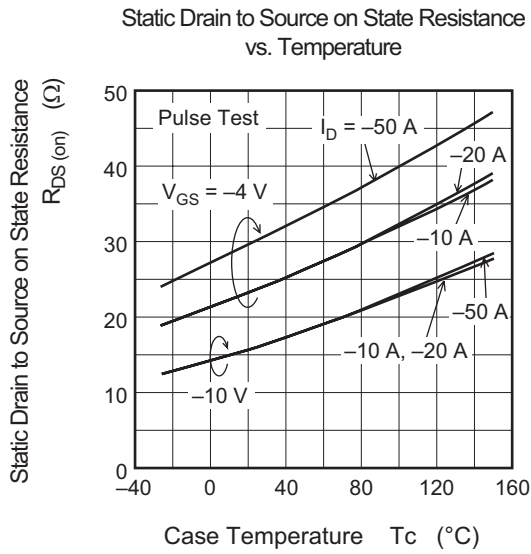
(Ta = 25°C)

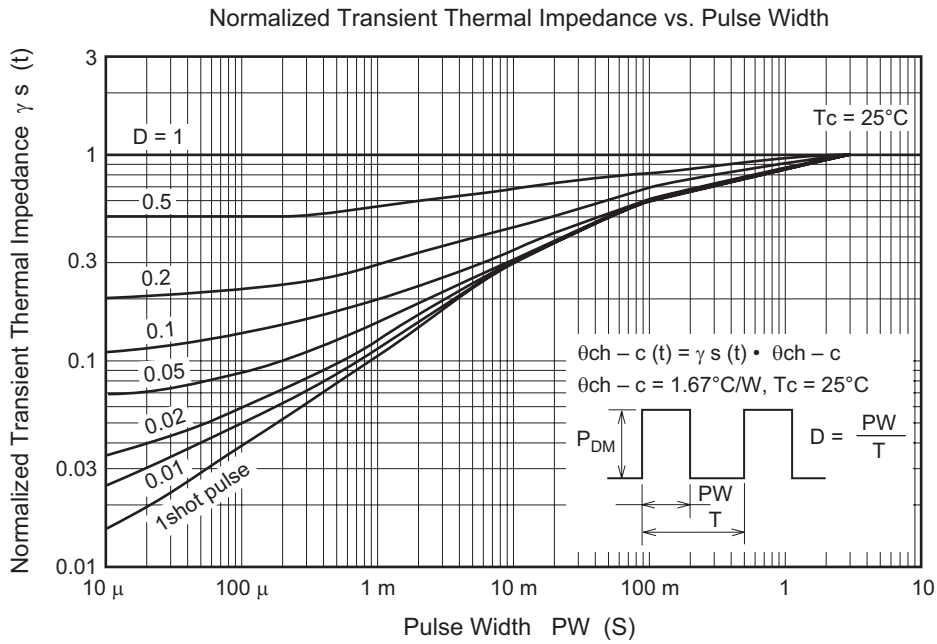
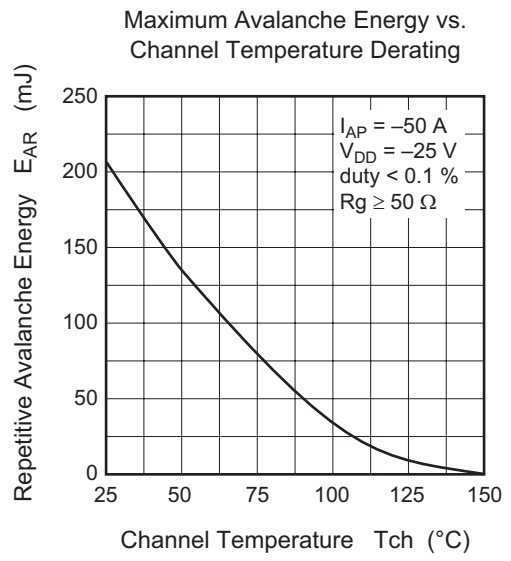
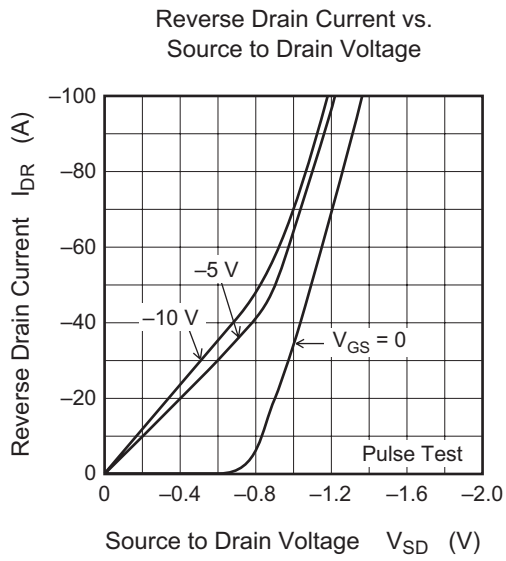
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1 \text{ mA}$, $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.017	0.022	Ω	$I_D = -25 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note 4}
	$R_{DS(on)}$	—	0.024	0.036	Ω	$I_D = -25 \text{ A}$, $V_{GS} = -4 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	27	39	—	S	$I_D = 25 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	4100	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	2100	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	450	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	32	—	ns	$V_{GS} = -10 \text{ V}$
Rise time	t_r	—	225	—	ns	$I_D = -25 \text{ A}$
Turn-off delay time	$t_{d(off)}$	—	530	—	ns	$R_L = 1.2 \Omega$
Fall time	t_f	—	330	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -50 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	110	—	ns	$I_F = -50 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$

- Note: 4. Pulse test

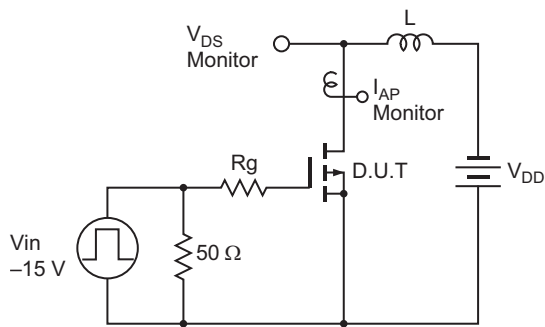
Main Characteristics



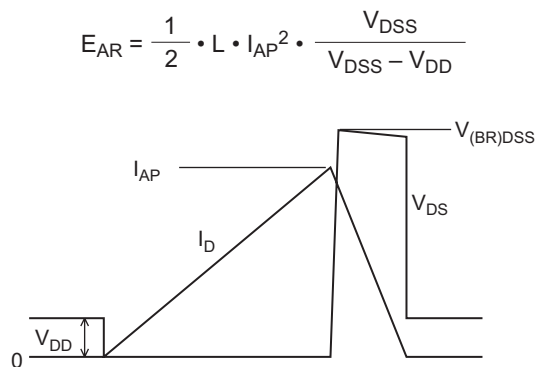




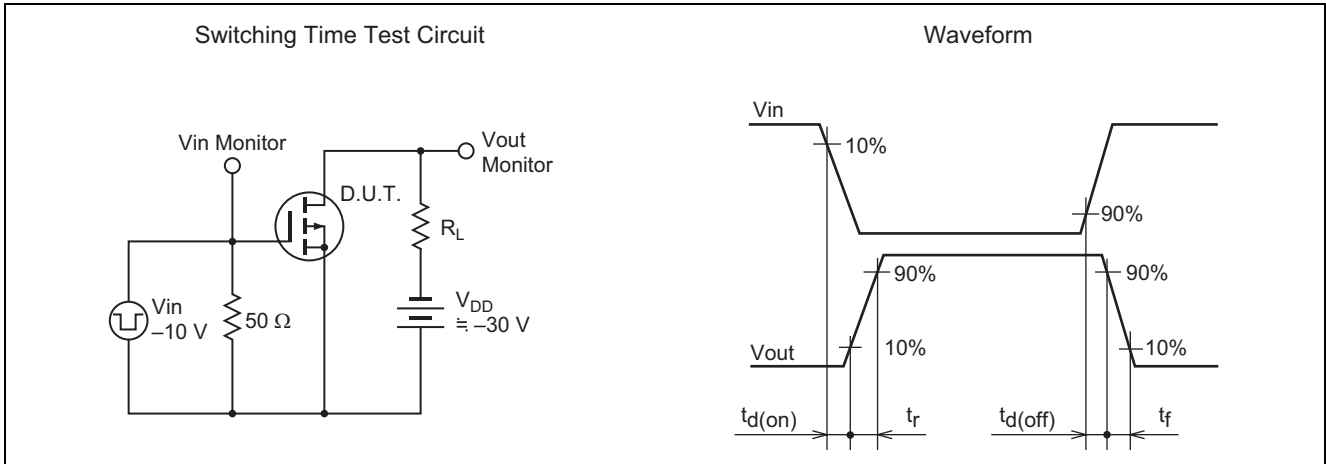
Avalanche Test Circuit



Avalanche Waveform

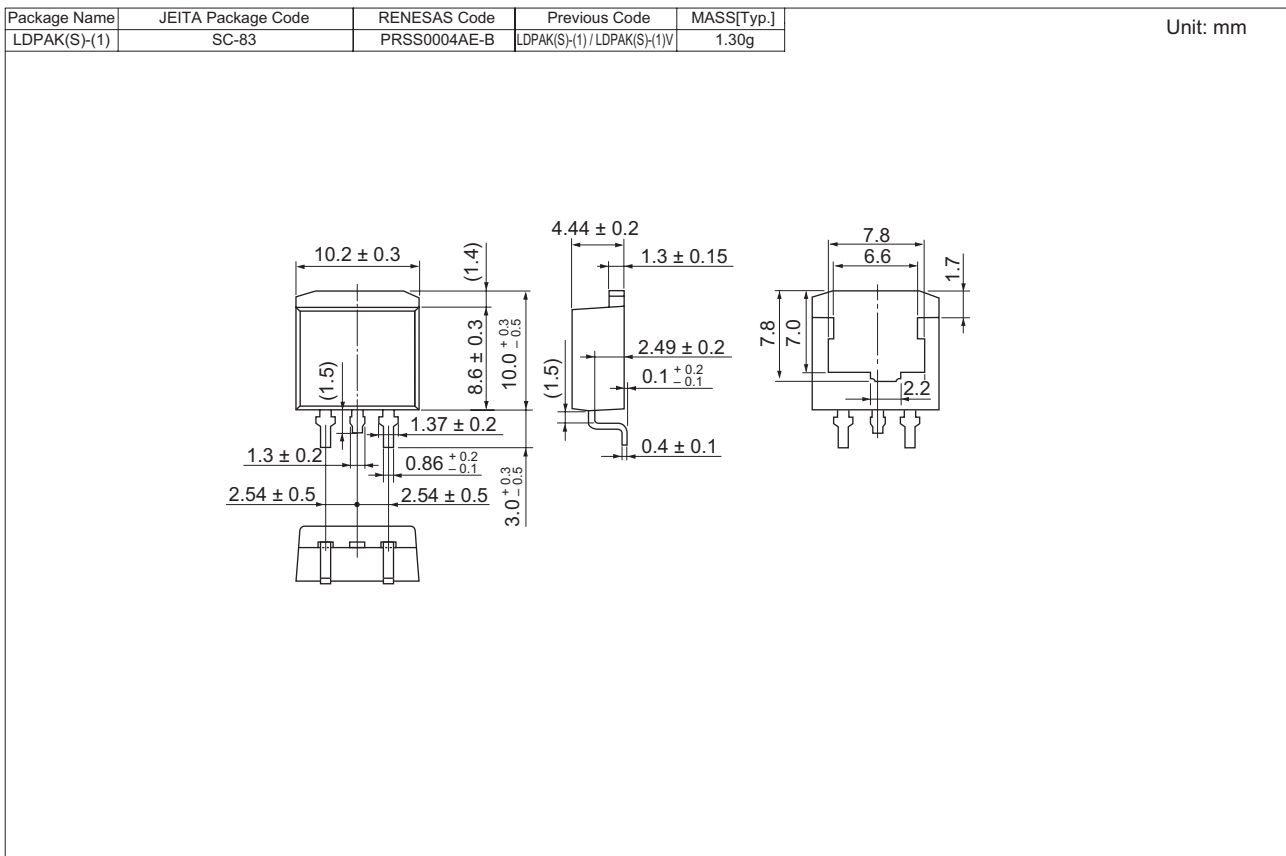
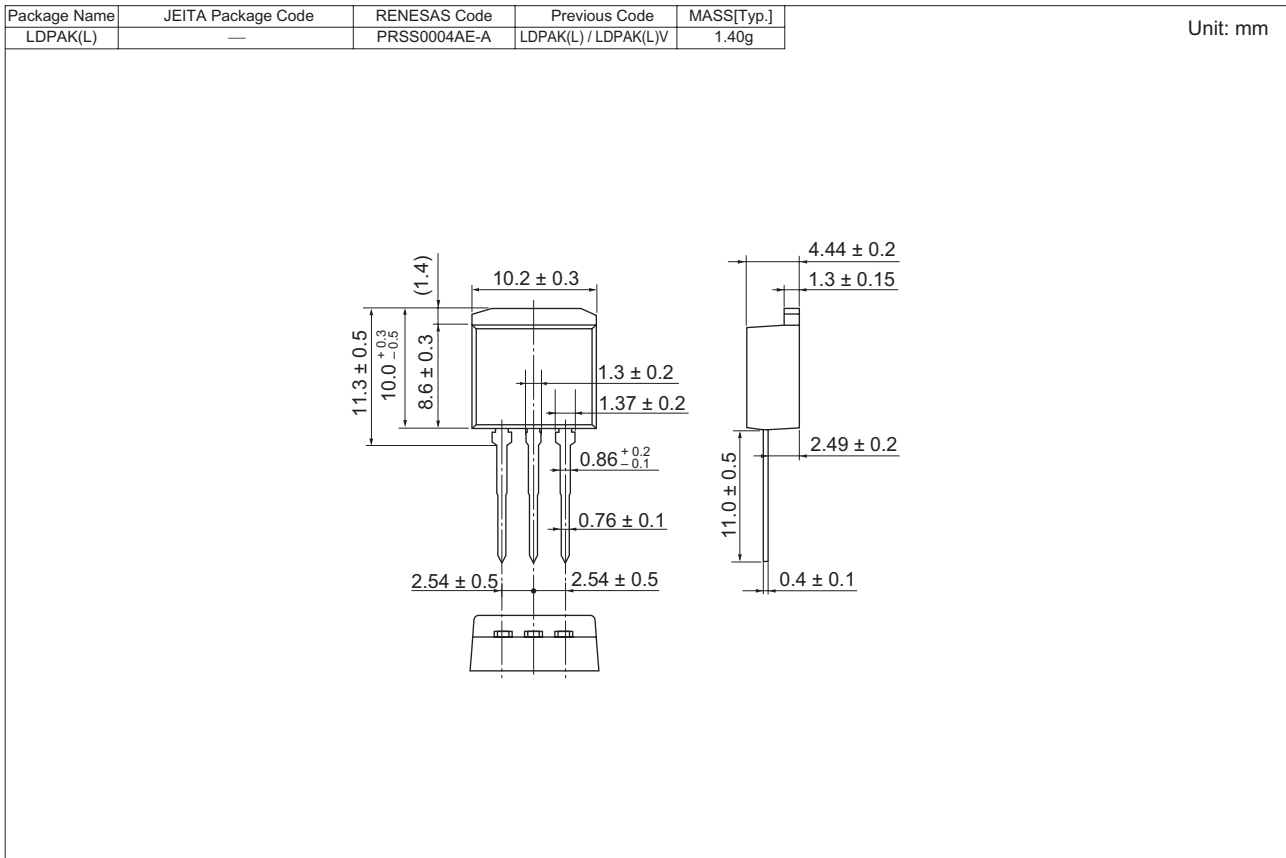


2SJ505(L), 2SJ505(S)



2SJ505(L), 2SJ505(S)

Package Dimensions



2SJ505(L), 2SJ505(S)

Ordering Information

Part Name	Quantity	Shipping Container
2SJ505L-E	500 pcs	Box (Sack)
2SJ505STL-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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