

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK702

DESCRIPTION The 2SK702 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

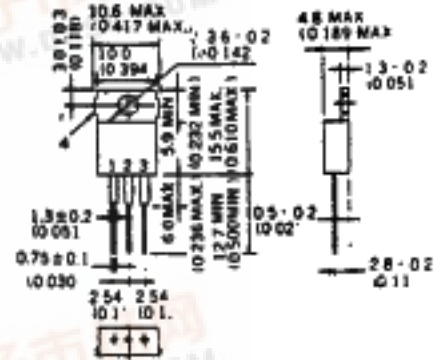
- FEATURES**
- 4 V Gate Drive – Logic level –
 - Low $R_{DS(on)}$
 - No Second Breakdown

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures	
Storage Temperature	-55 to +150 °C
Junction Temperature	150 °C Maximum
Maximum Power Dissipations	
Total Power Dissipation	1.5 W
Total Power Dissipation ($T_C = 25\text{ °C}$)	50 W
Maximum Voltages and Currents ($T_A = 25\text{ °C}$)	
V_{DS} Drain to Source Voltage	100 V
V_{GS} Gate to Source Voltage	±20 V
$I_{D(DC)}$ Drain Current (DC)	±5 A
$I_{D(pulse)}$ Drain Current (pulse)*	±20 A

* $PW \leq 300\ \mu s$, Duty Cycle $\leq 2\%$

PACAKEGE DIMENSIONS
in millimeters (inches)



1. Gate
 2. Drain
 3. Source
 4. Pin (Drain)
- JEDEC: TO-220AB

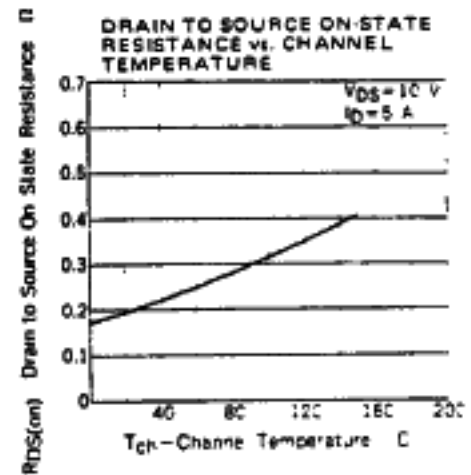
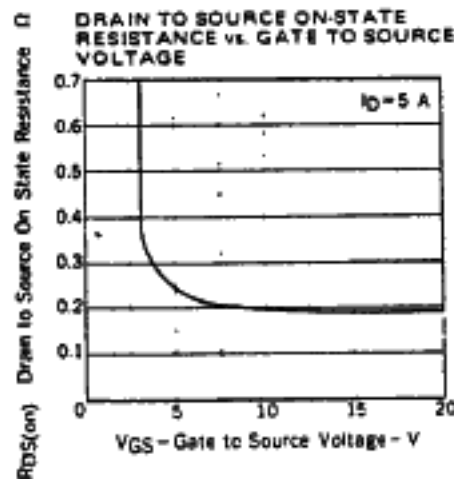
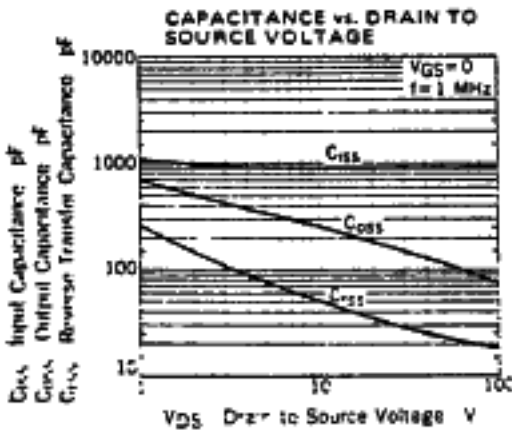
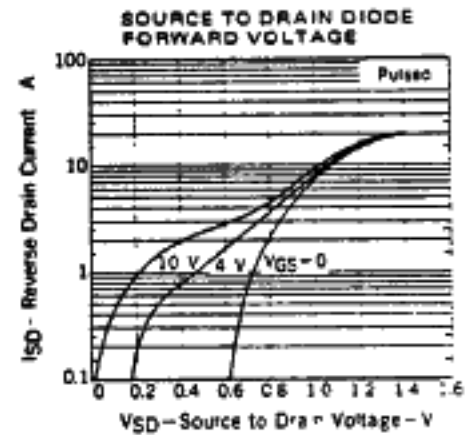
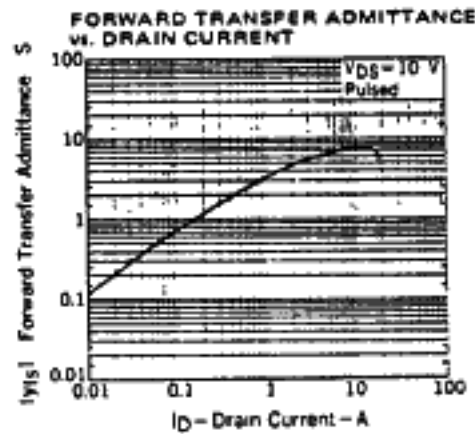
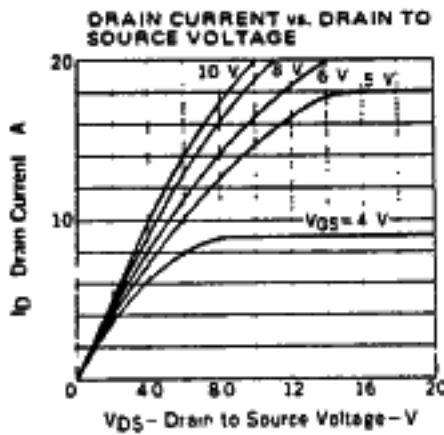
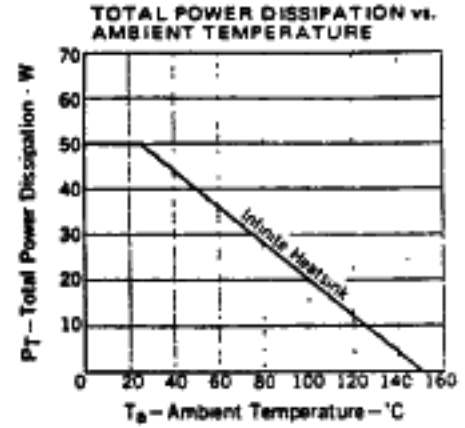
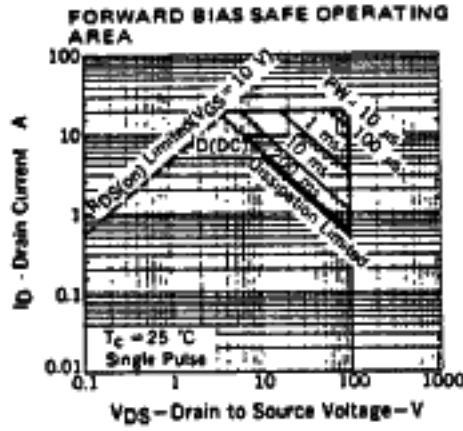
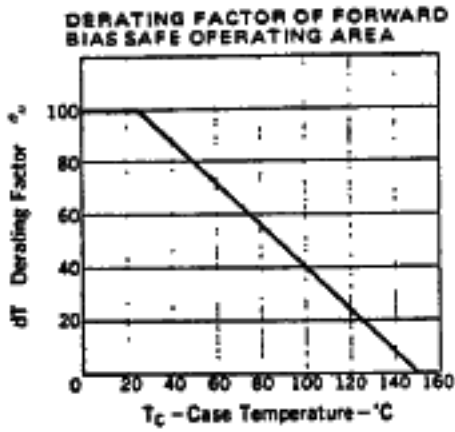
ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ °C}$)

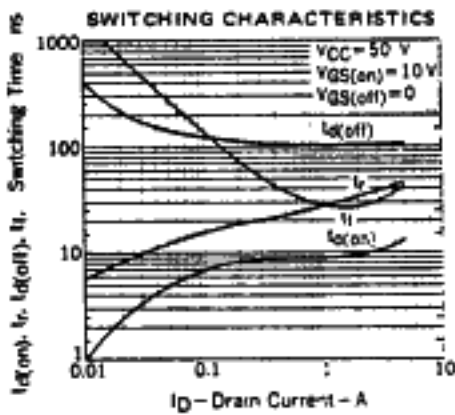
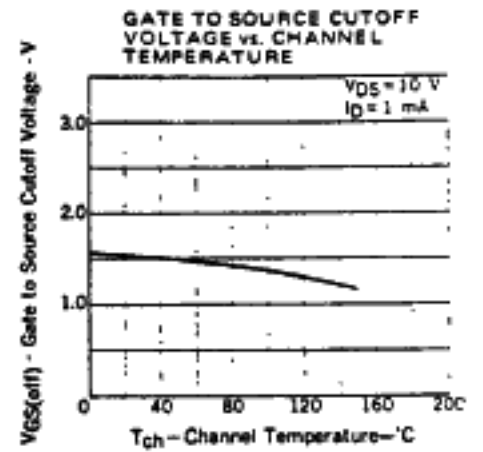
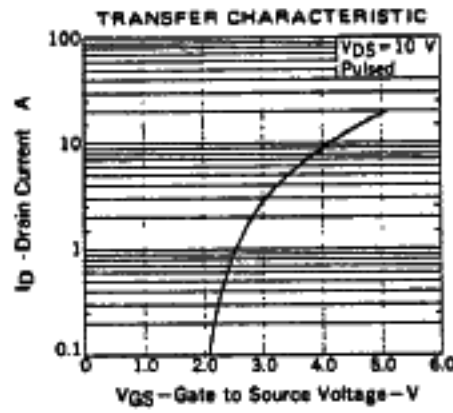
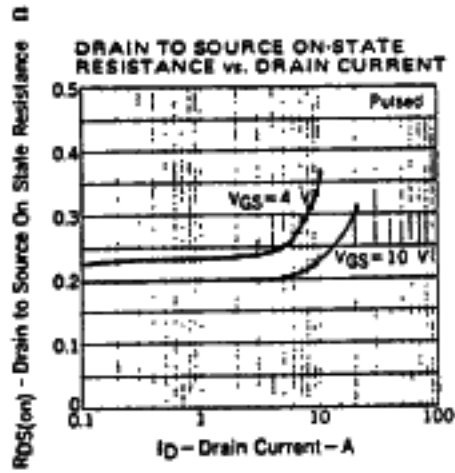
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.20	0.45	Ω	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$
$R_{DS(on)}$	Drain to Source On-State Resistance		0.25	0.50	Ω	$V_{GS} = 4\text{ V}, I_D = 5\text{ A}$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
y_{fs}	Forward Transfer Admittance	4			S	$V_{DS} = 10\text{ V}, I_D = 3\text{ A}$
I_{DSS}	Drain Leakage Current			10	μA	$V_{DS} = 100\text{ V}, V_{GS} = 0$
I_{GSS}	Gate to Source Leakage Current			±100	nA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0$
C_{iss}	Input Capacitance		900		pF	$V_{DS} = 10\text{ V}$
C_{oss}	Output Capacitance		250		pF	$V_{GS} = 0$
C_{rss}	Reverse Transfer Capacitance		50		pF	$f = 1\text{ MHz}$
$t_d(on)$	Turn On Delay Time		10		ns	
t_r	Rise Time		40		ns	$I_D = 3\text{ A}, V_{CC} = 50\text{ V}$
$t_d(off)$	Turn Off Delay Time		110		ns	$R_L = 17\ \Omega$
t_f	Fall Time		30		ns	$R_{in} = 10\ \Omega$



NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

TYPICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$)





SWITCHING TIME TEST CIRCUIT

