

TOSHIBA Field Effect Transistor Silicon N Channel Dual Gate MOS Type

## 3SK195

TV Tuner, VHF RF Amplifier Applications  
FM Tuner Applications

Unit: mm

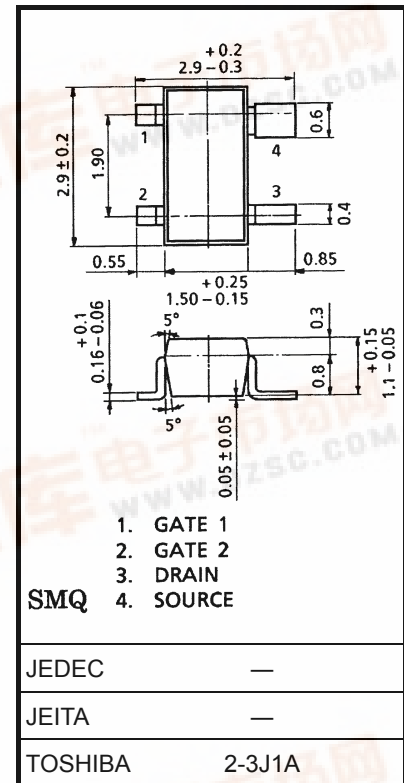
- Superior cross modulation performance.
- Low reverse transfer capacitance:  $C_{rss} = 0.015$  pF (typ.)
- Low noise figure: NF = 1.1dB (typ.)

Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DS}$	13.5	V
Gate 1-source voltage	$V_{G1S}$	$\pm 8$	V
Gate 2-source voltage	$V_{G2S}$	$\pm 8$	V
Drain current	$I_D$	30	mA
Drain power dissipation	$P_D$	150	mW
Channel temperature	$T_{ch}$	125	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	$-55 \sim 125$	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

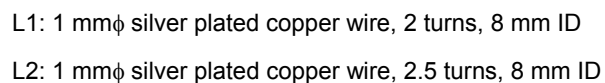
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



Weight: 0.013 g (typ.)

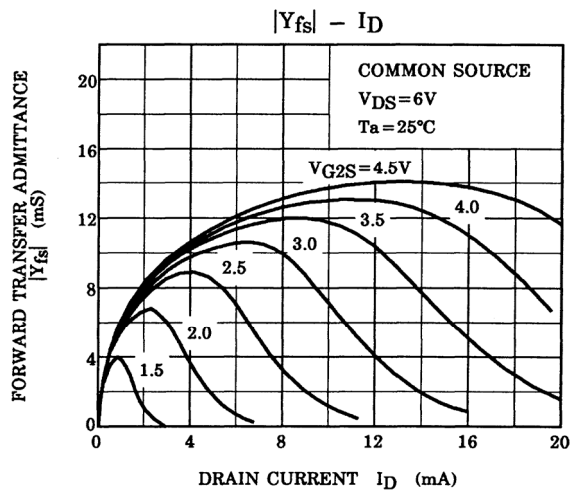
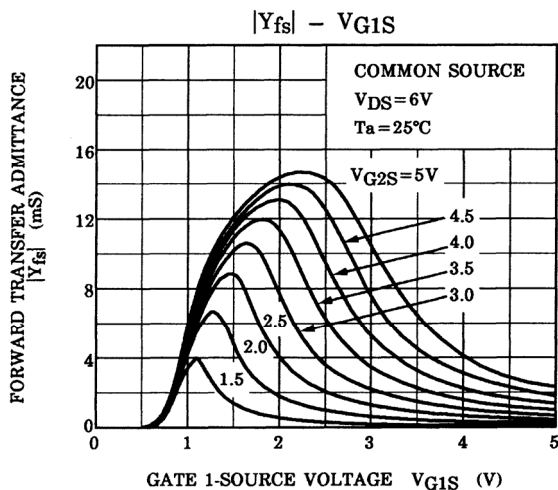
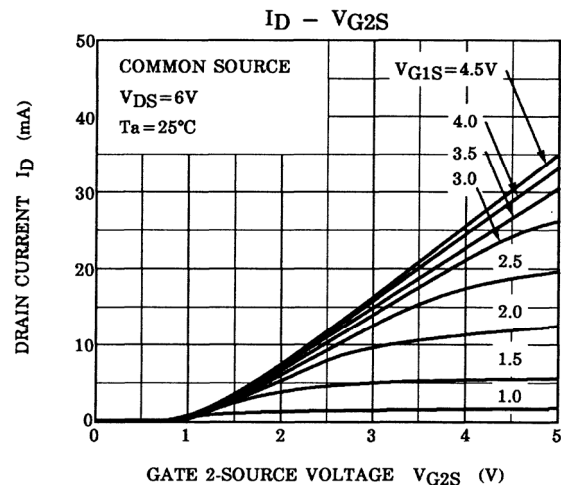
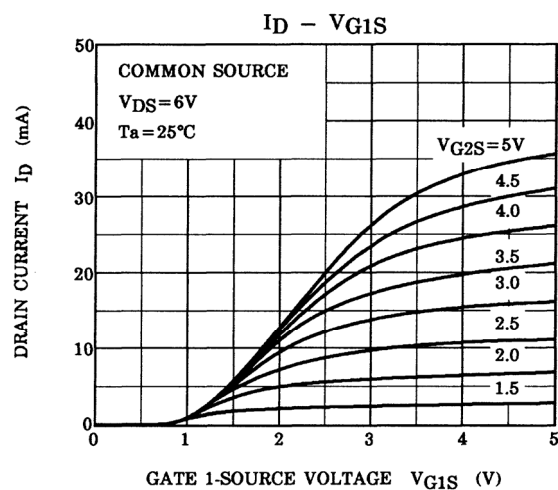
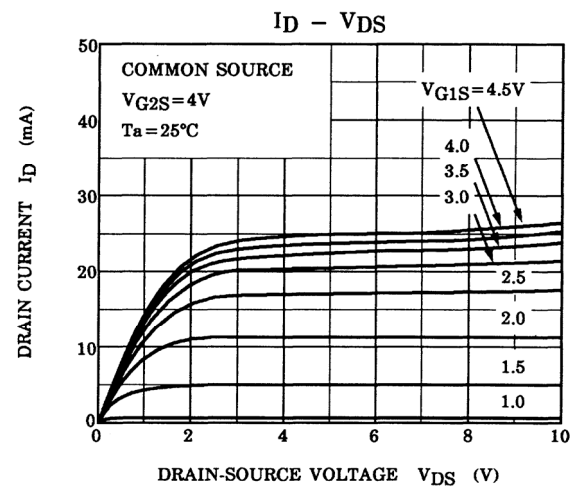
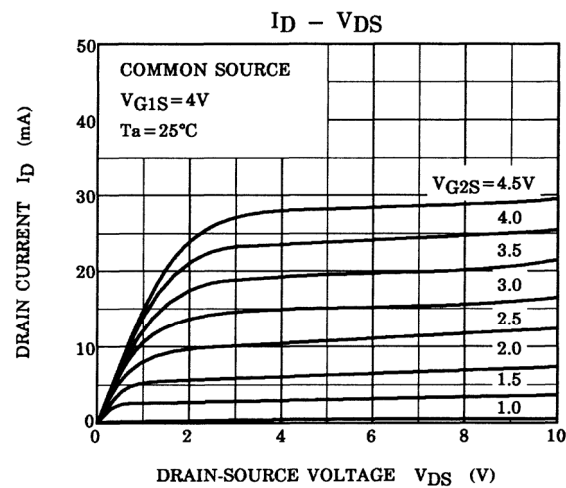
Electrical Characteristics ( $T_a = 25^\circ\text{C}$ )

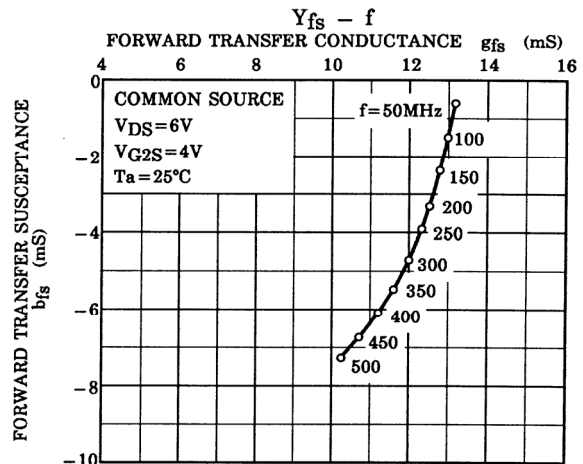
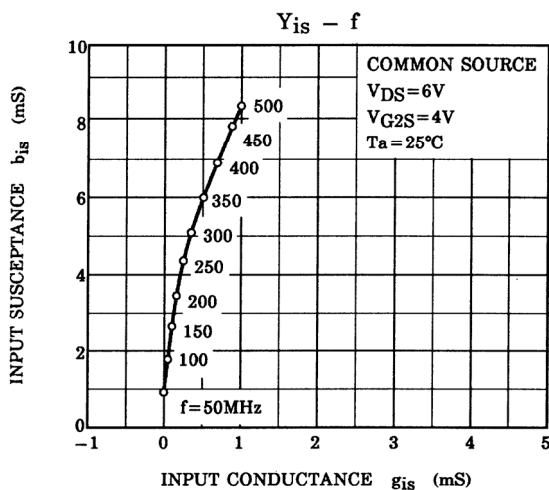
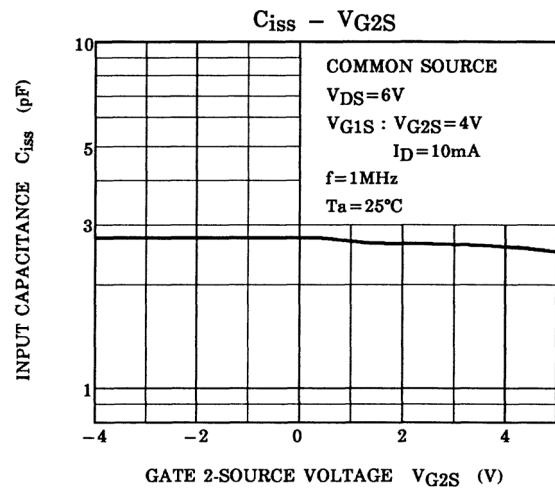
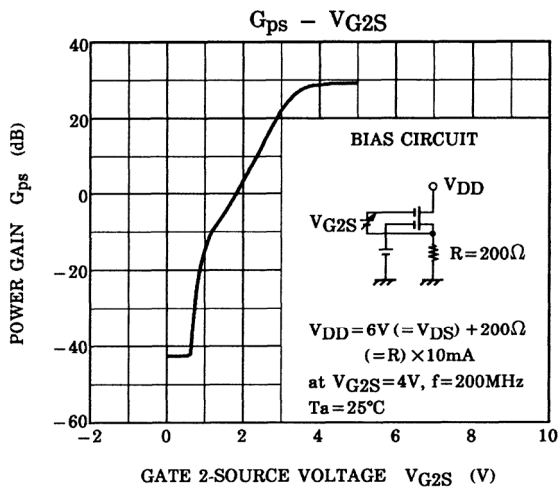
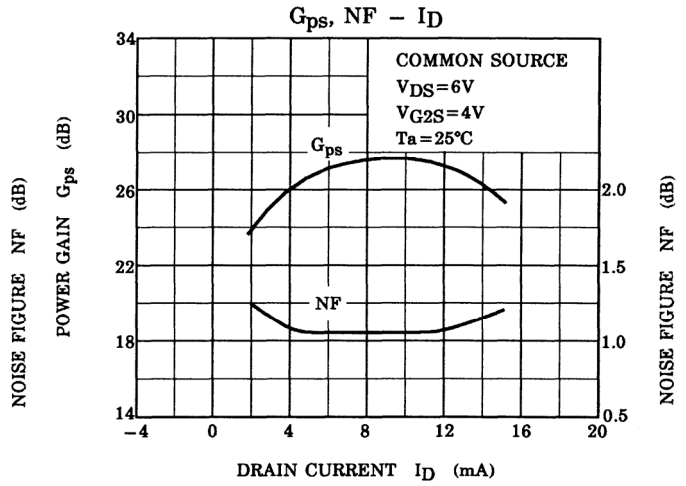
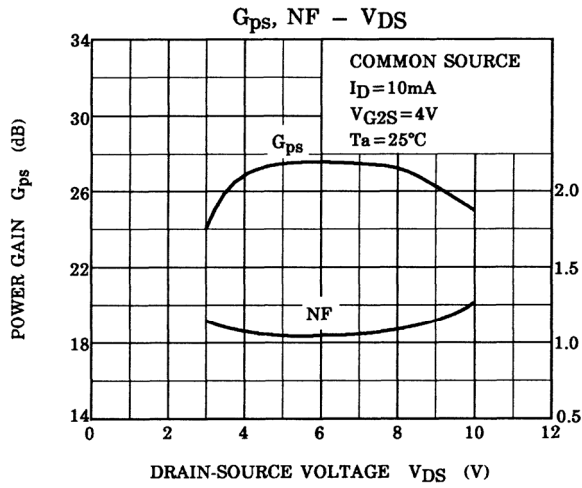
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate 1 leakage current	$I_{G1SS}$	$V_{DS} = 0, V_{G1S} = \pm 4 \text{ V}, V_{G2S} = 0$	—	—	$\pm 50$	nA
Gate 2 leakage current	$I_{G2SS}$	$V_{DS} = 0, V_{G1S} = 0, V_{G2S} = \pm 4 \text{ V}$	—	—	$\pm 50$	nA
Drain-source voltage	$V_{(BR)DSX}$	$V_{G1S} = -4 \text{ V}, V_{G2S} = -4 \text{ V}, I_D = 100 \mu\text{A}$	13.5	—	—	V
Drain current	$I_{DSS}$	$V_{DS} = 6 \text{ V}, V_{G1S} = 0, V_{G2S} = 4 \text{ V}$	0	—	0.1	mA
Gate 1-source cut-off voltage	$V_{G1S(OFF)}$	$V_{DS} = 6 \text{ V}, V_{G2S} = 4 \text{ V}, I_D = 100 \mu\text{A}$	0	—	1.0	V
Gate 2-source cut-off voltage	$V_{G2S(OFF)}$	$V_{DS} = 6 \text{ V}, V_{G1S} = 4 \text{ V}, I_D = 100 \mu\text{A}$	0	—	1.2	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 6 \text{ V}, V_{G2S} = 4 \text{ V}, I_D = 10 \text{ mA}, f = 1 \text{ kHz}$	—	13	—	mS
Input capacitance	$C_{iss}$	$V_{DS} = 6 \text{ V}, V_{G2S} = 4 \text{ V}, I_D = 10 \text{ mA}, f = 1 \text{ MHz}$	2.0	2.7	3.4	pF
Reverse transfer capacitance	$C_{rss}$		—	0.015	0.03	pF
Power gain	$G_{ps}$	$V_{DS} = 6 \text{ V}, V_{G2S} = 4 \text{ V}, I_D = 10 \text{ mA}, f = 200 \text{ MHz}$ (Figure 1)	22	27	—	dB
Noise figure	NF		—	1.1	2.2	dB

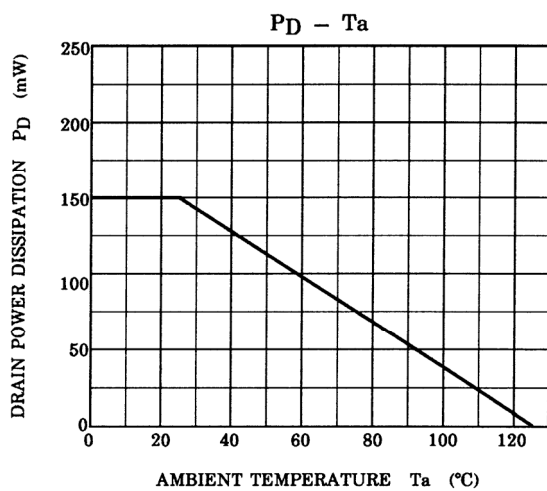
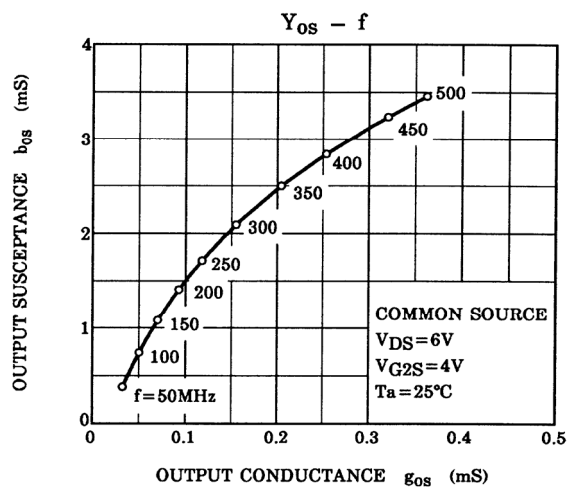
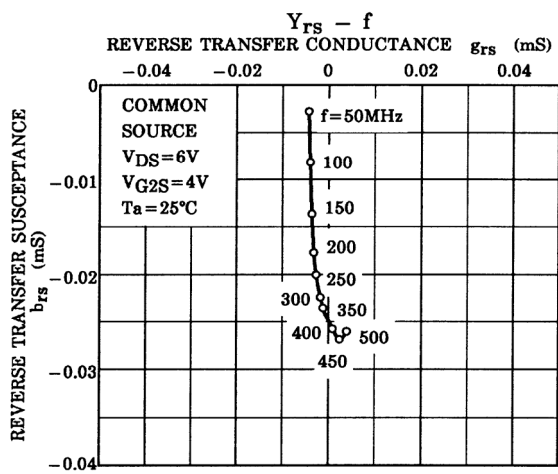


**Figure 1 200 MHz,  $G_{ps}$  NF Test Circuit**

A diagram showing a central rectangular box labeled "U J". Surrounding this box are four smaller squares, each containing a number. Square 1 is at the top right, square 2 is at the top left, square 3 is at the bottom left, and square 4 is at the bottom right.







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20070701-EN GENERAL

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