Mitsubishi Microcomputers

32170 Group, 32174 Group

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Description

The M32170 and M32174 Group are 32-bit single chip RISC microcomputers designed for use in general industrial and household equipment.

These microcomputers contains a variety of peripheral functions ranging from16-channel A-D converters to 64channel multifunction timers, 10-channel DMAs, 6-channel serial I/Os, 1-channel real time debugger, 1-channel Full-CAN, and JTAG (boundary scan facility).

With lower power consumption and low noise characteristics also considered, these microcomputers are ideal for embedded equipment applications.

Features

M32R RISC CPU core

- Uses the M32R family RISC CPU core (Instruction set common to all microcomputers in the M32R family)
- Five-stage pipelined processing
- Sixteen 32-bit general-purpose registers
- 16-bit/32-bit instructions implemented
- DSP function instructions (sum-of-products calculation using 56-bit accumulator)
- Built-in flash memory
- Built-in flash programming boot program
- Built-in RAM
- PLL clock generating circuit ..... Built-in × 4 PLL circuit
- Maximum operating frequency of the CPU clock
  40MHz(when operating at -40 to +85°C)
  32MHz(when operating at -40 to +125°C)

Table 1 32170 Group Name List by type

Type Name	RAM Size	ROM Size	Package
M32170F6VFP	40K bytes	768K bytes	240QFP
M32170F4VFP	32K bytes	512K bytes	240QFP
M32170F3VFP	32K bytes	384K bytes	240QFP
M32170F6VWG	40K bytes	768K bytes	255FBGA
M32170F4VWG	32K bytes	512K bytes	255FBGA
M32170F3VWG	32K bytes	384K bytes	255FBGA

Note: 255FBGA is currently under development.

Table 2 32170 Group Name List by type

Type Name	RAM Size	ROM Size	Package
M32174F4VFP	40K bytes	512K bytes	240QFP
M32174F3VFP	40K bytes	384K bytes	240QFP
M32174F4VWG	40K bytes	512K bytes	255FBGA
M32174F3VWG	40K bytes	384K bytes	255FBGA

Note: 255FBGA is currently under development.

64-channel multijunction timers (MJT)

Multifunction timers are incorporated that support various purposes of use.

16-bit output related timers 35ch
16-bit input/output related timers 10ch
16-bit input related timers 11ch
32-bit input related timers 8ch

- Flexible configuration is possible through interconnection of timers.
- The internal DMAC and A-D converter can be started by a timer.

Real-time Debugger

- Includes dedicated clock-synchronized serial I/O that can read and write the contents of the internal RAM independently of the CPU.
- Can look up and update the data table in real time while the program is running.
- Can generate a dedicated interrupt based on RTD communication.

Abundant internal peripheral functions

In addition to the timers and real-time debugger, the microcomputer contains the following peripheral functions.

- DMAC ..... 10 channels
- Two independent A-D converter ..... (10-bit converter × 16 channels) × 2
- Serial I/O ..... 6 channels
- Interrupt controller ..... 31 interrupt sources, 8 priority levels
- Wait controller
- Full CAN ..... 1 channel
- JTAG (boundary scan function)

Designed to operate at high temperatures

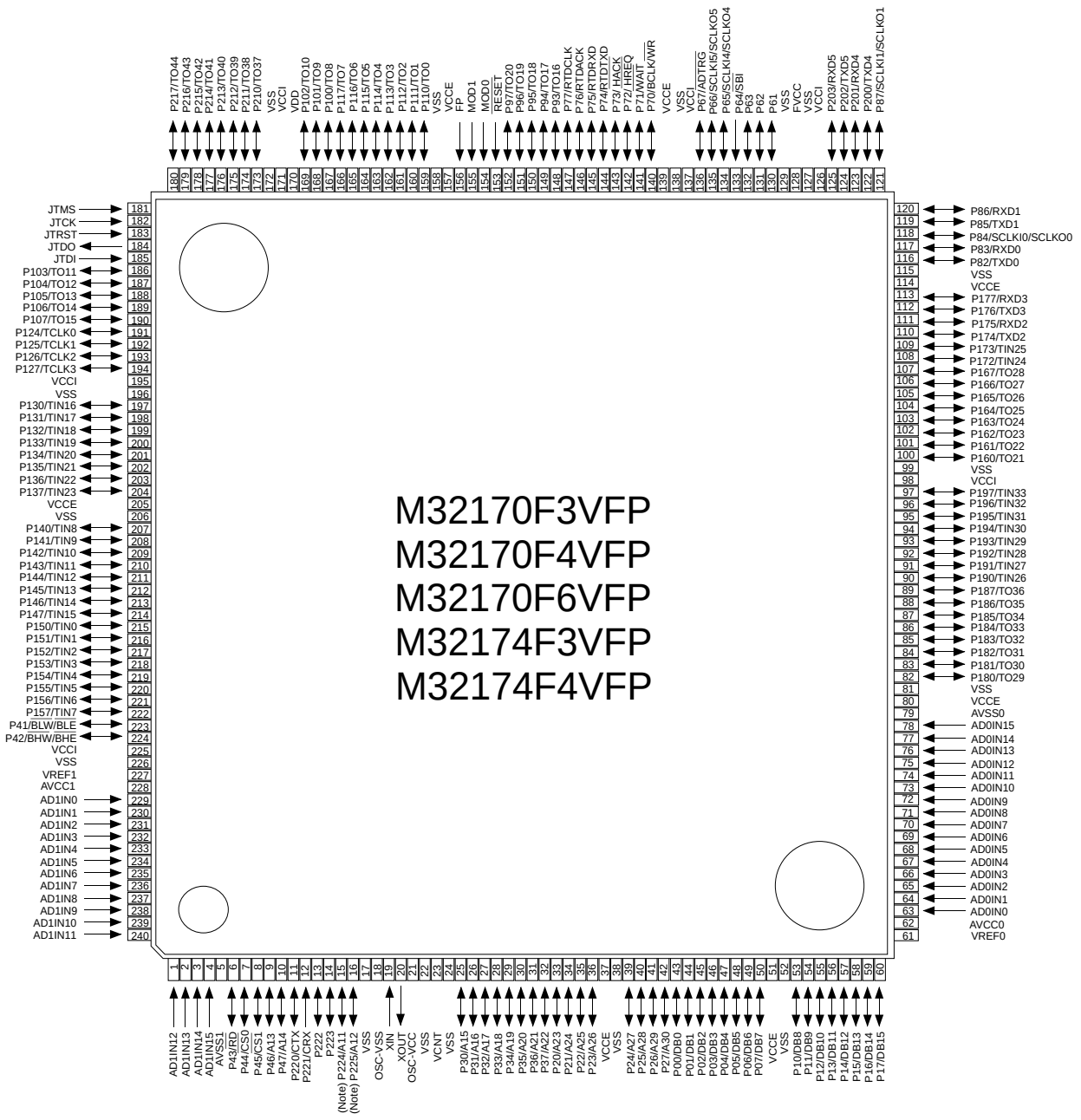
To meet the need for use at high temperatures, the microcomputer is designed to be able to operate in the temperature range of -40 to +125°C when CPU clock operating frequency = 32 MHz. When CPU clock operating frequency = 40 MHz, the microcomputer can be used in the temperature range of -40 to +85°C.

Note: This does not guarantee continuous operation at 125°C. If you are considering use of the microcomputer at 125°C, please consult Mitsubishi.

Applications

Automobile equipment control (e.g., Engine, ABS, AT), industrial equipment system control, and high-function OA equipment (e.g., PPC)

Pin Assignment(top view)



Package 240P6Y-A

Note: Use caution when using these pins because they nave a debug event function.

Figure 1 Pin Layout Diagram of the 240QFP

Pin Assignment(top view)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	JTMS	P216 /TO43	P214 /TO41	P210 /TO37	P102 /TO10	P116 /TO6	TRDATA 6	P112 /TO2	VCCE	$\overline{\text{RESET}}$	P96 /TO19	P77/ RTDCLK	P73 /$\overline{\text{HACK}}$	VCCE	P66 /SCLK5	P62	VSS	P202 /TXD5	P201 /RXD4	TRDATA 3
19	JTCK	P217 /TO44	P215 /TO42	P211 /TO38	VDD	P117 /TO7	TRDATA 7	P113 /TO3	VSS	MOD0	P95 /TO18	P76/ RTDACK	P72 /$\overline{\text{HREQ}}$	VSS	P65 /SCLK4	P61	VCCI	P200 /TXD4	N.C	TRDATA 1
18	JEVENT 0	JDBI	P213 /TO40	P212 /TO39	VCCI	P100 /TO8	P114 /TO4	TRDATA 4	P110 /TO0	MOD1	P94 /TO17	P75/ RTDRXD	P71 /$\overline{\text{WAIT}}$	VCCI	P64 /$\overline{\text{SBI}}$	VSS	P203 /RXD5	P87 /SCLK1	TRDATA 2	TRDATA 0
17	JEVENT 1	JTRST	JTDO	VSS	P101 /TO9	P115 /TO5	TRDATA 5	P111 /TO1	FP	P97 /TO20	P93 /TO16	P74/ RTDTXD	P70 /BCLK	P67 /$\overline{\text{ADTRG}}$	P63	FVCC	P83 /RXD0	P84 /SCLK0	P86 /RXD1	P85 /TXD1
16	P104 /TO12	P103 /TO11	P105 /TO13	JTDI													P177 /RXD3	VCCE	P82 /TXD0	VSS
15	P124 /TCLK0	P107 /TO15	P125 /TCLK1	P106 /TO14													P173 /TIN25	P174 /TXD2	P176 /TXD3	P175 /RXD2
14	VCCI	P127 /TCLK3	VSS	P126 /TCLK2													P165 /TO26	P166 /TO27	P172 /TIN24	P167 /TO28
13	P132 /TIN18	P131 /TIN17	P133 /TIN19	P130 /TIN16													P161 /TO22	P162 /TO23	P164 /TO25	P163 /TO24
12	P136 /TIN22	P135 /TIN21	P137 /TIN23	P134 /TIN20													P197 /TIN33	VCCI	P160 /TO21	VSS
11	P140 /TIN8	VSS	P141 /TIN9	VCCE													P193 /TIN29	P194 /TIN30	P196 /TIN32	P195 /TIN31
10	P144 /TIN12	P145 /TIN13	P143 /TIN11	P142 /TIN10													P187 /TO36	P192 /TIN28	P190 /TIN26	P191 /TIN27
9	P150 /TIN0	P151 /TIN1	P147 /TIN15	P146 /TIN14													P183 /TO32	P186 /TO35	P184 /TO33	P185 /TO34
8	P154 /TIN4	P155 /TIN5	P153 /TIN3	P152 /TIN2													VSS	P182 /TO31	P180 /TO29	P181 /TO30
7	P41 /$\overline{\text{BLW}}$	P42 /$\overline{\text{BHW}}$	P157 /TIN7	P156 /TIN6													AD0IN14	VCCE	AD0IN15	AVSS0
6	VREF1	AVCC1	VSS	VCCI													AD0IN10	AD0IN13	AD0IN11	AD0IN12
5	AD1IN2	AD1IN3	AD1IN1	AD1IN0													AD0IN6	AD0IN9	AD0IN7	AD0IN8
4	AD1IN6	AD1IN7	AD1IN5	AD1IN15	P45 /$\overline{\text{CS1}}$	P221 /CRX	P225 /A12	XOUT	VSS	P33 /A18	TRSYNC	P21 /A24	VSS	P27 /A30	P03 /DB3	P07 /DB7	P11 /DB9	AD0IN5	AD0IN3	AD0IN4
3	AD1IN8	AD1IN10	AD1IN4	AVSS1	P46 /A13	P222	VSS	OSC-VCC	P30 /A15	P34 /A19	P20 /A23	VCCE	P26 /A29	P02 /DB2	P06 /DB6	P10 /DB8	P14 /DB12	AD0IN1	AD0IN0	AD0IN2
2	AD1IN9	AD1IN11	AD1IN13	P43 /$\overline{\text{RD}}$	P47 /A14	P223	OSC-VSS	VSS	P31 /A16	P35 /A20	P37 /A22	P23 /A26	P25 /A28	P01 /DB1	P05 /DB5	VSS	P13 /DB11	P17 /DB15	VREF0	AVCC0
1		AD1IN12	AD1IN14	P44 /$\overline{\text{CS0}}$	P220 /CTX	P224 /A11	XIN	VCNT	P32 /A17	TRCLK	P36 /A21	P22 /A25	P24 /A27	P00 /DB0	P04 /DB4	VCCE	P12 /DB10	P15 /DB13	P16 /DB14	N.C

M32170F3VWG
M32170F4VWG
M32170F6VWG
M32174F3VWG
M32174F4VWG

Package 255FBGA

Note 1: NC pin (W19, Y1) shows non-connect. Be open state.
Note 2: Use caution when using P224/A11 and P225/A12 because they have a debug event function.
Note 3: 255FBGA is currently under development.

Figure 2 Pin Layout Diagram of the 255FBGA

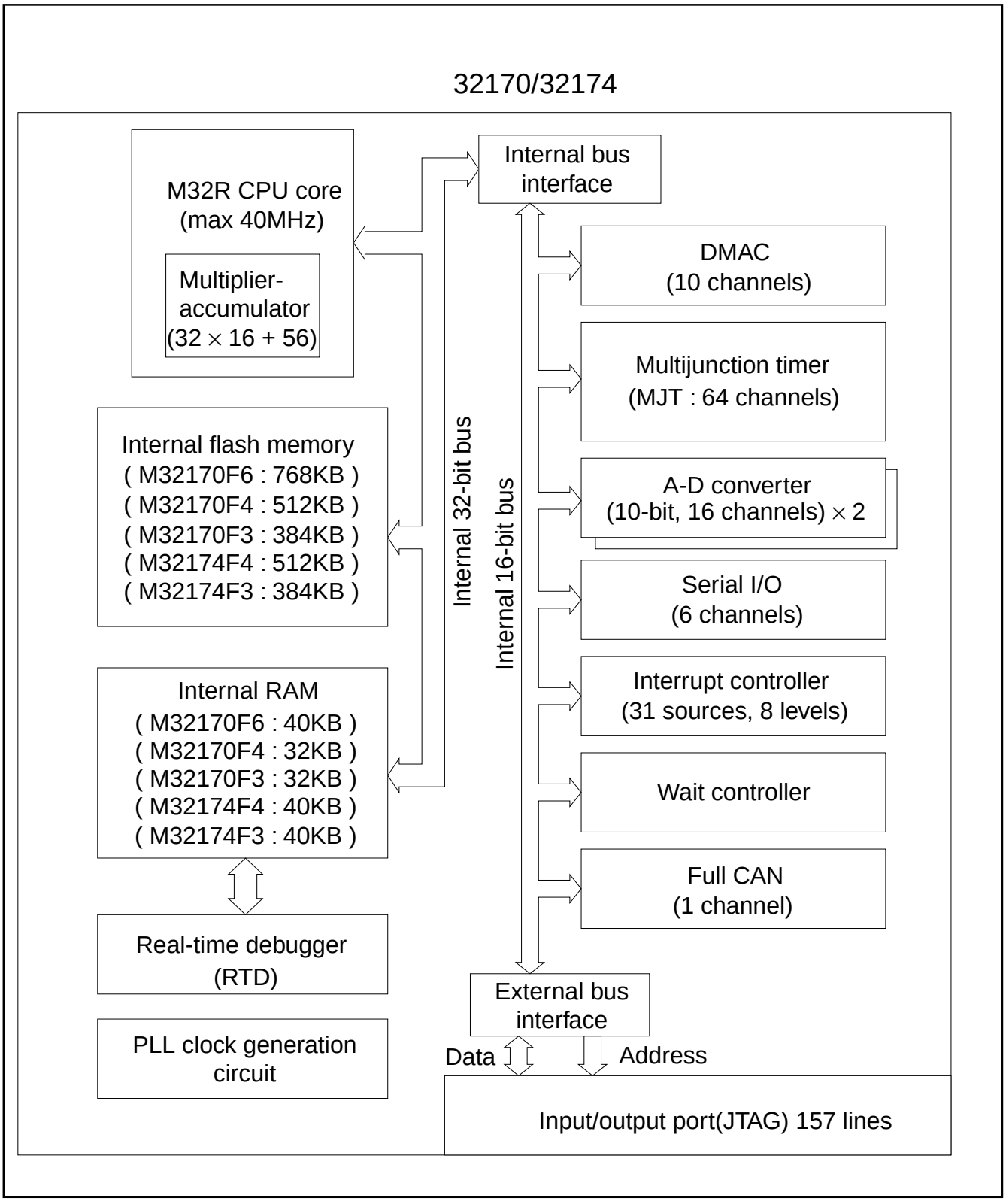


Figure 3 Block diagram

Table 3 Outline Performance (1/2)

Functional Block	Features
M32R CPU core	M32R family CPU core, internally configured in 32 bits Built-in multiplier-accumulator (32 × 16 + 56) Basic bus cycle : 25 ns (Internal CPU clock frequency at 40 MHz, Internal peripheral clock frequency at 20 MHz) Logical address space : 4G bytes, linear General-purpose register : 32-bit register × 16, Control register: 32-bit register × 5 accumulator : 56 bits
External data bus	16 bits data bus
Instruction set	16-bit/32-bit instruction formats 83 instructions/ 9 addressing modes
Internal flash memory	M32170F6 : 768K bytes M32170F4, M32174F4 : 512K bytes M32170F3, M32174F3 : 384K bytes Rewrite durability : 100 times
Internal RAM	M32170F6, M32174F4, M32174F3 : 40K bytes M32170F4, M32170F3 : 32K bytes
DMAC	10 channels (DMA transfers between internal peripheral I/Os, between internal peripheral I/O and internal RAM, and between internal RAMs) Channels can be cascaded and can operate in combination with internal peripheral I/O
Multijunction timer	64 channels of multijunction timers. • 16-bit output-related timers × 35 channels (single-shot, delayed single-shot, PWM, single-shot PWM) • 16-bit input/output-related timers × 10 channels (event count mode, single-shot, PWM, measurement) • 16-bit input-related timers × 11 channels (measurement, event count mode, multiply-by-4 count 3 channels) • 32-bit input-related timers × 8 channels (measurement) Flexible timer configuration is possible through interconnection of channels using the event bus.
A-D converter	2 independent 10-bit multifunction A-D converters • Input 16 channels × 2 • Scan-based conversion can be switched with 4, 8, and 16 • Capable of interrupt conversion during scan • 8-bit/10-bit readout function available
Serial I/O	6 channels (The serial I/Os can be set for synchronous serial I/O or UART. SIO2,3 are UART mode only)
Real-time debugger (RTD)	1-channels dedicated clock-synchronized serial The entire internal RAM can be read or rewritten from the outside without CPU intervention.
Interrupt controller	Controls interrupts from internal peripheral I/Os (Priority can be set to one of 8 levels including interrupt disabled)
Wait controller	Controls wait when accessing external extended area (1 to 4 wait cycles inserted + prolonged by external WAIT signal input)
CAN	16-channels message slots
JTAG	Boundary-Scan function

Table 4 Outline Performance (2/2)

Function Block	Features
Clock	Maximum internal CPU memory clock : 40MHz (access to CPU, internal ROM, and internal RAM) Maximum internal peripheral clock : 20MHz (access to internal peripheral module) Maximum external input clock : 10.0MHz, Built-in multiply-by-4 PLL circuit
Power Supply Voltage	External I/O : 5V (±0.5V) or 3.3V (±0.3V) Internal logic : 3.3V (±0.3V)
Operating temperature rang	-40 to +125°C(Internal CPU memory clock 32MHz, internal peripheral clock 16MHz) -40 to +85°C(Internal CPU memory clock 40MHz, internal peripheral clock 20MHz)
Package	0.5mm pitches / 240-pin plastic QFP, 0.8mm pitches / 255-pin FBGA (Note)

Note: 255-pin FBGA is currently under development.

Outline of the CPU core

The M32170 and M32174 Group uses the M32R RISC CPU core, and has an instruction set which is common to all microcomputers in the M32R family.

Instructions are processed in five pipelined stages consisting of instruction fetch, decode, execution, memory access, and write back. Thanks to its “out-of-order-completion” mechanism, the M32R CPU allows for clock cycle efficient, instruction execution control.

The M32R CPU internally has sixteen 32-bit general-purpose registers. The instruction set consists of 83 discrete instructions, which come in either a 16-bit instruction or a 32-bit instruction format. Use of the 16-bit instruction format helps to reduce the code size of a program. Also, the availability of 32-bit instructions facilitates programming and increases the performance at the same clock speed, as compared to architectures with segmented address spaces.

Sum-of-products instructions comparable to DSP

The M32R CPU contains a multiplier/accumulator that can execute 32 bits × 16 bits in one cycle. Therefore, it executes a 32 bit × 32 bit integer multiplication instruction in three cycles. Also, the M32R CPU supports the following four sum-of-products instructions (or multiplication instructions) for DSP function use.

(1) 16 high-order register bits × 16 high-order register bits
(2) 16 low-order register bits × 16 low-order register bits
(3) All 32 register bits × 16 high-order register bits
(4) All 32 register bits × 16 low-order register bits

Furthermore, the M32R CPU has instructions for rounding the value stored in the accumulator to 16 or 32 bits, and instructions for shifting the accumulator value to adjust digits before storing in a register. Because these instructions also can be executed in one cycle, DSP comparable data processing capability can be obtained by using them in combination with high-speed data transfer instructions such as Load & Address Update or Store & Address Update.

Built-in clock multiplier circuit

The clock multiplier circuit multiplies the frequency of the input clock signal by 4 to produce the internal operating clock. When the maximum CPU memory clock frequency = 40 MHz, the input clock frequency is 10.0 MHz.

Three operation modes

The M32170 and M32174 Group has three operation modes: single-chip mode, external extended mode, and processor mode. These operation modes are changed from one to another by setting the MOD0 and MOD1 pins.

Address space

The M32170 and M32174 Group’s logical addresses are always handled in 32 bits, providing 4 Gbytes of linear address space. The M32170 and M32174 Group’s address space consists of the following.

User space

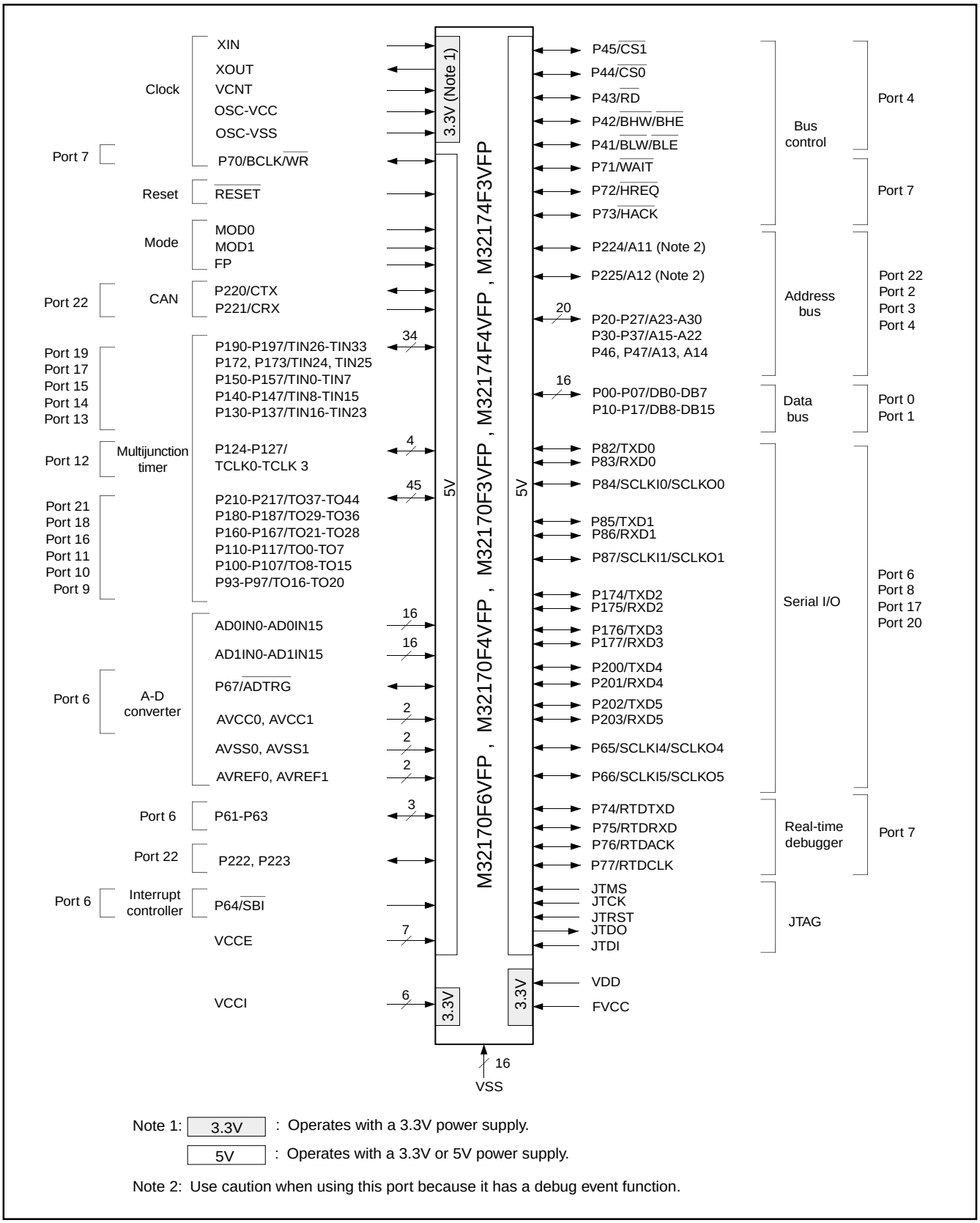
A 2-Gbyte area from H’0000 0000 to H’7FFF FFFF is the user space. Located in this space are the user ROM area, external extended area, internal RAM area, and SFR (Special Function Register) area (internal peripheral I/O registers). Of these, the user ROM area and external extended area are located differently depending on mode settings.

Boot program space

A 1-Gbyte area from H’8000 0000 to H’BFFF FFFF is the boot program area. This space contains the on-board programming program (boot program) used in blank state by the internal flash memory.

System space

A 1-Gbyte area from H’C000 0000 to H’FFFF FFFF is the system area. This space is reserved for use by development tools such as an in-circuit emulator and debug monitor, and cannot be used by the user.

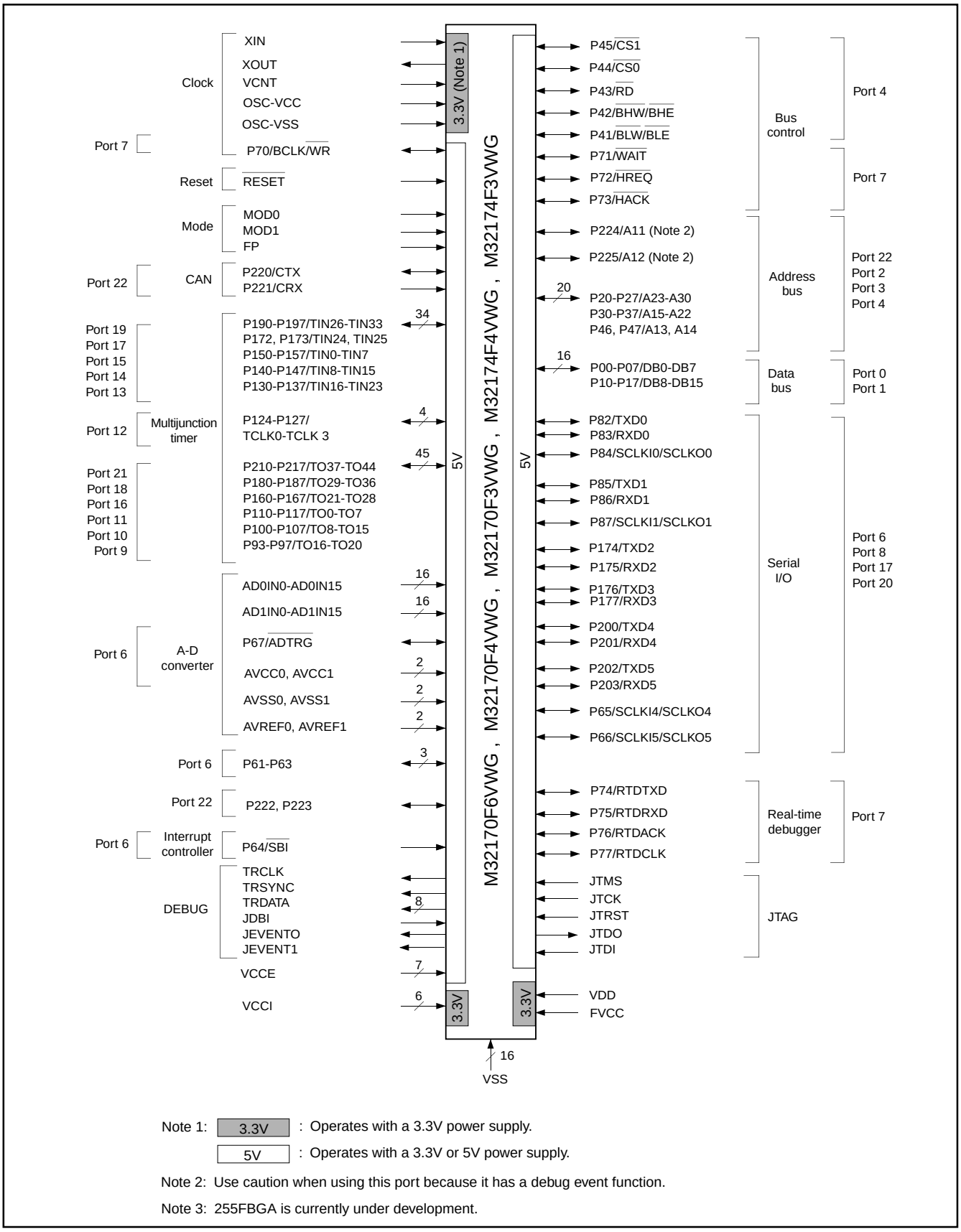


Note 1: 3.3V : Operates with a 3.3V power supply.

5V : Operates with a 3.3V or 5V power supply.

Note 2: Use caution when using this port because it has a debug event function.

Figure 4 Pin Function Diagram of 240QFP



Note 1: 3.3V : Operates with a 3.3V power supply.

5V : Operates with a 3.3V or 5V power supply.

Note 2: Use caution when using this port because it has a debug event function.

Note 3: 255FBGA is currently under development.

Figure 5 Pin Function Diagram of 255FBGA

Table 5 Description of Pin Function (1/5)

Type	Pin Name	Description	Input/Output	Function
Power	VCCE	Power supply	—	Supplies power (5 V or 3.3V) to external I/O ports.
supply	VCCI	Power supply	—	Supplies power (3.3 V) to the internal logic.
	VDD	RAM power supply	—	nternal RAM backup power supply (3.3 V).
	FVCC	Flash power supply	—	Internal flash memory backup power supply (3.3 V).
	VSS	Ground	—	Connect all VSS pins to ground (GND).
Clock	XIN, XOUT	Clock	Input Output	Clock input/output pins. These pins contain a PLL-based frequency multiply-by-4, so input the clock whose frequency is quarter the operating frequency. (XIN input = 10 MHz when CPU clock operates at 40 MHz)
	BCLK / $\overline{WR}$	System clock	Output	When this signal is System Clock(BCLK), it outputs a clock whose is twice that of external inpout clock. (BCLK output = 20 MHz when CPU clock operates at 40 MHz). Use this clock when circuits are synchronized externally. When this signal is Write($\overline{WR}$),during external write access it indicates the valid data on the data bus to transfer.
	OSC-VCC	Power supply	—	Power supply to the PLL circuit. Connect OSC-VCC to the power supply(3.3V)
	OSC-VSS	Ground	—	Connect OSC-VSS to ground.
	VCNT	PLL control	Input	This pin controls the PLL circuit. Connect a resistor and capacitor to this pin.
Reset	$\overline{RESET}$	Reset	Input	This pin resets the internal circuits.
Mode	MOD0 MOD1	Mode	Input	These pins set an operation mode. MOD0 | MOD1 | Mode 0 | 0 | Single-chip mode 0 | 1 | Expanded external mode 1 | 0 | Processor mode (Boot mode) (Note) 1 | 1 | (Reserved)
Address bus	A11-A30	Address bus	Output	20 lines of address bus (A11-A30) are provided to accommodate two channels of 2 MB memory space (max.) connected external to the chip. A31 is not output. In the write cycle, of the 16-bit data bus the valid byte positions to write are output as $\overline{BHW}$/ $\overline{BHE}$ and $\overline{BLW}$/ $\overline{BLE}$. In read cycle, data on the entire 16-bit data bus is read. However, only the data at the valid byte positions are transferred to the M32R's internal circuit.
Data bus	DB0-DB15	Data bus	Input/output	This 16-bit data bus connects to external device.

Note: FP pin should be "H" level in Boot Mode.

Table 6 Description of Pin Function (2/5)

Type	Pin type	Description	Input/Output	Function
Bus control	$\overline{CS0}$, CS1	Chip select	Output	Chip select signals for external devices.
	$\overline{RD}$	Read	Output	This signal is output when reading external devices.
	$\overline{BHW}$/ $\overline{BHE}$	Byte high write	Output	Indicates the byte positions to which valid are transferred when writing to external devices.$\overline{BHW}$/ $\overline{BHE}$ and $\overline{BLW}$/ $\overline{BLE}$ correspond to the upper address side(D0-D7 effective) and the lower address side(D8-D15 effective),respectivel.
	$\overline{BLW}$/ $\overline{BLE}$	Byte low write	Output	
	$\overline{WAIT}$	Wait	Input	If $\overline{WAIT}$ input is low when the M32R accesses external devices, the wait cycle extended.
	$\overline{HREQ}$	Hold request	Input	This pin is used by an external device to request control of the external bus. The M32R goes to a hold state when $\overline{HREQ}$ input is pulled low.
	$\overline{HACK}$	Hold acknowledge	Output	This signal indicates to the external device that the M32R has entered a hold state and relinquished control of the external bus.
Multijunction timer	TIN0 -TIN33	Timer input	Input	Input pins for multijunction timer.
	TO0 -TO44	Timer output	Output	Output pins for multijunction timer.
	TCLK0 -TCLK3	Timer clock	Input	Clock input pins for multijunction timer.
A-D converter	AVCC0, AVCC1	Analog power upply	–	AVCC0 is the power supply for the A-D0 converters. AVCC1 is the power supply for the A-D1 converters. Connect AVCC0 and AVCC1 to the power supply (5V or 3.3V).
	AVSS0, AVSS1	Analog ground	–	AVSS0 is the analog ground for the A-D0 converters. AVSS1 is the analog ground for the A-D1 converters. Connect AVCC0 and AVCC1 to ground.
	AD0IN0 -AD0IN15 AD1IN0 -AD1IN15	Analog input	Input	One block of 16-channel analog input pin for A-D0 converter. Two blocks of 16-channel analog input pin for A-D1 converter.
	VREF0, VREF1	Reference voltage input	Input	VREF0 is the reference voltage input pin (5V or 3.3V) for the A-D0 converters. VREF1 is the reference voltage input pin (5V or 3.3V) for the A-D1 converters.
	$\overline{ADTRG}$	Conversion trigger	Input	Hardware trigger input pin to start A-D conversion.
Interrupt controller	$\overline{SBI}$	System break interrupt	Input	System break interrupt(SBI) input pin of the interrupt controller.

Table 7 Description of Pin Functions (3/5)

Type	Pin name	Description	Input/output	Function
Serial I/O	SCLKI0/ SCLKO0	UART transmit/ receive clock output or CSIO transmit/receive clock input/output	Input/output	When channel 0 is in UART mode: Clock output derived from BRG output by dividing it by 2 When channel 0 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	SCLKI1/ SCLKO1	UART transmit/ receive clock output or CSIO transmit/receive clock input/output	Input/output	When channel 1 is in UART mode: Clock output derived from BRG output by dividing it by 2 When channel 1 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	SCLKI4/ SCLKO4	UART transmit/ receive clock output or CSIO transmit/receive clock input/output	Input/output	When channel 4 is in UART mode: Clock output derived from BRG output by dividing it by 2 When channel 4 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	SCLKI5 SCLKO5	UART transmit/ receive clock output or CSIO transmit/receive clock input/output	Input/output	When channel 5 is in UART mode: Clock output derived from BRG output by dividing it by 2 When channel 5 is in CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	TXD0	Transmit data	Outpt	Transmit data output pin for serial I/O channel 0
	RXD0	Receive data	Input	Receive data input pin for serial I/O channel 0
	TXD1	Transmit data	Output	Transmit data output pin for serial I/O channel 1
	RXD1	Receive data	Input	Receive data input pin for serial I/O channel 1
	TXD2	Transmit data	Output	Transmit data output pin for serial I/O channel 2
	RXD2	Receive data	Input	Receive data input pin for serial I/O channel 2
	TXD3	Transmit data	Output	Transmit data output pin for serial I/O channel 3
	RXD3	Receive data	Input	Receive data input pin for serial I/O channel 3
	TXD4	Transmit data	Output	Transmit data output pin for serial I/O channel 4
	RXD4	Receive data	Input	Receive data input pin for serial I/O channel 4
	TXD5	Transmit data	Output	Transmit data output pin for serial I/O channel 5
	RXD5	Receive data	Input	Receive data input pin for serial I/O channel 5

Table 8 Description of Pin Functions (4/5)

Type	Pin name	Description	Input/output	Function
Real-Time Debugger	RTDTXD	Transmit data	Output	Serial data output pin of the real-time debugger
	RTDRXD	Receive data	Input	Serial data input pin of the real-time debugger
	RTDCLK	Clock input	Input	Serial data transmit/receive clock input pin of the real-time debugger
	RTDACK	Acknowledge	Output	This pin outputs a low pulse synchronously with the real-time debugger's first clock of serial data output word. The low pulse width indicates the type of the command/data the realtime debugger has received.
Flash-only	FP	Flash protect	Input	This pin protects the flash memory against E/W in hardware.
CAN	CTX	Transmit data	Output	Data output pin from CAN module.
	CRX	Receive data	Input	Data input pin to CAN module.
JTAG	JTMS	Test mode	Input	Test select input for controlling the test circuit's state transition
	JTCK	Clock	Input	Clock input to the debugger module and test circuit.
	JTRST	Test reset	Input	Test reset input for initializing the test circuit asynchronously.
	JTDO	Serial output	Output	Serial output of test instruction code or test data.
	JTDI	Serial input	Input	Serial input of test instruction code or test data.
Input/ output port (Note)	P00-P07	Input/output port 0	Input/output	Programmable input/output port.
	P10-P17	Input/output port 1	Input/output	Programmable input/output port.
	P20-P27	Input/output port 2	Input/output	Programmable input/output port.
	P30-P37	Input/output port 3	Input/output	Programmable input/output port.
	P41-P47	Input/output port 4	Input/output	Programmable input/output port.
	P61-P67	Input/output port 6	Input/output	Programmable input/output port. (However, P64 is an input-only port)
	P70-P77	Input/output port 7	Input/output	Programmable input/output port.
	P82-P87	Input/output port 8	Input/output	Programmable input/output port.
	P93-P97	Input/output port 9	Input/output	Programmable input/output port.
	P100 -P107	Input/output port 10	Input/output	Programmable input/output port.

Note: Input/output port 5 is reserved for future use.

Table 9 Description of Pin Functions (5/5)

Type	Pin name	Description	Input/output	Function
Input/ output port	P110 -P117	Input/output port 11	Input/output	Programmable input/output port.
	P124 -P127	Input/output port 12	Input/output	Programmable input/output port.
	P130 -P137	Input/output port 13	Input/output	Programmable input/output port.
	P140 -P147	Input/output port 14	Input/output	Programmable input/output port.
	P150 -P157	Input/output port 15	Input/output	Programmable input/output port.
	P160 -P167	Input/output port 16	Input/output	Programmable input/output port.
	P172 -P177	Input/output port 17	Input/output	Programmable input/output port.
	P180 -P187	Input/output port 18	Input/output	Programmable input/output port.
	P190 -P197	Input/output port 19	Input/output	Programmable input/output port.
	P200 -P203	Input/output port 20	Input/output	Programmable input/output port.
	P210 -P217	Input/output port 21	Input/output	Programmable input/output port.
	P220 -P225	Input/output port 22	Input/output	Programmable input/output port. (Note) (However, P221 is an input-only port)

Note: Use caution when using P224 and P225 because they have a debug event function.

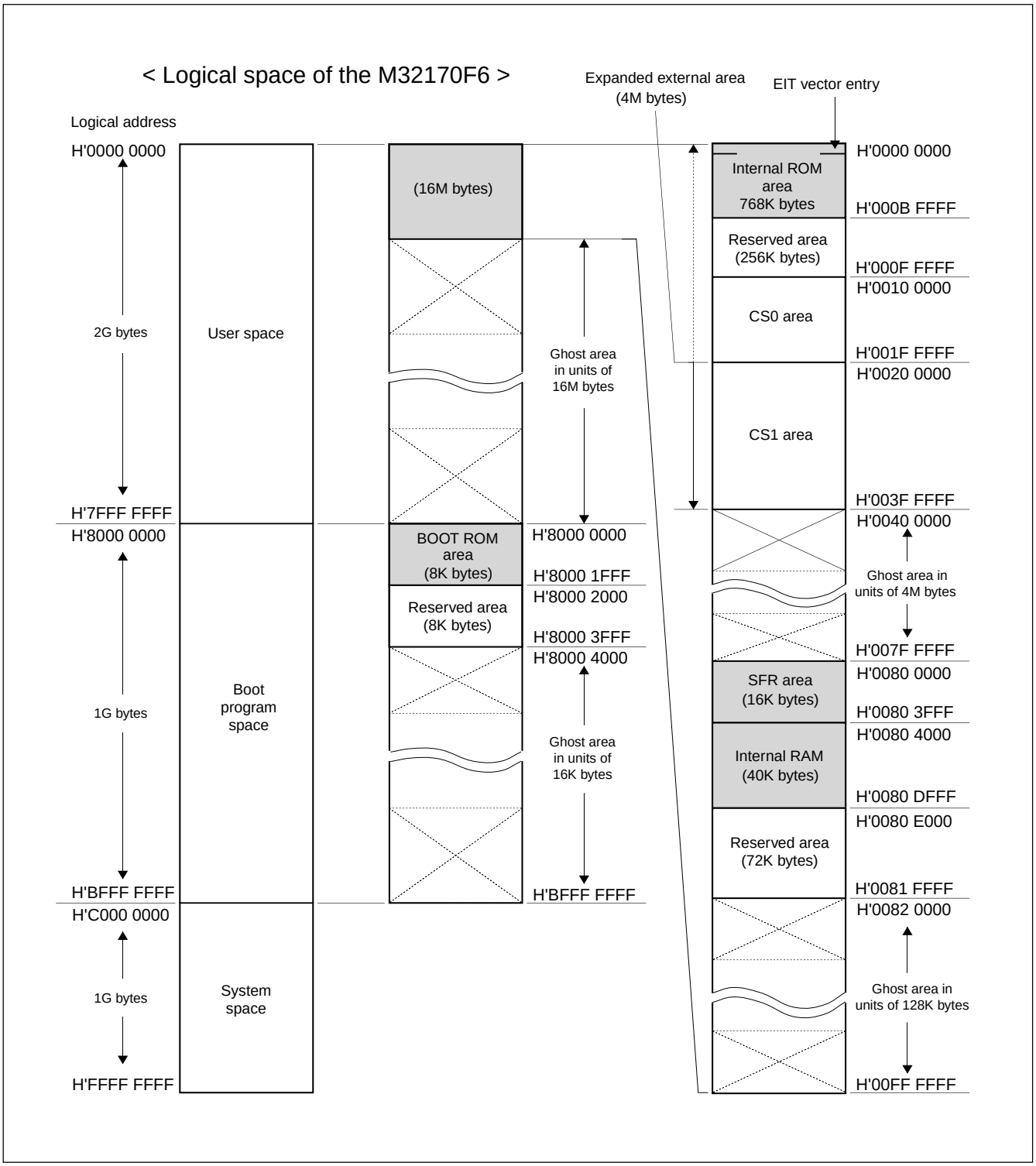


Figure 6 Address Space of the M32170F6

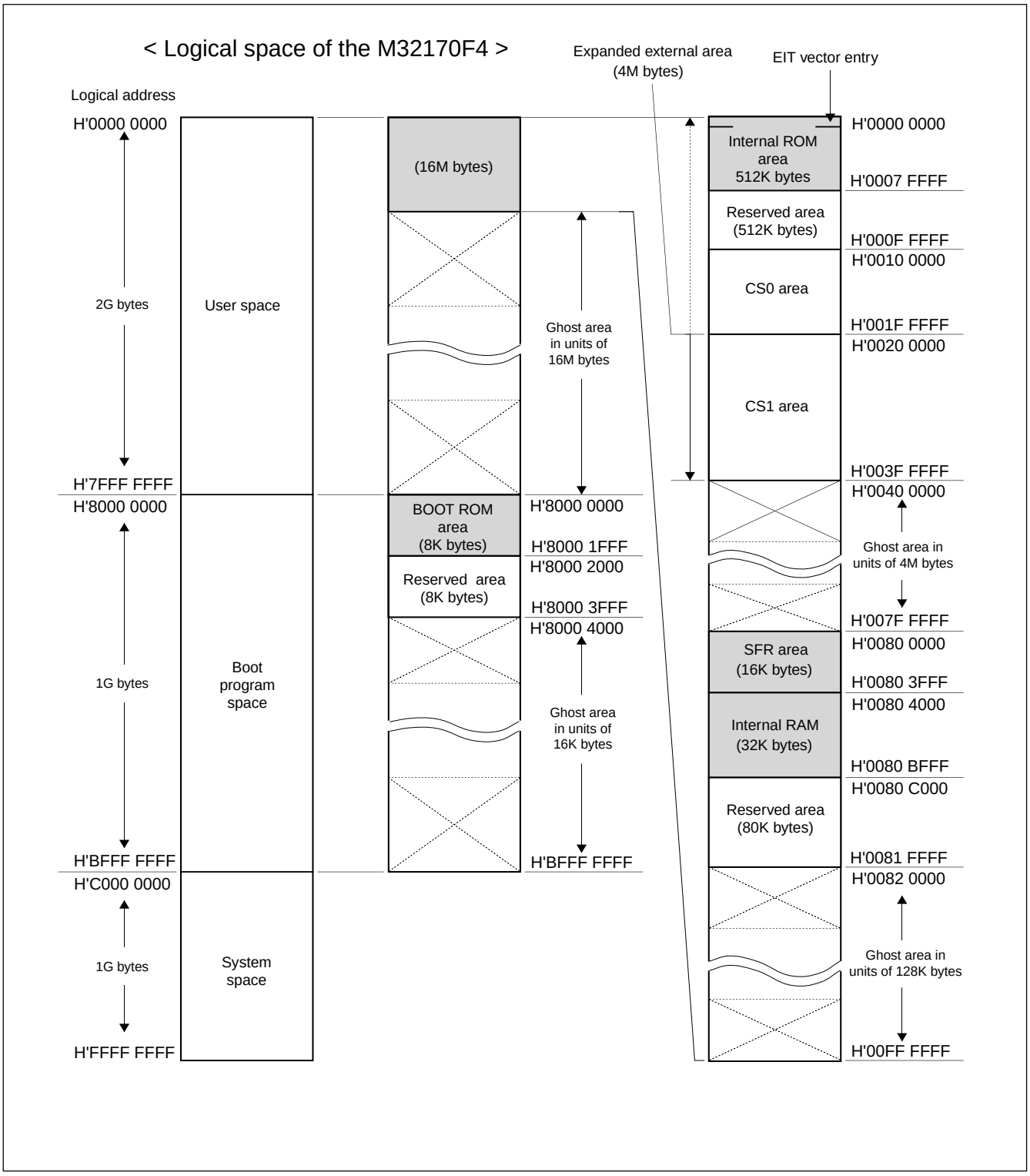


Figure 7 Address Space of the M32170F4

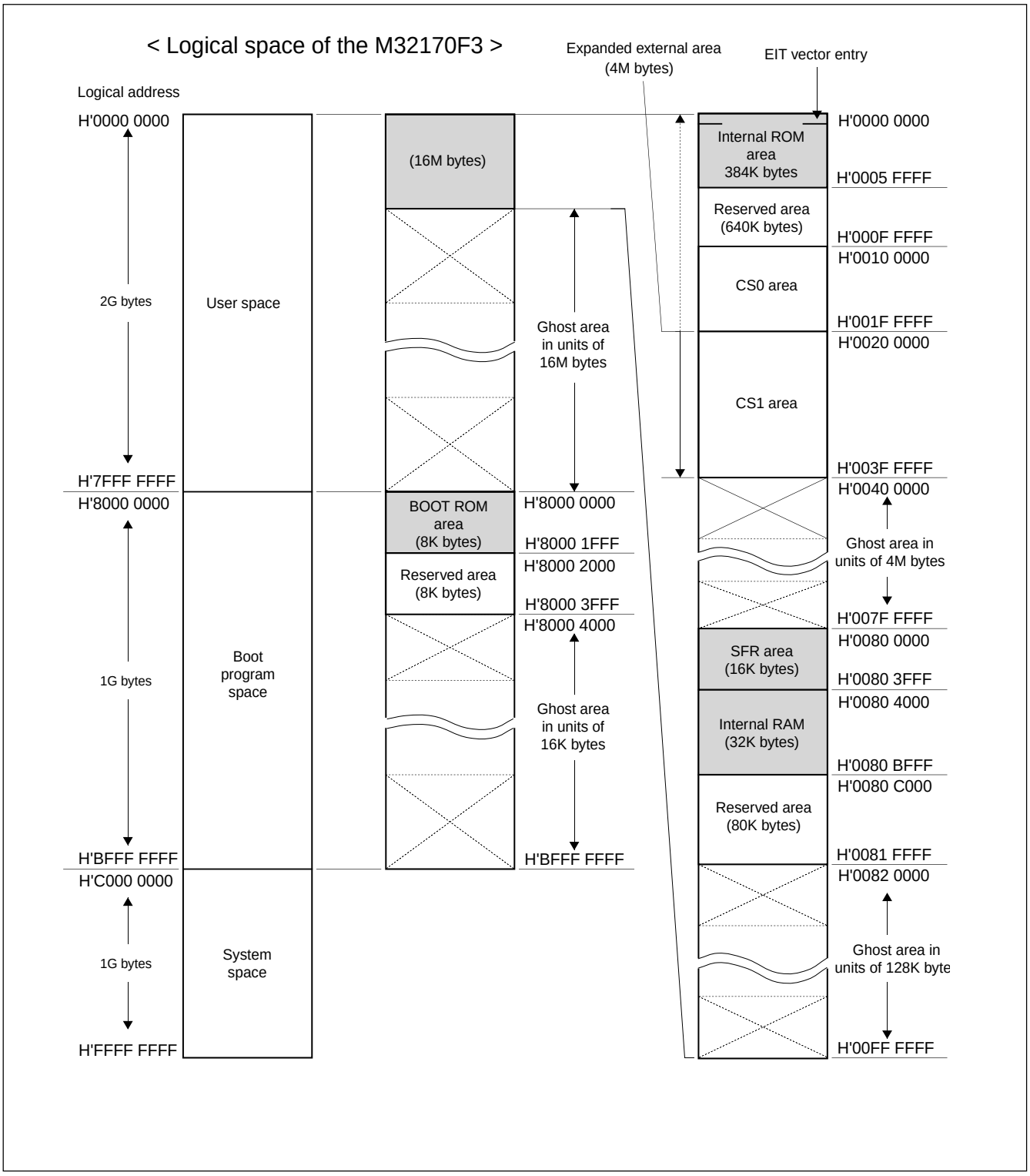


Figure 8 Address Space of the M32170F3

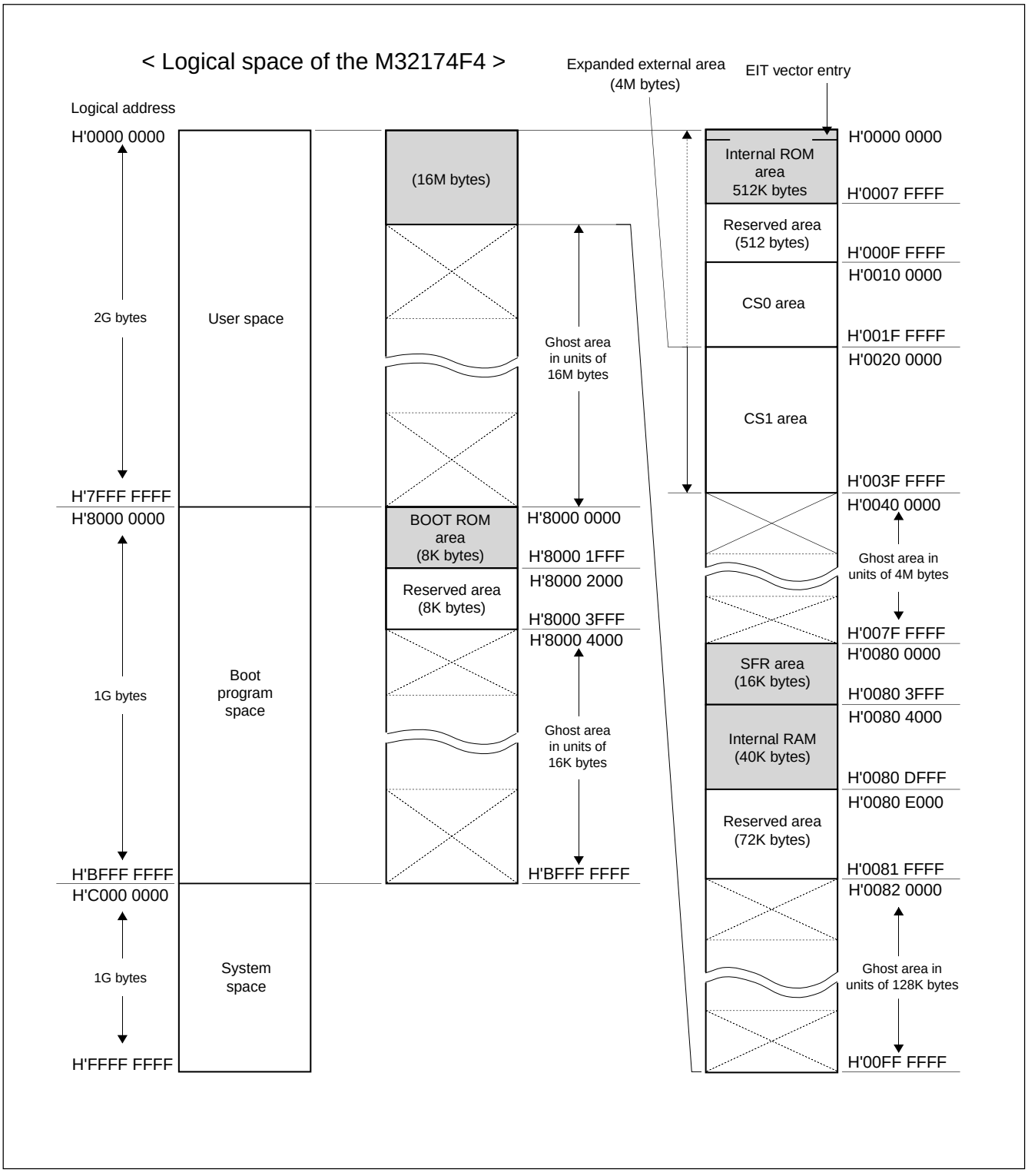


Figure 9 Address Space of the M32174F4

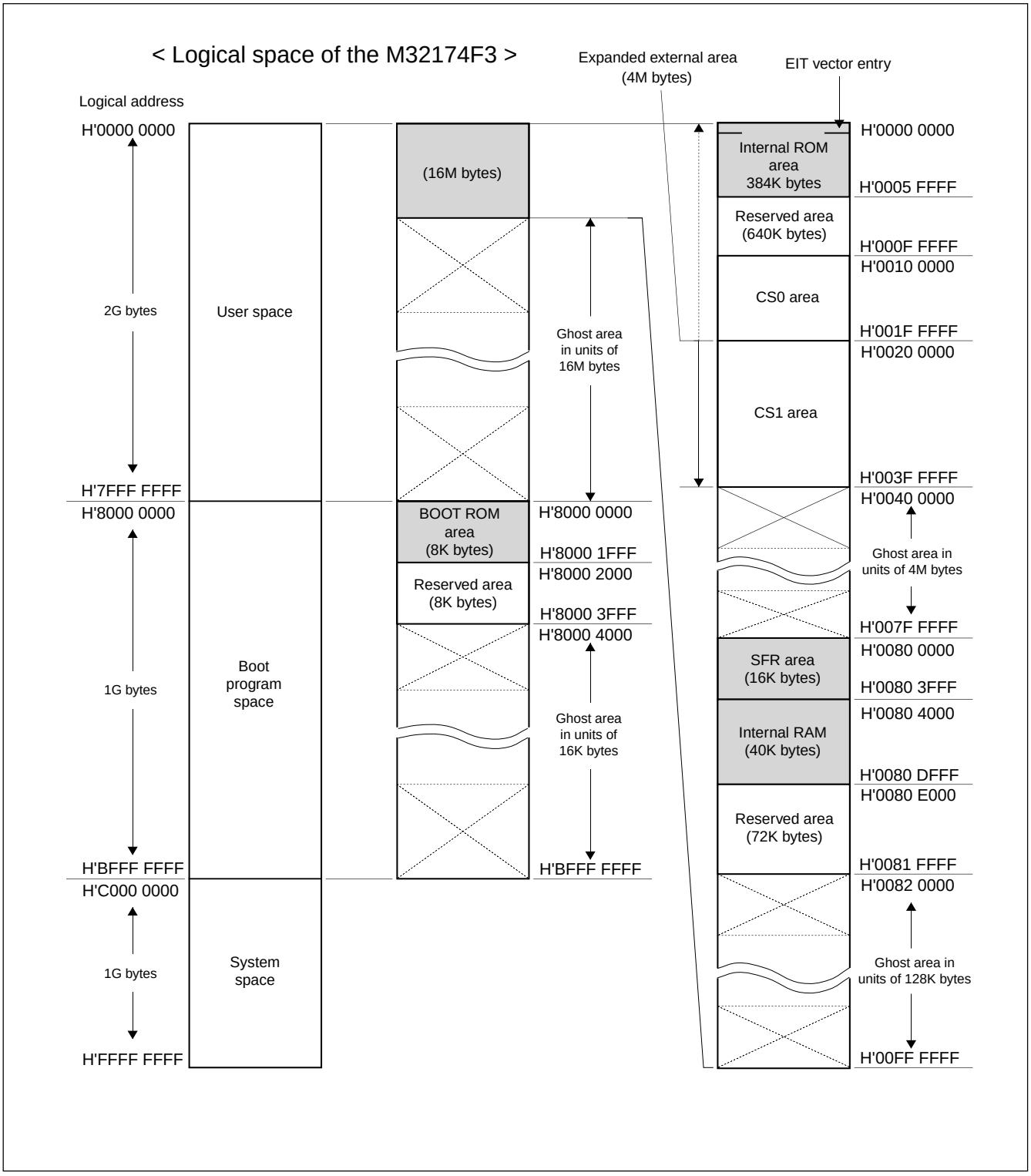
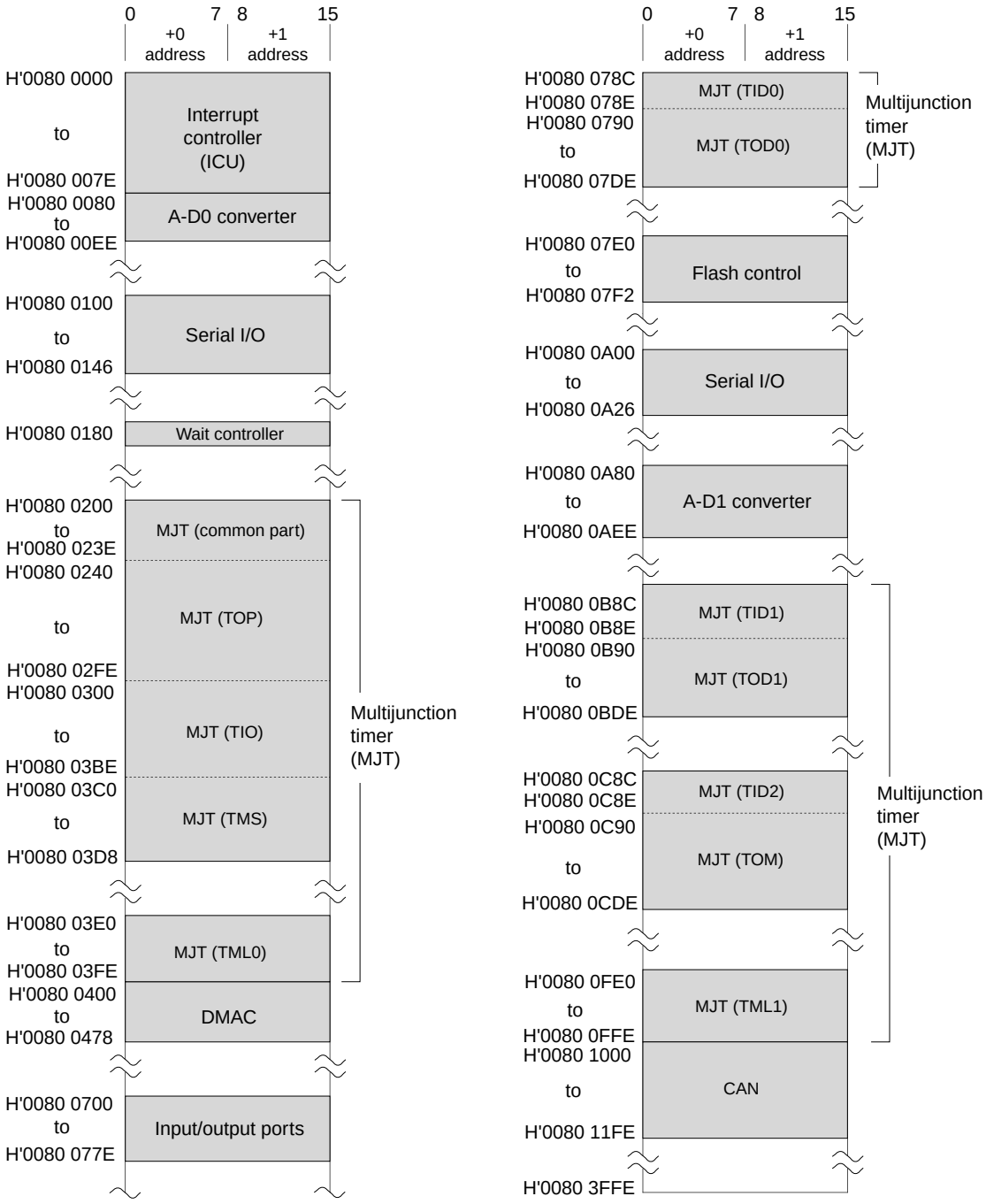


Figure 10 Address Space of the M32174F3



Note: The Real-time debugger (RTD) is an independent module operated from external circuits, and is transparent to the CPU.

Figure 11 SFR Area

Built-in Flash Memory and RAM

32170 and 32174 Group contain Flash Memory and RAM stated as follows.

The internal flash memory can be programmed on-board (i.e., while being mounted on the printed circuit board). This means that the same chip as will be used in mass-production can be used directly from the development stage on, allowing for system development without having to change the printed circuit board when proceeding from trial production to mass-production.

Table 10 Flash memory and RAM Size (32170 Group)

Type Name	ROM Size	RAM Size
M32170F6VFP	768K bytes	40K bytes
M32170F4VFP	512K bytes	32K bytes
M32170F3VFP	384K bytes	32K bytes
M32170F6VWG	768K bytes	40K bytes
M32170F4VWG	512K bytes	32K bytes
M32170F3VWG	384K bytes	32K bytes

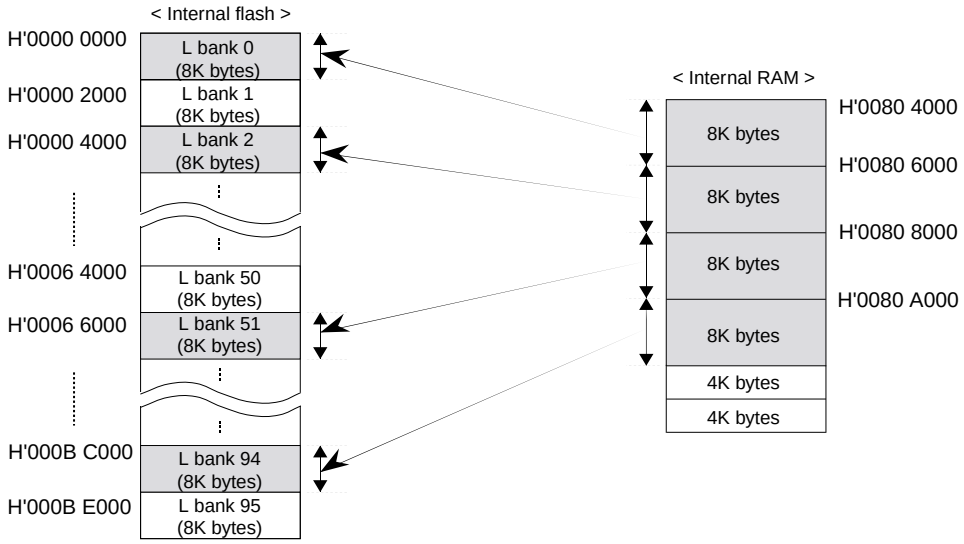
Table 11 Flash memory and RAM Size (32174 Group)

Type Name	ROM Size	RAM Size
M32174F4VFP	512K bytes	40K bytes
M32174F3VFP	384K bytes	40K bytes
M32174F4VWG	512K bytes	40K bytes
M32174F3VWG	384K bytes	40K bytes

Built-in Virtual-flash Emulation Function

Internal flash memory, which is divided from the first address in units of 8 Kbyte (L banks), can be replaced in 8 -Kbyte blocks (H70080 4000-H'0080 5FFF) of the internal RAM. And also the internal flash memory, which is divided from the first address in units of 4-Kbyte areas (S banks), can be replaced in 4 Kbytes areas.

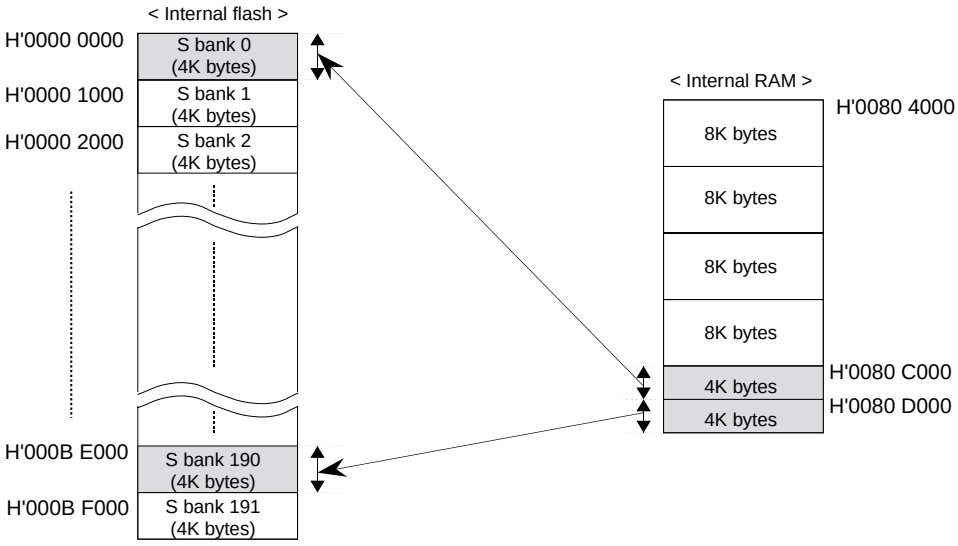
This function allows parts of the program which are frequently changed during development to be altered or evaluated without having to reset the microcomputer each time. What's more, when combined with the realtime debugger, this function helps to reduce the program evaluation period, because data in the RAM can be rewritten without requiring any CPU load.



Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FELBANK3 > FESBANK0 > FESBANK1.

Note 2: When access is made to the 8-Kbyte area (L bank) specified with virtual-flash bank registers 0-3, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

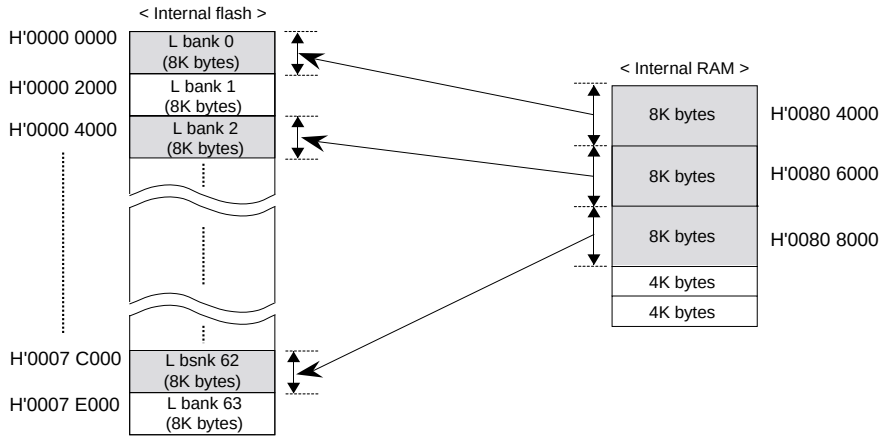
Figure 12 Virtual-Flash Emulation Areas of the M32170F6VFP (Replaced in Units of 8 Kbytes)



Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FELBANK3 > FESBANK0 > FESBANK1.

Note 2: When access is made to the 4-Kbyte area (S bank) specified with virtual-flash bank registers 0 and 1, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

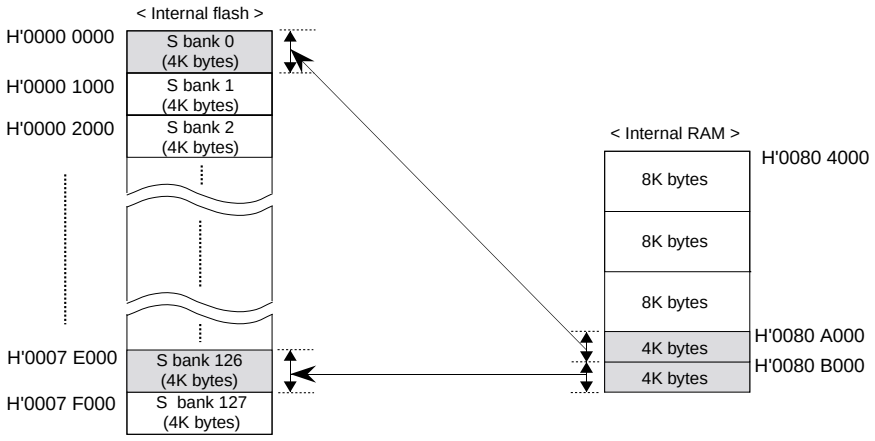
Figure 13 Virtual-Flash Emulation Areas of the M32170F6VFP (Replaced in Units of 4 Kbytes)



Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FESBANK0 > FESBANK1.

Note 2: When access is made to the 8-Kbyte area (L bank) specified with virtual-flash bank registers 0-2, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

Figure 14 Virtual-Flash Emulation Areas of the M32170F4VFP (Replaced in Units of 8 Kbytes)



Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FESBANK0 > FESBANK1.

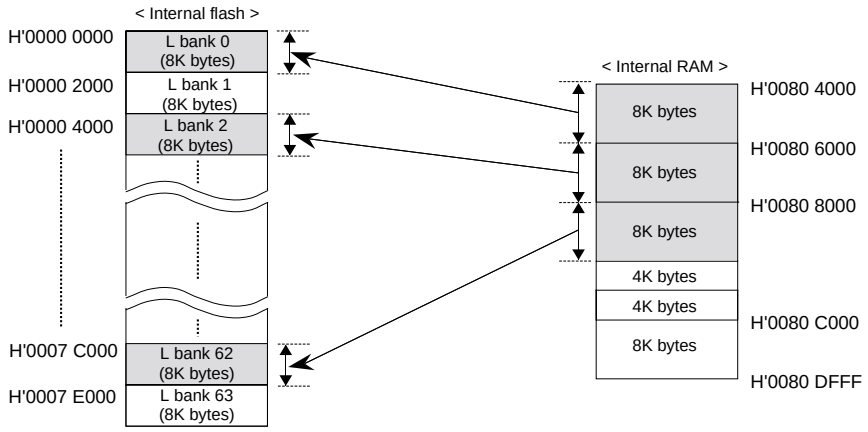
Note 2: When access is made to the 4-Kbyte area (S bank) specified with virtual-flash bank registers 0 and 1, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

Figure 15 Virtual-Flash Emulation Areas of the M32170F4VFP (Replaced in Units of 4 Kbytes)

The table below shows Virtual-Flash Emulation Areas of the M32170F4 and M32170F3.

Table 12 Virtual-Flash Emulation Areas of the M32170F4 and M32170F3

Type	Virtual-Flash Emulation Areas
M32170F4VFP,M32170F4VWG	H' 0000 0000 - H' 0007 FFFF
M32170F3VFP,M32170F3VWG	H' 0000 0000 - H' 0005 FFFF

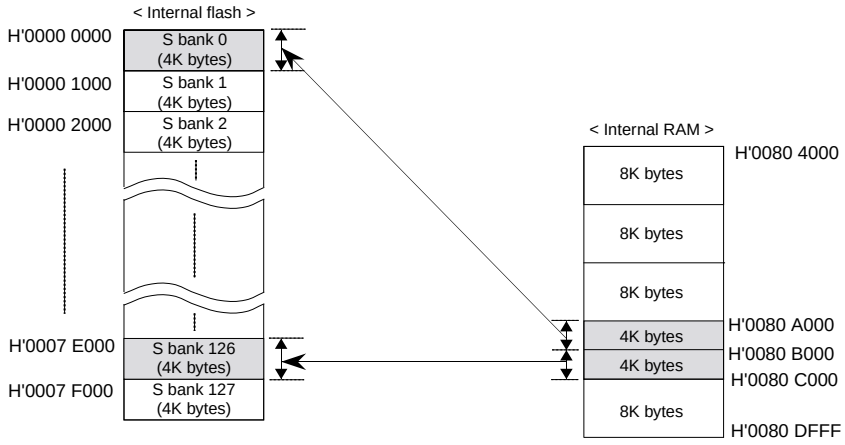


Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FESBANK0 > FESBANK1.

Note 2: When access is made to the 8-Kbyte area (L bank) specified with virtual-flash bank registers 0-2, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

Note 3: Internal RAM area (H'0080 C000-H'0080 DFFF) cannot be used as Virtual Flash Emulation area.

Figure 16 Virtual-Flash Emulation Areas of the M32174F4VFP (Replaced in Units of 8 Kbytes)



Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FESBANK0 > FESBANK1.

Note 2: When access is made to the 4-Kbyte area (S bank) specified with virtual-flash bank registers 0 and 1, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

Note 3: Internal RAM area (H'0080 C000-H'0080 DFFF) cannot be used as Virtual Flash Emulation area.

Figure 17 Virtual-Flash Emulation Areas of the M32174F4VFP (Replaced in Units of 4 Kbytes)

The table below shows Virtual-Flash Emulation Areas of the M32174F4 and M32174F3.

Table 13. Virtual-Flash Emulation Areas of the M32174F4 and M32174F3

Type Name	Virtual-Flash Emulation Areas
M32174F4VFP,M32174F4VWG	H' 0000 0000 - H' 0007 FFFF
M32174F3VFP,M32174F3VWG	H' 0000 0000 - H' 0005 FFFF

Input/output Ports

The microcomputer has a total of 157 input/output ports P0-P22. (However, P5 is reserved for future use.) The input/output ports can be used as input ports or output ports by setting up their direction registers.

Each input/output port is a dual-function pin shared with otherinternal peripheral I/O or external extended bus signal lines. These pin functions are selected by using the chip operation mode select or the input/output port operation mode registers. These input/output ports are interfaced using a dedicated power supply to allow for connections to the peripheral circuits operating with 5V or 3.3V.

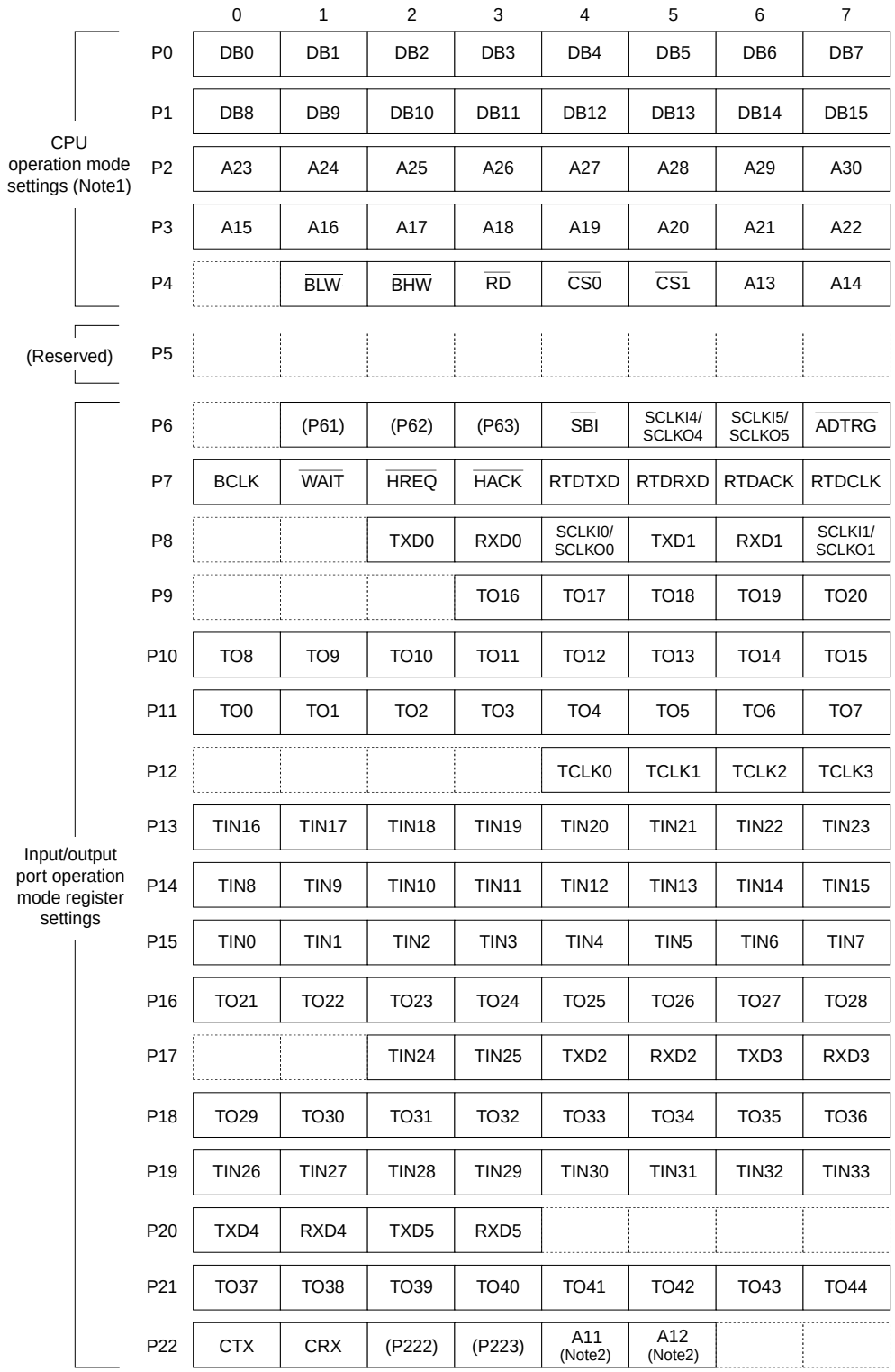
Table 14 Outline of Input/output Ports

Item	Specification
Number of Port	Total 157 ports P0 : P00 - P07 (8 lines) P1 : P10 - P17 (8 lines) P2 : P20 - P27 (8 lines) P3 : P30 - P37 (8 lines) P4 : P41 - P47 (7 lines) P6 : P61 - P67 (7 lines) P7 : P70 - P77 (8 lines) P8 : P82 - P87 (6 lines) P9 : P93 - P97 (5 lines) P10 : P100 - P107 (8 lines) P11 : P110 - P117 (8 lines) P12 : P124 - P127 (4 lines) P13 : P130 - P137 (8 lines) P14 : P140 - P147 (8 lines) P15 : P150 - P157 (8 lines) P16 : P160 - P167 (8 lines) P17 : P172 - P177 (6 lines) P18 : P180 - P187 (8 lines) P19 : P190 - P197 (8 lines) P20 : P200 - P203 (4 lines) P21 : P210 - P217 (8 lines) P22 : P220 - P225 (6 lines)
Port function	The input/output ports can be set for input or output mode bitwise by using the input/output port direction control register. (However, P64 is an $\overline{\text{SBI}}$ input-only port, and P221 is CAN input-only port.)
Pin function	Dual-functions shared with peripheral I/O or external extended signals (or multi-functions shared with peripheral I/Os which have multiple functions.)
Pin function changeover	P0-4, P225, P225 : Changed by setting CPU operation mode (MOD0 and MOD1 pins) P6-22 : Changed by setting the input/output port operation mode register. (However, peripheral I/O pin functions are selected using the peripheral I/O register.)

Table 15 CPU Operation Modes and P0-P4, P224, and P225 Pin Functions

MOD0	MOD1	Operation mode	Pin functions of P0-P4, P224, P225
VSS	VSS	Single-chip mode	nput/output port pin
VSS	VCCE	External extended mode	External extended signal pin
VCCE	VSS	Processor mode (FP pin = VSS)	
VCCE	VCC	Reserved (use inhibited)	–

Note: VCC and VSS are connected to +5 V and GND, respectively.



Note 1: The pin function are selected by setting the MOD0 and MOD1 pins.
Note 2: The pin function are selected by setting the MOD0 and MOD1 pins. Also, use of this pin requires caution because it has a debug event function.

Figure 18 Input/output Ports and Pin Function Assignments

Built-in 10-Channel DMAC

The microcomputer contains 10 channels of DMAC, allowing for data transfer between internal peripheral I/Os, between internal RAM and internal peripheral I/O, and between internal RAMs.

DMA transfer requests can be issued from the user-cre ated software, as well as can be triggered by a signal generated by the internal peripheral I/O (A-D converter, MJT, or serial I/O).

The microcomputer also supports cascaded connection between DMA channels (starting DMA transfer on a channel at end of transfer on another channel). This makes advanced transfer processing possible without causing any additional CPU load.

Table 16 Outline of the DMAC

Item	Content
Number of channels	10 channels
Transfer request	• Software trigger • Request from internal peripheral I/O: A-D converter, multijunction timer, or serial I/O (reception completed, transmit buffer empty) • Cascaded connection between DMA channels possible (Note)
Maximum number of times transferred	256 times
Transferable address space	• 64 Kbytes (address space from H'0080 0000 to H'0080 FFFF) • Transfers between internal peripheral I/Os, between internal RAM and internal peripheral IO, and between internal RAMs are supported
Transfer data size	16 bits or 8 bits
Transfer method	Single transfer DMA (control of the internal bus is relinquished for each transfer performed), dual-address transfer
Transfer mode	Single transfer mode
Direction of transfer	One of three modes can be selected for the source and destination of transfer: • Address fixed • Address increment • 32-channel ring buffer
Channel priority	Channel 0 > channel 1 > channel 2 > channel 3 > channel 4 > channel 5 > channel 6 > channel 7 > channel 8 > channel 9 (Fixed priority)
Maximum transfer rate	13.3 Mbytes per second (when internal peripheral clock = 20 MHz)
Interrupt request	Group interrupt request can be generated when each transfer count register underflows
Transfer area	64 Kbytes from H'0080 0000 to H'0080 FFFF (Transfer is possible in the entire internal RAM/SFR area)

Note: The following DMA channels can be cascaded.

DMA transfer on channel 1 started at end of one DMA transfer on channel 0
DMA transfer on channel 2 started at end of one DMA transfer on channel 1
DMA transfer on channel 0 started at end of one DMA transfer on channel 2
DMA transfer on channel 4 started at end of one DMA transfer on channel 3
DMA transfer on channel 6 started at end of one DMA transfer on channel 5
DMA transfer on channel 7 started at end of one DMA transfer on channel 6
DMA transfer on channel 5 started at end of one DMA transfer on channel 7
DMA transfer on channel 9 started at end of one DMA transfer on channel 8
DMA transfer on channel 5 started at end of all DMA transfers on channel 0 (underflow of transfer count register)

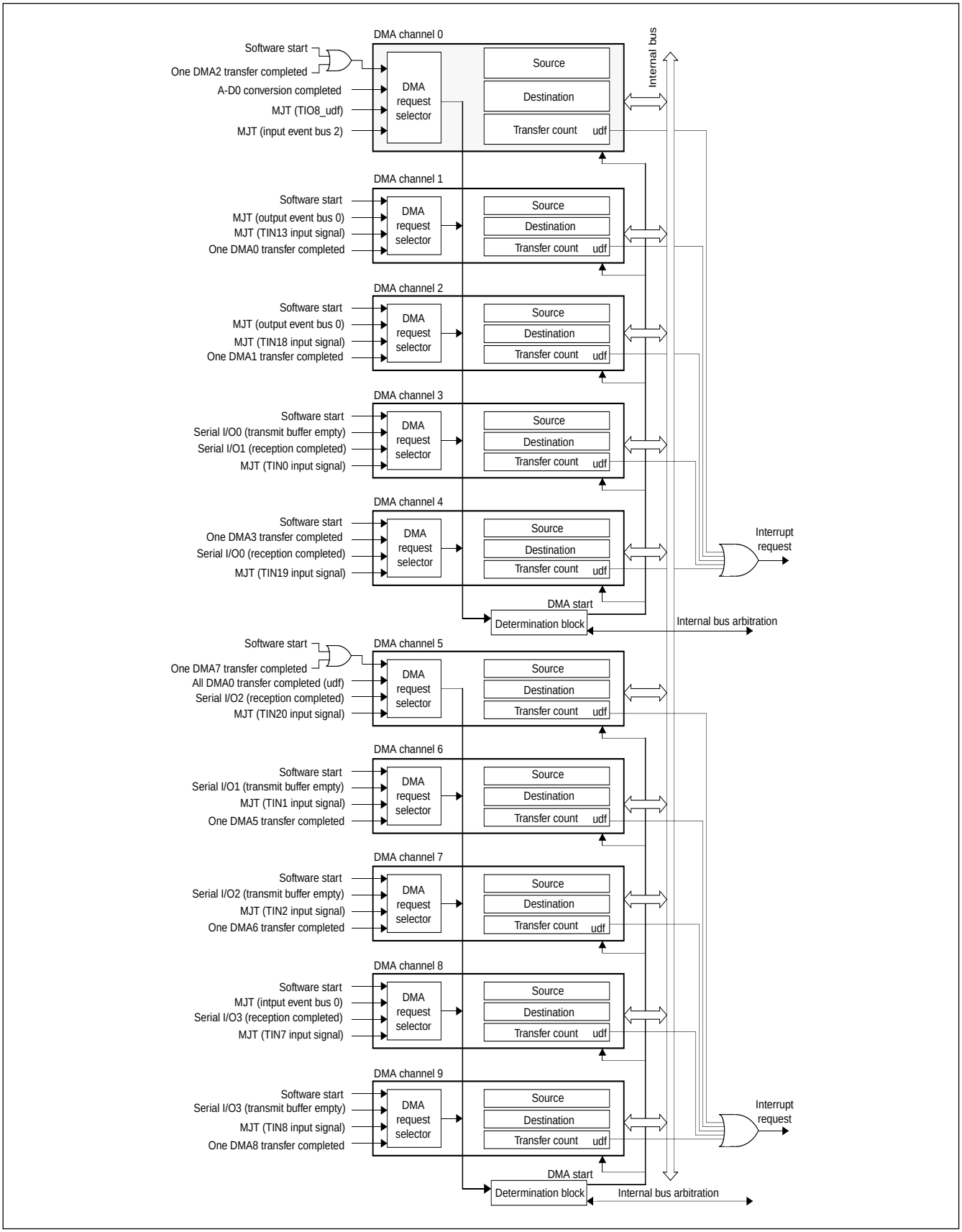


Figure 19 Block Diagram of the DMAC

Built-in 64-Channel Multijunction Timers (MJT)

The microcomputer contains a total of 64 channels of multijunction timers consisting of 35 channels of 16-bit output related timers, 10 channels of 16-bit input/output related timers, 11 channels of 16-bit input related timers, eight channels of 32-bit input related timers. Each timer has multiple operation modes to choose from, depending on the purposes of use.

Also, the maltijunction timers internally have a clock bus, input event bus, and an output event bus, so that multiple timers can be used in combination allowing for a flexible timer configuration.

The output related timers have a correcting function that allows the timer's count value to be incremented or decremented as necessary while count is in progress, making real time output control possible.

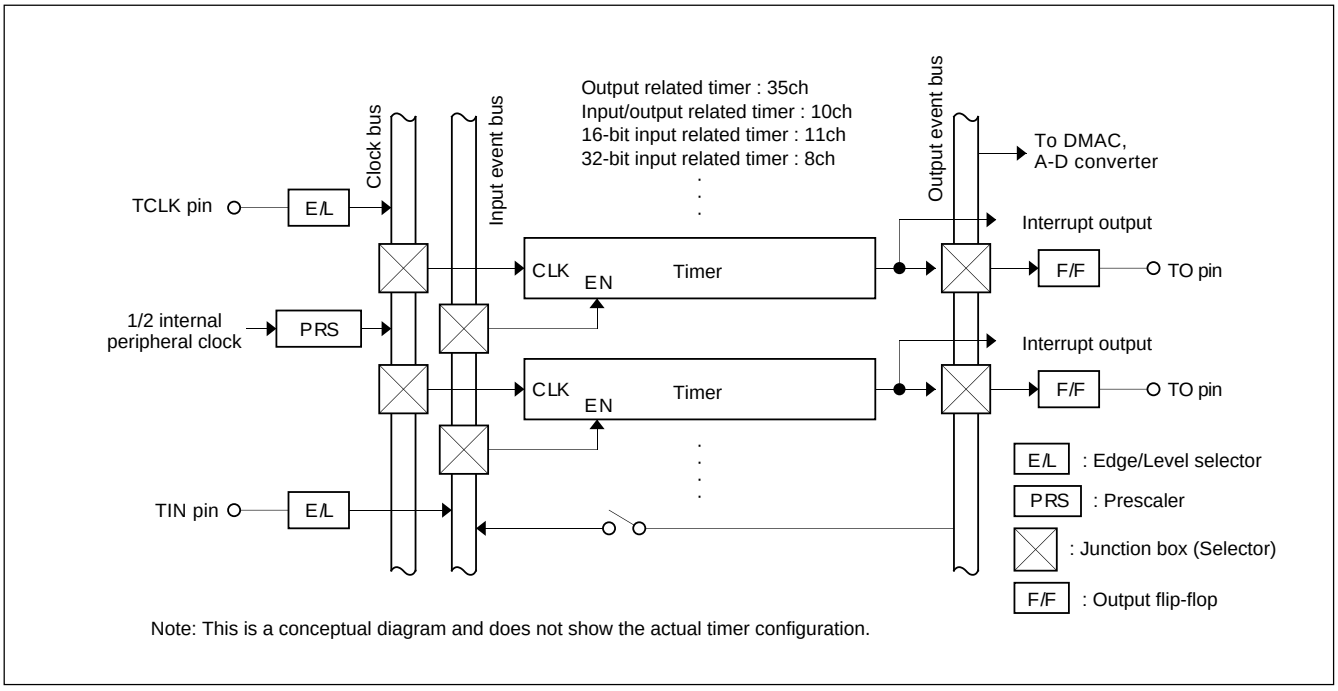


Figure 20 Conceptual Diagram of the Multijunction Timer (MJT)

Table 17 Outline of Multijunction Timers (1/2)

Name	Type	Number of channels	Content
TOP (Timer Output)	Output-related 16-bit timer (down-counter)	11	One of three input modes can be selected in software. < With correction function > • Single-shot output mode • Delayed single-shot output mode < Without correction function > • Continuous output mode
TIO (Timer Input Output)	Input/output-related 16-bit timer (down-counter)	10	One of three input modes or four output modes can be selected by software. < Input modes > • Measure clear input mode • Measure free-run input mode • Noise processing input mode < Output mode without correction function • PWM output mode • Single-shot output mod • Delayed single-shot output mode • Continuous output mode
TMS (Timer Measure Small)	Input-related 16-bit timer (up counter)	8	16-bit input measure timer.
TML (Timer Measure Large)	Input-related 32-bit timer (up counter)	8	32-bit input measure timer.
TID (Timer Input Derivation)	Input-related 16-bit timer (up counter)	3	One of three input modes can be selected in software. • Fixed cycle mode • Event count mode • Multiply-by-4 event count mode

Table 18 Outline of Multijunction Timers (2/2)

Name	Type	Number of channels	Content
TOD (Timer output Modification)	output-related 16-bit timer (down-counter)	16	One of four output modes can be selected in software. < No correction function > • PWM output mode • Single-shot output mode • Delayed single-shot output mode • Continuous output mode
TOM (Timer output Modification)	output-related 16-bit timer (down-counter)	8	One of four output modes can be selected in software. < No correction function > • PWM output mode • Single-shot PWM output mode • One-shot output mode • Continuous output mode

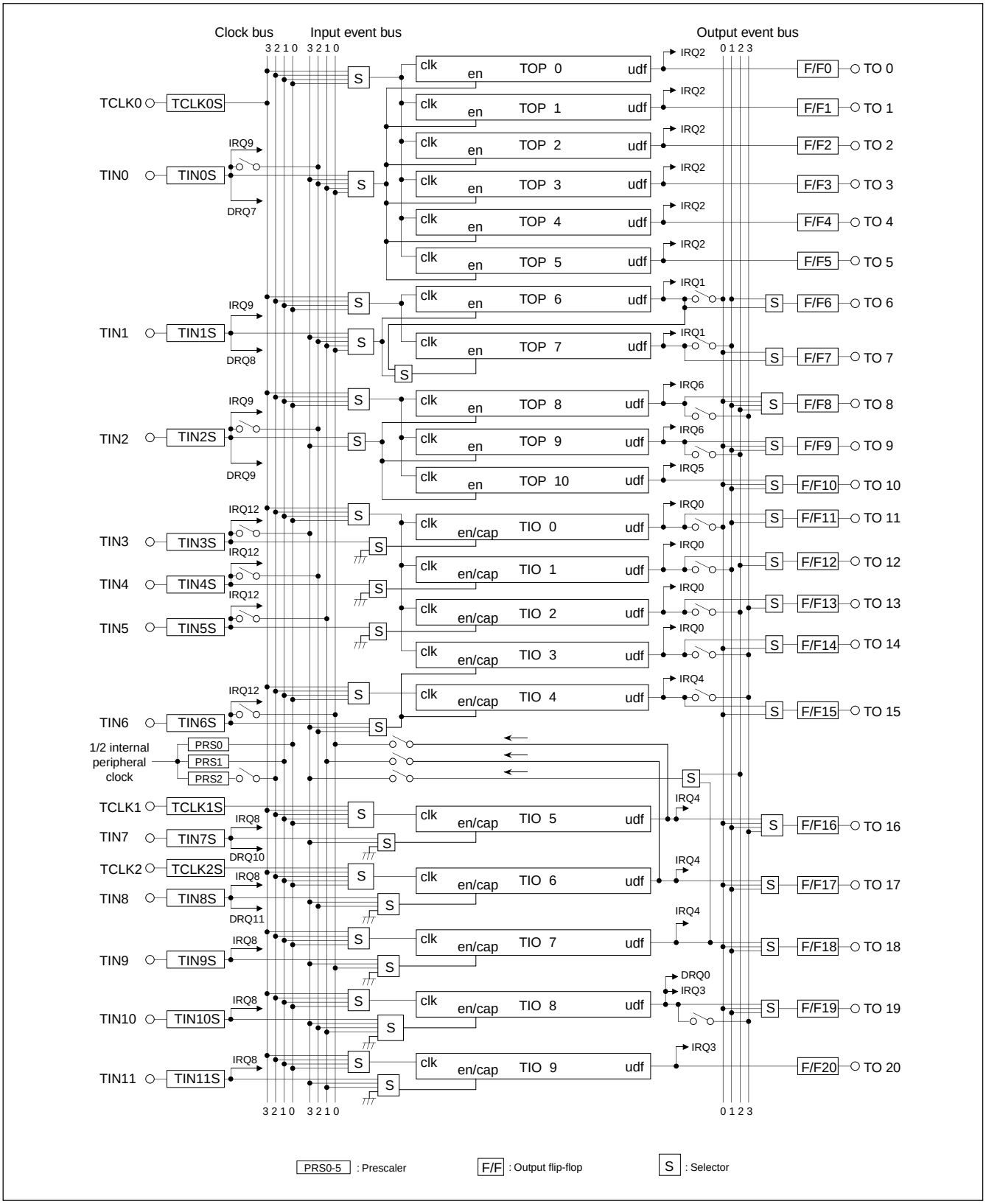


Figure 21 Block Diagram of Multijunction Timers (MJT) (1/4)

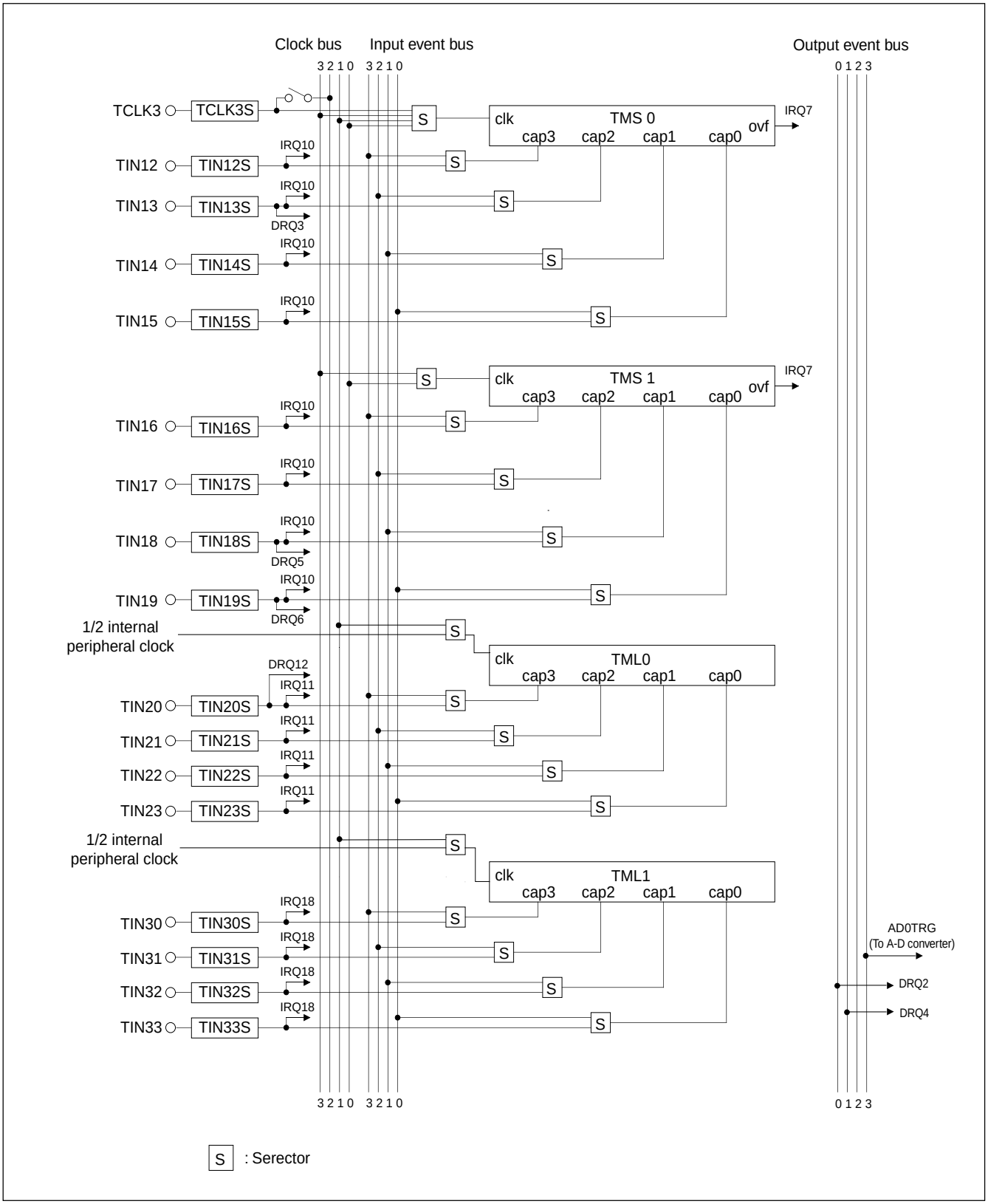


Figure 22 Block Diagram of Multijunction Timers (MJT) (2/4)

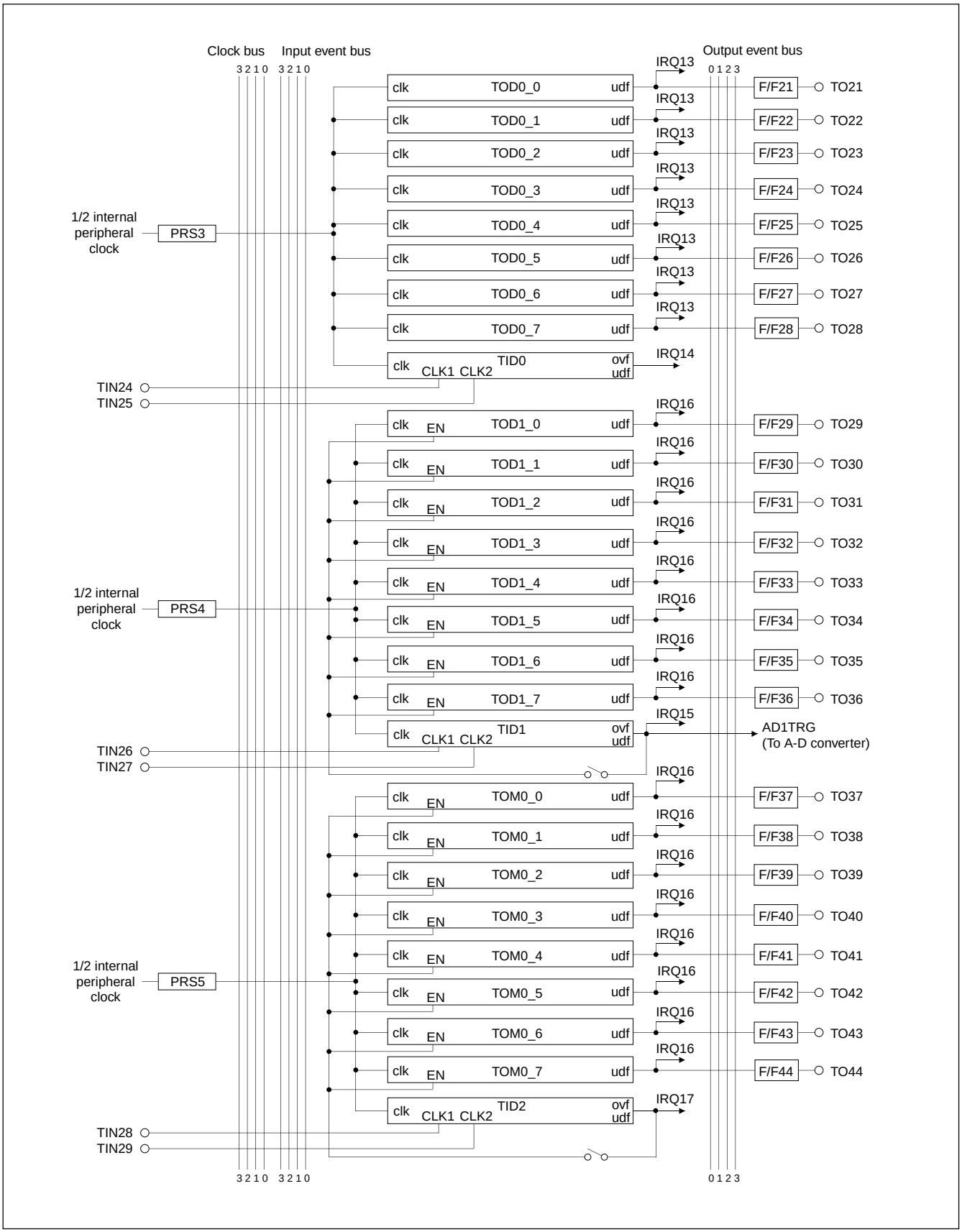


Figure 23 Block Diagram of Multijunction Timers (MJT) (3/4)

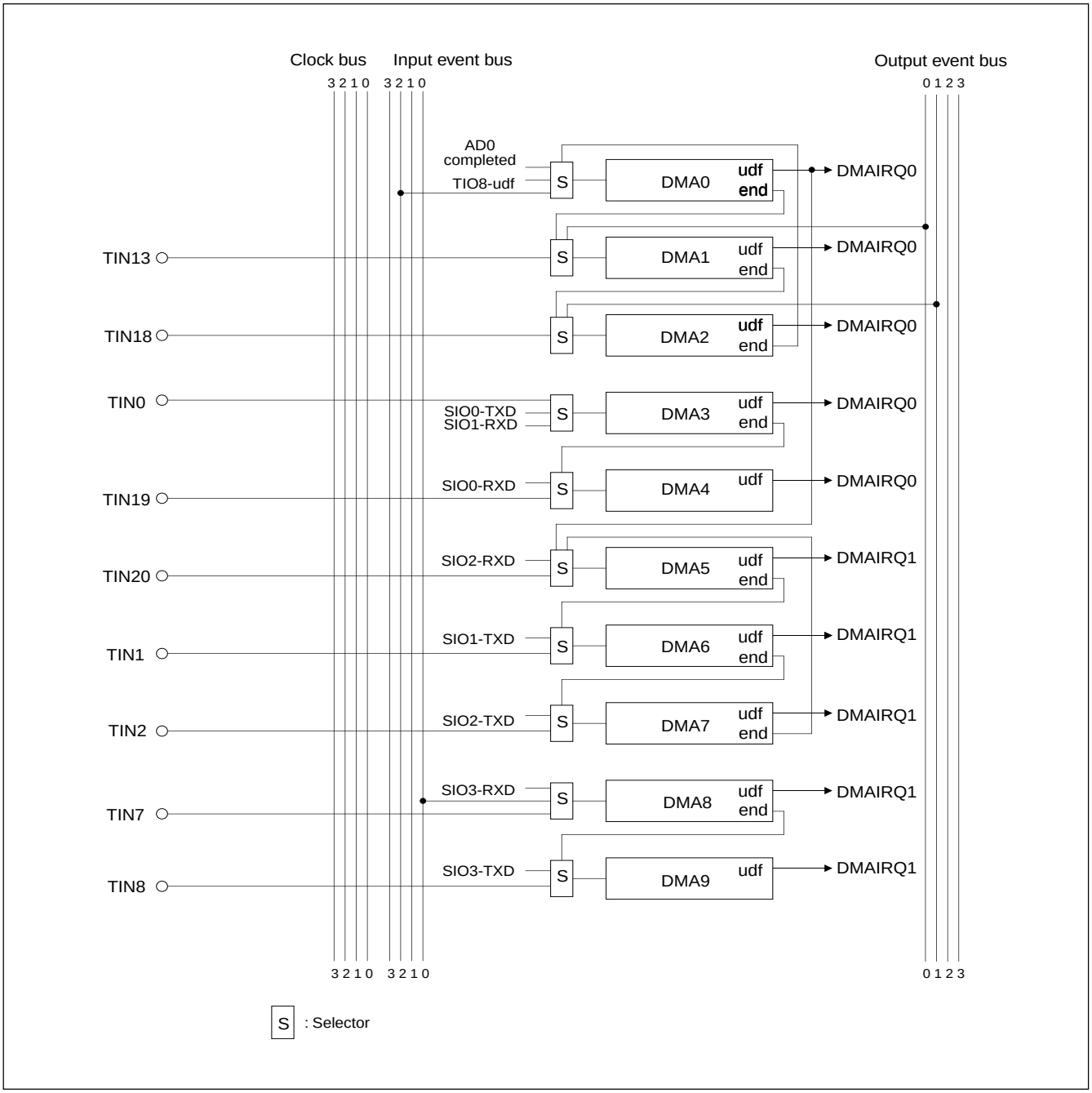


Figure 24 Block Diagram of Multijunction Timers (MJT) (4/4)

Built-in Two Independent A-D Converters

The microcomputer contains two 16-channel converters with 10-bit resolution (A-D0 converter and A-D1 converter). In addition to single conversion on each channel, continuous A-D conversion on a combined group of 4, 8, and 16 channels is possible. The A-D converted value can be read out in either 10 bits or 8 bits.

In addition to ordinary A-D conversion, the converters support comparator mode in which the set value and A-D converted value are compared to determine which is larger or smaller than the other.

When A-D conversion is finished, the converters can generated a DMA transfer request (A-D0 converter only), as well as an interrupt.

The A-D converters are interfaced using a dedicated power supply to allow for connections to the peripheral circuits operating with 5 V or 3.3V.

Table 19 Outline of the A-D Converters

Item	Content		
Analog input	16 channels × 2		
A-D conversion method	Successive approximation method.		
Resolution	10 bits (Conversion results can be read out in either 10 or 8 bits.)		
Absolute accuracy (Note 1)	Normal rate mode	±2 LSB	
(Conditions: Ta = -40 ~ +125°C, AVCC0,1 = VREF0,1 = 5.12V)	Double rate mode	±2 LSB	
Conversion mode	A-D conversion mode,comparator mode		
Operation mode	Single mode, scan mode		
Scan mode	Single -shot scan mode, continuous scan mode.		
Conversion start trigger	Software start	Started by setting A-D conversion start bit to 1.	
	Hardware start	A-D0 converter started by MJT output event bus 3, A-D1 converter started by TID1 overflow or underflow.	
		Started by external $\overline{\text{ADTRG}}$ pin input.	
Conversion rate	During single mode	Normal	299 × 1/ f (BCLK) (Note 2)
f(BCLK) : Internal peripheral clock operating frequency	(Shortest time)	Double speed	173 × 1/ f (BCLK)
	During comparator mode	Normal	47 × 1/ f (BCLK)
	(Shortest time)	Double speed	29 × 1/ f (BCLK)
Interrupt request generation	When A-D conversion is finished, when comparate operation is finished, when single-shot scan is finished, or when one cycle of continuous scan is finished.		
DMA transfer request generation (Note 3)	When A-D conversion is finished, when comparate operation is finished, when single-shot scan is finished, or when one cycle of continuous scan is finished.		

Note 1: The rated value of conversion accuracy here is that of the microcomputer's own as a single unit which can be exhibited when the microcomputer is used in an environment where it may not be affected by the power supply wiring or noise on the board.

Note 2: When BCLK = 20 MHz, this is1/f (BCLK) = 50ns.

Note 3: The DMA transfer request generation function is available for only the A-D0 converter. The A-D1 converter does not have this function.

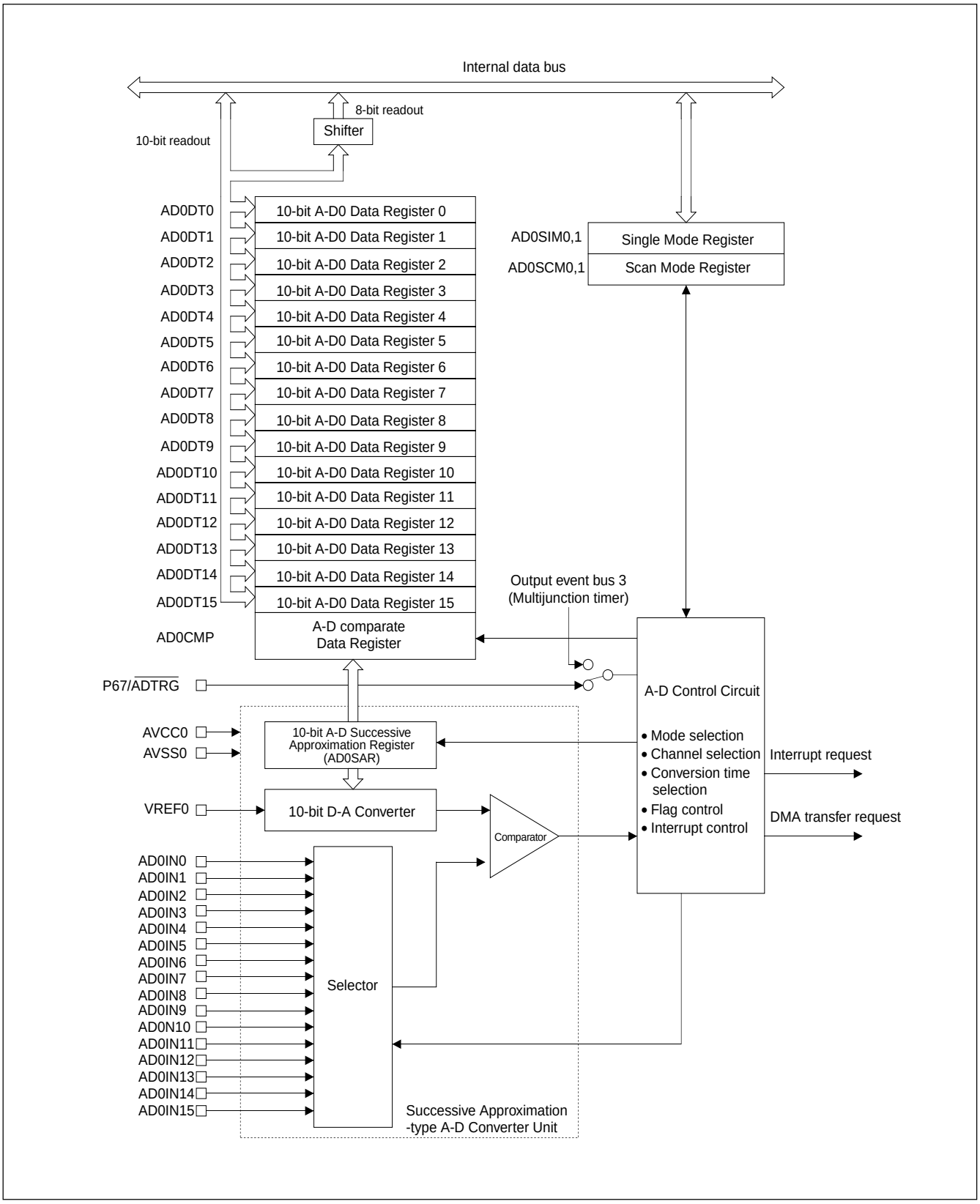
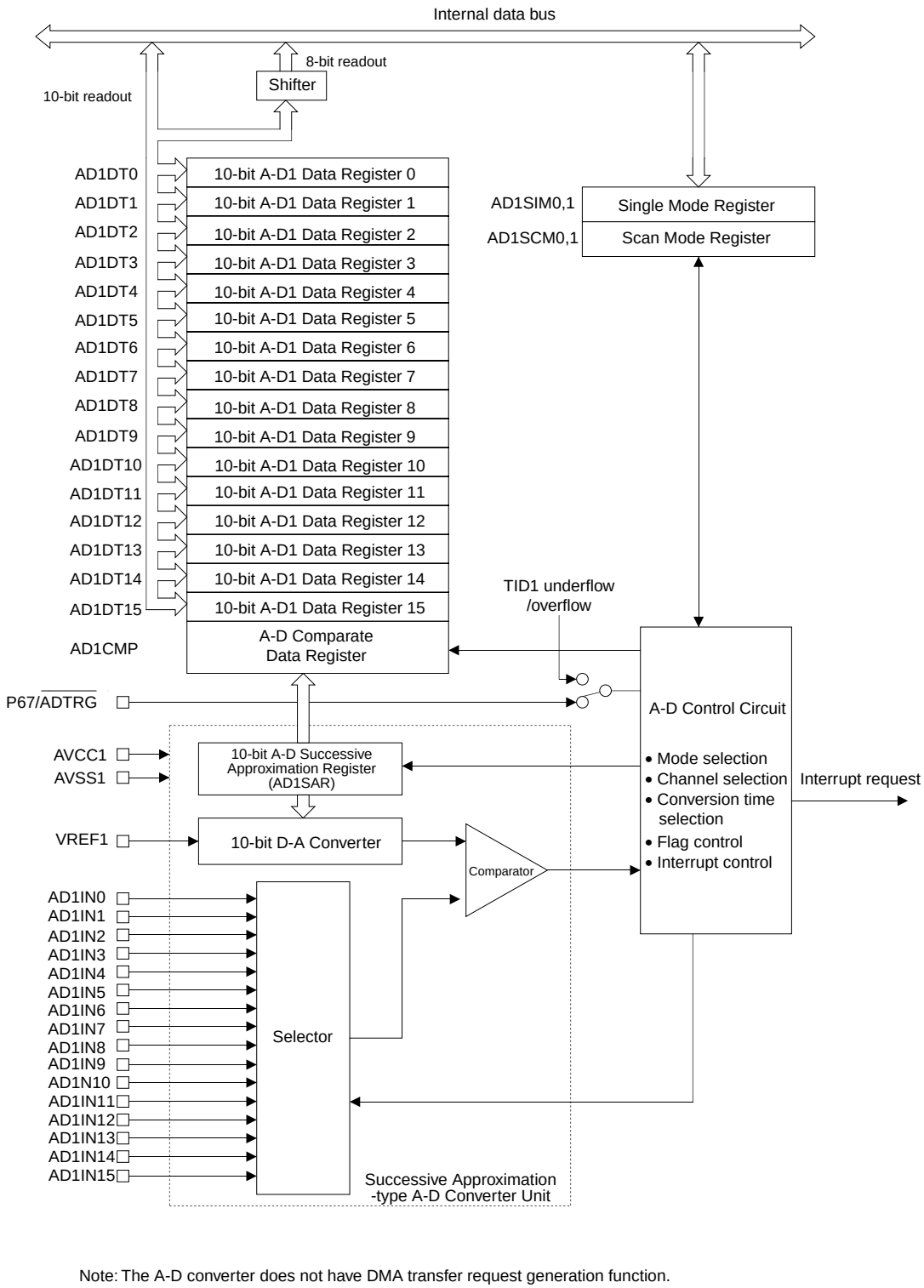


Figure 25 Block Diagram of the A-D0 Converter



Note: The A-D converter does not have DMA transfer request generation function.

Figure 26 Block Diagram of the A-D1 Converter

6-channel High-speed Serial I/Os

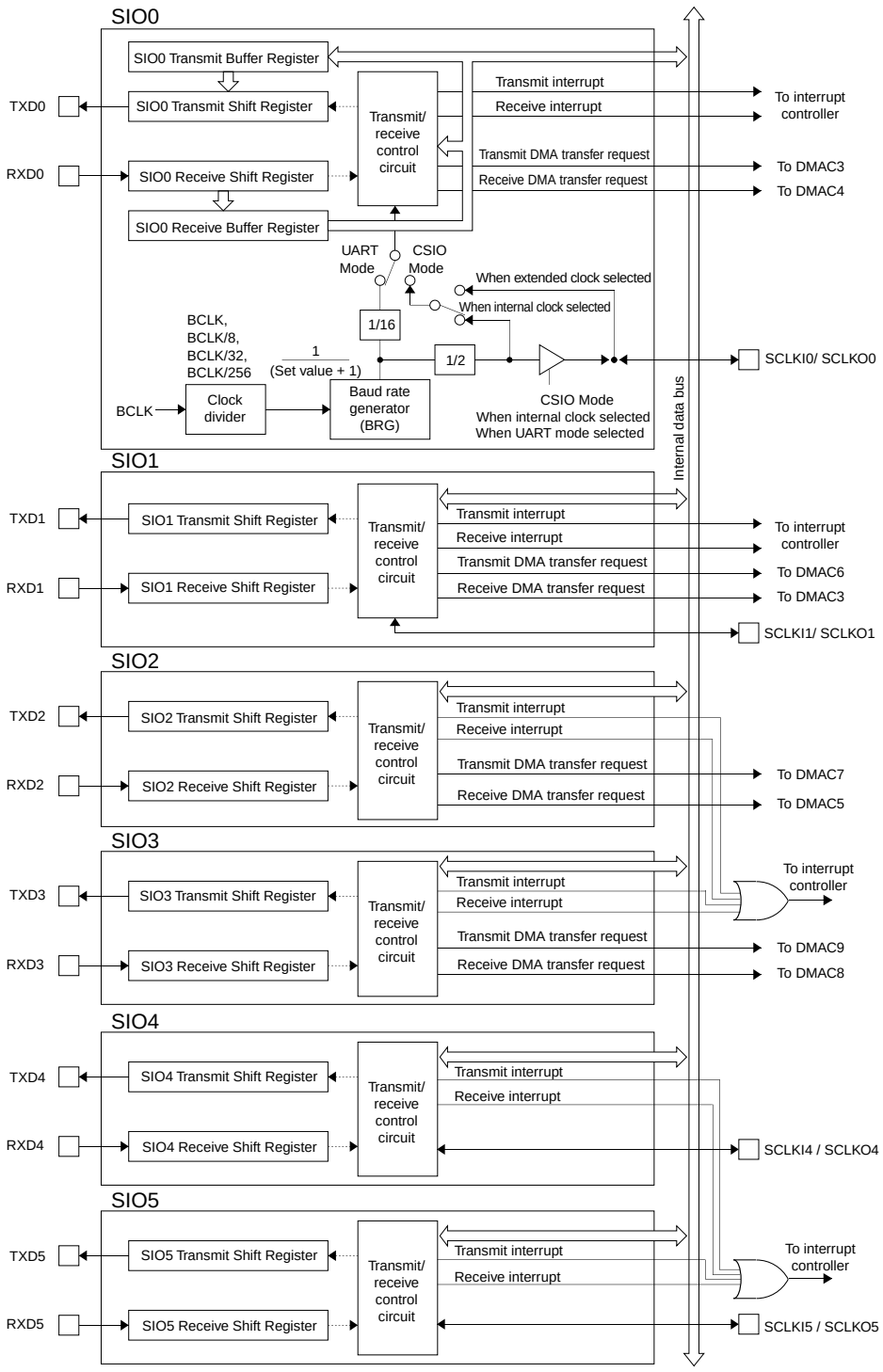
The microcomputer contains six channels of serial I/Os consisting of four channels that can be set for CSIO mode (clock-synchronized serial I/O) or UART mode (asynchronous serial I/O) and two other channels that can only be set for UART mode.

The SIO has the function to generate a DMA transfer request when data reception is completed or the transmit register becomes empty, and is capable of high-speed serial communication without causing any additional CPU load.

Table 20 Outline of Serial I/O

Item	Content	
Number of channels	CSIO/UART: 4 channels (SIO0,SIO1,SIO4,SIO5)	
	UART only : 2 channels (SIO2,SIO3)	
Clock	During CSIO mode : Internal clock / external clock, selectable (Note1)	
	During UART mode : Internal clock only	
Transfer mode	Transmit half-duplex, receive half-duplex, transmit/receive full-duplex	
BRG count sourcef	(BCLK), f(BCLK)/8, f(BCLK)/32, f(BCLK)/256 (When internal clock is selected) (Note2)	
Data format	CSIO mode :	Data length = Fixed to 8 bits Order of transfer = Fixed to LSB first
	UARTmode :	Start bit = 1 bit Character length = 7, 8, or 9 bits Parity bit = Added or not added (When added, selectable between odd and even parity) Stop bit = 1 or 2 bits Order of transfer = Fixed to LSB first
Baud rate	CSIO mode :	152 bits per second to 2 Mbits per second (when operating with f(BCLK) = 20 MHz)
	UARTmode :	19 bits per second to 156 Kbits per second (when operating with f(BCLK) = 20 MHz)
Error detection	CSIO mode :	Overrun error only
	UARTmode :	Overrun, parity, and framing errors (The error-sum bit indicates which error has occurred)
Fixed cycle clock output function	When SIO0, SIO1, SIO4, or SIO5 is in UART mode, this function outputs a 1/2 BRG clock from the SCLK pin.	

Note 1: During CSIO mode, the maximum input frequency of an external clock is f(BCLK) divided by 16.
Note 2: When f(BCLK) is selected for the BRG count source, the BRG set value is subject to limitations.



Note 1: When BCLK is selected, the BRG set value is subject to limitations.

Note 2: SIO2 and SIO3 do not have the SCLKI/SCLKO function.

Figure 27 Block Diagram of Serial I/O

CAN Module

The M32170 and M32174 Group contains two Full CAN modules compliant with CAN Specification V2.0B (CAN0 and CAN1), each of which has 16-channel message slots and three mask registers.

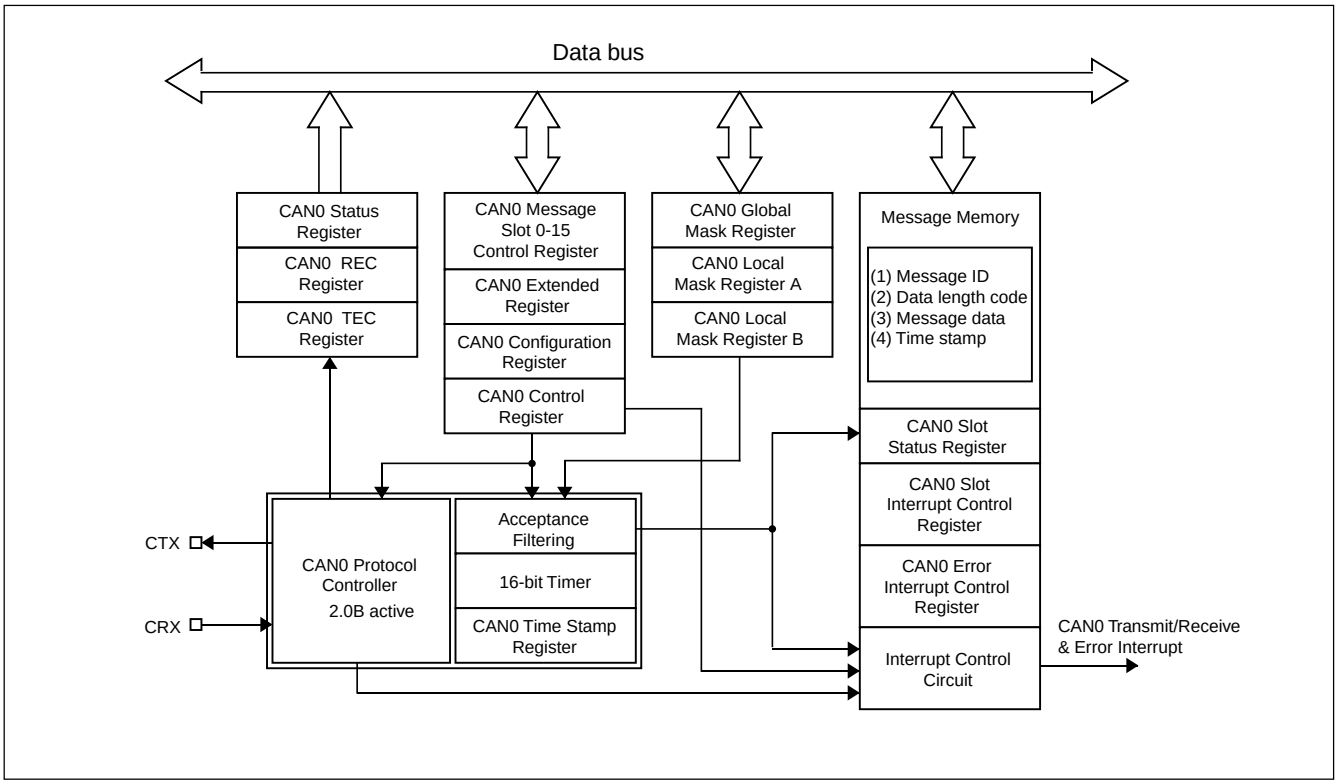


Figure 28 Block Diagram of the CAN Module

8-level Interrupt Controller

The Interrupt Controller controls interrupt requests from each internal peripheral I/O (31 sources) by using eight priority levels assigned to each interrupt source, including interrupts disabled. In addition to these interrupts, it handles System Break Interrupt (SBI), Reserved Instruction Exception (RIE), and Address Exception (AE) as nonmaskable interrupts.

Wait Controller

The Wait Controller supports access to external devices.
For access to an external extended area of up to 1 Mbytes (during external extended or processor mode), the Wait Controller controls bus cycle extension by inserting one to four wait cycles or using external $\overline{\text{WAIT}}$ signal input.

Realtime Debugger (RTD)

The Realtime Debugger (RTD) provides a function for accessing directly from the outside to the internal RAM. It uses a dedicated clock-synchronized serial I/O to communicate with the outside.
Use of the RTD communicating via dedicated serial lines allows the internal RAM to be read out and rewritten without having to halt the CPU.

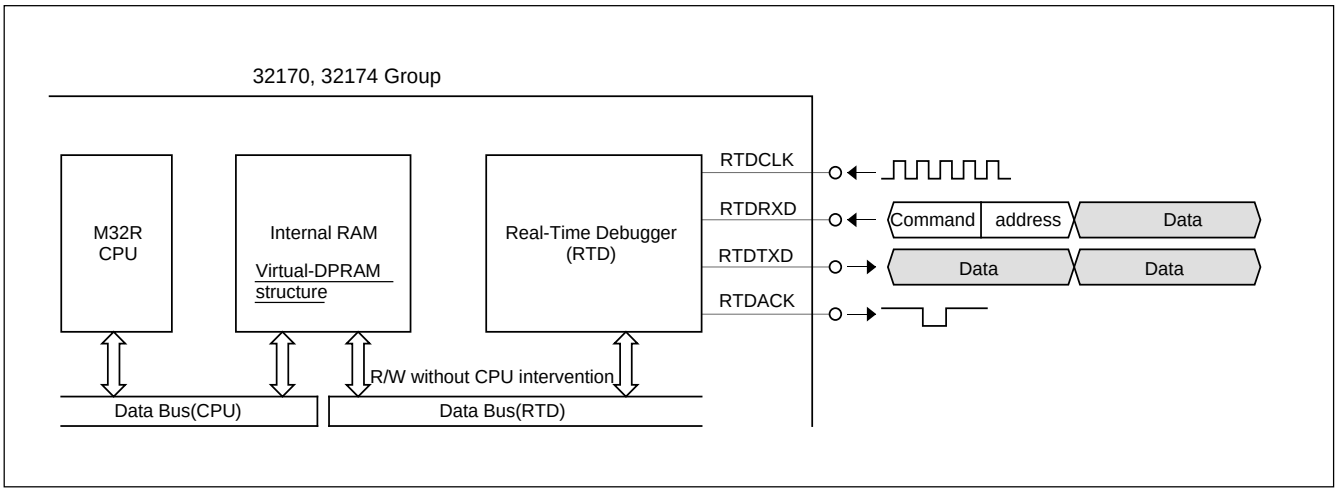


Figure 29 Conceptual Diagram of the Realtime Debugger (RTD)

CPU Instruction Set

The M32R employs a RISC architecture, supporting a total of 83 discrete instructions.

(1) Load/store instructions

Perform data transfer between memory and registers.

LD	Load
LDB	Load byte
LDUB	Load unsigned byte
LDH	Load halfword
LDUH	Load unsigned halfword
LOCK	Load locked
ST	Store
STB	Store byte
STH	Store halfword
UNLOCK	Store unlocked

(2) Transfer instructions

Perform register to register transfer or register to immediate transfer.

LD24	Load 24-bit immediate
LDI	Load immediate
MV	Move register
MVFC	Move from control register
MVTC	Move to control register
SETH	Set high-order 16-bit

(3) Branch instructions

Used to change the program flow.

BC	Branch on C-bit
BEQ	Branch on equal
BEQZ	Branch on equal zero
BGEZ	Branch on greater than or equal zero
BGTZ	Branch on greater than zero
BL	Branch and link
BLEZ	Branch on less than or equal zero
BLTZ	Branch on less than zero
BNC	Branch on not C-bit
BNE	Branch on not equal
BNEZ	Branch on not equal zero
BRA	Branch
JL	Jump and link
JMP	Jump
NOP	No operation

(4) Arithmetic/logic instructions

Perform comparison, arithmetic/logic operation, multiplication/division, or shift between registers.

• Comparison

CMP	Compare
CMPI	Compare immediate
CMPU	Compare unsigned
CMPUI	Compare unsigned immediate

• Logical operation

AND	AND
AND3	AND 3-operand
NOT	Logical NOT
OR	OR
OR3	OR 3-operand
XOR	Exclusive OR
XOR3	Exclusive OR 3-operand

• Arithmetic operation

ADD	Add
ADD3	Add 3-operand
ADDI	Add immediate
ADDV	Add (with overflow checking)
ADDV3	Add 3-operand
ADDX	Add with carry
NEG	Negate
SUB	Subtract
SUBV	Subtract (with overflow checking)
SUBX	Subtract with borrow

• Multiplication/division

DIV	Divide
DIVU	Divide unsigned
MUL	Multiply
REM	Remainder
REMU	Remainder unsigned

• Shift

SLL	Shift left logical
SLL3	Shift left logical 3-operand
SLLI	Shift left logical immediate
SRA	Shift right arithmetic
SRA3	Shift right arithmetic 3-operand
SRAI	Shift right arithmetic immediate
SRL	Shift right logical
SRL3	Shift right logical 3-operand
SRLI	Shift right logical immediate

(5) Instructions for the DSP function

Perform 32 bit × 16 bit or 16 bit × 16 bit multiplication or sum-of-products calculation. These instructions also perform rounding of the accumulator data or transfer between accumulator and general-purpose register.

MACHI	Multiply-accumulate high-order halfwords
MACLO	Multiply-accumulate low-order halfwords
MACWHI	Multiply-accumulate word and high-order halfword
MACWLO	Multiply-accumulate word and low-order halfword
MULHI	Multiply high-order halfwords
MULLO	Multiply low-order halfwords
MULWHI	Multiply word and high-order halfword
MULWLO	Multiply word and low-order halfword
MVFACHI	Move from accumulator high-order word
MVFACLO	Move from accumulator low-order word
MVFACMI	Move from accumulator middle-order word
MVTACHI	Move to accumulator high-order word
MVTACLO	Move to accumulator low-order word
RAC	Round accumulator
RACH	Round accumulator halfword

(6) EIT related instructions

Start trap or return from EIT processing.

RTE	Return from EIT
TRAP	Trap

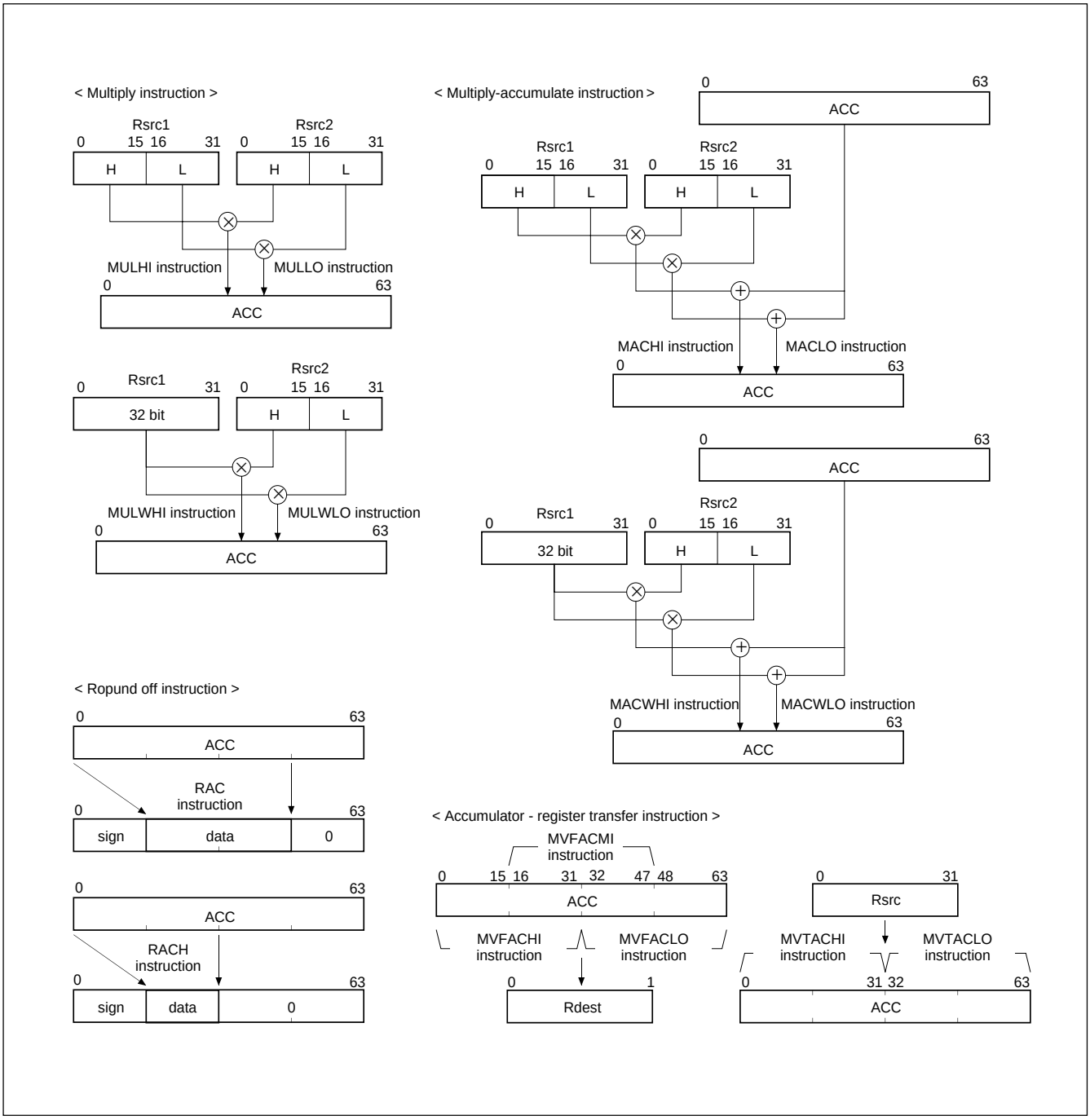


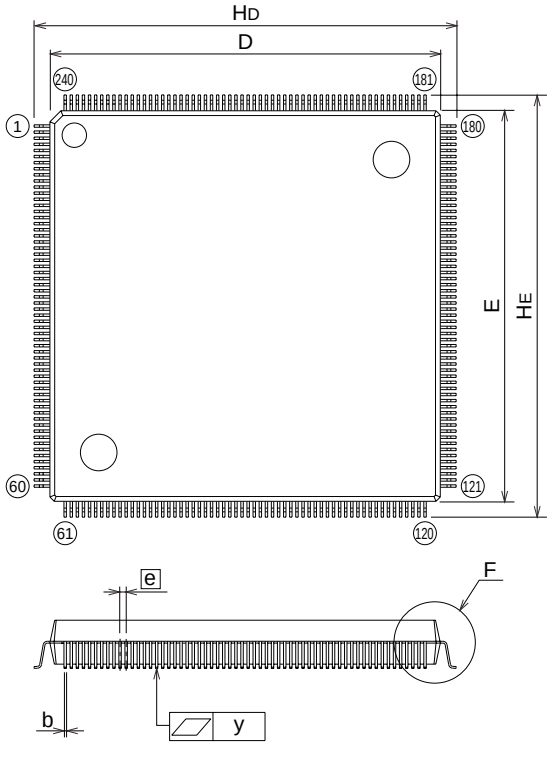
Figure 30 Instructions for the DSP Function

Package Dimensions Diagram

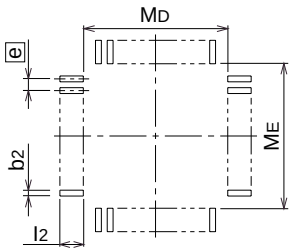
240P6Y-A

Plastic 240pin 32×32mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP240-P-3232-0.50	–		Cu Alloy



Detail F



Recommended Mount Pad

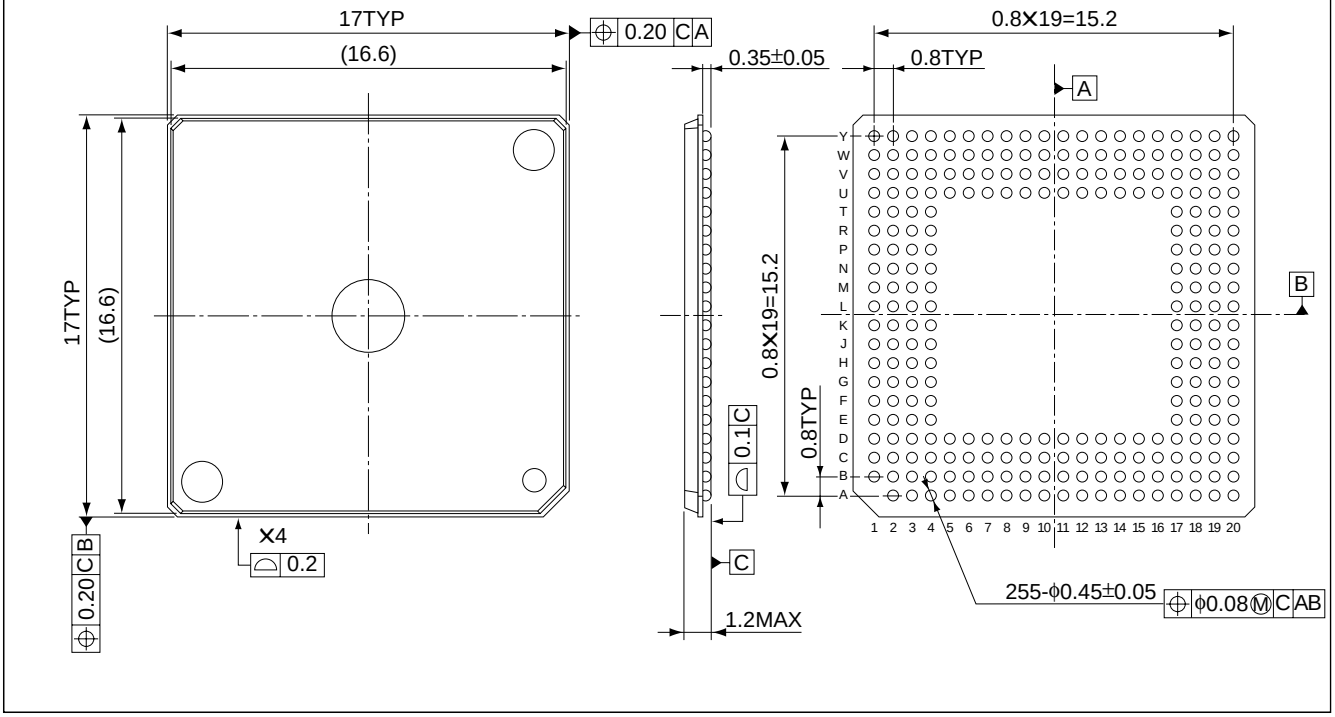
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	4.1
A1	0.25	0.35	0.45
A2	–	3.6	–
b	0.15	0.2	0.3
c	0.13	0.15	0.2
D	31.9	32.0	32.1
E	31.9	32.0	32.1
e	–	0.5	–
HD	34.4	34.6	34.8
HE	34.4	34.6	34.8
L	0.3	0.5	0.7
L1	–	1.3	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	1.2	–	–
MD	–	32.6	–
ME	–	32.6	–

255F7F

255pin 17X17mm body FBGA

EIAJ Package Code	JEDEC Code	Weight(g)
–	–	

Under Development



Note: 255FBGA is currently under development.

MEMO

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Mitsubishi Microcomputers

32170Group, 32174Group

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

MITSUBISHI ELECTRIC CORPORATION
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MITSUBISHI ELECTRIC

Revision Description List	32170 Group, 32174 Group Data Sheet

Rev. No.	Revision Description		Rev. date
	Page	Point	
1.0		First Edition	010514