# Freescale Semiconductor

Technical Data

Document Number: MC33385

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# **Quad Low-side Driver**

The MC33385 is a Quad Low-side Driver fully protected switch. This device is a general purpose Low-side Driver but has been especially designed to operate in engine management applications as injector driver or automotive gear box. It is interfaced directly with a microcontroller for parallel control of the load and the individual output diagnostic is done through a SPI. The diagnostic logic recognizes 4 failure types at each output stage: overcurrent, short to GND, open load, and over-temperature.

## **Features**

- RDSON of 250mΩ per Output at 25°C
- Supplied from the main 5V V<sub>CC</sub>
- Input CMOS Compatible
- Diagnostic through SPI
- Nominal Current of 2A per Output
- · Current Limitation at 3A with Automatic Turn Off
- Output Internally Clamped at 50V typ for Inductive Load Drive
- Junction to Case Thermal Resistance of 4.4°C/W
- Individual Output over Temperature Shutdown
- Pb-Free Packaging Designated by Suffix Code VW

33385

LOW-SIDE DRIVER



DH SUFFIX VW SUFFIX (PB-FREE) 98ASH70702A 20-PIN HSOP

ORDERING INFORMATION						
Device	Temperature Range (T <sub>A</sub> )	Package				
MC33385DH/R2	-40°C to 125°C	20 HSOP				
MC33385VW/R2	-40 0 10 125 0	201130P				

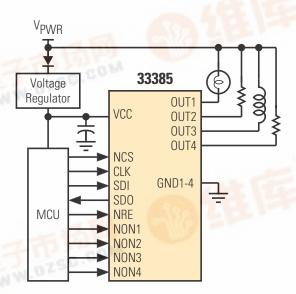


Figure 1. MC33385 Simplified Application Diagram



# **BLOCK DIAGRAM**

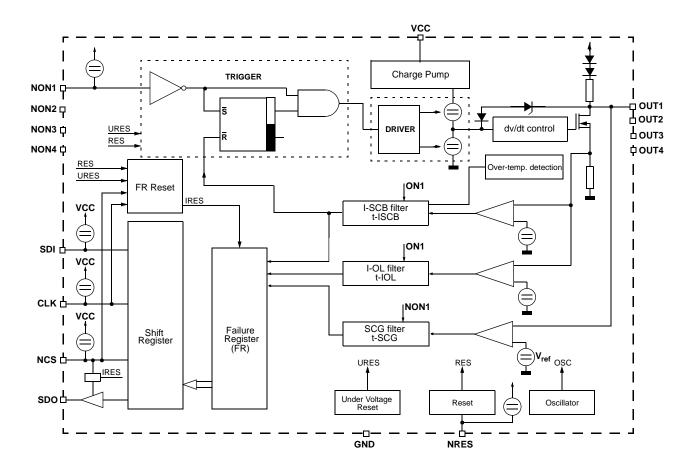


Figure 2. 33385 Simplified Internal Block Diagram

# **PIN CONNECTIONS**

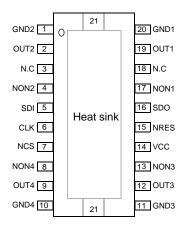


Figure 3. 33385 Pin Connections

Table 1. 33385 Pin Definitions

Pin Number	Pin Name	Definition
1	GND2	Ground 2
2	OUT2	Output Channel 2
3		NC
4	NON2	Input Control Signal for Channel 2
5	SDI	Serial Data Input
6	CLK	Clock Line for Serial Interface
7	NCS	Chip Select for Serial Interface
8	NON4	Input Control Signal for Channel 4
9	OUT4	Output Channel 4
10	GND4	Ground 4
11	GND3	Ground 3
12	OUT3	Output Channel 3
13	NON3	Input Control Signal for Channel 3
14	Vcc	5V Power Supply
15	NRES	Reset Input
16	SDO	Data Output of Serial Interface
17	NON1	Input Control Signal Channel 1
18		NC NC
19	OUT1	Output Channel 1
20	GND1	Ground 1
	Case	Connected to the PCB Ground for Thermal Purposes

# **ELECTRICAL CHARACTERISTICS**

# **MAXIMUM RATINGS**

# **Table 2. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			<u>'</u>
Voltage Range	Vcc	7.0	V
Continuous Output Voltage (With no reverse current)	V <sub>OUT</sub>	45	V
Continuous Current	I <sub>OUTC</sub>	2.5	А
Peak Output Current	I <sub>OUTP</sub>	I <sub>SCBMAX</sub>	А
Clamped Energy at the Switching OFF (See Figure 9)	W <sub>OFF</sub>	70	mJ for 1ms
Input Voltage (Inputs)	V <sub>IN</sub>	V <sub>CC</sub> + 0.3	V
Input Protection Diode Current	I <sub>IN</sub>	1.0	mA
Input Voltage (Outputs)	Vo	V <sub>CC</sub> + 0.3	V
Input Protection Diode Current	I <sub>O</sub>	1.0	mA
THERMAL RATINGS			•
Operating Junction Temperature	$T_J$	150	°C
Thermal Resistance : Junction-case (One power stage in use)	R <sub>THJC</sub>	4.5	kΩ
Thermal Resistance : Junction-ambient (Device soldered on printed circuit board)	R <sub>THJA</sub>	50	kΩ
Peak Package Reflow Temperature During Reflow (1), (2)	T <sub>PPRT</sub>	Note 2	°C

## Notes

- 1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

# **STATIC CHARACTERISTICS**

**Table 3. Static Electrical Characteristics** 

Characteristics noted under conditions 7.0 V  $\leq$  V<sub>SUP</sub>  $\leq$  18 V, -40°C  $\leq$  T<sub>A</sub>  $\leq$  125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T<sub>A</sub> = 25°C under nominal conditions unless otherwise noted.

Supply Voltage Range	Characteristic	Symbol	Min	Тур	Max	Unit
Supply Current (without load) (NON1NON4 = High Level)   S.15V ≥ V <sub>CC</sub>   V	SUPPLY VOLTAGE		<u>'</u>		1	
Junction Temperature Continuous (Continuous) $T_{J1}$ -40   150   $^{\circ}$ C Junction Temperature Dynamical (Time limited) $T_{J2}$   185   $^{\circ}$ C DUTPUT CURRENT   $^{\circ}$ CUDUTPUT   $^{\circ}$ CUDUTPUT CURRENT   $^{\circ}$ CUDUTPUT   $^{\circ}$ CUDUTPUTPUT   $^{\circ}$ CUDUTPUT   $^{\circ}$ CUDUTPUT   $^{\circ}$ CUDUTPUT   $^{\circ}$ CUDUTPUT   $^{\circ}$ CUDUTPUT   $^{\circ}$ CUDUT   $^{\circ}$ CUDUTPUT   $^{\circ}$	Supply Voltage Range	V <sub>CC</sub>	4.5		5.5	V
Junction Temperature Dynamical (Time limited)   T_{J2}   185 °CC	JUNCTION TEMPERATURE		<u>'</u>		1	
DUTPUT CURRENT   DU	Junction Temperature Continuous (Continuous)	T <sub>J1</sub>	- 40		150	°C
Output Current Range         IouT         Iscandax         A           RESET BEHAVIOUR         Reset Changeable (at NRES-Pin)         Vcc         Vccres         5.5         V           Undervoltage Reset (Independent of NRES)         Vccres         3.35         3.95         V           Active for Vcc = OV to VcCPRO         VcCRES         3.35         3.95         V           INDERVOLTAGE PROTECTION         Protection active for Vcc = OV to VcCPRO         VcCPRO         1.5         4.0         V           VVER TEMPERATURE         Temperature Detection Threshold         TopF         155         185         *C           Supply Current (without load) (NON1NON4 = High Level)         Standby Current (without load) (NON1NON4 = High Level)         IccSTB1	Junction Temperature Dynamical (Time limited)	T <sub>J2</sub>			185	°C
Reset Changeable (at NRES-Pin)   V <sub>CC</sub>   V <sub>CCRES</sub>   5.5   V	OUTPUT CURRENT	1	<u> </u>			
Reset Changeable (at NRES-Pin)         V <sub>CC</sub> V <sub>CCRES</sub> 5.5         V           Undervoltage Reset (Independent of NRES)         V <sub>CCRES</sub> 3.35         3.95         V           Active for V <sub>CC</sub> = 0V to V <sub>CCPRO</sub> V <sub>CCPRO</sub> 1.5         4.0         V           DIDDERVOLTAGE PROTECTION           Protection active for V <sub>CC</sub> = 0V to V <sub>CCPRO</sub> V <sub>CCPRO</sub> 1.5         4.0         V           DVER TEMPERATURE           Temperature Detection Threshold         T <sub>OFF</sub> 155         185         °C           SUPPLY CURRENT           Standby Current (without load) (NON1NON4 = High Level)         I <sub>CCSTB1</sub> I <sub>CCSTB2</sub> 6.0         mA           5.15V ≥ V <sub>CC</sub> I <sub>CCSTB2</sub> I <sub>CCSTB2</sub> 7.0         mA           Alc <sub>CC</sub> During Reverse Output Current         ΔI <sub>CC</sub> 100         mA           Alc <sub>CC</sub> During Reverse Output Current         ΔI <sub>CC</sub> 100         mA           INPUTS (NONx, NCS, CLK, NRES, SDI)           Low Threshold         V <sub>IN</sub> -0.3         0.2*V <sub>CC</sub> V           High Threshold         V <sub>IN</sub> -0.3         0.2*V <sub>CC</sub> V	Output Current Range	I <sub>OUT</sub>			I <sub>SCBMAX</sub>	A
Undervoltage Reset (Independent of NRES)         VCCRES         3.35         3.95         V           Active for V <sub>CC</sub> = 0V to V <sub>CCPRO</sub> VCCRES         3.35         3.95         V           JNDERVOLTAGE PROTECTION         Protection active for V <sub>CC</sub> = 0V to V <sub>CCPRO</sub> VCCPRO         1.5         4.0         V           OVER TEMPERATURE         Temperature Detection Threshold         ToFF         155         185         °C           SUPPLY CURRENT         Standby Current (without load) (NON1NON4 = High Level)         IccSTB1         6.0         mA           5.15V ≥ V <sub>CC</sub> IccSTB2         7.0         mA           Operating Mode (For 5.15V ≥ V <sub>CC</sub> ) (lout 14) = 2A         IcCSTB2         7.0         mA           ΔI <sub>CC</sub> During Reverse Output Current (I <sub>OUT</sub> = -5A on one output)         ΔI <sub>CC</sub> 100         mA           INPUTS (NONx, NCS, CLK, NRES, SDI)         Low Threshold         VINL         -0.3         0.2*V <sub>CC</sub> V           High Threshold         VINH         0.7*V <sub>CC</sub> V <sub>CC</sub> + 0.3         V           Hysteresis         VHYST         0.85         V           Input Current (V <sub>IN</sub> = V <sub>CC</sub> )         InN         -100         -20         µA	RESET BEHAVIOUR	1	l l			
Undervoltage Reset (Independent of NRES)         V <sub>CCRES</sub> 3.35         3.95         V           Active for V <sub>CC</sub> = 0V to V <sub>CCPRO</sub> V <sub>CCPRO</sub> 3.35         3.95         V           INDERVOLTAGE PROTECTION           Protection active for V <sub>CC</sub> = 0V to V <sub>CCPRO</sub> V <sub>CCPRO</sub> 1.5         4.0         V           VEX. 200 (C) (VCC) (C) (C) (C) (C) (C) (C) (C) (C) (C)	Reset Changeable (at NRES-Pin)	V <sub>CC</sub>	V <sub>CCRES</sub>		5.5	V
Active for $V_{CC} = 0V$ to $V_{CCPRO}$ JNDERVOLTAGE PROTECTION  Protection active for $V_{CC} = 0V$ to $V_{CCPRO}$ VCCPRO  VCCPRO  1.5  4.0  V  DVER TEMPERATURE  Temperature Detection Threshold  TOFF  155  185  CC  SUPPLY CURRENT  Standby Current (without load) (NON1NON4 = High Level) 5.15V $\geq V_{CC}$ 5.5V $\geq V_{CC}$ 1.5.5V $\geq V_{CC}$ 1.6.0  TOPER TEMPERATURE  Temperature Detection Threshold  TOFF  155  185  CC  SUPPLY CURRENT  Standby Current (without load) (NON1NON4 = High Level) 5.15V $\geq V_{CC}$ 1.0.0  TOPER TEMPERATURE  Temperature Detection Threshold  Solve Temperature Detection Threshold (NON1NON4 = High Level) 5.15V $\geq V_{CC}$ 1.0.0  TOPERATURE  TOPERATURE  TOPERATURE  1.0.0  TOPERATURE	Undervoltage Reset (Independent of NRES)	V <sub>CCRES</sub>	+		3.95	V
Protection active for V <sub>CC</sub> =0V to V <sub>CCPRO</sub>   V <sub>CCP</sub>	Active for $V_{CC} = 0V$ to $V_{CCPRO}$					
DVER TEMPERATURE  Temperature Detection Threshold $T_{OFF}$ 155 185 °C  SUPPLY CURRENT  Standby Current (without load) (NON1NON4 = High Level)  5.15V ≥ V <sub>CC</sub> 5.5V ≥ V <sub>CC</sub> 1 CCSTB1 1 CCSTB2 7.0 mA  Al <sub>CC</sub> During Reverse Output Current (lout 14) = 2A 1 CCOPM 177 mA  Al <sub>CC</sub> During Reverse Output Current (lout 14) = 2A 1 CCOPM 5.50 mA  INPUTS (NONX, NCS, CLK, NRES, SDI)  Low Threshold V <sub>INL</sub> -0.3 0.2°V <sub>CC</sub> V  High Threshold V <sub>INH</sub> 0.7°V <sub>CC</sub> V <sub>CC+0.3</sub> V  Hysteresis V <sub>HYST</sub> 0.85 V  Input Current (V <sub>IN</sub> = V <sub>CC</sub> ) Input Current (lin) 10 $\mu$ A  Input Current (V <sub>CC</sub> > V <sub>RES</sub> & 0V <v<sub>IN &lt; 0.9°V<sub>CC</sub>) Input Current (V<sub>CC</sub> &gt; V<sub>CC+0.3</sub> V  High Output Level (I<sub>SDO</sub> = -2mA) V  Low Output Level (I<sub>SDO</sub> = -2mA) V  Low Output Level (I<sub>SDO</sub> = 3.2mA) V  OUTPUTS (OUT 14)  Average Output Current Input Current (I<sub>OUTA</sub> 2.5 A A</v<sub>	UNDERVOLTAGE PROTECTION					
Temperature Detection Threshold T <sub>OFF</sub> 155 185 °C  SUPPLY CURRENT  Standby Current (without load) (NON1NON4 = High Level)  5.15V ≥ V <sub>CC</sub> 5.5V ≥ V <sub>CC</sub> 1   CCSTB1   CCSTB2   F.O.0	Protection active for $V_{CC} = 0V$ to $V_{CCPRO}$	V <sub>CCPRO</sub>	1.5		4.0	V
Supply Current (without load) (NON1NON4 = High Level)   Standby Current (without load) (NON1NON4 = High Level)   Sit5V ≥ V <sub>CC</sub>	OVER TEMPERATURE		•		•	
Standby Current (without load) (NON1NON4 = High Level) $  \begin{array}{ccccccccccccccccccccccccccccccccccc$	Temperature Detection Threshold	T <sub>OFF</sub>	155		185	°C
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	SUPPLY CURRENT	- I				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Standby Current (without load) (NON1NON4 = High Level)					
Operating Mode (For 5.15V $\geq$ V <sub>CC</sub> ) (Iout 14) = 2A		I <sub>CCSTB1</sub>			6.0	mA
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	5.5V ≥ V <sub>CC</sub>	I <sub>CCSTB2</sub>			7.0	mA
INPUTS (NONx, NCS, CLK, NRES, SDI)	Operating Mode (For $5.15V \ge V_{CC}$ ) (lout $14$ ) = 2A	I <sub>CCOPM</sub>			17	mA
INPUTS (NONx, NCS, CLK, NRES, SDI)  Low Threshold $V_{INL}$ -0.3 0.2*V <sub>CC</sub> V  High Threshold $V_{INH}$ 0.7*V <sub>CC</sub> V <sub>CC</sub> +0.3 V  Hysteresis $V_{HYST}$ 0.85 V  Input Current ( $V_{IN} = V_{CC}$ ) $I_{IN}$ 10 $\mu$ A  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9*V_{CC}$ ) $I_{IN}$ -100 -20 $\mu$ A  SERIAL DATA OUTPUT  High Output Level ( $I_{SDO} = -2mA$ ) $V_{SDOH}$ V <sub>CC</sub> -0.4 V  Low Output Level ( $I_{SDO} = 3.2mA$ ) $V_{SDOL}$ 0.4 V  Tristate Leakage Current (NCS = HIGH, $V_{SDO} = 0V$ to $V_{CC}$ ) $I_{SDOL}$ -10 10 $\mu$ A  OUTPUTS (OUT 14)  Average Output Current $I_{OUTA}$ 2.5 $I_{OUTA}$	ΔI <sub>CC</sub> During Reverse Output Current	Δl <sub>CC</sub>			100	mA
Low Threshold $V_{INL}$ -0.3       0.2*V <sub>CC</sub> V         High Threshold $V_{INH}$ 0.7*V <sub>CC</sub> $V_{CC} + 0.3$ V         Hysteresis $V_{HYST}$ 0.85       V         Input Current ( $V_{IN} = V_{CC}$ ) $I_{IN}$ 10 $\mu$ A         Input Current ( $V_{CC} > V_{RES} & 0V < V_{IN} < 0.9*V_{CC}$ ) $I_{IN}$ -100       -20 $\mu$ A         SERIAL DATA OUTPUT       High Output Level ( $I_{SDO} = -2mA$ ) $V_{SDOH}$ $V_{CC} - 0.4$ $V_$	(I <sub>OUT</sub> = - 5A on one output)				50	mA
High Threshold $V_{INH}$ $0.7^*V_{CC}$ $V_{CC} + 0.3$ $V$ Hysteresis $V_{HYST}$ $0.85$ $V$ Input Current ( $V_{IN} = V_{CC}$ ) $I_{IN}$ $10$ $\mu A$ Input Current ( $V_{CC} > V_{RES} & 0V < V_{IN} < 0.9^*V_{CC}$ ) $I_{IN}$ $-100$ $-20$ $\mu A$ SERIAL DATA OUTPUTHigh Output Level ( $I_{SDO} = -2mA$ ) $V_{SDOH}$ $V_{CC} - 0.4$ $V$ Low Output Level ( $I_{SDO} = 3.2mA$ ) $V_{SDOL}$ $0.4$ $V$ Tristate Leakage Current (NCS = HIGH, $V_{SDO} = 0V$ to $V_{CC}$ ) $I_{SDOL}$ $-10$ $10$ $\mu A$ OUTPUTS (OUT 14)Average Output Current $I_{OUTA}$ $2.5$ $A$	INPUTS (NONx, NCS, CLK, NRES, SDI)				•	
Hysteresis $V_{HYST}$ 0.85 $V_{HYST}$ 0.85 $V_{HYST}$ Input Current ( $V_{IN} = V_{CC}$ ) $I_{IN}$ 10 $\mu$ A Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9*V_{CC}$ ) $I_{IN}$ -100 -20 $\mu$ A SERIAL DATA OUTPUT  High Output Level ( $I_{SDO} = -2mA$ ) $V_{SDOH}$ $V_{CC} = 0.4$ $V_{SDOH}$ Low Output Level ( $I_{SDO} = 3.2mA$ ) $V_{SDOL}$ 0.4 $V_{SDOL}$ 10	Low Threshold	V <sub>INL</sub>	-0.3		0.2*V <sub>CC</sub>	V
Input Current ( $V_{IN} = V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  Input Current ( $V_{CC} > V_{RES} \& 0V < V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{RES} \& 0V < V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} > V_{CC} > V_{CC} > V_{CC}$ )  Input Current ( $V_{CC} $	High Threshold	V <sub>INH</sub>	0.7*V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
Input Current ( $V_{CC} > V_{RES} \& 0V < V_{IN} < 0.9^*V_{CC}$ )  IIN  - 100  - 20 $\mu A$ SERIAL DATA OUTPUT  High Output Level ( $I_{SDO} = -2mA$ ) $V_{SDOH}$ $V_{SDOH}$ $V_{CC} - 0.4$ $V_{SDOL}$ Tristate Leakage Current ( $V_{CC} = V_{CC} = V$	Hysteresis	V <sub>HYST</sub>	0.85			V
High Output Level ( $I_{SDO}$ = -2mA) $V_{SDOH}$ $V_{CC}$ - 0.4 $V_{CC}$ Using the leakage Current (NCS = HIGH, $V_{SDO}$ = 0V to $V_{CC}$ ) $V_{SDOL}$ 10 10 $V_{CC}$ OUTPUTS (OUT 14)  Average Output Current $V_{CC}$	Input Current (V <sub>IN</sub> = V <sub>CC</sub> )	I <sub>IN</sub>			10	μΑ
High Output Level ( $I_{SDO} = -2mA$ )  V <sub>SDOH</sub> V <sub>CC</sub> - 0.4  V  Low Output Level ( $I_{SDO} = 3.2mA$ )  V <sub>SDOL</sub> V <sub>SDOL</sub> Output Level ( $I_{SDO} = 3.2mA$ )  V <sub>SDOL</sub> V <sub>SDOL</sub> 10  10 $I_{SDOL}$ Outputs (OUT 14)  Average Output Current  I <sub>OUTA</sub> 2.5  A	Input Current (V <sub>CC</sub> >V <sub>RES</sub> & 0V <v<sub>IN &lt; 0.9*V<sub>CC</sub>)</v<sub>	I <sub>IN</sub>	- 100		- 20	μΑ
Low Output Level ( $I_{SDO} = 3.2 \text{mA}$ )  Tristate Leakage Current (NCS = HIGH, $V_{SDO} = 0 \text{V to } V_{CC}$ ) $I_{SDOL}$ - 10  10 $\mu \text{A}$ OUTPUTS (OUT 14)  Average Output Current $I_{OUTA}$ 2.5  A	SERIAL DATA OUTPUT		<u>'</u>		<u> </u>	
Low Output Level ( $I_{SDO} = 3.2 \text{mA}$ )  Tristate Leakage Current (NCS = HIGH, $V_{SDO} = 0 \text{V to } V_{CC}$ ) $I_{SDOL}$ - 10  10 $\mu A$ OUTPUTS (OUT 14)  Average Output Current $I_{OUTA}$ 2.5  A	High Output Level (I <sub>SDO</sub> = -2mA)	V <sub>SDOH</sub>	V <sub>CC</sub> - 0.4			V
Tristate Leakage Current (NCS = HIGH, $V_{SDO}$ = 0V to $V_{CC}$ )  I <sub>SDOL</sub> - 10  10 $\mu$ A  OUTPUTS (OUT 14)  Average Output Current  I <sub>OUTA</sub> 2.5  A	Low Output Level (I <sub>SDO</sub> = 3.2mA)				0.4	V
OUTPUTS (OUT 14)  Average Output Current  I OUTA  2.5  A	Tristate Leakage Current (NCS = HIGH, $V_{SDO} = 0V$ to $V_{CC}$ )		- 10		10	μА
O to I Publication	OUTPUTS (OUT 14)	l	<u> </u>		1	
O to d Park O mark	Average Output Current	I <sub>OUTA</sub>	2.5			Α
	Output Peak Current	I <sub>OUTP</sub>	I <sub>SCBMAX</sub>			Α

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V  $\leq$  V<sub>SUP</sub>  $\leq$  18 V, -40°C  $\leq$  T<sub>A</sub>  $\leq$  125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T<sub>A</sub> = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
Leakage Current 1 (NON = High, V <sub>OUT</sub> = 25V, V <sub>CC</sub> = 5V)	I <sub>OUTL</sub>			10	μА
Leakage Current 2 (NON = High, V <sub>OUT</sub> = 16V, V <sub>CC</sub> = 1V)	I <sub>OUTL2</sub>			10	μА
Output Clamp Voltage (I <sub>OUT</sub> = 1A)	V <sub>CLP</sub>	45	50	58	V
Matching Clamp Voltage (Between two outputs)	V <sub>CLPM</sub>	V <sub>CLP-1</sub>		V <sub>CLP+1</sub>	V
Clamped Energy at the Switching OFF (See Figure 9)	W <sub>OFF</sub>	50			mJ for 1ms
On Resistance (I <sub>OUT</sub> = 2A, T <sub>J</sub> = 150°C, NON = LOW)	R <sub>DSON</sub>			500	mΩ
Output Low Voltage Limitation (I <sub>OUT</sub> = 150mA)	V <sub>OUTLIM</sub>	65		220	mV
Output Capacitance (Guaranteed by design)	C <sub>OUT</sub>			350	pF
OUTPUTS REVERSE DIODE		•		1	•
Reverse Output Current	I <sub>RD</sub>	2,5			А
Reverse Peak current (1)	I <sub>RDP</sub>	5.0			А
Reverse Voltage Drop					
- I <sub>OUT</sub> = - 5A	V <sub>RD1</sub>	1.0		1.7	V
- I <sub>OUT</sub> = - 2,5A	$V_{RD2}$	0.85		1.7	V
POWERSTAGE PROTECTION					
Short Current Limit	I <sub>SCB</sub>	3.0		5	Α
V <sub>CC</sub> Undervoltage	V <sub>CCMIN</sub>	3.35		3.95	V
DIAGNOSTIC		•		1	•
Short to GND Threshold Voltage for $I_{OUT} \le 2A$	$V_{REF}$	0.390xV <sub>CC</sub>		0.435xV <sub>CC</sub>	V
Open Load Threshold Current	I <sub>OL</sub>	10		50	mA
Pull-up Resistor	R <sub>OL</sub>	2.0		8.0	kΩ
Temperature Detection Threshold	T <sub>OFF</sub>	155		185	°C

## Notes

1. For  $t \le 2ms$ . Max. reverse current is limited to - 10A (for all outputs together)

# **DYNAMIC CHARACTERISTIC**

**Table 4. Dynamic Electrical Characteristics** 

Characteristics noted under conditions 7.0 V  $\leq$  V<sub>SUP</sub>  $\leq$  18 V, -40°C  $\leq$  T<sub>A</sub>  $\leq$  125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T<sub>A</sub> = 25°C under nominal conditions unless otherwise noted.

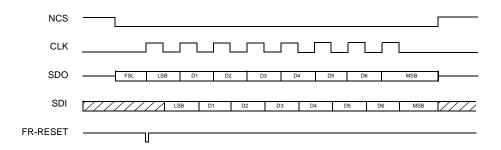
Characteristic	Symbol	Min	Тур	Max	Unit
NPUTS	l .		ı		l
Input Frequency (NON1 to NON4)	f <sub>IN</sub>	0.0		1000	Hz
OUTPUTS TIMING	l .		ı		l
Positive Output Voltage Ramp (with inductive load)					
V <sub>OUT</sub> = 4V 16V	OVR <sub>P1</sub>	2.0	3.0	5.0	V/μs
V <sub>OUT</sub> = 16V Vclp	OVR <sub>P2</sub>	3.5	6.0	10	V/μs
Negative Output Voltage Ramp (25% 75%)	OVR <sub>N</sub>	1.75	3.0	4.0	V/μs
Internal Switch-on-Time Charge Pump	t <sub>DCP</sub>			40	μS
$(NON = LOW V_{GATE} = 0.9 * V_{BAT})$					
Turn ON Delay	t <sub>DON</sub>	1.0	2.5	5.0	μS
$(NON = 50\%, V_{OUT} = 0.9 * V_{BAT})$					
Turn OFF Delay					
$(NON = 50\%, V_{OUT} = 0.1 * V_{BAT})$	t <sub>DOFFA</sub>		1.0	3.0	μS
$(NON = 50\%, V_{OUT} = 4V)$	tDOFFB		4.7	7.5	μS
Undervoltage Protection	t <sub>RPON</sub>			100	μS
Max ON time after a output voltage ramp from 0V to 25V at $V_{CC} = 0VV_{CCPRO}$					
Matching Turn ON Delay	t <sub>MON</sub>	- 3.0		3.0	μS
$(NON = 50\%, V_{OUT} = 0.9 * V_{BAT})$					
Rise time Turn OFF	t <sub>ROFF</sub>		8.5	12	μS
(10% - 90% of V <sub>CLP</sub> )					
DIAGNOSTIC					
Short to GND Filter Time	T <sub>SCG</sub>	140		250	μS
Open Load Filter Time	t <sub>OL</sub>	140		250	μS
SERIAL DIAGNOSTIC LINK : LOAD CAPACITOR AT SDI AND SDO = 1	00PF			•	ı
Clock Frequency (50% duty cycle)	f <sub>CLK</sub>	3.0			MHz
Minimum Time CLK = HIGH	t <sub>CLH</sub>	100			ns
Minimum Time CLK = LOW	t <sub>CLL</sub>	100			ns
Propagation Delay (CLF Data at SDO valid)	t <sub>PCLD</sub>			100	ns
NCS = LOW to Data at SDO Valid	t <sub>PCLD</sub>			100	ns
CLK Low Before NCS Low	t <sub>SCLCH</sub>	100			ns
(Setup time CLK to NCS change High/Low)					
CLK Change Low/High after NCS = Low	t <sub>HCLCL</sub>	100			ns
SDI Input Set up Time	t <sub>SCLD</sub>	20			ns
(CLK change High/Low after SDI data valid)					
SDI Input Hold Time (SDI data hold after CLK change High/Low)	t <sub>HCLD</sub>			20	ns
		<b>-</b>	t	l	1

# Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V  $\leq$  V<sub>SUP</sub>  $\leq$  18 V, -40°C  $\leq$  T<sub>A</sub>  $\leq$  125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T<sub>A</sub> = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
CLK High After NCS High	t <sub>HCLCH</sub>	150			ns
NCSLow/High to Output Data Flout	t <sub>PCHDZ</sub>			100	ns
Capacitance at SDI, SDO, CLk, CS	t <sub>PCLD</sub>			10	pF
NCS Filter time (Pulses $\leq$ t <sub>FNCS</sub> will be ignored)	t <sub>FNCS</sub>	10		40	ns

# **TIMING DIAGRAMS**



NOTE: FR -RESET means Reset failure storage (internal signal)

Figure 4. Timing Diagram to Read the Diagnostic Register

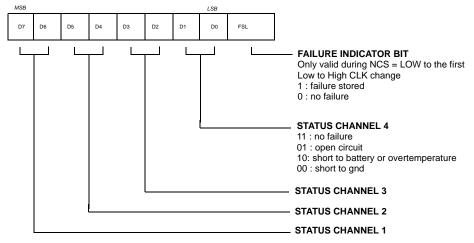


Figure 5. Diagnostic Failure Register Structure

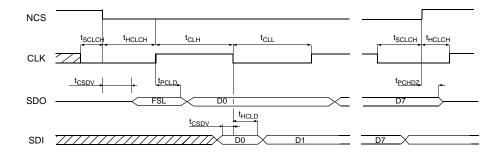


Figure 6. Serial Interface Timing

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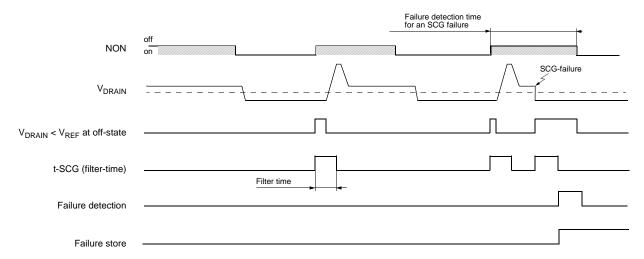


Figure 7. Diagram to Short-Circuit to GND Failure (SCG-Failure) Detection

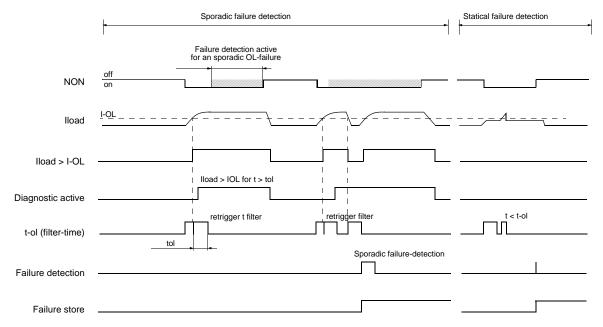


Figure 8. Diagram to Open Load Failure (OL-Failure) Detection

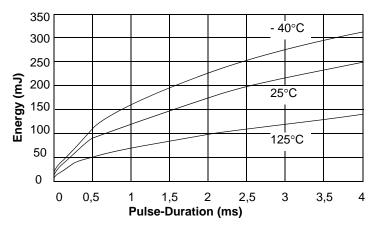


Figure 9. Max Clamp- Energy Specification

# **ELECTRICAL PERFORMANCE CURVES**

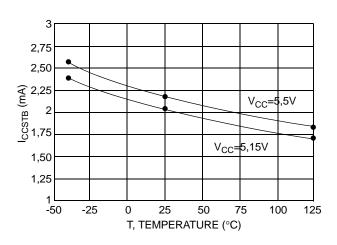


Figure 10. Standby Current versus Temperature

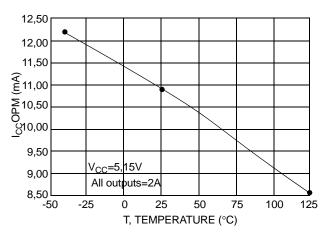


Figure 11. Operating Mode Current versus Temperature

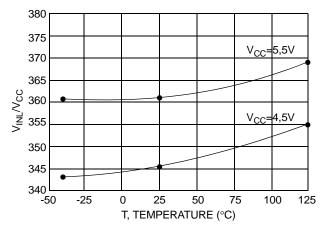


Figure 12. Low Threshold Input Voltage versus Temperature

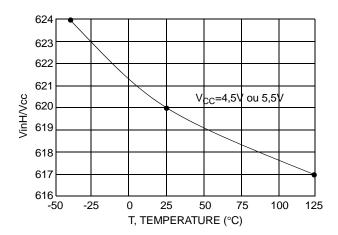


Figure 13. High Threshold Input Voltage versus Temperature

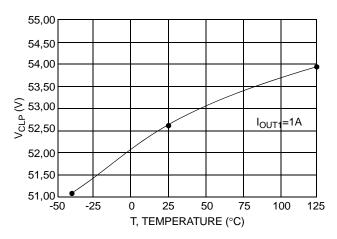


Figure 14. Output Clamp Voltage versus Temperature

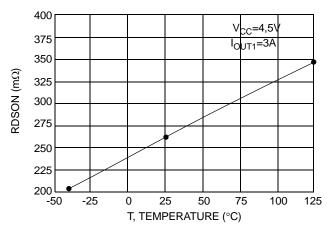


Figure 15. Rdson versus Temperature

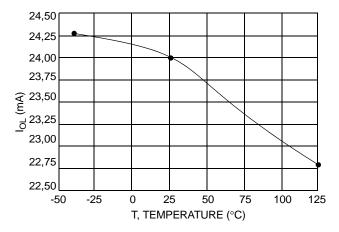


Figure 16. Open Load versus Temperature

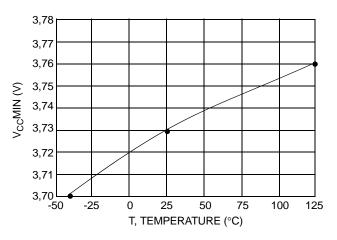


Figure 17. Vcc Undervoltage versus Temperature

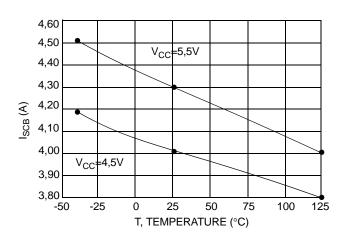


Figure 18. Short Current Limit versus Temperature

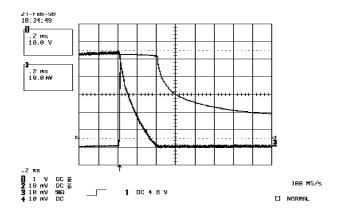
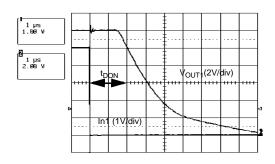


Figure 19. Inductive Switching



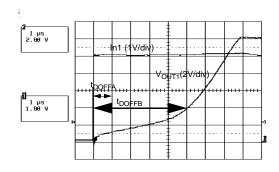


Figure 20. Turn on Delay

4S/s

Figure 21. Turn off Delay

# FUNCTIONAL DESCRIPTION

## INTRODUCTION

The device is a Quad Low-side Driver driven by four CMOS input stages. Each output power transistor is protected against short to  $V_{BAT}$  by a zener clamp against overvoltage.

A diagnostic logic recognizes four failure types at the output stage: overcurrent, short to GND, open-load and overtemperature.

The failures are individually stored in a byte which can be read out via the serial interface (SPI).

## **OUTPUT STAGE CONTROL**

Each of the four output stages is switched ON and OFF by an individual control line (NON-Input). The logic level of the control line is CMOS compatible. The output transistors are switched off when the inputs are not connected.

### **POWER TRANSISTORS**

Each of the four output stages has its own zener clamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. The drain voltage ramp occurring when output is switched on or off, is within defined limits. Output transistors can be connected in parallel to increase current capability. In this case, the associated inputs should be connected together.

# SHORT-CIRCUIT AND OVERTEMPERATURE PROTECTION

If the output current increases above the short current limit for a time longer than  $t_{SCB}$  or if the temperature increases above  $T_{OFF}$  then the power transistor is immediately switched off. It remains switched off until the control signal on the NON-Input is switched off and on again.

## **DIAGNOSTICS**

The following failures at the output stage are recognized : Short -Circuit to  $V_{BAT}$  or overtemp = SCB (Highest priority) Short -Circuit to GND..... = SCG Open Load..... = OL (Lowest priority)

The SCB failure is recognized by an overcurrent (current above the short current limit) or an overtemperature.

If the current through the output stage is lower than the IOL-reference, after a filter time an OL failure will be recognized. This measurement is active while the power stage is switched on.

The SCG failure will recognize when the drain voltage is lower than the OL reference limit, while the output stage is switched off. All four outputs have an independent overtemperature detection and shutdown. All failures are stored in individual registers.

They can be read by the microprocessor via the serial interface. There is no failure detected if the power stage control time is shorter than the filter time.

## **DIAGNOSTIC INTERFACE**

The communication between the microprocessor and the failure register runs via the SPI link. If there is a failure stored in the failure register, the first bit of the shift register is set to a high level. With the High/Low change on the NCS pin, the first bit of the diagnostic shift register will be transmitted to the SDO output. The SDO output is the serial output from the diagnostic shift register and it is put into a tri-state when the NCS pin is high. The CLK pin clocks the diagnostic shift register. New SDO data will appear on every rising edge of this pin and new SDI data will be latched on every CLK's falling edge into the shift register. With the first positive pulse of the CLK, the failure register will be cleared. There is no bus collision at a small spike at the NCS. The CLK is always LOW while the NCS-signal is changing.

### RESET

There are two different reset functions realized:

Under voltage reset : as long as the  $V_{CC}$  voltage is lower than  $V_{CCRES}$ , the power stages are switched off and the failure-registers are reset.

Reset pin : as long as the NRES-pin is low, following circuits are reset :

- Power stages
- · Failure register

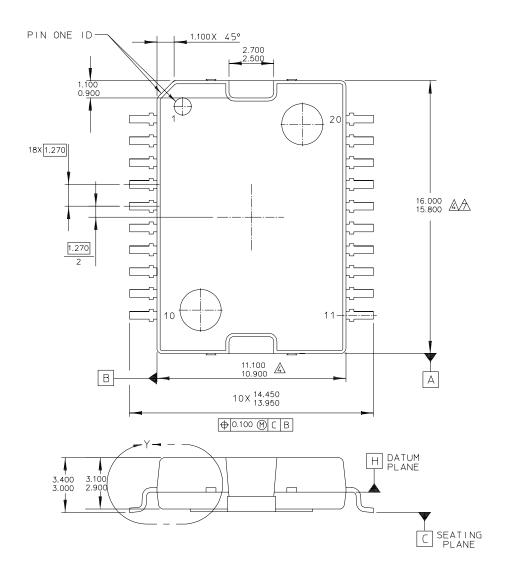
# **UNDERVOLTAGE PROTECTION**

At low  $V_{CC}$  voltage, the device remains switched off even if there is a voltage ramp at the OUT pin.

# **PACKAGING**

# **PACKAGE DIMENSIONS**

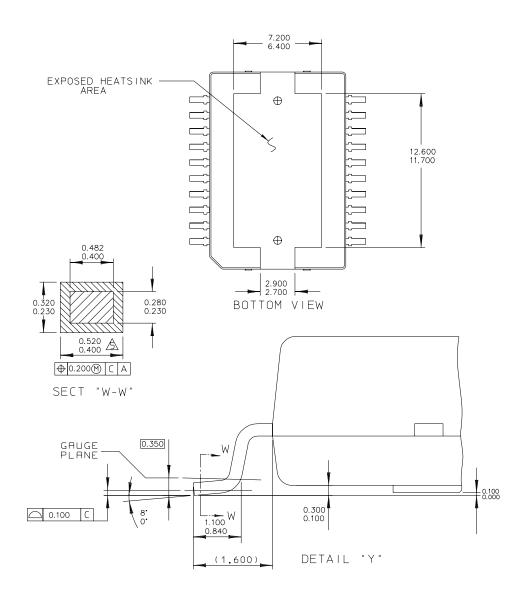
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20 LEAD HSOP W/PROTRUDING HEATSINK		CASE NUMBER	979	11 OCT 2005
		STANDARD: NO	IN-JEDEC	

DH SUFFIX VW (PB-FREE) SUFFIX 20-PIN HSOP PLASTIC PACKAGE 98ASH70702A ISSUE B

# **PACKAGE DIMENSIONS (CONTINUED)**



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		STANDARD: NE	IN-JEDEC	

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# **REVISION HISTORY**

REVISION	DATE	DESCRIPTION OF CHANGES
6.0	11/2006	<ul> <li>Implemented Revision History page</li> <li>Added Pb-Free suffix code VW</li> <li>Converted to Freescale format, and adjusted to the prevailing form and style</li> </ul>

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