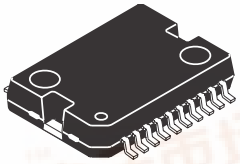
Freescale Semiconductor
Technical Data

Document order number: MC33486A
Rev 2.0, 12/2005

Dual High-Side Switch for H-Bridge Applications

33486A

DUAL HIGH-SIDE SWITCH



DH SUFFIX
98ASH70702A
20-TERMINAL HSOP

This 33486A is a self-protected dual 15 mΩ high-side switch that incorporates a dual low-side switch control and protection features. This device is used to replace electromechanical relays and discrete devices in power management applications. It is designed for typical DC-motor control in an H-Bridge configuration.

The 33486A can directly interface with a microcontroller for control and diagnostic functions. It is PWM-capable and has a self-adjusting switching speed for minimizing electromagnetic emission.

Features

- Dual 15 mΩ High-Side Switch with Dual Low-Side Control
- 10 A Nominal DC Current
- 8.0 V to 28 V Operating Voltage with Standby Current < 10 µA
- High-Side Overtemperature Protection
- High-Side and Low-Side Overcurrent Protection
- Current Recopy to Monitor High-Side Current
- PWM Capability up to 30 kHz
- Common Diagnostic Output
- Overvoltage and Undervoltage Detection
- Cross-Conduction Management

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33486ADH/R2	-40°C to 125°C	20 HSOP

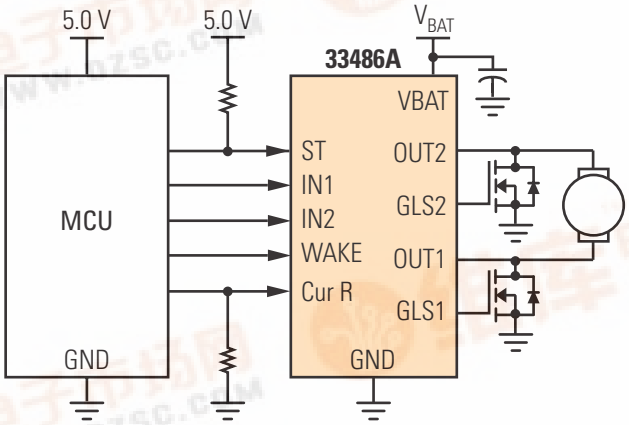


Figure 1. 33486A Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

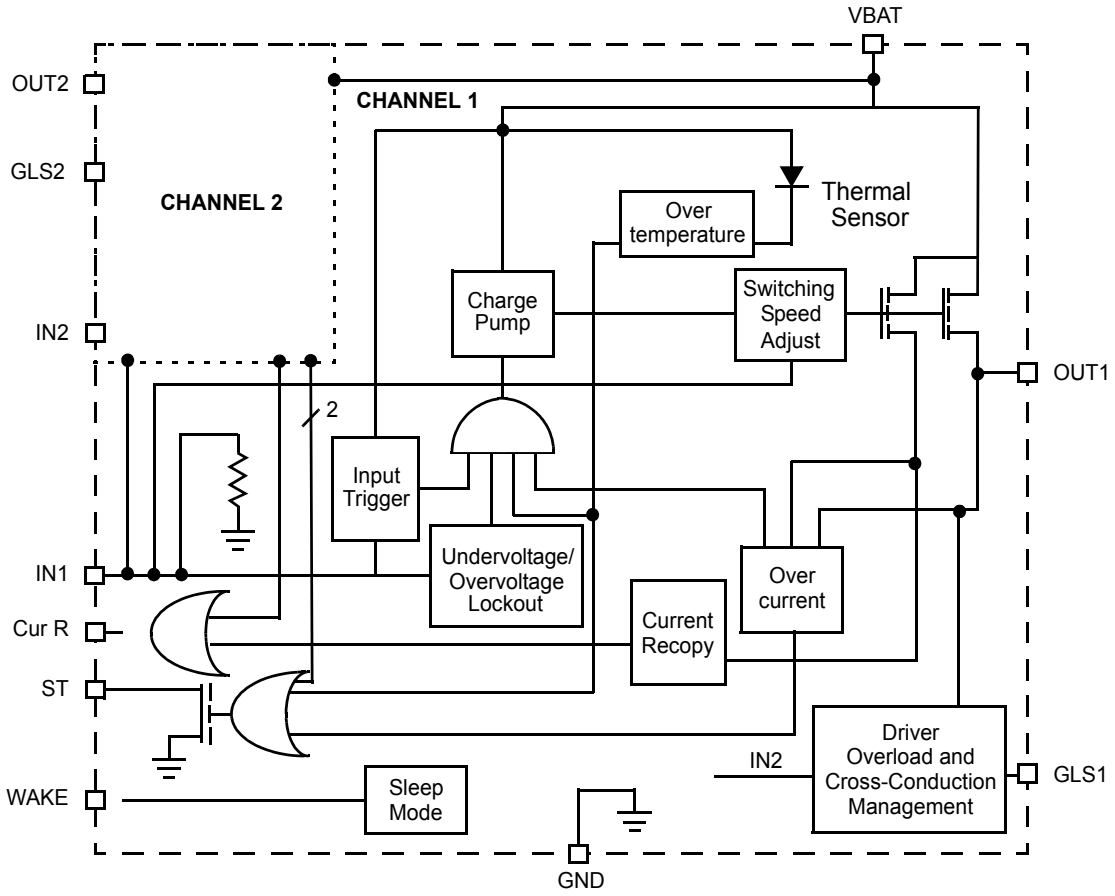

Figure 2. 33486A Simplified Internal Block Diagram

TERMINAL CONNECTIONS

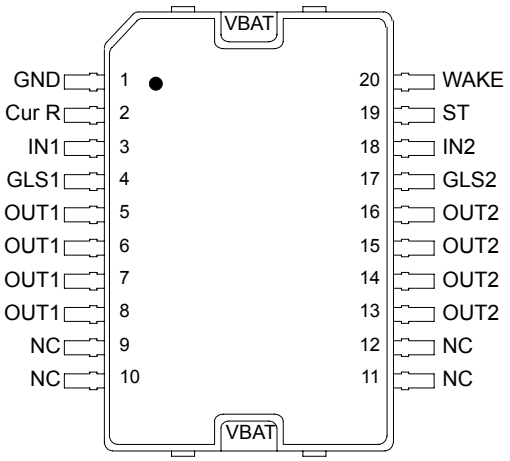

Figure 3. 33486A Terminal Locations

Table 1. TERMINAL DEFINITIONS

Terminal	Terminal Name	Formal Name	Definition
1	GND	Ground	This is the ground terminal of the device.
2	Cur R	Load Current Sense	The Current Sense terminal delivers a ratio amount of the sum of the high-side currents.
3 18	IN1 IN2	Input Channel 1 Input Channel 2	These are the device input terminals that directly control their associated outputs. Each input terminal has an internal active pull-down so that the input terminal will not float if disconnected.
4 17	GLS1 GLS2	Gate Low-Side 1 Gate Low-Side 2	Each terminal must be connected to one gate of an external low-side MOSFET.
5–8	OUT1	Output Channel 1	Terminals 5, 6, 7, and 8 are the source of the Output Channel 1 15 mΩ high-side MOSFET1.
9–12	NC	No Connect	These terminals are not used.
13–16	OUT2	Output Channel 2	Terminals 13, 14, 15, and 16 are the source of the Output Channel 2 15 mΩ high-side MOSFET2.
19	ST	Status for Both Channels	The status output goes low when a fault mode is detected. It is an open drain with an internal clamp at 6.0 V. An external pull-up resistor connected to V_{DD} (5.0 V) is needed.
20	WAKE	Wake	This logic input enables control of the device. (Wake logic LOW = Sleep Mode, Wake logic HIGH = full operation.) The WAKE terminal has a pull-down resistor.
TAB	VBAT	Supply Voltage	The backside TAB is connected to the power supply of the 33486A.

MAXIMUM RATINGS

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Power Supply Voltage: Continuous/Pulse	V_{BAT}	-0.3 to 40	V
OUT1, OUT2 to V_{BAT} Voltage: Continuous/Pulse	V_{OUT}	-0.3 to 40	V
IN1, IN2, WAKE, ST Input DC Voltage: Continuous/Pulse	V_{IN}	-0.3 to 7.0	V
IN1, IN2, WAKE Input Current	I_{IN}	±5.0	mA
Output DC Output Current, 1 Channel ON, T_A = 85°C (1)	I_{OUTDC}	10	A
Output Current: Pulse (2)	I_{OUTP}	Self-Limited	A
Operating Junction Temperature	T_J	-40 to 150	°C
Operating Ambient Temperature	T_A	-40 to 125	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Thermal Resistance Junction to Case Junction to Ambient (1)	 $R_{\theta JC}$ $R_{\theta JA}$	 2.0 25	°C/W
Power Dissipation at T_{CASE} 140°C (3)	P_D	5.0	W
ESD All Terminals Human Body Model (4) Machine Mode (5)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Terminal Soldering Temperature (6)	T_{SOLDER}	240	°C

Notes

1. Device mounted on dual-side printed circuit board with 70 μm copper thickness and 10 cm^2 copper heatsink (2.5 cm^2 on top side and 7.5 cm^2 on down side).
2. See high-side output current shutdown, I_{LIM}.
3. Assuming a 150°C maximum junction temperature.
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}= 100 pF, R_{ZAP}= 1500 Ω).
5. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}= 200 pF, R_{ZAP}= 0 Ω).
6. The maximum peak temperature during the soldering process should not exceed 235°C (+5.0°C/-0°C). The time within 5.0°C of actual peak temperature should range from 10 s to 30 s max.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 9.0 V ≤ V_{BAT} ≤ 16 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_J = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY					
Nominal Operating Voltage	V_{BAT}	V_{UV}	–	V_{OV}	V
Standby Current V_{BAT} < 13.5 V, WAKE = 0 V, IN1 = IN2 = 0 V	I_{STDBY}	– –	– –	 10	μA
Supply Current in Operation Mode No PWM, IN1 or IN2 = 5.0 V, WAKE = 5.0 V	I_{ON}	– –	 9.0	 15	mA
Supply Current in Operation Mode PWM = 20 kHz, d = 50% Without Load	I_{ONPWM}	– –	 15	 –	mA
OUTPUTS					
High-Side Drain to Source On Resistance I_{OUT} = 5.0 A, V_{BAT} > 10 V, T_J = 25°C I_{OUT} = 5.0 A, V_{BAT} > 10 V, T_J = 150°C	$R_{DS(ON)}$	 – –	 12 21	 15 30	mΩ
High-Side Body Diode Voltage (OUTn to V_{BAT}) I_{OUT} = -5.0 A, T_J = 150°C	V_{BD}	– –	– –	 0.7	V
Low-Side Gate Output Voltage Internally Clamped	V_{GS}	– –	– –	 14	V
IN1, IN2, WAKE					
Input Low Levels	V_{IL}	–	–	1.5	V
Input High Levels	V_{IH}	3.5	–	–	V
Input Hysteresis IN1 and IN2 Terminals Only	V_{HYST}	 0.2	 0.6	 1.0	V
Logic Input Current V_{IN} = 1.5 V V_{IN} = 3.5 V	I_{IN}	 1.0 –	 – –	 – 50	μA
STATUS					
Status Voltage I_{ST} = 1.0 mA, Output in Fault	V_{ST}	– –	– –	 0.5	V
Status Leakage V_{ST} = 5.0 V	I_{STLK}	– –	– –	 10	μA

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 9.0 V ≤ V_{BAT} ≤ 16 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_J = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OVERLOAD PROTECTION					
High-Side Output Current Shutdown	I_{LIM}	20	35	50	A
Low-Side Over Load Detection (V_{OUT}-GND)	$V_{OUT-FAULT}$	1.0	–	1.6	V
Thermal Shutdown	T_{SHUT}	150	175	190	°C
Thermal Shutdown Hysteresis	T_{HYST}	–	10	–	°C
Undervoltage Shutdown Threshold	V_{UV}	6.0	7.0	8.0	V
Undervoltage Shutdown Hysteresis	V_{UYST}	–	0.15	–	V
Overvoltage Shutdown Threshold	V_{OV}	27	29	31	V
Overvoltage Shutdown Hysteresis	$V_{OV-HYST}$	–	0.15	–	V
CURRENT RECOPY					
Current Recopy Ratio	C_R				–
I_{OUT} from 4.0 A to 8.0 A, T_J = -40°C to 105°C		3145	3700	4255	
I_{OUT} from 2.0 A to 4.0 A, T_J = -40°C to 105°C		2960	3700	4440	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 9.0 V ≤ V_{BAT} ≤ 16 V, -40°C ≤ T_J ≤ 150°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_J = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OVERLOAD PROTECTION					
High-Side Overcurrent Shutdown Delay (7)	t_{ILIM}	–	3.0	20	µs
Low-Side Over Load Detection (V_{OUT}-GND) Shutdown Delay (8)	$t_{OUT-FAULT}$	–	3.0	10	µs
OUTPUT TIMING					
High-/Low-Speed Mode to Low-/High-Speed Mode Transition Pulse Width	t_{SMOD}	150	250	350	µs
Gate Low-Side Rise Time in High Speed Mode From 10% to 90% V_{OUT}, Load = 3.3 nF and 10 Ω	t_{PSRLS}	–	3.6	–	µs
Gate Low-Side Fall Time in High Speed Mode From 90% to 10% V_{OUT}, Load = 3.3 nF and 10 Ω	t_{NSRLS}	–	0.25	–	µs
HIGH-SPEED MODE					
High-Side Positive Slew Rate From 10% to 65% V_{OUT}, Load = 3.0 Ω	t_{HR}	–	10	–	V/µs
High-Side Negative Slew Rate From 90% to 35% V_{OUT}, Load = 3.0 Ω	t_{HF}	–	40	–	V/µs
High-Side Turn-On Delay Time To 10% V_{OUT}, Load = 3.0 Ω	t_{HDON}	–	2.5	–	µs
High-Side Turn-Off Delay Time To 90% V_{OUT}, Load = 3.0 Ω	t_{HDOFF}	–	1.5	–	µs
LOW-SPEED MODE					
High-Side Maximum Output Positive Slew Rate From 10% to 65% V_{OUT}, Load = 3.0 Ω	t_{LR}	–	1.0	–	V/µs
High-Side Maximum Output Negative Slew Rate From 90% to 35% V_{OUT}, Load = 3.0 Ω	t_{LF}	–	0.5	–	V/µs
High-Side Turn On Delay TIme To 10% V_{OUT}, Load = 3.0 Ω	t_{LDON}	–	10	–	µs
High-Side Turn Off Delay Time To 90% V_{OUT}, Load = 3.0 Ω	t_{LOFF}	–	80	–	µs

Notes

7. Time between fault occurrence and output shutdown.
8. Time between fault occurrence and gate low-side (GLS) shutdown.

TIMING DIAGRAMS

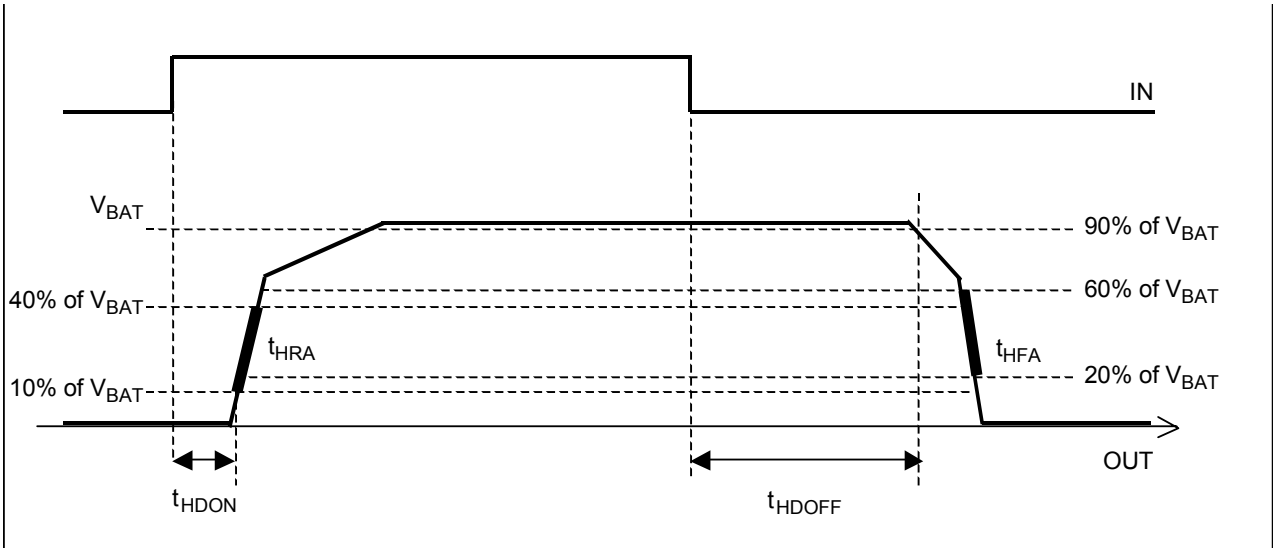

Figure 4. Outputs Slew Rate and Timing Delay

FUNCTIONAL DESCRIPTION

INTRODUCTION

The full bridge is partitioned into three blocks, the 33486A and two low-side MOSFETS. Each block has a dedicated package.

The 33486A incorporates two 15 mΩ N-channel high-side power MOSFETS and two low-side gate drivers. The outputs are fully protected against shorts to ground, shorts to V_{BAT}, shorted loads, overvoltage/undervoltage, and overtemperature. The device can directly interface with a microcontroller for control and diagnostic functions.

The 33486A is designed for typical DC-motor control in an H-Bridge configuration.

FUNCTIONAL TERMINAL DESCRIPTION

SUPPLY VOLTAGE (V_{BAT})

The backside of the 33486A, called the tab, is the power supply of the device. It has undervoltage and overvoltage detection. In addition to its supply function, the tab contributes to the thermal behavior of the device by conducting the heat from the switching MOSFET to the printed circuit board.

INPUTS (IN1 AND IN2)

IN1 and IN2 terminals are input control terminals used to control the outputs (OUT1 and OUT2) and the gates of the low-side power MOSFETs (GLS1 and GLS2). When the input is a logic LOW, the associated output is low (high-side internal MOSFETs OFF and low-side external MOSFETs ON). (Refer to Table 5, TRUTH TABLE, page 21, for more information.) These terminals are 5.0 V CMOS-compatible inputs.

OUTPUTS (OUT1 AND OUT2)

OUT1 and OUT2 terminals are the sources of the internal high-side MOSFETs. OUT1 and OUT2 are controlled using the IN1 and IN2 inputs, respectively. These outputs are current limited and thermally protected.

GATE LOW SIDE (GLS1 AND GLS2)

GLS1 and GLS2 terminals are the gates of the external low-side MOSFETs. These MOSFETs are controlled using IN1 and IN2 inputs. When the input (INn) is logic HIGH, the associated GLS is grounded to turn off the external low-side MOSFET. (Refer to Table 5, TRUTH TABLE for more information.)

WAKE

The WAKE terminal is used to place the device in a sleep mode. When WAKE terminal voltage is a logic LOW state, the device is in sleep mode and its bias current is at a minimum. The device is enabled and fully operational when WAKE terminal voltage is logic HIGH.

STATUS (ST)

The status terminal indicates when the device is in fault mode. It reports overtemperature and/or overcurrent faults. It goes active low when a fault mode is detected by the device on either one channel or both simultaneously. Its internal structure is an open-drain architecture with an internal clamp at 6.0 V. An external 10 kΩ pull-up resistor connected to V_{DD} (5.0 V) is needed. Refer to Table 5, TRUTH TABLE.

CURRENT SENSE (CUR R)

The Current Sense terminal delivers a ratio amount (1/3700) of the sum of the high-side currents that can be used to generate signal ground-referenced output voltages for use by the microcontroller with a 1.0 kΩ pull-down resistor.

GROUND (GND)

This terminal is the ground of the device.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

Power Supply

The 33486A can be directly connected to the power supply line. The device has a standby mode (Wake at low logic level) with a ultra-low consumption (10 μA max). In operation when inputs are active, the supply current is up to 20 mA.

With the high current and fast switching ability of the 33486A, it is recommended that sufficient capacitance (tens of microfarads) be placed between VBAT and GND of the IC. This will help ensure that the power supply stays within the specified limits.

The internal charge pump is activated when Wake is at high logic level. It is self-oscillating with a frequency that can

vary typically from 1.0 MHz to 7.0 MHz. It starts operating at low frequency.

Reverse Battery Protection

During reverse battery the current flows in the body diodes of the power MOSFETs, which are forward biased. Figure 5 shows the specific protection that must be implemented.

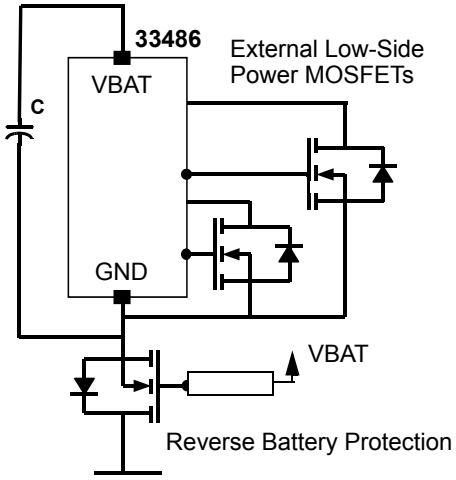

Figure 5. Reverse Battery Protection Schematic

A reverse battery component might be needed in the GND or in the VBAT terminal of the application (i.e., diode or MOSFET) in order to achieve both reverse battery and negative transient pulses immunity. If a polarized capacitor is used, it can be placed as shown in in Figure 5.

Loss of Ground Protection

As Figure 5 shows, a loss of ground will not damage the 33486A because the ground terminal of the device is the same as the ground of the low side.

Overvoltage/Undervoltage Protection

If the battery voltage falls below 7.0 V typical, the outputs are turned low (low-side MOSFETs ON) in a low-speed mode. The 33486A goes back into normal operation mode as soon as V_{BAT} rises above the undervoltage threshold. The undervoltage protection circuitry has hysteresis.

The control circuitry also has an overvoltage detection that turns the external low-side MOSFETs ON and protects the load in case V_{BAT} exceeds 29 V typical. The gate drivers will also be clamped to 14 V to protect the external low-side MOSFETs. The low-side MOSFETs remain in the ON state until the overvoltage condition is removed.

Undervoltage and overvoltage are not reported on the status output.

Self-Adjusting Switching Speed Mode

This feature allows for reduction in EMC and power dissipation depending on the application. The 33486A has two switching speeds (high and low) depending on the input pulse width. The high-speed condition is active when the delay between two consecutive input edges is below 250 μs typical. The low-speed mode is active when the delay between two consecutive input edges is above 250 μs typical. The 250 μs delay corresponds about to a 2.0 kHz frequency with a duty cycle of 50%.

Current Recopy

This feature provides a current mirror with the ratio of 1/3700 of the sum of the high-side output current. An external resistor must be connected to the Cur R terminal, then tied to a microcontroller A/D input for analog voltage measurement (see Figure 6). This current recopy uses the well-known Wheatstone bridge principle with the Sense, the Power, and the load as the three known resistances.

Owing to the internal zener clamp in the gate of the M1 transistor, the Cur R max voltage is typically 11 V.

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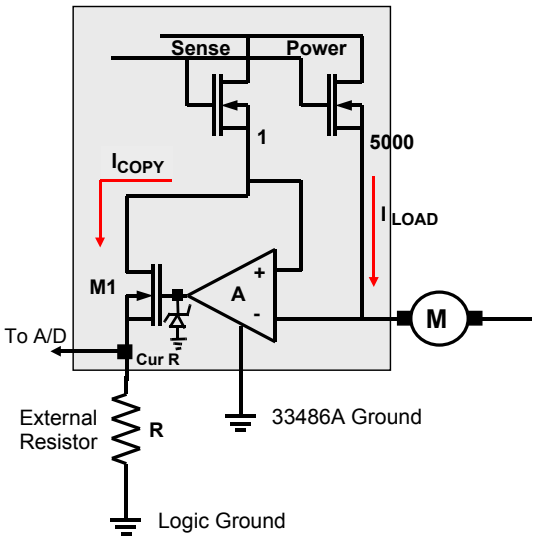


Figure 6. Current Recopy Principle

In case a ground shift occurs between the MCU and the 33486A, the amplifier A (Figure 6, page 10) will adapt its output to keep the same I_{COPY}. Of course the shift has to keep between ±1.0 V.

Overtemperature Protection

The 33486A incorporates overtemperature protection. Overtemperature detection occurs when an internal high-side MOSFET is in the ON state. When an overtemperature condition occurs, both outputs are affected. Both high-side MOSFETs are turned OFF to protect the 33486A from

damage (low-side MOSFETs ON). The overtemperature protection circuitry incorporates hysteresis.

Overtemperature fault condition is reported on the status output.

High-Side Overcurrent Protection

The 33486A incorporates a current shutdown threshold of 35 A typical. When this limit is reached due to an overload condition or a short to ground, the faulty output is tri-stated. To clear the fault, the input (INn) line needs to return low, then on the next high transition the output will be enabled.

This information is reported on the status output.

Low-Side Block

The low-side block has control circuitry for two external N-channel power MOSFETs. The low-side control circuitry is PWM capable and protects the low-side MOSFETs in case of overcurrent (short to V_{BAT}). This information is reported on the status output.

The low-side gate controls are clamped at 14 V maximum to protect the gates of the low-side MOSFETs. Figures 13, page 15, and 14, page 15, depict the characteristics of the low-side block when a current is sourced from the GLS pin or sinked from the GLS pin, respectively.

During normal operation, the outputs OUT1 and OUT2 are driven by the high side. The low-side gate driver will only turn on when the voltage (same connection as OUT1 or OUT2) of the internal high sides is less than 2.0 V, which prevents any cross-conduction in the bridge.

Low-Side Overcurrent Protection

Unlike the high-side overcurrent circuitry, this overcurrent protection does not measure the current; rather, it measures the effect of current on the low-side power MOSFETs through a condition: V_{GS} > 4.3 V and V_{DS} > 1.0 V. When this set of conditions occurs for 3.0 μs typical (blanking time), both outputs OUT1 and OUT2 are tri-stated. The full bridge is tri-stated to prevent the motor running in case of short to V_{BAT}. Once the fault is removed, the input INn of the OUTn that experienced the fault must be reset in order to recover normal mode operation.

The 33486A can be used without the external low-side MOSFETs only if the overcurrent protection condition is not reached. If the external low-side power MOSFETs are not used, a 470 pF capacitor in parallel with a 100 kΩ resistor can be connected at the GLSn pin to prevent the activation of the low-side MOSFET overcurrent protection.

As V_{GS} and V_{DS} are measured in respect to the 33486A ground terminal, it is essential that the low-side source is connected to this same ground in order to prevent false overcurrent detection due to ground shifts.

Thermal Management

The high-side block is assembled into a power surface mount package. This package offers high thermal performances and high current capabilities. It offers 10 terminals on each package side and one additional connection, which is the package heat sink (called terminal 21). The heatsink acts as the device power VBAT connection.

The junction-to-case thermal resistance is 2.0°C/W maximum. The junction-to-ambient thermal resistance is dependant on the mounting technology and if an additional heat sink is used. One of the most commonly used mounting technique consists of using the printed circuit board and the copper lines as heatsink.

Figure 7 is an example of printed circuit board layout. It has a total of 10 cm^2 additional copper on two sides (2.5 cm^2 on the top side and 7.5 cm^2 on the down side).

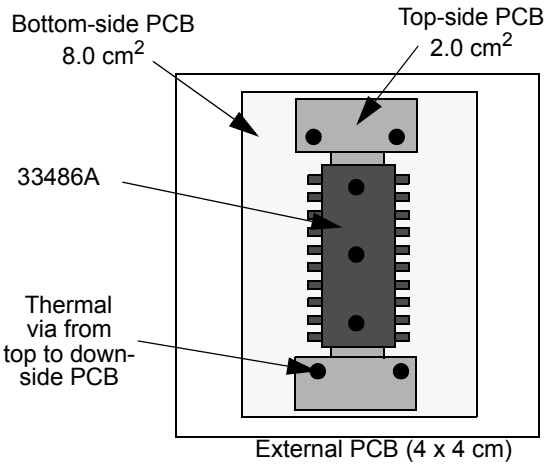


Figure 7. Printed Board Layout Example (not to scale)

With the above layout, thermal resistance junction-to-ambient of 25°C/W can be achieved. This value is split into:

- Junction to case ($R_{\theta JC}$) = 2.0°C/W
- Case to ambient ($R_{\theta CA}$) = 23°C/W

Lower value can be reached with the help of larger and thicker copper metal, higher number of thermal via from top to bottom side PCB, and the use of additional thermal via from the circuit board to the module case.

Thermal Model

The junction-to-ambient thermal resistance of the circuit mounted on a printed circuit board can be spit into two main parts: junction-to-case and case-to-ambient resistances.

Figure 8 shows a simplified steady state model.

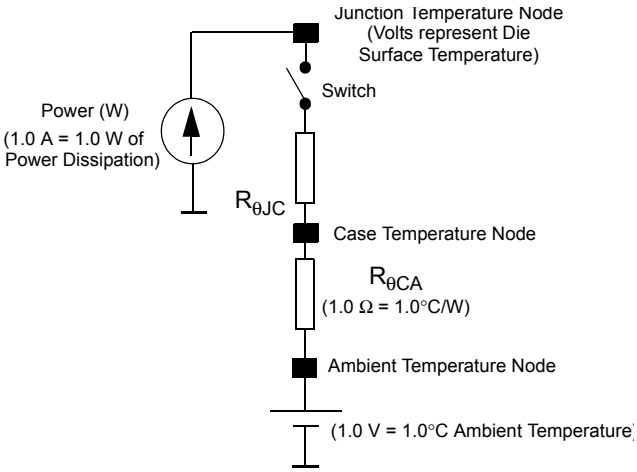


Figure 8. Simplified Thermal Model (Electrical Equivalent)

The use of this model is similar to the electrical Ohm law (voltage = resistance x current), where:

- Voltage represents temperature.
- Current represents power dissipated by the device.
- Resistance represents thermal resistance.

We finally have:

Temperature or delta temperature = power dissipation times thermal resistance; that is, °C = W x °C/W.

Any node temperature can easily be calculated knowing the amount of power flowing through the thermal resistances.

Example

1. Numerical Value
   - Junction-to-case thermal resistance ($R_{\theta JC}$): 2.0°C/W
   - Power into the switch: Assuming the device is driving 8.0 A at 150°C junction temperature ($R_{DS(ON)}$ at 150°C is 40 mΩ), the total power dissipation is 0.04 * 8 * 8 = 2.56 W
   - Case-to-ambient thermal resistance ($R_{\theta CA}$): 20°C/W
2. Results
   - Junction-to-case delta temperature: 5.0°C (2.5 W x 2.0°C/W)
   - Case delta temperature from ambient: 50°C (20°C/W x 2.5 W)
   - Actual junction temperature node will be: 50°C + 5.0°C = 55°C above the ambient temperature.

Assuming an 85°C ambient temperature, the junction temperature is 85°C + 55°C = 140°C.

The above example takes into account the junction-to-ambient thermal resistance, assuming that ambient temperature is 85°C.

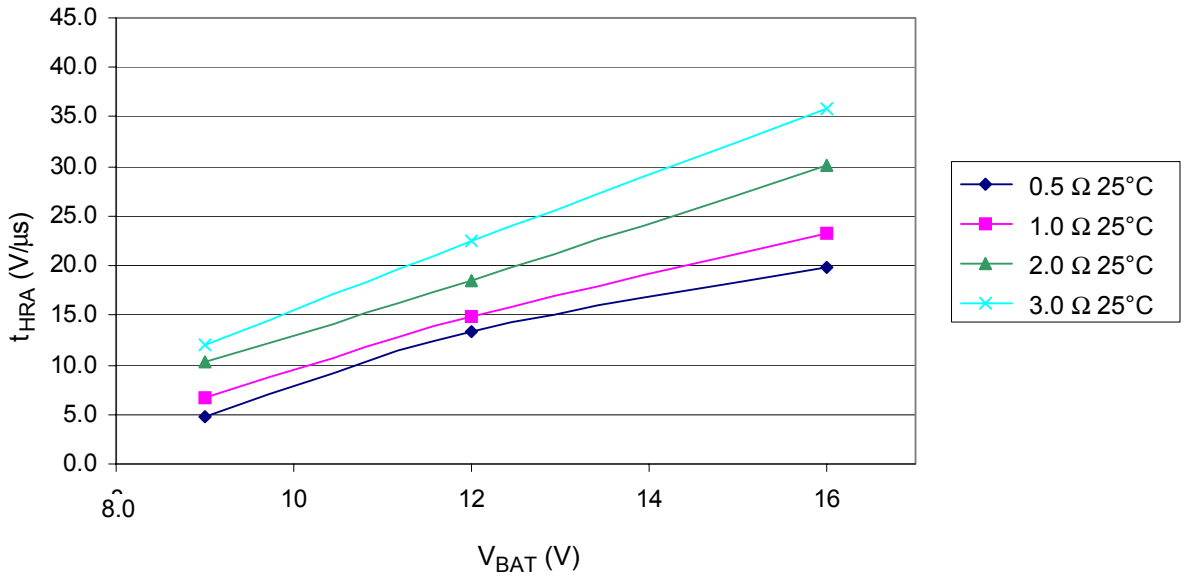
In the case where the device plus its printed circuit board are located inside a module, the ambient temperature of the module should be taken into account. Or an additional thermal resistance from inside module to external ambient temperature must be added. The calculation method remains the same.

The low-side block is packaged into D^2PAK or DPAK package. Junction-to-case thermal resistance is approximately 2/0°C/W. The junction-to-ambient thermal resistance follows the same rules as for the high-side block and is in the same range.

FUNCTIONAL DEVICE OPERATION

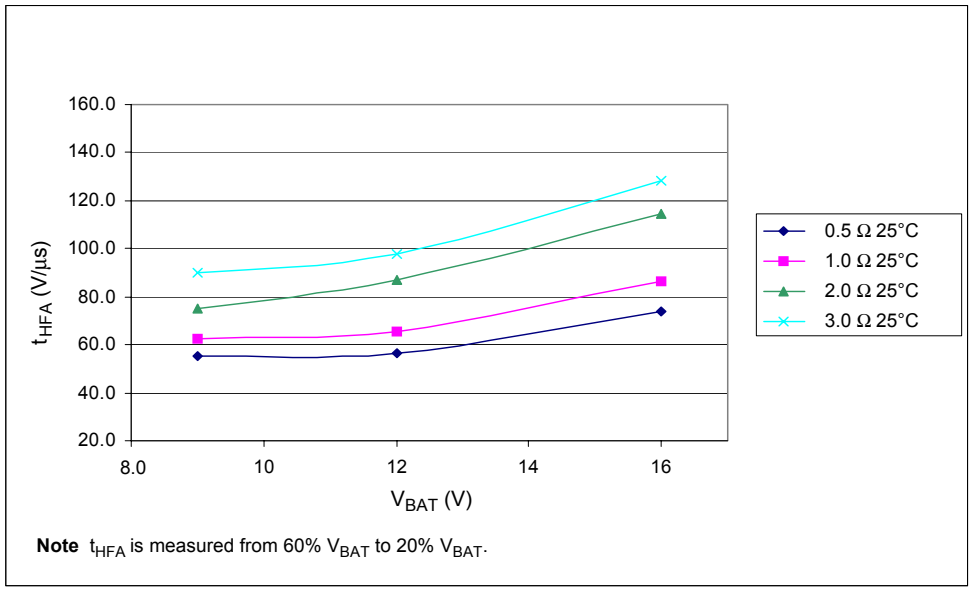
TYPICAL ELECTRICAL CHARACTERISTICS

Note t_{HF} A is measured from 60% V_{BAT} to 20% V_{BAT}.



Note t_{HRA} is measured from 10% V_{BAT} to 40% V_{BAT}.

Figure 9. High-Speed Positive Slew Rate (t_{HRA}) at 25°C for Different Loads



Note t_{HFA} is measured from 60% V_{BAT} to 20% V_{BAT}.

Figure 10. High-Speed Negative Slew Rate (t_{HFA}) at 25°C for Different Loads

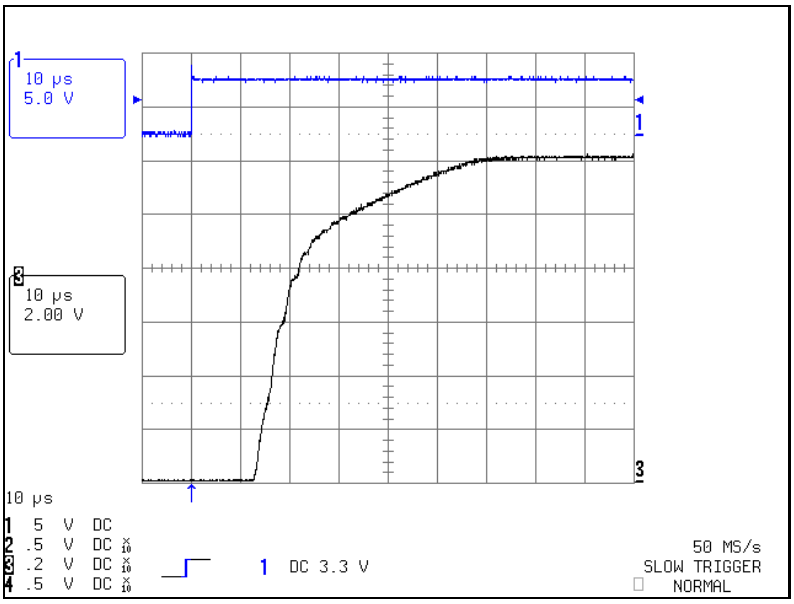


Figure 11. Low-Speed Mode, Oscilloscope Format

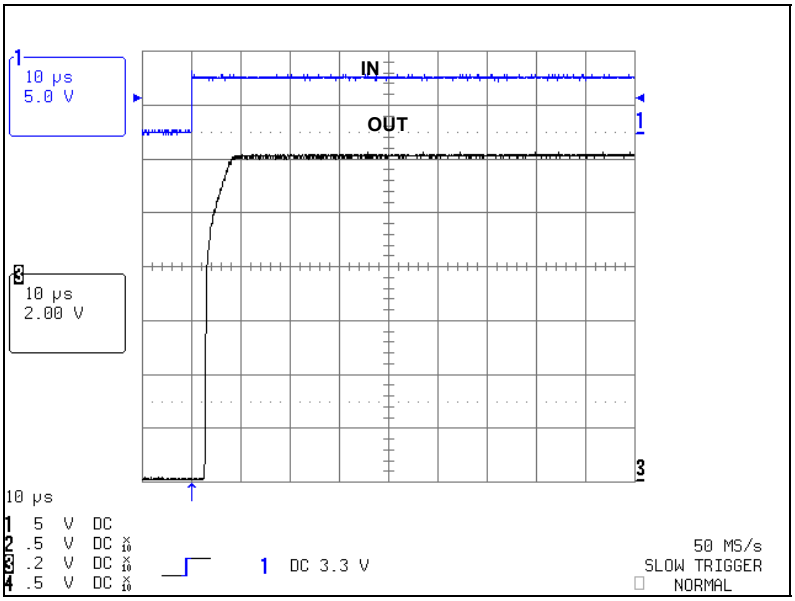


Figure 12. High-Speed Mode, Oscilloscope Format

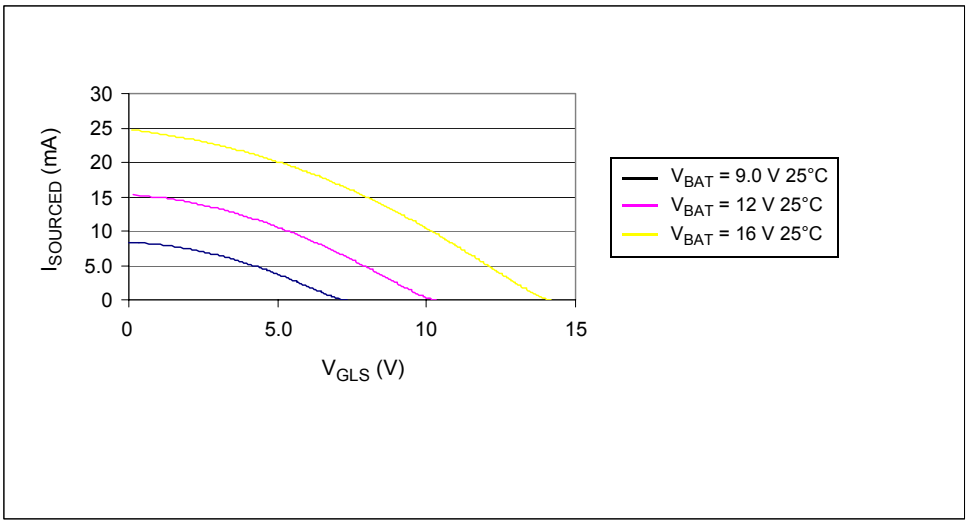


Figure 13. Gate Low-Side (GLS) Sourced Current Capability (High-Speed Mode)

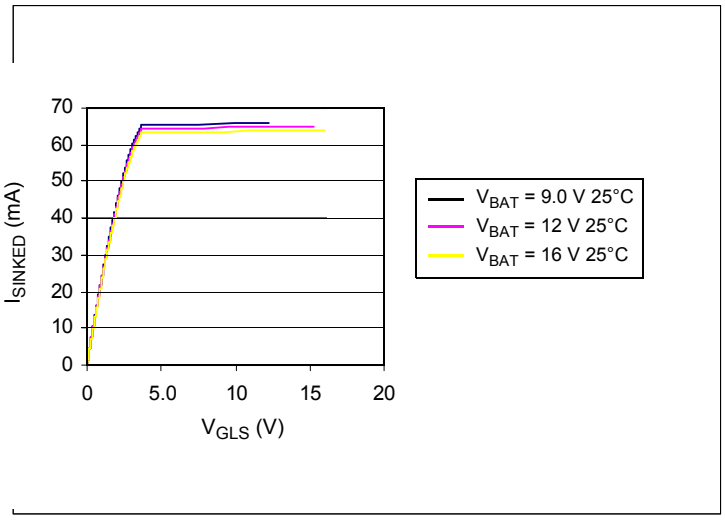
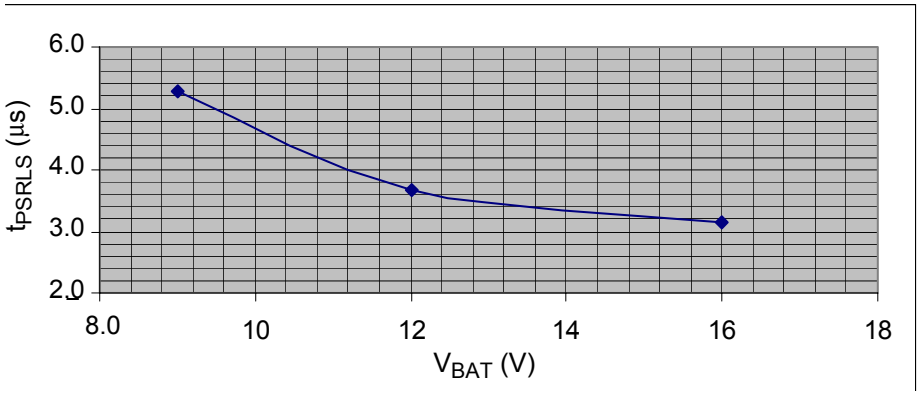
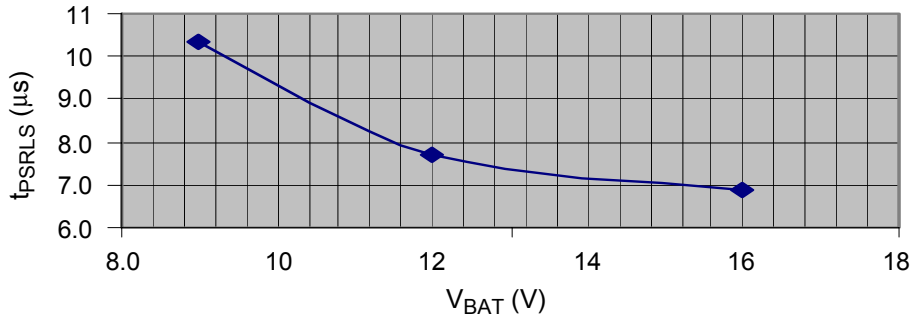


Figure 14. Gate Low-Side (GLS) Sinked Current Capability (High-Speed Mode)



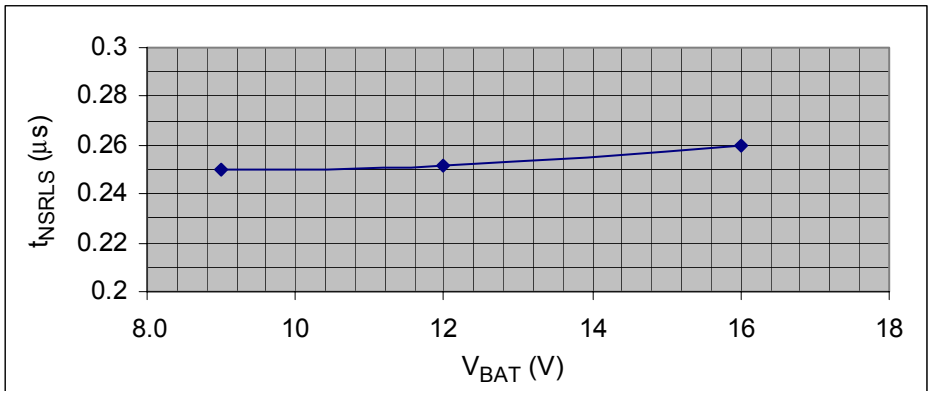
Note Curve is obtained with a load at GLS of 3.3 nF and 10 Ω at 25°C.

Figure 15. Gate Low-Side (GLS) Rise Time (High-Speed Mode)



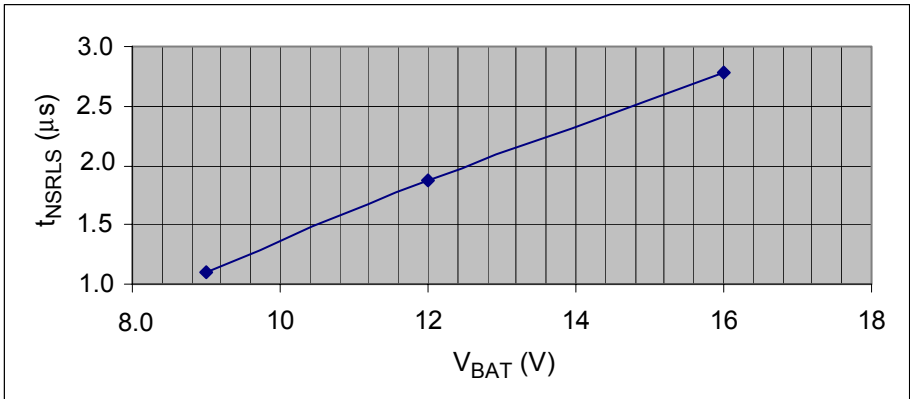
Note Curve is obtained with a load at GLS of 3.3 nF and 10 Ω at 25°C.

Figure 16. Gate Low-Side (GLS) Rise Time (Low-Speed Mode)



Note Curve is obtained with a load at GLS of 3.3 nF and 10 Ω at 25°C.

Figure 17. Gate Low-Side Fall Time (High-Speed Mode)



Note Curve is obtained with a load at GLS of 3.3 nF and 10 Ω at 25°C.

Figure 18. Gate Low-Side Fall Time (Low-Speed Mode)

FUNCTIONAL CURVES

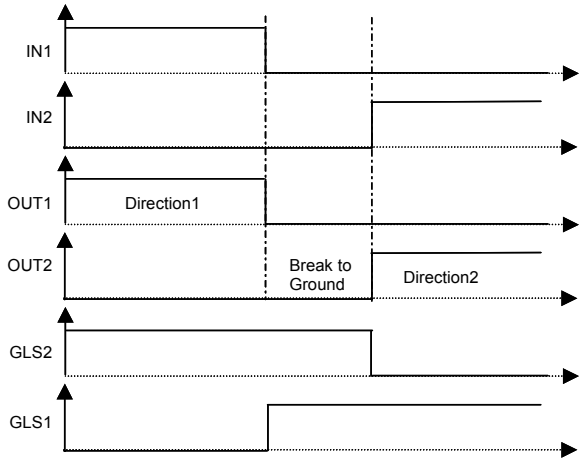


Figure 19. Normal Operation

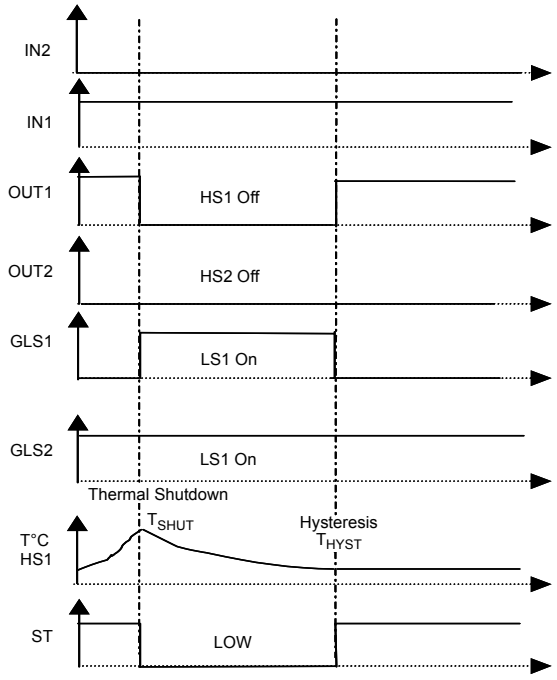


Figure 20. Overtemperature on High-Side 1

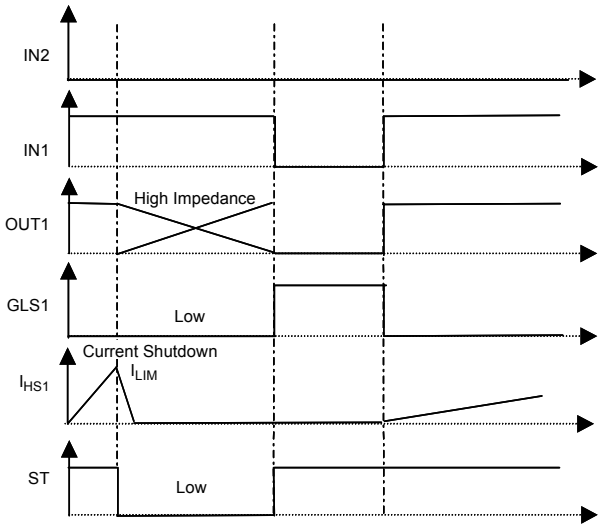


Figure 21. Overcurrent on High-Side 1

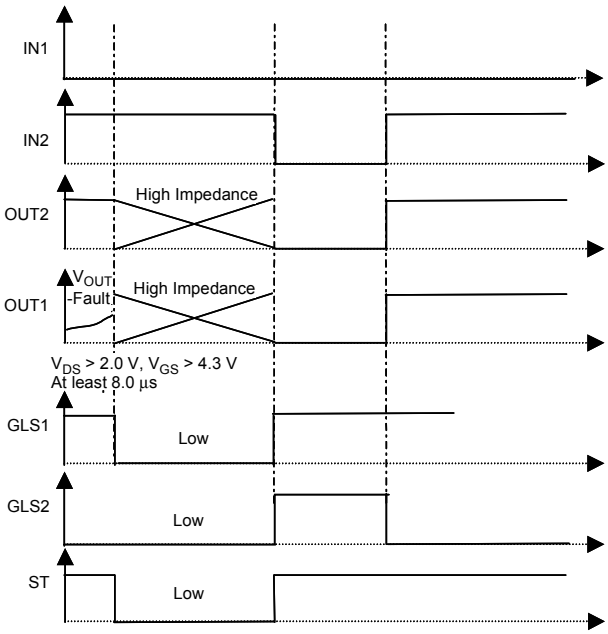


Figure 22. Overload on Low-Side 1

ELECTRICAL PERFORMANCE

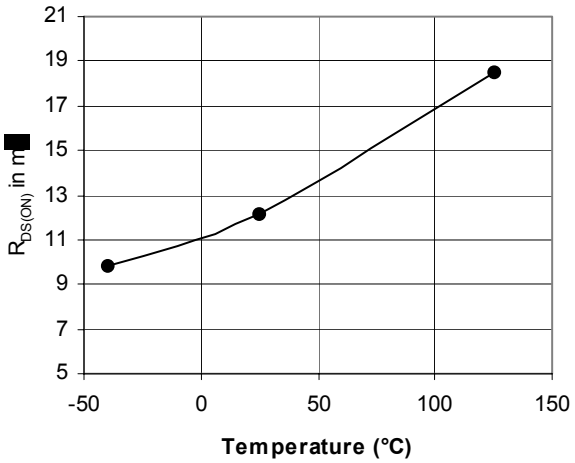


Figure 23. $R_{DS(ON)}$ versus Temperature for V_{BAT} > 10 V

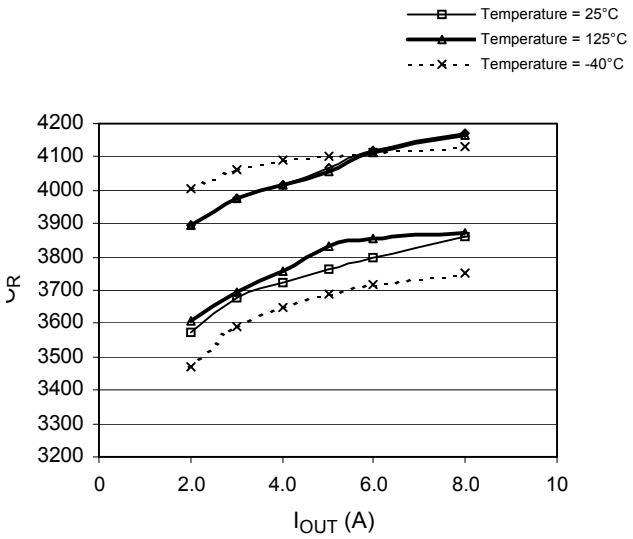


Figure 25. C_R versus I_{OUT} Overtemperature for V_{BAT} = 10 V

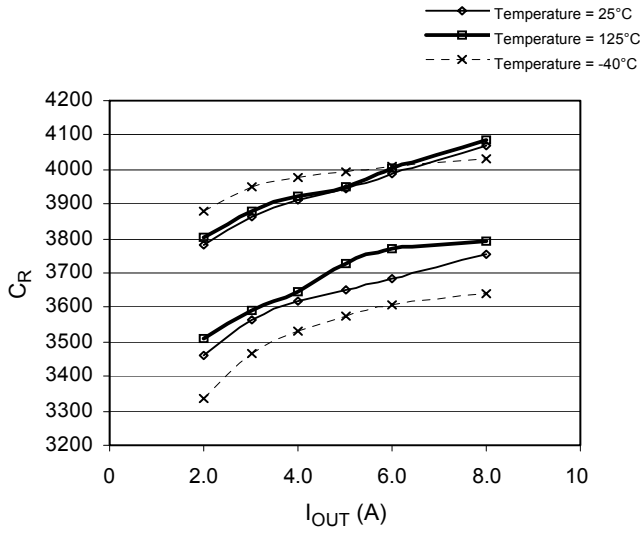


Figure 24. C_R versus I_{OUT} Overtemperature for V_{BAT} = 12 V

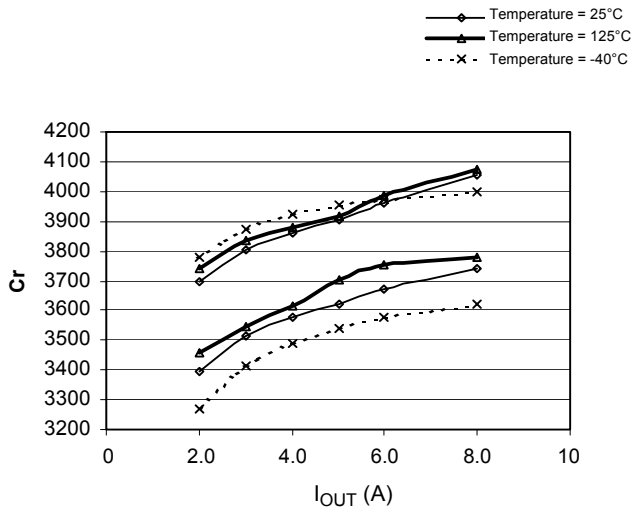


Figure 26. C_R versus I_{OUT} Overtemperature for V_{BAT} = 16 V

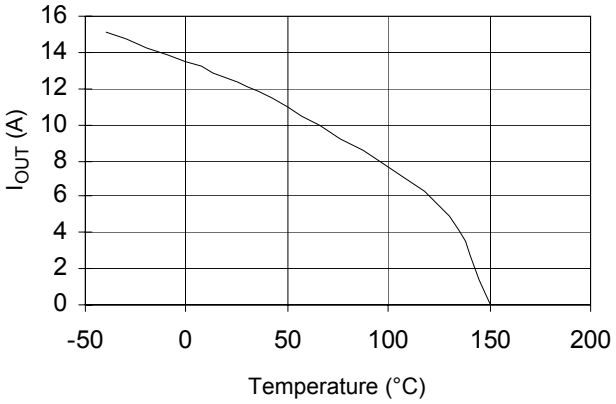


Figure 27. Continuous Current versus Temperature with $R_{\theta JA}$ = 27.5°C/W

Figure 28.

OPERATIONAL MODES

Table 5. TRUTH TABLE

Standard H-Bridge Conditions	IN1	IN2	WAKE	OUT1	OUT	GLS1	GLS2	ST	Comment
Normal Operation	X	X	0	Z	Z	L	L	1	Standby Mode
	0	0	1	L	L	H	H	1	Brake to Ground
	1	0	1	H	L	L	H	1	Direction 1
	0	1	1	L	H	H	L	1	Direction 2
	1	1	1	H	H	L	L	1	Not Recommended (9)
Undervoltage	X	X	1	L	L	H	H	1	(10)
Overvoltage	X	X	1	L	L	H	H	1	(10)
Overtemperature High-Side 1	H	L	1	L	L	H	H	0	(11)
Overtemperature High-Side 2	L	H	1	L	L	H	H	0	(11)
Overcurrent High-Side 1	1	X	1	Z	X	L	X	0	(12)
Overcurrent High-Side 2	X	1	1	X	Z	X	L	0	(12)
Overcurrent Low-Side 1	X	X	1	Z	Z	L	L	0	(13)
Overcurrent Low-Side 2	X	X	1	Z	Z	L	L	0	(13)

Legend

0, L = Low level.
1, H = High level.
X = Don’t care.
Z = High impedance.

Notes

9. In H-Bridge configuration it is not advisable to short the motor to V_{BAT}. If an overvoltage condition occurred in this mode, it would damage the 33486A. The current recirculation in the low-side MOSFET is a preferred solution, with IN1=0 and IN2=0.
10. Once the overvoltage condition or undervoltage condition is removed, the H-Bridge recovers its normal operation mode.
11. When the thermal shutdown is reached on one of the high-side MOSFETs, both high sides are turned off with the motor tied to ground. When the overtemperature condition is finished, the H-Bridge recovers it previous normal operation mode.
12. The high-side MOSFET HSn that experienced an overcurrent is latched off. The corresponding output OUTn is open. Once the high-side overcurrent condition is removed, the input INn must be reset in order to recover the normal operation mode.
13. When a short to V_{BAT} of one of the low-side MOSFETs occurs, both outputs are opened to prevent the motor from running. Once the low-side overcurrent is removed, the input INn of the output that experienced the fault must be reset in order to recover the normal operation mode. Figure 22, Overload on Low-Side 1, page 18, shows an example. If an overload happens in low-side 1, OUT1 and OUT2 are both put in high impedance. IN2 must be reset to recover normal mode.

TYPICAL APPLICATIONS

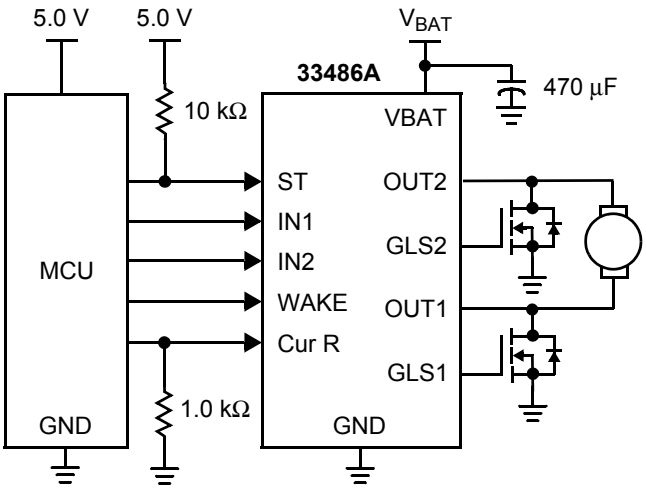


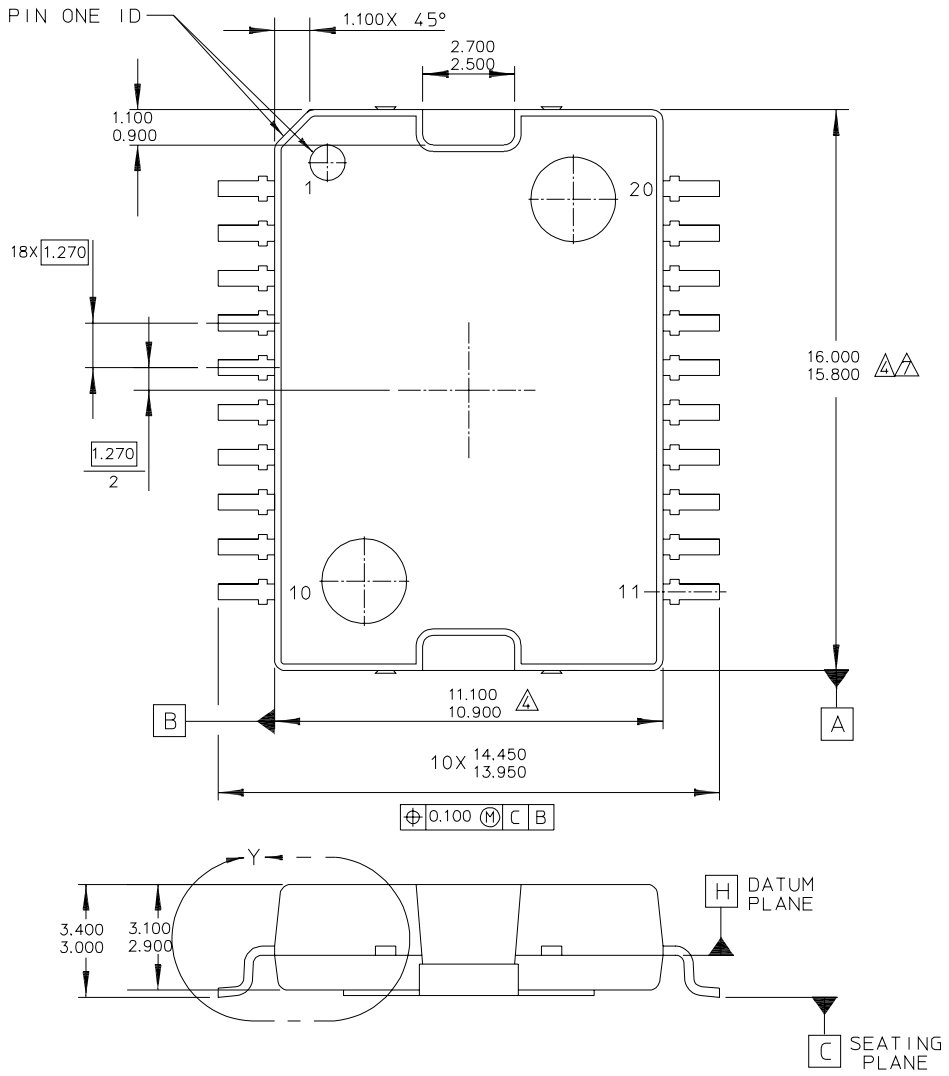
Figure 29. 33486A Typical Application Diagram

PACKAGING

PACKAGING DIMENSIONS

For the most current revision of the package, visit www.freescale.com and do a keyword search using the 98A number for the specific device related to the data sheet.

DW SUFFIX
20-TERMINAL HSOP
98ASH70702A
ISSUE B



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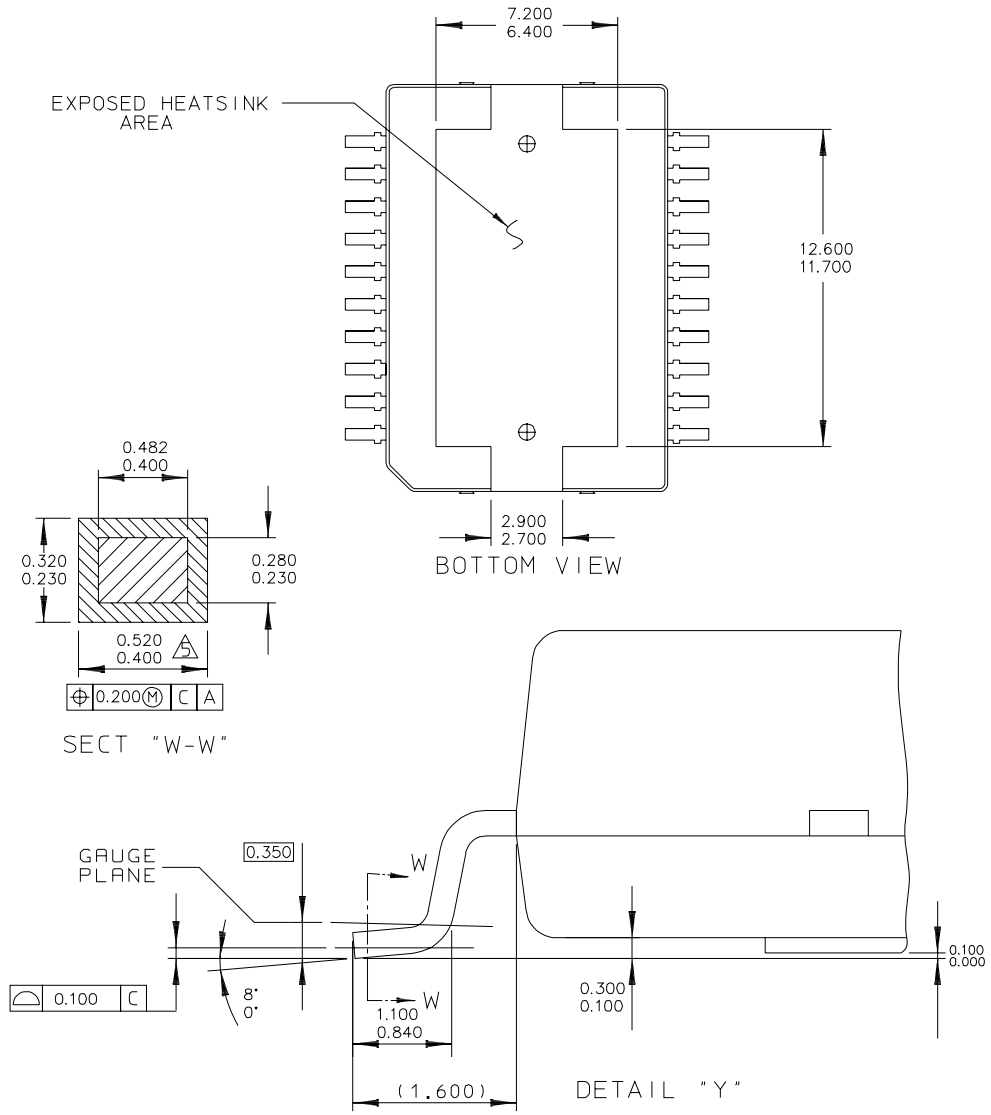
	CASE NUMBER: 979	11 OCT 2005
	STANDARD: NON-JEDEC	

PACKAGING DIMENSIONS (CONTINUED)

DW SUFFIX
20-TERMINAL HSOP
98ASH70702A
ISSUE B



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	CASE NUMBER: 979	11 OCT 2005
	STANDARD: NON-JEDEC	

REVISION HISTORY

Revision	Date	Description of Changes
2.0	12/2005	Updated to Freescale Format Added Thermal Addendum

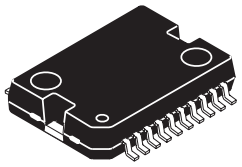
ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 1.0)

DUAL HIGH-SIDE SWITCH FOR H-BRIDGE APPLICATIONS

33486A

20-TERMINAL HSOP



DH SUFFIX
98ASH70702A
20-TERMINAL HSOP

Note For package dimensions, refer to the 33486A device datasheet.

Introduction

This thermal addendum is provided as a supplement to the MC33486 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

The MC33486A package is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 6. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	19	18	21
$R_{\theta JBmn}$ (2)(3)	7.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	51	50	53
$R_{\theta JCmn}$ (5)	< 0.5	0	3.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.

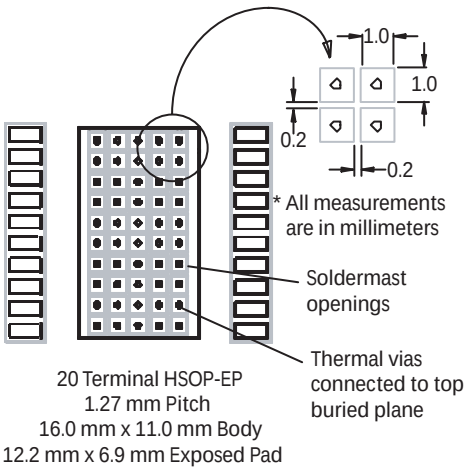


Figure 30. Thermal Land Pattern for Direct Thermal Attachment per JESD51-5

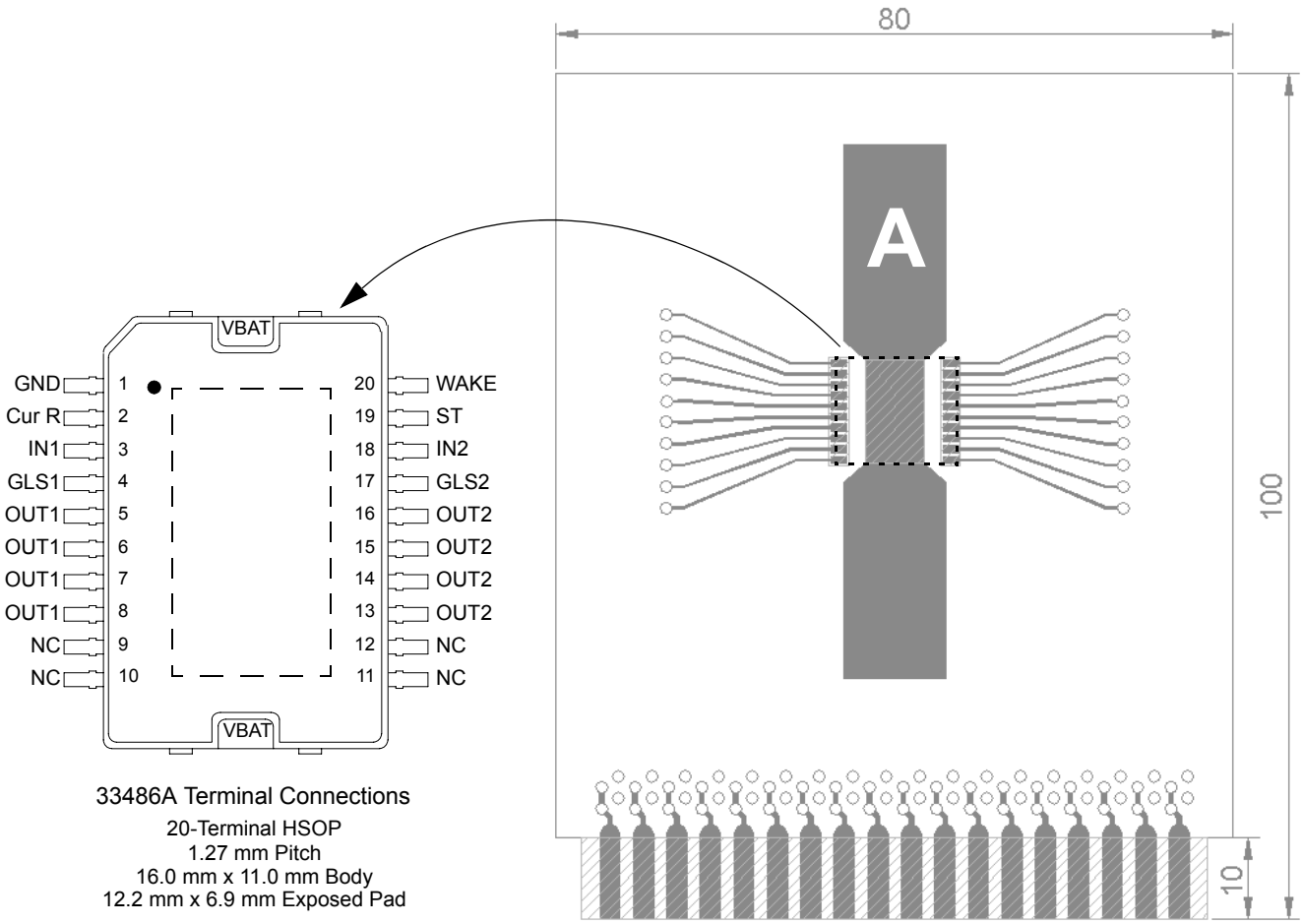


Figure 31. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 7. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JA}$	0	51	50	53
	300	35	34	38
	600	31	30	33
$R_{\theta JS}$	0	11	10	13
	300	7.0	7.0	10
	600	7.0	6.0	9.0

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JS}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package (see Figure 31).

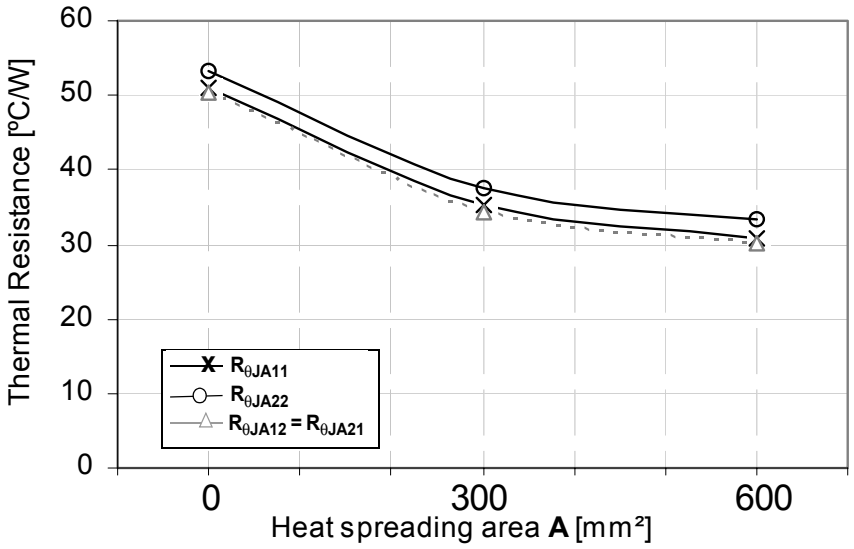


Figure 32. Device on Thermal Test Board $R_{\theta JA}$

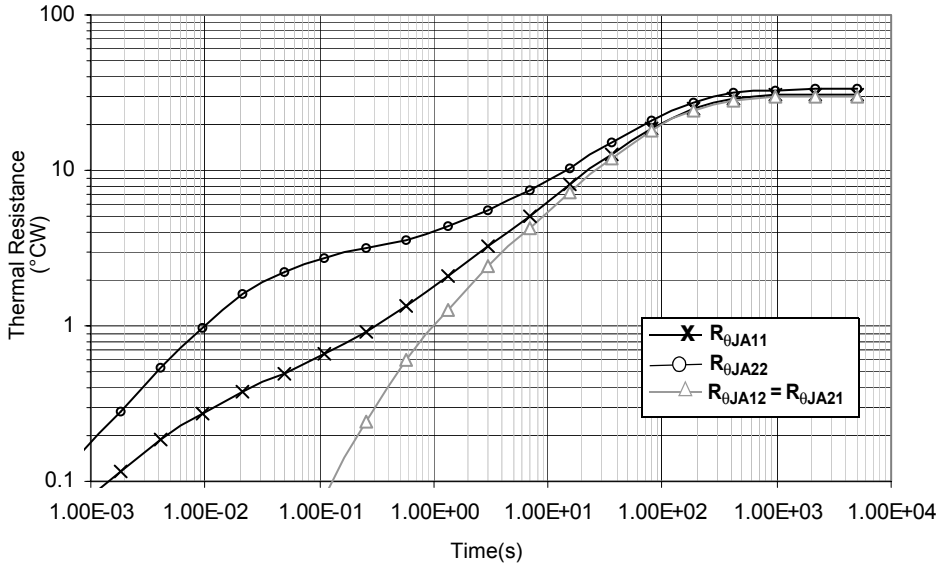


Figure 33. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

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