National Semiconductor

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# 54ABT/74ABT373
# Octal Transparent Latch with TRI-STATE® Outputs

## General Description

The 'ABT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

## Features

- TRI-STATE outputs for bus interfacing
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down
- Nondestructive hot insertion capability
- Standard Military Drawing (SMD) 5962-9321801

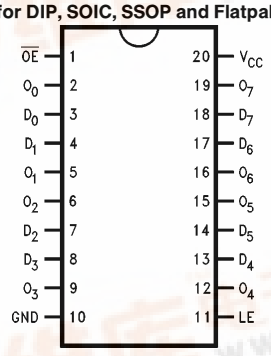
| Commercial | Military | Package Number | Package Description |
|---|---|---|---|
| 74ABT373CSC (Note 1) | | M20B | 20-Lead (0.300″ Wide) Molded Small Outline, JEDEC |
| 74ABT373CSJ (Note 1) | | M20D | 20-Lead (0.300″ Wide) Molded Small Outline, EIAJ |
| 74ABT373CPC | | N20B | 20-Lead (0.300″ Wide) Molded Dual-In-Line |
| | 54ABT373J/883 | J20A | 20-Lead Ceramic Dual-In-Line |
| 74ABT373CMSA (Note 1) | | MSA20 | 20-Lead Molded Shrink Small Outline, EIAJ Type II |
| | 54ABT373W/883 | W20A | 20-Lead Cerpack |
| | 54ABT373E/883 | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |
| 74ABT373CMTC (Notes 1, 2) | | MTC20 | 20-Lead Molded Thin Shrink Small Outline, JEDEC |

**Note 1:** Devices also available in 13″ reel. Use suffix = SCX, SJX, MSAX, and MTCX.

**Note 2:** Contact factory for package availability.

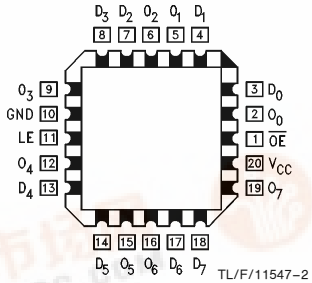
## Connection Diagrams

**Pin Assignment for DIP, SOIC, SSOP and Flatpak**




TL/F/11547–1

**Pin Assignment for LCC**




TL/F/11547–2

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| LE | Latch Enable Input (Active HIGH) |
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| $O_0$–$O_7$ | TRI-STATE Latch Outputs |

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## Functional Description

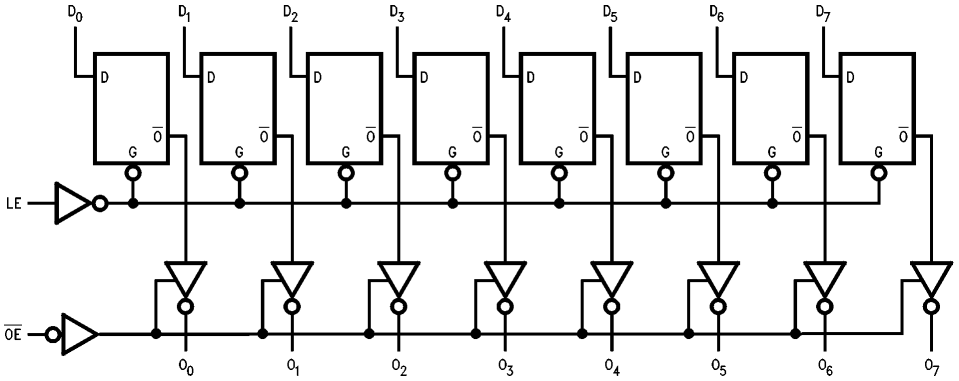
The 'ABT373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the $D_n$ inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Table

| Inputs | | | Output |
|---|---|---|---|
| **LE** | **$\overline{OE}$** | **$D_n$** | **$O_n$** |
| H | L | H | H |
| H | L | L | L |
| L | L | X | $O_n$ (no change) |
| X | H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance State

## Logic Diagram




TL/F/11547–3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | |
| Ceramic | −55°C to +175°C |
| Plastic | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Any Output | |
| in the Disabled or Power-Off State | −0.5V to +5.5V |
| in the HIGH State | −0.5V to $V_{CC}$ |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| DC Latchup Source Current: $\overline{OE}$ Pin | −150 mA |
| (Across Comm Operating Range) Other Pins | −500 mA |
| Over Voltage Latchup (I/O) | 10V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Military | −55°C to +125°C |
| Commercial | −40°C to +85°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |
| Minimum Input Edge Rate | (ΔV/Δt) |
| Data Input | 50 mV/ns |
| Enable Input | 20 mV/ns |

## DC Electrical Characteristics

| Symbol | Parameter | | ABT373 Min | ABT373 Typ | ABT373 Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 54ABT/74ABT | 2.5 | | | V | Min | $I_{OH}$ = −3 mA |
| | | 54ABT | 2.0 | | | | | $I_{OH}$ = −24 mA |
| | | 74ABT | 2.0 | | | | | $I_{OH}$ = −32 mA |
| $V_{OL}$ | Output LOW Voltage | 54ABT | | | 0.55 | V | Min | $I_{OL}$ = 48 mA |
| | | 74ABT | | | 0.55 | | | $I_{OL}$ = 64 mA |
| $I_{IH}$ | Input HIGH Current | | | | 5 | μA | Max | $V_{IN}$ = 2.7V (Note 2) |
| | | | | | 5 | | | $V_{IN}$ = $V_{CC}$ |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | | 7 | μA | Max | $V_{IN}$ = 7.0V |
| $I_{IL}$ | Input LOW Current | | | | −5 | μA | Max | $V_{IN}$ = 0.5V (Note 2) |
| | | | | | −5 | | | $V_{IN}$ = 0.0V |
| $V_{ID}$ | Input Leakage Test | | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 μA<br>All Other Pins Grounded |
| $I_{OZH}$ | Output Leakage Current | | | | 50 | μA | 0 − 5.5V | $V_{OUT}$ = 2.7V; $\overline{OE}$ = 2.0V |
| $I_{OZL}$ | Output Leakage Current | | | | −50 | μA | 0 − 5.5V | $V_{OUT}$ = 0.5V; $\overline{OE}$ = 2.0V |
| $I_{OS}$ | Output Short-Circuit Current | | −100 | | −275 | mA | Max | $V_{OUT}$ = 0.0V |
| $I_{CEX}$ | Output High Leakage Current | | | | 50 | μA | Max | $V_{OUT}$ = $V_{CC}$ |
| $I_{ZZ}$ | Bus Drainage Test | | | | 100 | μA | 0.0 | $V_{OUT}$ = 5.5V; All Others GND |
| $I_{CCH}$ | Power Supply Current | | | | 50 | μA | Max | All Outputs HIGH |
| $I_{CCL}$ | Power Supply Current | | | | 30 | mA | Max | All Outputs LOW |
| $I_{CCZ}$ | Power Supply Current | | | | 50 | μA | Max | $\overline{OE}$ = $V_{CC}$<br>All Others at $V_{CC}$ or GND |
| $I_{CCT}$ | Additional $I_{CC}$/Input | Outputs Enabled | | | 2.5 | mA | Max | $V_I$ = $V_{CC}$ − 2.1V |
| | | Outputs TRI-STATE | | | 2.5 | mA | | Enable Input $V_I$ = $V_{CC}$ − 2.1V |
| | | Outputs TRI-STATE | | | 2.5 | mA | | Data Input $V_I$ = $V_{CC}$ − 2.1V<br>All Others at $V_{CC}$ or GND |
| $I_{CCD}$ | Dynamic $I_{CC}$ (Note 2) | No Load | | | 0.12 | mA/MHz | Max | Outputs Open, LE = $V_{CC}$<br>$\overline{OE}$ = GND, (Note 1)<br>One Bit Toggling, 50% Duty Cycle |

**Note 1:** For 8 bits toggling, $I_{CCD}$ < 0.8 mA/MHz.
**Note 2:** Guaranteed, but not tested.

## DC Electrical Characteristics (SOIC Package) (Continued)

| Symbol | Parameter | Min | Typ | Max | Units | $V_{CC}$ | Conditions $C_L = 50$ pF, $R_L = 500\Omega$ |
|---|---|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | | 0.4 | 0.8 | V | 5.0 | $T_A = 25°C$ (Note 1) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −1.2 | −0.8 | | V | 5.0 | $T_A = 25°C$ (Note 1) |
| $V_{OHV}$ | Minimum High Level Dynamic Output Voltage | 2.5 | 3.0 | | V | 5.0 | $T_A = 25°C$ (Note 3) |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | 2.0 | 1.7 | | V | 5.0 | $T_A = 25°C$ (Note 2) |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 0.9 | 0.6 | V | 5.0 | $T_A = 25°C$ (Note 2) |

**Note 1:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

**Note 2:** Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to theshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$). Guaranteed, but not tested.

**Note 3:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

## AC Electrical Characteristics

| Symbol | Parameter | 74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | | 54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF | | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$D_n$ to $O_n$ | 1.9<br>1.9 | 2.7<br>2.8 | 4.5<br>4.5 | 1.0<br>1.0 | 6.8<br>7.0 | 1.9<br>1.9 | 4.5<br>4.5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LE to $O_n$ | 2.0<br>2.0 | 3.1<br>3.0 | 5.0<br>5.0 | 1.0<br>1.5 | 7.7<br>7.7 | 2.0<br>2.0 | 5.0<br>5.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | 1.5<br>1.5 | 3.1<br>3.1 | 5.3<br>5.3 | 1.0<br>1.5 | 6.7<br>7.2 | 1.5<br>1.5 | 5.3<br>5.3 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time | 2.0<br>2.0 | 3.6<br>3.4 | 5.4<br>5.4 | 1.7<br>1.0 | 8.0<br>7.0 | 2.0<br>2.0 | 5.4<br>5.4 | ns |

## AC Operating Requirements

| Symbol | Parameter | 74ABT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | | 54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF | | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $f_{toggle}$ | Max Toggle Frequency | | 100 | | 100 | | | | MHz |
| $t_s(H)$<br>$t_s(L)$ | Setup Time, HIGH<br>or LOW $D_n$ to LE | 1.5<br>1.5 | | | 2.5<br>2.5 | | 1.5<br>1.5 | | ns |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH<br>or LOW $D_n$ to LE | 1.0<br>1.0 | | | 2.5<br>2.5 | | 1.0<br>1.0 | | ns |
| $t_w(H)$ | Pulse Width,<br>LE HIGH | 3.0 | | | 3.3 | | 3.0 | | ns |

## Extended AC Electrical Characteristics

(SOIC package)

| Symbol | Parameter | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 4) | | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 5) | | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 6) | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$D_n$ to $O_n$ | 1.5<br>1.5 | 5.2<br>5.2 | 2.0<br>2.0 | 6.8<br>6.8 | 2.0<br>2.0 | 9.0<br>9.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LE to $O_n$ | 1.5<br>1.5 | 5.5<br>5.5 | 2.0<br>2.0 | 7.5<br>7.5 | 2.0<br>2.0 | 9.5<br>9.5 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | 1.5<br>1.5 | 6.2<br>6.2 | 2.0<br>2.0 | 8.0<br>8.0 | 2.0<br>2.0 | 10.5<br>10.5 | ns |
| $t_{PHZ}$<br>$t_{PZL}$ | Output Disable Time | 1.0<br>1.0 | 5.5<br>5.5 | (Note 7) | | (Note 7) | | ns |

**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

**Note 5:** This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in plce of the 50 pF load capacitors in the standard AC load. This specificaiton pertains to single output switching only.

**Note 6:** This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 7:** The TRI-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

## Skew

| Symbol | Parameter | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 3) | 74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 4) | Units |
|---|---|---|---|---|
| | | Max | Max | |
| $t_{OSHL}$ (Note 1) | Pin to Pin Skew HL Transitions | 1.0 | 1.5 | ns |
| $t_{OSLH}$ (Note 1) | Pin to Pin Skew LH Transitions | 1.0 | 1.5 | ns |
| $t_{PS}$ (Note 5) | Duty Cycle LH–HL Skew | 1.4 | 3.5 | ns |
| $t_{OST}$ (Note 1) | Pin to Pin Skew LH/HL Transitions | 1.5 | 3.9 | ns |
| $t_{PV}$ (Note 2) | Device to Device Skew LH/HL Transitions | 2.0 | 4.0 | ns |

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW ($t_{OSHL}$), LOW to HIGH ($t_{OSLH}$), or any combination switching LOW to HIGH and/or HIGH to LOW ($t_{OST}$). This specification is guaranteed but not tested.

**Note 2:** Propagation delay variation for a given set of conditions (i.e., temperature and $V_{CC}$) from device to device. This specification is guaranteed but not tested.

**Note 3:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

**Note 4:** This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

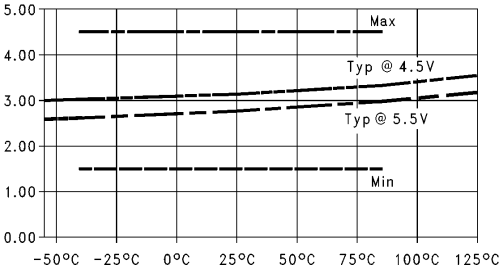
**Note 5:** This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions ($T_A$ = 25°C) |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | pF | $V_{CC}$ = 0V |
| $C_{OUT}$ (Note 1) | Output Capacitance | 9 | pF | $V_{CC}$ = 5.0V |

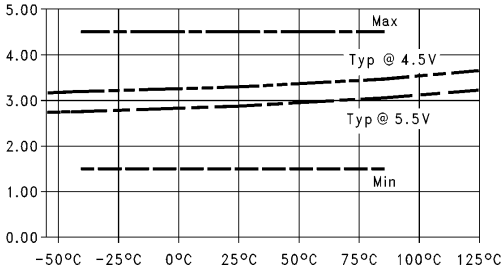
**Note 1:** $C_{OUT}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

**$t_{PLH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**Data to Output**



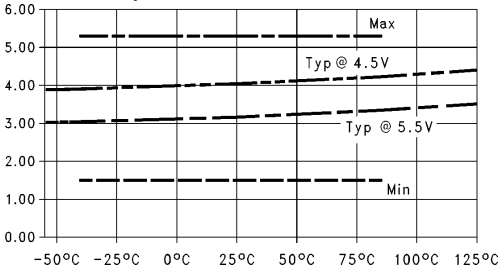

TL/F/11547–11

**$t_{PHL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**Data to Output**



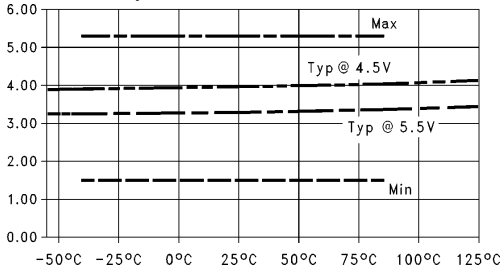

TL/F/11547–12

**$t_{PZH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**$\overline{OE}$ to Output**



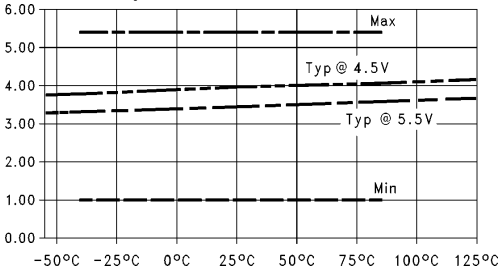

TL/F/11547–13

**$t_{PZL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**$\overline{OE}$ to Output**



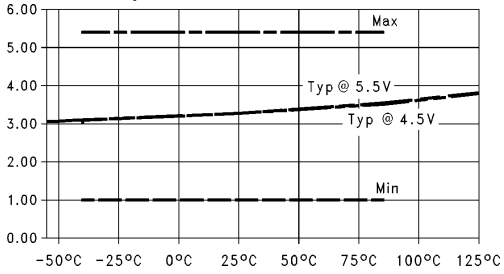

TL/F/11547–14

**$t_{PHZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**$\overline{OE}$ to Output**




TL/F/11547–15

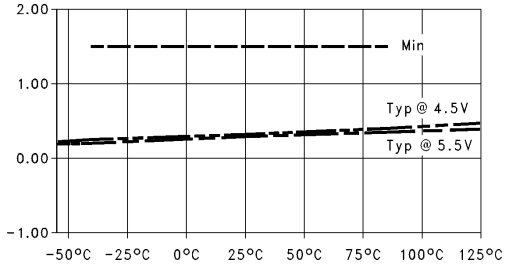
**$t_{PLZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**$\overline{OE}$ to Output**




TL/F/11547–16

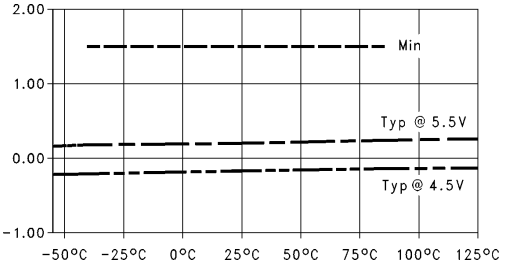
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

**$t_{SET}$ LOW vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**Data to LE**




TL/F/11547–17

**$t_{SET}$ HIGH vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**Data to LE**

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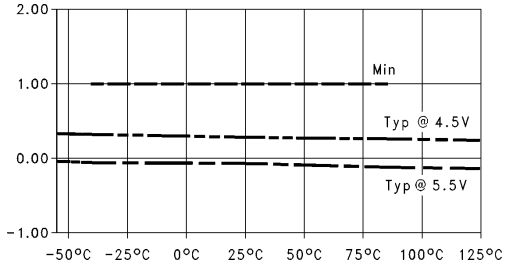
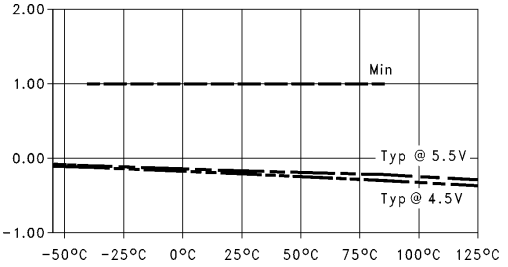
**$t_{HOLD}$ HIGH vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**Data to LE**



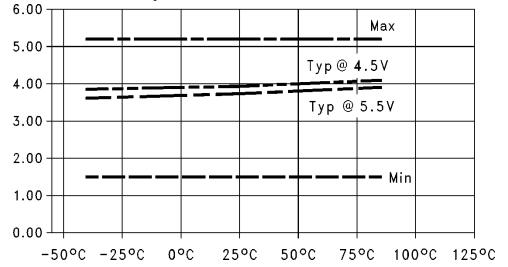

TL/F/11547–19

**$t_{HOLD}$ LOW vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**Data to LE**



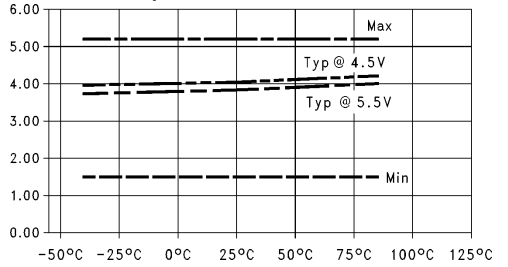

TL/F/11547–20

**$t_{PLH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**Data to Output**



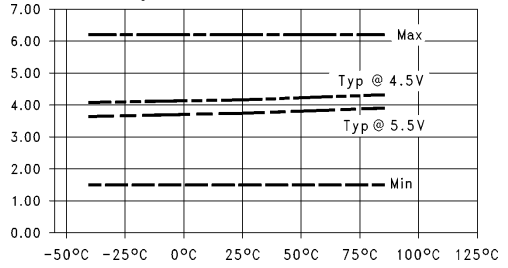

TL/F/11547–21

**$t_{PHL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**Data to Output**



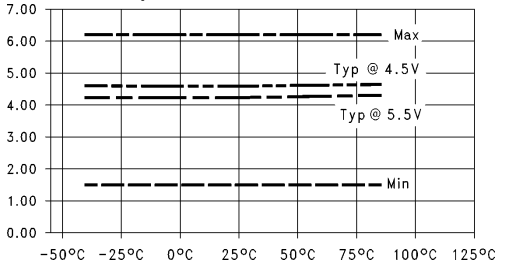

TL/F/11547–22

**$t_{PZH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**$\overline{OE}$ to Output**




TL/F/11547–23

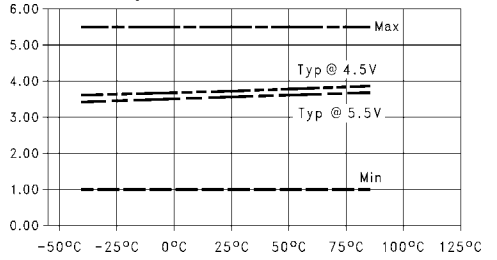
**$t_{PZL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**$\overline{OE}$ to Output**




TL/F/11547–24

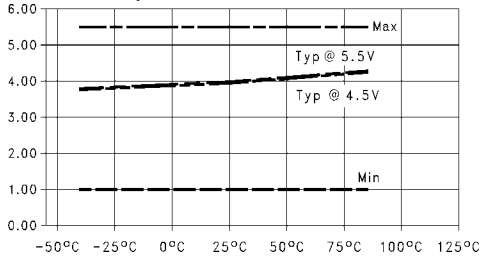
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

**$t_{PHZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**$\overline{OE}$ to Output**



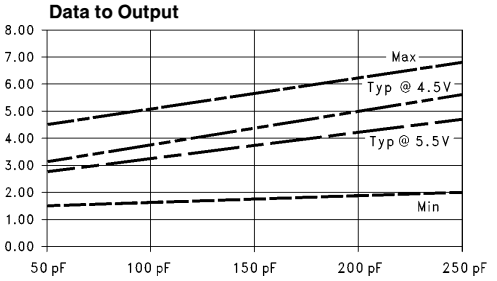

TL/F/11547–25

**$t_{PLZ}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**$\overline{OE}$ to Output**



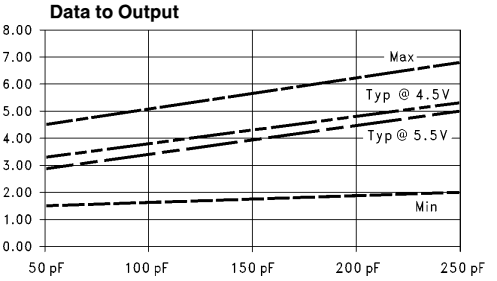

TL/F/11547–26

**$t_{PLH}$ vs Load Capacitance**
**$T_A$ = 25°C, 1 Output Switching**
**Data to Output**



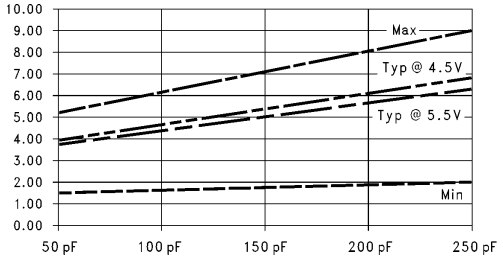

TL/F/11547–27

**$t_{PHL}$ vs Load Capacitance**
**$T_A$ = 25°C, 1 Output Switching**
**Data to Output**



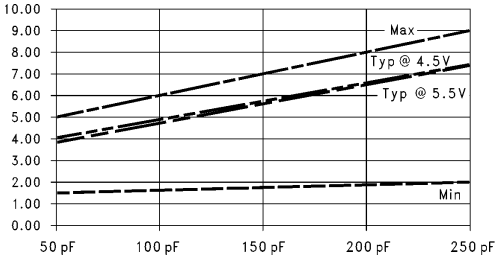

TL/F/11547–28

**$t_{PLH}$ vs Load Capacitance**
**$T_A$ = 25°C, 8 Outputs Switching**
**Data to Output**



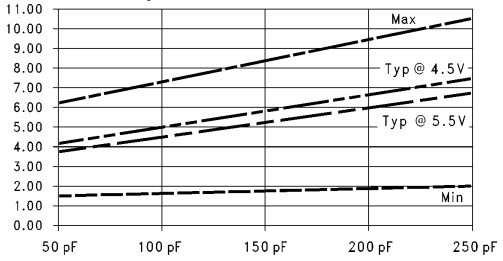

TL/F/11547–29

**$t_{PHL}$ vs Load Capacitance**
**$T_A$ = 25°C, 8 Outputs Switching**
**Data to Output**



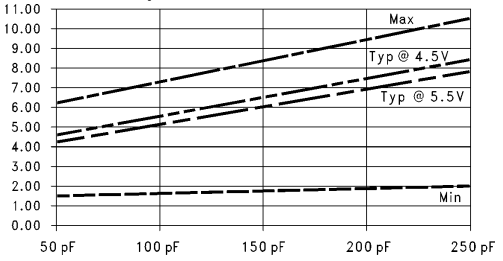

TL/F/11547–30

**$t_{PZH}$ vs Load Capacitance**
**$T_A$ = 25°C, 8 Outputs Switching**
**$\overline{OE}$ to Output**




TL/F/11547–31

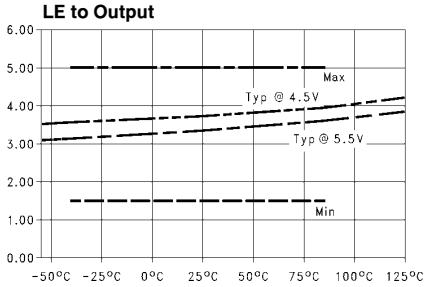
**$t_{PZL}$ vs Load Capacitance**
**$T_A$ = 25°C, 8 Outputs Switching**
**$\overline{OE}$ to Output**




TL/F/11547–32

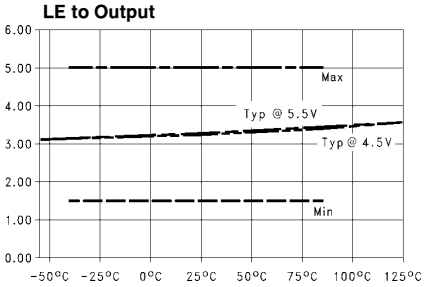
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

**$t_{PLH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**LE to Output**



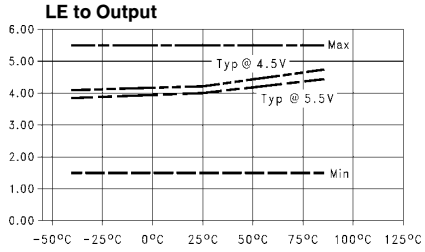

TL/F/11547–35

**$t_{PHL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 1 Output Switching**
**LE to Output**



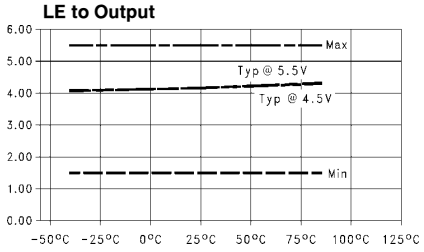

TL/F/11547–36

**$t_{PLH}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**LE to Output**



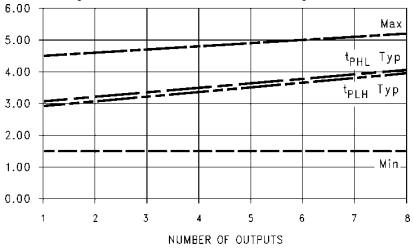

TL/F/11547–37

**$t_{PHL}$ vs Temperature ($T_A$)**
**$C_L$ = 50 pF, 8 Outputs Switching**
**LE to Output**



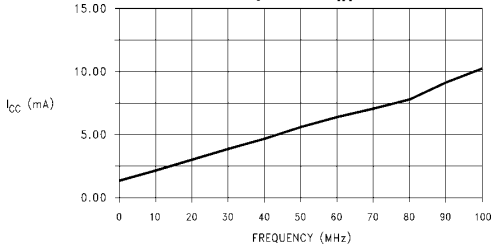

TL/F/11547–38

**$t_{PLH}$ and $t_{PHL}$ vs Number Outputs Switching**
**$C_L$ = 50 pF, $T_A$ = 25°C, $V_{CC}$ = 5.0V,**
**Outputs In Phase Data to Output**




TL/F/11547–33

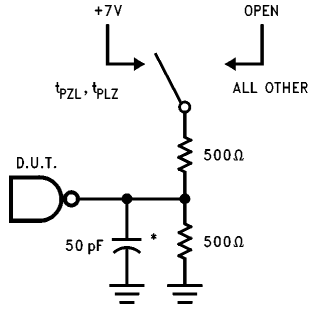
**Typical $I_{CC}$ vs Output Switching Frequency**
**$C_L$ = 0 pF, $V_{CC}$ = $V_{IH}$ = 5.5V, LE = GND,**
**1 Output Switching at 50% Duty Cycle**
**Data to Output, Transparent Mode with**
**Unused Data Inputs = $V_{IH}$**




TL/F/11547–34

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

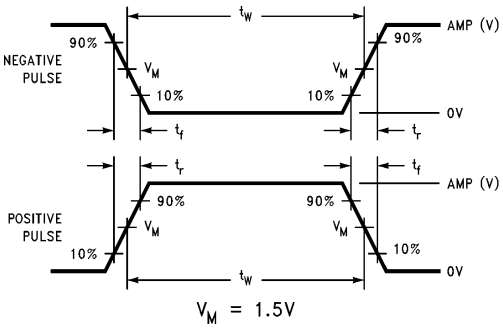
## AC Loading




*Includes jig and probe capacitance

TL/F/11547–4

**FIGURE 1. Standard AC Test Load**

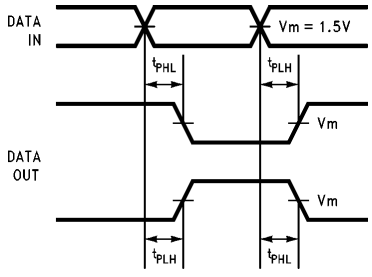



TL/F/11547–6

**FIGURE 2a. Test Input Signal Levels**

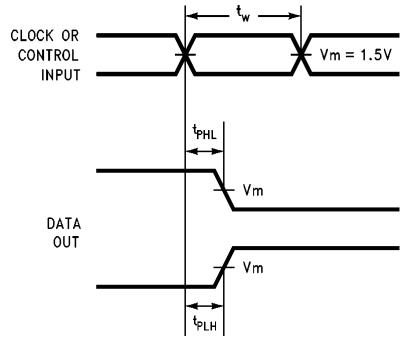
| Amplitude | Rep. Rate | $t_w$ | $t_r$ | $t_f$ |
|---|---|---|---|---|
| 3.0V | 1 MHz | 500 ns | 2.5 ns | 2.5 ns |

**FIGURE 2b. Test Input Signal Requirements**



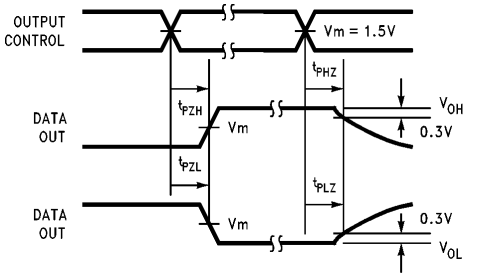

TL/F/11547–8

**FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



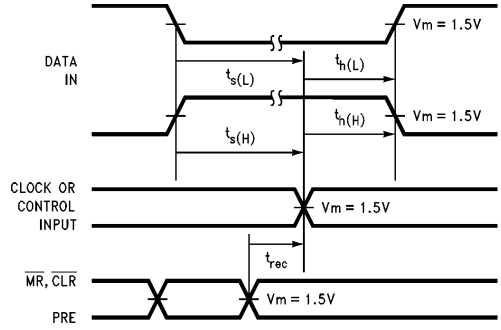

TL/F/11547–5

**FIGURE 4. Propagation Delay, Pulse Width Waveforms**




TL/F/11547–7

**FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times**

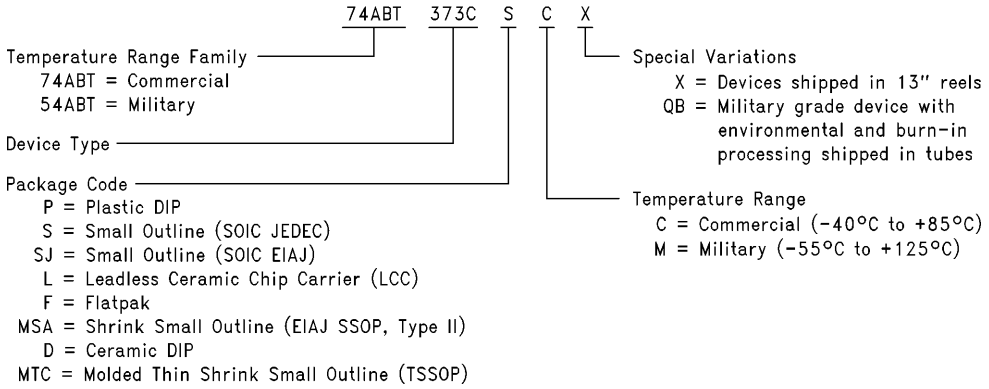



TL/F/11547–9

**FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms**

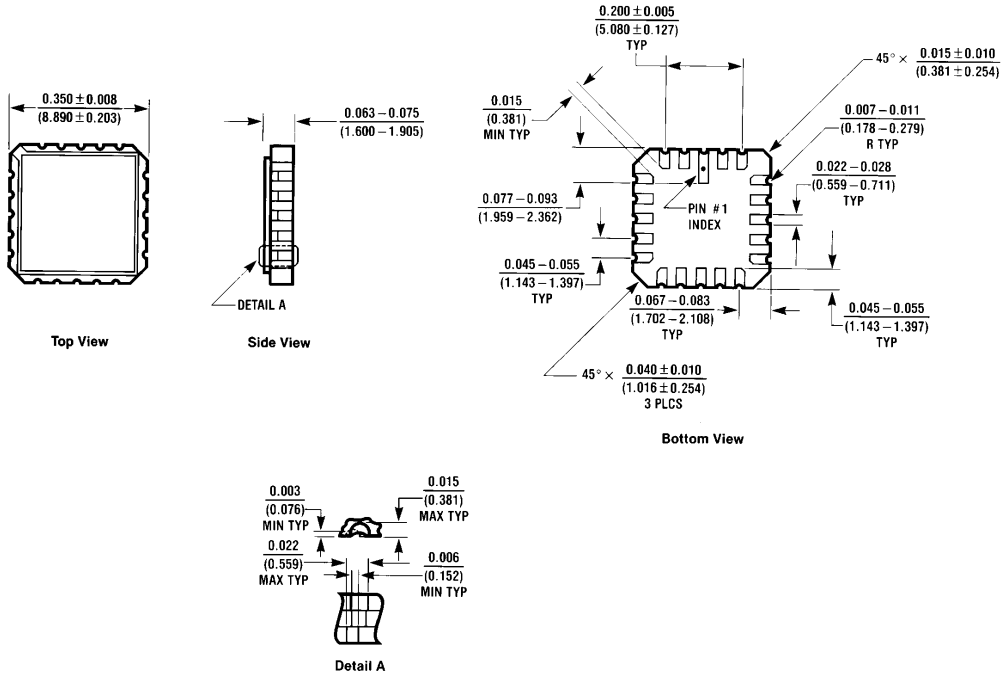
## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



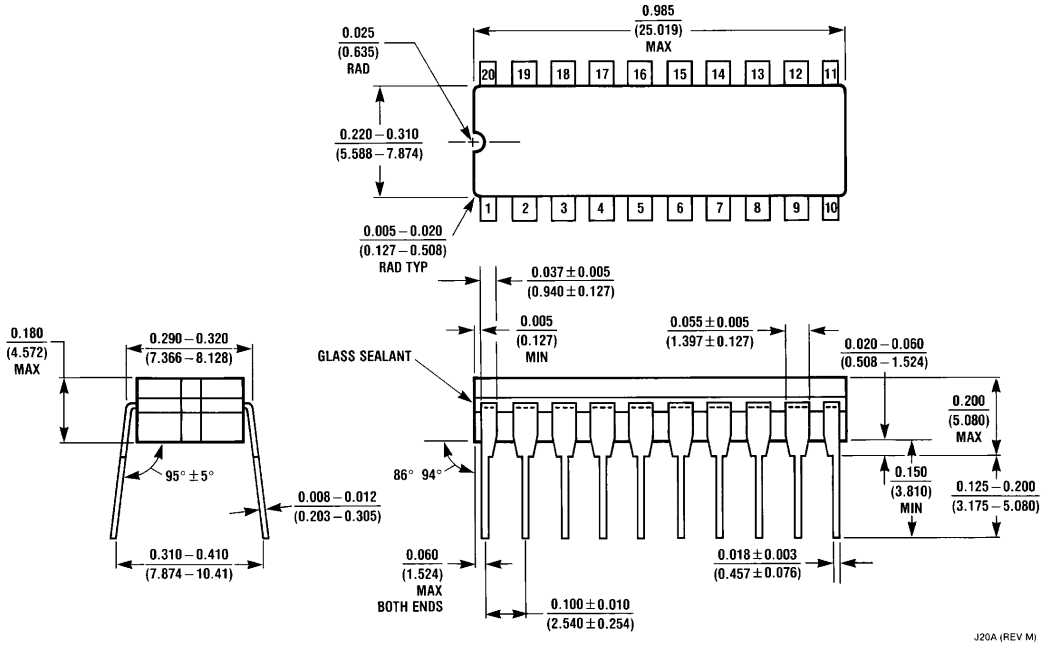

TL/F/11547–39

## Physical Dimensions inches (millimeters)

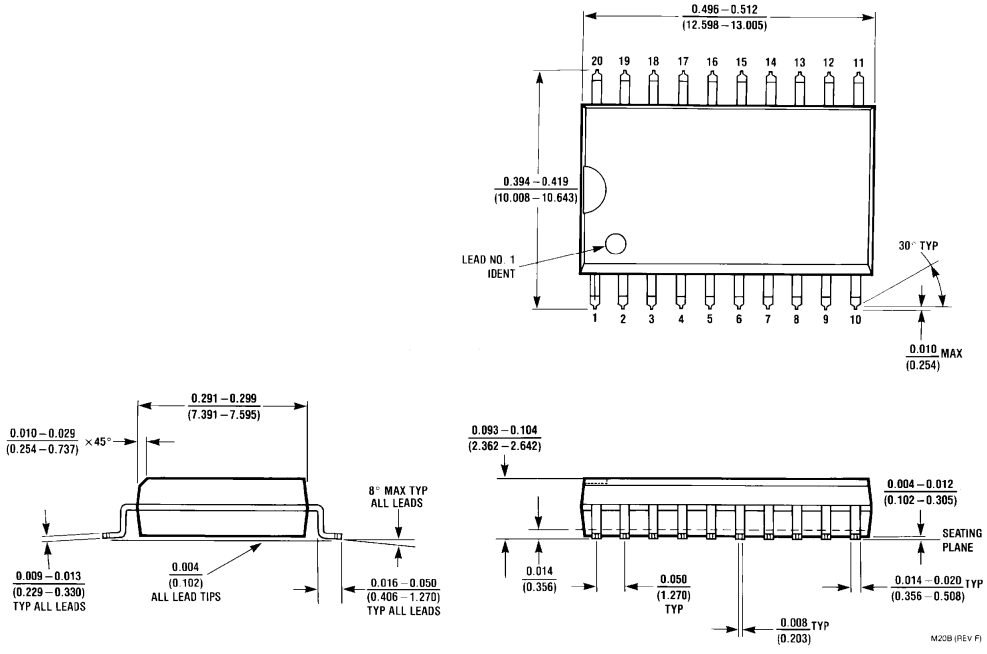



**20-Terminal Ceramic Chip Carrier (L)**
**NS Package Number E20A**

## Physical Dimensions inches (millimeters) (Continued)

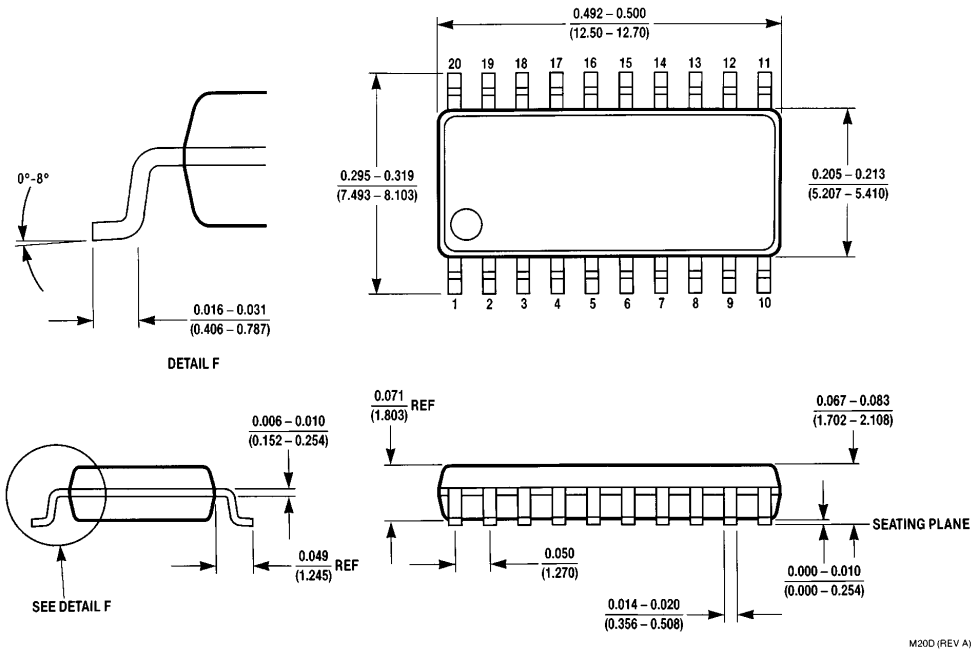



**20-Lead Ceramic Dual-In-Line (D)**
**NS Package Number J20A**

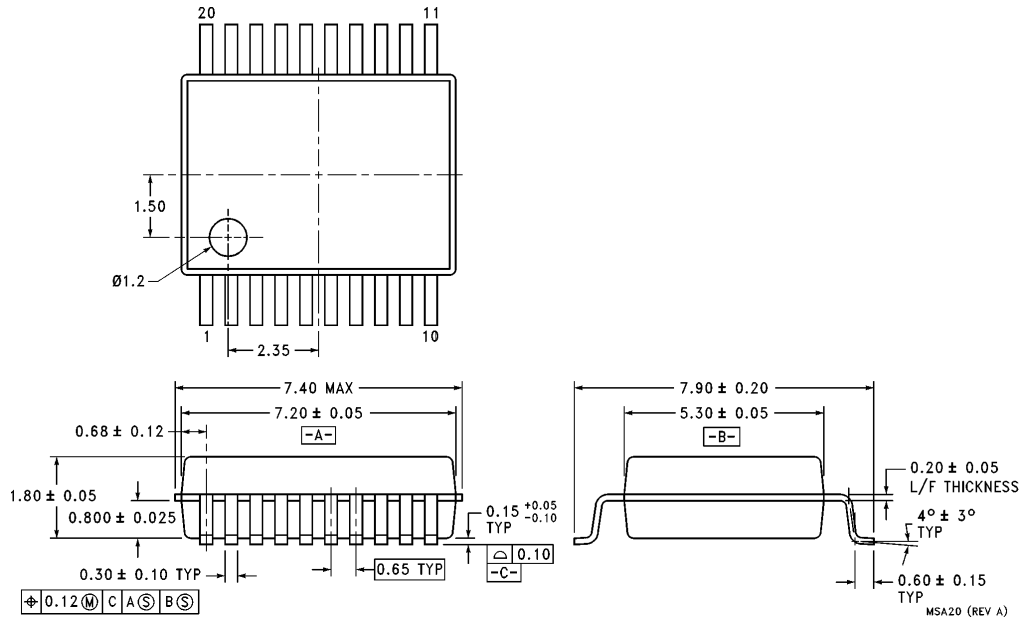



**20-Lead Small Outline Integrated Circuit JEDEC (S)**
**NS Package Number M20B**

## Physical Dimensions inches (millimeters) (Continued)

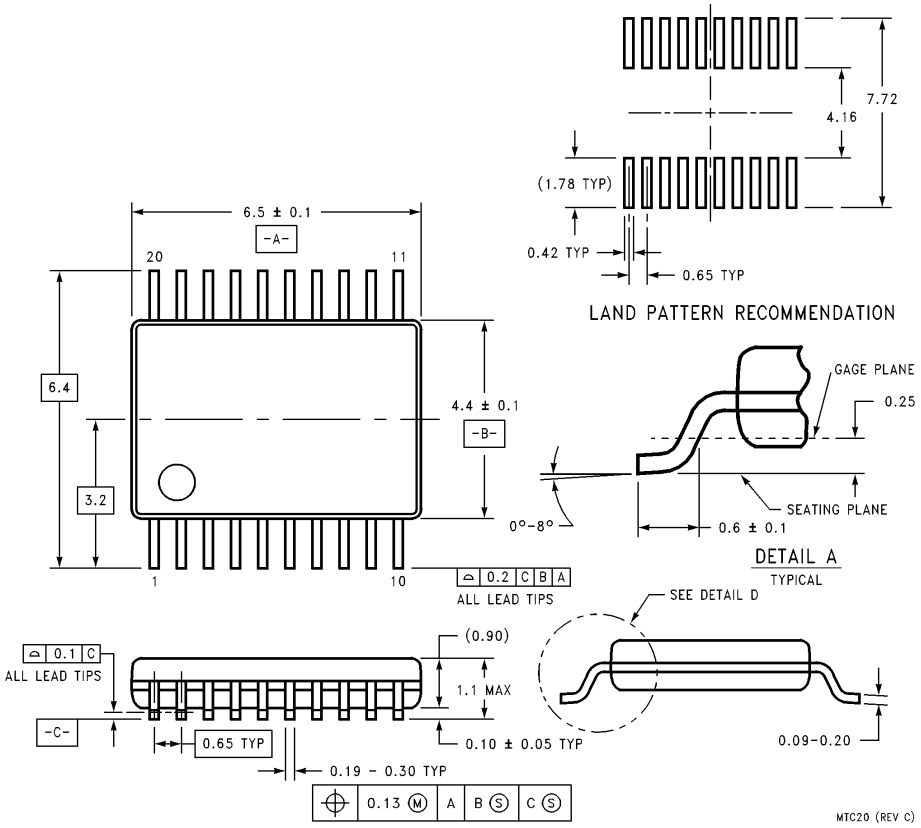



**20-Lead Small Outline Integrated Circuit EIAJ (SJ)**
**NS Package Number M20D**



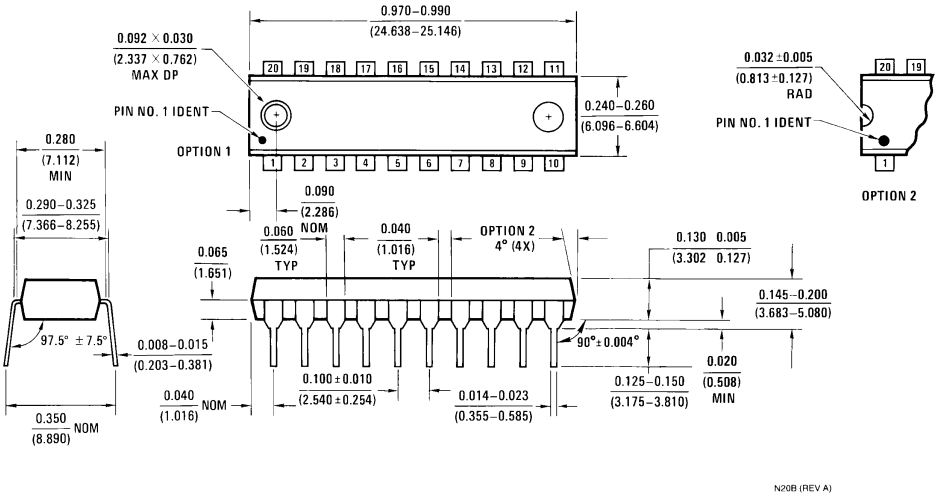

**20-Lead Plastic EIAJ SSOP (MSA)**
**NS Package Number MSA20**

## Physical Dimensions inches (millimeters) (Continued)



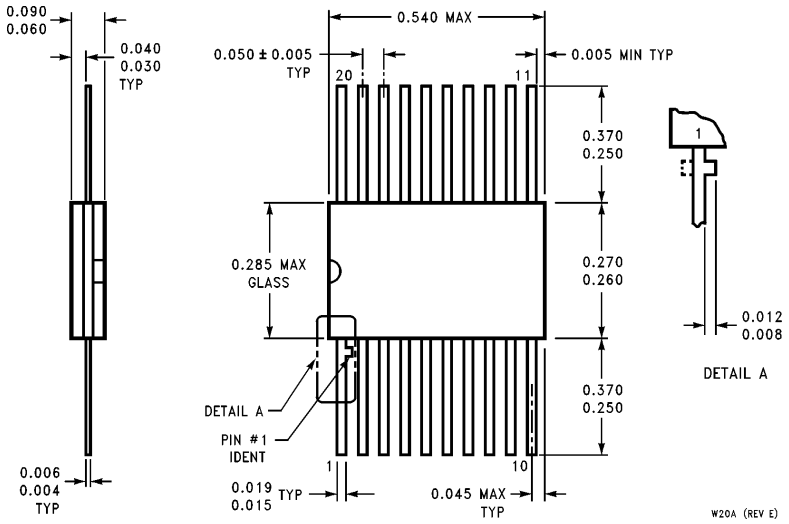

All dimensions are in millimeters.

**20-Lead Molded Thin Shrink Small Outline Package JEDEC (MTC)**
**NS Package Number MTC20**




**20-Lead Plastic Dual-In-Line Package (P)**
**NS Package Number N20B**

## Physical Dimensions inches (millimeters) (Continued)




**20-Lead Ceramic Flatpak (F)**
**NS Package Number W20A**

### LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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