

74AHC00; 74AHCT00

Quad 2-input NAND gate

Rev. 03 — 8 January 2008

Product data sheet

1. General description

The 74AHC00; 74AHCT00 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74AHC00; 74AHCT00 provides the quad 2-input NAND function.

2. Features

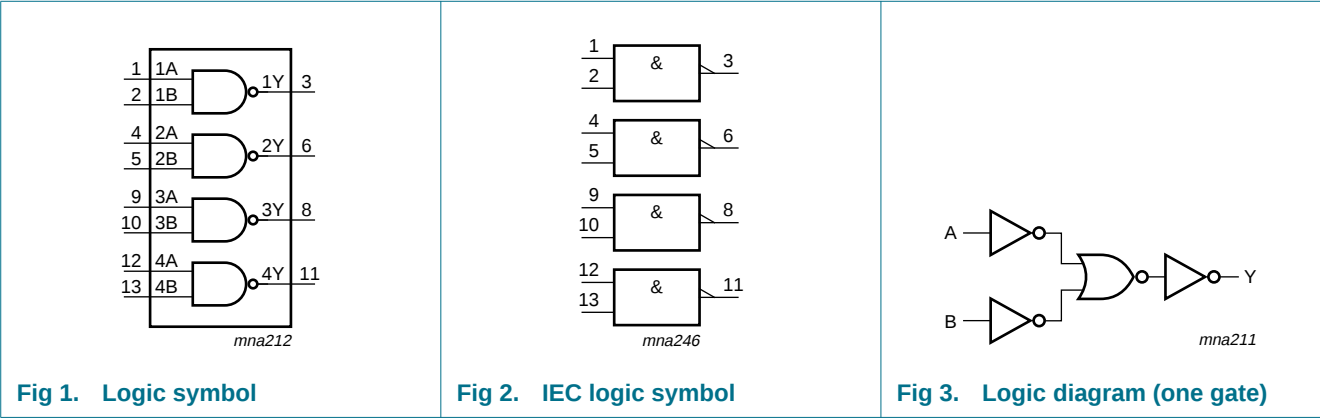
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- For 74AHC00 only: operates with CMOS input levels
- For 74AHCT00 only: operates with TTL input levels
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

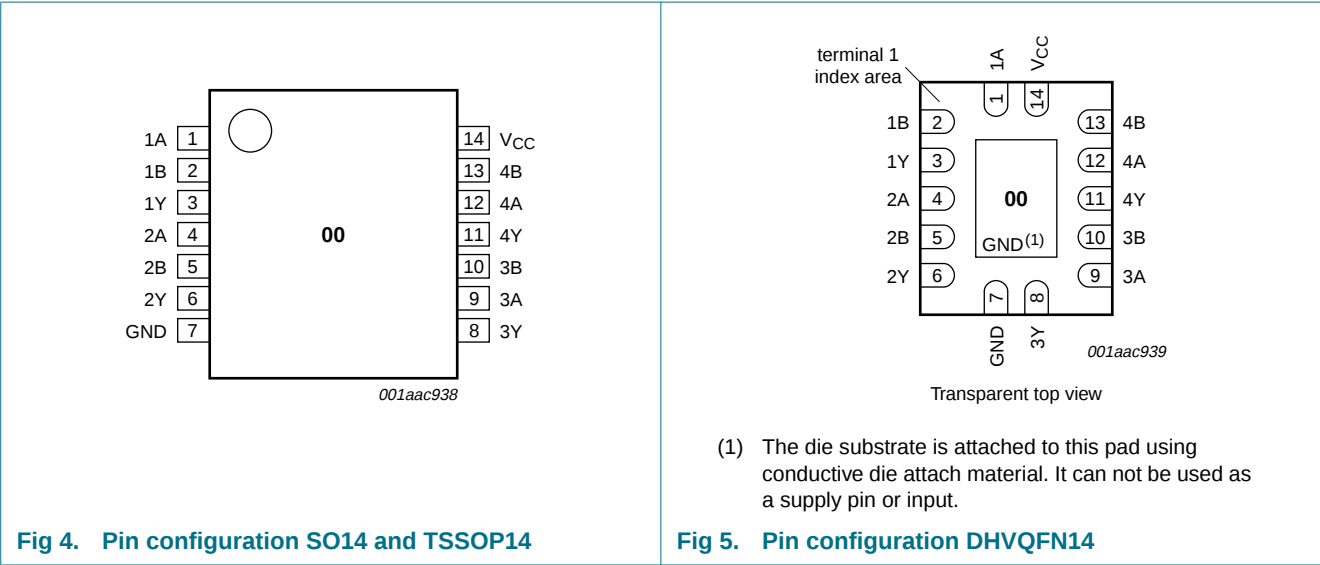
Type number	Package			
	Temperature range	Name	Description	Version
74AHC00D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT00D				
74AHC00PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT00PW				
74AHC00BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1
74AHCT00BQ				

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)

Table 2. Pin description ...continued

Symbol	Pin	Description
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection^[1]

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	^[1] -20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	^[1] -	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
	SO14 package		^[2] -	500	mW
	TSSOP14 package		^[3] -	500	mW
	DHVQFN14 package		^[4] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC00			74AHCT00			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC00										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = −50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.4	-	V
		I _O = −8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
C _I	input capacitance		-	3.0	10	-	10	-	10	pF

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHCT00										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = –50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = –8.0 mA	3.94	-	-	3.8	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} – 2.1 V; I _O = 0 A; other pins at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	3.0	10	-	10	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
 GND = 0 V; For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
For type 74AHC00										
t _{pd}	propagation delay	nA, nB to nY; see Figure 6 ^[2]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.5	7.9	1.0	9.5	1.0	10.0	ns
		C _L = 50 pF	-	6.0	11.4	1.0	13.0	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.2	5.5	1.0	6.5	1.0	7.0	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; ^[3]	-	7.0	-	-	-	-	-	pF
		V _I = GND to V _{CC}								

Table 7. Dynamic characteristics ...continued
GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
For type 74AHCT00										
t _{pd}	propagation delay	nA, nB to nY; see Figure 6 ^[2]								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.3	6.9	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF	-	4.5	7.9	1.0	9.0	1.0	10.0	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} ^[3]	-	7.0	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\text{ V}$ and $V_{CC} = 5.0\text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

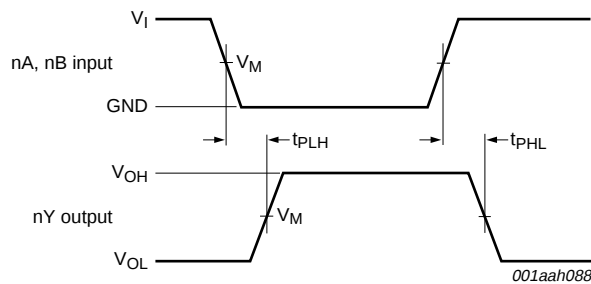
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input (nA, nB) to output (nY) propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC00	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT00	1.5 V	$0.5V_{CC}$

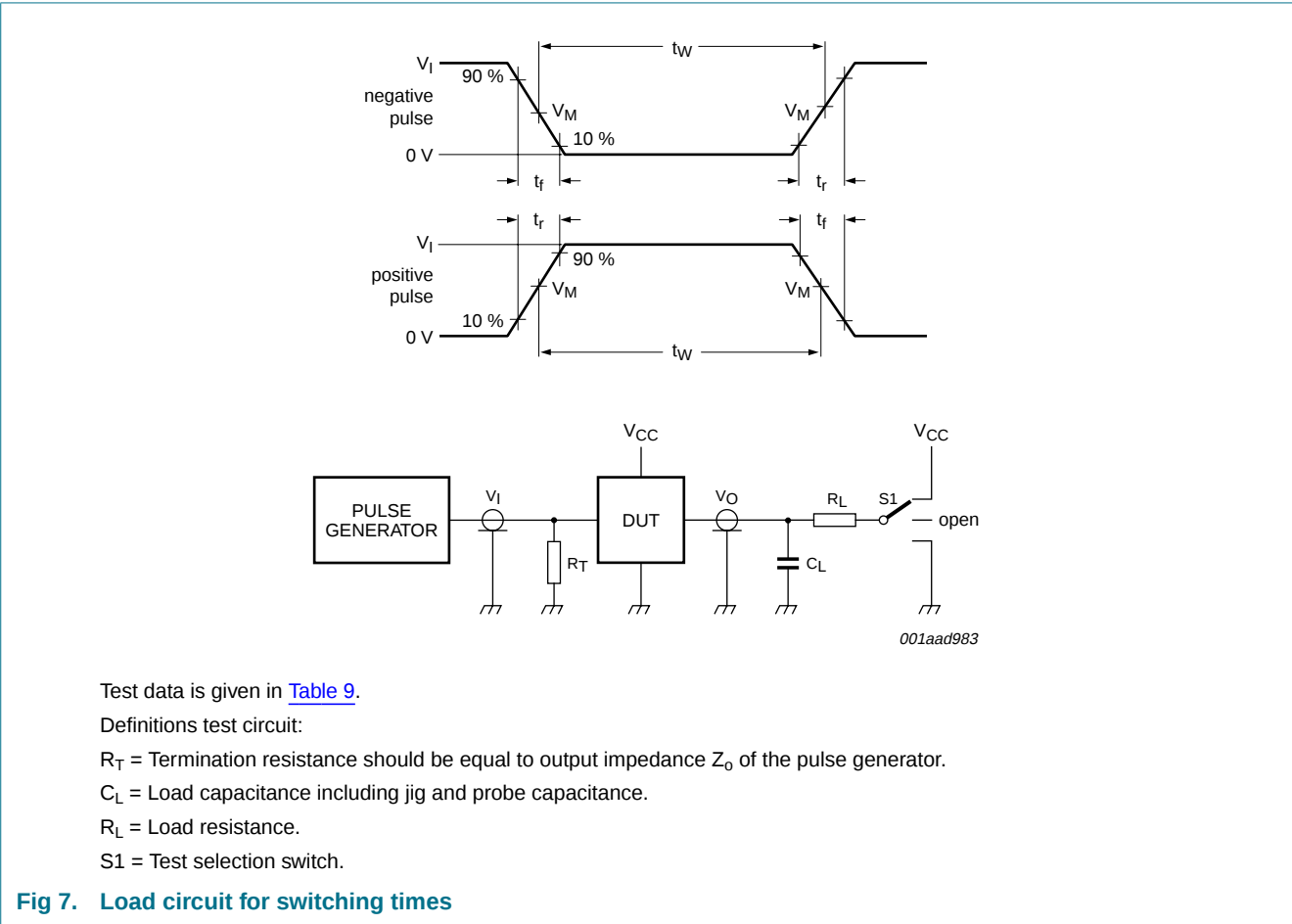


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC00	V_{CC}	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT00	3.0 V	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

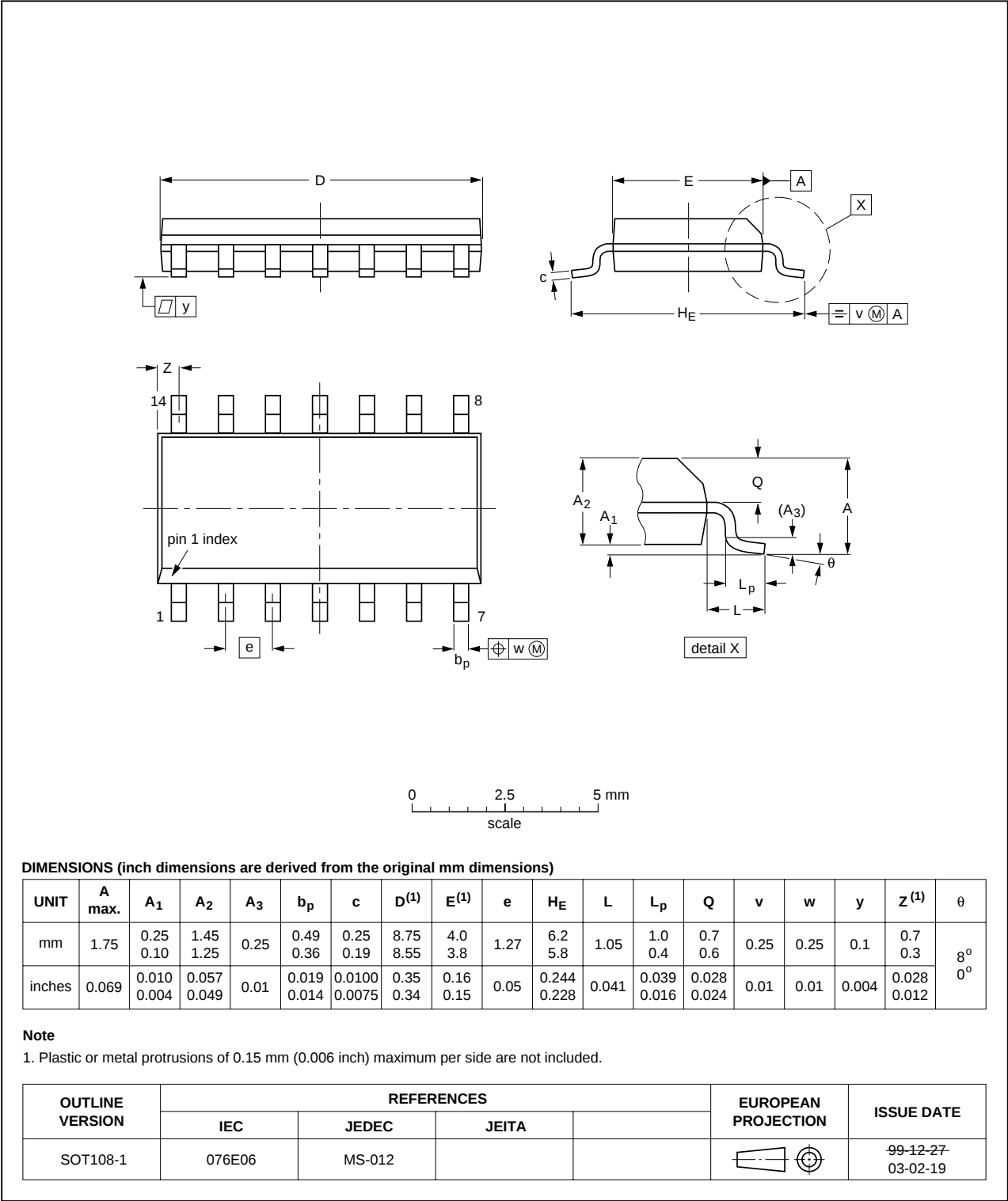
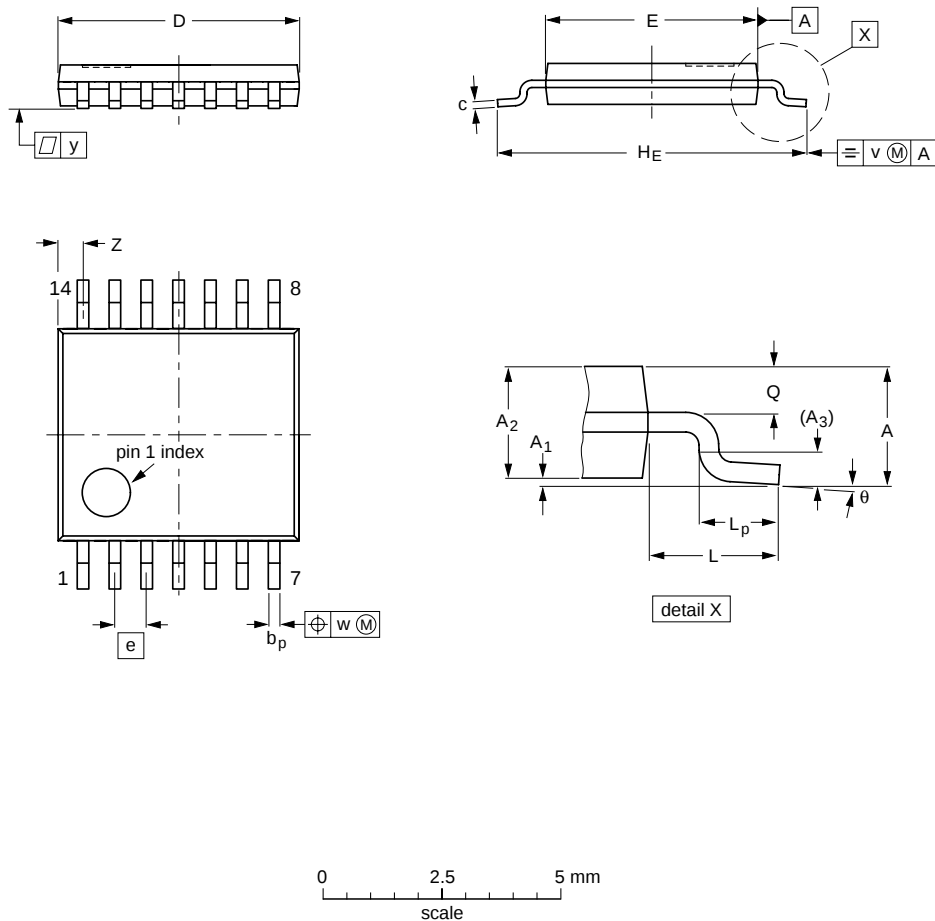


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

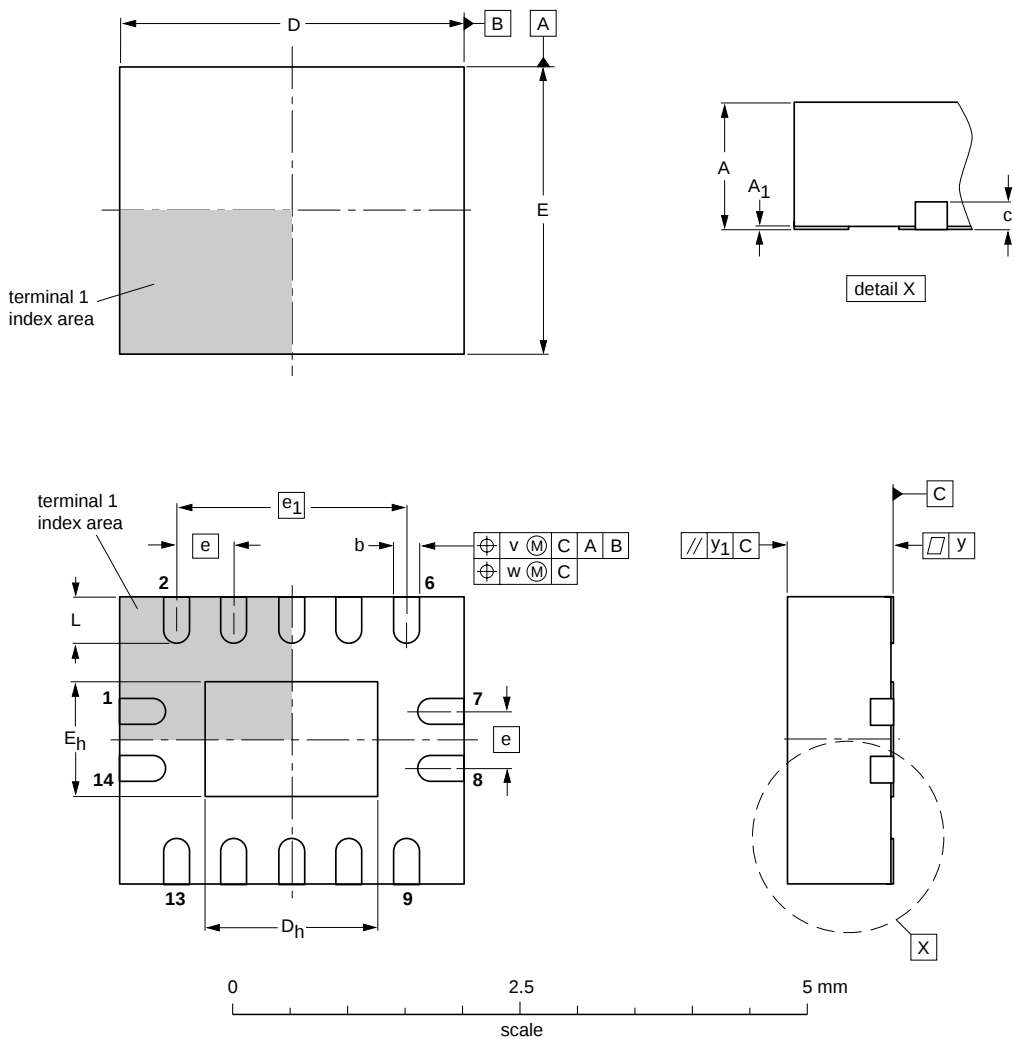
Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27 03-02-18

Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

Fig 10. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT00_3	20080108	Product data sheet	-	74AHC_AHCT00_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN14 package added. • Section 8: derating values added for DHVQFN14 package. • Section 12: outline drawing added for DHVQFN14 package.			
74AHC_AHCT00_2	19990923	Product specification	-	74AHC_AHCT00_1
74AHC_AHCT00_1	19981209	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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