

# DATA SHEET

**74ALS20A**

Dual 4-Input NAND gate

Product specification

1996 Jul 01

IC05 Data Handbook



# Dual 4-input NAND gate

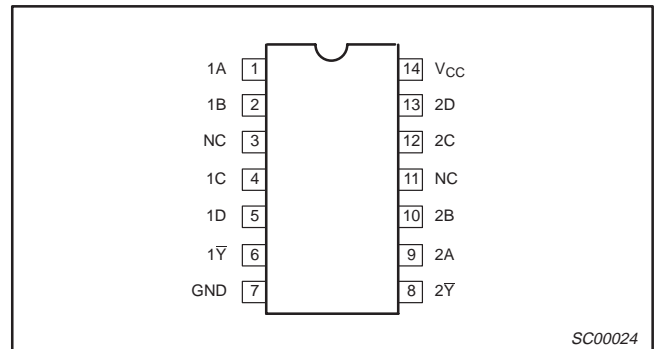
# 74ALS20A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS20A	4.5ns	0.65mA

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	
14-pin plastic DIP	74ALS20AN	SOT27-1
14-pin plastic SO	74ALS20AD	SOT108-1

### PIN CONFIGURATION

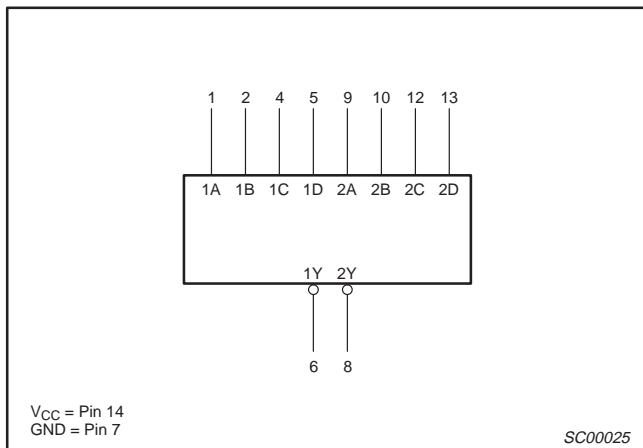


### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

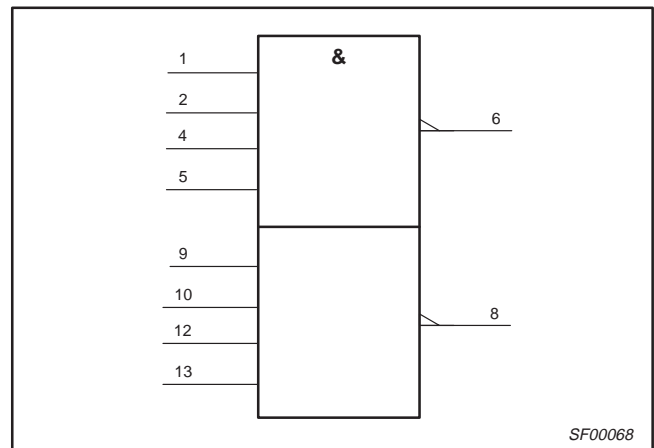
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC, nD	Data inputs	1.0/1.0	20 $\mu$ A/0.1mA
n $\bar{Y}$	Data outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20 $\mu$ A in the High state and 0.1mA in the Low state.

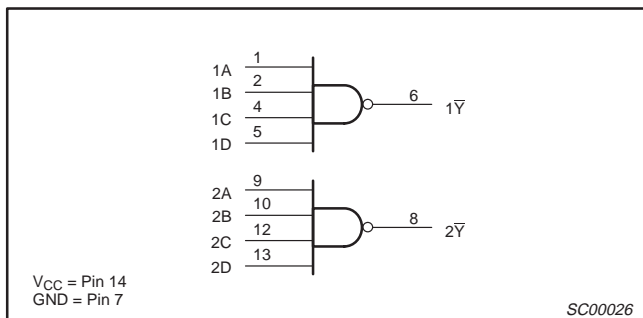
### LOGIC SYMBOL



### IEC/IEEE SYMBOL



### LOGIC DIAGRAM



### FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	n $\bar{Y}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

H = High voltage level  
 L = Low voltage level  
 X = Don't care

## Dual 4-input NAND gate

74ALS20A

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	16	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-0.4	mA
$I_{OL}$	Low-level output current			8	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
			MIN	TYP <sup>2</sup>	MAX	
$V_{OH}$	High-level output voltage	$V_{CC} \pm 10\%$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$ , $I_{OH} = -0.4\text{mA}$	$V_{CC} - 2$			V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$	$I_{OL} = 4\text{mA}$	0.25	0.40	V
			$I_{OL} = 8\text{mA}$	0.35	0.50	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = I_{IK}$		-0.73	-1.5	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 7.0\text{V}$			0.1	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$			20	μA
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.5\text{V}$			-0.1	mA
$I_O$	Output current <sup>3</sup>	$V_{CC} = \text{MAX}$ , $V_O = 2.25\text{V}$	-30		-112	mA
$I_{CC}$	Supply current (total)	$V_{CC} = \text{MAX}$	$V_I = 0\text{V}$	0.3	0.4	mA
			$V_I = 4.5\text{V}$	1.0	1.5	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current,  $I_{OS}$ .

# Dual 4-input NAND gate

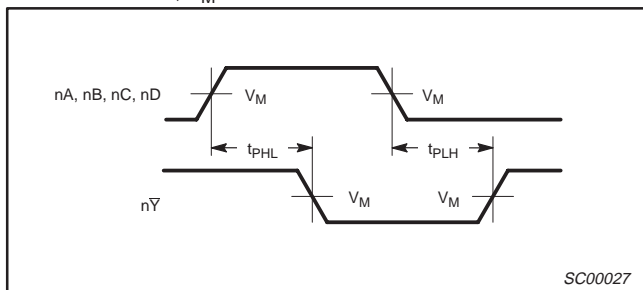
# 74ALS20A

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$		
			MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay nA, nB, nC, nD to nY	Waveform 1	2.0 3.0	11.0 10.0	ns

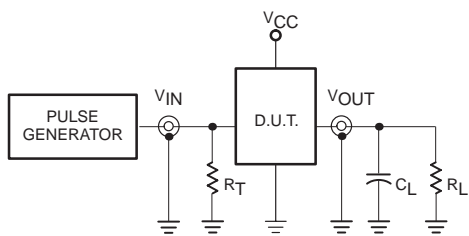
## AC WAVEFORMS

For all waveforms,  $V_M = 1.3\text{V}$ .

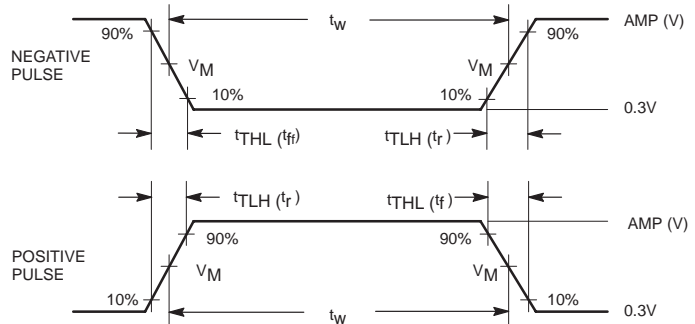


Waveform 1. Propagation Delay for Data to Output

## TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

### DEFINITIONS:

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

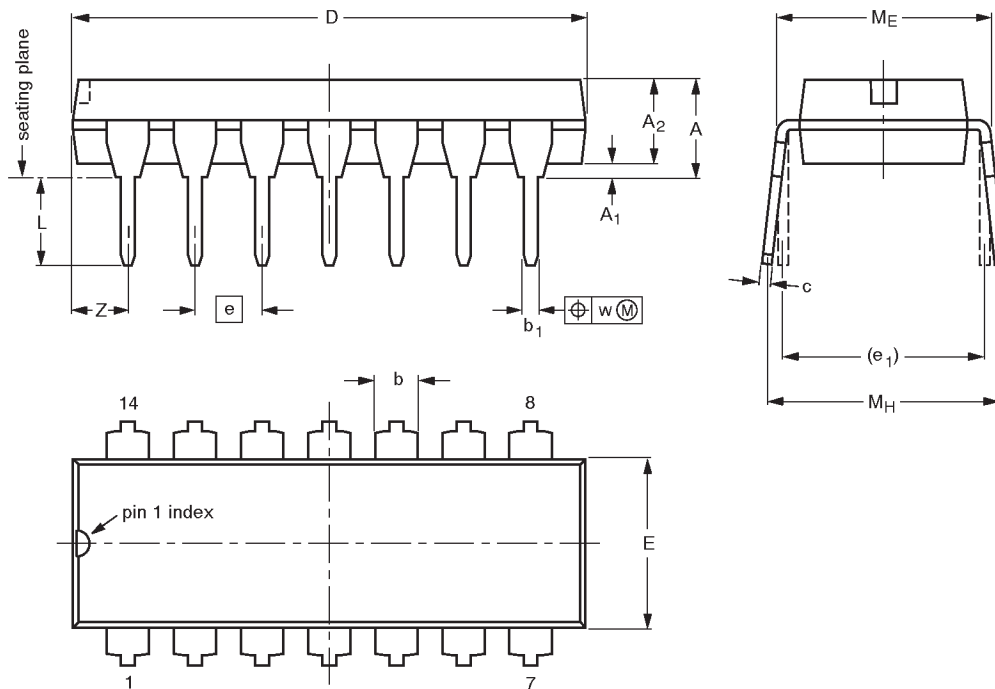
Family	INPUT PULSE REQUIREMENTS					
	Amplitude	$V_M$	Rep.Rate	$t_w$	$t_{TLH}$	$t_{THL}$
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

Dual 4-input NAND gate

74ALS20A

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

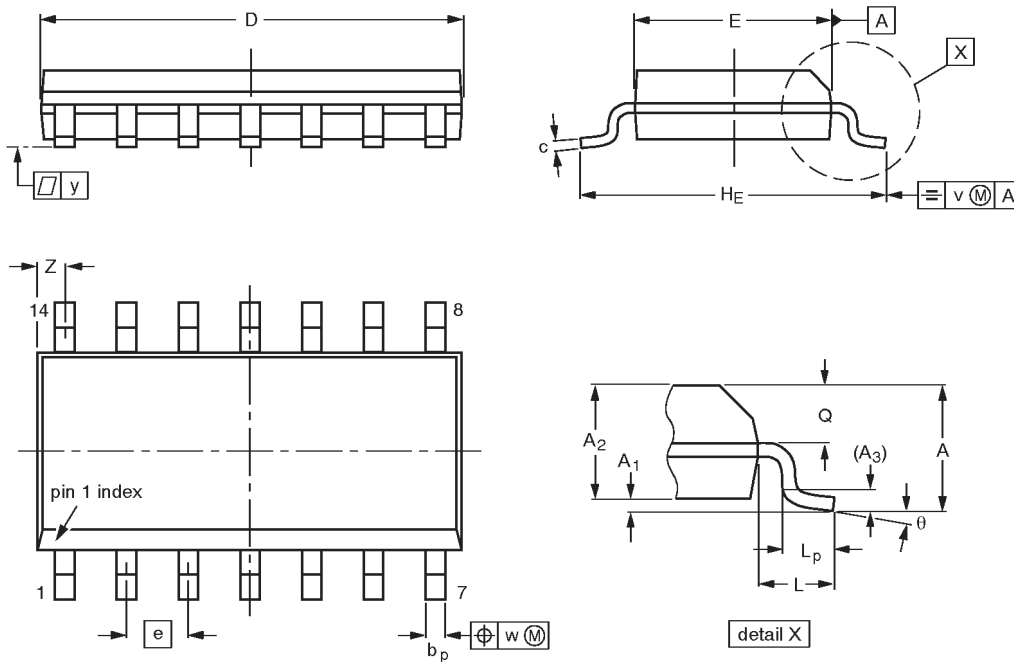
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

# Dual 4-input NAND gate

# 74ALS20A

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.45	1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.0039	0.0098 0.057	0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-13 95-01-23

## Dual 4-input NAND gate

74ALS20A

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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print code

Date of release: 05-96

Document order number:

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