

74AUP1G00

Low-power 2-input NAND gate

Rev. 02 — 29 June 2006

Product data sheet

1. General description

The 74AUP1G00 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Schmitt-trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial Power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74AUP1G00 provides the single 2-input NAND function.

2. Features

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - ◆ JESD8-12 (0.8 V to 1.3 V)
 - ◆ JESD8-11 (0.9 V to 1.65 V)
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114-C Class 3A. Exceeds 5000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101-C exceeds 1000 V
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AUP1G00GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AUP1G00GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AUP1G00GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891

4. Marking

Table 2. Marking

Type number	Marking code
74AUP1G00GW	pA
74AUP1G00GM	pA
74AUP1G00GF	pA

5. Functional diagram

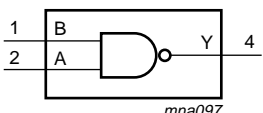


Fig 1. Logic symbol




Fig 2. IEC logic symbol

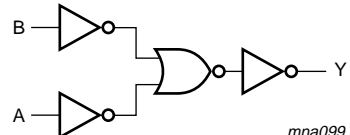


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

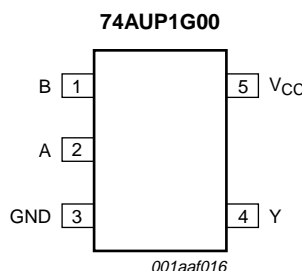


Fig 4. Pin configuration SOT353-1 (TSSOP5)

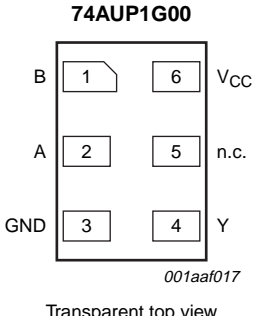


Fig 5. Pin configuration SOT886 (XSON6)

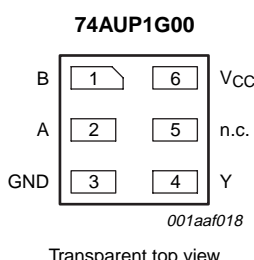


Fig 6. Pin configuration SOT891 (XSON6)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5	XSON6	
B	1	1	data input B
A	2	2	data input A
GND	3	3	ground (0 V)
Y	4	4	data output Y
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output	
A	B	Y	
L	L	H	
L	H	H	
H	L	H	
H	H	L	

- [1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-	-50	mA
V _I	input voltage		^[1] -0.5	+4.6	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	Active mode	^[1] -0.5	V _{CC} + 0.5	V
		Power-down mode	^[1] -0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CC}	-	±20	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-	-50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[2] -	250	mW

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For TSSOP5 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
V_{IH}	HIGH-state input voltage	$V_{CC} = 0.8$ V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 0.8$ V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1$ mA; $V_{CC} = 1.1$ V	$0.75 \times V_{CC}$	-	-	V
		$I_O = -1.7$ mA; $V_{CC} = 1.4$ V	1.11	-	-	V
		$I_O = -1.9$ mA; $V_{CC} = 1.65$ V	1.32	-	-	V
		$I_O = -2.3$ mA; $V_{CC} = 2.3$ V	2.05	-	-	V
		$I_O = -3.1$ mA; $V_{CC} = 2.3$ V	1.9	-	-	V
		$I_O = -2.7$ mA; $V_{CC} = 3.0$ V	2.72	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.1	V
		$I_O = 1.1$ mA; $V_{CC} = 1.1$ V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7$ mA; $V_{CC} = 1.4$ V	-	-	0.31	V
		$I_O = 1.9$ mA; $V_{CC} = 1.65$ V	-	-	0.31	V
		$I_O = 2.3$ mA; $V_{CC} = 2.3$ V	-	-	0.31	V
		$I_O = 3.1$ mA; $V_{CC} = 2.3$ V	-	-	0.44	V
		$I_O = 2.7$ mA; $V_{CC} = 3.0$ V	-	-	0.31	V
	$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	-	-	0.44	V	

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	$V_I = \text{GND to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	± 0.1	μA
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	± 0.2	μA
ΔI_{OFF}	additional power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	± 0.2	μA
I_{CC}	supply current	$V_I = \text{GND or } V_{CC}; I_O = 0 \text{ A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.5	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	1 -	-	40	μA
C_I	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V}; V_I = \text{GND or } V_{CC}$	-	0.8	-	pF
C_O	output capacitance	$V_O = \text{GND}; V_{CC} = 0 \text{ V}$	-	1.7	-	pF
$T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-state input voltage	$V_{CC} = 0.8 \text{ V}$	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 0.8 \text{ V}$	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -20 \mu\text{A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.7 \times V_{CC}$	-	-	V
		$I_O = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.03	-	-	V
		$I_O = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.30	-	-	V
		$I_O = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.97	-	-	V
		$I_O = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.85	-	-	V
		$I_O = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.67	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 20 \mu\text{A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.1	V
		$I_O = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.37	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.35	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_O = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.33	V
I_I	input leakage current	$V_I = \text{GND to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	± 0.5	μA
		$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	± 0.5	μA
ΔI_{OFF}	additional power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	± 0.6	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	$V_I = \text{GND or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.9	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	[1]	-	50	μA
$T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-state input voltage	$V_{CC} = 0.8 \text{ V}$	$0.75 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 0.8 \text{ V}$	-	-	$0.25 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -20 \mu\text{A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.11$	-	-	V
		$I_O = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.6 \times V_{CC}$	-	-	V
		$I_O = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	0.93	-	-	V
		$I_O = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.17	-	-	V
		$I_O = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.77	-	-	V
		$I_O = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.67	-	-	V
		$I_O = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.40	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 20 \mu\text{A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.11	V
		$I_O = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.33 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.41	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.39	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.36	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.50	V
		$I_O = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
I_I	input leakage current	$V_I = \text{GND to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	± 0.75	μA
		$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	± 0.75	μA
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	± 0.75	μA
ΔI_{OFF}	additional power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	± 0.75	μA
I_{CC}	supply current	$V_I = \text{GND or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	1.4	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	[1]	-	75	μA

[1] One input at $V_{CC} - 0.6 \text{ V}$, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#)

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = 25 °C; C_L = 5 pF						
t _{PHL} , t _{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7				
		V _{CC} = 0.8 V	-	17.5	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.5	5.3	11.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.0	3.8	6.8	ns
		V _{CC} = 1.65 V to 1.95 V	1.6	3.1	5.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.3	2.5	4.0	ns
T_{amb} = 25 °C; C_L = 10 pF						
t _{PHL} , t _{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7				
		V _{CC} = 0.8 V	-	21.0	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.4	6.1	13.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.4	4.4	7.9	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	3.7	6.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	3.0	4.7	ns
T_{amb} = 25 °C; C_L = 15 pF						
t _{PHL} , t _{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7				
		V _{CC} = 0.8 V	-	24.5	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.4	6.9	14.8	ns
		V _{CC} = 1.4 V to 1.6 V	2.8	5.0	8.9	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	4.1	7.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	3.5	5.3	ns
T_{amb} = 25 °C; C_L = 30 pF						
t _{PHL} , t _{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7				
		V _{CC} = 0.8 V	-	34.8	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.6	9.2	20.1	ns
		V _{CC} = 1.4 V to 1.6 V	3.0	6.5	11.8	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	5.4	9.3	ns
		V _{CC} = 2.3 V to 2.7 V	2.4	4.6	7.1	ns
T_{amb} = 25 °C; C_L = 30 pF						
t _{PHL} , t _{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	V _{CC} = 3.0 V to 3.6 V	2.3	4.3	6.5	ns

Table 8. Dynamic characteristics ...continued
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#)

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = 25 °C						
C _{PD}	power dissipation capacitance	f = 1 MHz; V _I = GND to V _{CC} [2]				
		V _{CC} = 0.8 V	-	2.6	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.8	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	2.9	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	3.1	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.6	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	4.2	-	pF

- [1] All typical values are measured at nominal V_{CC}.
- [2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

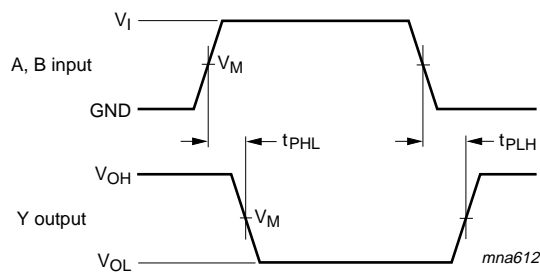
Table 9. Dynamic characteristics
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#)

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
C_L = 5 pF							
t _{PHL} , t _{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7					
		V _{CC} = 1.1 V to 1.3 V	2.1	12.2	2.1	13.5	ns
		V _{CC} = 1.4 V to 1.6 V	1.8	7.8	1.8	8.6	ns
		V _{CC} = 1.65 V to 1.95 V	1.4	6.2	1.4	6.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.1	4.7	1.1	5.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	4.2	1.0	4.7	ns
C_L = 10 pF							
t _{PHL} , t _{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7					
		V _{CC} = 1.1 V to 1.3 V	2.2	14.4	2.2	15.9	ns
		V _{CC} = 1.4 V to 1.6 V	2.2	9.2	2.2	10.2	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	7.3	1.9	8.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.3	5.6	1.3	6.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	4.9	1.2	5.4	ns

Table 9. Dynamic characteristics ...continued
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#)

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$C_L = 15\text{ pF}$							
t_{PHL} , t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7					
		$V_{CC} = 1.1\text{ V to }1.3\text{ V}$	3.1	16.5	3.1	18.2	ns
		$V_{CC} = 1.4\text{ V to }1.6\text{ V}$	2.5	10.5	2.5	11.6	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.0	8.3	2.0	9.2	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.5	6.4	1.5	7.1	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.4	5.7	1.4	6.3	ns
$C_L = 30\text{ pF}$							
t_{PHL} , t_{PLH}	HIGH-to-LOW and LOW-to-HIGH propagation delay A or B to Y	see Figure 7					
		$V_{CC} = 1.1\text{ V to }1.3\text{ V}$	4.1	22.6	4.1	24.9	ns
		$V_{CC} = 1.4\text{ V to }1.6\text{ V}$	2.9	14.0	2.9	15.4	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.3	11.1	2.3	12.3	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.1	8.5	2.1	9.4	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.1	7.6	2.1	8.4	ns

12. Waveforms

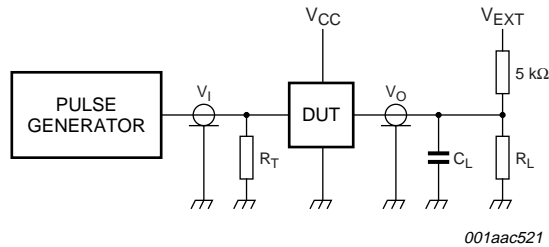


Measurement points are given in [Table 10](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 7. The data input (A or B) to output (Y) propagation delays

Table 10. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	$\leq 3.0\text{ ns}$



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Load circuitry for switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5 \text{ k}\Omega$, for measuring propagation delays, setup and hold times and pulse width $R_L = 1 \text{ M}\Omega$.

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

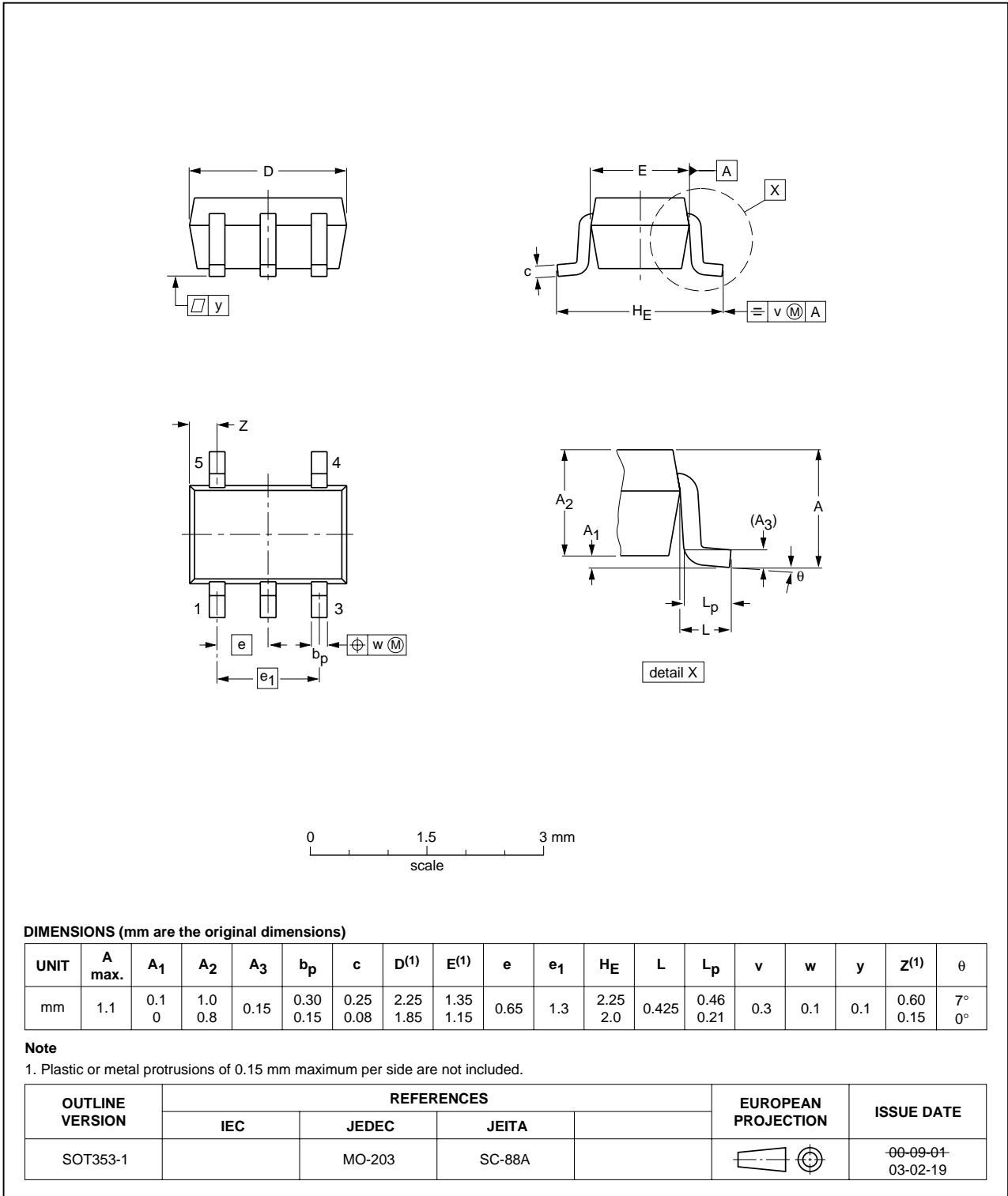


Fig 9. Package outline SOT353-1 (TSSOP5)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

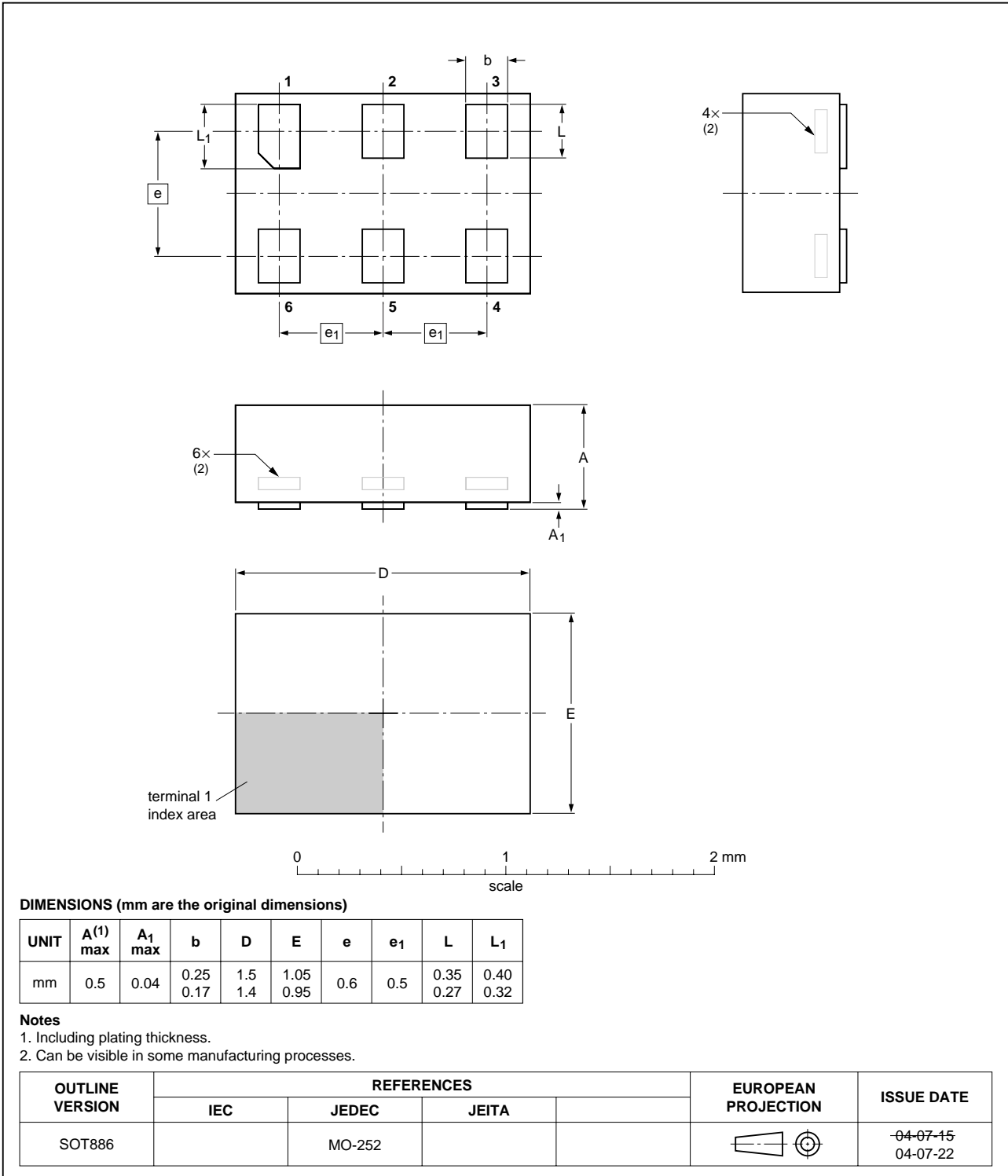


Fig 10. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

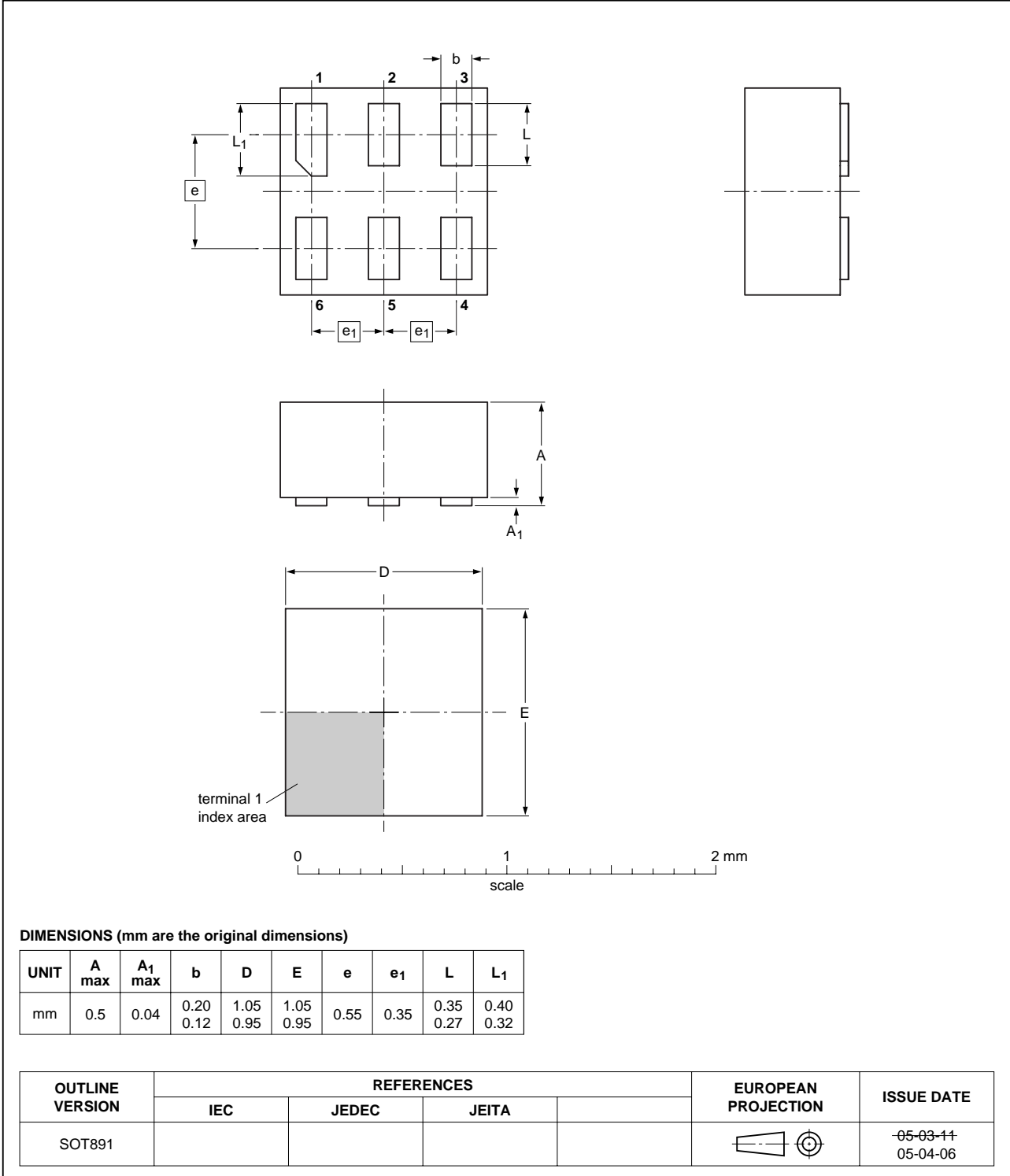


Fig 11. Package outline SOT891 (XSON6)

14. Abbreviations

Table 12: Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor Transistor Logic

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G00_2	20060629	Product data sheet	-	74AUP1G00_1
Modifications:	<ul style="list-style-type: none">• ESD HBM and C_{PD} values modified in Section 2, Table 8• Added type number 74AUP1G00GF (XSON6/SOT891) package			
74AUP1G00_1	20050711	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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