FAIRCHILD SEMICONDUCTOR™

September 1986
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DM74ALS245A
Octal 3-STATE Bus Transceiver

General Description

This advanced low power Schottky device contains 8 pairs of 3-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data transmits either from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode so that the buses are effectively isolated.

Features

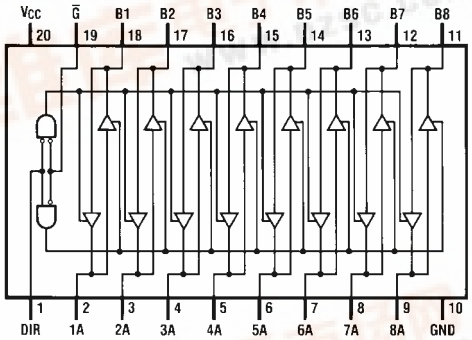
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Non-inverting logic output
- Glitch free bus during power up and down
- 3-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$
- PNP inputs to reduce input loading
- Switching specifications guaranteed over full temperature and V_{CC} range

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS245AWM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74ALS245ASJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS245AMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS245AN	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

H = HIGH Logic Level
L = LOW Logic Level
X = Either HIGH or LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	53.0°C/W
M Package	72.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Operating Free Air Temperature	0		70	°C

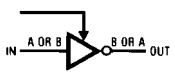
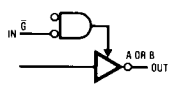
Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA					−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA			2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max			2	2.3		V
		I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V			V_{CC} − 2			V
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 24 mA			0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V	V_{IN} = 7V	Control Inputs			0.1	mA
			V_{IN} = 5.5V	A or B Ports			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V					20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V					−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V			−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs HIGH			30	45	mA
			Outputs LOW			36	55	mA
			3-STATE			38	58	mA

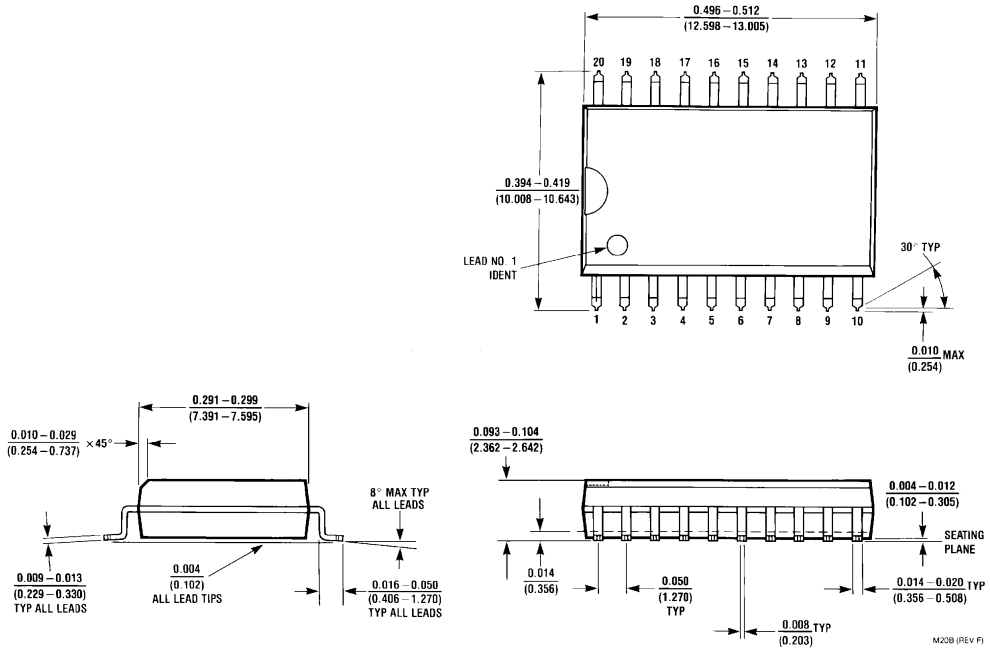
Switching Characteristics (Note 2)

over recommended operating free air temperature range

Symbol	Parameter	Circuit Configuration	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		3	10	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		3	10	ns
t_{PZL}	Output Enable Time to LOW Level		5	20	ns
t_{PZH}	Output Enable Time to HIGH Level		5	20	ns
t_{PLZ}	Output Disable Time from LOW Level		4	15	ns
t_{PHZ}	Output Disable Time from HIGH Level		2	10	ns

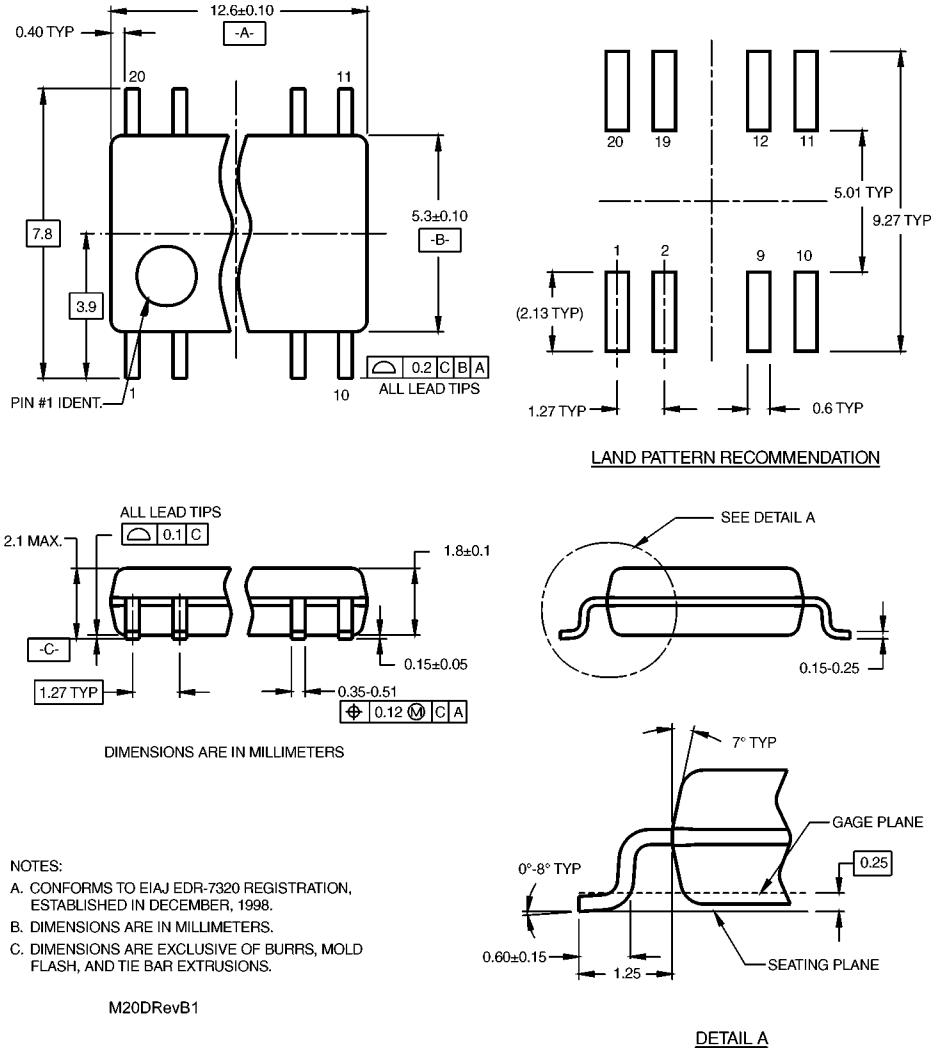
Note 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF.

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

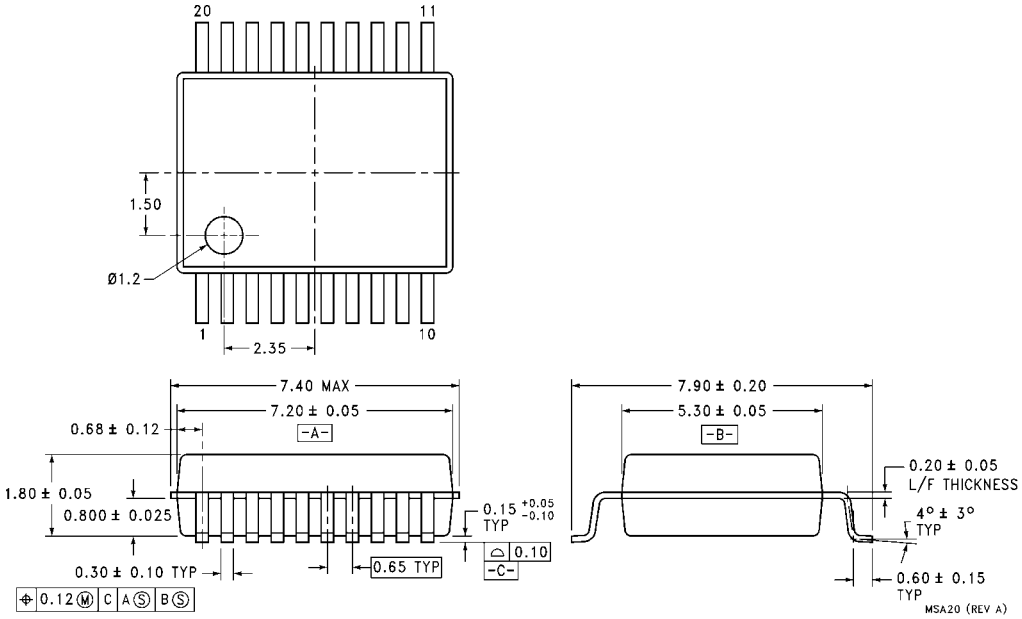
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

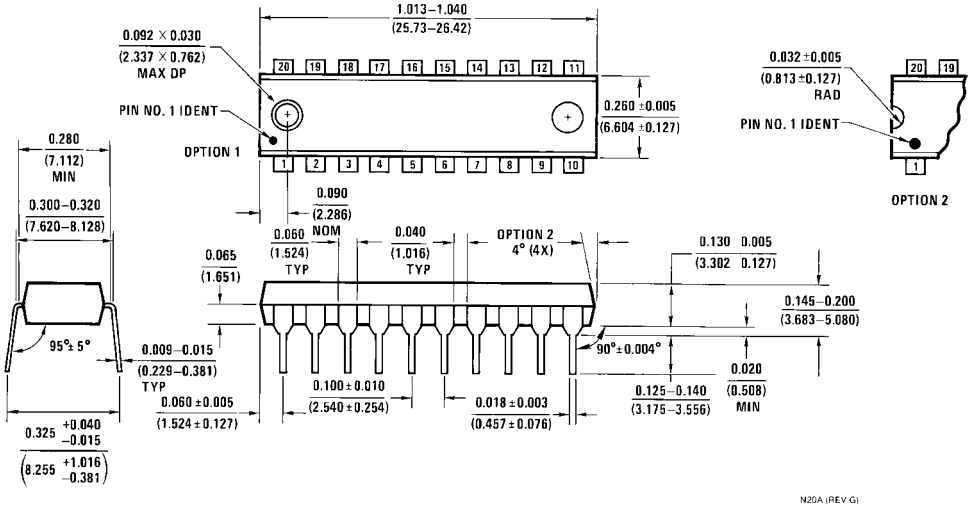
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A