National Semiconductor

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74ABT16952
16-Bit Registered Transceiver with TRI-STATE® Outputs

General Description

The 'ABT16952 is a 16-bit registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and TRI-STATE® output enable signals are provided for each register. The output pins are guaranteed to source 32 mA (24 mA mil.) and to sink 64 mA (48 mA mil).

Features

- Separate clock, clock enable and TRI-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Commercial	Package Number	Package Description
74ABT16952CSSC (Note 1)	MS56A	56-Lead (0.300″ Wide) Molded Shrink Small Outline, JEDEC (SSOP)
74ABT16952CMTD (Notes 1, 2)	MTD56	56-Lead Molded Thin Shrink Small Outline, JEDEC (TSSOP)

Note 1: Devices also available in 13″ reel. Use suffix = SSCX and MTDX.

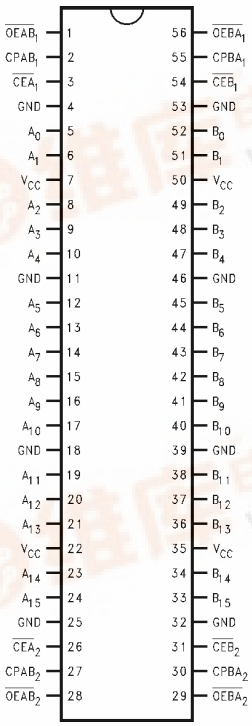
Note 2: Contact factory for package availability.

Pin Descriptions

Pin Names	Description
A_0–A_{16}	Data Register A Inputs/ B-Register TRI-STATE Outputs
B_0–B_{16}	Data Register B Inputs/ A-Register TRI-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
$\overline{CEA}_n$, $\overline{CEB}_n$	Clock Enable
$\overline{OEAB}_n$, $\overline{OEBA}_n$	Output Enable Inputs

Connection Diagram

Pin Assignment for SSOP



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Pin Descriptions (Continued)

Output Control

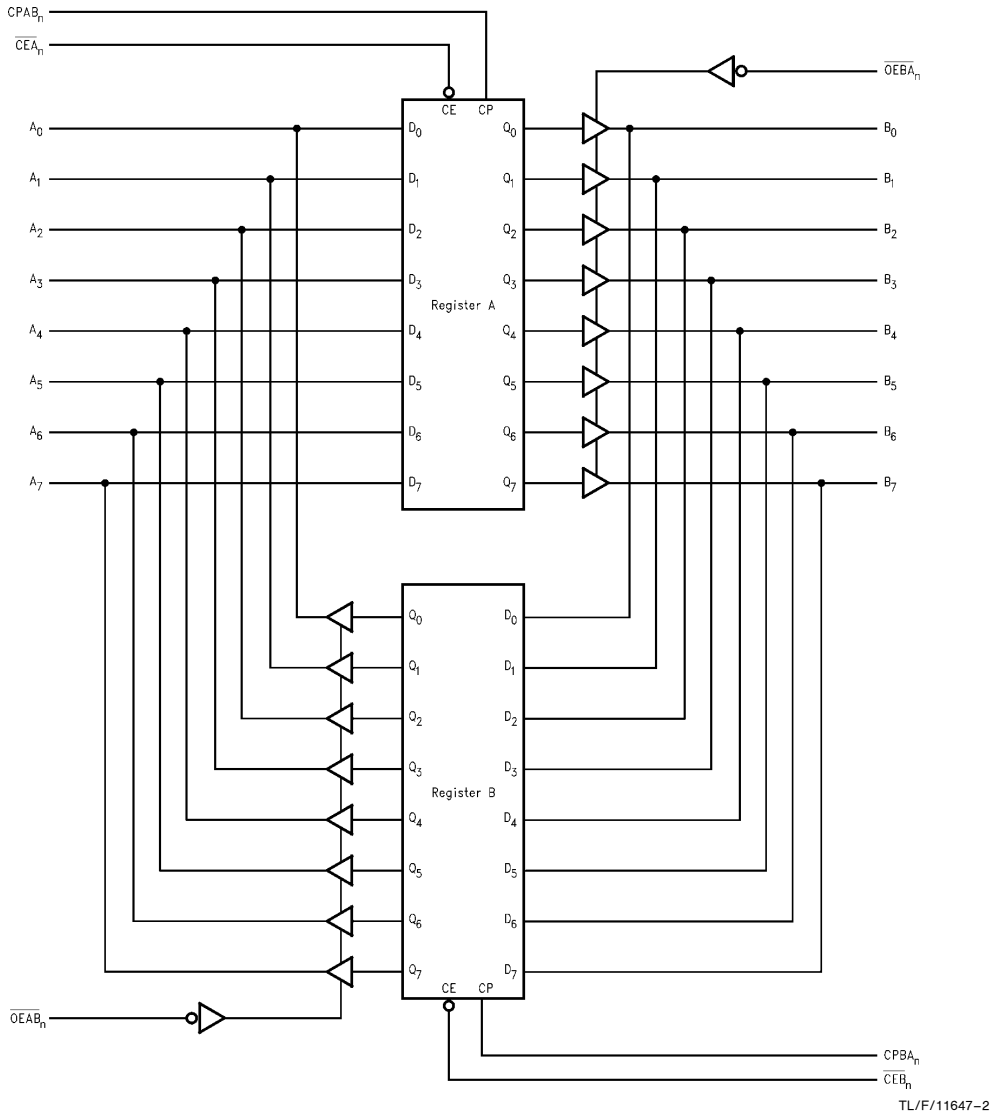
$\overline{OE}$	Internal Q	Output	Function
H	X	Z	Disable Outputs
L L	L H	L H	Enable Outputs

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
⌐‾ = LOW-to-HIGH Transition
NC = No Change

Register Function Table (Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L H	⌐‾ ⌐‾	L L	L H	Load Data

Block Diagram



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n for either byte 1 or byte 2

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	−40°C to +85°C
Supply Voltage	
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT16952 Min	ABT16952 Typ	ABT16952 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 74ABT	2.5					I_{OH} = −3 mA (A_n, B_n)
	74ABT	2.0					I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage 74ABT			0.55			I_{OL} = 64 mA (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 2) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	μA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 2) V_{IN} = 0.0V (Non-I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current			50	μA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
$I_{IL} + I_{OZL}$	Output Leakage Current			−50	μA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			1.0	mA	Max	Outputs TRI-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V; All Others at V_{CC} or GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT16952			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{CCD}	Dynamic I_{CC} No Load (Note 2)			0.18	mA/MHz	Max	Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND, Non-I/O = GND or V_{CC} One Bit toggling, 50% duty cycle (Note 1)

Note 1: For 8-bit toggling, $I_{CCD} < 1.4$ mA/MHz.

Note 2: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ABT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		Units
		Min	Max	Min	Max	
f_{max}	Max Clock Frequency	200		200		MHz
t_{PLH} t_{PHL}	Propagation Delay $CPAB_n$ or $CPBA_n$ to A_n or B_n	1.5 1.5	5.3 5.3	1.5 1.5	5.3 5.3	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEAB}_n$ or $\overline{OEBA}_n$ to A_n or B_n	1.5 1.5	5.5 5.5	1.5 1.5	5.5 5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEAB}_n$ or $\overline{OEBA}_n$ to A_n or B_n	1.5 1.5	6.0 6.0	1.5 1.5	6.0 6.0	ns

AC Operating Requirements

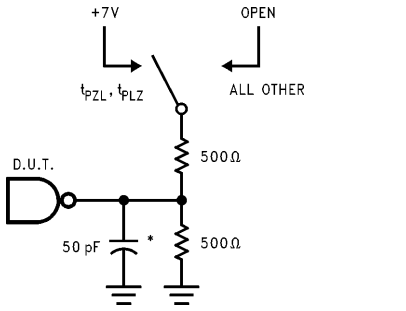
Symbol	Parameter	74ABT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		74ABT $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	2.5 2.5		2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	1.5 1.5		1.5 1.5		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEA}_n$ or $\overline{CEB}_n$ to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	2.5 2.5		2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEA}_n$ or $\overline{CEB}_n$ to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	1.5 1.5		1.5 1.5		ns
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	3.0 3.0		3.0 3.0		ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ (Non I/O Pins)
$C_{I/O}$ (Note 1)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

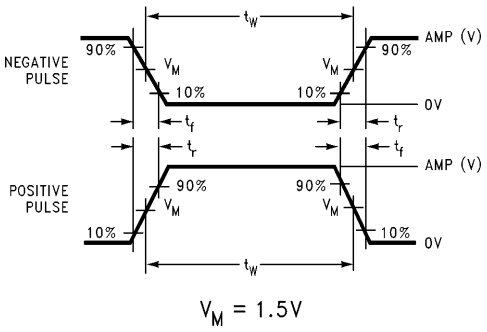

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FIGURE 2a. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Input Signal Requirements

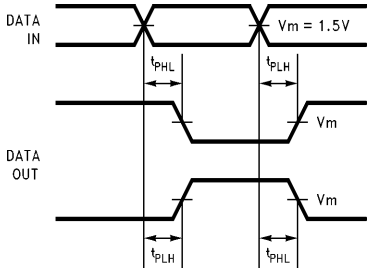

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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inveting Functions

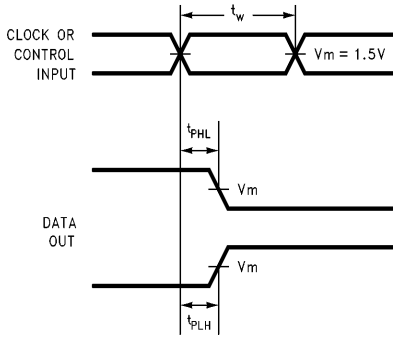

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FIGURE 4. Propagation Delay, Pulse Width Waveforms

AC Loading (Continued)

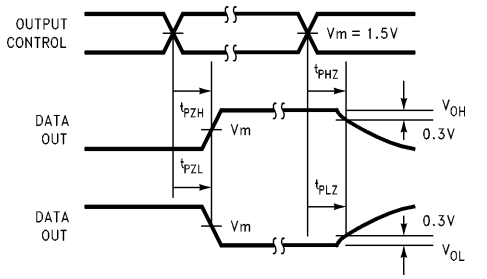


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

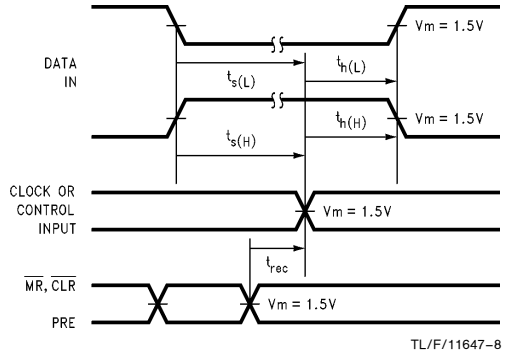
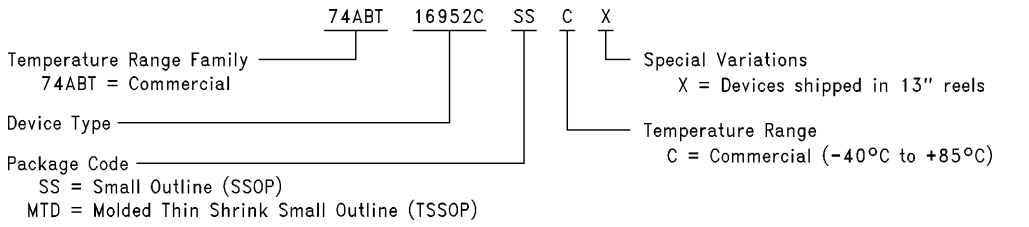


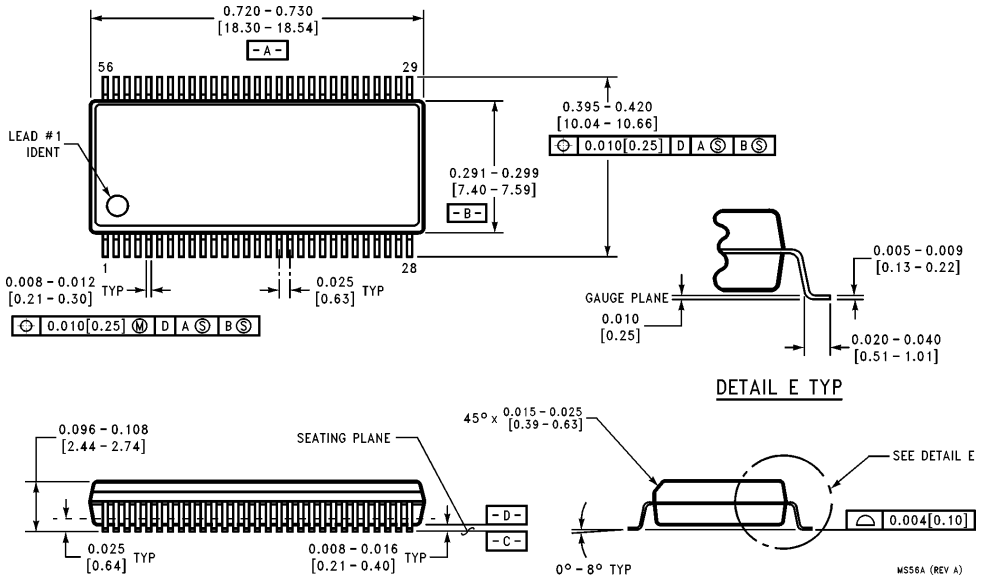
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

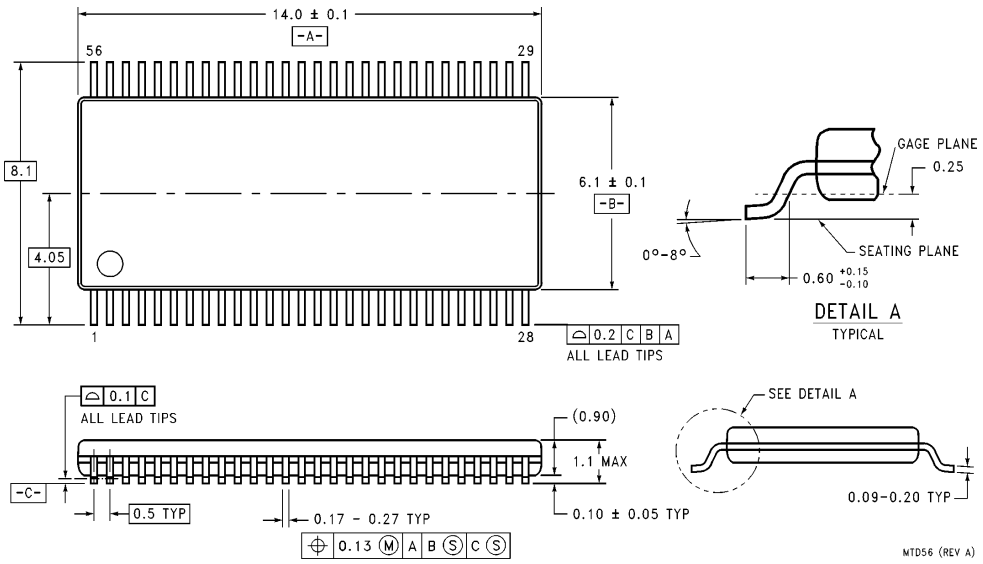


Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead SSOP (0.300″ Wide) (SS)
74ABT16952CSSC or 74ABT16952CSSCX
NS Package Number MS56A

Physical Dimensions millimeters (Continued)



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
74ABT16952CMTD
NS Package Number MTD56

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408