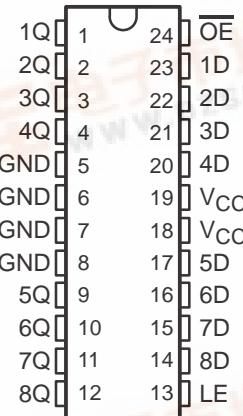


- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (NT)

DB, DW, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit latch features 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 74AC11373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

\overline{OE} can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 74AC11373 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each latch)

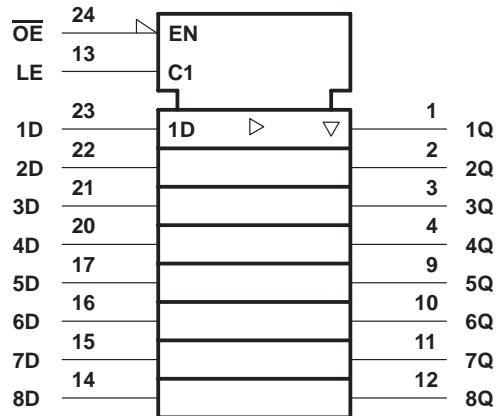
INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

 Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

74AC11373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

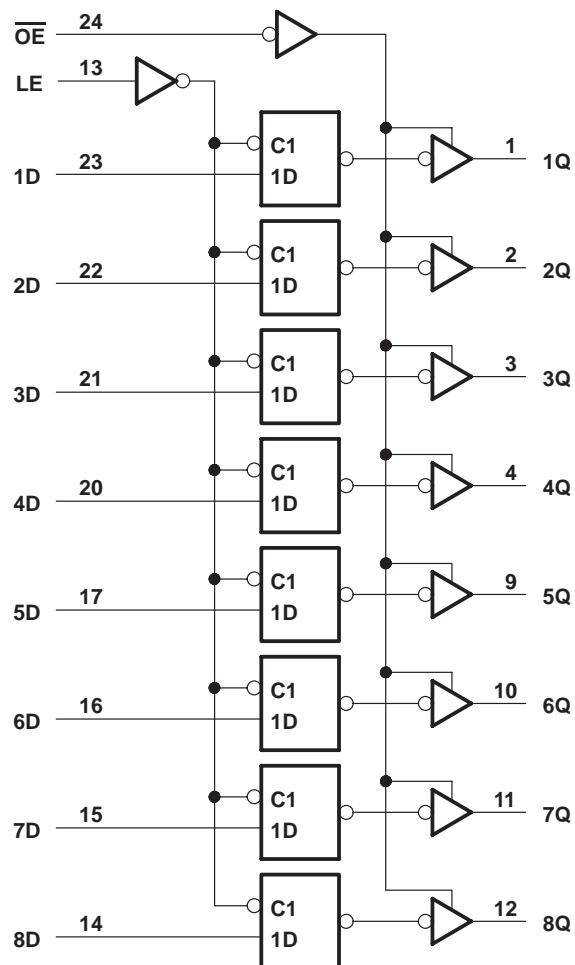
SCAS213A – MAY 1987 – REVISED APRIL 1996

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



74AC11373
**OCTAL TRANSPARENT D-TYPE LATCH
 WITH 3-STATE OUTPUTS**

SCAS213A – MAY 1987 – REVISED APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input voltage range, V_I (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.65 W
	DW package
	NT package
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current	$V_{CC} = 3$ V		–4	mA
		$V_{CC} = 4.5$ V		–24	
		$V_{CC} = 5.5$ V		–24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	\overline{OE}	0	5	ns/V
		Data, LE	0	10	
T_A	Operating free-air temperature	–40	85		°C

74AC11373
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCAS213A – MAY 1987 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 µA	3 V	2.9		2.9	V		
		4.5 V	4.4		4.4			
		5.5 V	5.4		5.4			
	I _{OH} = -4 mA	3 V	2.58		2.48			
		4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	I _{OH} = -24 mA	5.5 V			3.85			
		3 V						
		4.5 V						
	I _{OH} = -75 mA [†]	5.5 V						
		3 V						
		4.5 V						
V _{OL}	I _{OL} = 50 µA	5.5 V		0.1	0.1	V		
		4.5 V		0.1	0.1			
		3 V		0.1	0.1			
	I _{OL} = 12 mA	5.5 V		0.36	0.44			
		4.5 V		0.36	0.44			
		3 V		0.36	0.44			
	I _{OL} = 24 mA	5.5 V		0.36	0.44			
		4.5 V		0.36	0.44			
		3 V		0.36	0.44			
	I _{OL} = 75 mA [†]	5.5 V			1.65			
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5	±5	µA		
I _I	V _I = V _{CC} or GND	5.5 V		±0.1	±1	µA		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8	80	µA		
C _i	V _I = V _{CC} or GND	5 V		4		pF		
C _o	V _O = V _{CC} or GND	5 V		10		pF		

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _W	Pulse duration, LE high	5.5		5.5		ns
t _{su}	Setup time, data before LE↓	4		4		ns
t _h	Hold time, data after LE↓	2		2		ns

timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _W	Pulse duration, LE high	4		4		ns
t _{su}	Setup time, data before LE↓	3.5		3.5		ns
t _h	Hold time, data after LE↓	2		2		ns

74AC11373
**OCTAL TRANSPARENT D-TYPE LATCH
 WITH 3-STATE OUTPUTS**
 SCAS213A – MAY 1987 – REVISED APRIL 1996

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
tPLH	D	Q	1.5	9	13.1	1.5	14.8	ns
tPHL			1.5	8	10.6	1.5	11.7	
tPLH	LE	Any Q	1.5	10	14.5	1.5	16.3	ns
tPHL			1.5	9.5	12.8	1.5	14.2	
tPZH	OE	Any Q	1.5	9	13.1	1.5	14.7	ns
tPZL			1.5	8.5	11.6	1.5	13.1	
tPHZ	\overline{OE}	Any Q	1.5	9.5	12	1.5	12.7	ns
tPLZ			1.5	7.5	10.2	1.5	10.8	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
tPLH	D	Q	1.5	6	8.9	1.5	10.3	ns
tPHL			1.5	5.5	7.6	1.5	8.4	
tPLH	LE	Any Q	1.5	6.5	10	1.5	11.3	ns
tPHL			1.5	6.5	9.1	1.5	10.2	
tPZH	\overline{OE}	Any Q	1.5	6.5	9.5	1.5	10.8	ns
tPZL			1.5	6	8.6	1.5	9.7	
tPHZ	\overline{OE}	Any Q	1.5	8.5	10.6	1.5	11.1	ns
tPLZ			1.5	6	8.2	1.5	8.7	

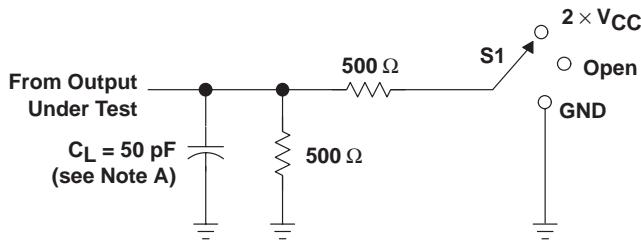
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	47	pF
		Outputs disabled		36	

74AC11373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

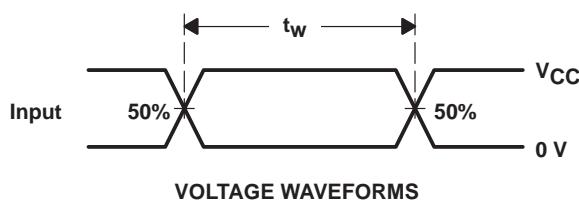
SCAS213A – MAY 1987 – REVISED APRIL 1996

PARAMETER MEASUREMENT INFORMATION

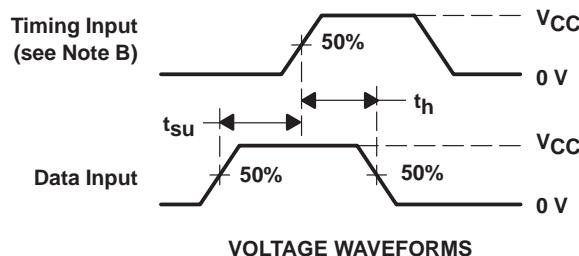


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

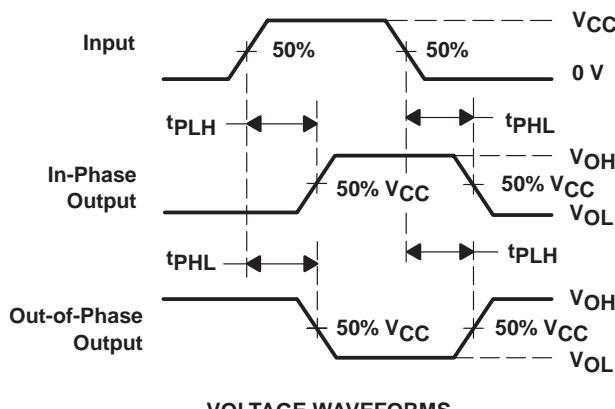
LOAD CIRCUIT



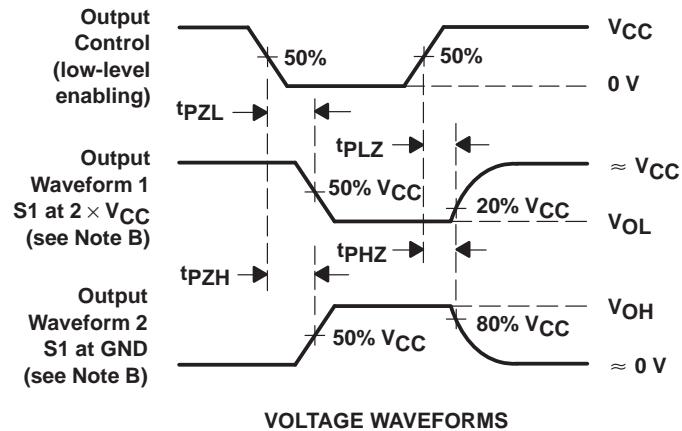
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.