

Philips Components—Signetics

Document No.	853-1514
ECN No.	00732
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11827

10-wide buffer/line driver (3-State)

FEATURES

- 3-State buffers
- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11827 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11827 device is a 10-wide buffer/line driver and provides high performance bus interface buffering for wide data/address paths or busses carrying parity. It has NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}$; GND = 0V; $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to Y_n	$C_L = 50\text{pF}$	5.8	6.6	ns
C_{PD}	Power dissipation capacitance per buffer ¹	$f = 1\text{MHz}$; Enabled $C_L = 50\text{pF}$ Disabled	35 9	35 10	pF
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4.5	4.5	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} ; Disabled	12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

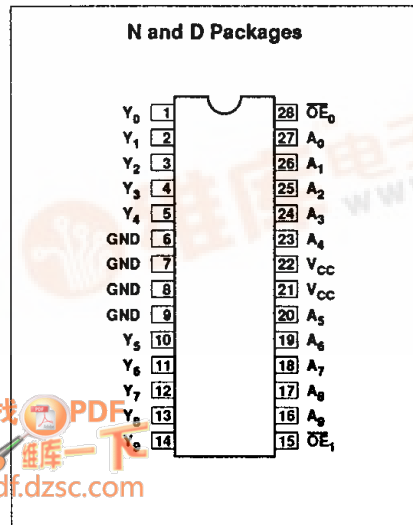
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

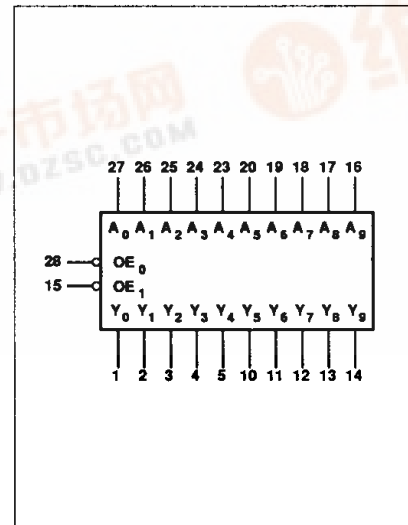
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11827N 74ACT11827N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11827D 74ACT11827D

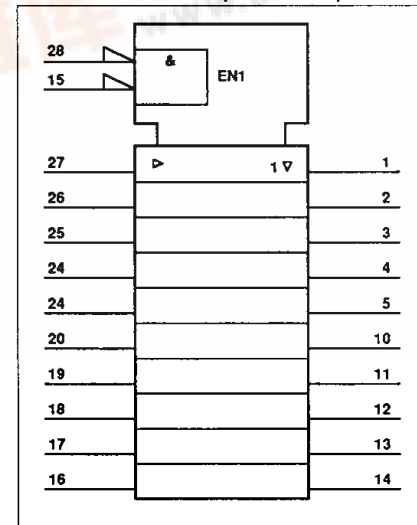
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



10-wide buffer/line driver (3-State)

74AC/ACT11827

PIN DESCRIPTION

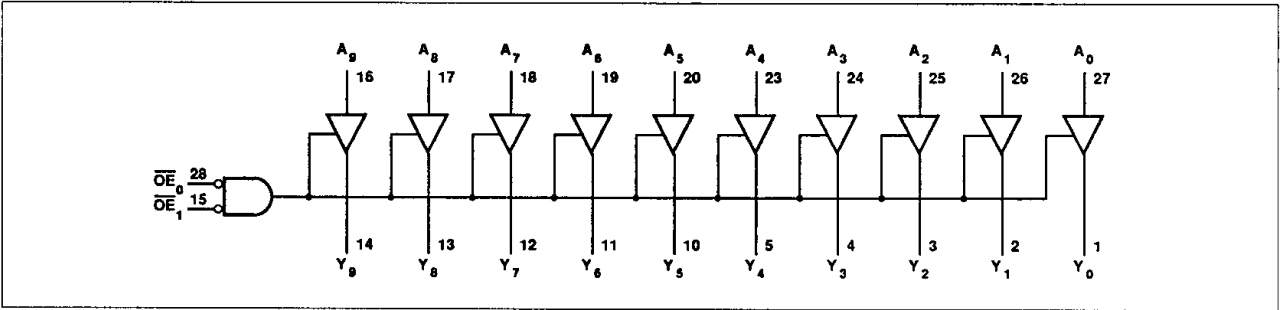
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$\overline{OE}_0, \overline{OE}_1$	Output enable input (active Low)
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	$A_0 - A_9$	Data inputs
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	$Y_0 - Y_9$	Data inputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}_n$	A_n	Y_n
L	L	L
L	H	H
H	X	Z

H = Highvoltage level
L = Low voltage level
X = Don't care
Z = High-impedance

LOGIC DIAGRAM



10-wide buffer/line driver (3-State)**74AC/ACT11827****RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	74AC11827			74ACT11827			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

10-wide buffer/line driver (3-State)

74AC/ACT11827

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V _{CC}	74AC11827				74ACT11827				UNIT
					T _{amb} = +25°C		T _{amb} = -40°C to +85°C		T _{amb} = +25°C		T _{amb} = -40°C to +85°C		
					Min	Max	Min	Max	Min	Max	Min	Max	
V _{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V _{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
			I _{OH} = -24mA	5.5	4.94		4.8		4.94		4.8		
				I _{OH} = -75mA ¹	5.5		4	3.85				3.85	
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36		0.44	
			I _{OL} = 24mA	5.5		0.36		0.44		0.36		0.44	
				I _{OL} = 75mA ¹	5.5				1.65				
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		5.0		±0.5		5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

10-wide buffer/line driver (3-State)

74AC/ACT11827

AC ELECTRICAL CHARACTERISTICS AT 3.3V ± 0.3 V

SYMBOL	PARAMETER	WAVEFORM	74AC11827					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to Y _n	1	4.8 6.8	8.4 10.4	10.8 12.6	4.8 6.8	12.4 13.4	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	6.3 10.0	10.2 16.0	12.7 19.2	6.3 10.0	14.5 21.7	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	5.9 5.4	8.5 8.0	10.4 10.0	5.9 5.4	11.1 10.5	ns

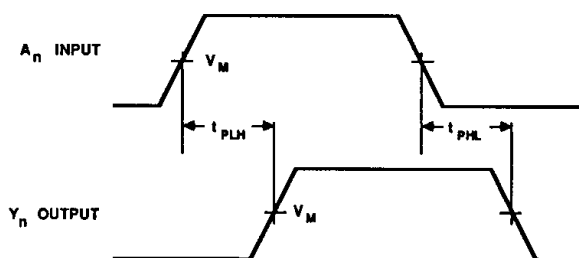
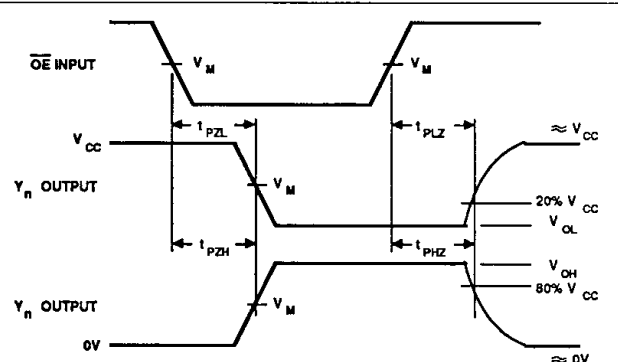
AC ELECTRICAL CHARACTERISTICS AT 5.0V ± 0.5 V

SYMBOL	PARAMETER	WAVEFORM	74AC11827					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to Y _n	1	2.1 2.9	5.3 6.2	7.5 8.4	2.1 2.9	8.7 9.7	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	3.1 4.1	5.9 7.7	8.2 10.6	3.1 4.1	9.7 13.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	3.9 4.0	6.6 6.3	8.4 7.9	3.9 4.0	9.1 8.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ± 0.5 V

SYMBOL	PARAMETER	WAVEFORM	74ACT11827					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A _n to Y _n	1	3.8 2.7	6.3 6.9	8.0 9.5	3.8 2.7	9.2 11.2	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	2.6 3.2	6.4 8.0	9.2 11.2	2.6 3.2	11.3 14.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	6.1 5.8	8.8 8.3	11.1 10.6	6.1 5.8	12.0 11.6	ns

AC WAVEFORMS

Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays

Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

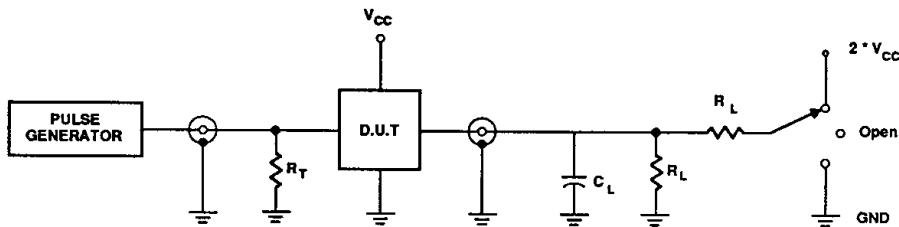
10-wide buffer/line driver (3-State)

74AC/ACT11827

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC},$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V,$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: $PRR \leq 10\text{MHz}$

$t_r = t_f = 3\text{ns}$