



November 1988  
Revised August 2000

## 74AC11 Triple 3-Input AND Gate

### General Description

The AC11 contains three 3-input AND gates.

### Features

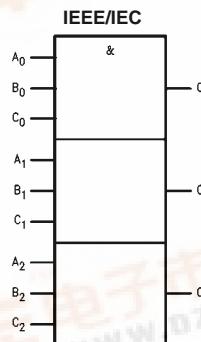
- $I_{CC}$  reduced by 50%
- Outputs source/sink 24 mA

### Ordering Code:

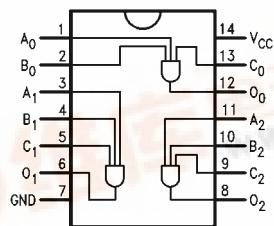
Order Number	Package Number	Package Description
74AC11SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74AC11SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC11MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC11PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$A_n, B_n, C_n$ $O_n$	Inputs Outputs

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74AC11 Triple 3-Input AND Gate

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	2.0V to 6.0V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ C$		$T_A = -40^\circ C$ to $+85^\circ C$	Units	Conditions
			Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 mA$ $I_{OH} = -24 mA$ $I_{OH} = -24 mA$ (Note 2)
		4.5		3.86	3.76		
		5.5		4.86	4.76		
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 mA$ $I_{OL} = 24 mA$ $I_{OL} = 24 mA$ (Note 2)
		4.5		0.36	0.44		
		5.5		0.36	0.44		
$I_{IN}$ (Note 4)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}$ , GND
$I_{OLD}$	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$		5.5			-75	mA	$V_{OHD} = 3.85V$ Min
$I_{CC}$ (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	$\mu A$	$V_{IN} = V_{CC}$ or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			Units	
			Min Typ Max			Min Max				
			1.5	5.5	9.5	1.0	10.0			
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	5.5	9.5	1.0	10.0	ns		
		5.0	1.5	4.0	8.0	1.0	8.5			
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	5.5	8.5	1.0	9.5	ns		
		5.0	1.5	4.0	7.0	1.0	7.5			

**Note 5:** Voltage Range 3.3 is 3.3V ± 0.3V

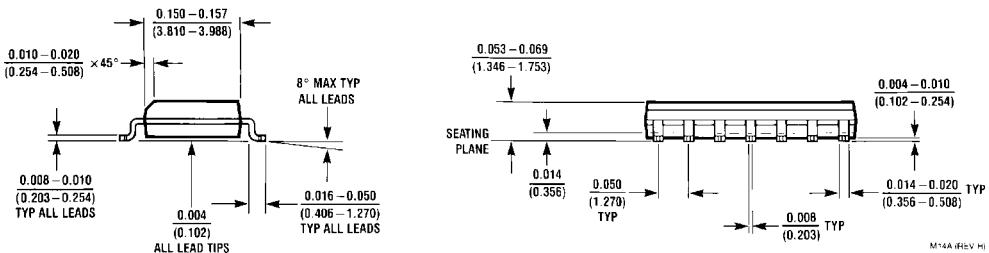
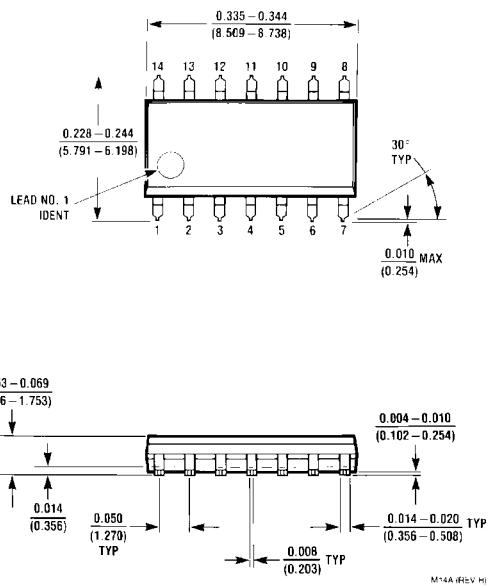
Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	20.0	pF	V <sub>CC</sub> = 5.0V

74AC11

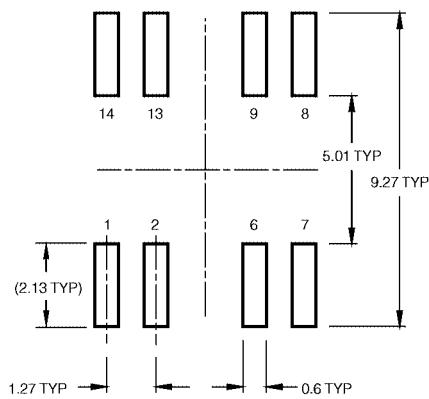
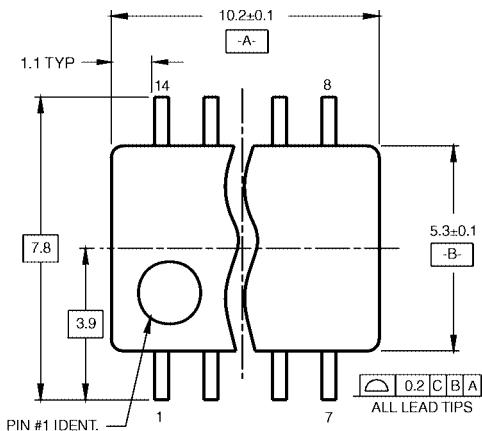
**Physical Dimensions** inches (millimeters) unless otherwise noted



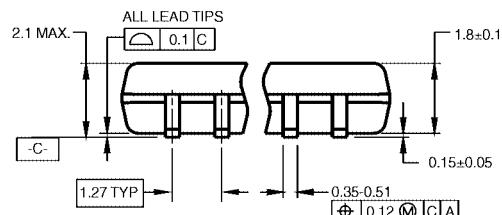
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow  
Package Number M14A

M14A (Rev. H)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



#### LAND PATTERN RECOMMENDATION

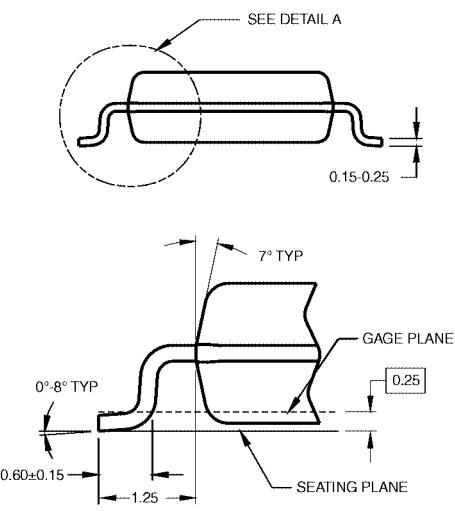


DIMENSIONS ARE IN MILLIMETERS

## NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

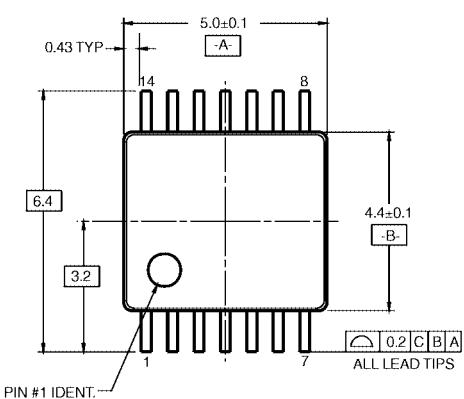
M14DRevB1



**DETAIL A**

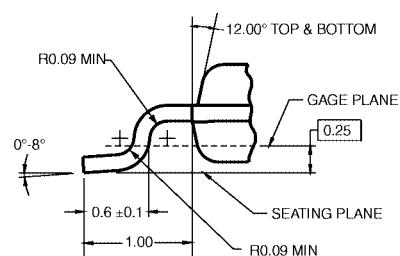
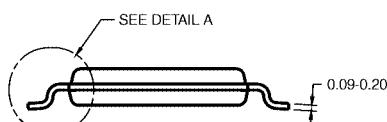
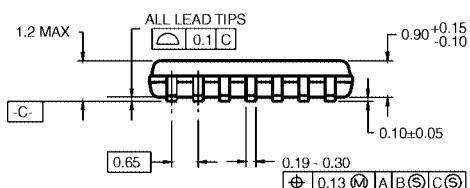
**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



The diagram shows a stepped profile with a total height of 7.72. The profile is divided into two main sections. The upper section has a height of 4.16 and consists of a series of rectangular steps. The lower section has a height of 1.78 and also consists of a series of rectangular steps. The widths of the steps are labeled as 0.65 and 0.42. A vertical dashed line is drawn through the center of the profile, and a horizontal dashed line is drawn across the middle of the profile.

#### LAND PATTERN RECOMMENDATION



## NOTES:

NOTES.

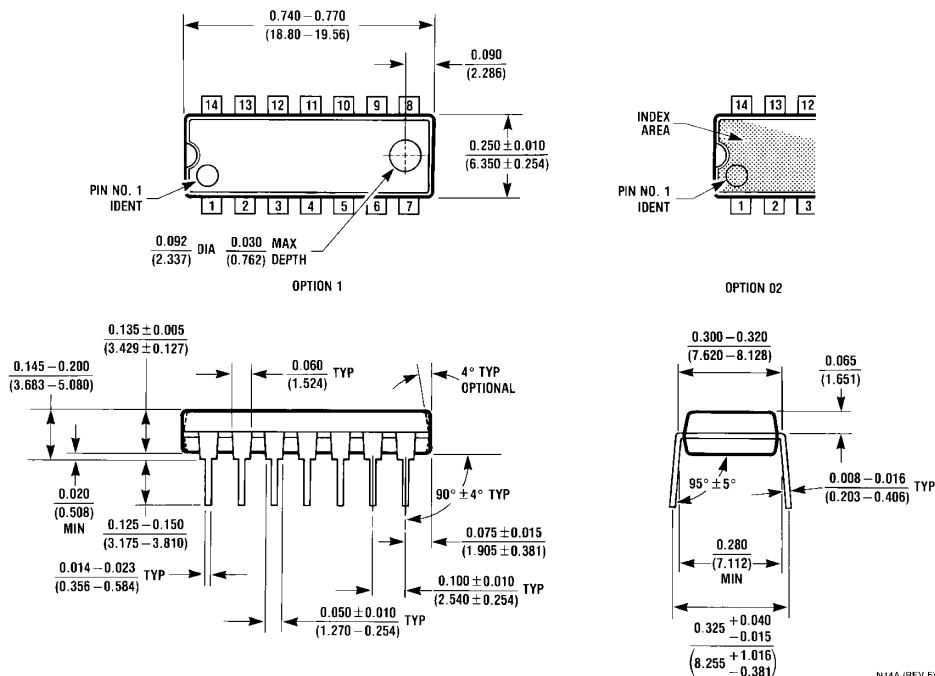
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

**DETAIL A**

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N14A

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