

74FST6800

10-Bit Bus Switch with Precharged Outputs

The ON Semiconductor 74FST6800 is a 10-bit bus switch with precharged outputs. The device is CMOS TTL compatible when operating between 4.0 and 5.5 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

Features

- $R_{ON} < 4 \Omega$ Typical
- Less Than 0.25 ns–Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS6800, FST6800, CBT6800
- All Popular Packages: SOIC–24, TSSOP–24, QSOP–24
- All Devices in Package TSSOP are Inherently Pb–Free*

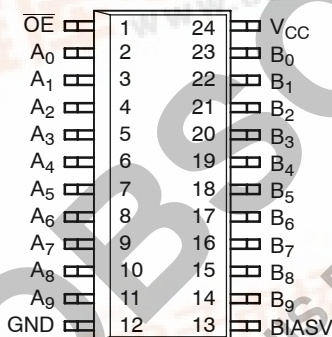


Figure 1. 24-Lead Pinout

TRUTH TABLE

OE	B ₀ –B ₉	Function
L	A ₀ –A ₉	Connect
H	Bias V	Precharge

NOTE:

H = HIGH Voltage Level

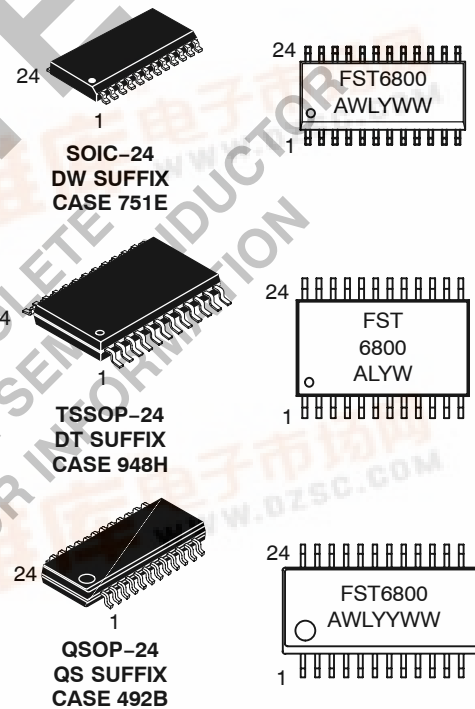
L = LOW Voltage Level



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

PIN NAMES

Pin	Description
OE	Bus Switch Enable
A	Bus A
B	Bus B

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

74FST6800

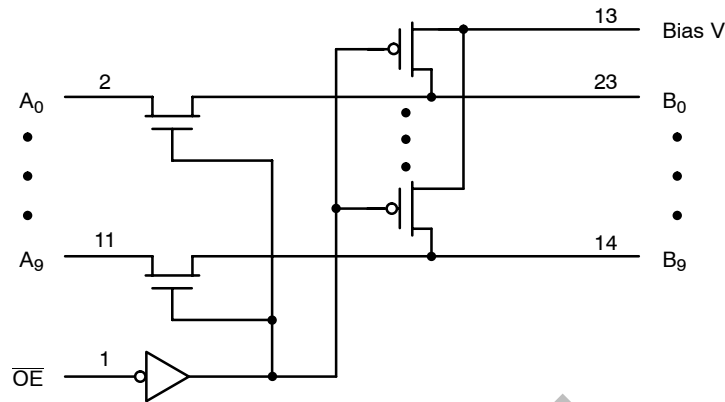


Figure 2. Logic Diagram

ORDERING INFORMATION

Device Order Number	Package	Shipping [†]
74FST6800DW	SOIC-24	48 Units / Rail
74FST6800DWR2	SOIC-24	2500 Units / Tape & Reel
74FST6800DT	TSSOP-24* (Pb-Free)	96 Units / Rail
74FST6800DTR2	TSSOP-24* (Pb-Free)	2500 Units / Tape & Reel
74FST6800QS	QSOP-24	96 Units / Rail
74FST6800QSR	QSOP-24	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to +7.0	V
I_{IK}	DC Input Diode Current $V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	-50	mA
I_O	DC Output Sink Current	128	mA
I_{CC}	DC Supply Current per Supply Pin	±100	mA
I_{GND}	DC Ground Current per Ground Pin	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance SOIC TSSOP QSOP	125 170 200	°C/W
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 N/A	V
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 85°C (Note 4)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

74FST6800

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating, Data Retention Only	4.0	5.5	V
V _I	Input Voltage (Note 5)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	5.5	V
T _A	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate Switch Control Input Switch I/O V _{CC} = 5.0 V ± 0.5 V	0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C			Unit
				Min	Typ*	Max	
V _{IK}	Clamp Diode Resistance	I _{IN} = -18mA	4.5			-1.2	V
V _{IH}	High-Level Input Voltage		4.0 to 5.5	2.0			V
V _{IL}	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I _I	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	5.5			±1.0	μA
I _{OZ}	OFF-STATE Leakage Current	0 ≤ A, B ≤ V _{CC}	5.5			±1.0	μA
R _{ON}	Switch On Resistance (Note 6)	V _{IN} = 0 V, I _{IN} = 64 mA	4.5		4	7	Ω
		V _{IN} = 0 V, I _{IN} = 30 mA	4.5		4	7	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.5		8	15	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.0		11	20	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0	5.5			3	μA
ΔI _{CC}	Increase In I _{CC} per Input	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5			2.5	mA

*Typical values are at V_{CC} = 5.0 V and T_A = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	T _A = −40°C to +85°C C _L = 50 pF, R _U = R _D = 500 Ω				Unit
			V _{CC} = 4.5–5.5 V		V _{CC} = 4.0 V		
			Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Prop Delay Bus to Bus (Note 7)	V _I = OPEN		0.25		0.25	ns
t _{PZH} , t _{PZL}	Output Enable Time, I _{OE} to Bus A, B	Bias V = GND V _I = OPEN for t _{PZH}	1.0	5.1		5.6	ns
t _{PHZ} , t _{PLZ}	Output Disable Time, I _{OE} to Bus A, B	Bias V = GND V _I = OPEN for t _{PHZ}	1.0	5.5		5.5	ns

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

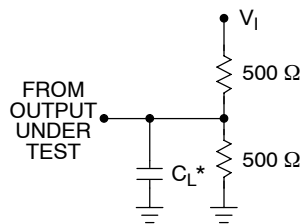
CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Unit
C _{IN}	Control Pin Input Capacitance	V _{CC} = 5.0 V	3		pF
C _{I/O}	A/B Port Input/Output Capacitance	V _{CC} , \overline{OE} = 5.0 V	5		pF

8. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

74FST6800

AC Loading and Waveforms



NOTES:

1. Input driven by $50\ \Omega$ source terminated in $50\ \Omega$.
 2. C_L includes load and stray capacitance.
- * $C_L = 50\ \text{pF}$

Figure 3. AC Test Circuit

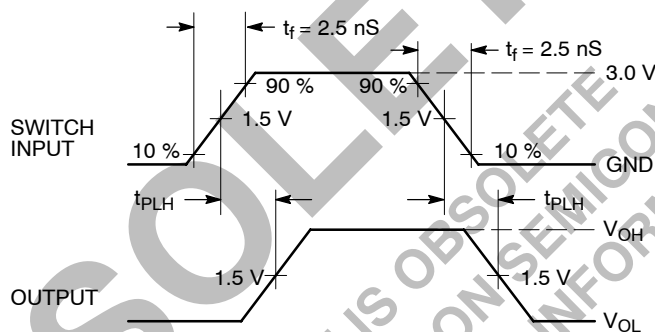


Figure 4. Propagation Delays

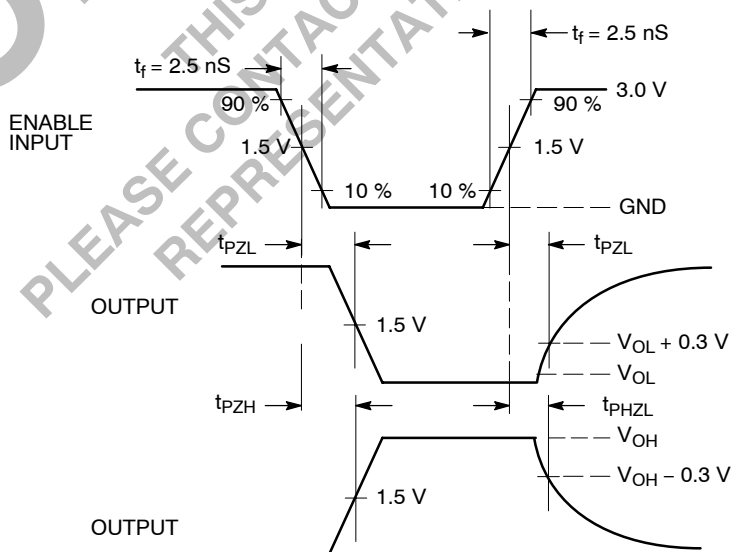
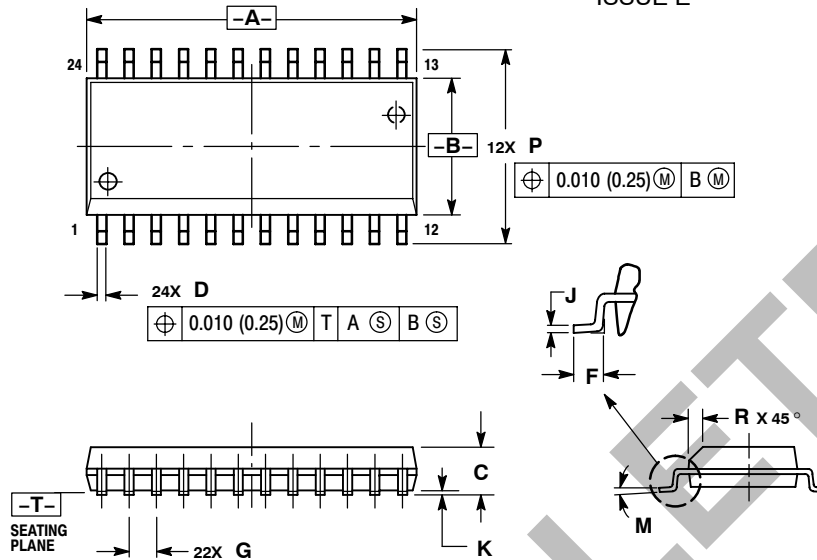


Figure 5. Enable/Disable Delays

74FST6800

PACKAGE DIMENSIONS

SOIC-24
D SUFFIX
CASE 751E-04
ISSUE E

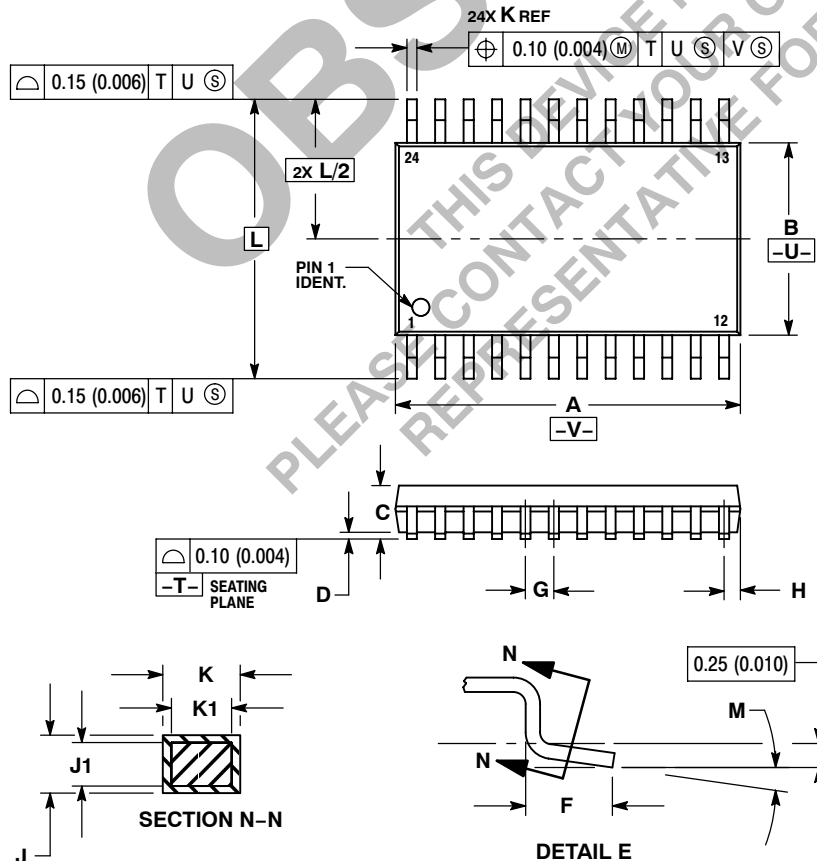


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

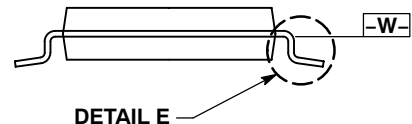
TSSOP-24
DT SUFFIX
CASE 948H-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

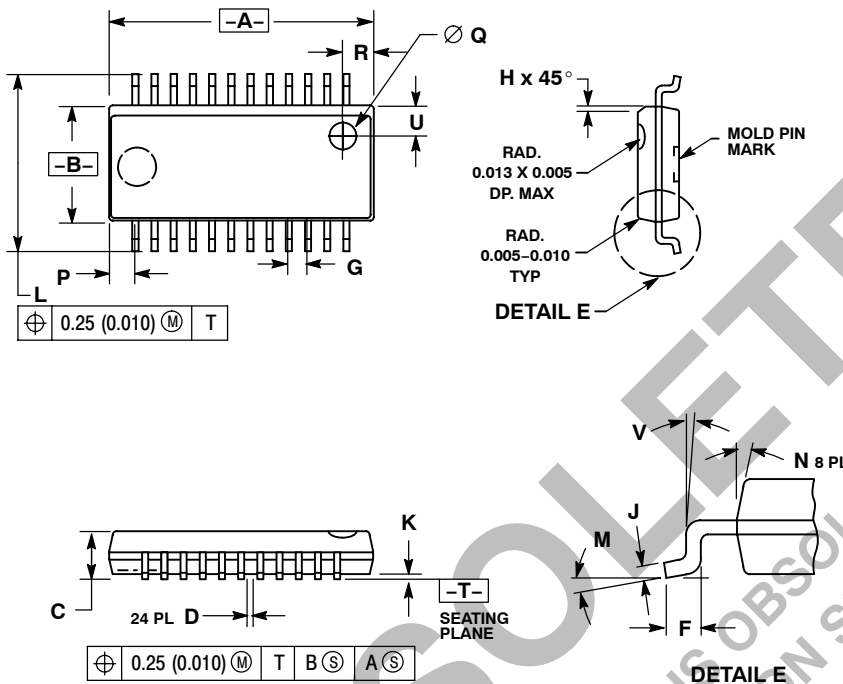
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



74FST6800

PACKAGE DIMENSIONS


QSOP-24
QS SUFFIX
CASE 492B-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

DIM	INCHES		MILLIMETERS	
	MAX	MIN	MAX	MIN
A	0.337	0.344	8.56	8.74
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.027	0.037	0.69	0.94
Q	0.035 DIA		0.89 DIA	
R	0.035	0.045	0.89	1.14
U	0.035	0.045	0.89	1.14
V	0°	8°	0°	8°

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative