

April 1988 Revised August 1999

74F251A

8-Input Multiplexer with 3-STATE Outputs

General Description

The 74F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Features

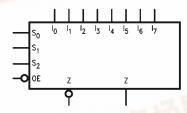
- Multifunctional capability
- On-chip select logic decoding
- Inverting and non-inverting 3-STATE outputs

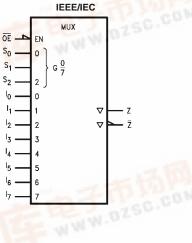
Ordering Code:

Order Number	Package Number	Package Description
74F251ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F251ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F251APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

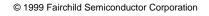
Logic Symbols





Connection Diagram





Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I _{IH} /I _{IL}	
	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
S ₀ -S ₂	Select Inputs	1.0/1.0	20 μA/-0.6 mA	
ŌĒ	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA	
I ₀ –I ₇	Multiplexer Inputs	1.0/1.0	20 μA/-0.6 mA	
Z	3-STATE Multiplexer Output	150/40 (33.3)	-3 mA/24 mA (20 mA)	
Z	Complementary 3-STATE Multiplexer Output	150/40 (33.3)	-3 mA/24 mA (20 mA)	

Functional Description

This device is a logical implementation of a single-pole, 8position switch with the switch position controlled by the state of three Select inputs, S₀, S₁, S₂. Both assertion and negation outputs are provided. The Output Enable input (OE) is active LOW. When it is activated, the logic function provided at the output is:

$$\begin{split} Z &= \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + \\ &I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + \\ &I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + \\ &I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2) \end{split}$$

When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

Truth Table

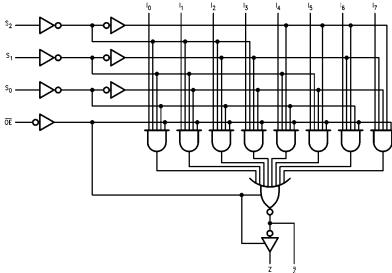
	Inp	Outputs			
OE	S ₂	S ₂ S ₁		Z	Z
Н	Х	Х	Х	Z	Z
L	L	L	L	Ī ₀	I ₀
L	L	L	Н	Ī ₁	I ₁
L	L	Н	L	Ī ₂	I_2
L	L	Н	Н	Ī ₃	I_3
L	Н	L	L	\overline{I}_4	I_4
L	Н	L	Н	Ī ₅	l ₅
L	Н	Н	L	Ī ₆	I ₆
L	Н	Н	Н	Ī ₇	l ₇

H = HIGH Voltage Level

L = LOW Voltage Level X = Immaterial

Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \end{array}$

Junction Temperature under Bias -55°C to +125°C -55°C to +150°C

 $\begin{array}{lll} \text{V}_{\text{CC}} \text{ Pin Potential to Ground Pin} & -0.5 \text{V to } +7.0 \text{V} \\ \text{Input Voltage (Note 2)} & -0.5 \text{V to } +7.0 \text{V} \\ \text{Input Current (Note 2)} & -30 \text{ mA to } +5.0 \text{ mA} \\ \end{array}$

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

 $\begin{array}{ll} \mbox{Standard Output} & -0.5\mbox{V to V}_{\mbox{CC}} \\ \mbox{3-STATE Output} & -0.5\mbox{V to } +5.5\mbox{V} \end{array}$

Current Applied to Output

in LOW State (Max) $\qquad \qquad \text{twice the rated I}_{\text{OL}} \, (\text{mA})$

Free Air Ambient Temperature $0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

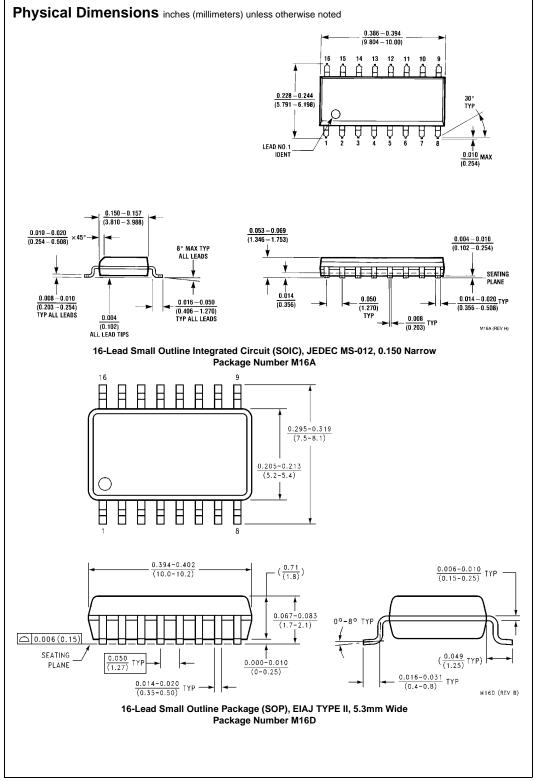
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH	10% V _{CC}	2.5					I _{OH} = -1 mA	
	Voltage	10% V _{CC}	2.4			V	Min	$I_{OH} = -3 \text{ mA}$	
		5% V _{CC}	2.7			V	IVIII	$I_{OH} = -1 \text{ mA}$	
		5% V _{CC}	2.7					$I_{OH} = -3 \text{ mA}$	
V _{OL}	Output LOW	10% V _{CC}			0.5	.,	N.45	1 04 4	
	Voltage				0.5	V	Min	I _{OL} = 24 mA	
I _{IH}	Input HIGH)/ 0.71/	
	Current				5.0	μΑ	Max	V _{IN} = 2.7V	
I _{BVI}	Input HIGH Current				7.0			1/ 7.01/	
	Breakdown Test				7.0	μА	Max	V _{IN} = 7.0V	
I _{CEX}	Output HIGH				50	μА	Max	V _{OUT} = V _{CC}	
	Leakage Current				50	μΑ	IVIAX	v _{OUT} = v _{CC}	
V _{ID}	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9 \mu A$	
	Test		4.75					All Other Pins Grounded	
I _{OD}	Output Leakage				2.75	^	0.0	V _{IOD} = 150 mV	
	Circuit Current				3.75	μА		All Other Pins Grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$	
l _{ozh}	Output Leakage Current				50	μА	Max	V _{OUT} = 2.7V	
I _{OZL}	Output Leakage Current				-50	μΑ	Max	V _{OUT} = 0.5V	
los	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V	
I _{ZZ}	Bus Drainage Test				500	μΑ	0.0V	V _{OUT} = 5.25V	
I _{CCL}	Power Supply Current			15	22	mA	Max	$V_O = LOW$	
I _{CCZ}	Power Supply Current			16	24	mA	Max	V _O = HIGH Z	

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_1 = 50 \text{ pF}$			$T_A = -55$ °C to +125°C $V_{CC} = 5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0$ V $C_1 = 50$ pF		Units
		t _{PLH}	Propagation Delay	3.5	6.0	9.0	3.5	11.5	3.5
t _{PHL}	S_n to \overline{Z}	3.2	5.0	7.5	3.2	8.0	3.2	7.5	ns
t _{PLH}	Propagation Delay	4.5	7.5	10.5	3.5	14.0	4.5	12.5	ns
t _{PHL}	S _n to Z	4.0	6.0	8.5	3.0	10.5	4.0	9.0	
t _{PLH}	Propagation Delay	3.0	5.0	6.5	2.5	8.0	3.0	7.0	ns
t _{PHL}	I _n to Z	1.5	2.5	4.0	1.5	6.0	1.5	5.0	
t _{PLH}	Propagation Delay	3.5	5.0	7.0	2.5	9.0	2.5	8.0	
t _{PHL}	I _n to Z	3.5	5.5	7.0	3.5	9.0	3.5	7.5	ns
t _{PZH}	Output Enable Time	2.5	4.3	6.0	2.0	7.0	2.5	7.0	
t_{PZL}	OE to Z	2.5	4.3	6.0	2.5	7.5	2.5	6.5	
t _{PHZ}	Output Disable Time	2.5	4.0	5.5	2.5	6.0	2.5	6.0	ns
t_{PLZ}	OE to Z	1.5	3.0	4.5	1.5	5.0	1.5	4.5	
t _{PZH}	Output Enable Time	3.5	5.0	7.0	3.0	8.5	3.0	7.5	
t_{PZL}	OE to Z	3.5	5.5	7.5	3.5	9.0	3.5	8.0	ns
t _{PHZ}	Output Disable Time	2.0	3.8	5.5	2.0	5.5	2.0	5.5	115
t_{PLZ}	OE to Z	1.5	3.0	4.5	1.5	5.5	1.5	4.5	



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)14 13 12 11 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT PIN NO. 1 2 3 4 5 6 7 8 1 2 OPTION 01 OPTION 02 0.065 $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ $\frac{0.060}{(1.524)}$ TYP 4° TYP 0.300 - 0.320 (1.651)OPTIONAL (7.620 - 8.128)0.145 - 0.200 (3.683 - 5.080)95° ± 5° $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 0.020 MIN 0.280 0.125 - 0.150 (3.175 - 3.810) (7.112) MIN 0.030 ± 0.015 (0.762 ± 0.381) 0.014 - 0.023 (0.325 +0.040 -0.015 0.100 ± 0.010 (0.356 - 0.584)(2.540 ± 0.254) TYP 0.050 ± 0.010 (1.270 ± 0.254) TYP N16E (REV F) (8.255 **+**1.016 **-**0.381

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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