

May 1995

54F/74F563 Octal D-Type Latch with TRI-STATE® Outputs

General Description

The 'F563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 'F573, but has inverted outputs.

Features

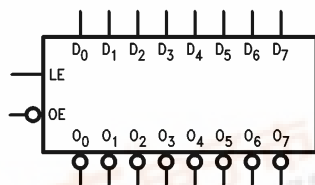
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F573

Commercial	Military	Package Number	Package Description
74F563PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F563DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F563SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F563SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F563FM (Note 2)	W20A	20-Lead Cerpack
	54F563LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

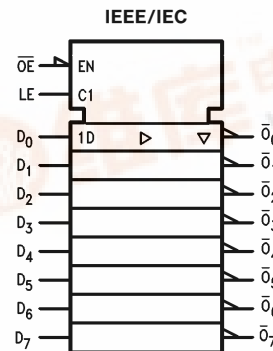
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMOB, FMOB and LMOB.

Logic Symbols



TL/F/9562-3



TL/F/9562-5

Unit Loading/Fan Out

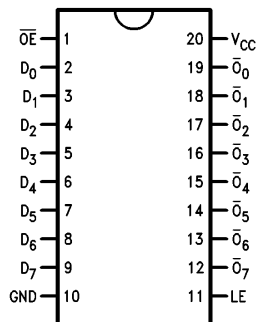
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0 – D_7	Data Inputs	1.0/1.0	20 μ A/ –0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 μ A/ –0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ –0.6 mA
$\overline{O_0}$ – $\overline{O_7}$	TRI-STATE Latch Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

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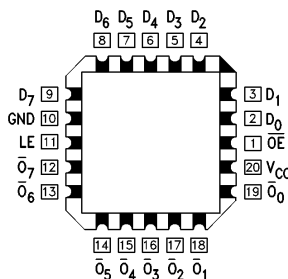
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



TL/F/9562-1

Pin Assignment
for LCC



TL/F/9562-2

Functional Description

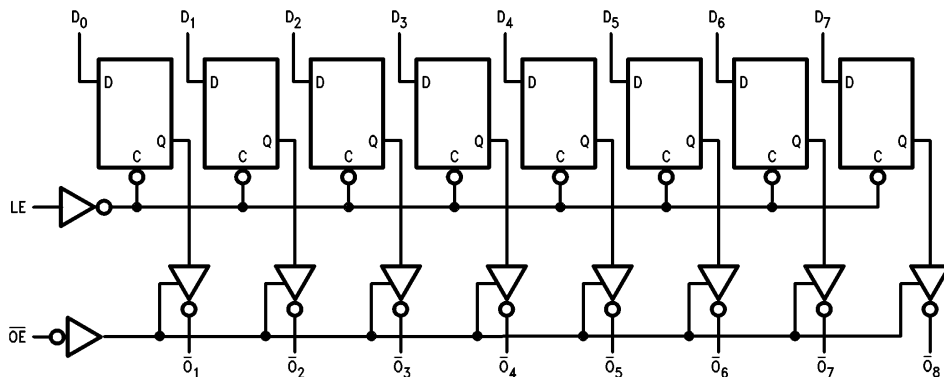
The 'F563 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/9562-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			−50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−60	−150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCL}	Power Supply Current		40	61	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		40	61	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

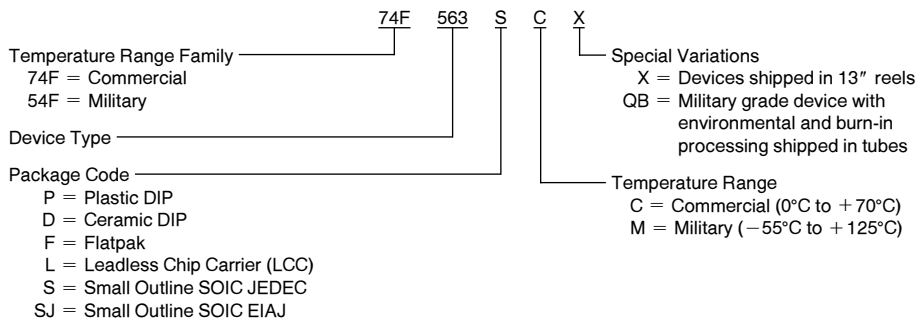
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	3.5		8.5	3.0	10.5	3.0	9.5	ns
		2.5		6.5	2.0	7.5	2.0	7.0	
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	4.5		9.5	4.0	11.0	4.0	10.5	ns
		3.0		7.0	2.5	7.5	2.5	7.0	
t_{PZH} t_{PZL}	Output Enable Time	2.0		7.5	2.0	9.5	2.0	9.0	ns
		3.0		8.5	2.5	10.0	1.5	9.5	
t_{PHZ} t_{PLZ}	Output Disable Time	1.5		5.5	1.5	7.0	1.5	6.5	
		1.5		5.5	1.5	5.5	1.5	5.5	

AC Operating Requirements

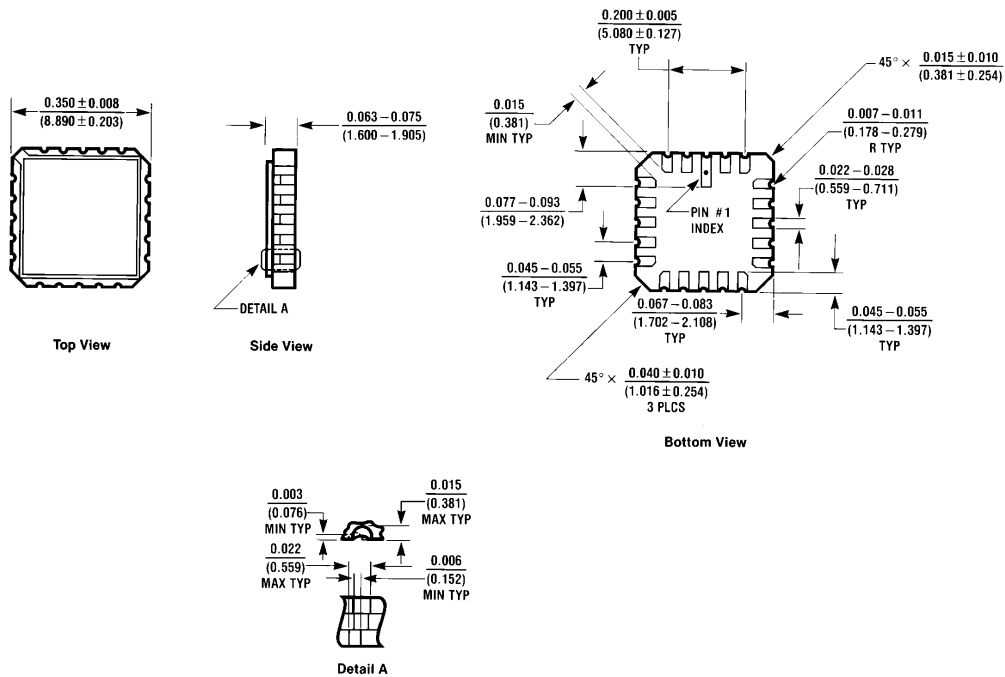
Symbol	Parameter	74F	54F	74F	Units
		T _A = +25°C V _{CC} = +5.0V	T _A , V _{CC} = Mil	T _A , V _{CC} = Com	
		Min Max	Min Max	Min Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to LE	2.0 2.0	2.0 2.0	2.0 2.0	ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to LE	3.0 3.0	3.0 3.0	3.0 3.0	ns
t _w (H)	LE Pulse Width, HIGH	4.0	4.0	4.0	ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



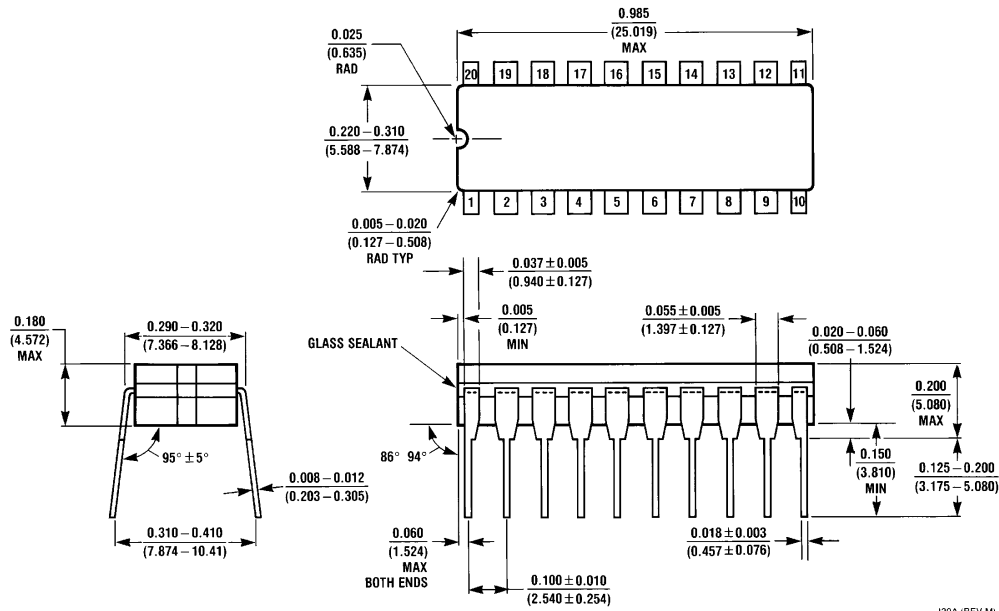
Physical Dimensions inches (millimeters)



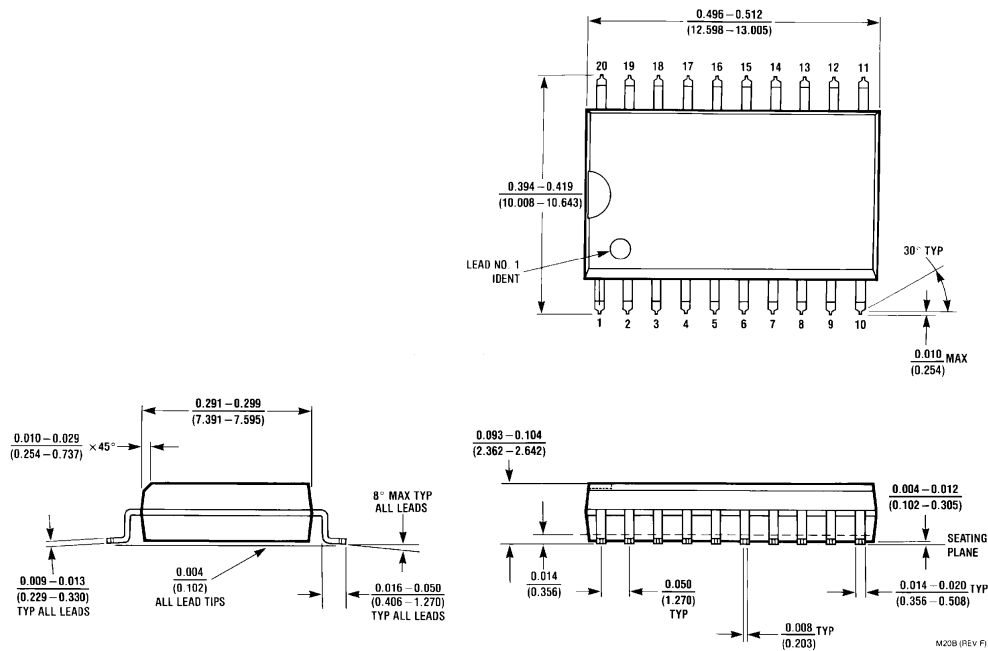
E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

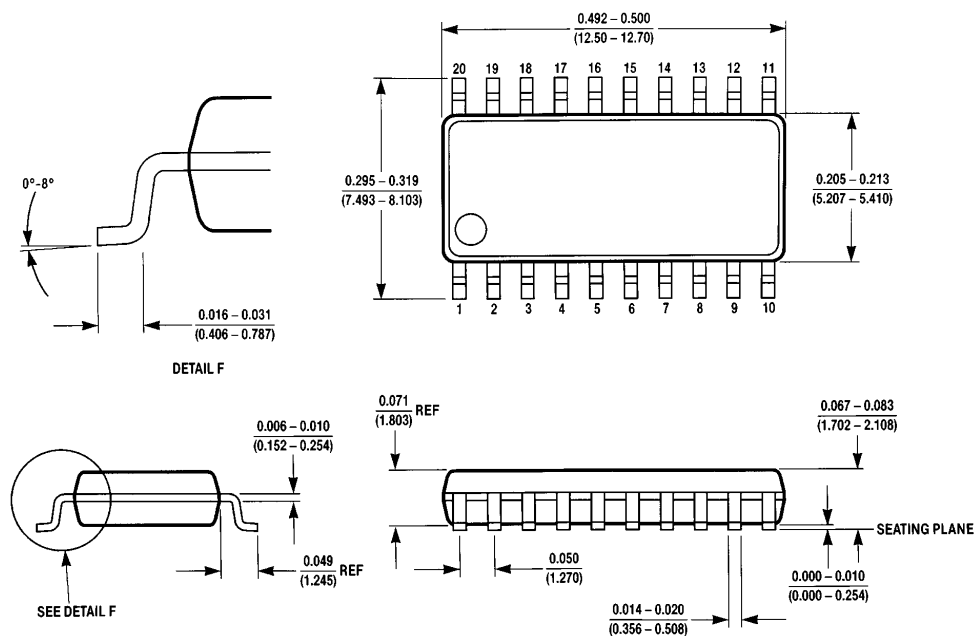
Physical Dimensions inches (millimeters) (Continued)



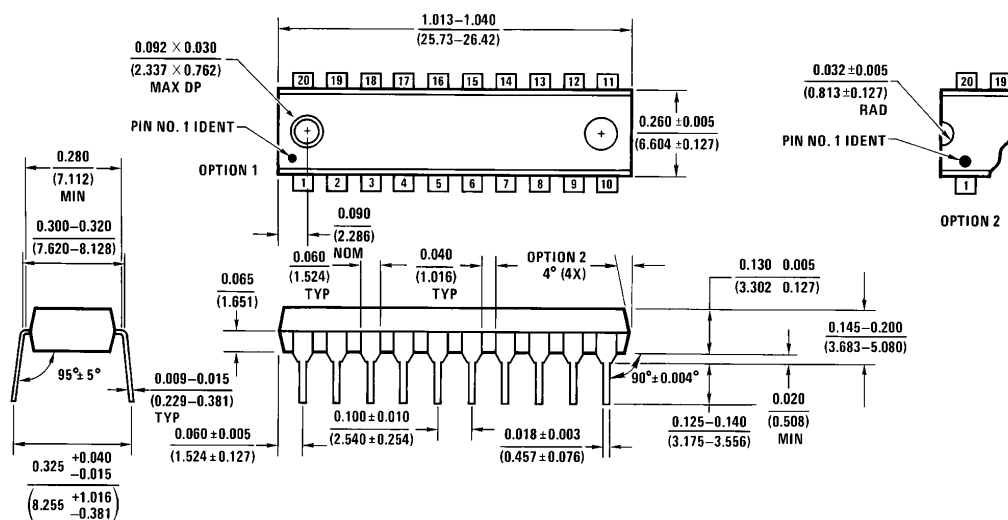
20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



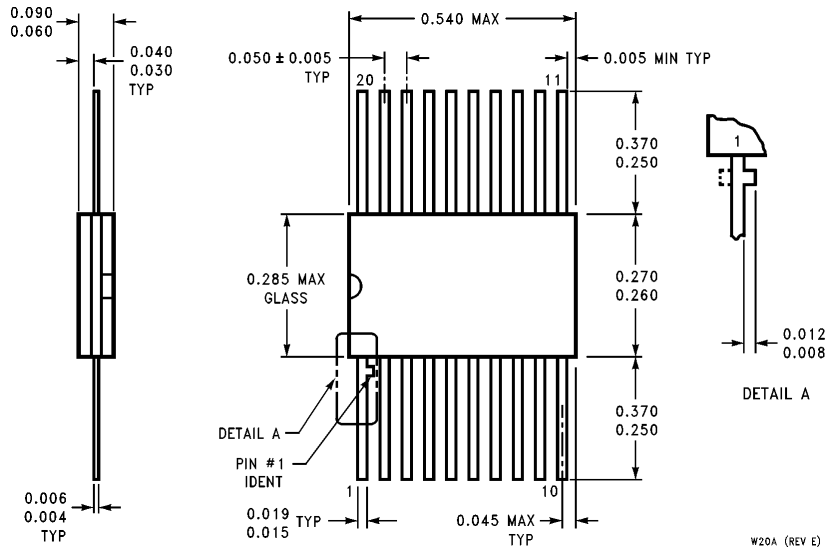
20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ
NS Package Number M20D**



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A**

Physical Dimensions inches (millimeters) (Continued)

20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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