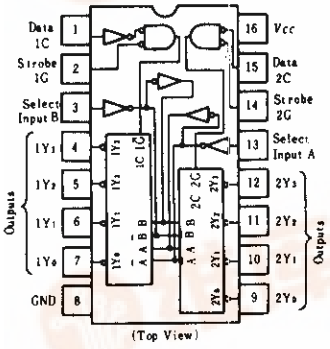
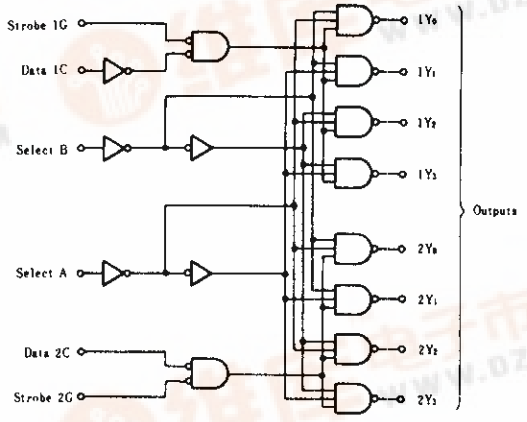
HD74LS156 ●Dual 2-line-to-4-line Decoders/Demultiplexers (with open collector outputs)

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address inputs. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output voltage	V_{OH}	—	—	5.5	V
Low level output current	I_{OL}	—	—	8	mA

■FUNCTION TABLE

●2-to-4-line Decoder/1-to-4-line Demultiplexer

Inputs				Outputs				Inputs				Outputs			
SELECT		STROBE	DATA					SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3	B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
×	×	H	×	H	H	H	H	×	×	H	×	H	H	H	H
L	L	L	H	L	H	H	H	L	L	L	L	L	H	H	H
L	H	L	H	H	L	H	H	L	H	L	L	H	L	H	H
H	L	L	H	H	H	L	H	H	L	L	L	H	H	L	H
H	H	L	H	H	H	H	L	H	H	L	L	H	H	H	L
×	×	×	L	H	H	H	H	×	×	×	H	H	H	H	H

●3-to-8-line Decoder/1-to-8-line Demultiplexer

Inputs				Outputs							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C[1]	B	A	G[2]	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
×	×	×	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Notes) 1. C; input 1C and 2C connected together
2. G; inputs 1G and 2G connected together
3. H; high level, L; low level, X; irrelevant

HD74LS156

■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—	—	V
	V_{IL}			—	—	0.8	V
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$		—	—	100	μA
Output voltage	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	—	—	0.4	V
			$I_{OL}=8mA$	—	—	0.5	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		—	—	0.1	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$		—	6.1	10	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

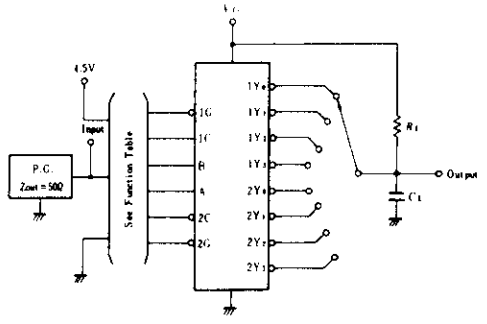
** I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

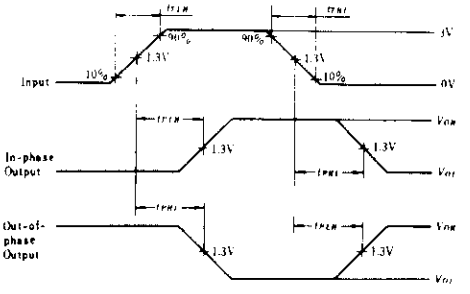
Item	Symbol	Inputs	Output	Level of logic	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	A, B, 2C, 1G or 2G	Y	2	$C_L=15pF$, $R_L=2k\Omega$	—	25	40	ns
	t_{PHL}	A, B, 2C, 1G or 2G	Y	2		—	34	51	
	t_{PLH}	A or B	Y	3		—	31	46	
	t_{PHL}	A or B	Y	3		—	34	51	
	t_{PLH}	1C	Y	3		—	32	48	
	t_{PHL}	1C	Y	3		—	32	48	

■TESTING METHOD

1) Test Circuit



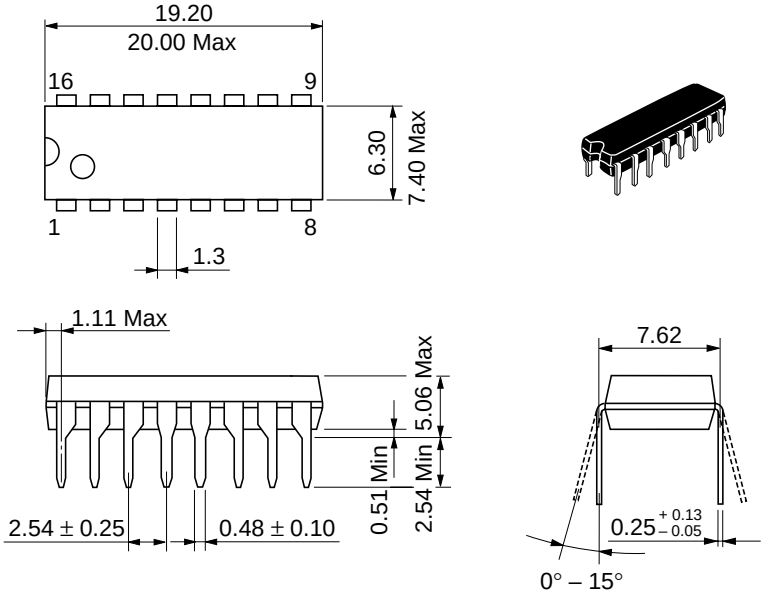
Waveform



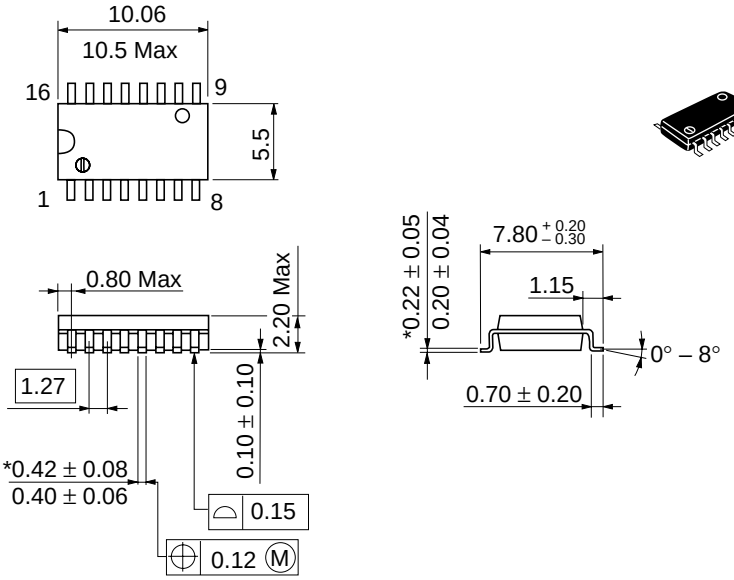
Notes) 1. Input pulse; $t_{TLH}\leqq15ns$, $t_{THL}\leqq6ns$, PRR=1MHz, duty cycle=50%.

2. C_L includes probe and jig capacitance.

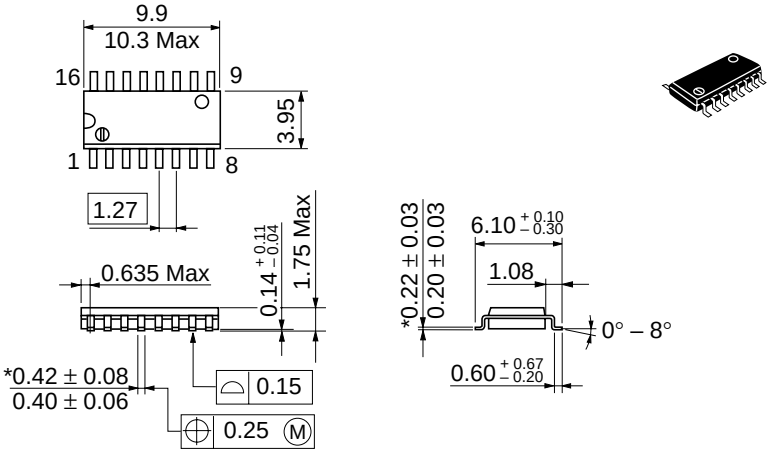
Unit: mm


19.20
20.00 Max
16
9
6.30
7.40 Max
1
8
1.3
1.11 Max
5.06 Max
0.51 Min
2.54 Min
2.54 ± 0.25
0.48 ± 0.10
7.62
0.25 + 0.13 − 0.05
0° – 15°

Unit: mm


10.06
10.5 Max
16
9
1
8
5.5
0.80 Max
2.20 Max
1.27
*0.42 ± 0.08
0.40 ± 0.06
0.10 ± 0.10
0.15
0.12 M
*0.22 ± 0.05
0.20 ± 0.04
7.80 +0.20 −0.30
1.15
0° – 8°
0.70 ± 0.20

Unit: mm


9.9
10.3 Max
16
9
1
8
3.95
1.27
0.635 Max
0.14 +0.11 −0.04
1.75 Max
*0.42 ± 0.08
0.40 ± 0.06
0.15
0.25 M
*0.22 ± 0.03
0.20 ± 0.03
6.10 +0.10 −0.30
1.08
0° – 8°
0.60 +0.67 −0.20

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