MOTOROLA

SN54/74LS196
SN54/74LS197

4-STAGE PRESETTABLE RIPPLE COUNTERS

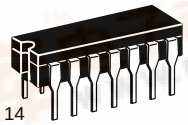
The SN54/74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8, 4, 2, 1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54/74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (PL) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when PL is LOW and storing the data when PL is HIGH.

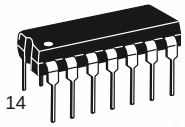
- Low Power Consumption — Typically 80 mW
- High Counting Rates — Typically 70 MHz
- Choice of Counting Modes — BCD, Bi-Quinary, Binary
- Asynchronous Presettable
- Asynchronous Master Reset
- Easy Multistage Cascading
- Input Clamp Diodes Limit High Speed Termination Effects

4-STAGE PRESETTABLE RIPPLE COUNTERS

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



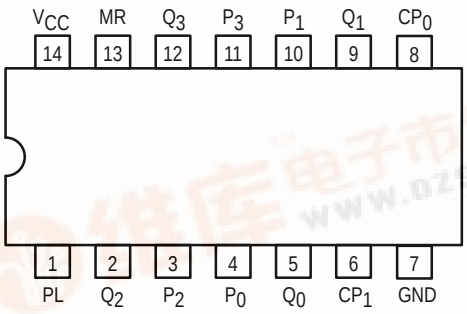
N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



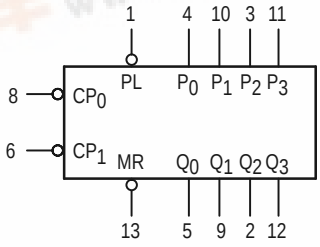
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CP_0}$	Clock (Active LOW Going Edge) Input to Divide-by-Two Section	1.0 U.L.	1.5 U.L.
$\overline{CP_1}$ (LS196)	Clock (Active LOW Going Edge) Input to Divide-by-Five Section	2.0 U.L.	1.75 U.L.
$\overline{CP_1}$ (LS197)	Clock (Active LOW Going Edge) Input to Divide-by-Eight Section	1.0 U.L.	0.8 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{PL}$	Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_0–P_3	Data Inputs	0.5 U.L.	0.25 U.L.
Q_0–Q_3	Outputs (Notes b, c)	10 U.L.	5 (2.5) U.L.

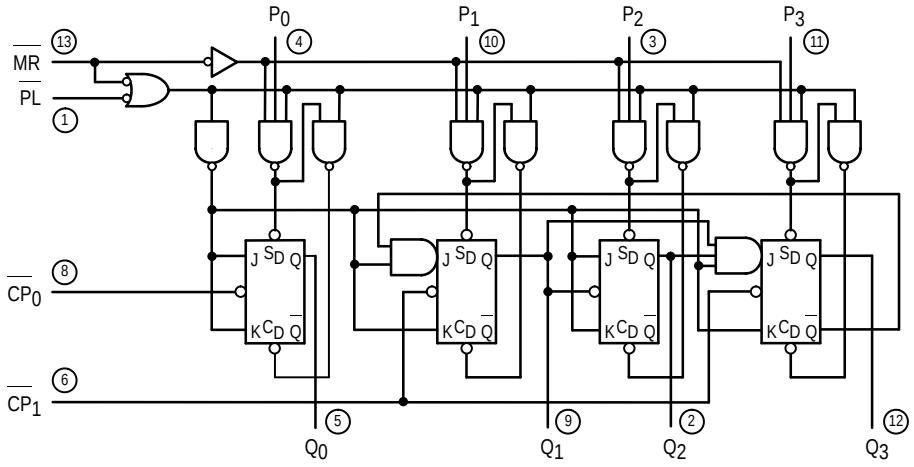
NOTES:
a. 1 TTL Unit Load (U.L.) = 40µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
c. In addition to loading shown, Q_0 can also drive $\overline{CP_1}$.

LOGIC SYMBOL

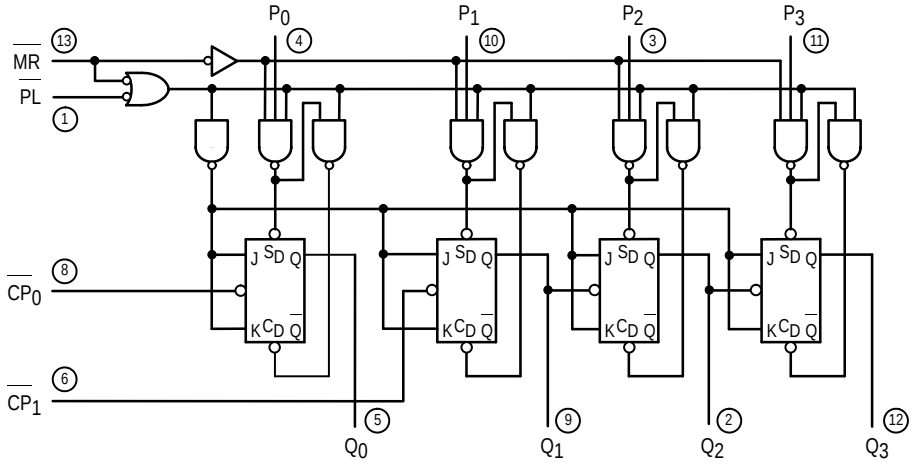


V_{CC} = PIN 14
GND = PIN 7

LOGIC DIAGRAM



LS196



LS197

V_{CC} = PIN 14
GND = PIN 7
◯ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The CP_0 input serves the Q_0 flip-flop in both circuit types while the CP_1 input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the CP_1 input. With the input frequency connected to CP_0 and Q_0 driving CP_1, the LS197 forms a straightforward module-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to CP_0 and with Q_0 driving CP_1, the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to CP_1 and Q_3 driving CP_0, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (P_0–P_3) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

Figure 2. LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:
1. Signal applied to CP_0, Q_0 connected to CP_1.
2. Signal applied to CP_1, Q_3 connected to CP_0.

MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	⌐	Count

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = HIGH to Low Clock Transition

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Data, PL MR, CP_0 (LS196) MR, CP_0, CP_1 (LS197) CP_1 (LS196)				20 40 40 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, PL MR, CP_0 (LS196) MR, CP_0, CP_1 (LS197) CP_1 (LS196)				0.1 0.2 0.2 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Data, PL MR CP_0 CP_1 (LS196) CP_1 (LS197)				−0.4 −0.8 −2.4 −2.8 −1.3	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				27	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS196			LS197				
		Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	30	40		30	40		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	$\overline{CP_0}$ Input to Q_0 Output		8.0 13	15 20		8.0 14	15 21	ns	
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_1 Output		16 22	24 33		12 23	19 35	ns	
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_2 Output		38 41	57 62		34 42	51 63	ns	
t_{PLH} t_{PHL}	$\overline{CP_1}$ Input to Q_3 Output		12 30	18 45		55 63	78 95	ns	
t_{PLH} t_{PHL}	Data to Output		20 29	30 44		18 29	27 44	ns	
t_{PLH} t_{PHL}	$\overline{PL}$ Input to Any Output		27 30	41 45		26 30	39 45	ns	
t_{PHL}	$\overline{MR}$ Input to Any Output		34	51		34	51	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS196			LS197				
		Min	Typ	Max	Min	Typ	Max		
t_W	$\overline{CP_0}$ Pulse Width	20			20			ns	V_{CC} = 5.0 V
t_W	$\overline{CP_1}$ Pulse Width	30			30			ns	
t_W	$\overline{PL}$ Pulse Width	20			20			ns	
t_W	$\overline{MR}$ Pulse Width	15			15			ns	
t_s	Data Input Setup Time — HIGH	10			10			ns	
t_s	Data Input Setup Time — LOW	15			15			ns	
t_h	Data Hold Time — HIGH	10			10			ns	
t_h	Data Hold Time — LOW	10			10			ns	
t_{rec}	Recovery Time	30			30			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

AC WAVEFORMS

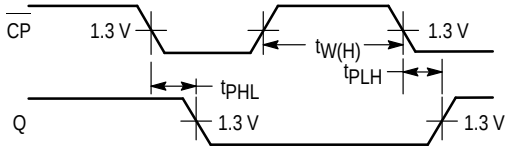
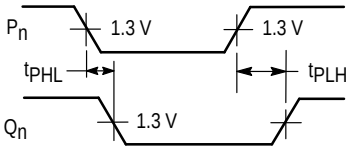


Figure 1



NOTE: $\overline{PL}$ = LOW

Figure 2

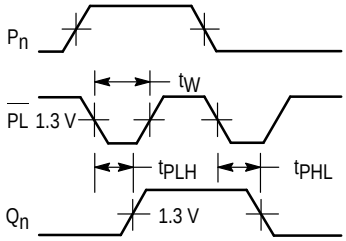


Figure 3

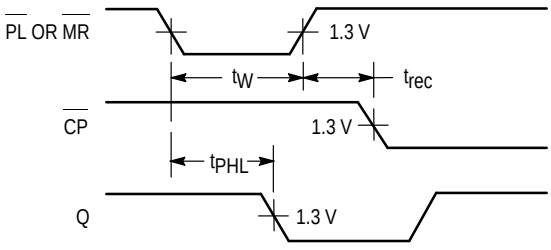
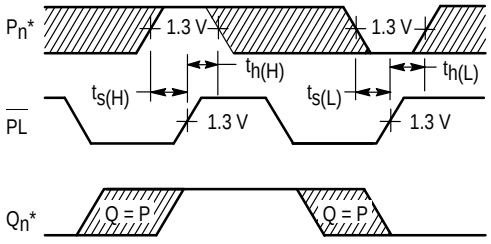


Figure 4



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 5