

# 74LV138

## 3-to-8 line decoder/demultiplexer; inverting

Rev. 03 — 15 November 2007

Product data sheet

### 1. General description

The 74LV138 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC138 and 74HCT138.

The 74LV138 is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address inputs (A0, A1 and A2) and, when enabled, provides eight mutually exclusive active LOW outputs ( $\bar{Y}0$  to  $\bar{Y}7$ ).

There are three enable inputs: two active LOW ( $\bar{E}1$  and  $\bar{E}2$ ) and one active HIGH (E3). Every output will be HIGH unless  $\bar{E}1$  and  $\bar{E}2$  are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LV138 devices and one inverter. The 74LV138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

### 2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical output ground bounce < 0.8 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot: > 2 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and from  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV138N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV138D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV138DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV138PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV138BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 4. Functional diagram

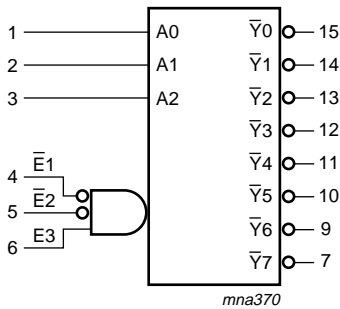


Fig 1. Logic symbol

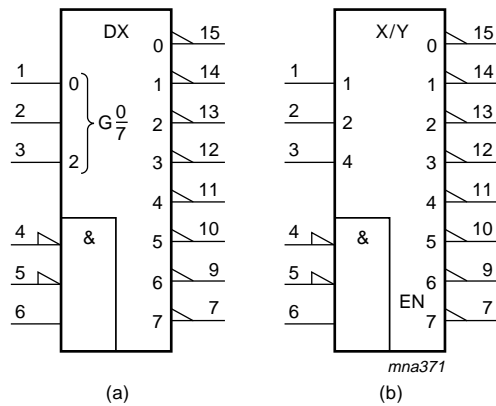


Fig 2. IEC logic symbol

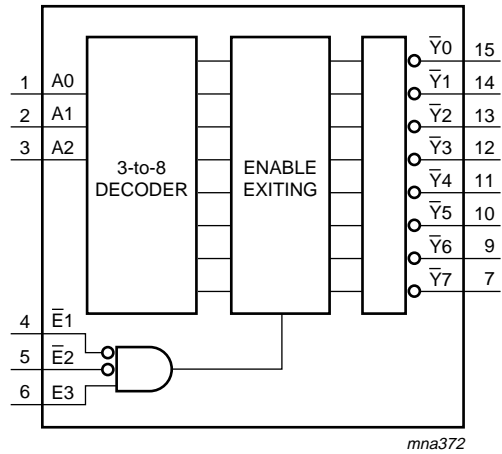


Fig 3. Functional diagram

## 5. Pinning information

### 5.1 Pinning

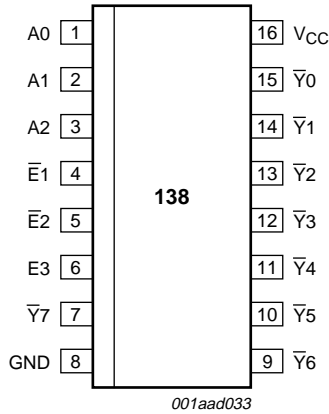


Fig 4. Pin configuration DIP16, SO16 and (T)SSOP16

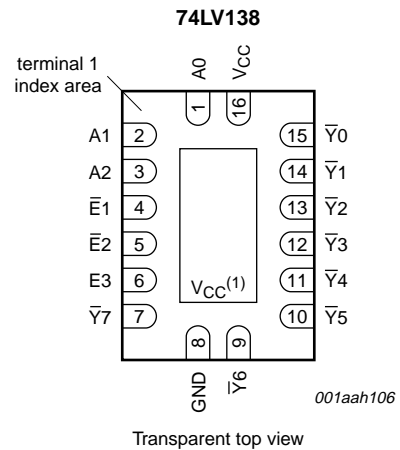


Fig 5. Pin configuration DHVQFN16

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input
A1	2	address input
A2	3	address input
$\bar{E}1$	4	enable input (active LOW)
$\bar{E}2$	5	enable input (active LOW)
E3	6	enable input (active HIGH)
GND	8	ground (0 V)
$\bar{Y}0$ to $\bar{Y}7$	15, 14, 13, 12, 11, 10, 9, 7	output
$V_{CC}$	16	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input						Output							
$\bar{E}1$	$\bar{E}2$	E3	A0	A1	A2	$\bar{Y}0$	$\bar{Y}1$	$\bar{Y}2$	$\bar{Y}3$	$\bar{Y}4$	$\bar{Y}5$	$\bar{Y}6$	$\bar{Y}7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	±50	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C

**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
	DIP16 package		[2] -	750	mW
	SO16 package		[3] -	500	mW
	(T)SSOP16 package		[4] -	500	mW
	DHVQFN16 package		[5] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.
- [3] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.
- [4] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.
- [5] P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage[1]		1.0	3.3	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.0 V to 2.0 V	-	-	500	ns/V
		V <sub>CC</sub> = 2.0 V to 2.7 V	-	-	200	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	100	ns/V
		V <sub>CC</sub> = 3.6 V to 5.5 V	-	-	50	ns/V

- [1] The static characteristics are guaranteed from V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 5.5 V, but LV devices are guaranteed to function down to V<sub>CC</sub> = 1.0 V (with input levels GND or V<sub>CC</sub>).

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-	V
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 3.0 V	2.4	2.82	-	2.2	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.6	4.2	-	3.5	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	0.25	0.40	-	0.50	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20.0	-	160	µA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

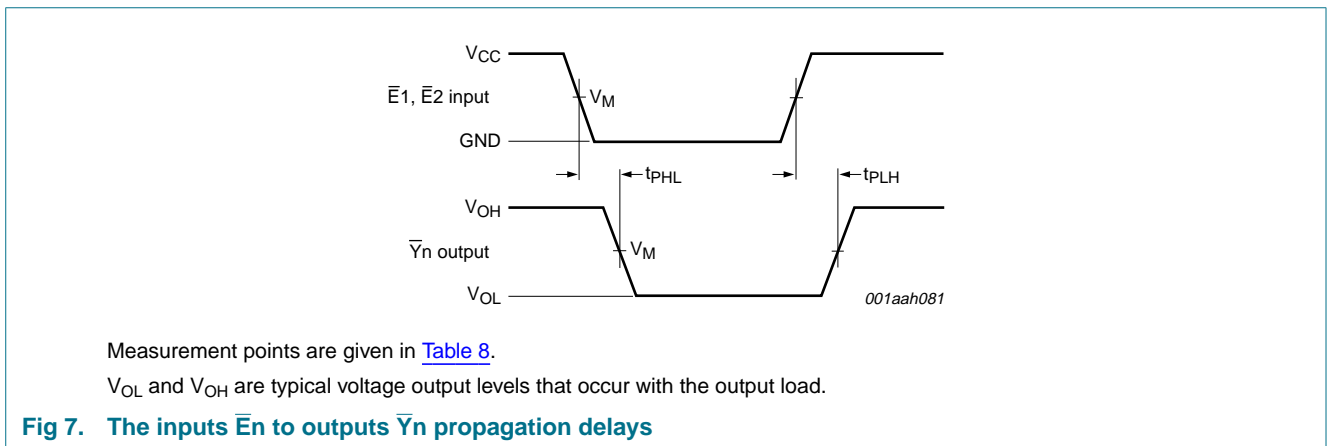
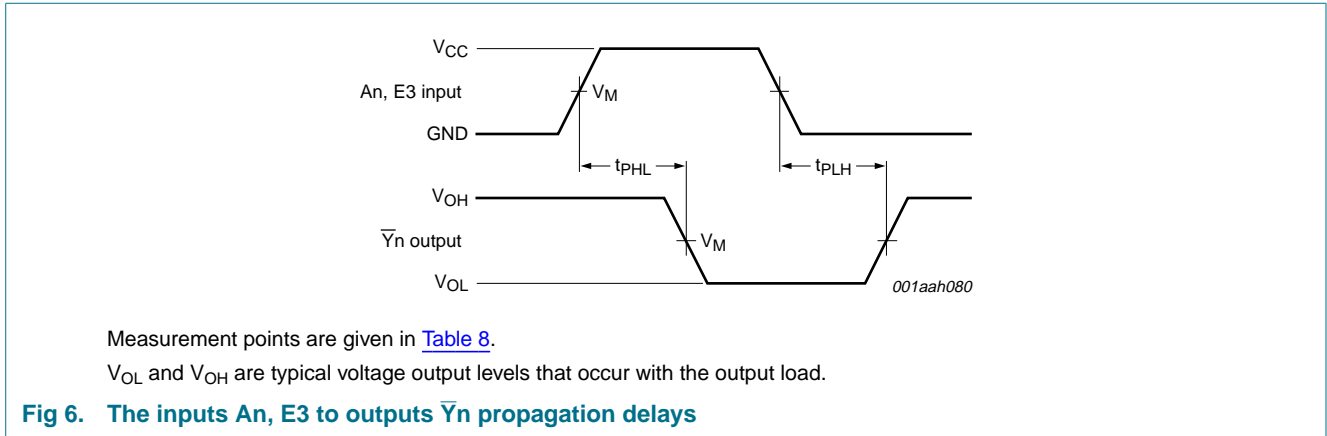
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V; For test circuit see Figure 8.*

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	An to $\bar{Y}_n$ ; see Figure 6 <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	75	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	26	44	-	55	ns
		V <sub>CC</sub> = 2.7 V	-	19	31	-	39	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	12	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	15	26	-	32	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	17	-	22	ns
		E3, $\bar{E}_n$ to $\bar{Y}_n$ ; see Figure 6 and Figure 7						
		V <sub>CC</sub> = 1.2 V	-	75	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	26	43	-	53	ns
		V <sub>CC</sub> = 2.7 V	-	19	30	-	38	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	14	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	15	25	-	31	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	19	-	24	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>i</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>	-	45	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V  
 N = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

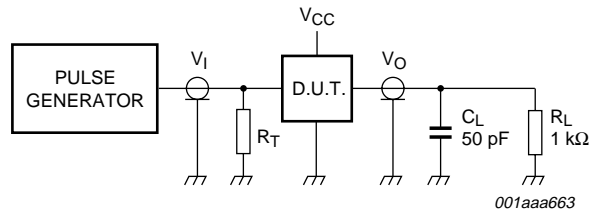
11. Waveforms



**Table 8. Measurement points**

Supply voltage $V_{CC}$	Input $V_M$	Output $V_M$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
$\geq 4.5$ V	$0.5V_{CC}$	$0.5V_{CC}$





Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

**Fig 8. Load circuit for switching times**

**Table 9. Test data**

Supply voltage	Input	$t_r, t_f$
$V_{CC}$	$V_I$	
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

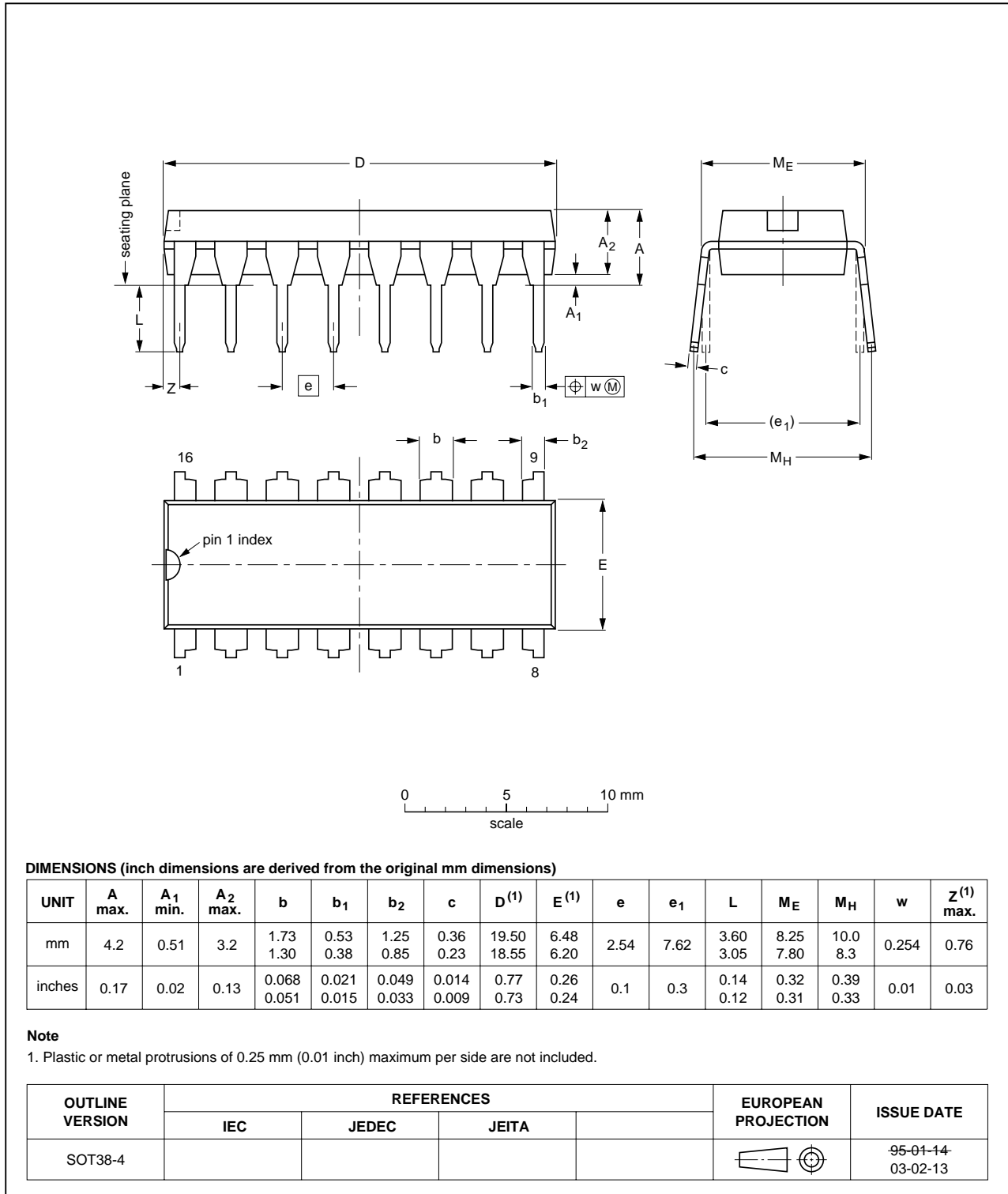


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

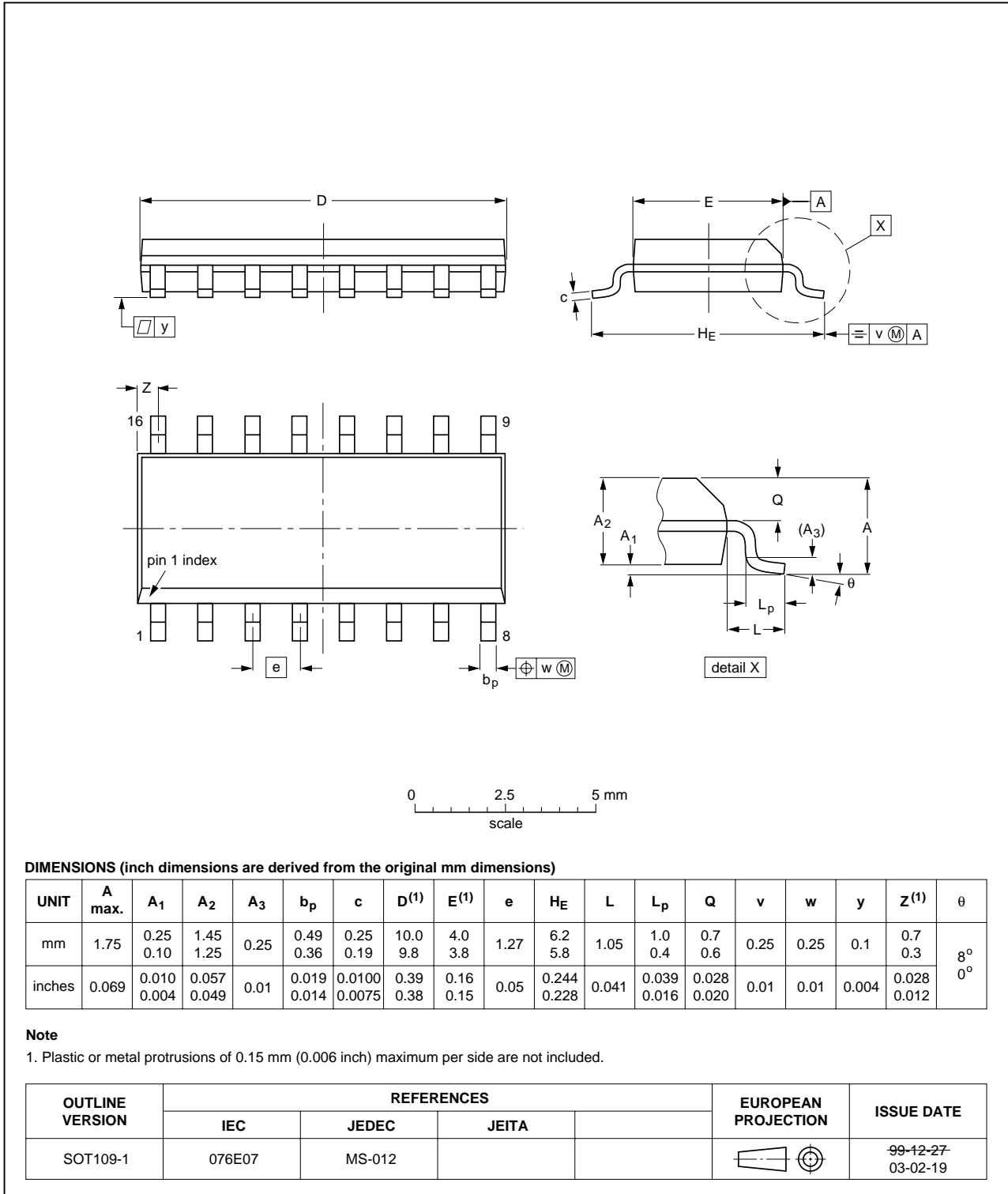
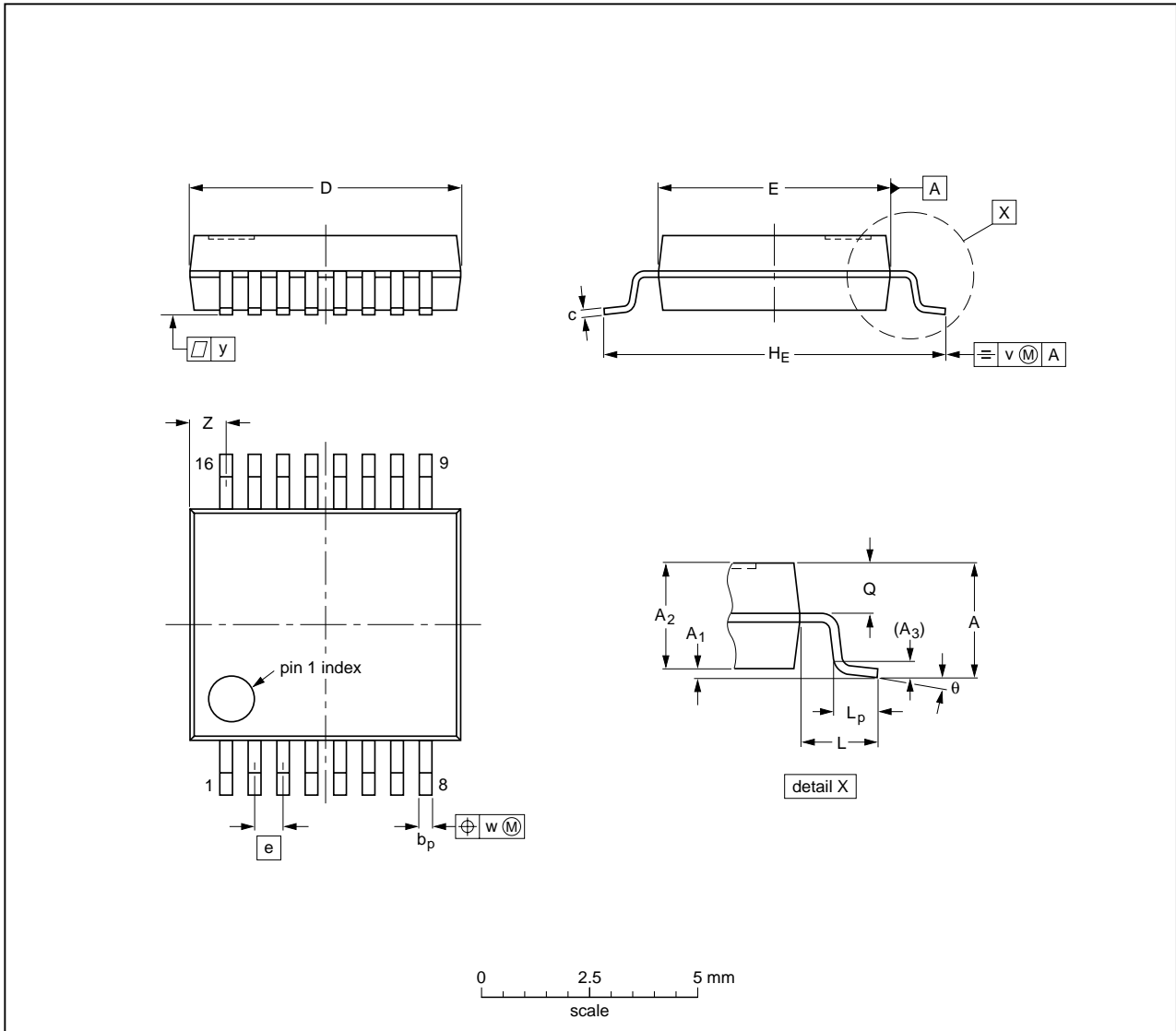


Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				99-12-27 03-02-19

Fig 11. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

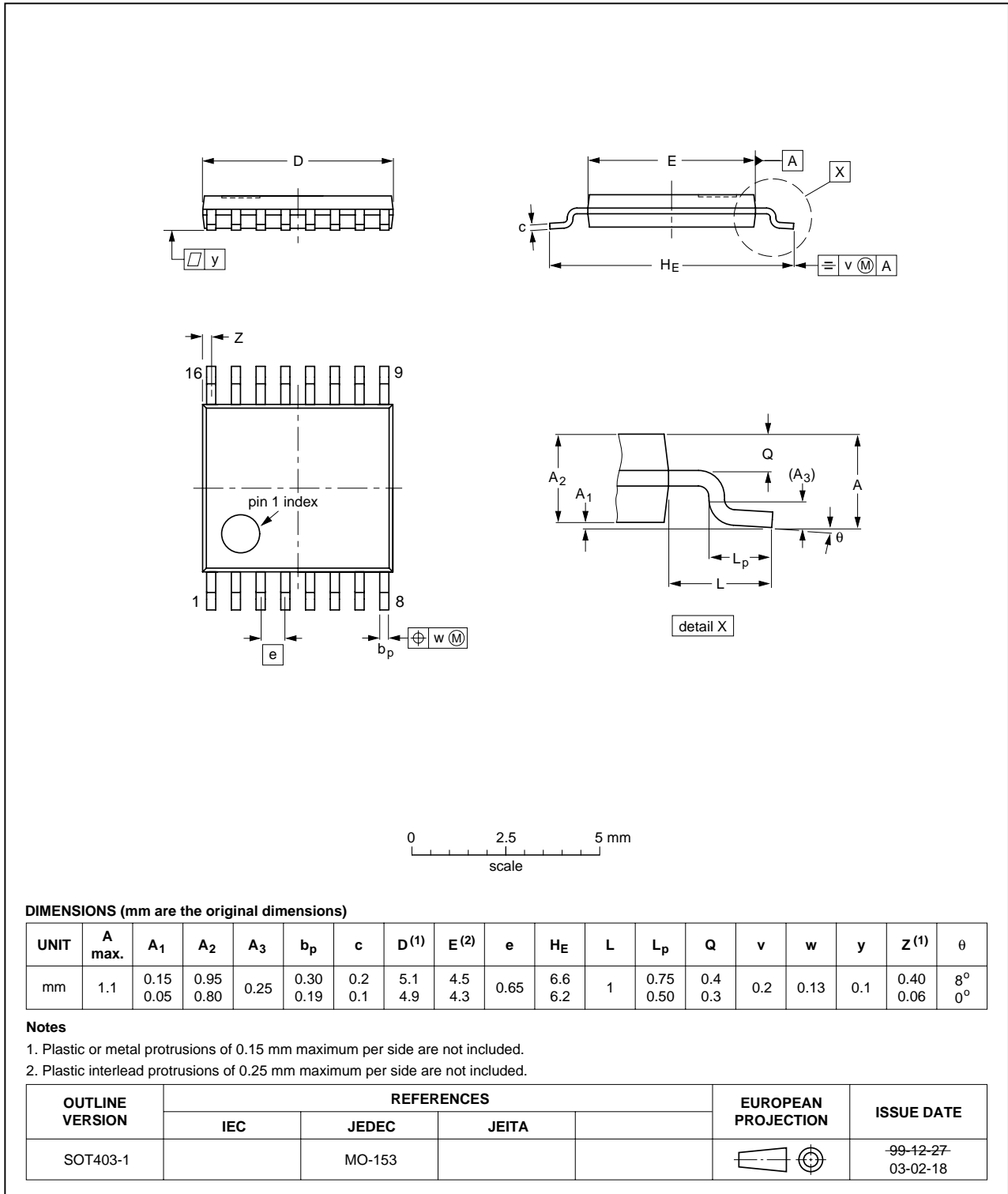
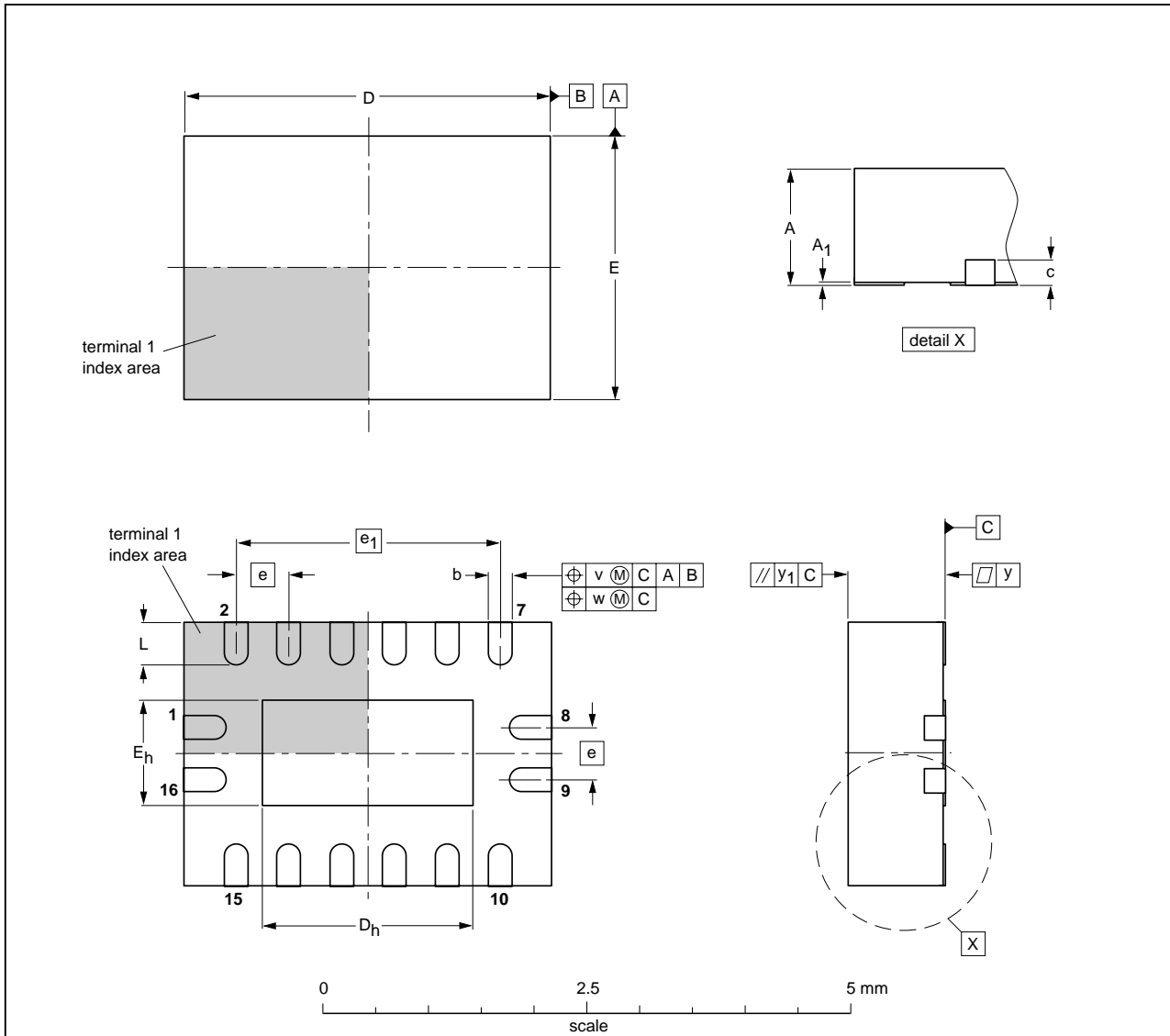


Fig 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT763-1	---	MO-241	---		02-10-17 03-01-27

Fig 13. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV138_3	20071115	Product data sheet	-	74LV138_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 3</a>: DHVQFN16 package added.</li> <li><a href="#">Section 8</a>: derating values added for DHVQFN16 package.</li> <li><a href="#">Section 12</a>: outline drawing added for DHVQFN16 package.</li> </ul>			
74LV138_2	19980428	Product specification	-	74LV138_1
74LV138_1	19970203	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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