

# DATA SHEET

**74LV257**

Quad 2-input multiplexer (3-State)

Product specification  
Supersedes data of 1997 Jun 06  
IC24 Data Handbook

1998 May 20



# Quad 2-input multiplexer (3-State)

# 74LV257

## FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Non-inverting data path
- Output capability: bus driver
- $I_{CC}$  category: MSI

## DESCRIPTION

The 74LV257 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT257.

The 74LV257 is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S). The data inputs from source 0 ( $1I_0$  to  $4I_0$ ) are selected when input S is LOW and the data inputs from source 1 ( $1I_1$  to  $4I_1$ ) are selected when S is HIGH. Data appears at the outputs ( $1Y$  to  $4Y$ ) in true (non-inverting) from the selected inputs. The 74LV257 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high impedance OFF-state when  $\overline{OE}$  is HIGH.

The logic equations for the outputs are:

$$1Y = \overline{OE} \times (1I_1 \times S + 1I_0 \times \overline{S})$$

$$2Y = \overline{OE} \times (2I_1 \times S + 2I_0 \times \overline{S})$$

$$3Y = \overline{OE} \times (3I_1 \times S + 3I_0 \times \overline{S})$$

$$4Y = \overline{OE} \times (4I_1 \times S + 4I_0 \times \overline{S})$$

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $nI_0, nI_1$ to $nY$ S to $nY$	$C_L = 15$ pF; $V_{CC} = 3.3$ V	10 14	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per gate	$V_I = \text{GND to } V_{CC}^1$	30	pF

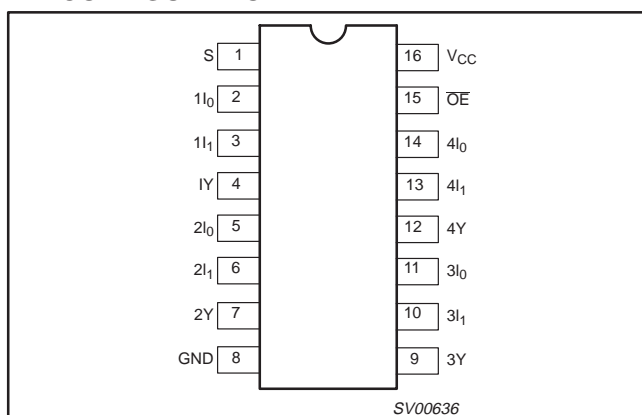
### NOTE:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV257 N	74LV257 N	SOT38-4
16-Pin Plastic SO	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV257 D	74LV257 D	SOT109-1
16-Pin Plastic SSOP Type II	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV257 DB	74LV257 DB	SOT338-1
16-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV257 PW	74LV257PW DH	SOT403-1

## PIN CONFIGURATION



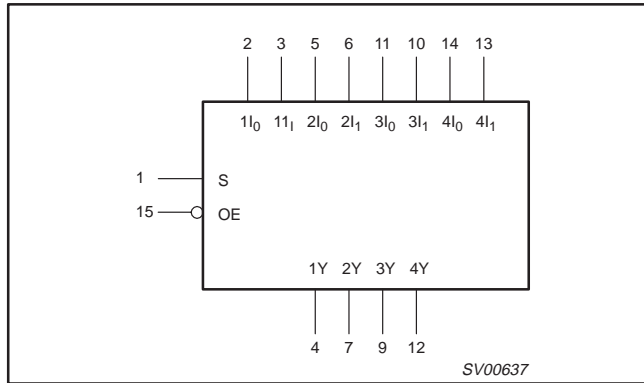
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	Data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	Data inputs from source 1
4, 7, 9, 12	$1Y$ to $4Y$	3-state multiplexer outputs
8	GND	Ground (0 V)
15	$\overline{OE}$	3-State output enable input (active LOW)
16	$V_{CC}$	Positive supply voltage

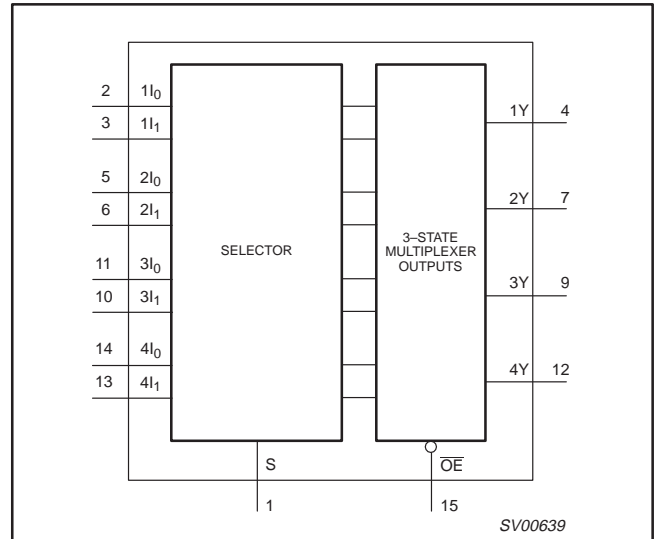
# Quad 2-input multiplexer (3-State)

# 74LV257

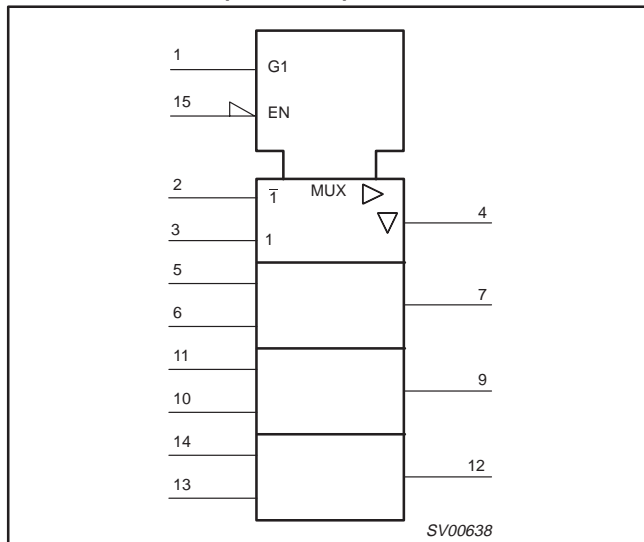
### LOGIC SYMBOL



### FUNCTIONAL DIAGRAM



### LOGIC SYMBOL (IEEE/IEC)



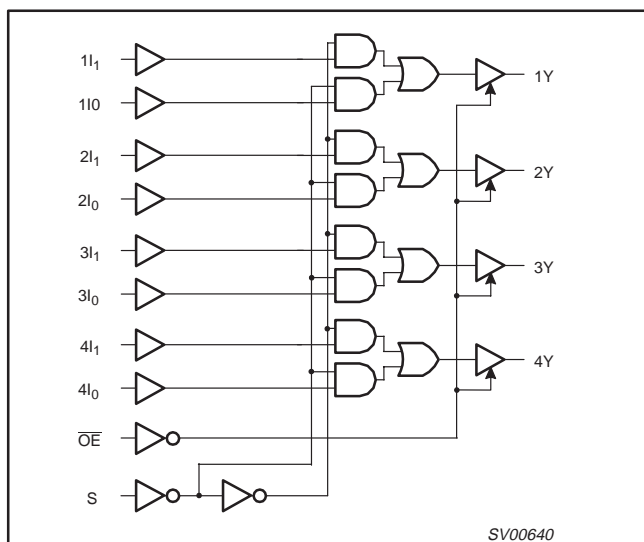
### FUNCTION TABLE

INPUTS				OUTPUTS
OE	S	nI <sub>0</sub>	nI <sub>1</sub>	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

#### NOTES:

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- Z = high impedance OFF-state

### LOGIC DIAGRAM



## Quad 2-input multiplexer (3-State)

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1	1.0	3.3	3.6	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$	– – –	– – –	500 200 100	ns/V

## NOTE:

- The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 3.6V$ .

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – bus driver outputs		70	mA
$T_{stg}$	Storage temperature range		–65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Quad 2-input multiplexer (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2 V	0.9			0.9		V
		V <sub>CC</sub> = 2.0 V	1.4			1.4		
		V <sub>CC</sub> = 2.7 to 3.6 V	2.0			2.0		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2 V			0.3		0.3	V
		V <sub>CC</sub> = 2.0 V			0.6		0.6	
		V <sub>CC</sub> = 2.7 to 3.6 V			0.8		0.8	
V <sub>OH</sub>	HIGH level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA		1.2				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	1.8	2.0		1.8		
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.5	2.7		2.5		
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA	2.8	3.0		2.8		
V <sub>OH</sub>	HIGH level output voltage; BUS driver outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 8mA	2.40	2.82		2.20		V
V <sub>OL</sub>	LOW level output voltage; all outputs	V <sub>CC</sub> = 1.2 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0				V
		V <sub>CC</sub> = 2.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA		0	0.2		0.2	
V <sub>OL</sub>	LOW level output voltage; BUS driver outputs	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8mA		0.20	0.40		0.50	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND			1.0		1.0	µA
I <sub>oz</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND			5		10	µA
I <sub>CC</sub>	Quiescent supply current; MSI	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			20.0		160	µA
ΔI <sub>CC</sub>	Additional quiescent supply current per input	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V			500		850	µA

**NOTE:**1. All typical values are measured at T<sub>amb</sub> = 25°C.

# Quad 2-input multiplexer (3-State)

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## AC CHARACTERISTICS

GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 1\text{K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				V <sub>CC</sub> (V)	MIN	TYP <sup>1</sup>	MAX	MIN	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nI <sub>0</sub> to nY nI <sub>1</sub> to nY	Figure 1	1.2		65				ns
			2.0		22	43		51	
			2.7		16	31		38	
			3.0 to 3.6		12 <sup>2</sup>	25		30	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay S to nY	Figure 1	1.2		85				ns
			2.0		29	56		66	
			2.7		21	41		49	
			3.0 to 3.6		16 <sup>2</sup>	33		39	
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time OE to nY	Figure 2	1.2		60				ns
			2.0		20	39		46	
			2.7		15	29		34	
			3.0 to 3.6		11 <sup>2</sup>	23		27	
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time OE to nY	Figure 2	1.2		65				ns
			2.0		24	40		49	
			2.7		18	32		37	
			3.0 to 3.6		14 <sup>2</sup>	26		30	

**NOTES:**

1. Unless otherwise stated, all typical values are measured at T<sub>amb</sub> = 25°C
2. Typical values are measured at V<sub>CC</sub> = 3.3 V.

## AC WAVEFORMS

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$   
 $V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$   
 $V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$   
 $V_X = V_{OL} + 0.1 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$   
 $V_Y = V_{OH} - 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$   
 $V_Y = V_{OH} - 0.1 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

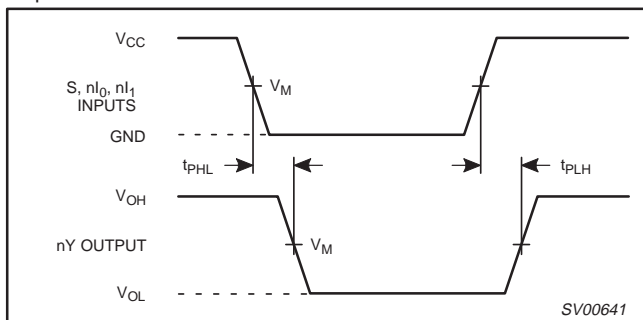


Figure 1. Input (S, nI<sub>0</sub>, nI<sub>1</sub>) to output (nY) propagation delays.

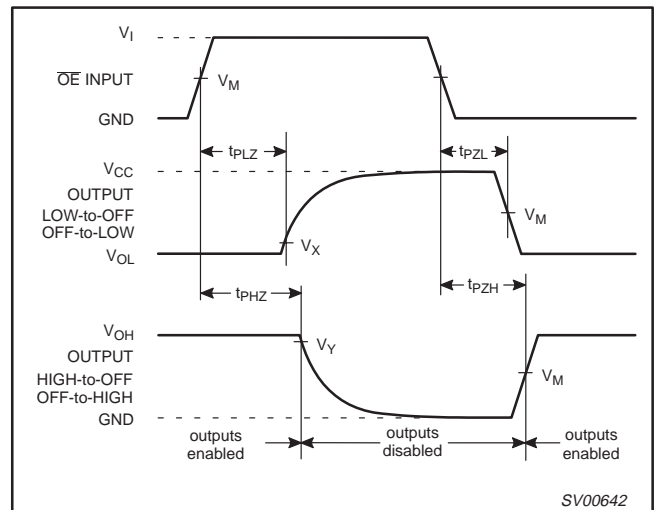


Figure 2. 3-State enable and disable times.

# Quad 2-input multiplexer (3-State)

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## TEST CIRCUIT

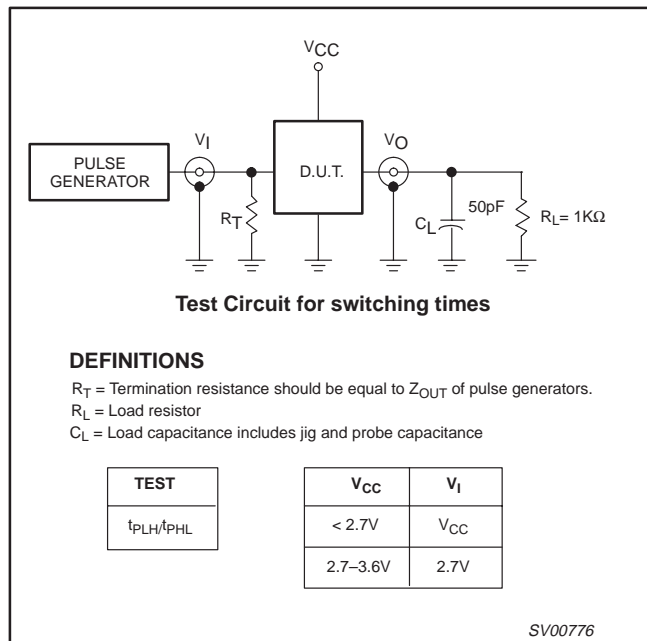


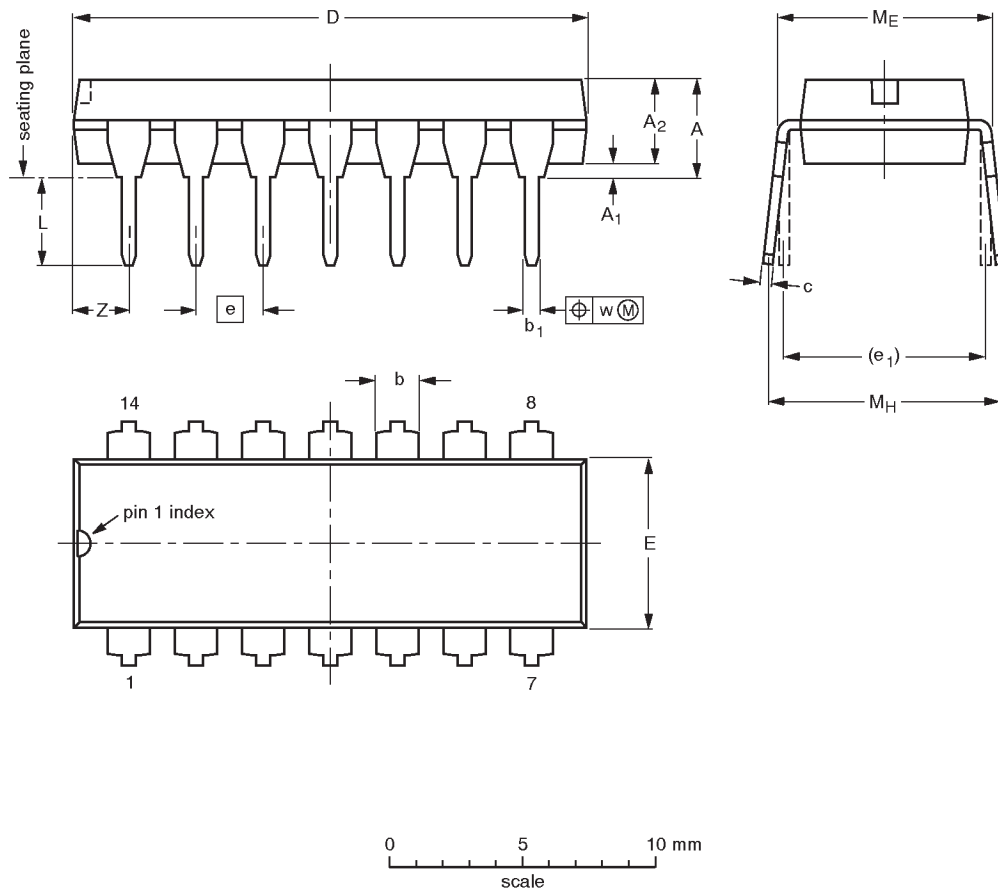
Figure 3. Load circuitry for switching times.

Quad 2-input multiplexer (3-State)

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

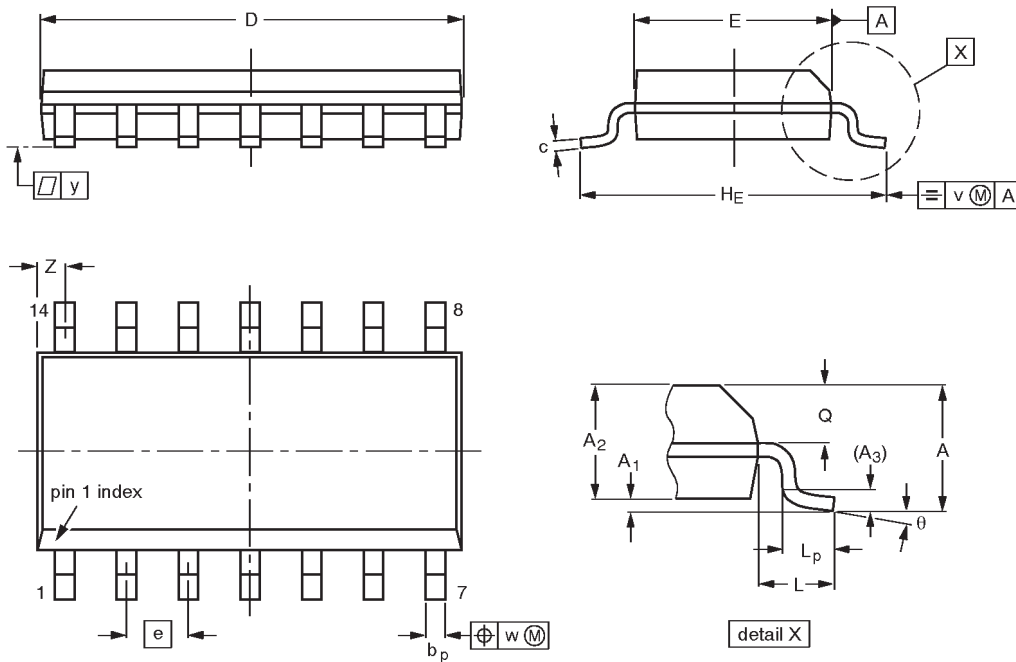


Quad 2-input multiplexer (3-State)

74LV257

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.25	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.0039	0.0098 0.049	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

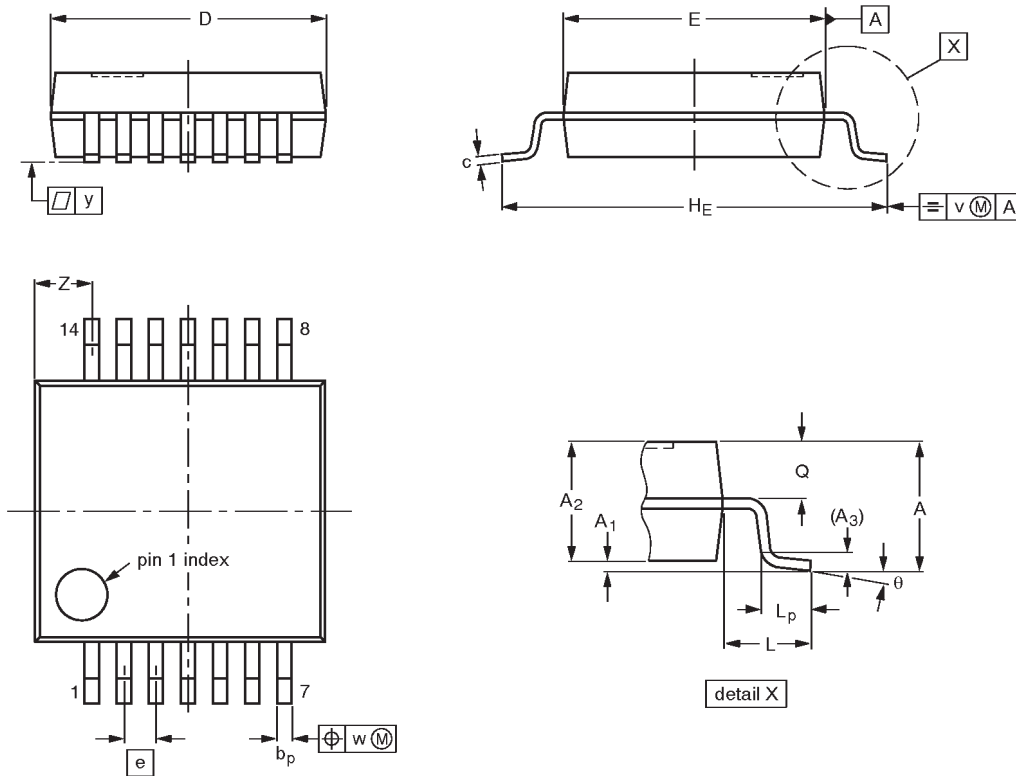
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	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-13 95-01-23

Quad 2-input multiplexer (3-State)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

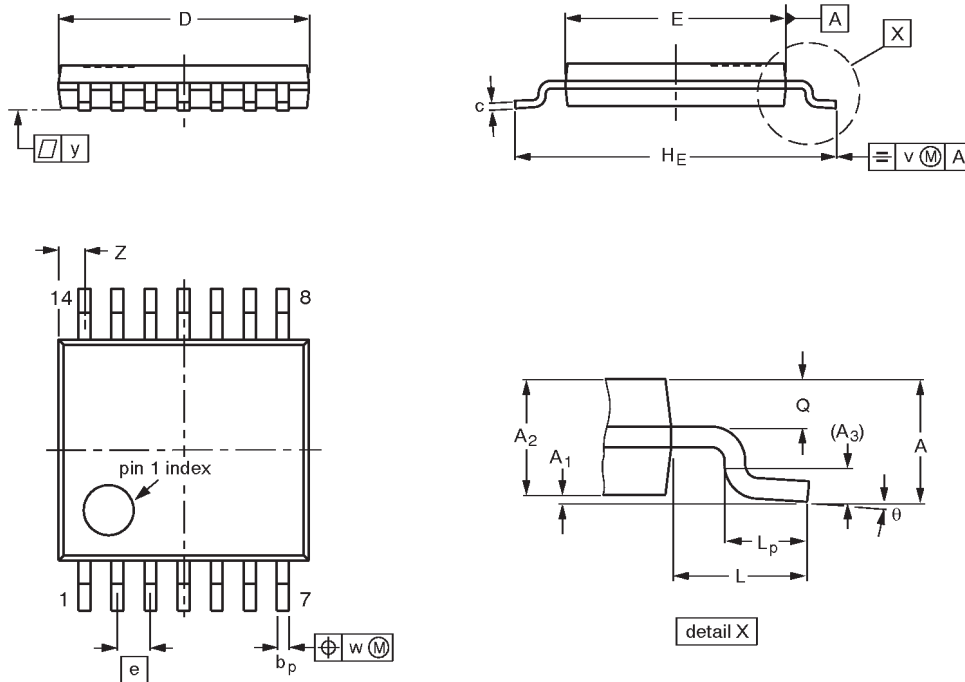
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				95-02-04 96-01-18

Quad 2-input multiplexer (3-State)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-94-07-12 95-04-04

## Quad 2-input multiplexer (3-State)

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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