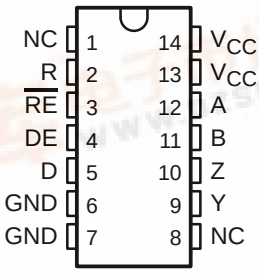
SN75ALS181
DIFFERENTIAL DRIVER AND RECEIVER PAIR

SLLS152B – DECEMBER 1992 – REVISED APRIL 2003

- **Meets TIA/EIA-422-B, TIA/EIA-485-A, and CCITT Recommendations V.11 and X.27**
- **Low Supply-Current Requirements . . . 30 mA Max**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Common-Mode Output Voltage Range of –7 V to 12 V**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Receiver Common-Mode Input Voltage Range of ±12 V**
- **Operates From Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

N OR NS PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The SN75ALS181 is a differential driver and receiver pair designed for bidirectional data communication on multipoint bus transmission lines. The design provides for balanced transmission lines and meets TIA/EIA-422-B and TIA/EIA-485-A, and CCITT recommendations V.10, V.11, X.26, and X.27.

The SN75ALS181 combines a 3-state differential line driver and a differential-input line receiver that operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage changes, making the device suitable for party-line applications.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	SN75ALS181N	SN75ALS181N
	SOP (NS)	Reel of 2000	SN75ALS181NSR	75ALS181

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

EACH DRIVER

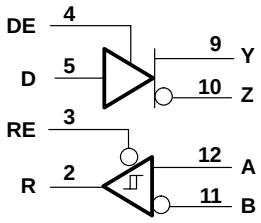
INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

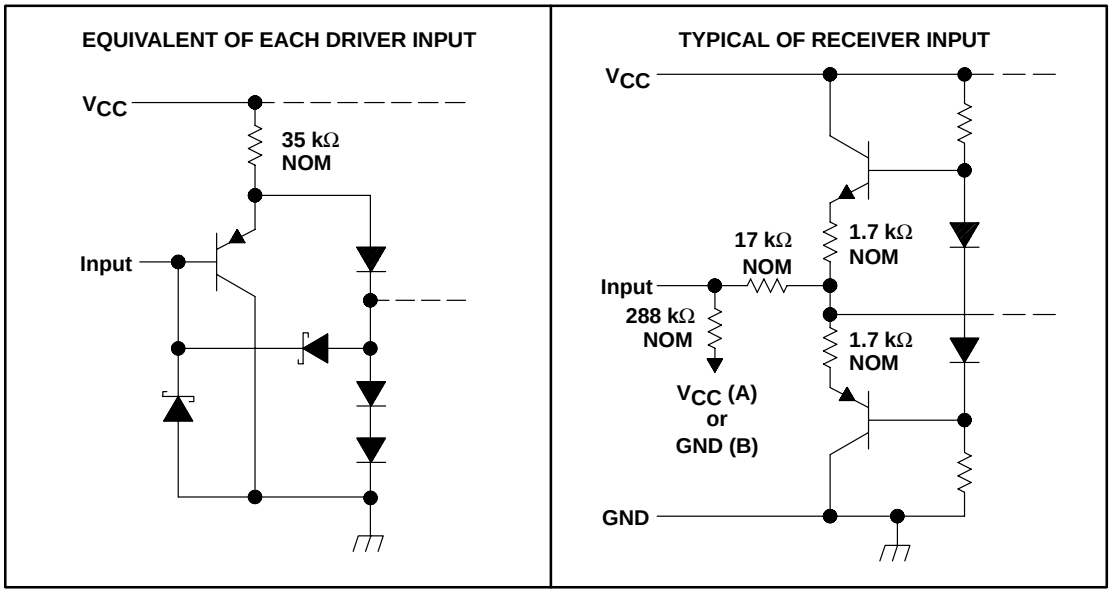
DIFFERENTIAL A–B	ENABLE $\overline{RE}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

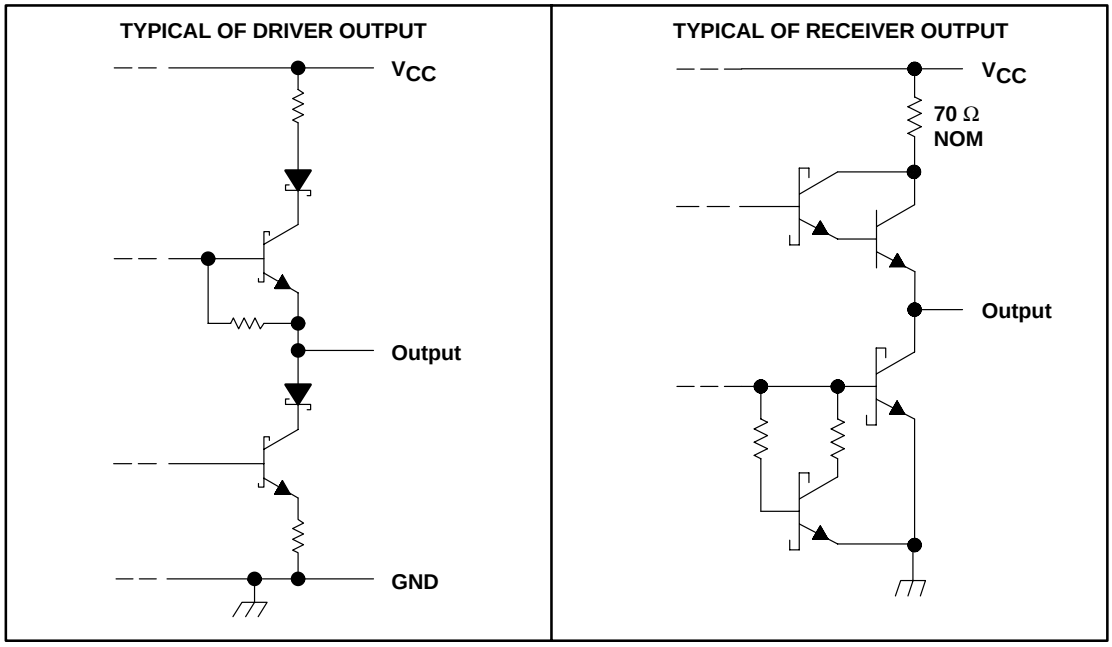
logic diagram (positive logic)



schematics of inputs



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, D, DE, and $\overline{RE}$ inputs . . . . . 7 V
Output voltage range, driver . . . . . –9 V to 14 V
Input voltage range, receiver . . . . . –14 V to 14 V
Receiver differential input voltage range (see Note 2) . . . . . –14 V to 14 V
Package thermal impedance, θ_{JA} (see Notes 3 and 4): N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{OC}	Common-mode output voltage (see Note 5)	Driver	–7		12	V
V_{IC}	Common-mode input voltage (see Note 5)	Receiver	–12		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	μA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		0		70	°C

NOTE 5: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this table for common-mode output voltage level only.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See Figure 1	1/2 V_{OD1}			V
				2			
		R_L = 54 Ω		1.5	2.3	5	
$\|V_{OD3}\|$	Differential output voltage	V_{test} = –7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 6)	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,	See Figure 1			3	V
						–1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 6)	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V,	See Note 7			±100	µA
I_{IH}	High-level input current	V_{IH} = 2.4 V				20	µA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
		V_O = 0 V				–150	
I_{CC}	Supply current (total package)	No load	Outputs enabled		21	30	mA
			Outputs disabled		14	21	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 6. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

7. This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
t_{dD}	Differential output delay time, t_{dDH} or t_{dDL}	R_L = 54 Ω,	C_L = 50 pF,	See Figure 3	9	13	20	ns
$t_{sk(p)}$	Pulse skew ($\|t_{dDH} - t_{dDL}\|$)	R_L = 54 Ω,	C_L = 50 pF,	See Figure 3		1	8	ns
t_t	Differential output transition time	R_L = 54 Ω,	C_L = 50 pF,	See Figure 3	3	10	16	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4			36	53	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5			39	56	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4			20	31	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5			9	20	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage, differential input	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{T-}	Negative-going threshold voltage, differential input	V_O = 0.5 V,	I_O = 8 mA		–0.2			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 μA,	See Figure 6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA,	See Figure 6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V, See Note 7	V_I = 12 V				1	mA
			V_I = –7 V				–0.8	
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.4 V					–100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0 V		–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled			21	30	mA
			Outputs disabled			14	21	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 7: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (unless otherwise noted) (see Figure 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V	10	16	25	ns
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V	10	16	25	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)	V_{ID} = –1.5 V to 1.5 V		1	8	ns
t_{PZH}	Output enable time to high level			7	15	ns
t_{PZL}	Output enable time to low level			9	19	ns
t_{PHZ}	Output disable time from high level			18	27	ns
t_{PLZ}	Output disable time from low level			10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

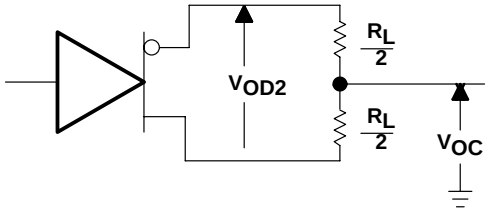


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

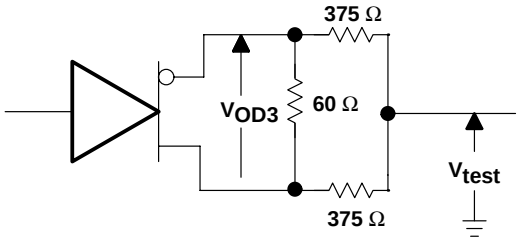
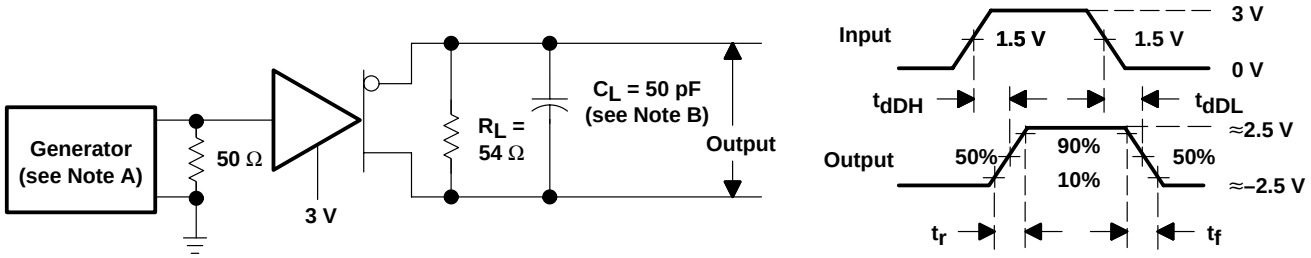


Figure 2. Driver Circuit, V_{OD3}

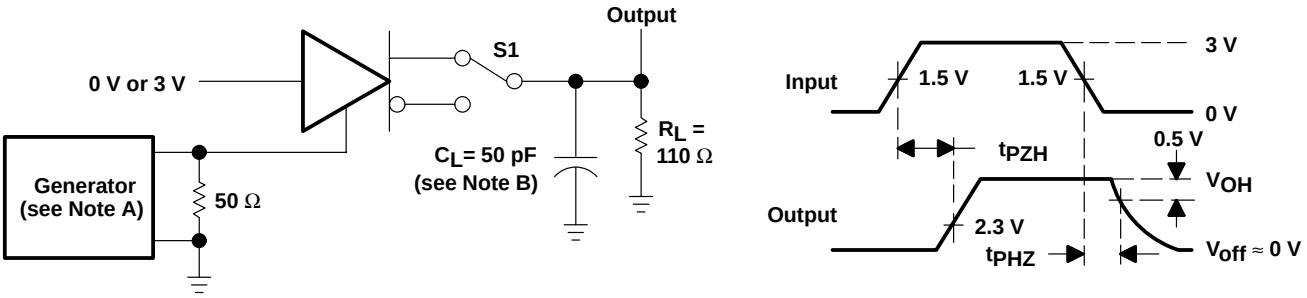


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Differential-Output Delay and Transition Times

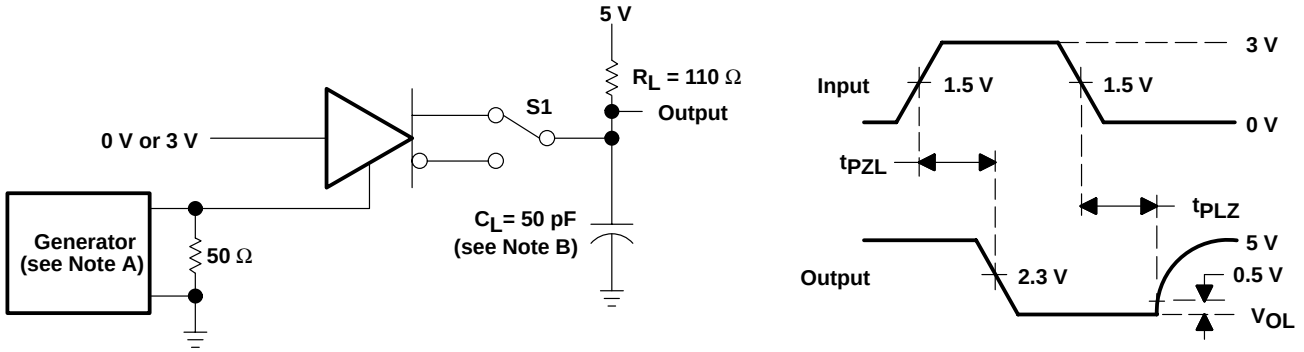
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Enable and Disable Times



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Enable and Disable Times

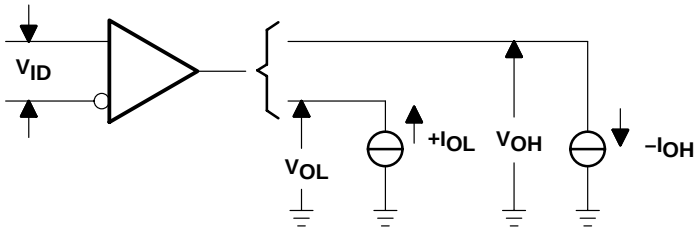
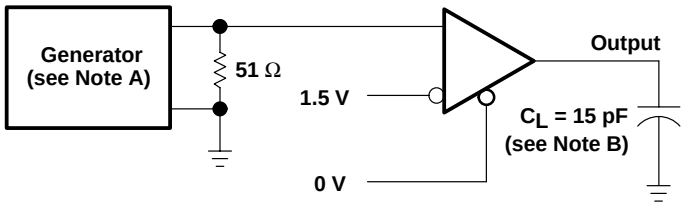
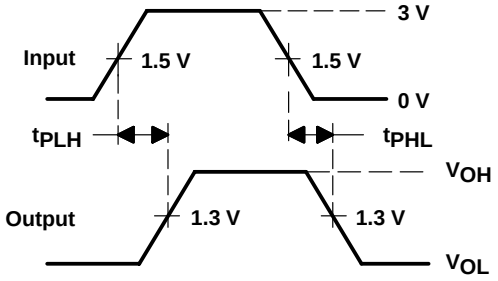


Figure 6. Receiver, V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

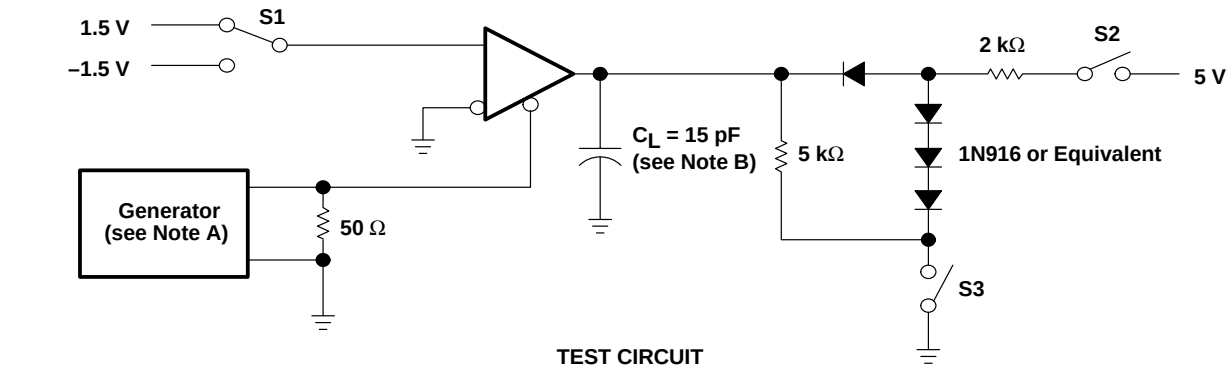


VOLTAGE WAVEFORMS

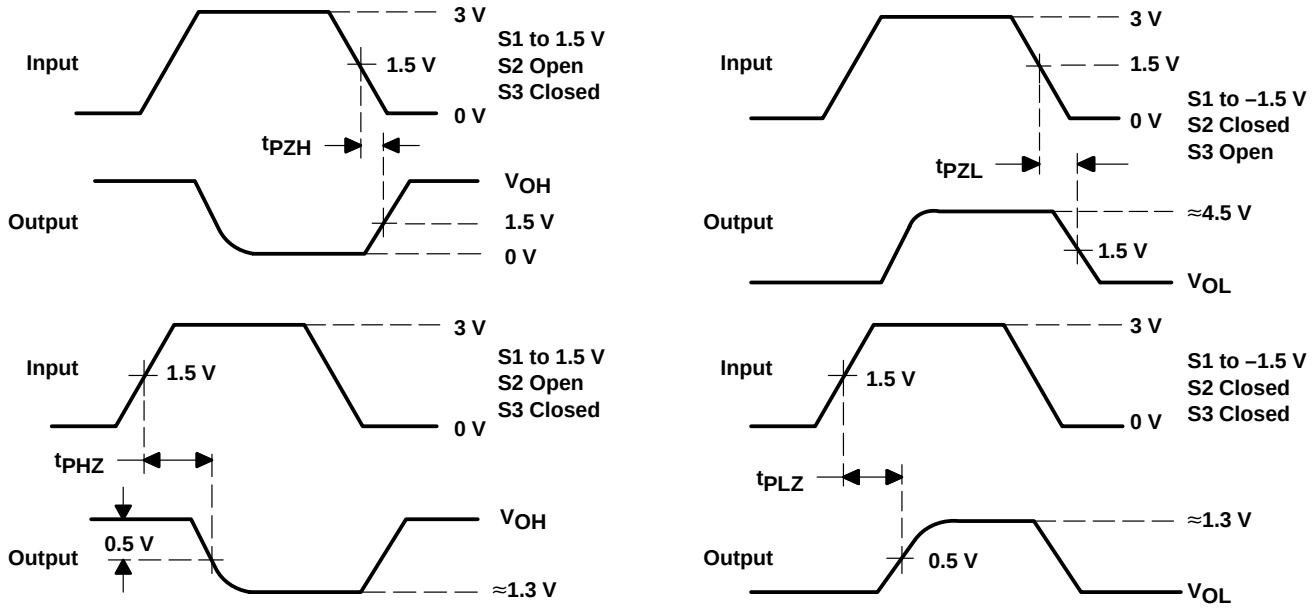
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Propagation-Delay Times

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Output Enable and Disable Times

PACKAGE OPTION ADDENDUM

18-Jul-2006

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75ALS181N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS181NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS181NSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
SN75ALS181NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS181NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

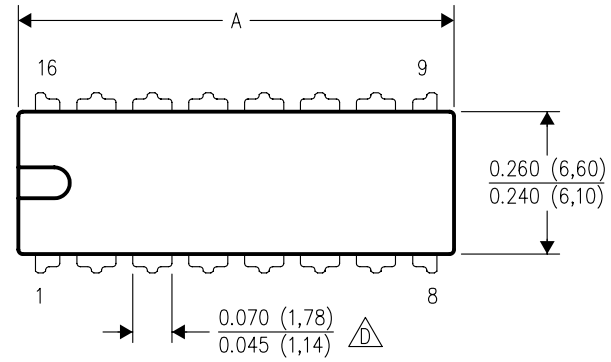
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

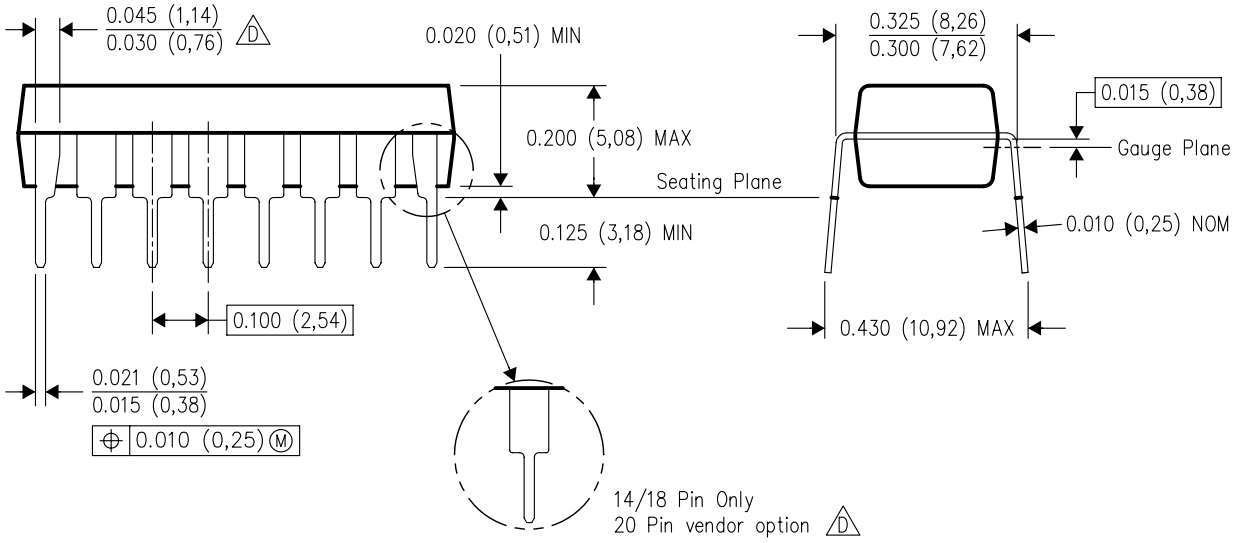
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



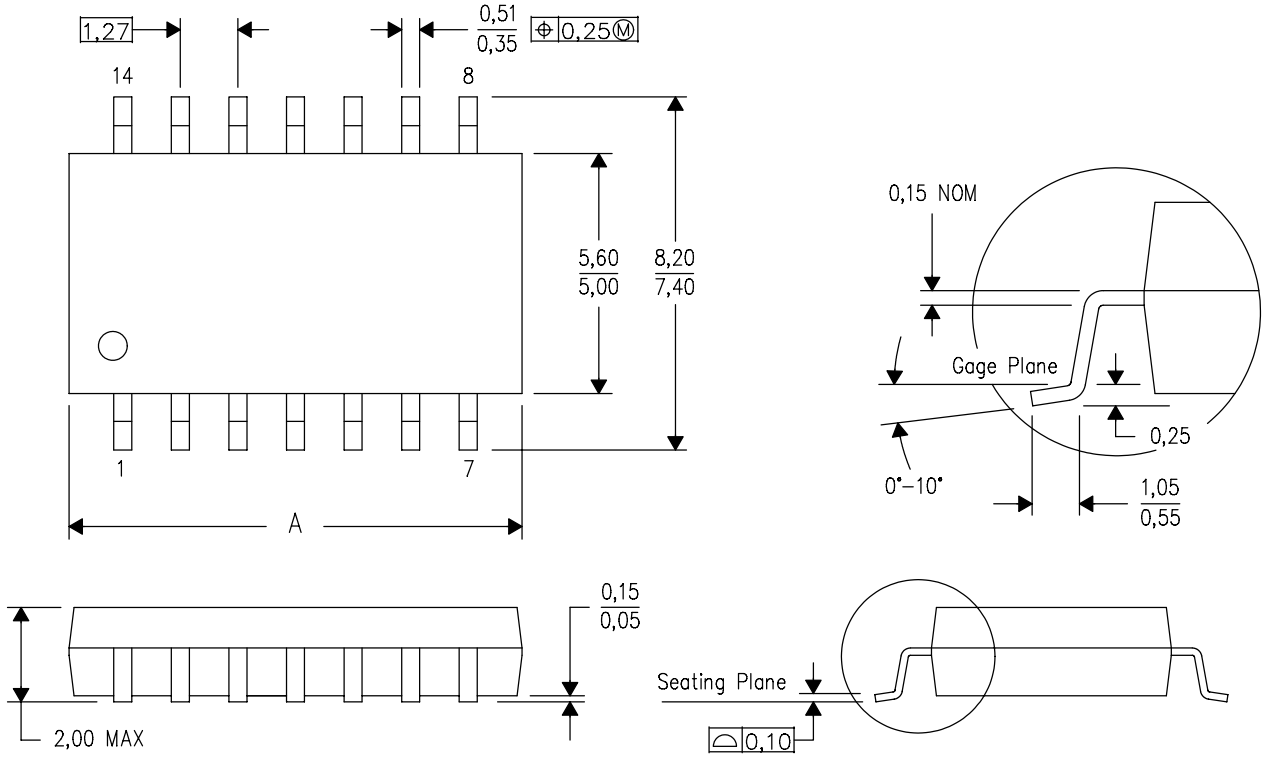
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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