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MITSUBISHI 16-BIT SINGLE-CHIP MICROCOMPUTER
7700 FAMILY / 7700 SERIES

7733 Group
7735 Group
7736 Group

User's Manual

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Preface

This manual describes the hardware of the Mitsubishi CMOS 16-bit microcomputers 7733/7735/7736 Group. After reading this manual, the user will be able to understand the functions, so that the capabilities of the microcomputers can fully be utilized.

For details concerning the software for the 7733/7735/7736 Group, refer to the 7700 Family Software Manual.

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BEFORE USING THIS MANUAL

1. INTRODUCTION

This manual consists of the following: PART 1: 7733 Group, PART 2: 7735 Group, and PART 3: 7736 Group.

The peripheral functions are common to all of these groups, but the external bus mode differs according to the group, as follows:

- 7733 Group: external bus mode A is assigned.
- 7735 Group: external bus mode B is assigned.
- 7736 Group: external bus mode A or B is selectable.

In parts 2 and 3, only the differences occurring between the 7735/7736 Group and the 7733 Group are described. Also, the chapter, section, table and figure numbers are the same as those in part 1 and the differences are described by the section.

PART 1: 7733 Group

● Chapter 1. OVERVIEW through Chapter 17. APPLICATIONS

The common functions of the 7733 Group microcomputers are described.

The M37733MHBXXXFP is used as a typical microcomputer in this group to describe all common functions.

● Chapter 18. LOW VOLTAGE VERSION

Read this chapter when using the microcomputers with the electrical characteristics indicated by "L." (See page 1-2 in part 1.) Ex.: M37733MHLXXXHP

The differences between the M37733MHLXXXHP, which is a typical low voltage version of the 7733 Group, and the M37733MHBXXXFP are described.

● Chapter 19. BUILT-IN PROM VERSION

Read this chapter when using the microcomputers with the memory type indicated by "E." (See page 1-2 in part 1.) Ex.: M37733EHBXXXFP

The differences between the M37733EHBXXXFP, which is a typical built-in PROM version of the 7733 Group, and the M37733MHBXXXFP are described.

● Chapter 20. EXTERNAL ROM VERSION

Read this chapter when using the microcomputers with the memory type indicated by "S." (See page 1-2 in part 1.) Ex.: M37733S4BFP

The differences between the M37733S4BFP, which is a typical external ROM version of the 7733 Group, and the M37733MHBXXXFP are described.

● APPENDIX

Practical information for using the 7733 Group is described .

PART 2: 7735 Group, PART 3: 7736 Group

Refer to the table on the next page.

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2: When referring to the chapters and sections listed below, use the following guide: External bus mode A: refer to part 1, External bus mode B: refer to part 2.

- **Chapter 11. STOP AND WAIT MODES**
- **Chapter 12. CONNECTING EXTERNAL DEVICES"**
- **Chapter 15. ELECTRICAL CHARACTERISTICS" (electrical characteristics related to the external bus mode)**
- **Paragraph 17.1 Memory expansion**
- **Chapter 18. LOW VOLTAGE VERSION (electrical characteristics related to the external bus mode)**
- **Paragraph 18.6 Applications**

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2. NOTES

● For product expansion information, refer to the latest catalog and data book, or contact the appropriate office, as listed in "CONTACT ADDRESSES FOR FURTHER INFORMATION" on the last page.

● Always refer to the latest data book for electrical characteristics.

● This manual does not include the forms listed below. When necessary, copy the corresponding page of the latest data book, or contact the appropriate office, as listed in "CONTACT ADDRESSES FOR FURTHER INFORMATION":

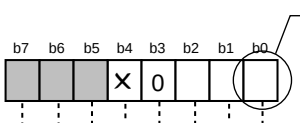
- MASK ROM ORDER CONFIRMATION FORM
- PROM ORDER CONFIRMATION FORM
- MARK SPECIFICATION FORM

● For details concerning development support tools, refer to the latest data book of development support tools.

● For details concerning software, refer to the 7700 Family Software Manual.

3. REGISTER STRUCTURE

Below is the structure diagram for all registers.



*2 *3

Bit	Bit name	Functions	At reset	RW
0	... select bit	0 : ... 1 : ...	0	RW
1	... select bit	0 : ... 1 : ... The value is “0” at reading.	Undefined	WO
2	... flag	0 : ... 1 : ...	0	RO
3	Fix this bit to “0.”		0	RW
4	This bit is ignored in ... mode.		0	RW
7 to 5	Not implemented.		Undefined	–

*4

*1

Blank : Set to “0” or “1” according to the usage.
0 : Set to “0” at writing.
1 : Set to “1” at writing.
X : Ignored depending on the mode or state. It may be “0” or “1.”
▨ : Not implemented.

*2

0 : “0” immediately after reset.
1 : “1” immediately after reset.
Undefined : Undefined immediately after reset.

*3

RW : It is possible to read the bit state at reading. The written value becomes valid.
RO : It is possible to read the bit state at reading. The written value becomes invalid. Accordingly, the written value may be “0” or “1.”
WO : The written value becomes valid. It is impossible to read the bit state. The value is undefined at reading. However, when [“0” at reading] is indicated in the “Function” or “Note” column, the bit is always “0” at reading.(See to *4 above.)
— : It is impossible to read the bit state. The value is undefined at reading. However, when [“0” at reading] is indicated in the “Function” or “Note” column, the bit is always “0” at reading.(See to *4 above.)
The written value becomes invalid. Accordingly, the written value may be “0” or “1.”

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GLOSSARY

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PART 1

7733 Group

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PART 1 7733 Group

The 7733 Group is described in part 1.

For the 7735 Group, refer to part **"2. 7735 Group."** In part 2, the differences between the 7735 Group and the 7733 Group are mainly described.

For the 7736 Group, refer to part **"3. 7736 Group."** In part 3, the differences between the 7736 Group and the 7733 Group are mainly described.

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CHAPTER 1
OVERVIEW

1.1 Performance overview
1.2 Pin configuration
1.3 Pin description
1.4 Block diagram

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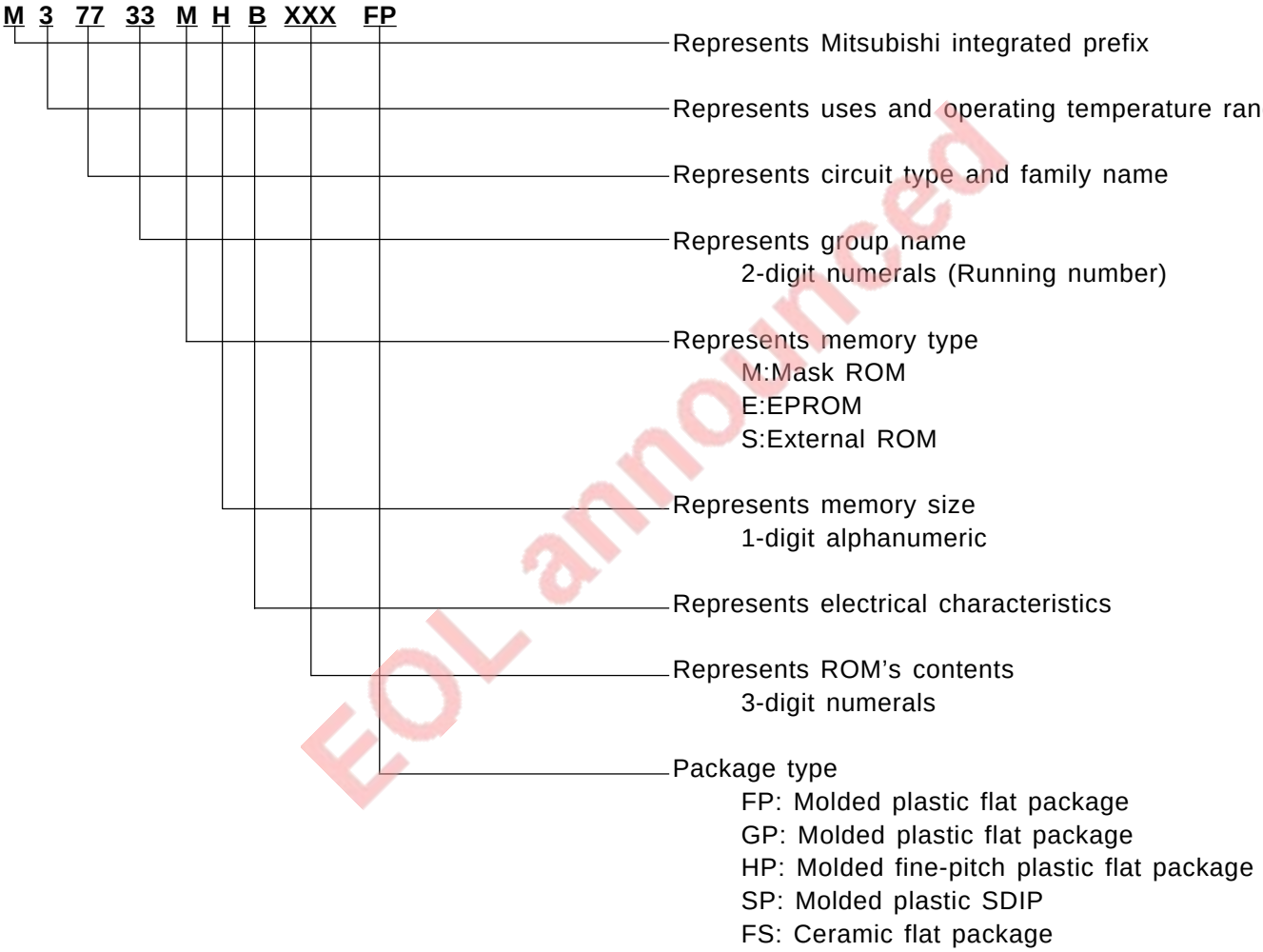
OVERVIEW

The 7733 Group is a 16-bit single-chip microcomputer designed with high-performance CMOS silicon gate technology. It is housed in an 80-pin plastic molded flat package.
This single-chip microcomputer has a large 16-Mbyte accessible space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for communication and office equipment controllers.

❋ About details concerning each microcomputer's development state of the 7733 Group, inquire **"CONTACT ADDRESSES FOR FURTHER INFORMATION"** described last.
❋ Functional codes of the 7733 Group are described below.



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1.1 Performance overview

Table 1.1.1 lists the M37733MHBXXXFP's performance overview.

Table 1.1.1 M37733MHBXXXFP's performance overview

Items		Performance
Number of basic instructions		103
The minimum instruction execution time		160 ns (When f(XIN) = 25 MHz and the main clock is the system clock)
Main-clock frequency f(XIN)		25 MHz (Max.) **(Note 3)**
Sub-clock frequency f(XCIN)		32.768 kHz (Typ.)
Memory size	ROM	124 Kbytes
	RAM	3968 bytes
Programmable I/O ports	Ports P0–P2, P4–P8	8 bits × 8
	Port P3	4 bits × 1
Multifunction timers	Timers A0–A4	16 bits × 5
	Timers B0–B2	16 bits × 3
Serial I/O	UART0–UART2	(UART or clock synchronous serial I/O) × 3
A-D converter		(10-bit successive approximation method) × 1 (8 channels)
Watchdog timer		12 bits × 1
Interrupts		3 external, 16 internal (By software, one of interrupt priority levels 0 to 7 can be set for each interrupt)
Clock generating circuits	Main-clock oscillation circuit	Built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator.)
	Sub-clock oscillation circuit	Built-in (externally connected to a quartz-crystal oscillator)
Power source voltage		5 V ± 10% (When the main clock is the system clock)
		2.7 V to 5.5 V (When the sub clock is the system clock)
Power consumption in single-chip mode		47.5 mW (When f(XIN) = 25 MHz, VCC = 5 V, and the main clock is the system clock, Typ.)
		250 μW (When f(XCIN) = 32 kHz, VCC = 5 V, the sub clock is the system clock, and the main clock is stopped, Typ.)
Port input/output characteristics	Input/Output withstand voltage	5 V
	Output current	5 mA
Memory expansion		Possible (Maximum of 16 Mbytes)
Operating temperature range		–20 °C to +85 °C
Device structure		High-performance CMOS silicon gate process
Package		80-pin plastic molded QFP

Notes 1: All of the 7733 Group microcomputers are the same except for package type, memory type, memory size, and electrical characteristics.
2: For the low voltage version, refer to chapter **"18. LOW VOLTAGE VERSION."**
3: When the main clock division selection bit = "1," the maximum value of f(XIN) = 12.5 MHz.

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1.2 Pin configuration

Figure 1.2.1 shows the M37733MHBXXXFP pin configuration.

Note: For the low voltage version, refer to chapter **"18. LOW VOLTAGE VERSION."**

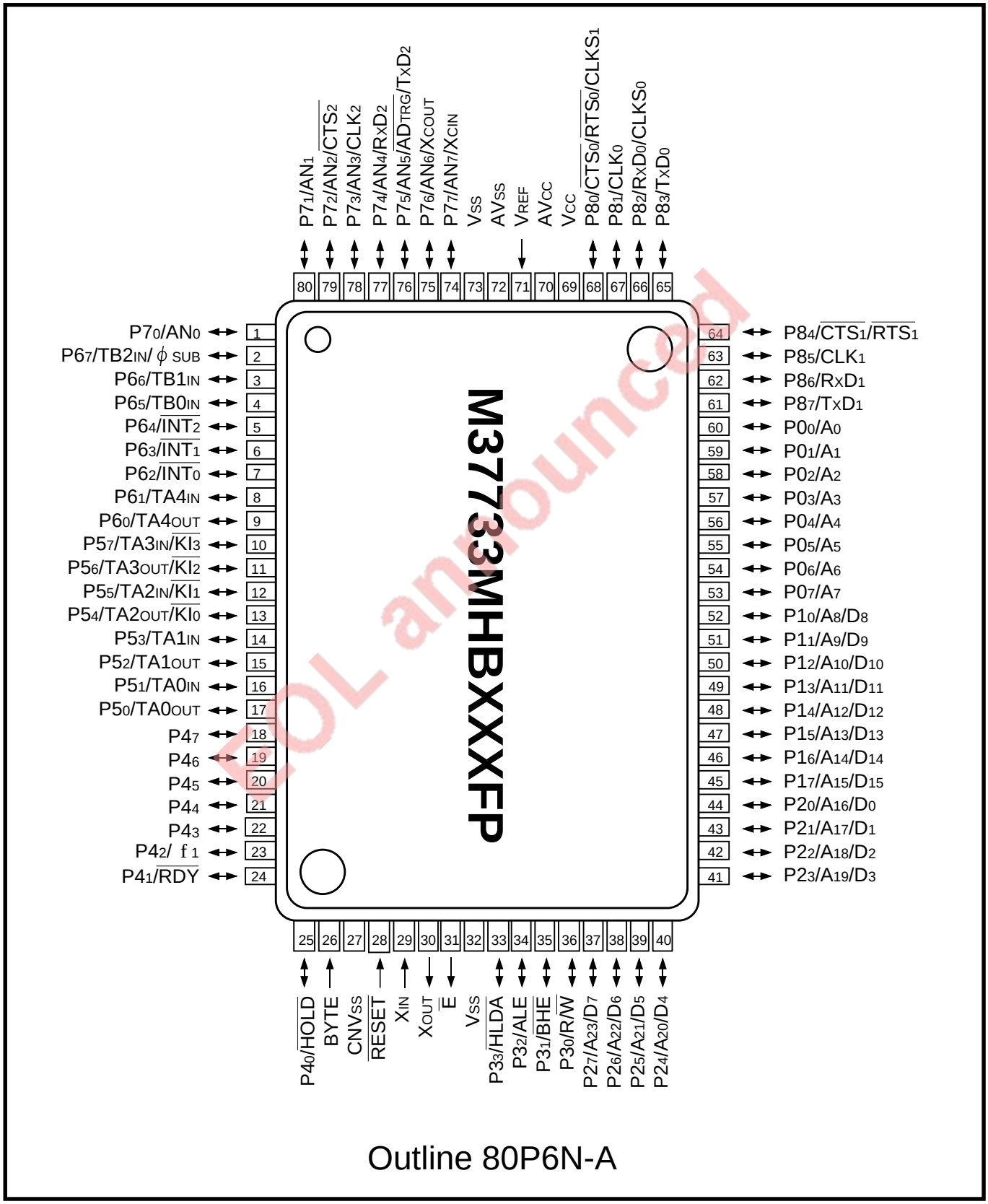

Fig. 1.2.1 M37733MHBXXXFP pin configuration (Top view)

1.3 Pin description

Tables 1.3.1–1.3.3 list the pin description. Note that the pin description of the built-in PROM version in the EPROM mode is described in section **"19.1 EPROM mode."**

Table 1.3.1 Pin description (1)

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power source input		To pin V_{CC}, apply 5 V±10% **(Note)** (When the main clock is the system clock) or 2.7 V to 5.5 V (When the sub clock is the system clock). To pin V_{SS}, apply 0 V.
CNVSS	CNVSS	Input	This pin switches the processor mode. **[Single-chip Mode] [Memory Expansion Mode]** Connect to pin V_{SS}. **[Microprocessor Mode]** Connect to pin V_{CC}.
$\overline{RESET}$	Reset input	Input	The microcomputer is reset when "L" level is input to this pin.
X_{IN}	Clock input	Input	Pins X_{IN} and X_{OUT} are the I/O pins of the clock generating circuit, respectively. Connect these pins via a ceramic resonator or a quartz-crystal oscillator. When an external clock is used, the clock should be input to pin X_{IN}, and pin X_{OUT} should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	This pin outputs signal $\overline{E}$. When $\overline{E}$'s level is "L," the microcomputer reads data and instruction codes or writes data. Also, output of signal $\overline{E}$ can be stopped by software.
BYTE	External data bus width selection input	Input	**[Single-chip Mode]** Connect to pin V_{SS}. **[Memory Expansion Mode] [Microprocessor Mode]** Input level to this pin determines whether the external data bus has a 16-bit width or an 8-bit width. A 16-bit width is selected when the level is "L," and an 8-bit width is selected when the level is "H."
AV_{CC}	Analog power source input		Power source input for the A-D converter. Connect to pin V_{CC}.
AV_{SS}			Power source input for the A-D converter. Connect to pin V_{SS}.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.

Note: In the low voltage version, it is 2.7 V to 5.5 V.

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OVERVIEW

1.3 Pin description

Table 1.3.2 Pin description (2)

Pin	Name	Input/Output	Functions
P00–P07	I/O port P0	I/O	**[Single-chip Mode]** P0 is an 8-bit CMOS I/O port and has an I/O direction register. Each pin can be programmed for input or output.
$\overline{A_0}$–$\overline{A_7}$		Output	**[Memory Expansion Mode] [Microprocessor Mode]** Address's low-order 8 bits ($\overline{A_0}$–$\overline{A_7}$) are output.
P10–P17	I/O port P1	I/O	**[Single-chip Mode]** P1 is an 8-bit I/O port with the same function as port P0.
$\overline{A_8}$/D8– $\overline{A_{15}}$/D15			**[Memory Expansion Mode] [Microprocessor Mode]** ● When the external data bus width = 8 bits (Pin BYTE is at "H" level) Address's middle-order 8 bits ($\overline{A_8}$–$\overline{A_{15}}$) are output. ● When the external data bus width = 16 bits (Pin BYTE is at "L" level) Input/Output of data (D8–D15) and output of address's middle-order 8 bits ($\overline{A_8}$–$\overline{A_{15}}$) are performed with the time sharing method.
P20–P27	I/O port P2	I/O	**[Single-chip Mode]** P2 is an 8-bit I/O port with the same function as port P0.
$\overline{A_{16}}$/D0– $\overline{A_{23}}$/D7			**[Memory Expansion Mode] [Microprocessor Mode]** Input/Output of data (D0–D7) and output of address's high-order 8 bits ($\overline{A_{16}}$–$\overline{A_{23}}$) are performed with the time sharing method.
P30–P33	I/O port P3	I/O	**[Single-chip Mode]** P3 is a 4-bit I/O port with the same function as port P0.
R/$\overline{W}$, $\overline{BHE}$, ALE, $\overline{HLDA}$		Output	**[Memory Expansion Mode] [Microprocessor Mode]** These pins respectively output signals R/$\overline{W}$, $\overline{BHE}$, ALE, and $\overline{HLDA}$. ● Signal R/$\overline{W}$ This signal indicates the data bus state. When this signal level is "H," a data bus is in the read state. When this signal level is "L," a data bus is in the write state. ● Signal $\overline{BHE}$ This signal's level is "L" when the microcomputer accesses an odd address. ● Signal ALE This signal is used to separate the multiplexed signal which consists of an address and data to the address and the data. ● Signal $\overline{HLDA}$ This signal informs the external whether this microcomputer enters the Hold state or not. In Hold state, pin $\overline{HLDA}$ outputs "L" level.

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Table 1.3.3 Pin description (3)

Pin	Name	Input/Output	Functions
P40–P47	I/O port P4	I/O	**[Single-chip Mode]** P4 is an 8-bit I/O port with the same function as port P0. P42 can also be programmed as the clock ϕ1 output pin. (Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)
$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, P42–P47		Input Input I/O	**[Memory Expansion Mode]** P40 functions as pin $\overline{\text{HOLD}}$, and P41 as pin $\overline{\text{RDY}}$. The microcomputer is in Hold state while pin $\overline{\text{HOLD}}$'s input level is "L" and is in Ready state while pin $\overline{\text{RDY}}$'s input level is "L." P42–P47 function as I/O ports with the same function as port P0. P42 can also be programmed as the clock ϕ1 output pin. (Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)
$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, ϕ1, P43–P47		Input Input Output I/O	**[Microprocessor Mode]** P40 functions as pin $\overline{\text{HOLD}}$, P41 as pin $\overline{\text{RDY}}$, and P42 as the clock ϕ1 output pin. (Refer to **"[Memory Expansion Mode]."**) P43–P47 function as I/O ports with the same function as port P0.
P50–P57	I/O port P5	I/O	P5 is an 8-bit I/O port with the same function as port P0 and can be programmed as I/O pins for timers A0–A3 and input pins ($\overline{\text{KI}}_0$–$\overline{\text{KI}}_3$) for the key input interrupt.
P60–P67	I/O port P6	I/O	P6 is an 8-bit I/O port with the same function as port P0 and can be programmed as I/O pins for timer A4, external interrupt input pins, and input pins for timers B0–B2. P67 also functions as an output pin for the sub clock (ϕSUB).
P70–P77	I/O port P7	I/O	P7 is an 8-bit I/O port with the same function as port P0 and can be programmed as analog input pins for the A-D converter. P76 and P77 can be programmed as I/O pins (XCOUT, XCIN) for the sub-clock (32 kHz) oscillation circuit. When using P76 and P77 as pins XCOUT and XCIN, connect a quartz-crystal oscillator between them. When inputting an external clock, input the clock from pin XCIN. P72–P75 also function as UART2's I/O pins.
P80–P87	I/O port P8	I/O	P8 is an 8-bit I/O port with the same function as port P0 and can be programmed as serial I/O's I/O pins.

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OVERVIEW

1.3 Pin description

1.3.1 Examples of handling unused pins

The following are examples of handling unused pins.
These are, however, just examples. In actual use, make the necessary adaptations and properly evaluate performance according to the user's application.

(1) In single-chip mode

Table 1.3.4 Examples of handling unused pins in single-chip mode

Pins	Handling example
P0–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Note 1**).
$\overline{E}$	Leave this pin open.
XOUT (**Note 2**)	
AVcc	Connect this pin to pin Vcc.
AVss, VREF, BYTE	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.
For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).
2: This is applied when an external clock is input to pin XIN.

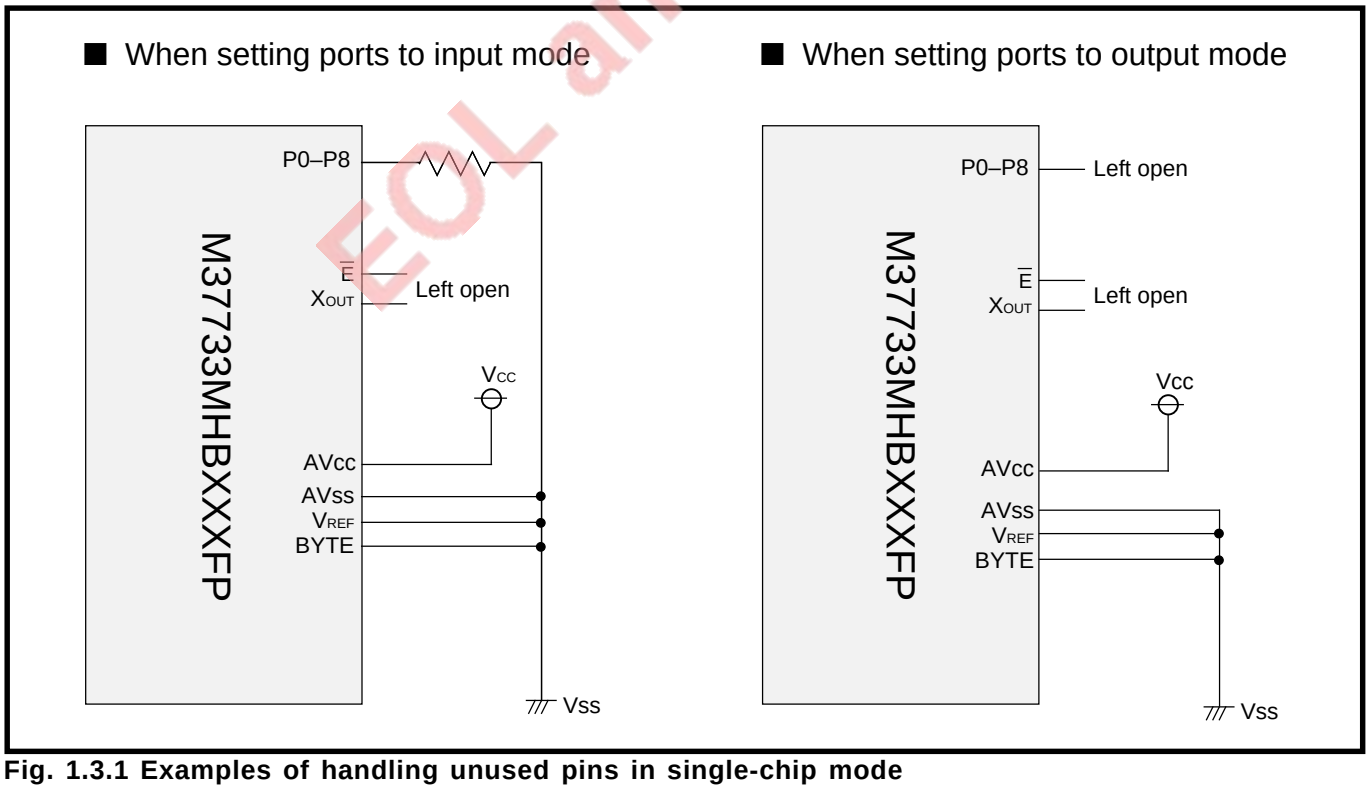

Fig. 1.3.1 Examples of handling unused pins in single-chip mode

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(2) In memory expansion mode

Table 1.3.5 Examples of handling unused pins in memory expansion mode

Pins	Handling example
P42–P47, P5–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Notes 1, 2, and 7**).
$\overline{\text{BHE}}$ (**Note 3**)	Leave this pin open. (**Note 5**)
ALE (**Note 4**)	
$\overline{\text{HLDA}}$	
XOUT (**Note 6**)	Leave this pin open.
$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: this pin functions as an input port from reset until the processor mode is switched to the memory expansion mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

6: This is applied when an external clock is input to pin XIN.

7: Set pin P42/ϕ1 as pin P42. (Clock ϕ1 output is disabled.) And then, for this pin, do the same handling as that for pins P43 to P47 and P5 to P8.

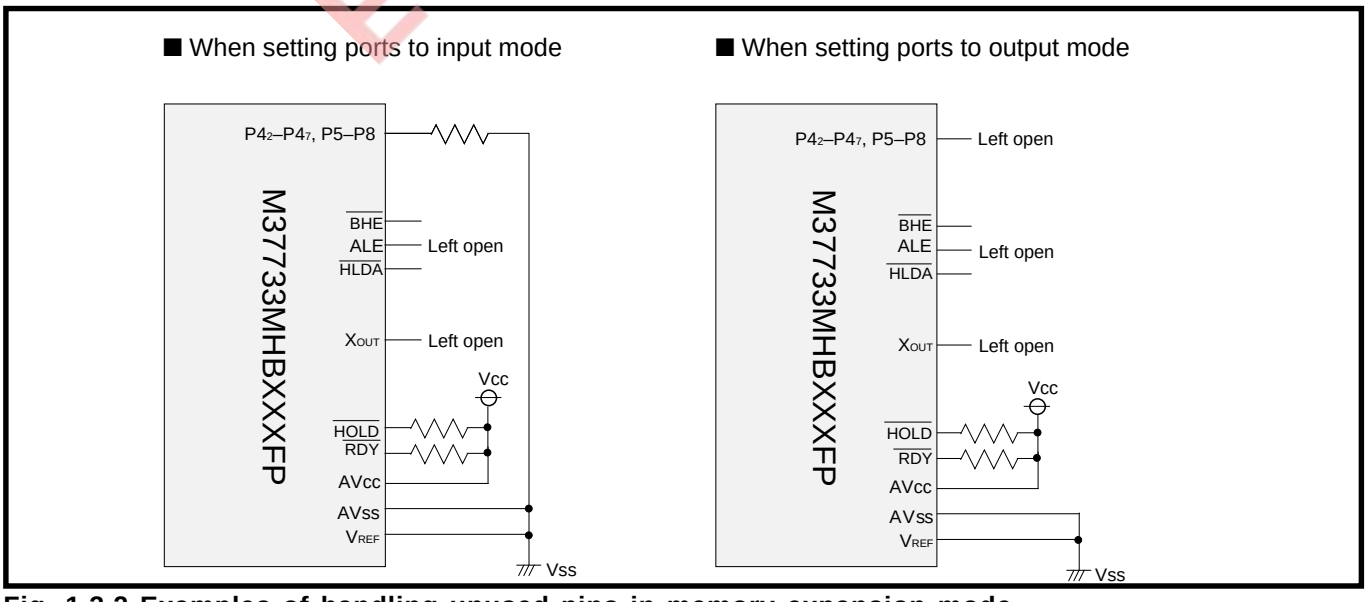

Fig. 1.3.2 Examples of handling unused pins in memory expansion mode

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(3) In microprocessor mode

Table 1.3.6 Examples of handling unused pins in microprocessor mode

Pins	Handling example
P43–P47, P5–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Notes 1 and 2**).
$\overline{BHE}$ (**Note 3**)	Leave this pin open. (**Note 5**)
ALE (**Note 4**)	
$\overline{HLDA}$, ϕ1	
XOUT (**Note 6**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: this pin functions as an input port from reset until the processor mode is switched to the microprocessor mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

6: This is applied when an external clock is input to pin XIN.

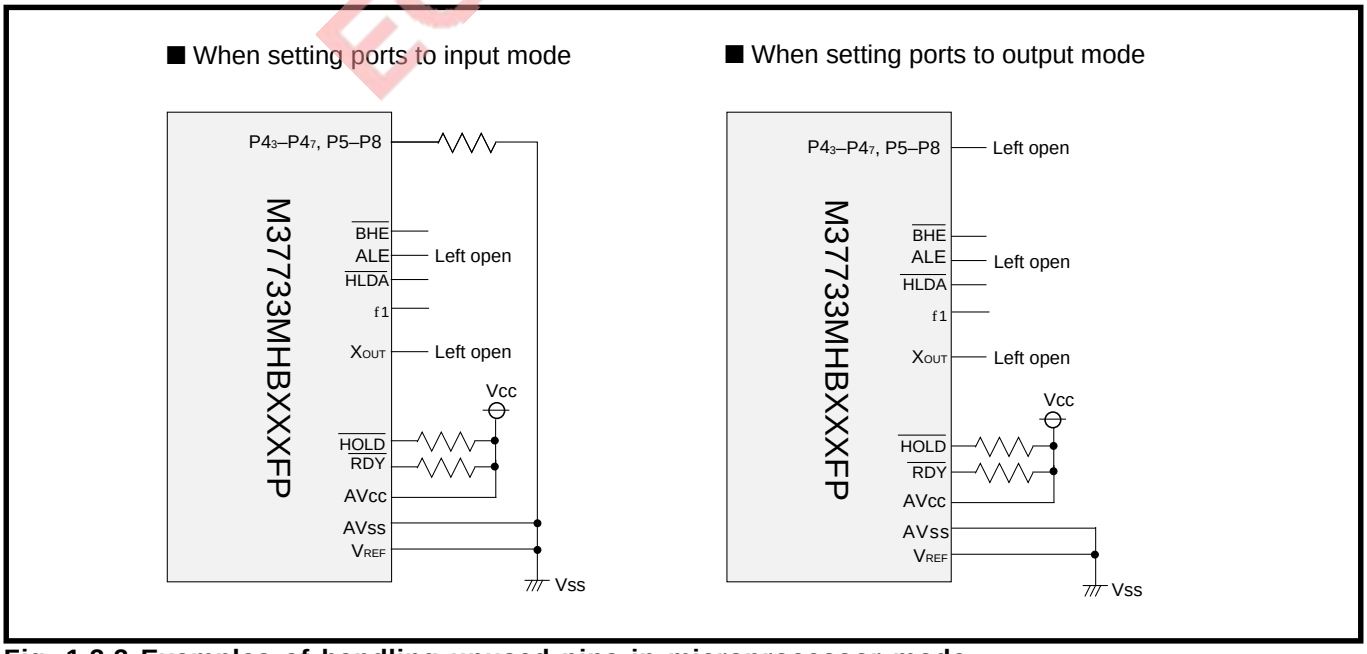

Fig. 1.3.3 Examples of handling unused pins in microprocessor mode

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1.4 Block diagram

Figure 1.4.1 shows the M37733MHBXXXFP block diagram.

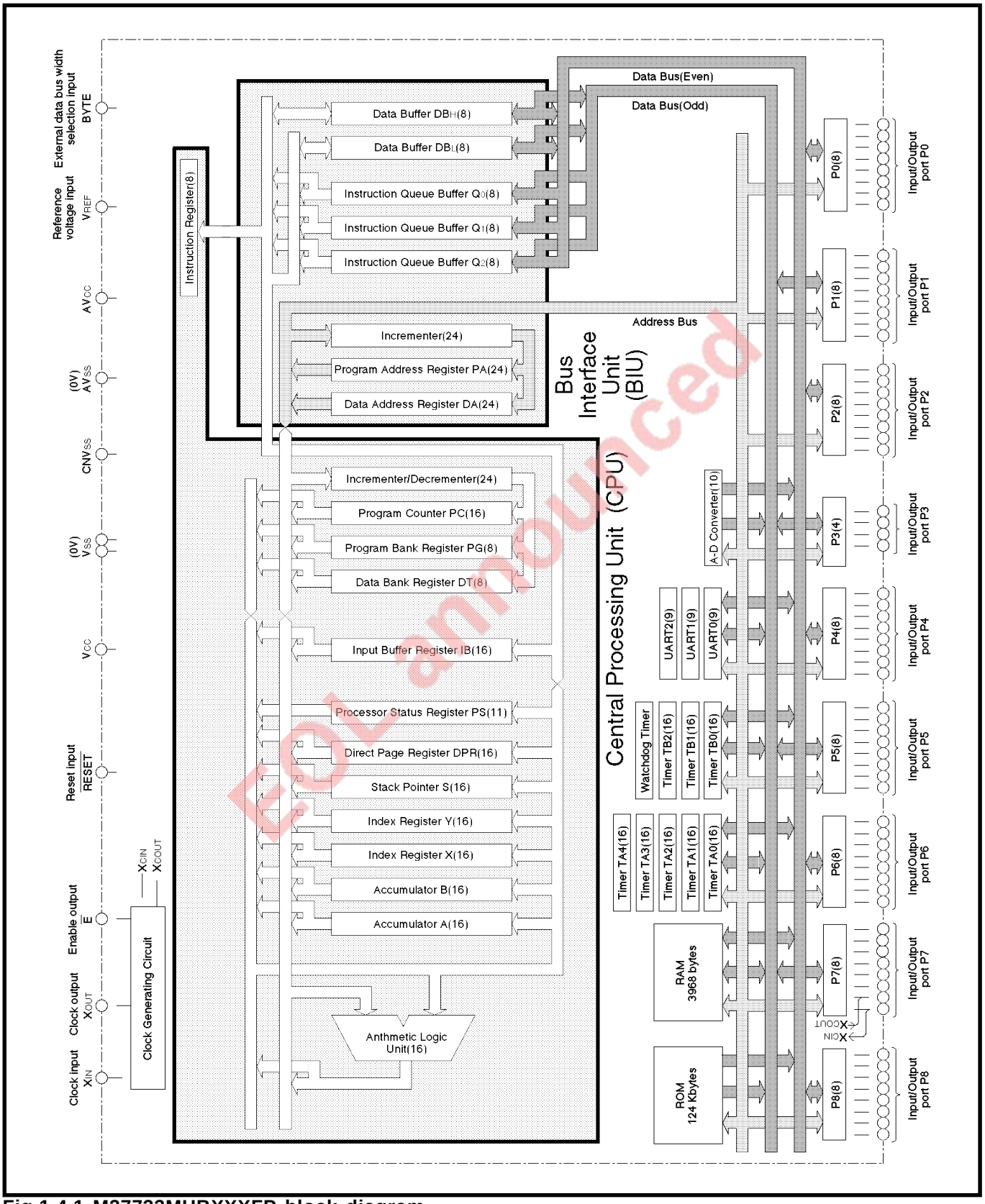

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Fig.1.4.1 M37733MHBXXXFP block diagram

MEMO

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CHAPTER 2

CENTRAL PROCESSING UNIT (CPU)

EOL announced

2.1 Central processing unit
2.2 Bus interface unit
2.3 Accessible area
2.4 Memory allocation
2.5 Processor modes

CENTRAL PROCESSING UNIT (CPU)

2.1 Central processing unit

The CPU of the 7733 Group has ten registers as shown in Figure 2.1.1. Each of these registers is described below.

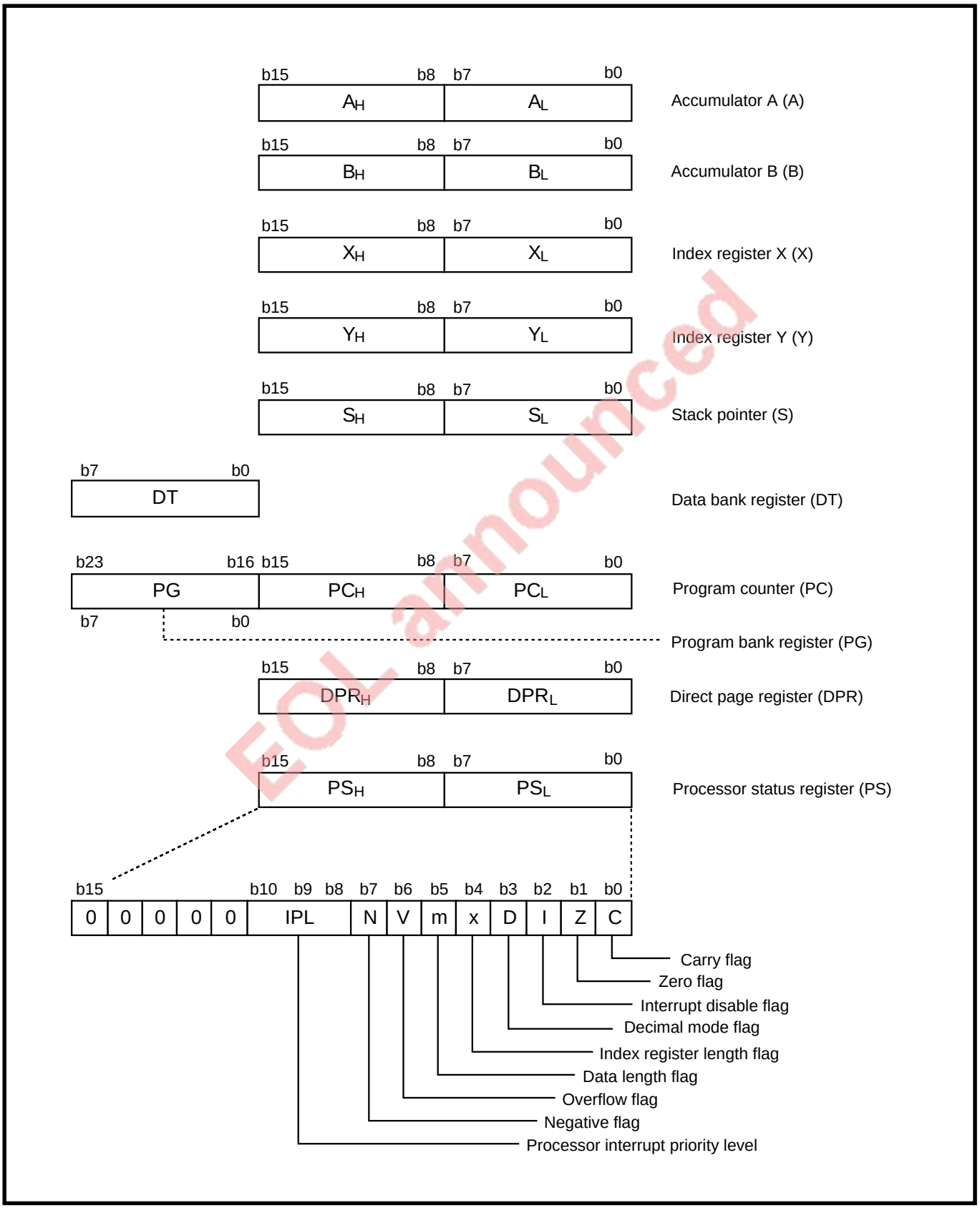

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Fig. 2.1.1 CPU registers structure

2.1.1 Accumulator (Acc)

Accumulators A and B are available.

(1) Accumulator A (A)

Data processing such as calculation, data transfer, or data input/output is executed mainly through accumulator A. It consists of 16 bits and its low-order 8 bits can also be used separately. The data length flag (m), which is a part of the processor status register, specifies whether accumulator A is used as a 16-bit register or an 8-bit register. When the data length is 8 bits wide, only the low-order 8 bits of accumulator A are used and the contents of the high-order 8 bits is unchanged.

(2) Accumulator B (B)

Accumulator B has the same function as accumulator A and can be used instead of accumulator A. Note that, except for some instructions, the use of accumulator B requires more instruction bytes and execution cycles than that of accumulator A. Accumulator B consists of 16 bits and is also affected by the data length flag (m) just as for accumulator A.

2.1.2 Index register X (X)

Index register X consists of 16 bits and its low-order 8 bits can also be used separately. The index register length flag (x), which is a part of the processor status register, specifies whether index register X is used as a 16-bit register or an 8-bit register. When the index register length is 8 bits wide, only the low-order 8 bits of index register X are used and the contents of the high-order 8 bits is unchanged.
In an addressing mode where index register X is used as an index register, the address obtained by adding the contents of index register X to the operand is accessed. In execution of a block transfer instruction **(MVP** or **MVN)**, the contents of index register X is the low-order 16 bits of the source address and the third byte of the instruction is the high-order 8 bits of the address.

✵ Refer to **"7700 Family Software Manual"** for addressing modes.

2.1.3 Index register Y (Y)

Index register Y has the same function as index register X. Index register Y consists of 16 bits and is also affected by the index register length flag (x) just as for index register X.
In execution of a block transfer instruction **(MVP** or **MVN)**, the contents of index register Y is the low-order 16 bits of the destination address and the second byte of the instruction is the high-order 8 bits of the address.

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CENTRAL PROCESSING UNIT (CPU)

2.1 Central processing unit

2.1.4 Stack pointer (S)

The stack pointer (S) consists of 16 bits and is used for an interrupt, a subroutine call, or execution of an addressing mode where a stack is used. The contents of S indicates a store address for a register and so on during an interrupt or a subroutine call (stack area). The stack area is set in bank 0_{16}. (Refer to section **"2.1.6 Program bank register (PG)."**)

When an interrupt request is accepted, the microcomputer stores the contents of the program bank register (PG) into an address indicated by the contents of S and decrements the contents of S by 1. Then the microcomputer stores the contents of the program counter (PC) and the processor status register (PS). After acceptance of an interrupt request, the contents of S becomes [S] – 5. ([S] is the initial address that the stack pointer (S) indicates when an interrupt request is accepted.) (Refer to **Figure 2.1.2.**)

After processing in an interrupt routine is finished, processing for return to the original routine is performed as follows.

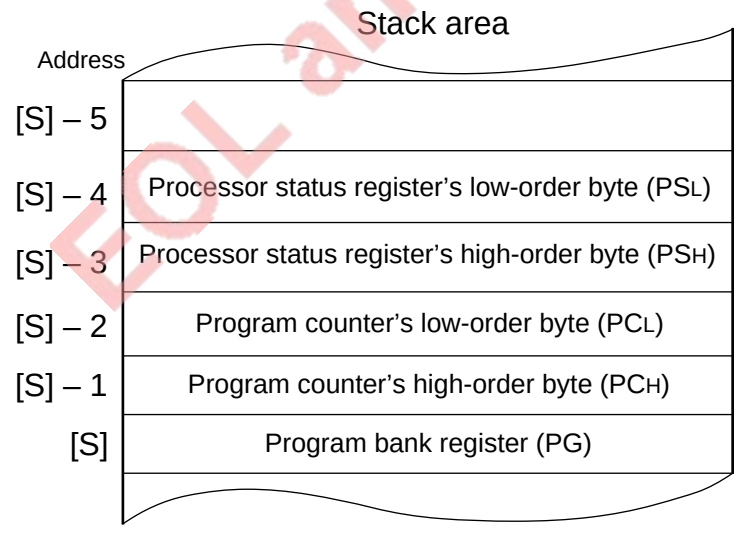
When the **RTI** instruction is executed, the contents of registers which were stored in the stack area are restored into the original registers. (The contents are restored PS, PC, and PG in that order.) The contents of S is also returned to the state before acceptance of an interrupt request.

During a subroutine call, the same processing as for an interrupt is performed. The contents of PS, however, are not automatically stored. (The contents of PG may not be stored. This depends on the addressing mode.)

During an interrupt or a subroutine call, registers other than the above registers are not automatically stored. Therefore, be sure to store necessary registers by software.

The contents of S is undefined at reset. Therefore, be sure to initialize S at the start of a program. Furthermore, a stack area changes according to subroutine's nesting or acceptance of multiple interrupts' requests. Therefore, give careful consideration to subroutine's nesting depth not to destroy the necessary data.

❋ Refer to **"7700 Family Software Manual"** for addressing modes.



❋ [S] is the initial address that the stack pointer (S) indicates when an interrupt request is accepted.
S's contents is "[S] – 5" after all of the above registers are pushed.

Fig. 2.1.2 Stored registers in stack area

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2.1.5 Program counter (PC)

The program counter consists of 16 bits. This counter indicates the low-order 16 bits of a store address, which consists of 24 bits, of an instruction to be executed next, in other words an instruction which is read from an instruction queue buffer.

At reset, value "FF_{16}" is set to the high-order byte (PC_H) of the program counter and value "FE_{16}" is set to the low-order byte (PC_L) of the counter. And then, immediately after reset, the contents of the reset's vector addresses (addresses $FFFE_{16}$, $FFFF_{16}$) are set to the counter.

Figure 2.1.3 shows the program counter and the program bank register.

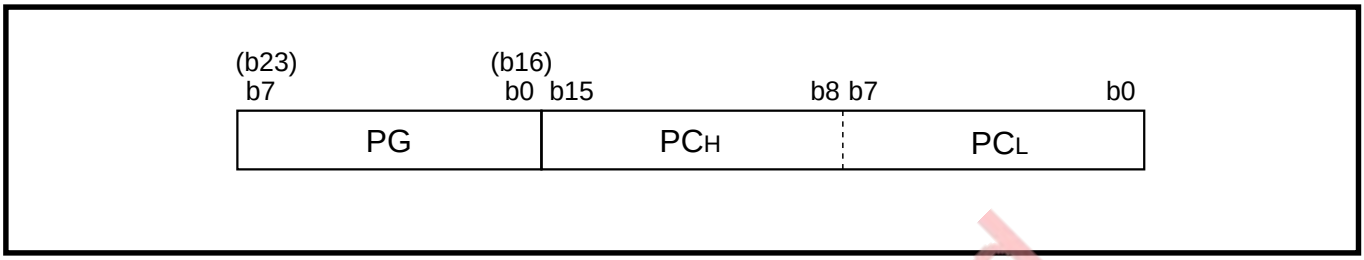

Fig. 2.1.3 Program counter and program bank register

2.1.6 Program bank register (PG)

The program bank register consists of 8 bits. (Refer to **Figure 2.1.3.**) This register indicates the high-order 8 bits of a store address, which consists of 24 bits, of an instruction to be executed next, in other words an instruction which is read from an instruction queue buffer. These 8 bits indicate "bank." The contents of the program bank register is automatically incremented by 1 when a carry occurs in the following cases:

•When a certain value is added to the contents of the program counter

•When the displacement is added to the program counter by executing a branch instruction and others

The contents of the program bank register is automatically decremented by 1 when a borrow occurs in the following case:

•When a certain value is subtracted from the contents of the program counter

Therefore, when normally programming, it is not necessary to give consideration to bank boundaries.

At reset, this register is cleared to "00_{16}."

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CENTRAL PROCESSING UNIT (CPU)

2.1 Central processing unit

2.1.7 Data bank register (DT)

The data bank register consists of 8 bits. In an addressing mode where the data bank register is used, the contents of this register is processed as the high-order 8 bits (bank) of an address to be accessed, which consists of 24 bits.
When setting a certain value to this register, execute the **LDT** instruction.
At reset, this register is cleared to "00_{16}."

✵ Addressing modes where the data bank register is used are listed below:

- Direct • indirect
- Direct • indexed X • indirect
- Direct • indirect • indexed Y
- Absolute
- Absolute • bit
- Absolute • indexed X
- Absolute • indexed Y
- Absolute • bit • relative
- Stack pointer • relative • indirect • indexed Y

2.1.8 Direct page register (DPR)

The direct page register consists of 16 bits. The contents of this register specifies a direct page area to bank 0_{16} or an area which extends banks 0_{16} and 1_{16}. The direct page area can be accessed with two bytes (**Note**) by using the direct page addressing mode.
The contents of the direct page register indicates the base address (the lowest address) of a direct page area which is extended to 256 bytes above this address.
Values from 0000_{16} to $FFFF_{16}$ can be set to the direct page register. When a certain value equal to or more than "$FF01_{16}$" is set to the direct page register, the direct page area is specified to an area which extends banks 0_{16} and 1_{16}. When the contents of low-order 8 bits of the direct page register is cleared to "00_{16}," the number of cycles required to generate the address to be accessed is decremented by 1. Therefore, efficient access is possible.
At reset, this register is cleared to "0000_{16}."
Figure 2.1.4 shows a setting example of direct page areas.

Note: For the **DIV** and **MPY** instructions, the direct page area is accessed with 3 bytes.
When accumulator B is used, for each instruction, the number of instruction bytes is incremented by 1.

✵ Addressing modes where the direct page register is used are listed below:

- Direct
- Direct • bit
- Direct • indexed X
- Direct • indexed Y
- Direct • indirect
- Direct • indexed X • indirect
- Direct • indirect • indexed Y
- Direct • indirect long
- Direct • indirect long • indexed Y
- Direct • bit • relative

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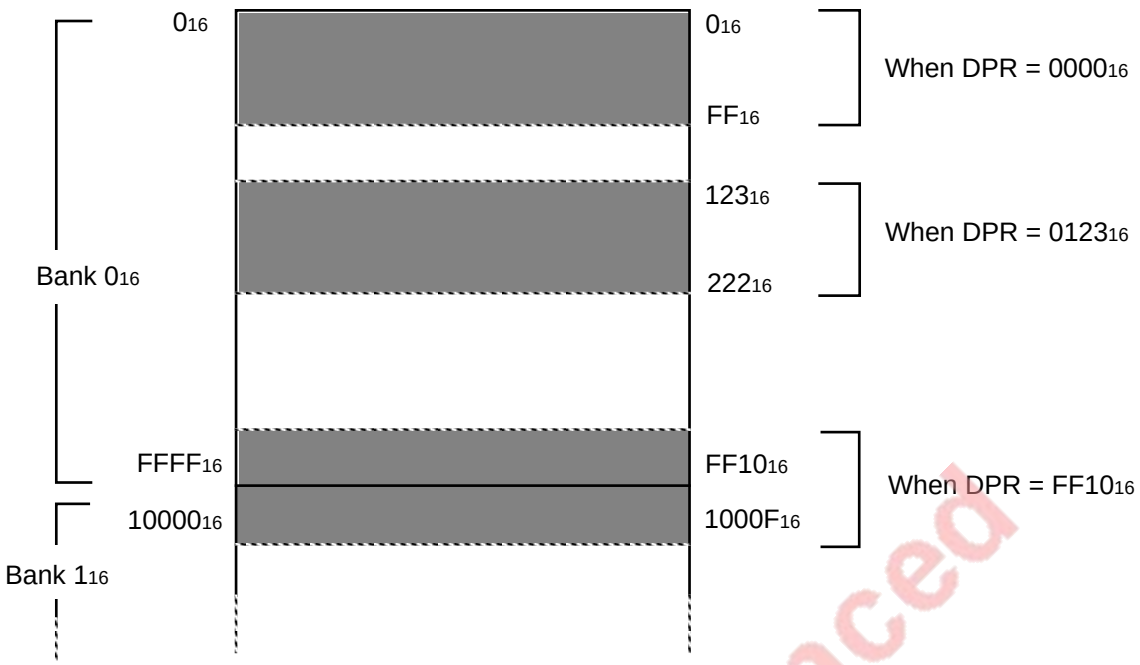

Notes 1: When the low-order 8 bits of DPR = "00$_{16}$," the number of cycles required to generate the address to be accessed is decremented by 1.
2: When DPR = "FF01$_{16}$" or more, the direct page area is specified to the area which extends banks 0$_{16}$ and 1$_{16}$.

Fig. 2.1.4 Setting example of direct page area

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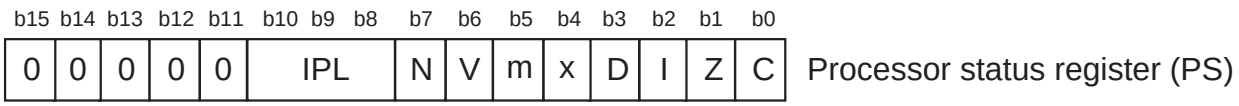
CENTRAL PROCESSING UNIT (CPU)

2.1 Central processing unit

2.1.9 Processor status register (PS)

The processor status register consists of 11 bits.
Figure 2.1.5 shows the structure of the processor status register.



Note: "0" is always read from bits 11 to 15.

Fig. 2.1.5 Structure of processor status register

(1) Bit 0: Carry flag (C)

This flag retains a carry or borrow which occur in the Arithmetic Logic unit (ALU) during an arithmetic or logic operation. This flag is also affected by a shift or rotate instruction. When the **BCC** or **BCS** instruction is executed, the program branches according to this flag's state. When setting this flag to "1," execute the **SEC** or **SEP** instruction; when clearing this flag to "0," execute the **CLC** or **CLP** instruction.

(2) Bit 1: Zero flag (Z)

This flag is set to "1" when the result of an arithmetic operation or data transfer is "0" and cleared to "0" when otherwise. When the **BNE** or **BEQ** instruction is executed, the program branches according to this flag's state. This flag is ignored for an addition and subtraction instructions (the **ADC** and the **SBC** instructions) in the decimal mode. When setting this flag to "1," execute the **SEP** instruction; when clearing this flag to "0," execute the **CLP** instruction.

(3) Bit 2: Interrupt disable flag (I)

This flag disables all maskable interrupts, in other words interrupts other than watchdog timer, the **BRK** instruction, and zero division interrupts. Interrupts are disabled when this flag is "1." When an interrupt request is accepted, this flag is automatically set to "1" and disables multiple interrupts. When setting this flag to "1," execute the **SEI** or **SEP** instruction; when clearing this flag to "0," execute the **CLI** or **CLP** instruction.
At reset, this flag is set to "1."

(4) Bit 3: Decimal mode flag (D)

This flag determines whether addition and subtraction are performed in binary or decimal.
Binary arithmetic is performed when this flag is "0."
When it is "1," decimal arithmetic is performed. At this time, each word is processed as 2- or 4-digit decimal data. (The digit's number is determined by the data length flag (m)).
Decimal adjust is automatically performed. (Note that a decimal operation is enabled only in execution of the **ADC** or **SBC** instruction.)
When setting this flag to "1," execute the **SEP** instruction; when clearing this flag to "0," execute the **CLP** instruction.
At reset, this flag is cleared to "0."

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(5) Bit 4: Index register length flag (x)

This flag determines whether index register X or index register Y is used as a 16-bit register or an 8-bit register. The register is used as a 16-bit register when this flag is "0" and as an 8-bit register when this flag is "1." When setting this flag to "1," execute the **SEP** instruction; when clearing this flag to "0," execute the **CLP** instruction.
At reset, this flag is cleared to "0."

Note: When data is transferred between registers which are different in bit length, the data is transferred with the bit length of the destination register. But this is not applied to the case where the **TXA**, **TYA**, **TXB**, or **TYB** instruction is executed. Refer to **"7700 Family Software Manual"** for details.

(6) Bit 5: Data length flag (m)

This flag determines whether data is used as 16-bit data or 8-bit data. Data is used as 16-bit data when this flag is "0" and as 8-bit data when this flag is "1." When setting this flag to "1," execute the **SEM** or **SEP** instruction; when clearing this flag to "0," execute the **CLM** or **CLP** instruction.
At reset, this flag is cleared to "0."

Note: When data is transferred between registers which are different in bit length, the data is transferred with the data length of the destination register. But this is not applied to the case where the **TXA**, **TYA**, **TXB**, or **TYB** instruction is executed. Refer to **"7700 Family Software Manual"** for details.

(7) Bit 6: Overflow flag (V)

This flag is valid when addition or subtraction is executed for each word which is processed as signed binary data. If the data length flag (m) is "0," the overflow flag is set to "1" when the result of addition or subtraction exceeds the range between –32768 and +32767 and cleared to "0" in the other cases. If the data length flag (m) is "1," the overflow flag is set to "1" when the result of addition or subtraction exceeds the range between –128 and +127 and cleared to "0" in the other cases. Also, the overflow flag is set to "1" when the length of the division result obtained by the **DIV** instruction is longer than that of a register where the result is to be stored. When the **BVC** or **BVS** instruction is executed, the program branches according to this flag's state. This flag is ignored in the decimal mode. When setting this flag to "1," execute the **SEP** instruction; when clearing this flag to "0," execute the **CLV** or **CLP** instruction.

(8) Bit 7: Negative flag (N)

This flag is set to "1" when the result of an arithmetic operation or data transfer is negative. (Bit 15 of the result is "1" when the data length flag (m) is "0," or bit 7 of the result is "1" when the data length flag (m) is "1.") It is cleared to "0" in the other cases. When the **BPL** or **BMI** instruction is executed, the program branches according to this flag's state. This flag is ignored in the decimal mode. When setting this flag to "1," execute the **SEP** instruction; when clearing this flag to "0," execute the **CLP** instruction.

(9) Bits 8 to 10: Processor interrupt priority level (IPL)

These bits can specify one of levels 0 to 7 as the processor interrupt priority level. An interrupt is enabled when its interrupt priority level, which is set in the interrupt control register, is higher than IPL. When the interrupt request is accepted, the contents of IPL is stored into the stack area and the interrupt priority level of the accepted interrupt is set in IPL.
No instruction can directly set or clear each of these bits. When changing these bits, store a desired processor interrupt priority level into the stack area. And then, change the contents of the processor status register by executing the **PUL** or **PLP** instruction.
At reset, the contents of IPL is cleared to "000_2."

EOL announced

2.2 Bus interface unit

The microcomputer has a bus interface unit (BIU) between the central processing unit (CPU) and memory • I/O unit. The BIU's function and operation are described below. When connecting external devices, refer to chapter **"12. CONNECTING EXTERNAL DEVICES,"** also.

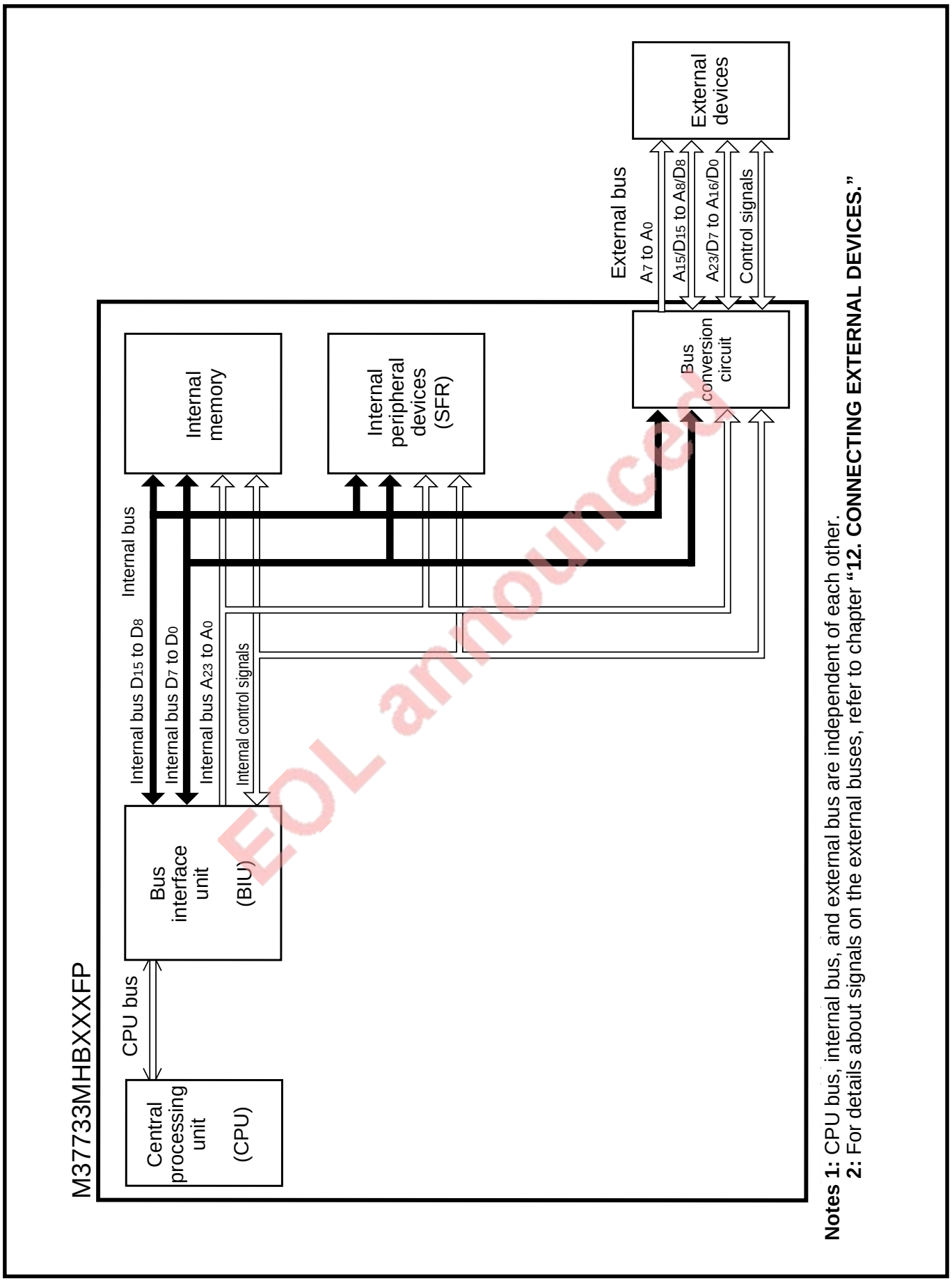
2.2.1 Overview

Transfer operation between the CPU and memory • I/O unit is always performed via the BIU.

① The BIU reads an instruction from the memory before the CPU executes it.
② When the CPU reads data from the memory • /O unit, the CPU informs the BIU of the address where the data resides. The BIU reads the data from the address and pass it to the CPU.
③ When the CPU writes data to the memory • I/O unit, the CPU informs the BIU of the address where the data resides. The BIU writes the data to the address.
④ In order to realize operations ① to ③, the BIU inputs and outputs bus control signals and controls the buses.

Figure 2.2.1 shows the buses and bus interface unit (BIU).

EOL announced



EOL announced

Fig. 2.2.1 Buses and bus interface unit (BIU)

CENTRAL PROCESSING UNIT (CPU)

2.2 Bus interface unit

2.2.2 Functions of bus interface unit (BIU)

The bus interface unit (BIU) consists of four registers shown in Figure 2.2.2. Table 2.2.1 lists each register's function.

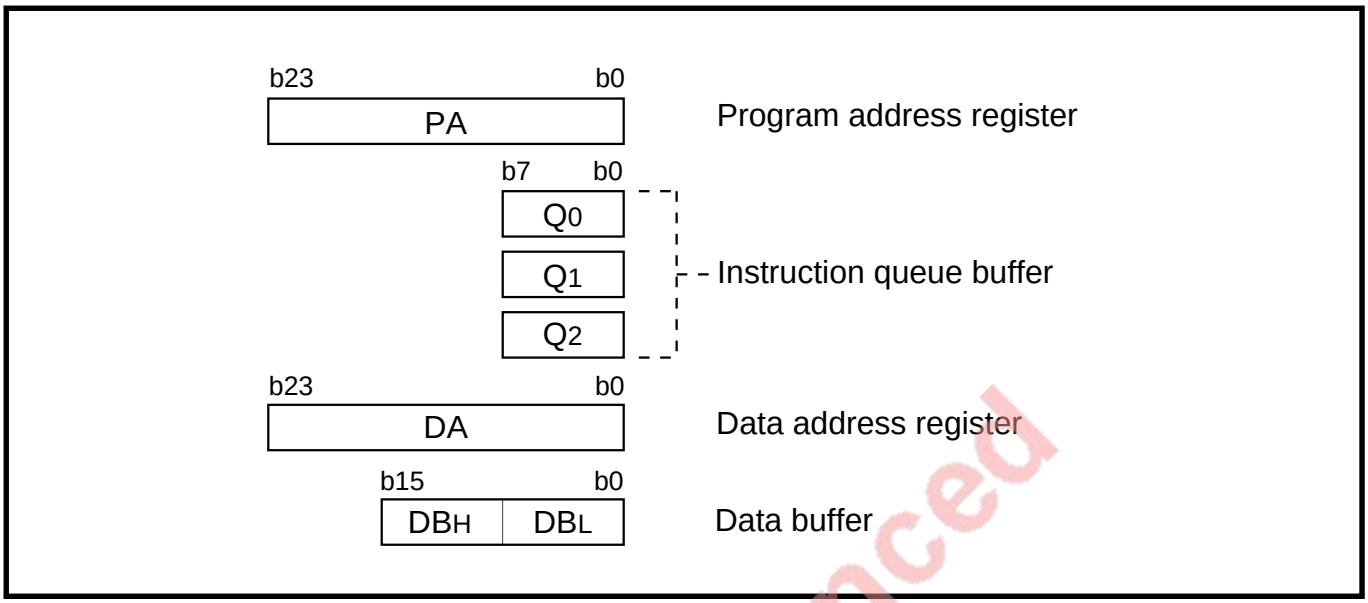


Fig. 2.2.2 Registers' structure of which bus interface unit (BIU) consists

Table 2.2.1 Each register's function

Name	Functions
Program address register	Indicates a store address for an instruction which is next fetched into an instruction queue buffer.
Instruction queue buffer	Temporarily stores an instruction which was fetched.
Data address register	Indicates an address for data which is next read or written.
Data buffer	Temporarily stores data which was read from the memory • I/O unit by the BIU or which is to be written to the memory • I/O unit by the CPU.

EOL announced

The CPU and buses operate on the basis of different signals (**Note**). Between the CPU and buses, therefore, data is passed or received via the BIU. Owing to the BIU's operation, the CPU can operate at high speed without waiting for the access by the low-speed memory • I/O unit.
When an external device is connected, it is necessary to secure an access time according to the external device's timing specifications. In this case, in order to secure an access time, the BIU extends the duration of signals required for the access.

Note: The CPU operates on the basis of ϕCPU. The period of ϕCPU is normally the same as that of ϕ.
The internal buses operate on the basis of $\overline{E}$. The period of $\overline{E}$ is at least twice that of ϕ.

The BIU's functions are described below.

(1) Reading out instruction (Instruction prefetch)

When the CPU does not request to read or write data, that is, when buses are not in use, the BIU reads instructions from the memory and stores them in an instruction queue buffer. This is called "instruction prefetch."
The CPU reads instructions from the instruction queue buffer and executes them. Therefore, the CPU can operate at high speed without waiting for the access by the low-speed memory.
When the instruction queue buffer becomes empty or stores only 1 byte of an instruction, the BIU prefetches a new instruction code. The instruction queue buffer can store instructions up to 3 bytes. The contents of the instruction queue buffer is initialized when a branch or jump instruction is executed and the BIU reads a new instruction code from the destination address.
If instructions in the instruction queue buffer are insufficient for the CPU's request, the BIU extends the "L"-level duration of clock ϕCPU in order to keep the CPU waiting until the BIU fetches the requested number of instructions or more.

(2) Writing data to memory • I/O

The CPU informs the BIU's data address register of an address to which data is written and writes the data to the data buffer. The BIU outputs the address received from the CPU to the address bus and writes the data in the data buffer to the specified address.
While the BIU is writing data to the specified address, the CPU advances to the next process without waiting for completion of BIU's write operation.
Note that while the BIU uses buses for instruction prefetch, the BIU keeps the CPU waiting even when the CPU requests to write data.

(3) Signal input/output for access to external device

When accessing external devices, the BIU inputs and outputs signals required for the access. (For details, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**)

EOL announced

CENTRAL PROCESSING UNIT (CPU)

2.2 Bus interface unit

2.2.3 Operation of bus interface unit (BIU)

Figure 2.2.3 shows the basic operating waveforms of the bus interface unit (BIU). When accessing external devices, some signals which are input or output to or from the external are required. For details about these signals, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**

(1) When fetching an instruction into an instruction queue buffer

① When an instruction which is next fetched resides at an even address
The BIU fetches two bytes of the instruction with waveform (a).
Note that when an external device which is connected by an 8-bit external data bus (BYTE = "H") is accessed, only one byte of the instruction is fetched.

② When an instruction which is next fetched resides at an odd address
The BIU fetches only one byte of the instruction with waveform (a). The contents at an even address is not fetched into an instruction queue buffer.

(2) When reading or writing data from or to memory • I/O

① When accessing 16-bit data which starts from an even address, waveform (a) is applied. The 16-bit data is accessed at a time.

② When accessing 16-bit data which starts from an odd address, waveform (b) is applied. The 16-bit data is accessed by the 8 bits. Invalid data is not fetched into a data buffer.

③ When accessing 8-bit data at an even address, waveform (a) is applied. Data at an odd address is not fetched into a data buffer.

④ When accessing 8-bit data at an odd address, waveform (a) is applied. Data at an even address is not fetched into a data buffer.

For instructions which are affected by the data length flag (m) or index register length flag (x), an operation is applied as follows:

- When "m" or "x" = "0," operation ① or ② is applied.
- When "m" or "x" = "1," operation ③ or ④ is applied.

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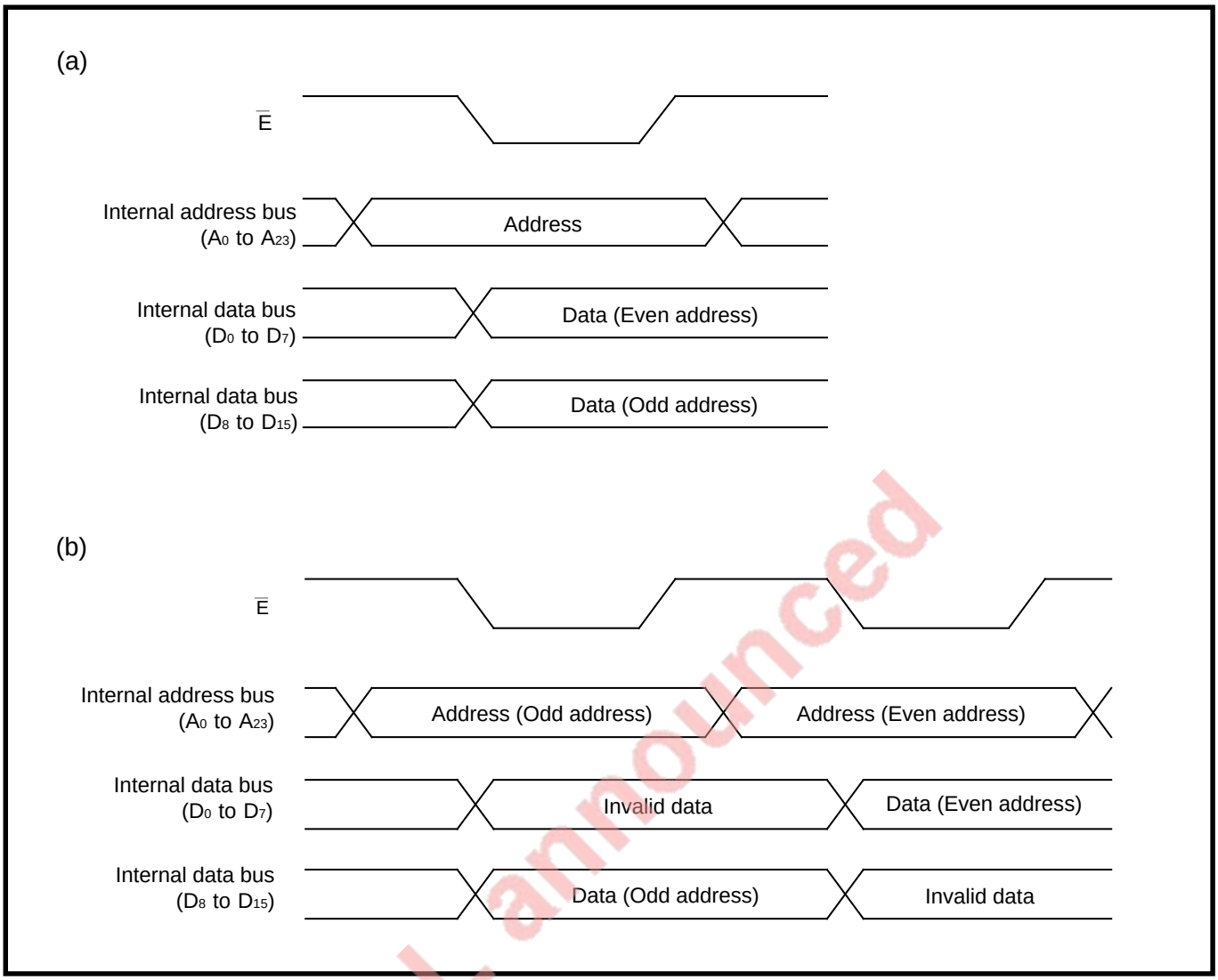
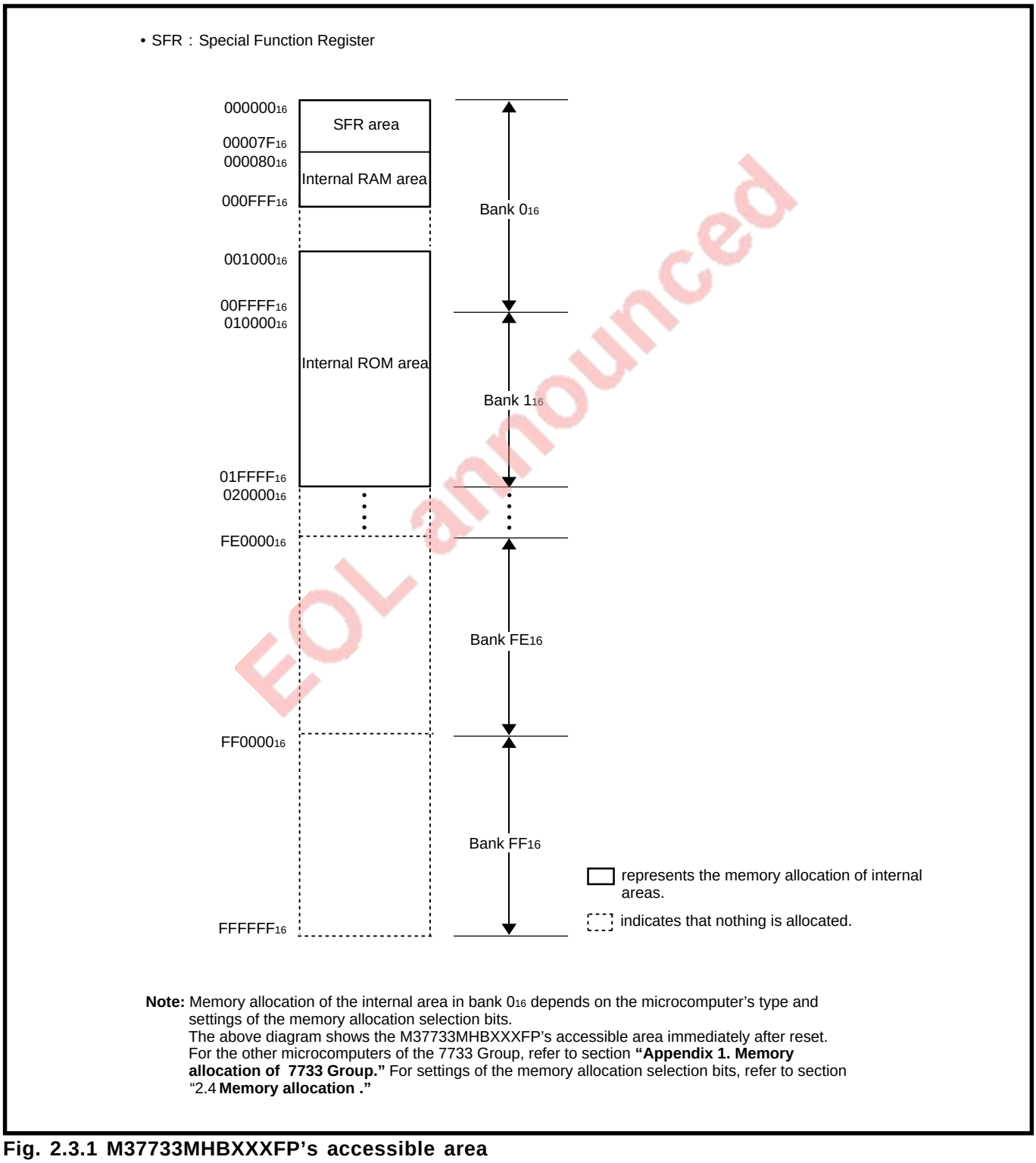


Fig. 2.2.3 Basic operating waveforms of bus interface unit (BIU)

EOL announced

2.3 Accessible area

Figure 2.3.1 shows the M37733MHBXXXFP's accessible area.
Although the program counter (PC) consists of 16 bits, it can access the 16-Mbyte area at addresses 0_{16} to $FFFFFF_{16}$, combined with the program bank register (PG). For details about access to the external, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**
The memories and I/O units are allocated in the same accessible area. Therefore, operations such as data transfer, arithmetic, and others can be performed with the same instructions. (It is not necessary to distinguish the memories and I/O units.)



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Note: Memory allocation of the internal area in bank 0_{16} depends on the microcomputer's type and settings of the memory allocation selection bits.
The above diagram shows the M37733MHBXXXFP's accessible area immediately after reset.
For the other microcomputers of the 7733 Group, refer to section **"Appendix 1. Memory allocation of 7733 Group."** For settings of the memory allocation selection bits, refer to section "2.4 **Memory allocation .**"

Fig. 2.3.1 M37733MHBXXXFP's accessible area

2.3.1 Banks

The accessible area is divided by the 64 Kbytes. This 64-Kbyte area is called “bank.” The high-order 8 bits of an address, which consists of 24 bits, indicate the bank. A bank is specified by the program bank register (PG) or data bank register (DT). Each bank can be accessed efficiently by using an addressing mode where the data bank register (DT) is used.

At each bank’s boundary, when an overflow occurs in the program counter (PC), the contents of the program bank register (PG) is incremented by 1; when a borrow occurs in the program counter (PC), the contents of the program bank register (PG) is decremented by 1. Accordingly, when normally programming, it is not necessary to give consideration to bank boundaries.

2.3.2 Direct page

A 256-byte area specified by the direct page register (DPR) is called “direct page.” When setting a direct page, set the base address (the lowest address) of an area which is to be specified as a direct page to the direct page register (DPR). (Refer to section **“2.1.8 Direct page register (DPR).”**)

By using a direct page addressing mode, a direct page can be accessed with less instruction cycles.

EOL announced

2.4 Memory allocation

The internal area's memory allocation is described below. For the external area, refer to section **"2.5 Processor modes."**

2.4.1 Memory allocation in internal area

SFR (Special Function Register), internal RAM, and internal ROM are allocated in the internal area.

(1) SFR (Special Function Register) area

Registers required for setting internal peripheral devices are allocated to addresses 0_{16} to $7F_{16}$. This area is called "SFR (Special Function Register) area." Figure 2.4.4 shows the SFR area's memory map.

For each register in the SFR area, refer to the corresponding functional description.

For the state of the SFR area immediately after reset, refer to section **"13.1.2 State of CPU, SFR area and internal RAM area."**

(2) Internal RAM area

In the M37733MHBXXXFP, a 3968-byte static RAM is allocated to addresses 80_{16} to FFF_{16} (**Note**). The internal RAM area is used as a data store area and as a stack area. Therefore, it is necessary to give careful consideration to nesting levels in subroutines and multiple interrupts' levels not to destroy necessary data.

(3) Internal ROM area

In the M37733MHBXXXFP, a 124-Kbyte mask ROM is allocated to addresses 1000_{16} to $1FFFF_{16}$ immediately after reset (**Note**). The internal ROM's size and area can be changed by the memory allocation selection bits (bits 0 to 2 at address 63_{16}). Figure 2.4.1 shows the structure of the memory allocation control register and its setting method. Figures 2.4.2 and 2.4.3 show the M37733MHBXXXFP's memory map. (Refer to section "**Appendix 9. Q & A.**") Vector addresses for reset and interrupts (interrupt vector table) are allocated to addresses $FFD6_{16}$ to $FFFF_{16}$ in the internal ROM. In the microprocessor mode, where the internal ROM area is inhibited from use, the ROM must be allocated to addresses $FFD6_{16}$ to $FFFF_{16}$.

Note: For the other microcomputers of the 7733 Group, refer to section **"Appendix 1. Memory allocation of 7733 Group."**

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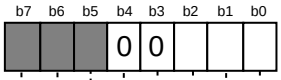

Memory allocation control register (address 63 16) **(Note 3)**

Bit	Bit name	Functions	At reset	RW
0	Memory allocation selection bits **(Notes 1 and 2)**	b2b1b0 ROM size ROM size 0 0 0: 124 Kbytes, 3968 bytes 0 0 1: 120 Kbytes, 3968 bytes 0 1 0: 60 Kbytes, 2048 bytes 0 1 1: Do not select. 1 0 0: 32 Kbytes, 2048 bytes 1 0 1: 16 Kbytes, 2048 bytes 1 1 0: 96 Kbytes, 3968 bytes 1 1 1: Do not select.	0	RW
1			0	RW
2			0	RW
3	Must be fixed to "0." **(Note 1)**		0	RW
4			0	RW
7 to 5	Not implemented.		Un-defined	

Notes 1: The case where value "55 16" is written in ① of the procedure listed below is not included.
2: When changing these bits, this change must be performed in an area which is internal ROM area before and after this change, for example addresses 00C000 16 to 00FFFF16. Also, when changing these bits, be sure to follow the procedure listed below.
3: This figure is applied only to the M37733MHBXXXFP. For the other microcoputers, please refer to the latest datasheets on the English document CD-ROM or our Web site.

Procedure

① By using the **LDM** instruction, write value "55 16" to address 6316.
(By this, writing to the memory allocation selection bits is enabled.)

② By using the **LDM** instruction, write value "00000XXX 2" to address 6316.
(Values of b2, b1, and b0 shown in the above Figure)

Writing is performed by the next instruction.

Note: When changing bits 2 to 0, be sure to follow this procedure.

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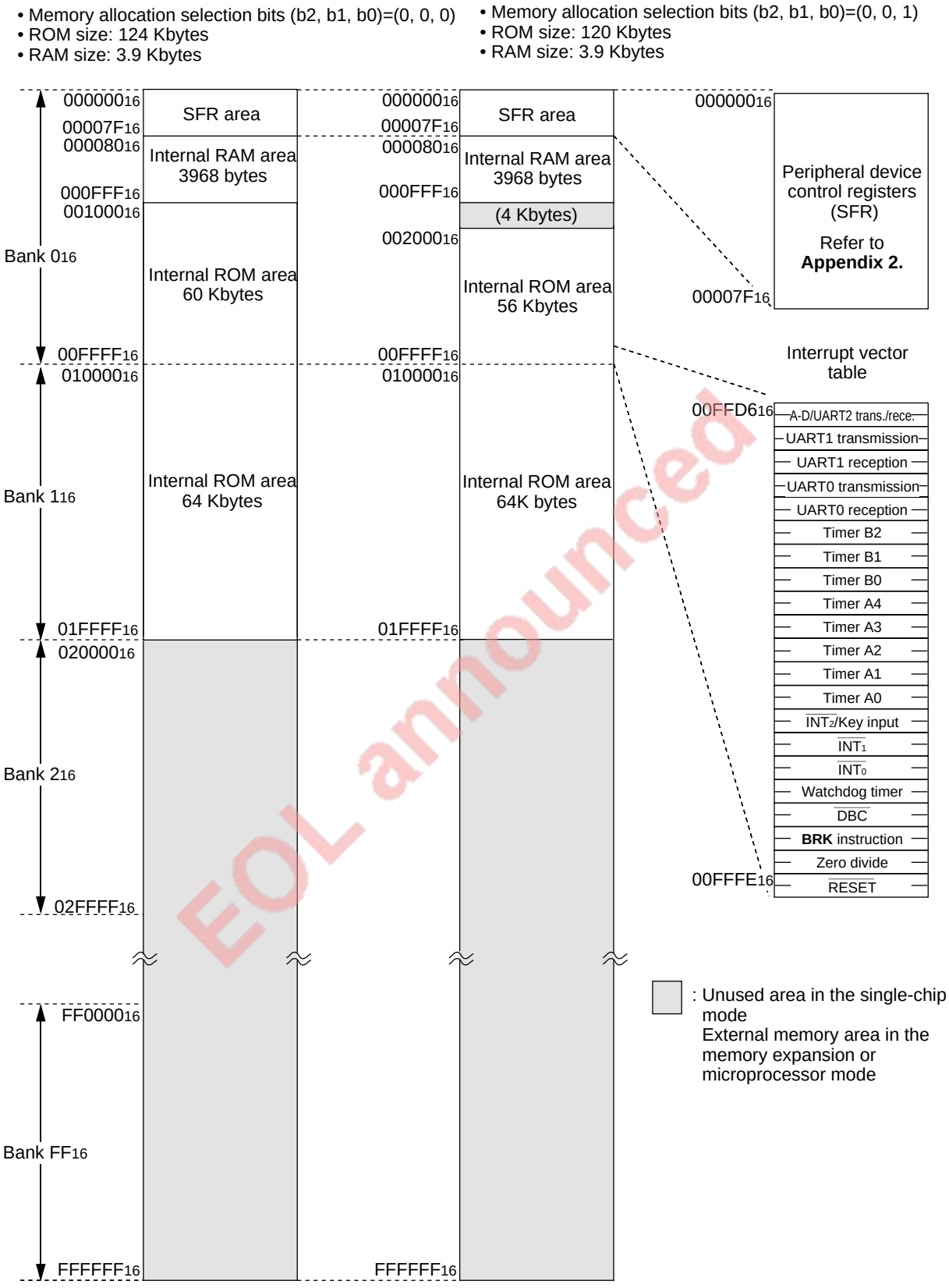
Fig. 2.4.1 Structure of memory allocation control register and its setting method

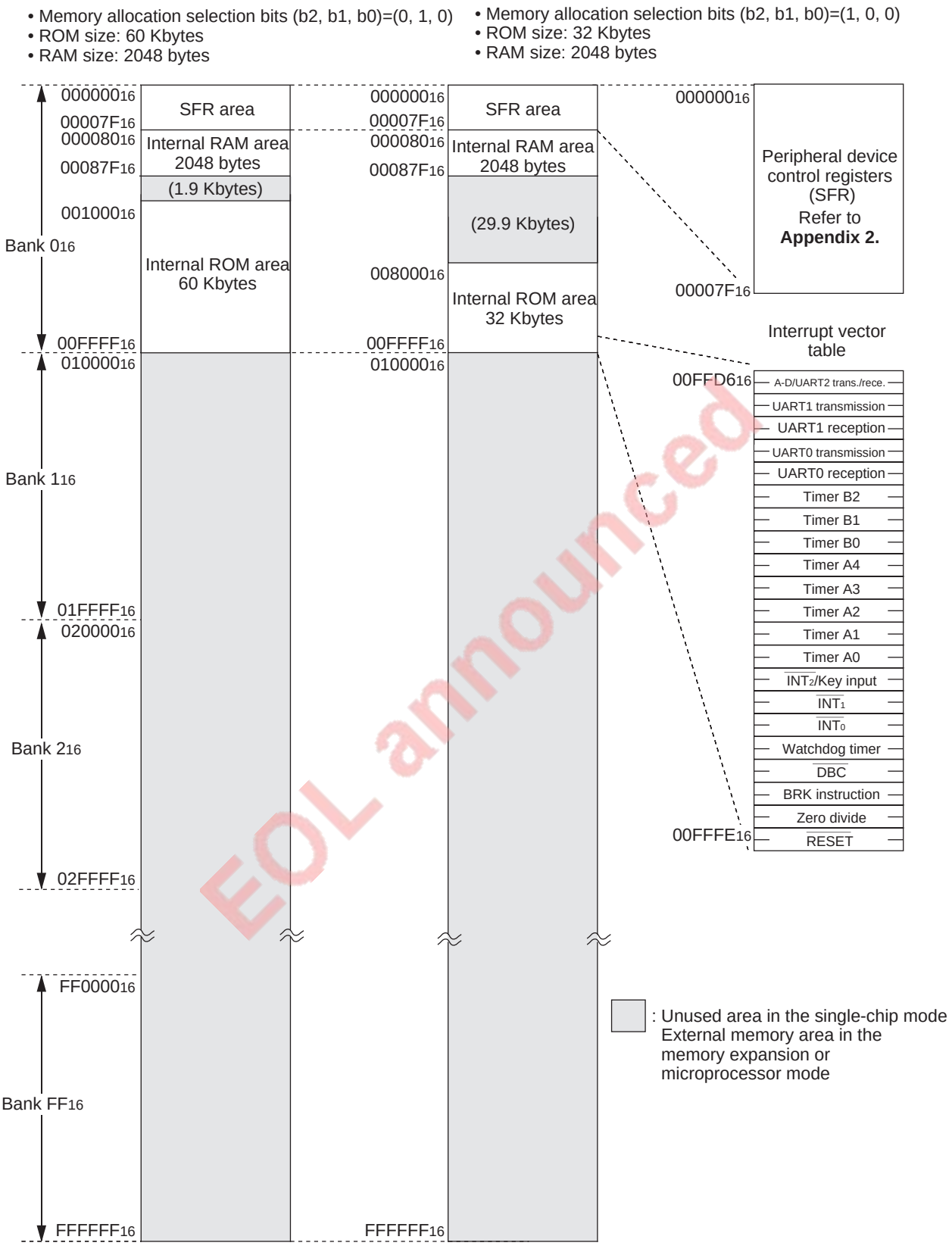
2.4 Memory allocation



Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)

2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group. (Refer to section **"Appendix 1 in part 2."**)

Fig. 2.4.2 M37733MHBXXXFP's memory map (1)

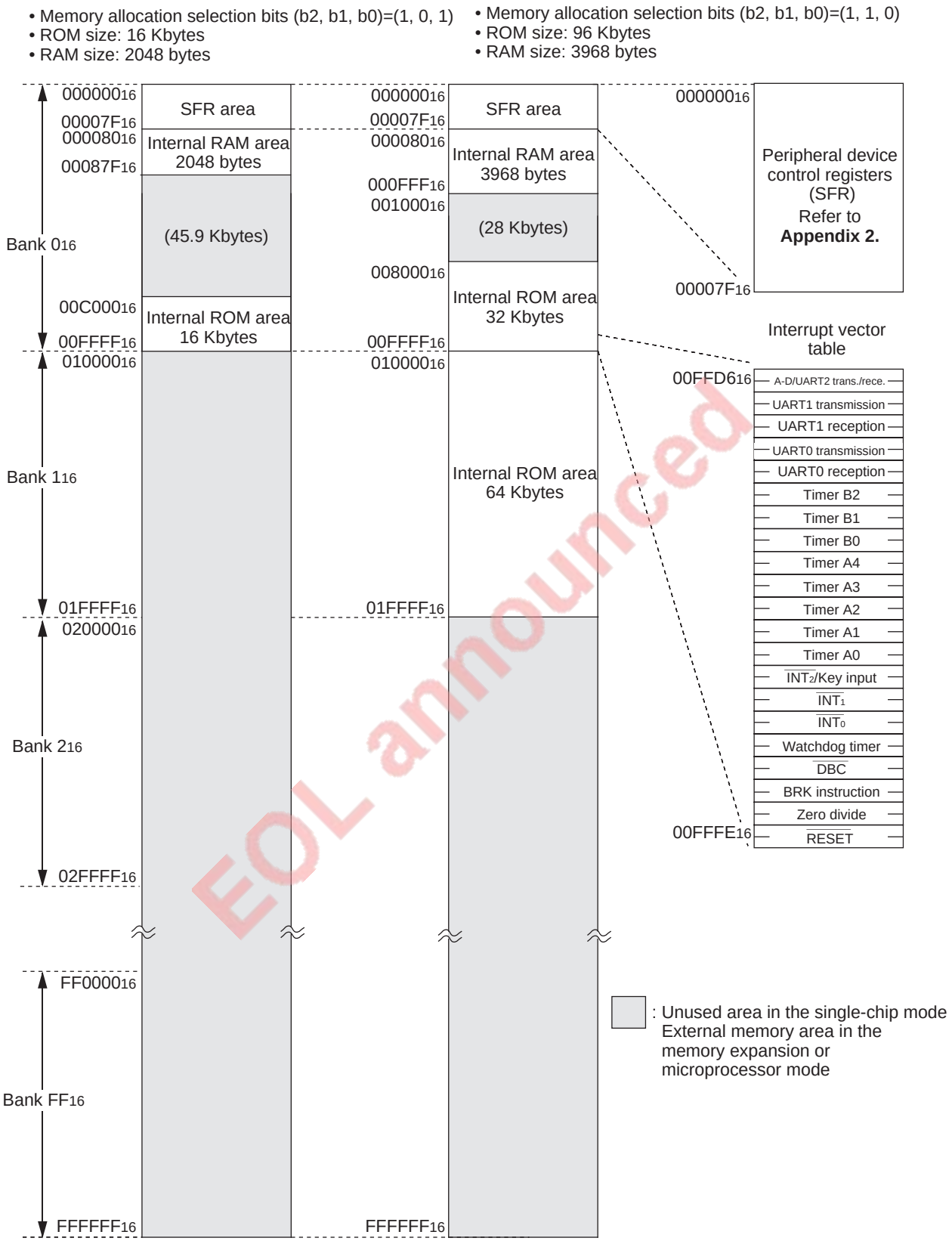


Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)

2: Banks 10$_{16}$ to FF$_{16}$ cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 2.4.3 M37733MHBXXXFP's memory map (2)

2.4 Memory allocation



EOL announced

Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)

2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 2.4.4 M37733MHBXXXFP's memory map (3)

Address (Hexadecimal notation)	
000000	
000001	
000002	Port P0 register
000003	Port P1 register
000004	Port P0 direction register
000005	Port P1 direction register
000006	Port P2 register
000007	Port P3 register
000008	Port P2 direction register
000009	Port P3 direction register
00000A	Port P4 register
00000B	Port P5 register
00000C	Port P4 direction register
00000D	Port P5 direction register
00000E	Port P6 register
00000F	Port P7 register
000010	Port P6 direction register
000011	Port P7 direction register
000012	Port P8 register
000013	
000014	Port P8 direction register
000015	
000016	
000017	
000018	
000019	
00001A	
00001B	
00001C	Reserved area **(Note)**
00001D	Reserved area **(Note)**
00001E	A-D control register 0
00001F	A-D control register 1
000020 000021	A-D register 0
000022 000023	A-D register 1
000024 000025	A-D register 2
000026 000027	A-D register 3
000028 000029	A-D register 4
00002A 00002B	A-D register 5
00002C 00002D	A-D register 6
00002E 00002F	A-D register 7
000030	UART 0 transmit/receive mode register
000031	UART 0 baud rate register (BRG0)
000032 000033	UART 0 transmission buffer register
000034	UART 0 transmit/receive control register 0
000035	UART 0 transmit/receive control register 1
000036 000037	UART 0 receive buffer register
000038	UART 1 transmit/receive mode register
000039	UART 1 baud rate register (BRG1)
00003A 00003B	UART 1 transmission buffer register
00003C	UART 1 transmit/receive control register 0
00003D	UART 1 transmit/receive control register 1
00003E 00003F	UART 1 receive buffer register

Address (Hexadecimal notation)	
000040	Count start flag
000041	
000042	One-shot start flag
000043	
000044	Up-down flag
000045	
000046 000047	Timer A0 register
000048 000049	Timer A1 register
00004A 00004B	Timer A2 register
00004C 00004D	Timer A3 register
00004E 00004F	Timer A4 register
000050 000051	Timer B0 register
000052 000053	Timer B1 register
000054 000055	Timer B2 register
000056	Timer A0 mode register
000057	Timer A1 mode register
000058	Timer A2 mode register
000059	Timer A3 mode register
00005A	Timer A4 mode register
00005B	Timer B0 mode register
00005C	Timer B1 mode register
00005D	Timer B2 mode register
00005E	Processor mode register 0
00005F	Processor mode register 1
000060	Watchdog timer register
000061	Watchdog timer frequency selection flag
000062	Reserved area **(Note)**
000063	Memory allocation control register
000064	UART2 transmit/receive mode register
000065	UART2 baud rate register (BRG2)
000066 000067	UART2 transmission buffer register
000068	UART2 transmit/receive control register 0
000069	UART2 transmit/receive control register 1
00006A 00006B	UART2 receive buffer register
00006C	Oscillation circuit control register 0
00006D	Port function control register
00006E	Serial transmit control register
00006F	Oscillation circuit control register 1
000070	A-D/UART2 trans./rece. interrupt control register
000071	UART 0 transmission interrupt control register
000072	UART 0 receive interrupt control register
000073	UART 1 transmission interrupt control register
000074	UART 1 receive interrupt control register
000075	Timer A0 interrupt control register
000076	Timer A1 interrupt control register
000077	Timer A2 interrupt control register
000078	Timer A3 interrupt control register
000079	Timer A4 interrupt control register
00007A	Timer B0 interrupt control register
00007B	Timer B1 interrupt control register
00007C	Timer B2 interrupt control register
00007D	$\overline{INT_0}$ interrupt control register
00007E	$\overline{INT_1}$ interrupt control register
00007F	$\overline{INT_2}$/Key input interrupt control register

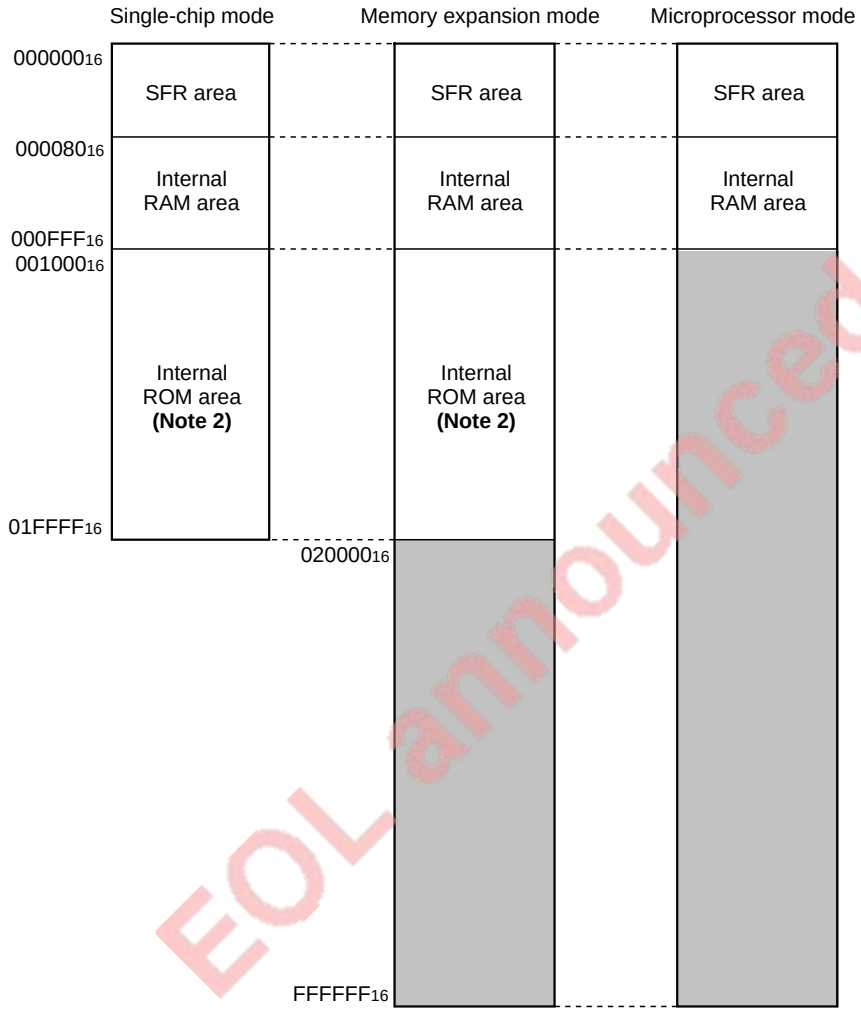
Note: Writing to reserved area is disabled.

EOL announced

Fig. 2.4.5 SFR area's memory map

2.5 Processor modes

The M37733MHBXXXFP can operate in the following three processor modes: single-chip mode, memory expansion mode, and microprocessor mode. In the M37733MHBXXXFP, some pins' functions, memory allocation, and accessible area differ according to processor modes. These differences according to processor modes are described below. Figure 2.5.1 shows the memory map in each processor mode.



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Notes 1: ▭ represents external memory area.
By accessing this area, an external device connected to the M37733MHBXXXFP can be accessed.
2: This is applied when the contents of memory allocation selection bits (bits 2 to 0 at address 63_{16}) = "000_2."
3: For the 7733 Group's microcomputers other than the M37733MHBXXXFP, refer to section **"Appendix 1. Memory allocation of 7733 Group."**

Fig. 2.5.1 Memory map in each processor mode (M37733MHBXXXFP)

2.5.1 Single-chip mode

When not using an external device, this mode is used. In this mode, ports P0 to P8 function as programmable I/O ports. (When using internal peripheral devices, they function as I/O pins.) Only the internal area (SFR, internal RAM, and internal ROM) can be accessed.
Output of $\overline{E}$ can be stopped by software. (Refer to section **"12.1 Signals required for accessing external devices."**)

2.5.2 Memory expansion and Microprocessor modes

When connecting an external device, these modes are used. In these modes, an external device can be connected to an arbitrary area in the 16-Mbyte accessible area. For access to an external device, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**
The memory expansion and microprocessor modes have the same functions except for the followings:

① In the microprocessor mode, access to the internal ROM area is forcibly disabled. This area is handled as the external area.
② In the microprocessor mode, port $P4_2$ functions as a clock ϕ_1 output pin. (**Note**)

In the memory expansion and microprocessor modes, pins P0 to P3, $P4_0$, and $P4_1$ function as I/O pins for signals required for access to an external device. Therefore, these pins cannot be used as programmable I/O ports.
If an external device is connected to a certain area which is allocated to the internal area, when this area is read, data in the internal area is fetched into the central processing unit (BIU) but data in the external area is not fetched; when data is written to this area, the data is written to the internal area and signals are output to the external at the same timing as writing to the internal area.

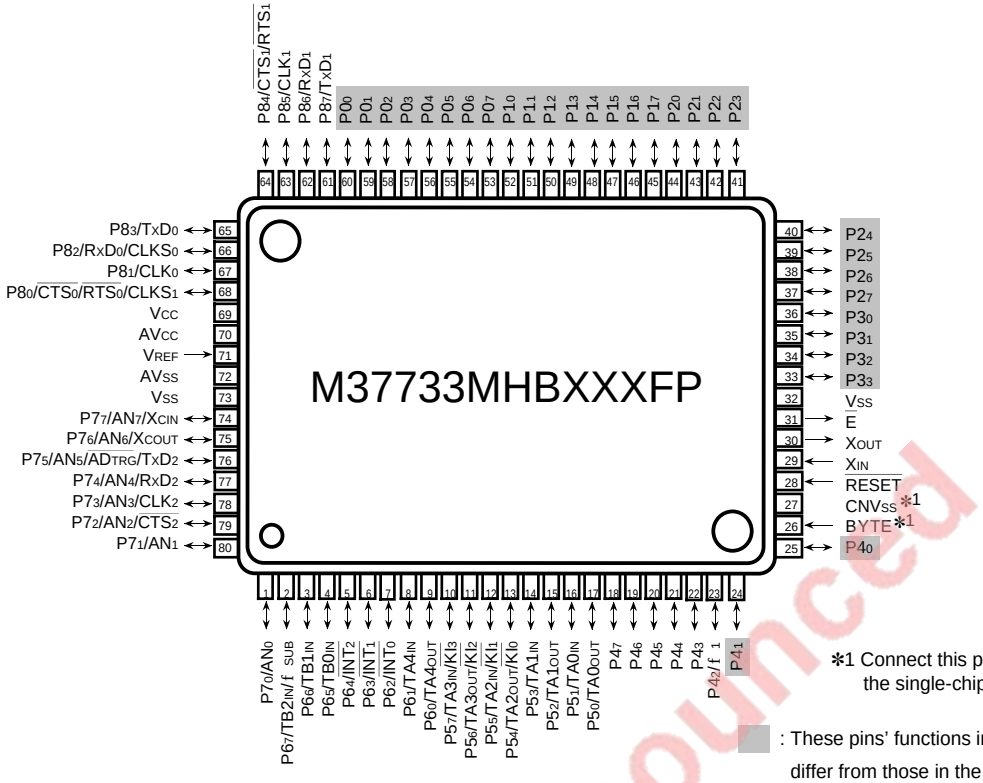
Note: Output of clock ϕ_1 can be stopped by software. (For details, refer to section **"12.1 Signals required for accessing external devices."**)

Figure 2.5.2 shows the pin configuration in each processor mode. Table 2.5.1 lists the relationship between processor modes and functions of P0 to P4.
For each pin's function, refer to section **"1.3 Pin description,"** chapters **"3. PROGRAMMABLE I/O PORTS" to "9. A-D CONVERTER"** and **"12. CONNECTING EXTERNAL DEVICES."**

EOL announced

2.5 Processor modes

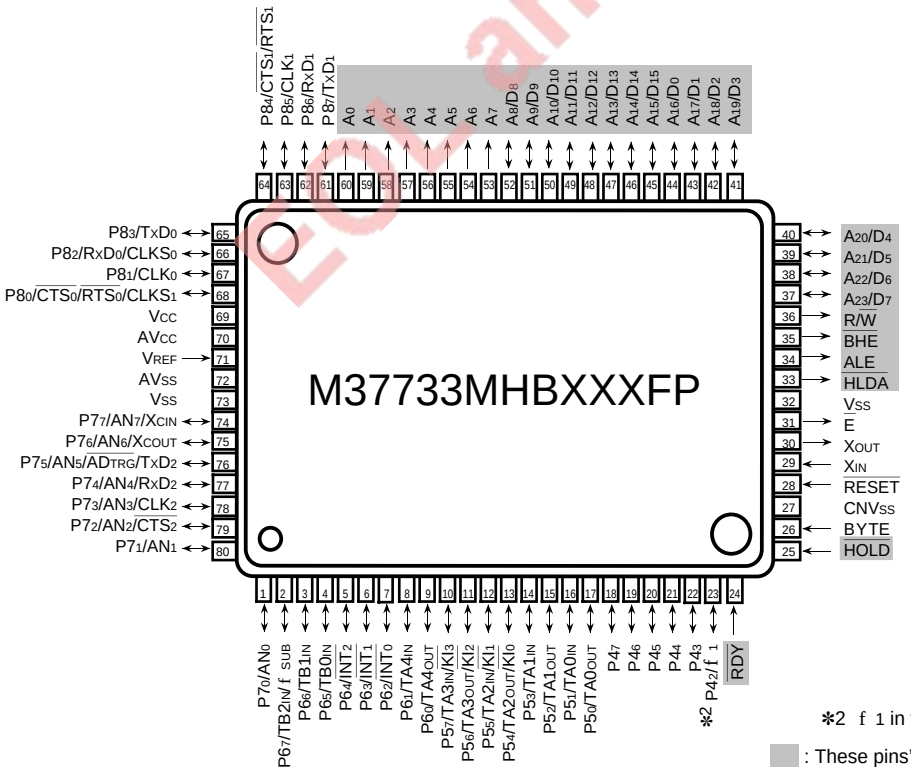
<Single-chip mode>



*1 Connect this pin to Vss in the single-chip mode.

: These pins' functions in the single-chip mode differ from those in the memory expansion or microprocessor mode.

<Memory expansion and Microprocessor modes>



*2 f 1 in the microprocessor mode

: These pins' functions in the single-chip mode differ from those in the memory expansion or microprocessor mode.

Fig. 2.5.2 Pin configuration in each processor mode (Top view)

Not announced

Table 2.5.1 Relationship between processor modes and functions of P0 to P4

Pin name \ Processor mode	Single-chip mode	Memory expansion and Microprocessor modes
P0	P P: Functions as a programmable I/O port.	A_7 to A_0
P1	P P: Functions as a programmable I/O port.	■ When external data bus is 16 bits wide (BYTE = "L") A_{15} to A_8 D(odd) D(odd): Data at odd address ■ When external data bus is 8 bits wide (BYTE = "H") A_{15} to A_8
P2	P P: Functions as a programmable I/O port.	■ When external data bus is 16 bits wide (BYTE = "L") A_{23} to A_{16} D(even) D(even): Data at even address ■ When external data bus is 8 bits wide (BYTE = "H") A_{23} to A_{16} D D: Data
P3	P P: Functions as a programmable I/O port.	$P3_3$ $\overline{HLDA}$ $P3_2$ ALE $P3_1$ $\overline{BHE}$ $P3_0$ R/$\overline{W}$
P4	P P: Functions as a programmable I/O port. (**Note 1**)	$P4_7$ to $P4_3$ P P: Functions as a programmable I/O port. $P4_2$ f_1 (**Note 2**) $P4_1$ $\overline{RDY}$ $P4_0$ $\overline{HOLD}$

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Notes 1: Pin $P4_2$ can also function as a clock f_1 output pin. (Refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**)

2: In the memory expansion mode, this pin functions as a programmable I/O port. Furthermore, it can be switched to be a clock f_1 output pin when selected by software. In the microprocessor mode, this pin is affected by the signal output disable selection bit (bit 6 at address $6C_{16}$). (Refer to chapter**"12. CONNECTING EXTERNAL DEVICES."**)

3: The above table indicates the change of pin functions owing to the switching of the processor mode.
For each signal's I/O timing in the memory expantion or microprocessor mode, refer to chapters**"12. CONNECTING EXTERNAL DEVICES"**and **"15. ELECTRICAL CHARACTERISTICS."**

2.5 Processor modes

2.5.3 Selection of processor mode

A processor mode can be selected by setting a voltage applied to pin CNVSS and the processor mode bits (bits 1 and 0 at address $5E_{16}$).

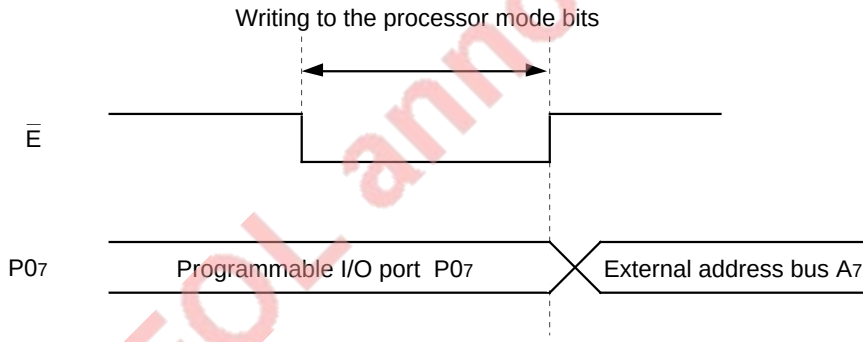
● **When Vss level is applied to pin CNVss**

After reset, the microcomputer starts operating in the single-chip mode. After the microcomputer starts operating, the processor mode can be switched by the processor mode bits. When the contents of the processor mode bits = "01_2," the memory expansion mode is selected; when the contents of these bits = "10_2," the microprocessor mode is selected. After the processor mode bits are set, the processor mode is actually switched at the rising edge of signal $\overline{E}$. Figure 2.5.3 shows the pin function switch timing when the processor mode is switched from the single-chip mode to the memory expansion or microprocessor mode by setting the processor mode bits. Note that, when the processor mode is switched during the program execution, the contents of the instruction queue buffer is not initialized. (Refer to section **"Appendix 9. Q & A."**)

● **When Vcc level is applied to pin CNVss**

After reset, the microcomputer starts operating in the microprocessor mode. In this case, the microcomputer cannot operate in the other modes. (Fix the processor mode bits to "10_2.")

Table 2.5.2 lists the method of selecting the processor mode. Figure 2.5.4 shows the structure of the processor mode register 0.



Note: Functions of pins $P0_0$ to $P0_6$, P1 to P3, $P4_0$ to $P4_2$ are switched at the timing shown above. Function of pin $P4_2$ is, however, switched only when the processor mode is switched to microprocessor mode.

Fig. 2.5.3 Pin function switch timing

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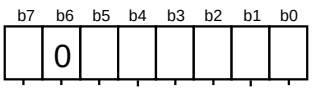
Table 2.5.2 Method of selecting processor mode

Processor mode	Pin CNVSS's level	Processor mode bits	
		b1	b0
Single-chip mode	VSS (0 V) (**Note 1**)	0	0
Memory expansion mode	VSS (0 V) (**Note 1**)	0	1
Microprocessor mode	VSS (0 V) (**Note 1**)	1	0
	VCC (5 V) (**Note 2**)		

Notes 1: The microcomputer starts operating in the single-chip mode after reset. By setting the processor mode bits, the processor mode of the microcomputer can be switched from the single-chip mode to the other modes.

2: The microcomputer starts operating in the microprocessor mode after reset. The microcomputer cannot operate in the other modes. Accordingly, so fix the processor mode bits (bits 1 and 0 at address $5E_{16}$) to "10_2."



Processor mode register 0 (address $5E_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Processor mode bits	b1 b0 0 0: Single-chip mode 0 1: Memory expansion mode 1 0: Microprocessor mode 1 1: Do not select.	0	RW
1			0 **(Note 1)**	RW
2	Wait bit	0: Software wait is inserted when accessing external area. 1: No software wait is inserted when accessing external area.	0	RW
3	Software reset bit	Microcomputer is reset by setting this bit to "1." This bit is "0" at reading.	0	WO
4	Interrupt priority detection time selection bits	b5 b4 0 0: 7 cycles of ϕ 0 1: 4 cycles of ϕ 1 0: 2 cycles of ϕ 1 1: Do not select.	0	RW
5			0	RW
6	Must be fixed to "0."		0	RW
7	Clock ϕ_1 output selection bit **(Note 2)**	0: Clock ϕ_1 output is disabled. ($P4_2$ functions as a programmable I/O port.) 1: Clock ϕ_1 output is enabled. (Port $P4_2$ functions as a clock ϕ_1 output pin.)	0	RW

Notes 1: When the Vcc-level voltage is applied to pin CNVss, this bit is set to "1" after reset. (When read, this bit is always "0.")

2: This bit is ignored in the microprocessor mode. (It may be "0" or "1.")

3: ▭ represents that bits 2 to 7 are not used for selecting a processor mode.

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Fig. 2.5.4 Structure of processor mode register 0

CENTRAL PROCESSING UNIT (CPU)

2.5 Processor modes

[Precautions on selecting processor mode]

1. The external ROM version can operate only in the microprocessor mode. Therefore, be sure to set as follows:
   •Connect pin CNVss to Vcc.
   •Fix the processor mode bits (b1, b0) to “10_2.”

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CHAPTER 3

PROGRAMMABLE I/O PORTS

3.1 Programmable I/O ports
3.2 Port peripheral circuits
3.3 Pullup function
3.4 Internal peripheral devices' I/O functions (Ports P42 and P5 to P8)

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PROGRAMMABLE I/O PORTS

3.1 Programmable I/O ports

Functions of all ports in the single-chip mode and that of ports $P4_3$ to $P4_7$ and P5 to P8 in the memory expansion and the microprocessor modes are described below. For more information about ports P0 to P4, whose functions depend on the processor mode, refer to section **"2.5 Processor modes"** and chapter **"12. CONNECTING EXTERNAL DEVICES."**

3.1 Programmable I/O ports

The 7733 Group has 68 programmable I/O ports (P0 to P8).
Each of ports P0 to P8 has a port direction register and a port register in the SFR area. Each input-only port has a port register in the SFR area. Figure 3.1.1 shows the memory map of port direction registers and port registers.
Note that ports $P4_2$ and P5 to P8 also function as I/O pins for internal peripheral devices. For details, refer to section **"3.4 Internal peripheral devices' I/O functions"** and the corresponding functional description.

addresses	
2_{16}	Port P0 register
3_{16}	Port P1 register
4_{16}	Port P0 direction register
5_{16}	Port P1 direction register
6_{16}	Port P2 register
7_{16}	Port P3 register
8_{16}	Port P2 direction register
9_{16}	Port P3 direction register
A_{16}	Port P4 register
B_{16}	Port P5 register
C_{16}	Port P4 direction register
D_{16}	Port P5 direction register
E_{16}	Port P6 register
F_{16}	Port P7 register
10_{16}	Port P6 direction register
11_{16}	Port P7 direction register
12_{16}	Port P8 register
13_{16}	
14_{16}	Port P8 direction register

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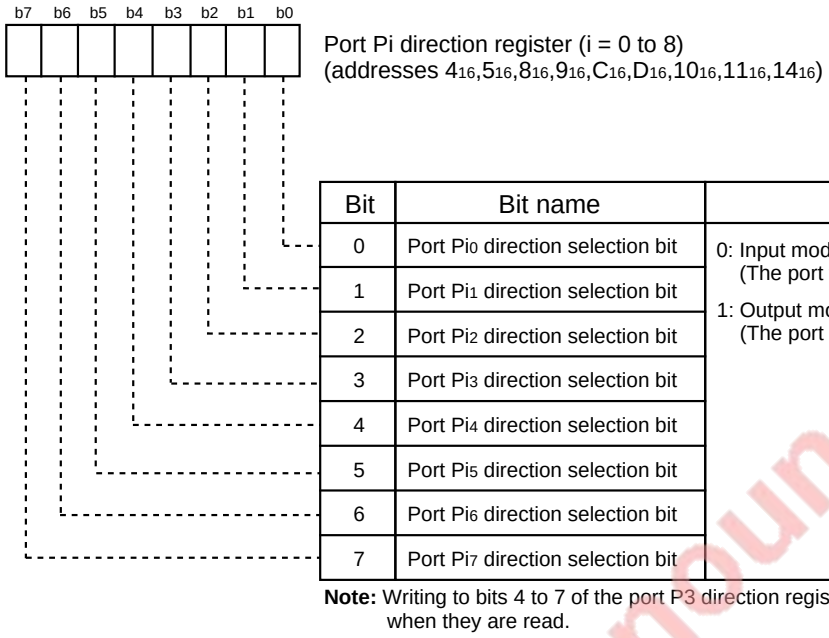
Fig. 3.1.1 Memory map of port direction registers and port registers

3.1.1 Port Pi direction register

This register determines the direction of programmable I/O ports. Each bit of this register corresponds to one specified pin.

Figure 3.1.2 shows the structure of the port Pi (i = 0 to 8) direction register.



Port Pi direction register (i = 0 to 8)
(addresses 4_{16},5_{16},8_{16},9_{16},C_{16},D_{16},10_{16},11_{16},14_{16})

Bit	Bit name	Functions	At reset	RW
0	Port Pi_0 direction selection bit	0: Input mode (The port functions as an input port.) 1: Output mode (The port functions as an output port.)	0	RW
1	Port Pi_1 direction selection bit		0	RW
2	Port Pi_2 direction selection bit		0	RW
3	Port Pi_3 direction selection bit		0	RW
4	Port Pi_4 direction selection bit		0	RW
5	Port Pi_5 direction selection bit		0	RW
6	Port Pi_6 direction selection bit		0	RW
7	Port Pi_7 direction selection bit		0	RW

Note: Writing to bits 4 to 7 of the port P3 direction register is invalid and these bits are fixed to “0” when they are read.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Corresponding pin	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0

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Fig. 3.1.2 Structure of port Pi (i = 0 to 8) direction register

PROGRAMMABLE I/O PORTS

3.1 Programmable I/O ports

3.1.2 Port Pi register

Data is input from or output to an external device by writing/reading data to/from a port register. A port register consists of a port latch, which holds the output data, and a circuit, which reads the pin state. Each bit of the port register corresponds to one specified pin. Figure 3.1.3 shows the structure of the port Pi (i = 0 to 8) register.

(1) How to output data from programmable I/O port

① Set the corresponding bit of the port direction register to the output mode.
② Write data to the corresponding bit of the port register, and then the data is written into the port latch.
③ Data set in the port latch is output.

When a bit of a port register which corresponds to a port set for the output mode is read out, the contents of the port latch, instead of pin state, is read out. Accordingly, output data can correctly be read out without influence of external load, etc. (Refer to **Figures 3.2.1 and 3.2.2**)

(2) How to input data from programmable I/O port

① Set the corresponding bit of the port direction register to the input mode.
② The pin enters a floating state.
③ When reading the corresponding bit of the port register in state ②, data input from the pin can be read in.

When data is written to a port register which corresponds to a port set for the input mode, the data is written only into the port latch and not output to the external devices. Pins retain a floating state.

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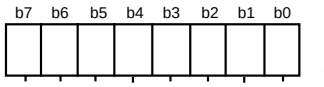

Port Pi register (i = 0 to 8)
(addresses 2_{16},3_{16},6_{16},7_{16},A_{16},B_{16},E_{16},F_{16},12_{16})

Bit	Bit name	Functions	At reset	RW
0	Port Pi_0's pin	Data is input from or output to a pin by reading from or writing to the corresponding bit. 0: "L" level 1: "H" level	Undefined	RW
1	Port Pi_1's pin		Undefined	RW
2	Port Pi_2's pin		Undefined	RW
3	Port Pi_3's pin		Undefined	RW
4	Port Pi_4's pin		Undefined	RW
5	Port Pi_5's pin		Undefined	RW
6	Port Pi_6's pin		Undefined	RW
7	Port Pi_7's pin		Undefined	RW

Note: Writing to bits 4 to 7 of the port P3 register is invalid and these bits are fixed to "0" when they are read.

Fig. 3.1.3 Structure of port Pi (i = 0 to 8) register

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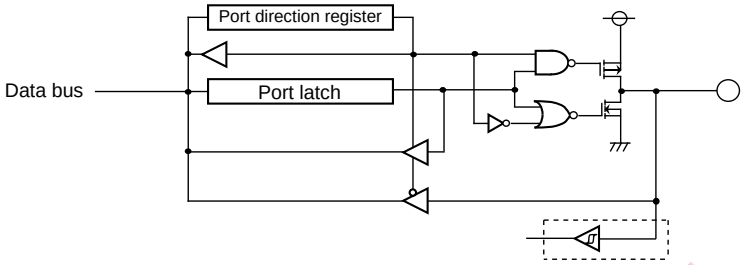
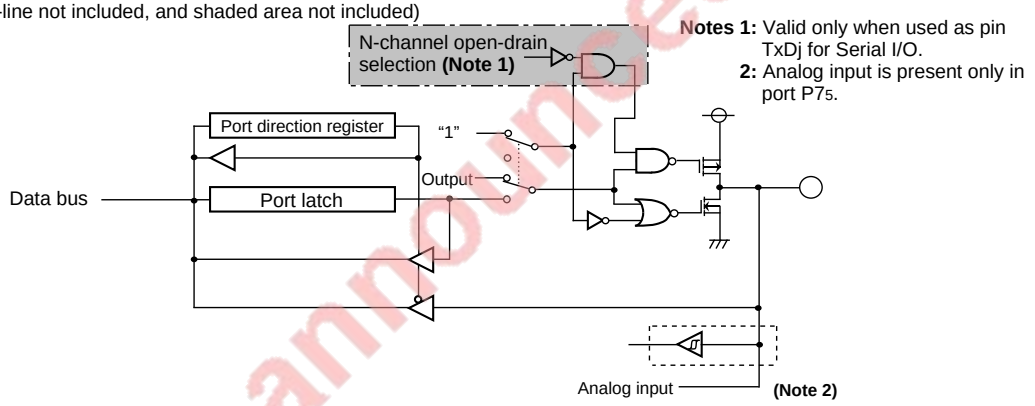
3.2 Port peripheral circuits

Figures 3.2.1 and 3.2.2 show the port peripheral circuits.

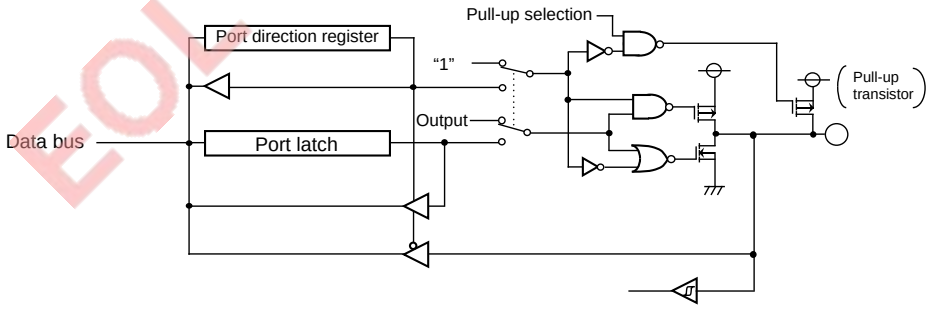
• Ports $P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_3$, $P4_3$ to $P4_6$ (Inside dotted-line not included)
Ports $P4_0/\overline{HOLD}$, $P4_1/\overline{RDY}$, $P4_7$, $P5_1/TA0_{IN}$, $P5_3/TA1_{IN}$, $P6_1/TA4_{IN}$, $P6_5/TB0_{IN}$ to $P6_7/TB2_{IN}/\phi_{SUB}$, $P8_6/RxD_1$ (Inside dotted-line included)



• Ports $P8_3/TxD_0$, $P8_7/TxD_1$ (Inside dotted-line not included, and shaded area included)
Ports $P5_0/TA0_{OUT}$, $P5_2/TA1_{OUT}$, $P6_0/TA4_{OUT}$, $P7_5/AN_5/\overline{AD_{TRG}}/TxD_2$, $P8_2/RxD_0/CLKS_0$ (Inside dotted-line included, and shaded area not included)
Port $P4_2/\phi_1$ (Inside dotted-line not included, and shaded area not included)



• Ports $P5_4/TA2_{OUT}/\overline{KI_0}$, $P5_6/TA3_{OUT}/\overline{KI_2}$



• Ports $P5_5/TA2_{IN}/\overline{KI_1}$, $P5_7/TA3_{IN}/\overline{KI_3}$, $P6_2/\overline{INT_0}$ to $P6_4/\overline{INT_2}$

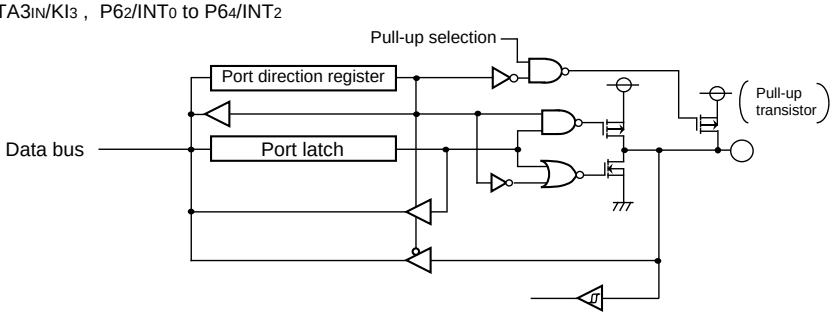


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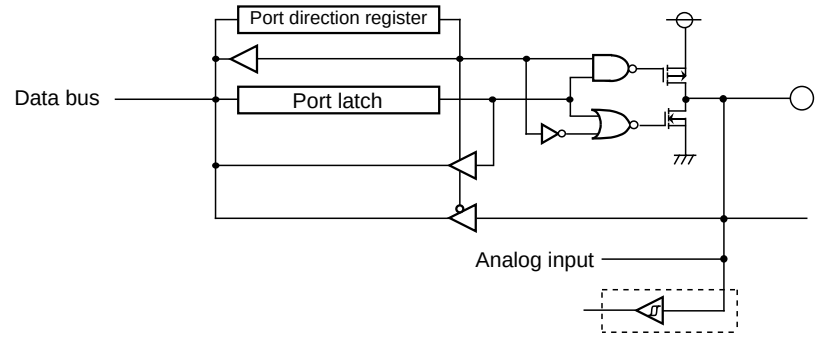
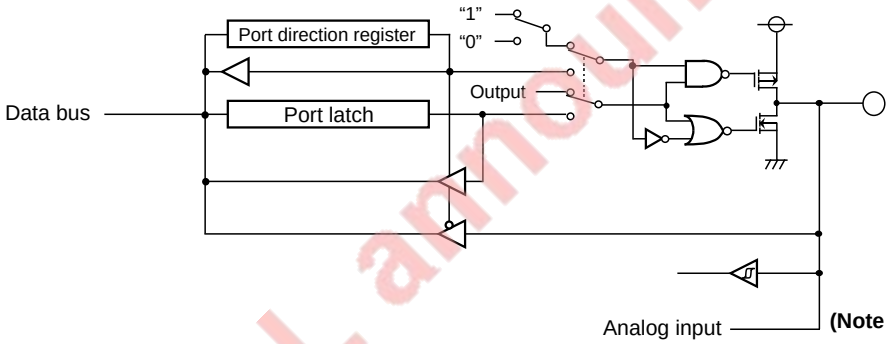
Fig. 3.2.1 Port peripheral circuits (1)

• Ports $P7_0/AN_0$, $P7_1/AN_1$, $P7_6/AN_6/X_{COUT}$, $P7_7/AN_7/X_{CIN}$ (Inside dotted-line not included)
Ports $P7_2/AN_2/\overline{CTS_2}$, $P7_4/AN_4/RxD_2$ (Inside dotted-line included)



Note 1: The sub-clock oscillation circuit is present only in ports $P7_6$ and $P7_7$

• Ports $P7_3/AN_3/CLK_2$, $P8_0/\overline{CTS_0}/\overline{RTS_0}/CLKS_1$, $P8_1/CLK_0$, $P8_4/\overline{CTS_1}/\overline{RTS_1}$, $P8_5/CLK_1$



Note 2: Analog input is present only in port $P7_3$

• $\overline{E}$

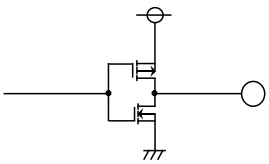


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Fig. 3.2.2 Port peripheral circuits (2)

3.3 Pull-up function

3.3.1 Pull-up function for ports P5$_4$ to P5$_7$ ($\overline{KI_0}$ to $\overline{KI_3}$)

Ports P5$_4$ to P5$_7$ ($\overline{KI_0}$ to $\overline{KI_3}$) can be pulled high by setting the port P5 pull-up selection bit (bit 6 at address 6D$_{16}$). Figure 3.3.1 shows the structure of the port function control register.
When pulling ports P5$_4$ to P5$_7$ high, clear bits 4 to 7 at address D$_{16}$ (Port P5 direction register) to “0.”

3.3.2 Pull-up function for ports P6$_2$ to P6$_4$ ($\overline{INT_0}$ to $\overline{INT_2}$)

Ports P6$_2$ and P6$_3$ ($\overline{INT_0}$ and $\overline{INT_1}$) can be pulled high by setting the port P6 pull-up selection bit 0 (bit 3 at address 6D$_{16}$). Port P6$_4$ ($\overline{INT_2}$) can be pulled high by setting the port P6 pull-up selection bit 1 (bit 5 at address 6D$_{16}$). Figure 3.3.1 shows the structure of the port function control register.
When pulling ports P6$_2$ to P6$_4$ high, clear bits 2 to 4 at address 10$_{16}$ (port P6 direction register) to “0.”

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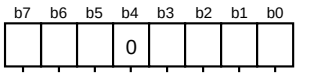

Port function control register (address $6D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Standby state selection bit	0: Pins P0 to P3 are used for the external bus output. 1: Pins P0 to P3 are used for the port output.	0	RW
1	Sub-clock output selection bit/ Timer B2 clock source selection bit	•Port-Xc selection bit* = "0" (when the sub clock is not used) Timer B2 (event counter mode) clock source selection **(Note 1)** 0: $TB2_{IN}$ input (event counter mode) 1: Main clock divided by 32 (clock timer) •Port-Xc selection bit = "1" (when the sub clock is used) Sub-clock output selection 0: Pin $P6_7/TB2_{IN}/\phi_{SUB}$ functions as a programmable I/O port. 1: Sub clock ϕ_{SUB} is output from pin $P6_7/TB2_{IN}/\phi_{SUB}$.	0	RW
2	Timer B1 internal connect selection bit **(Note 2)**	0: No internal connection 1: Internal connection with timer B2	0	RW
3	Port P6 pull-up selection bit 0	0: No pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$ 1: With pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$	0	RW
4	Must be fixed to "0."		0	RW
5	Port P6 pull-up selection bit 1	•Key input interrupt selection bit = "0" 0: No pull-up for pin $P6_4/\overline{INT_2}$ 1: With pull-up for pin $P6_4/\overline{INT_2}$ •Key input interrupt selection bit = "1" 0: Pin $P6_4/\overline{INT_2}$ is a port with no pull-up. 1: Pin $P6_4/\overline{INT_2}$ is an input pin with pull-up and is used for the key input interrupt.	0	RW
6	Port P5 pull-up selection bit	0: No pull-up for pins $P5_4/TA2_{OUT}/\overline{KI_0}$ to $P5_7/TA3_{IN}/\overline{KI_3}$ 1: With pull-up for pins $P5_4/TA2_{OUT}/\overline{KI_0}$ to $P5_7/TA3_{IN}/\overline{KI_3}$	0	RW
7	Key input interrupt selection bit	0: $\overline{INT_2}$ interrupt 1: Key input interrupt	0	RW

Port-Xc selection bit* : Bit 4 of the oscillation circuit control register 0 (address $6C_{16}$)

Notes 1: When the port-Xc selection bit = "0" and timer B2 operates in the timer mode or the pulse period /pulse width measurement mode, bit 1 is invalid.
2: When timer B1 operates in the event counter mode, bit 2 is valid.
3: ☐ represents that bits 0 to 2, 4, and 7 are not used for the pull-up function.

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Fig. 3.3.1 Structure of port function control register

3.4 Internal peripheral devices' I/O functions (Ports P42 and P5 to P8)

Ports P42 and P5 to P8 also function as I/O pins for the internal peripheral devices. Table 3.4.1 lists correspondence between each port and internal peripheral devices' I/O pin. For internal peripheral devices' I/O functions, refer to the corresponding functional description. For the clock ϕ_1 output pin, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."** For the sub-clock oscillation circuit's I/O pins, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Table 3.4.1 Correspondence between each port and internal peripheral devices' I/O pin

Port	Internal peripheral devices' I/O pin
P42	Clock ϕ_1 output pin
P50 to P53	Timer A's I/O pins
P54 to P57	Timer A's I/O pins/Key input interrupt function's input pins
P60, P61	Timer A's I/O pins
P62 to P64	Input pins for external interrupts
P65, P66	Timer B's input pins
P67	Timer B's input pin/Clock ϕ_{SUB} output pin
P70, P71	A-D converter's input pins
P72 to P75	A-D converter's input pins/I/O pins for serial I/O
P76, P77	Sub-clock oscillation circuit's I/O pins/A-D converter's input pins
P8	I/O pins for serial I/O

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CHAPTER 4

INTERRUPTS

EOL announced

4.1 Overview
4.2 Interrupt sources
4.3 Interrupt control
4.4 Interrupt priority level
4.5 Interrupt priority level detection circuit
4.6 Interrupt priority level detection time
4.7 How interrupts are processed (from acceptance of interrupt request till execution of interrupt routine)
4.8 Return from interrupt routine
4.9 Multiple interrupts
4.10 External interrupts ($\overline{\text{INTi}}$ interrupt)
4.11 Precautions for interrupts

INTERRUPTS

4.1 Overview

The 7733 Group provides 19 interrupt sources to generate interrupt requests.

4.1 Overview

Figure 4.1.1 shows how interrupts are processed.
When an interrupt request is accepted, a program branches to the start address of an interrupt routine which is set in the interrupt vector table (addresses FFD6$_{16}$ to FFFF$_{16}$). Set the start address of each interrupt routine to the corresponding interrupt vector address in the interrupt vector table.

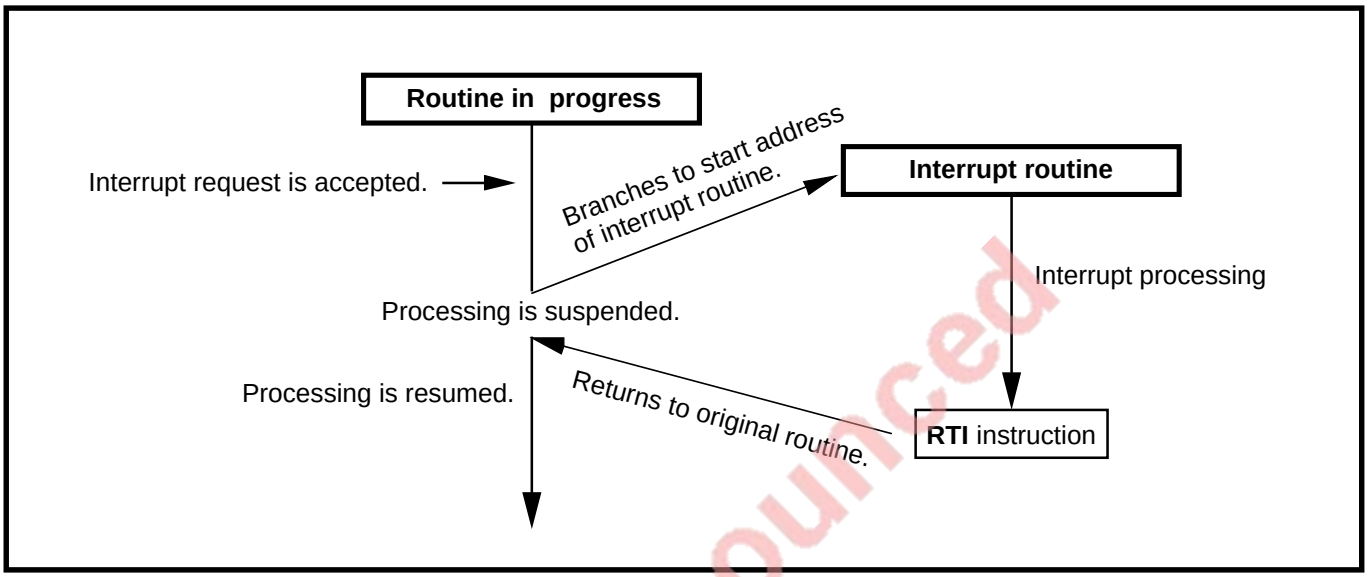

Fig. 4.1.1 How interrupts are processed

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4.1 Overview

When an interrupt request is accepted, the following registers' contents immediately before acceptance of an interrupt request are automatically pushed onto the stack area ①, ②, and ③ in that order:

① Program bank register (PG)
② Program counter (PCL, PCH)
③ Processor status register (PSL, PSH)

Figure 4.1.2 shows the state of the stack area immediately before the program branches to an interrupt routine.
At the end of the interrupt routine, execute the **RTI** instruction, which is an instruction for returning to the routine that was executed before acceptance of an interrupt request. By executing the **RTI** instruction, the above registers' contents, which were pushed onto the stack area, are popped ③, ②, and ① in that order. Then, execution of the suspended routine is resumed from where it left off.
When an interrupt request is accepted and the **RTI** instruction is executed, above registers (① to ③) are automatically pushed and popped. For other registers whose contents are necessary, be sure to push and pop them by software.

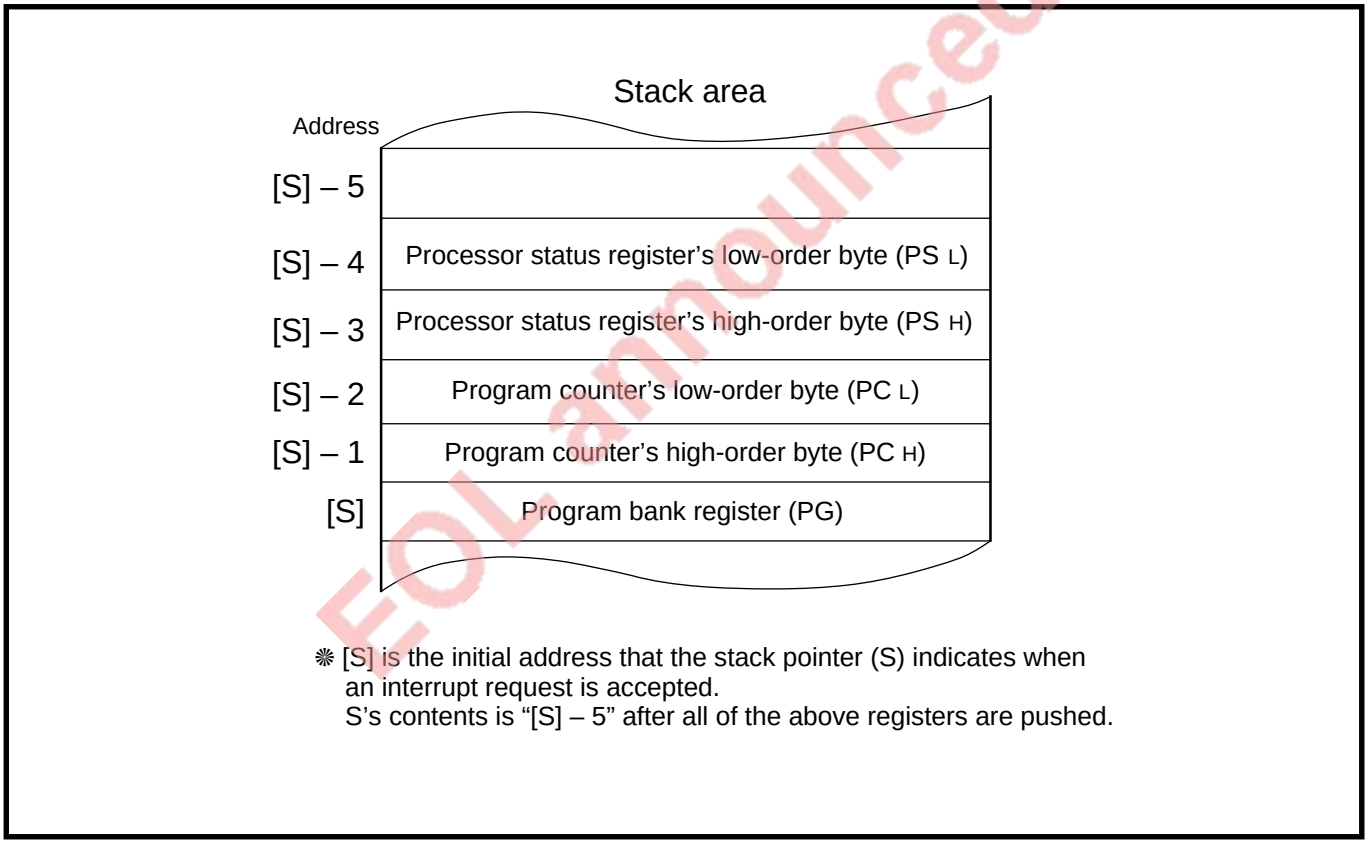

Fig. 4.1.2 State of stack area immediately before program branches to interrupt routine

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4.2 Interrupt sources

Table 4.2.1 lists interrupt sources and their vector addresses. When programming, set the start address of each interrupt routine to the vector addresses listed below.

Table 4.2.1 Interrupt sources and Interrupt vector addresses

Interrupt source	Interrupt vector addresses		Remarks
	High-order address	Low-order address	
Reset	$00FFFF_{16}$	$00FFFE_{16}$	Non-maskable
Zero division	$00FFFD_{16}$	$00FFFC_{16}$	Non-maskable software interrupt
BRK instruction	$00FFFB_{16}$	$00FFFA_{16}$	Non-maskable software interrupt
$\overline{DBC}$ (**Note 1**)	$00FFF9_{16}$	$00FFF8_{16}$	Not used usually
Watchdog timer	$00FFF7_{16}$	$00FFF6_{16}$	Non-maskable interrupt
INT_0	$00FFF5_{16}$	$00FFF4_{16}$	External interrupt by signal input from pin INT_0
INT_1	$00FFF3_{16}$	$00FFF2_{16}$	External interrupt by signal input from pin INT_1
INT_2/Key input (**Note 2**)	$00FFF1_{16}$	$00FFF0_{16}$	External interrupt by signal input from pin INT_2 or by key input
Timer A0	$00FFEF_{16}$	$00FFEE_{16}$	Internal interrupt from Timer A0
Timer A1	$00FFED_{16}$	$00FFEC_{16}$	Internal interrupt from Timer A1
Timer A2	$00FFEB_{16}$	$00FFEA_{16}$	Internal interrupt from Timer A2
Timer A3	$00FFE9_{16}$	$00FFE8_{16}$	Internal interrupt from Timer A3
Timer A4	$00FFE7_{16}$	$00FFE6_{16}$	Internal interrupt from Timer A4
Timer B0	$00FFE5_{16}$	$00FFE4_{16}$	Internal interrupt from Timer B0
Timer B1	$00FFE3_{16}$	$00FFE2_{16}$	Internal interrupt from Timer B1
Timer B2	$00FFE1_{16}$	$00FFE0_{16}$	Internal interrupt from Timer B2
UART0 reception	$00FFDF_{16}$	$00FFDE_{16}$	Internal interrupt from UART0
UART0 transmission	$00FFDD_{16}$	$00FFDC_{16}$	
UART1 reception	$00FFDB_{16}$	$00FFDA_{16}$	Internal interrupt from UART1
UART1 transmission	$00FFD9_{16}$	$00FFD8_{16}$	
A-D/UART2 trans./ /rece. **(Note 3)**	$00FFD7_{16}$	$00FFD6_{16}$	Internal interrupt from A-D converter or UART2

EOL announced

Notes 1: This is only for debugger control and is not used usually.

2: When the key input interrupt selection bit (bit 7 at address $6D_{16}$) = "1," the key input interrupt function is selected. For details, refer to chapter **"5 KEY INPUT INTERRUPT FUNCTION."**

3: The A-D conversion interrupt and the UART2 transmission/reception interrupt share the same interrupt vector addresses and interrupt control register. By setting the serial I/O mode selection bits (bits 0 to 2 at address 64_{16}), the A-D conversion interrupt or UART2 transmission/reception interrupt is selected.

Table 4.2.2 lists occurrence conditions of internal interrupt requests, which occur because of internal operations.

Table 4.2.2 Occurrence conditions of internal interrupt requests

Interrupt	Occurrence conditions of interrupt requests
Zero division interrupt	Occurs when divider is "0" in execution of **DIV** instruction (Division instruction). (Refer to **"7700 Family Software Manual."**)
BRK instruction interrupt	Occurs when the **BRK** instruction is executed. (Refer to **"7700 Family Software Manual."**)
Watchdog timer interrupt	Occurs when the most significant bit of the watchdog timer becomes "0." (Refer to chapter **"10 WATCHDOG TIMER."**)
Timer Ai interrupt (i = 0 to 4)	Occurrence condition depends on Timer Ai's operating modes. (Refer to chapter **"6 TIMER A."**)
Timer Bi interrupt (i = 0 to 2)	Occurrence condition depends on Timer Bi's operating modes. (Refer to chapter **"7 TIMER B."**)
UARTi reception interrupt (i = 0,1)	Occurs at serial data reception. (Refer to chapter **"8 SERIAL I/O."**)
UARTi transmission interrupt (i = 0,1)	Occurs at serial data transmission. (Refer to chapter **"8 SERIAL I/O."**)
UART2 transmission /reception interrupt	Occurs at serial data transmission/reception. (Refer to chapter **"8 SERIAL I/O."**)
A-D conversion interrupt	Occurs when A-D conversion is completed. (Refer to chapter **"9 A-D CONVERTER."**)

For external interrupts, refer to section **"4.10 External interrupts."** For the key input interrupt, refer to chapter **"5 KEY INPUT INTERRUPT FUNCTION."**

EOL announced

4.3 Interrupt control

Maskable interrupts are enabled or disabled by setting the following:

- Interrupt request bit
- Interrupt priority level selection bits
- Processor interrupt priority level (IPL)
- Interrupt disable flag (I)

The interrupt disable flag (I) and processor interrupt priority level (IPL) are allocated to the processor status register (PS). An interrupt request bit and the interrupt priority level selection bits are allocated to the interrupt control register for the corresponding interrupt.
Figure 4.3.1 shows the memory map of interrupt control registers and Figure 4.3.2 shows their structures.

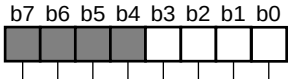
- **Maskable interrupts** : By software, acceptance of these interrupts' requests can be disabled.

- **Non-maskable interrupts** (Zero division, **BRK** instruction, and watchdog timer interrupts)
  : When an interrupt request occurs, it is certain to be accepted. They do not have interrupt control registers and are not affected by the interrupt disable flag (I).

EOL announced

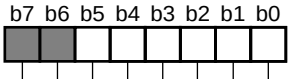
Address	
70₁₆	A-D/UART2 trans./rece. interrupt control register
71₁₆	UART0 transmission interrupt control register
72₁₆	UART0 receive interrupt control register
73₁₆	UART1 transmission interrupt control register
74₁₆	UART1 receive interrupt control register
75₁₆	Timer A0 interrupt control register
76₁₆	Timer A1 interrupt control register
77₁₆	Timer A2 interrupt control register
78₁₆	Timer A3 interrupt control register
79₁₆	Timer A4 interrupt control register
7A₁₆	Timer B0 interrupt control register
7B₁₆	Timer B1 interrupt control register
7C₁₆	Timer B2 interrupt control register
7D₁₆	$\overline{INT_0}$ interrupt control register
7E₁₆	$\overline{INT_1}$ interrupt control register
7F₁₆	$\overline{INT_2}$/Key input interrupt control register

Fig. 4.3.1 Interrupt control registers' memory map



A-D/UART2 trans./rece., UART0 and 1 transmission, UART0 and 1 receive, Timers A0 to A4, Timers B0 to B2 interrupt control registers (addresses 70₁₆ to 7C₁₆)

Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2b1b0 0 0 0 : Level 0 (Interrupt is disabled.) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
4	Not implemented.		Un-defined	—
5				
6				
7				



$\overline{INT0}$, $\overline{INT1}$, and $\overline{INT2}$/Key input interrupt control registers (addresses 7D₁₆ to 7F₁₆)

Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2b1b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit **(Note)**	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
4	Polarity selection bit	0: Interrupt request bit is set to "1" at "H" level when level sense is selected; this bit is set to "1" at falling edge when edge sense is selected. 1: Interrupt request bit is set to "1" at "L" level when level sense is selected; this bit is set to "1" at rising edge when level sense is selected.	0	RW
5	Level sense/Edge sense selection bit	0: Edge sense 1: Level sense	0	RW
6	Not implemented.		Un-defined	—
7				

Note: The interrupt request bits of $\overline{INT0}$ to $\overline{INT2}$/Key input interrupts are ignored when the level sense is selected.

EOL announced

Fig. 4.3.2 Interrupt control registers' structures

INTERRUPTS

4.3 Interrupt control

4.3.1 Interrupt disable flag (I)

This flag can disable all maskable interrupts. When this flag is set to “1,” all maskable interrupts are disabled; when this flag is cleared to “0,” all maskable interrupts are enabled. Because this flag is set to “1” at reset, clear this flag to “0” when enabling interrupts.
This flag is allocated to the processor status register (PS).

4.3.2 Interrupt request bit

When an interrupt request occurs, this bit is set to “1.” And then, this bit remains set to “1” until the interrupt request is accepted; this bit is cleared to “0” when the interrupt request is accepted.
This bit can be set to “1” or cleared to “0” by software, also.
Note that when an $\overline{INT_i}$ interrupt is used with the level sense selected, the $\overline{INT_i}$ interrupt request bit (i = 0 to 2) is ignored.

4.3.3 Interrupt priority level selection bits and Processor interrupt priority level (IPL)

The interrupt priority level selection bits are used to set the priority level of an interrupt.
When an interrupt request occurs, its interrupt priority level is compared with the processor interrupt priority level (IPL). Only when the comparison result satisfies the following relationship, the interrupt request is enabled. Therefore, by setting the interrupt priority level to 0, the interrupt can be disabled.
The processor interrupt priority level (IPL) is allocated to the processor status register (PS).

Interrupt priority level > Processor interrupt priority level (IPL)

Table 4.3.1 lists the settings of interrupt priority levels. Table 4.3.2 lists the relationship between the IPL’s contents and enabled interrupt priority levels.

The interrupt disable flag (I), interrupt request bit, interrupt priority level selection bits, and processor interrupt priority level (IPL) are independent of each other; they do not affect each other. Interrupt requests are accepted only when the following conditions are satisfied.

- Interrupt disable flag (I) = “0”
- Interrupt request bit = “1”
- Interrupt priority level > Processor interrupt priority level (IPL)

EOL announced

Table 4.3.1 Settings of interrupt priority levels

Interrupt priority level selection bits			Interrupt priority level	Priority
b2	b1	b0		
0	0	0	Level 0 (Interrupt is disabled.)	—
0	0	1	Level 1	Low
0	1	0	Level 2	↓
0	1	1	Level 3	
1	0	0	Level 4	
1	0	1	Level 5	
1	1	0	Level 6	
1	1	1	Level 7	High

Table 4.3.2 Relationship between IPL's contents and enabled interrupt priority levels

IPL_2	IPL_1	IPL_0	Enabled interrupt priority levels
0	0	0	Level 1 and above levels
0	0	1	Level 2 and above levels
0	1	0	Level 3 and above levels
0	1	1	Level 4 and above levels
1	0	0	Level 5 and above levels
1	0	1	Levels 6 and 7
1	1	0	Level 7 only
1	1	1	All maskable interrupts are disabled.

IPL_0: Bit 8 in the processor status register (PS)
IPL_1: Bit 9 in the processor status register (PS)
IPL_2: Bit 10 in the processor status register (PS)

EOL announced

4.4 Interrupt priority level

When the interrupt disable flag (I) = “0” (in other words, when interrupts are enabled), if multiple interrupt requests reside at the same sampling timing, where the presence of an interrupt request is checked, these requests are accepted in order of priority levels. In this case, an interrupt request which has the highest priority is accepted first.

For 16 interrupt sources other than software interrupts (the zero division and **BRK** instruction) and a watchdog timer interrupt, an arbitrary priority level can be set by specifying the interrupt priority level selection bits. Note that the priority level for reset (handled as an interrupt which has the highest priority) or a watchdog timer interrupt is set by hardware. Figure 4.4.1 shows the interrupt priority level set by hardware.

Note that software interrupts are not affected by the interrupt priority level. When the zero division or **BRK** instruction is executed, a program branches to an interrupt routine.

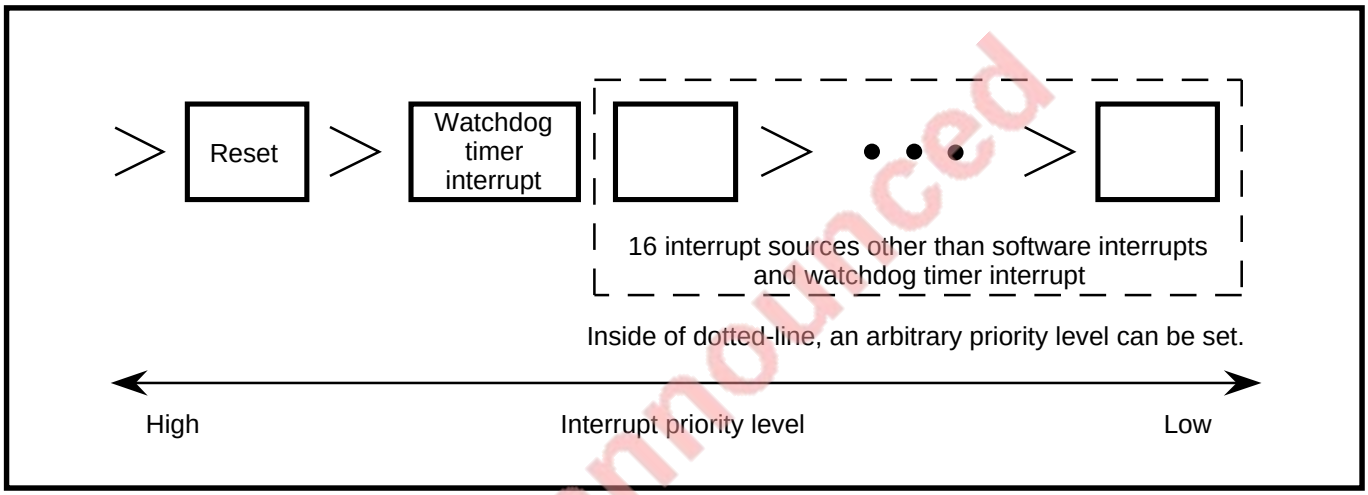
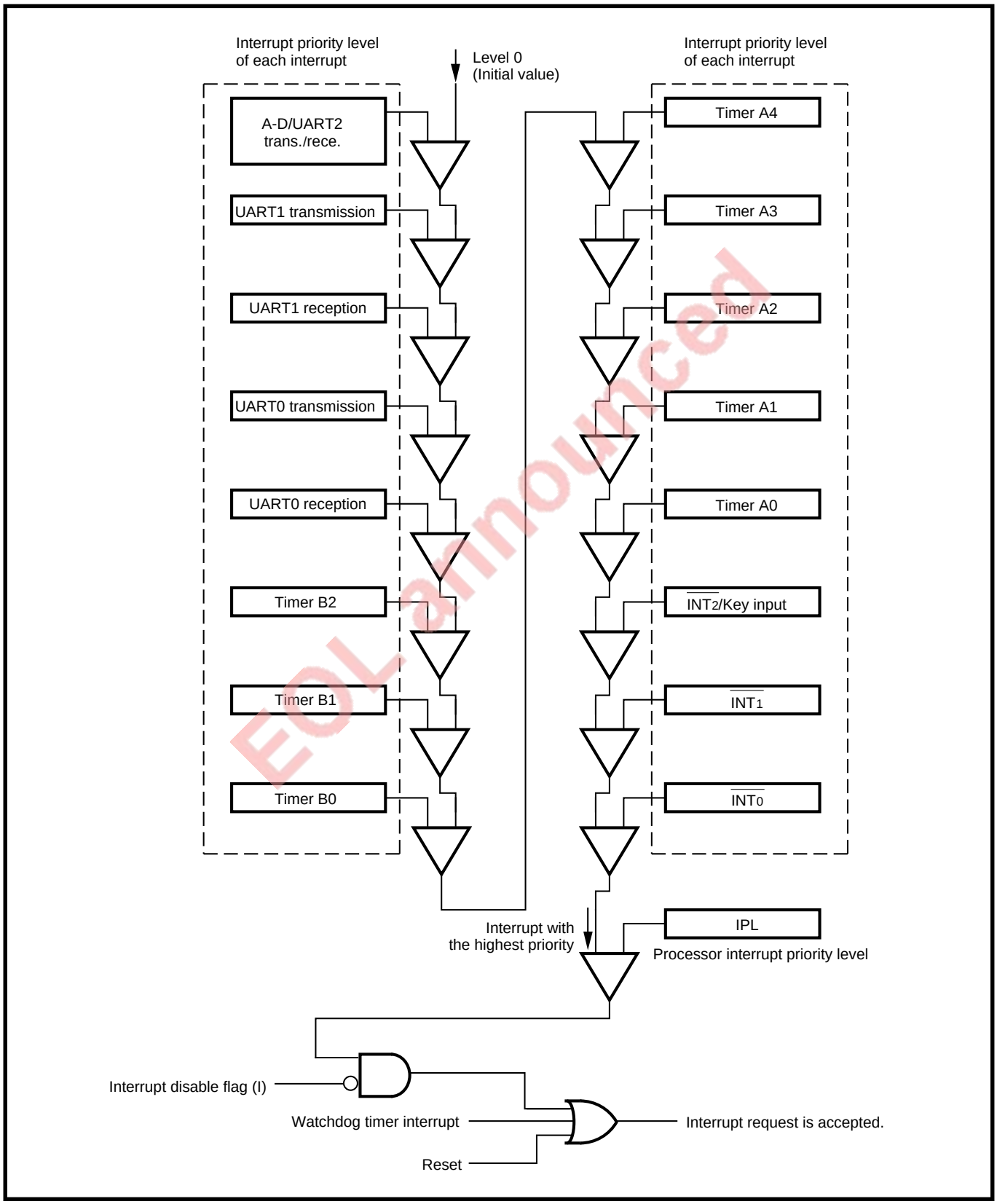


Fig. 4.4.1 Interrupt priority level set by hardware

EOL announced

4.5 Interrupt priority level detection circuit

The interrupt priority level detection circuit is used to select an interrupt with the highest priority from multiple interrupts which reside at the same sampling timing. Figure 4.5.1 shows the interrupt priority level detection circuit.



EOL announced

Fig. 4.5.1 Interrupt priority level detection circuit

INTERRUPTS

4.5 Interrupt priority level detection circuit

Figure 4.5.2 shows the operation of the interrupt priority detection circuit.
The interrupt priority level of a requested interrupt (“Y” in Figure 4.5.2) is compared with the priority level which is sent from the preceding comparator (“X” in Figure 4.5.2), and then the interrupt with the higher priority level is sent to the next comparator (“Z” in Figure 4.5.2). (Initial value of “X” is “0.”) For an interrupt which is not requested, the comparison is not performed and the priority level which is sent from the preceding comparator is forwarded to the next comparator as it is. After comparison, if the two priority levels are the same, the priority level which is sent from the preceding comparator is forwarded to the next comparator. Therefore, if the same priority is set by software, the interrupt priority levels are handled as follows:

A-D conversion > UART2 transmission/reception > UART1 transmission > UART1 reception > UART0 transmission > UART0 reception > Timer B2 > Timer B1 > Timer B0 > Timer A4 > Timer A3 > Timer A2 > Timer A1 > Timer A0 > $\overline{INT_2}$/Key input > $\overline{INT_1}$ > $\overline{INT_0}$

By the above comparison, among the multiple interrupt requests which reside at the same sampling timing, one request with the highest priority level is detected.

And then, the highest priority level detected by the above comparison is compared with the processor interrupt priority level (IPL). When this interrupt priority level is higher than the processor interrupt priority level (IPL) and the interrupt disable flag (I) = “0,” the corresponding interrupt request is accepted. An interrupt request which is not accepted at this time is held until it is accepted or the corresponding interrupt request bit is cleared to “0” by software (**CLB** instruction).
The interrupt priority level is detected synchronously with the CPU’s op-code fetch cycle. However, when an op-code fetch cycle starts during the interrupt priority detection, a new interrupt priority detection does not start. (Refer to **“Figure 4.6.1”**) Because the interrupt request bit’s state and interrupt priority level are latched during interrupt priority detection, if they change, the interrupt priority detection is performed for the previous state before the change occurred.

EOL announced

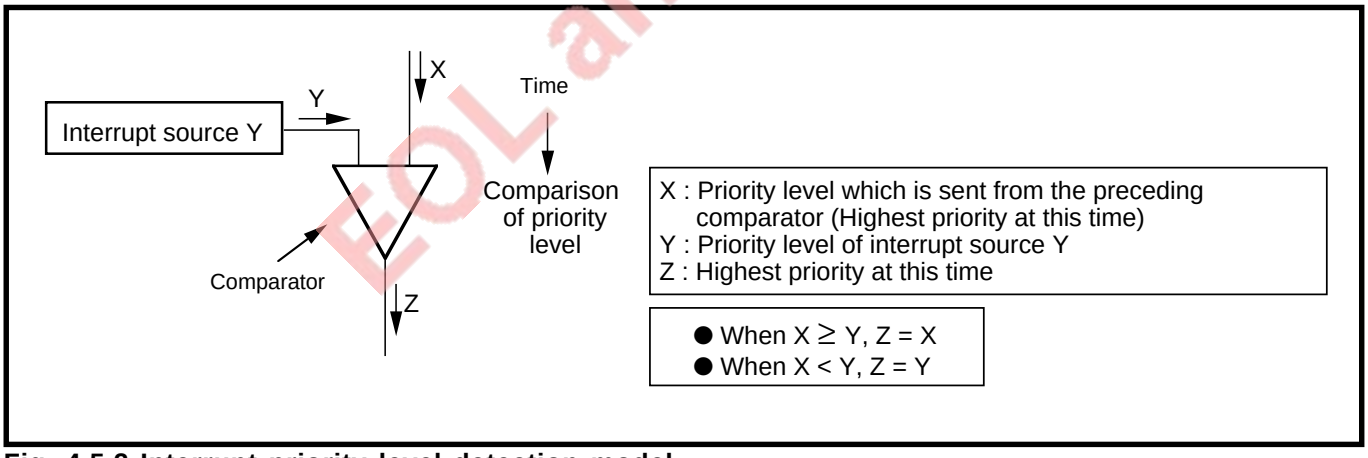
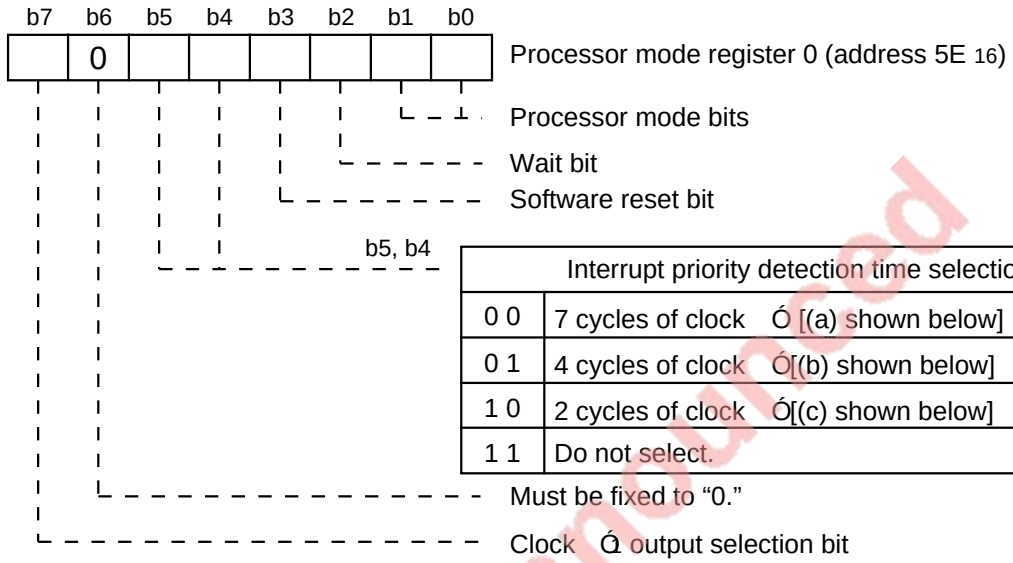


Fig. 4.5.2 Interrupt priority level detection model

4.6 Interrupt priority level detection time

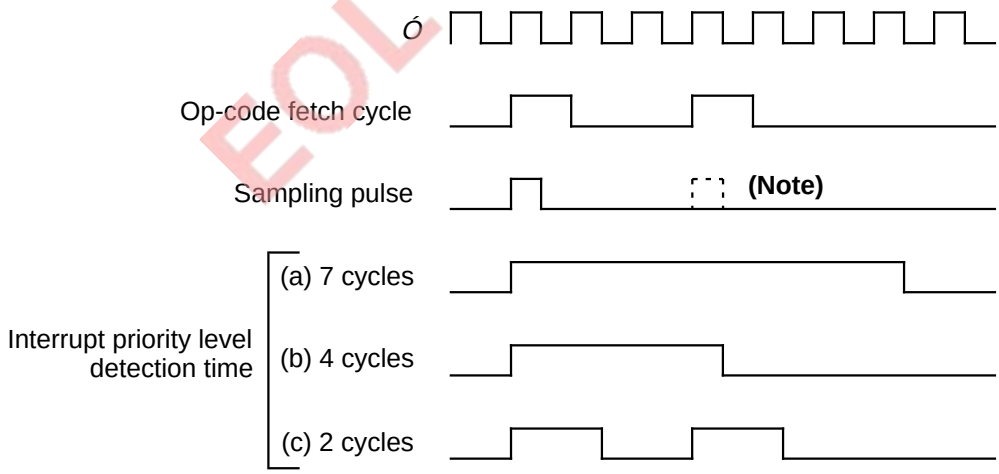
When the interrupt priority level detection time has passed after sampling starts, an interrupt request is accepted. The interrupt priority level detection time can be selected by software. Figure 4.6.1 shows the interrupt priority level detection time. Usually, select "2 cycles of ϕ" as the interrupt priority level detection time.

(1) Interrupt priority detection time selection bits



Interrupt priority detection time selection bits	
0 0	7 cycles of clock Ó [(a) shown below]
0 1	4 cycles of clock Ó[(b) shown below]
1 0	2 cycles of clock Ó[(c) shown below]
1 1	Do not select.

(2) Interrupt priority level detection time



Note: This pulse resides when "2 cycles of Ó" is selected.

Fig. 4.6.1 Interrupt priority level detection time

EOL announced

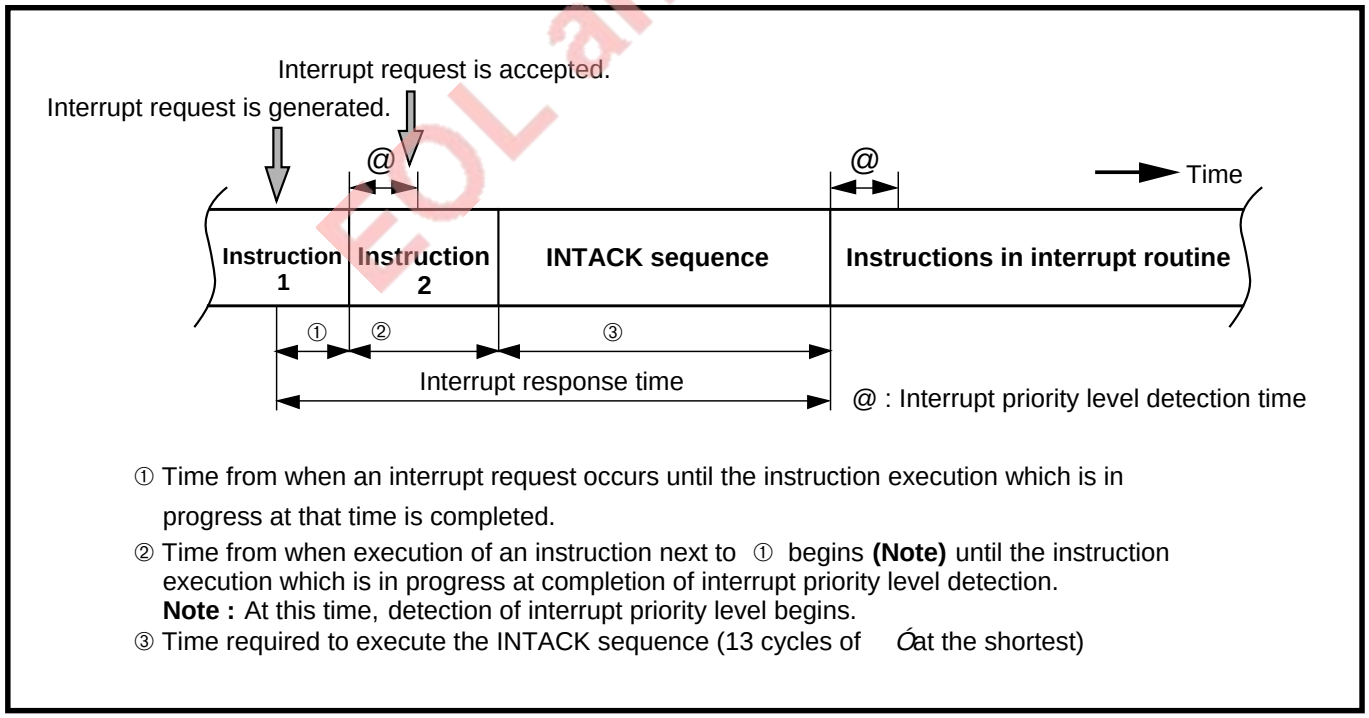
4.7 How interrupts are processed (from acceptance of interrupt request until execution of interrupt routine)

How interrupts are processed from accepting of an interrupt request until execution of the interrupt routine is described below.

When an interrupt request is accepted, the interrupt request bit which corresponds to the accepted interrupt is cleared to "0." And then, execution of an interrupt routine begins at the cycle immediately after the instruction execution which was in progress at acceptance of the interrupt request is completed. Figure 4.7.1 shows how interrupts are processed from acceptance of an interrupt request until execution of the interrupt routine. When the instruction execution which was in progress at acceptance of the interrupt request is completed, the INTACK (Interrupt acknowledge) sequence is executed and the program branches to the start address of the interrupt routine allocated in addresses 0_{16} to $FFFF_{16}$. In the INTACK sequence, the following procedure is automatically performed in this order.

①The contents of the program bank register (PG) immediately before the INTACK sequence is pushed onto the stack.
②The contents of the program counter (PC) immediately before the INTACK sequence is pushed onto the stack.
③The contents of the processor status register (PS) immediately before the INTACK sequence is pushed onto the stack.
④The interrupt disable flag (I) is set to "1."
⑤The interrupt priority level of the accepted interrupt is set to IPL.
⑥The contents of the program bank register (PG) is cleared to "00_{16}" and the contents of the interrupt vector address is set into the program counter (PC).

The INTACK sequence requires at least 13 cycles of ϕ. Figure 4.7.2 shows the INTACK sequence's timing. After the INTACK sequence is completed, the instruction execution begins at the start address of an interrupt routine.



① Time from when an interrupt request occurs until the instruction execution which is in progress at that time is completed.
② Time from when execution of an instruction next to ① begins **(Note)** until the instruction execution which is in progress at completion of interrupt priority level detection.
Note : At this time, detection of interrupt priority level begins.
③ Time required to execute the INTACK sequence (13 cycles of Ó at the shortest)

Fig. 4.7.1 How interrupts are processed from acceptance of interrupt request until execution of interrupt routine

EOL announced

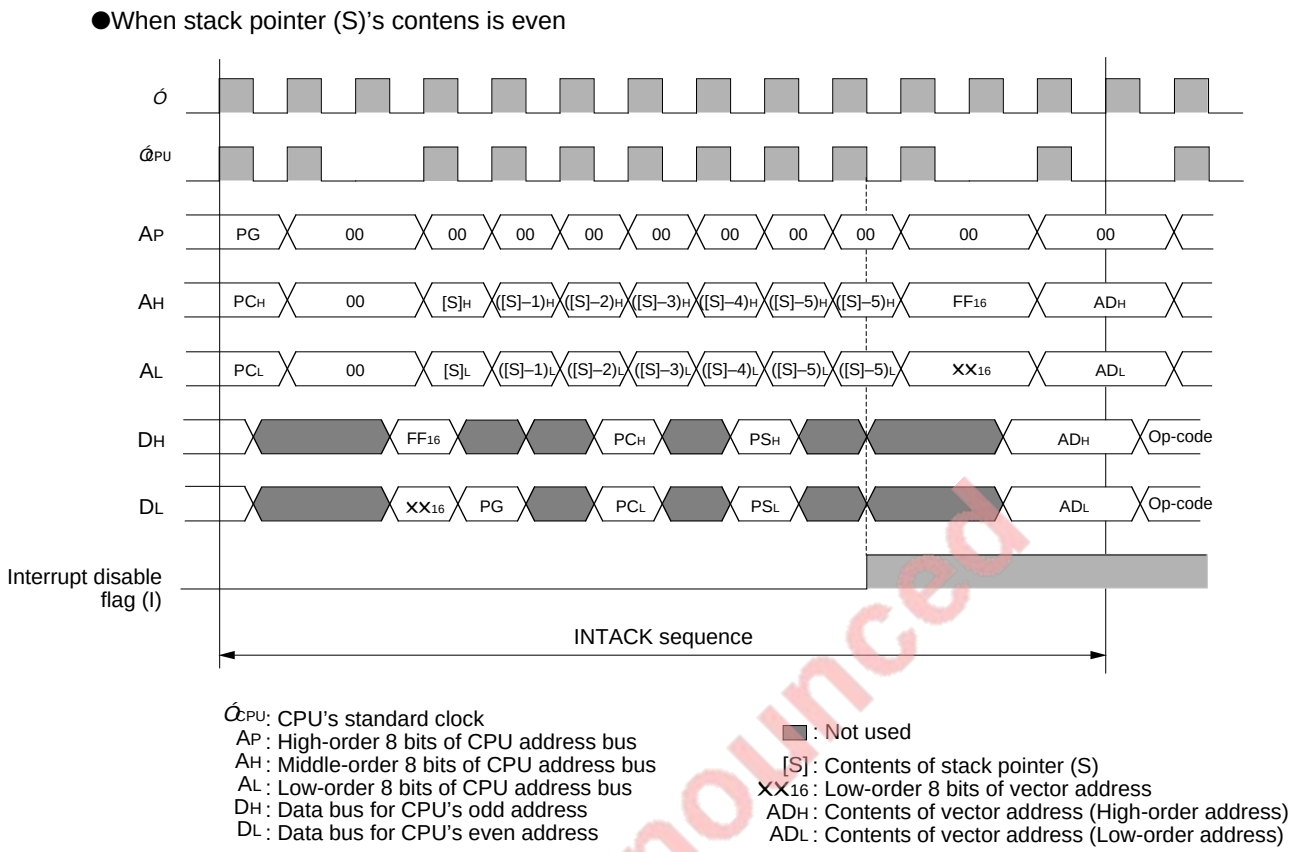


Fig. 4.7.2 INTACK sequence's timing

Not announced

4.7.1 Change in IPL at acceptance of interrupt request

When an interrupt request is accepted, the interrupt priority level of the accepted interrupt is set to the processor interrupt priority level (IPL). This operation makes the processing for multiple interrupts easy. (Refer to section **"4.9 Multiple interrupts."**

At reset or when a watchdog timer interrupt or software interrupt is accepted, a value listed in Table 4.7.1 is set into IPL.

Table 4.7.1 Change in IPL at acceptance of interrupt request

Interrupt source	Change in IPL
Reset	Level 0 (000_2) is set.
Watchdog timer interrupt	Level 7 (111_2) is set.
Zero division interrupt	Not changed
BRK instruction interrupt	Not changed
Other interrupts	Accepted interrupt's priority level is set.

INTERRUPTS

4.7 How interrupts are processed

4.7.2 How to push registers

The way to push registers depends on whether the stack pointer (S)'s contents at interrupt request acceptance is even or odd.

When the stack pointer (S)'s contents is even, each of the program counter (PC)'s contents and processor status register (PS)'s contents is simultaneously pushed by the 16 bits. When the stack pointer (S)'s contents is odd, each of these registers is pushed by the 8 bits. Figure 4.7.3 shows how the registers are pushed.

In the INTACK sequence, only the contents of the program bank register (PG), program counter (PC), and processor status register (PS) are pushed onto the stack area. Make sure to push other necessary registers by software at the beginning of an interrupt routine.

By executing the **PSH** instruction, all CPU registers other than the stack pointer can be pushed.

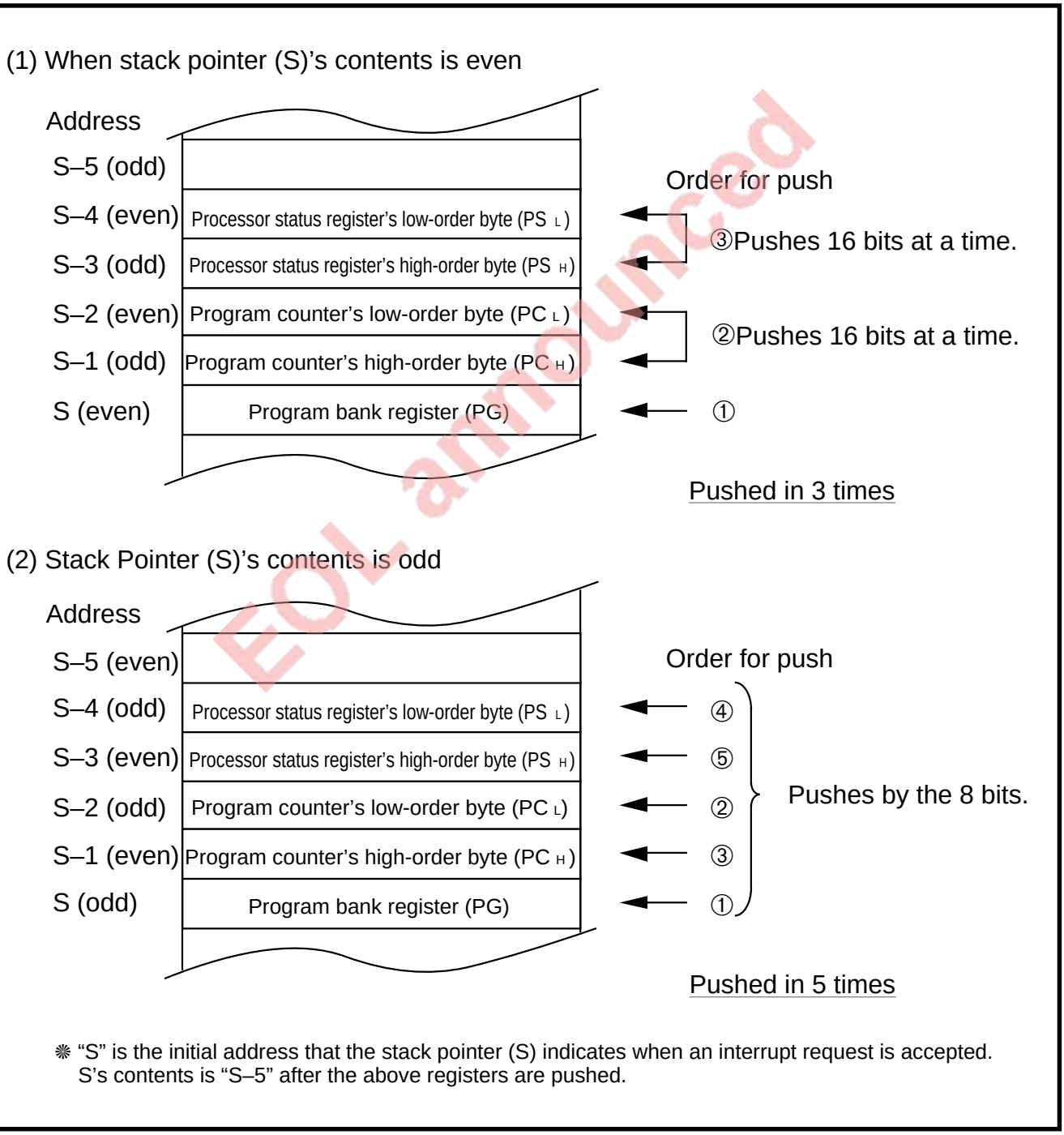


Fig. 4.7.3. How registers are pushed

EOL announced

4.8 Return from interrupt routine

When the **RTI** instruction is executed at the end of an interrupt routine, the contents of the program bank register (PG), program counter (PC), and processor status register (PS) which were pushed onto the stack area immediately before the INTACK sequence are automatically pulled. And then, a program returns to the original routine and the suspended process is resumed.
Before the **RTI** instruction is executed, by executing the **PUL** instruction or others, make sure to pull registers which were pushed by software in an interrupt routine. Make sure that the data length and register length for the pull operation are equal to those for the push operation.

4.9 Multiple interrupts

When a program branches to an interrupt routine, the following occurs:

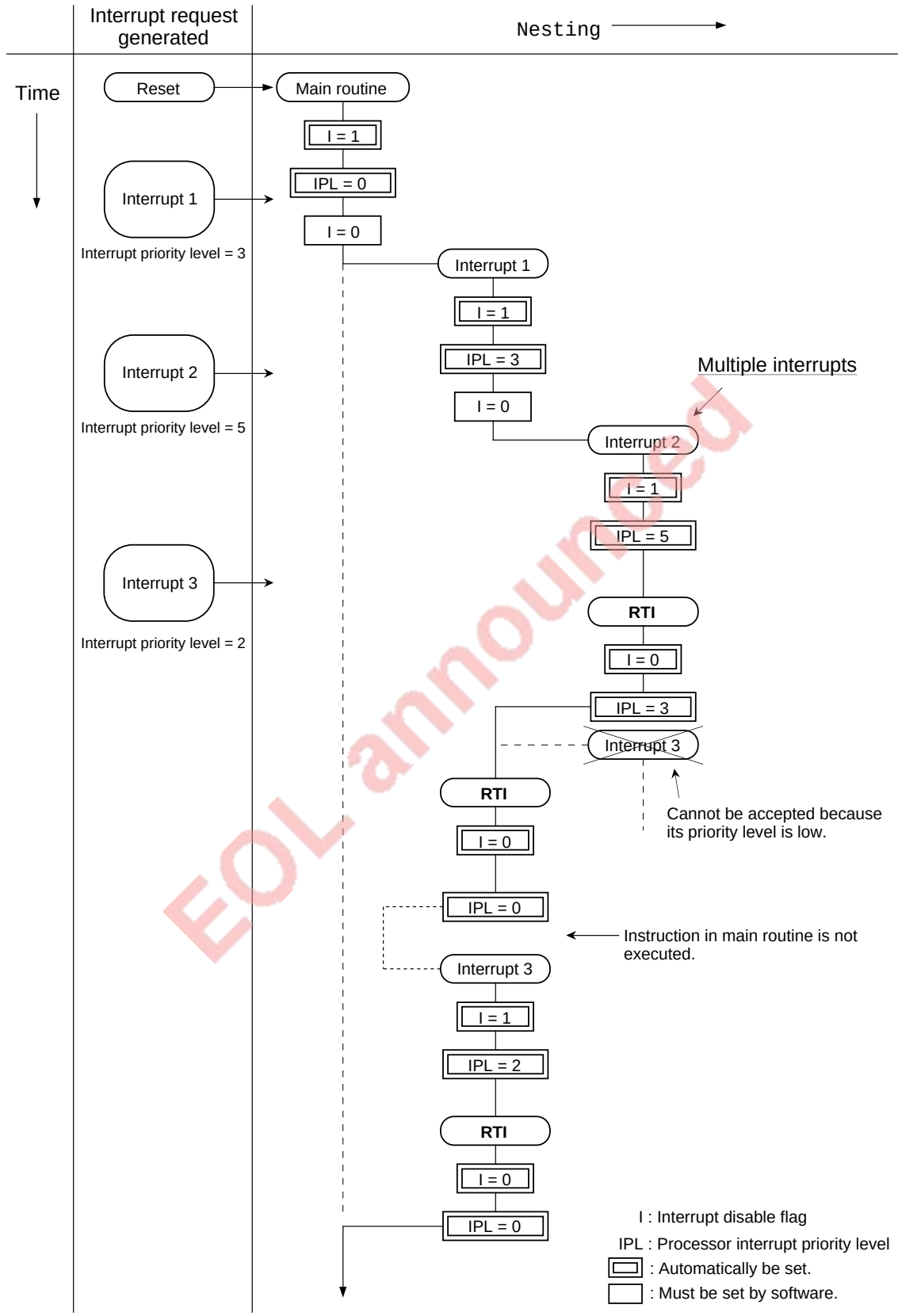
- Interrupt disable flag (I) = “1” (Interrupts are disabled.)
- Interrupt request bit of accepted interrupt = “0”
- Processor interrupt priority level (IPL) = Interrupt priority level of accepted interrupt

Therefore, as long as the IPL remains unchanged, by clearing the interrupt disable flag (I) to “0” in an interrupt routine, an interrupt request whose priority level is higher than the priority level of the interrupt which is in progress can be accepted. In this way, multiple interrupts are processed.
Figure 4.9.1 shows how multiple interrupts are processed.
An interrupt request which is not accepted because its priority level is lower is held. When the **RTI** instruction is executed, the interrupt priority level of the routine which was in progress at acceptance of an interrupt request is pulled to the IPL. Therefore, if the following relationship is satisfied when interrupt priority level detection is performed next, the held interrupt request is accepted.

Held interrupt request’s priority level > Processor interrupt priority level (IPL) which is pulled

EOL announced

4.9 Multiple interrupts



EOL announced

Fig. 4.9.1 How multiple interrupts are processed

4.10 External interrupts ($\overline{INT_i}$ interrupt)

An external interrupt request occurs by input signal from pin $\overline{INT_i}$ (i = 0 to 2). The occurrence condition of an external interrupt request can be selected by the level sense/edge sense selection bit and the polarity selection bit (bits 5 and 4 at addresses $7D_{16}$ to $7F_{16}$) shown in Figure 4.10.2. Table 4.10.1 lists the occurrence condition of $\overline{INT_i}$ interrupt request.

When using pins $P6_2/\overline{INT_0}$ to $P6_4/\overline{INT_2}$ as external interrupt input pins, set their corresponding bits at address 10_{16} (Port P6 direction register) to "0." (Refer to **"Figure 4.10.1."**) These pins can be pulled high by software. (Refer to section **"3.3 Pull-up function of $P6_2$ to $P6_4$ pins ($\overline{INT_0}$ to $\overline{INT_2}$)."**

The $\overline{INT_2}$ interrupt is invalid when the key input interrupt selection bit (bit 7 at address $6D_{16}$) = "1." (Refer to chapter **"5 KEY INPUT INTERRUPT FUNCTION."**) When using the $\overline{INT_2}$ interrupt function, clear the key input interrupt selection bit to "0."

A signal which is input to pin $\overline{INT_i}$ requires a "H"/"L"-level duration of 250 ns or more independent of the system clock frequency **(Note 1)**.

Note that even when pins $P6_2/\overline{INT_0}$ to $P6_4/\overline{INT_2}$ are used as external interrupt input pins, these pins' state can be read in by reading bits 2 to 4 at address E_{16} (Port P6 register).

Note 1: When the falling edge or "L" level is selected as the interrupt occurrence condition, make sure that "L"-level duration must be at least 250 ns: when the rising edge or "H" level is selected as the interrupt occurrence condition, make sure that "H"-level duration must be at least 250 ns.

Table 4.10.1 Occurrence condition of $\overline{INT_i}$ interrupt request

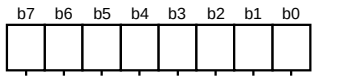
b5 **(Note 2)**	b4 **(Note 2)**	$\overline{INT_i}$ interrupt request occurrence condition
0	0	Occurs at the falling edge of an input signal to pin $\overline{INT_i}$ (Edge sense).
0	1	Occurs at the rising edge of an input signal to pin $\overline{INT_i}$ (Edge sense).
1	0	Occurs when pin $\overline{INT_i}$ is at "H" level (Level sense).
1	1	Occurs when pin $\overline{INT_i}$ is at "L" level (Level sense).

Note 2: "b5" and "b4" represent bits 5 and 4 of the $\overline{INT_0}$ to $\overline{INT_2}$/key input interrupt control register. (Refer to **"Figure 4.10.2."**)
In an $\overline{INT_i}$ interrupt, pin $\overline{INT_i}$'s state is always checked, and then an interrupt request is generated according to the state. Therefore, when an $\overline{INT_i}$ interrupt is not used, clear the $\overline{INT_i}$ interrupt's priority level to "0."

EOL announced

INTERRUPTS

4.10 External interrupts ($\overline{INTi}$ interrupt)



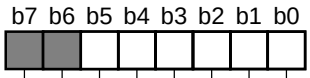
Port P6 direction register (address 10_{16})

Bit	Corresponding pin's name	Functions	At reset	RW
0	Pin TA4OUT	0 : Input mode 1 : Output mode When using a pin as an input pin for an external interrupt, clear the corresponding bit to "0."	0	RW
1	Pin TA4IN		0	RW
2	Pin $\overline{INT_0}$		0	RW
3	Pin $\overline{INT_1}$		0	RW
4	Pin $\overline{INT_2}$/Key input		0	RW
5	Pin TB0IN		0	RW
6	Pin TB1IN		0	RW
7	Pin TB2IN		0	RW

□ represents that bits 0, 1 and bits 5 to 7 are not used for external interrupts.

Fig. 4.10.1 Correspondence between port P6 direction register and input pins for external interrupts

EOL announced



$\overline{INT_0}$, $\overline{INT_1}$, and $\overline{INT_2}$/Key input interrupt control registers (addresses $7D_{16}$ to $7F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2b1b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit **(Note)**	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
4	polarity selection bit	0: Interrupt request bit is set to "1" at "H" level when level sense is selected; this bit is set to "1" at falling edge when edge sense is selected. 1: Interrupt request bit is set to "1" at "L" level when level sense is selected; this bit is set to "1" at rising edge when level sense is selected.	0	RW
5	Level sense/Edge sense selection bit	0: Edge sense 1: Level sense	0	RW
6	Not implemented.		Un-defined	—
7				

Note: The interrupt request bits of $\overline{INT_0}$ to $\overline{INT_2}$/Key input interrupts are ignored when the level sense is selected.

Fig. 4.10.2 $\overline{INT_0}$ to $\overline{INT_2}$ interrupt control register's structure

4.10.1 $\overline{INTi}$ interrupt request bit's function

(1) Functions when edge sense is selected

By clearing the level sense/edge sense selection bit to "0," the edge sense is selected. (Refer to **Figure 4.10.3.**)

The interrupt request bit has the same functions as those for the interrupt request bit of internal interrupts.

When an interrupt occurs, the interrupt request bit is set to "1" and retains this state until the interrupt request is accepted.

When the interrupt request bit is cleared to "0" by software, an interrupt request is cancelled; when the interrupt request bit is set to "1" by software, an interrupt request can be generated.

(2) Functions when level sense is selected

By setting the level sense/edge sense selection bit to "1," the level sense is selected. (Refer to **Figure 4.10.3.**)

The interrupt request bit is ignored. In this case, interrupt requests occur sequentially while pin $\overline{INTi}$ is at the valid level*1; when pin $\overline{INTi}$'s level changes to the invalid level*2 with the interrupt request not accepted, the interrupt request is not held. (Refer to **Figure 4.10.4.**)

Valid level*1: The level selected by the polarity selection bit (bit 4 at addresses 7D16 to 7F16)
Invalid level*2: The reverse level to "valid level"

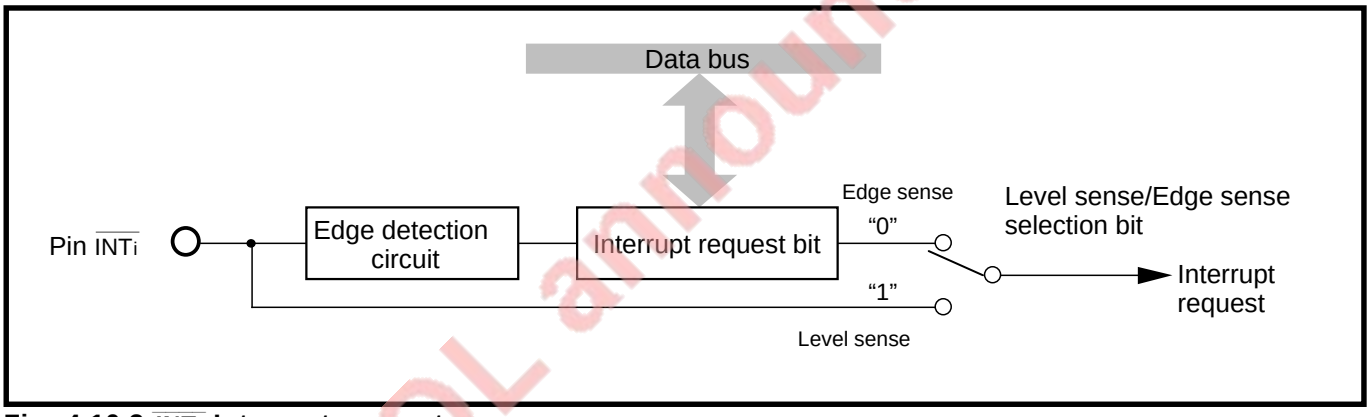


Fig. 4.10.3 $\overline{INTi}$ Interrupt request

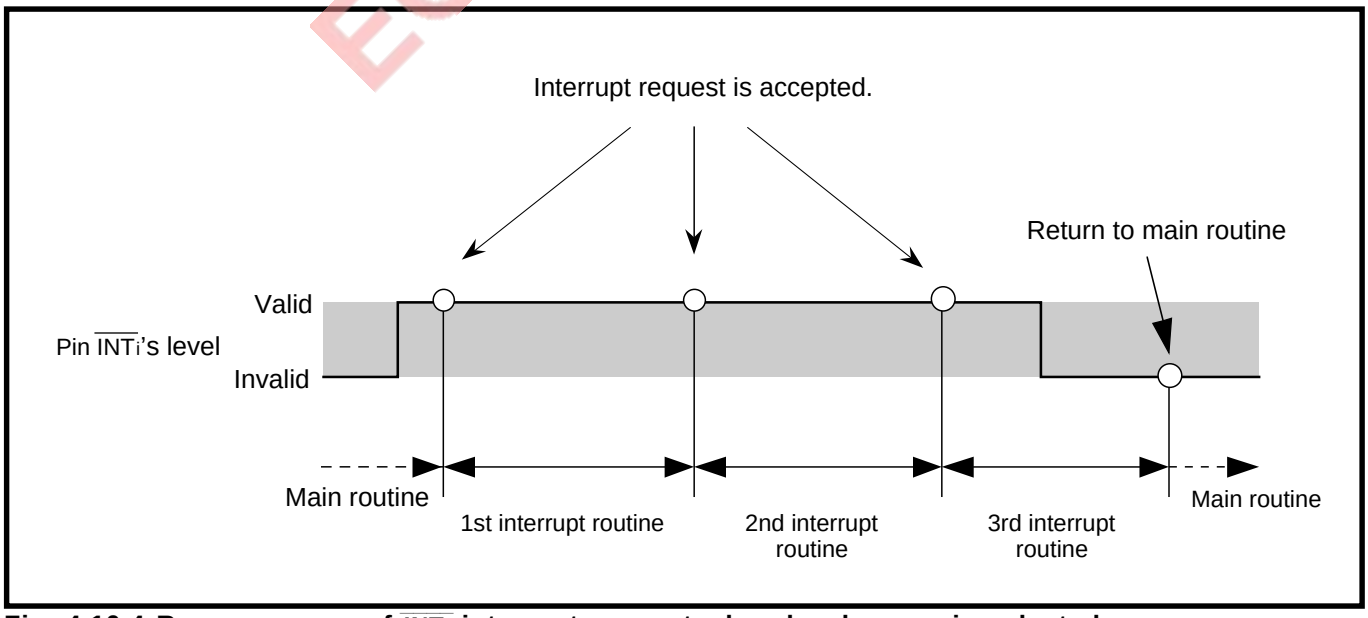


Fig. 4.10.4 Re-occurrence of $\overline{INTi}$ interrupt request when level sense is selected

EOL announced

4.10 External interrupts ($\overline{\text{INTi}}$ interrupt)

4.10.2 How to switch $\overline{\text{INTi}}$ interrupt request occurrence condition

The way to switch the $\overline{\text{INTi}}$ interrupt request occurrence condition from the level sense to the edge sense is shown in Figure 4.10.5 (1).
The way to switch the polarity is shown in Figure 4.10.5 (2).

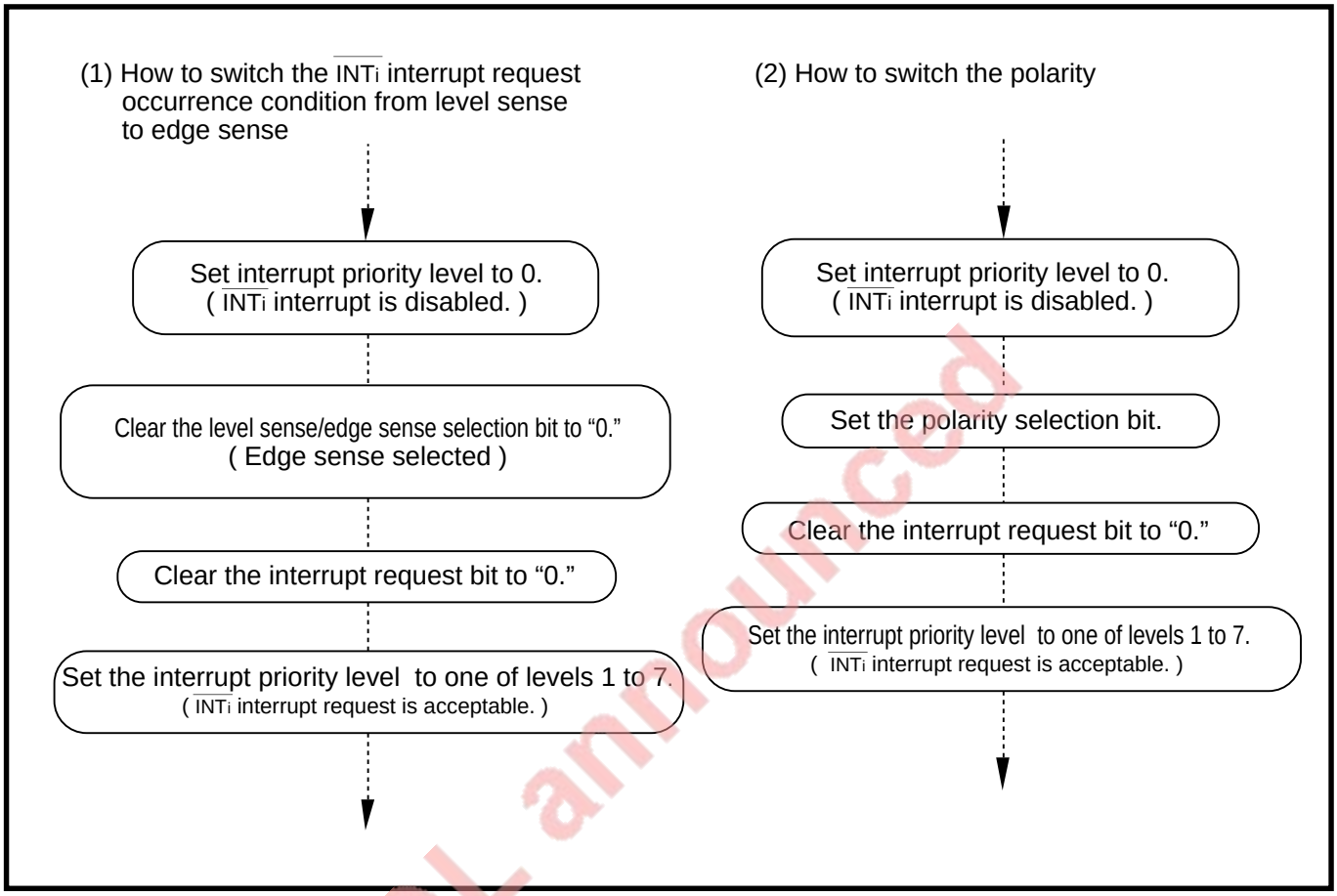


Fig. 4.10.5 How to switch $\overline{\text{INTi}}$ interrupt request occurrence condition

EOL announced

4.11 Precautions for interrupts

When the contents of the interrupt priority level selection bits (bits 0 to 2 at addresses 70_{16} to $7F_{16}$) is changed, 2 to 7 cycles of ϕ are required. Therefore, when the interrupt priority level of the same interrupt source is changed twice or more in a very short time, which consists of a few instructions, it is necessary to secure the required time by software. Figure 4.11.1 shows an program example to secure the time required for the change of an interrupt priority level. Note that the time required for the change depends on the contents of the interrupt priority level selection bits (bits 4 and 5 at address $5E_{16}$). Table 4.11.1 lists the correspondence between the number of instructions inserted in a program example and the interrupt priority level selection bits. (Refer to **Figure 4.11.1,** also.)

```
:
LDM .B #0XH, 007XH ; The write instruction for the interrupt priority level selection bits
NOP                ; The NOP instruction is inserted (Note)
NOP                ;
NOP                ;
LDM .B #0XH, 007XH ; The write instruction for the interrupt priority level selection bits
```

Note: Other instructions whose cycle number corresponds to that of the **NOP** instruction (other than the write instructions for address $7X_{16}$) can be inserted.
For number of the **NOP** instructions which are to be inserted, refer to **Table 4.11.1.**

Fig. 4.11.1 Program example to secure time required for change of interrupt priority level

Table 4.11.1 Correspondence between number of instructions to be inserted in Figure 4.11.1 and interrupt priority detection time selection bits

Interrupt priority detection time selection bits (**Note**)		Time required for change of interrupt priority level	Number of inserted **NOP** instruction
b5	b4		
0	0	7 cycles of ϕ	4 or more
0	1	4 cycles of ϕ	2 or more
1	0	2 cycles of ϕ	1 or more
1	1	Do not select.	

Set as follows, if possible:
[b5 = “1,” b4 = “0”]

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CHAPTER 5

KEY INPUT INTERRUPT FUNCTION

EOL announced

5.1 Overview
5.2 Block description
5.3 Initial setting example for related registers

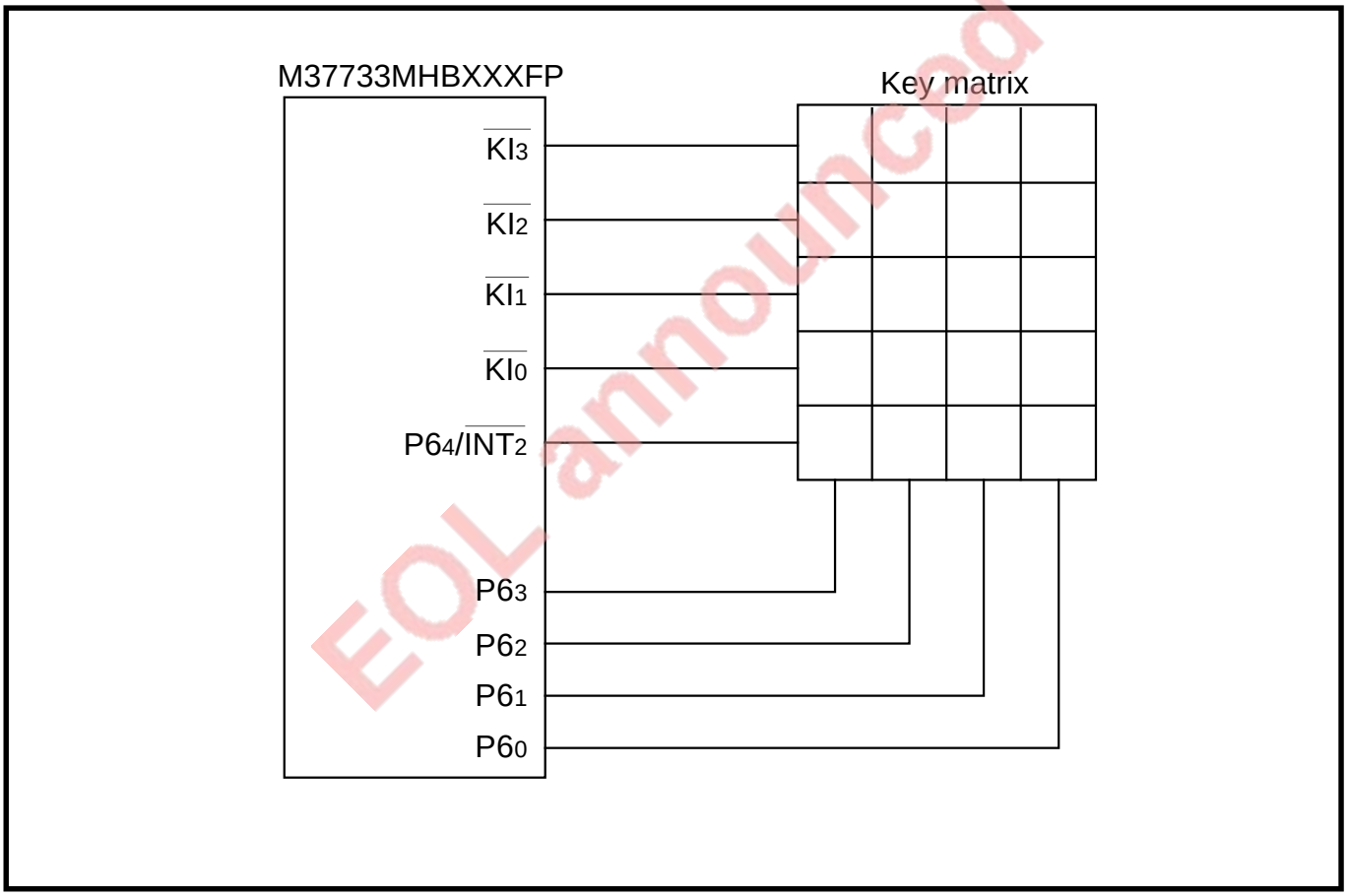
KEY INPUT INTERRUPT FUNCTION

5.1 Overview

The key input interrupt function is used to generate an interrupt request when one of the input levels of four or five pins falls. By using this function when terminating the stop or wait mode, the key-on wakeup can be realized.
For the way to terminate the stop or wait mode, refer to section **"17.4 Power saving."**
For the stop and wait modes, refer to chapter **"11. STOP AND WAIT MODES."**

5.1 Overview

A key input interrupt request occurs when one of the input levels of pins $\overline{KI_0}$ to $\overline{KI_3}$ falls. Therefore, by configuring an external key matrix shown in Figure 5.1.1, an interrupt request can be generated only by pushing a key. Pins $\overline{KI_0}$ to $\overline{KI_3}$ can be pulled high by software and the same function can also be selected for port $P6_4$. Therefore, when using the key input interrupt function, whether to use four pins (pins $\overline{KI_0}$ to $\overline{KI_3}$) or five pins (pins $\overline{KI_0}$ to $\overline{KI_3}$ and $P6_4$) can be selected.
The key input interrupt and the $\overline{INT_2}$ interrupt share the same interrupt vector addresses and interrupt control register.



EOL announced

Fig. 5.1.1 Key matrix example when key input interrupt function is used

5.2 Block description

Figure 5.2.1 shows the block diagram for the key input interrupt function.

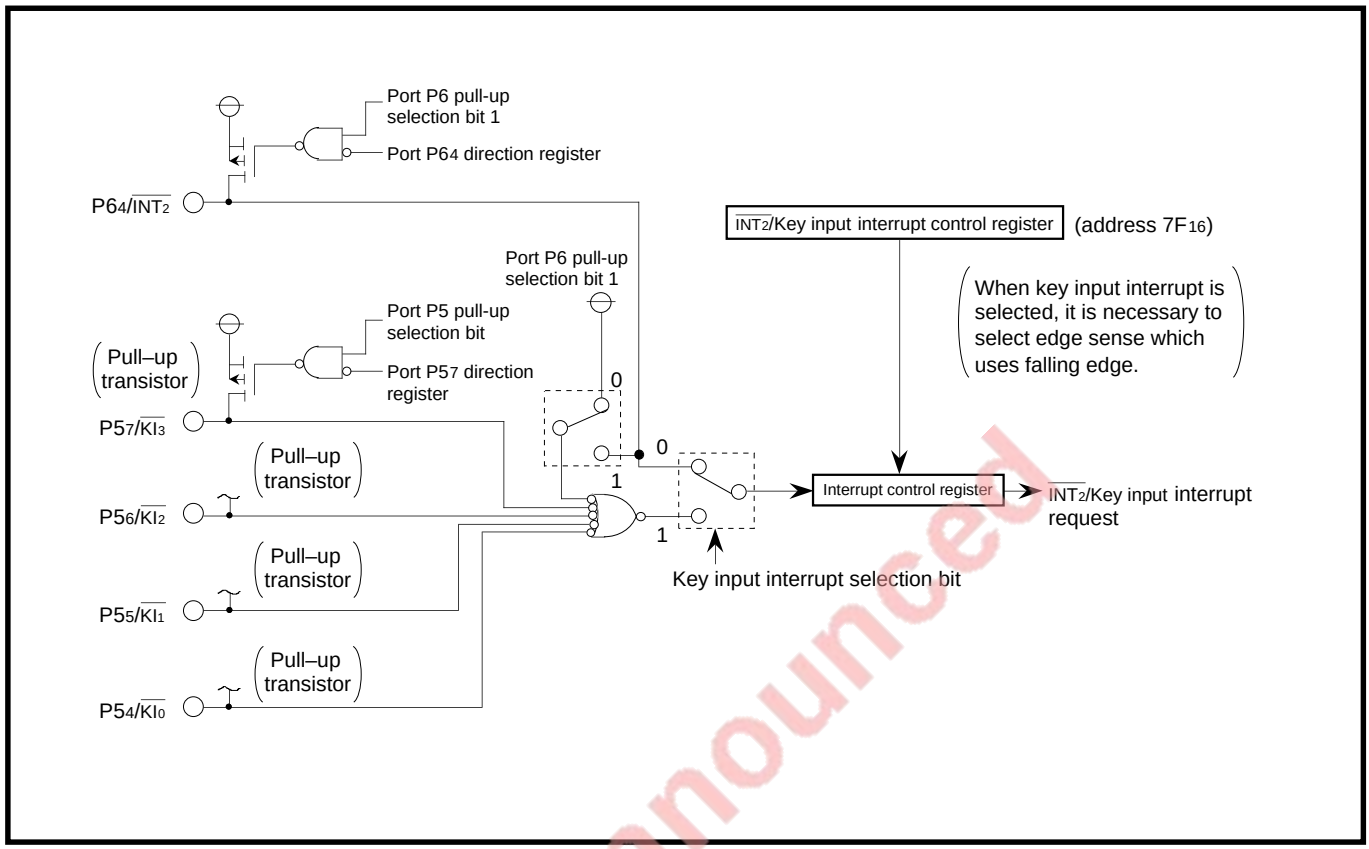


Fig. 5.2.1 Block diagram for key input interrupt function

5.2.1 Pins $\overline{KI_0}$ to $\overline{KI_3}$ and P64/$\overline{INT_2}$

When the key input interrupt function is selected, pins P54 to P57 become input pins for the key input interrupt ($\overline{KI_0}$ to $\overline{KI_3}$).

When selecting the key input interrupt function, clear all of bits 4 to 7 at address D16 (Port P5 direction register) to "0."

When bits 4 to 7 at address B16 (Port P5 register) are read out, the status of pins $\overline{KI_0}$ to $\overline{KI_3}$ can be read in. When using pin P64/$\overline{INT_2}$ as an input pin for the key input interrupt, set both of bits 5 and 7 at address 6D16 to "1" and bit 4 at address 1016 (Port P6 direction register) to "0." When bit 4 at address E616 (Port P6 register) is read out, the status of pin P64/$\overline{INT_2}$ can be read in.

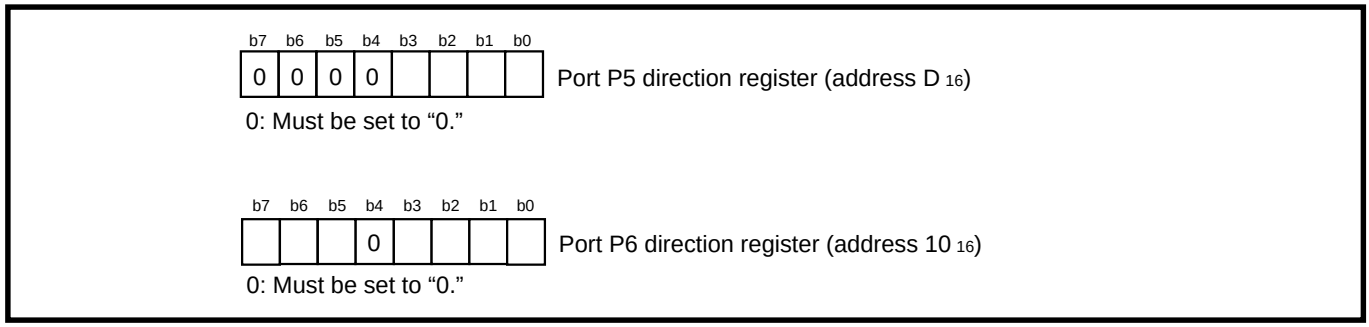


Fig. 5.2.2 Port P5 and P6 direction registers when key input interrupt function is selected

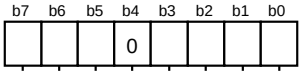
EOL announced

KEY INPUT INTERRUPT FUNCTION

5.2 Block description

5.2.2 Port function control register

Figure 5.2.3 shows the structure of the port function control register.



Port function control register (address 6D 16)

Bit	Bit name	Functions	At reset	RW
0	Standby state selection bit	0: Pins P0 to P3 are used for the external bus output. 1: Pins P0 to P3 are used for the port output.	0	RW
1	Sub-clock output selection bit/ Timer B2 clock source selection bit	•Port-Xc selection bit* = "0" (when the sub clock is not used) Timer B2 (event counter mode) clock source selection **(Note 1)** 0: TB2IN input (event counter mode) 1: Main clock divided by 32 (clock timer) •Port-Xc selection bit = "1" (when the sub clock is used) Sub-clock output selection 0: Pin P67/TB2IN/ f SUB functions as a programmable I/O port. 1: Sub clock f SUB is output from pin P67/TB2IN/f SUB	0	RW
2	Timer B1 internal connect selection bit **(Note 2)**	0: No internal connection 1: Internal connection with timer B2	0	RW
3	Port P6 pull-up selection bit 0	0: No pull-up for pins P62/$\overline{INT_0}$ and P63/$\overline{INT_1}$ 1: With pull-up for pins P62/$\overline{INT_0}$ and P63/$\overline{INT_1}$	0	RW
4	Must be fixed to "0."		0	RW
5	Port P6 pull-up selection bit 1	•Key input interrupt selection bit = "0" 0: No pull-up for pin P64/$\overline{INT_2}$ 1: With pull-up for pin P64/$\overline{INT_2}$ •Key input interrupt selection bit = "1" 0: Pin P64/$\overline{INT_2}$ is a port with no pull-up. 1: Pin P64/$\overline{INT_2}$ is an input pin with pull-up and is used for the key input interrupt.	0	RW
6	Port P5 pull-up selection bit	0: No pull-up for pins P54/TA2OUT/$\overline{KI_0}$ to P57/TA3IN/$\overline{KI_3}$ 1: With pull-up for pins P54/TA2OUT/$\overline{KI_0}$ to P57/TA3IN/$\overline{KI_3}$	0	RW
7	Key input interrupt selection bit	0: $\overline{INT_2}$ interrupt 1: Key input interrupt	0	RW

Port-Xc selection bit* : Bit 4 of the oscillation circuit control register 0 (address 6C 16)

Notes 1: When the port-Xc selection bit = "0" and timer B2 operates in the timer mode or the pulse period /pulse width measurement mode, bit 1 is invalid.
2: When timer B1 operates in the event counter mode, bit 2 is valid.
3: ☐ represents that bits 0 to 4 are not used for the key input interrupt function.

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Fig. 5.2.3 Structure of port function control register

(1) Port P6 pull-up selection bit (bit 5)

When using pin P64/$\overline{INT_2}$ as an input pin for the key input interrupt, set this bit to "1." When this bit is set to "1," pin P64/$\overline{INT_2}$ is pulled high.

(2) Port P5 pull-up selection bit (bit 6)

This is a bit to pull pins $\overline{KI_0}$ to $\overline{KI_3}$ high. When configuring a key matrix, there is no need to connect pull-up transistors externally if this bit is set to "1," in other words, if pins $\overline{KI_0}$ to $\overline{KI_3}$ are set to be pulled high.

(3) Key input interrupt selection bit (bit 7)

This is a bit to select the key input interrupt function.

The key input interrupt and the $\overline{INT_2}$ interrupt share the same interrupt vector addresses and interrupt control register. When this bit is set to "1," the key input interrupt function is selected. When this bit = "1" and bit 5 (Port P6 pull-up selection bit) = "0," pin P64/$\overline{INT_2}$ is a programmable I/O port. (At this time, the $\overline{INT_2}$ interrupt cannot be used.) When both of this bit and bit 5 (Port P6 pull-up selection bit 1) are "1," pin P64/$\overline{INT_2}$ can be used for the key input interrupt.

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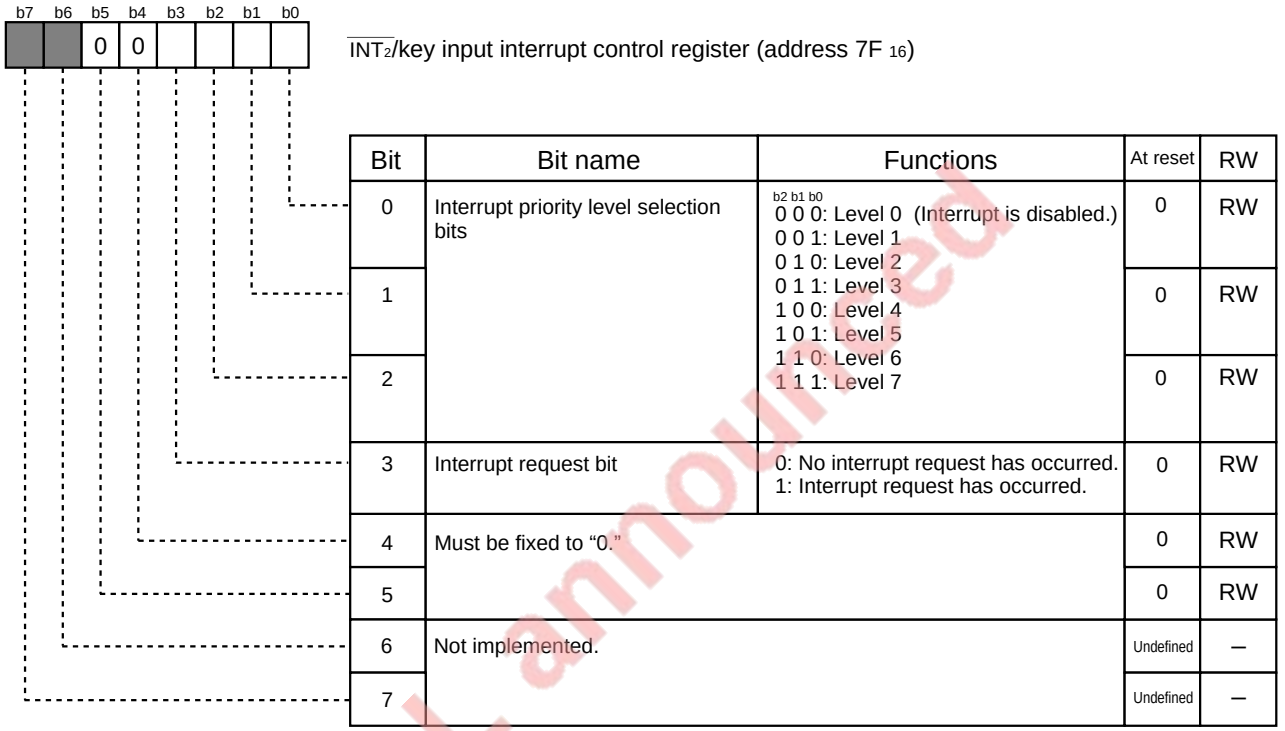
KEY INPUT INTERRUPT FUNCTION

5.2 Block description

5.2.3 Interrupt function

The key input interrupt and the $\overline{INT_2}$ interrupt share the same interrupt vector addresses and interrupt control register. Specify addresses FFF0$_{16}$ and FFF1$_{16}$ (in other words, the vector addresses for the $\overline{INT_2}$/key input interrupt) as the interrupt vector addresses; specify the $\overline{INT_2}$/key input interrupt control register (address 7F$_{16}$) as the interrupt control register. Figure 5.2.4 shows the structure of the $\overline{INT_2}$/key input interrupt control register when the key input interrupt function is selected.

The operation at accepting a key input interrupt request is the same as that at accepting an $\overline{INT_2}$ interrupt request.



Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2 b1 b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
4	Must be fixed to “0.”		0	RW
5			0	RW
6	Not implemented.		Undefined	—
7			Undefined	—

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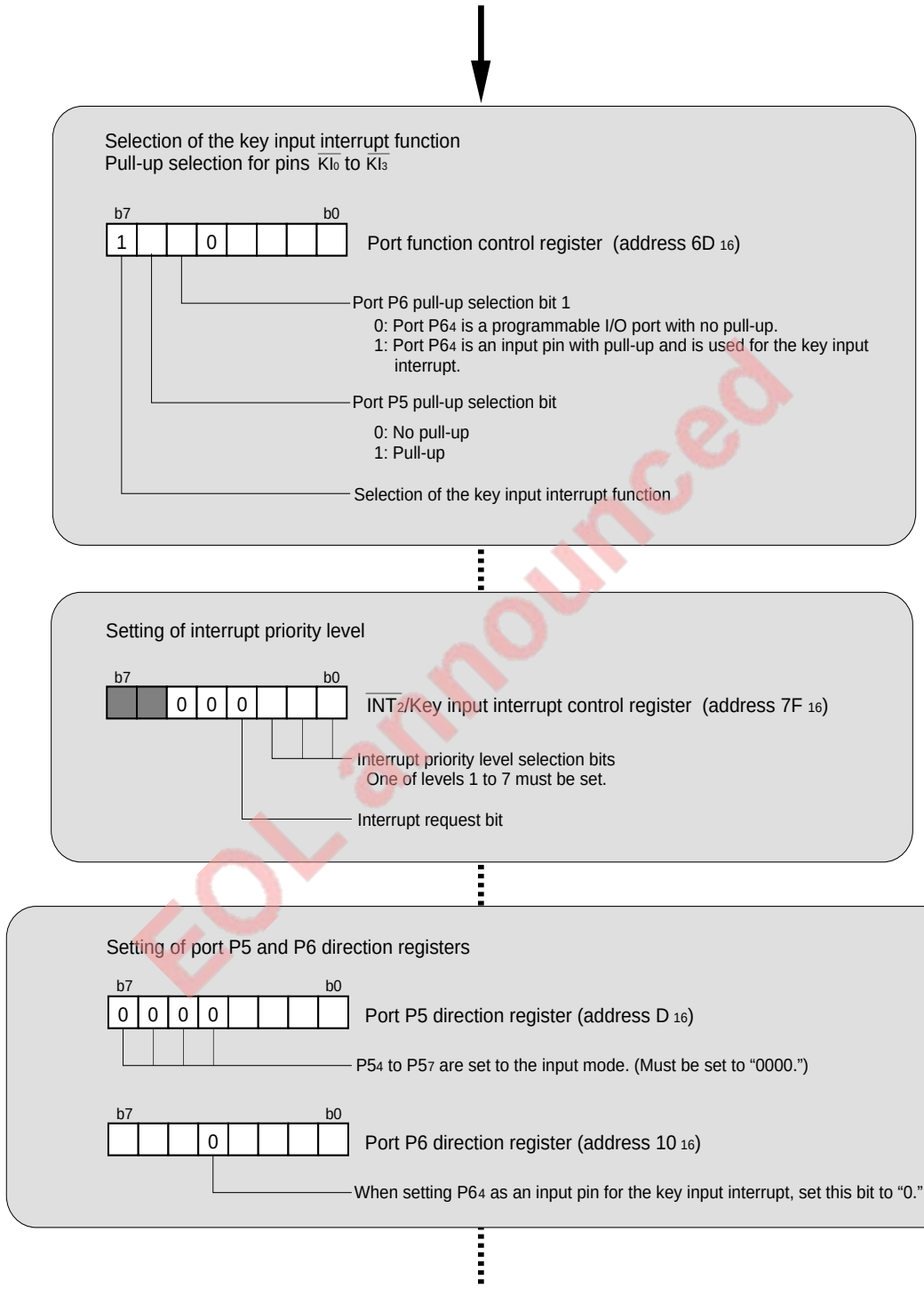
Fig. 5.2.4 Structure of $\overline{INT_2}$/key input interrupt control register when key input interrupt function is selected

5.3 Initial setting example for related registers

Figure 5.3.1 shows an initial setting example for registers related to the key input interrupt function.



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❋ In order to enable the key input interrupt, the interrupt disable flag (I) must be set to "0" and the processor interrupt priority level (IPL) must be a value smaller than the INT2/key input interrupt's priority level. (Refer to chapter **"4. INTERRUPTS."**)

Fig. 5.3.1 Initial setting example for registers related to key input interrupt function

5.3 Initial setting example for related registers

MEMO

EOL announced

CHAPTER 6

TIMER A

6.1 Overview
6.2 Block description
6.3 Timer mode
6.4 Event counter mode
6.5 One-shot pulse mode
6.6 Pulse width modulation (PWM) mode

EOL announced

TIMER A

6.1 Overview

Timer A is used mainly for output to the external. It consists of five counters (Timers A0 to A4), and each has a 16-bit reload function. Timers A0 to A4 operate independently of each other.
Timer Ai (i = 0 to 4) has four operating modes listed below. Except for the event counter mode, timers A0 to A4 all have the same functions.

■ Timer mode
Timer A counts a count source internally generated, and the following functions can be used:
- Gate function
- Pulse output function

■ Event counter mode
Timer A counts an external signal, and the following functions can be used:
- Free-run count function (Timers A2, A3, and A4)
- Pulse output function
- Two-phase pulse signal processing function (Timers A2, A3, and A4)

■ One-shot pulse mode
Timer A outputs a pulse which has an arbitrary width once.

■ Pulse width modulation (PWM) mode
Timer A outputs pulses which have an arbitrary width in succession and functions as one of the following pulse width modulators:
- 16-bit pulse width modulator
- 8-bit pulse width modulator

EOL announced

6.2 Block description

Figure 6.2.1 shows the timer A block diagram. Registers related to timer A are described below.

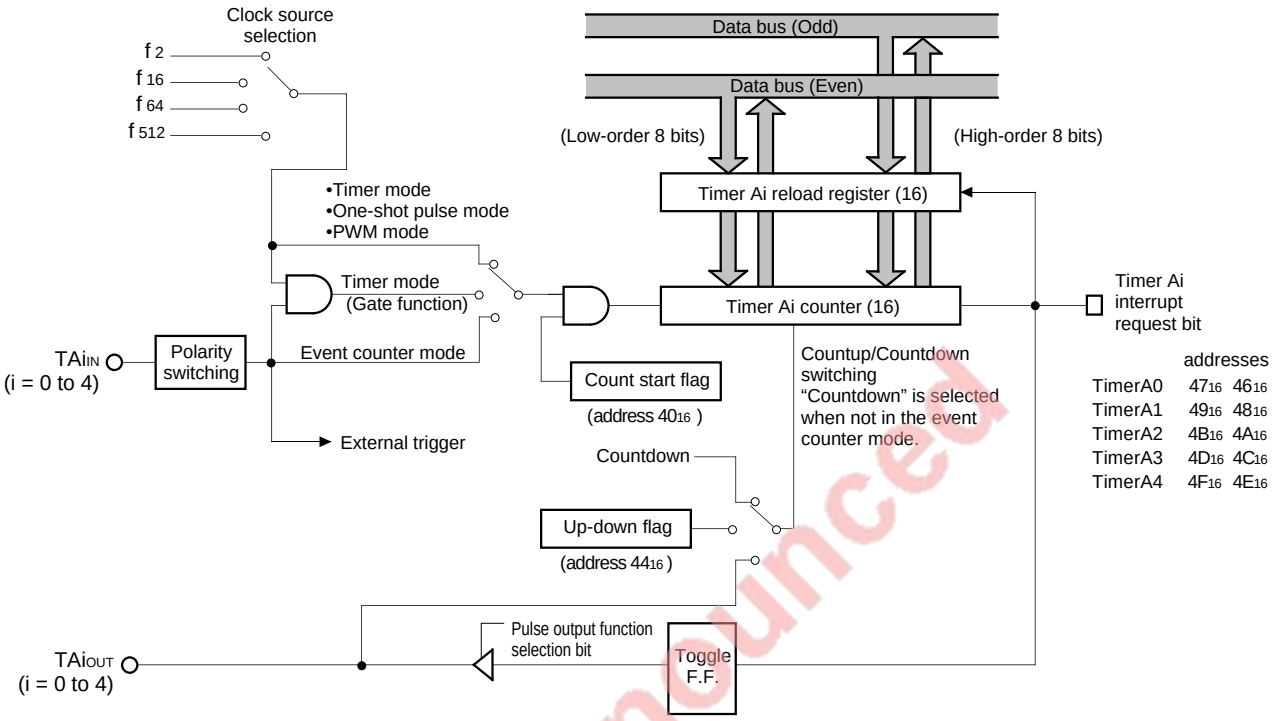


Fig. 6.2.1 Timer A block diagram

EOL announced

TIMER A

6.2 Block description

6.2.1 Counter and reload register (Timer Ai register)

Each of timer Ai counter and its reload register consists of 16 bits.

The counter performs countdown each time a count source is input. In the event counter mode, it can also function as an up-counter.

The reload register is used to memorize the initial value of a counter. When an underflow/overflow occurs in the counter, the reload register's contents is reloaded into the counter. However, when the free-run count function is used, the reload register's contents is not reloaded into the counter.

Values are set to the counter and reload register by writing the values to the timer Ai register. Table 6.2.1 lists the memory allocation of the timer Ai register.

A value written into the timer Ai register while counting is stopped is set to the counter and reload register. A value written into the timer Ai register while counting is in progress is set only to the reload register. In this case, the reload register's updated contents is transferred to the counter at the next reload time. A value obtained by reading out the timer Ai register depends on the operating mode. Table 6.2.2 lists reading and writing from and to the timer Ai register.

Table 6.2.1 Memory allocation of timer Ai register

Timer Ai register	High-order byte	Low-order byte
Timer A0 register	Address 47_{16}	Address 46_{16}
Timer A1 register	Address 49_{16}	Address 48_{16}
Timer A2 register	Address $4B_{16}$	Address $4A_{16}$
Timer A3 register	Address $4D_{16}$	Address $4C_{16}$
Timer A4 register	Address $4F_{16}$	Address $4E_{16}$

Note: At reset, the contents of the timer Ai register is undefined.

Table 6.2.2 Reading and writing from and to timer Ai register

Operating mode	Read	Write
Timer mode	Counter value is read out. (**Note 1**)	<While counting is in progress> Written only to the reload register. <While counting is stopped> Written to both of the counter and reload register.
Event counter mode		
One-shot pulse mode	Undefined value is read out.	
Pulse width modulation (PWM) mode		

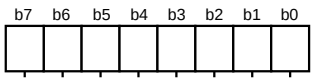
Notes 1: Also refer to **"Precautions in timer mode"** and **"Precautions in event counter mode."**

2: Perform reading or writing by the 16 bits.

EOL announced

6.2.2 Count start flag

This register is used to start or stop counting. Each bit of this register corresponds to each timer, respectively. Figure 6.2.2 shows the structure of the count start flag.



Count start flag (address 40_{16})

Bit	Bit name	Functions	At reset	RW
0	Timer A0 count start flag	0: Counting is stopped. 1: Counting is started.	0	RW
1	Timer A1 count start flag		0	RW
2	Timer A2 count start flag		0	RW
3	Timer A3 count start flag		0	RW
4	Timer A4 count start flag		0	RW
5	Timer B0 count start flag		0	RW
6	Timer B1 count start flag		0	RW
7	Timer B2 count start flag		0	RW

represents that bits 7 to 5 are not used for timer A.

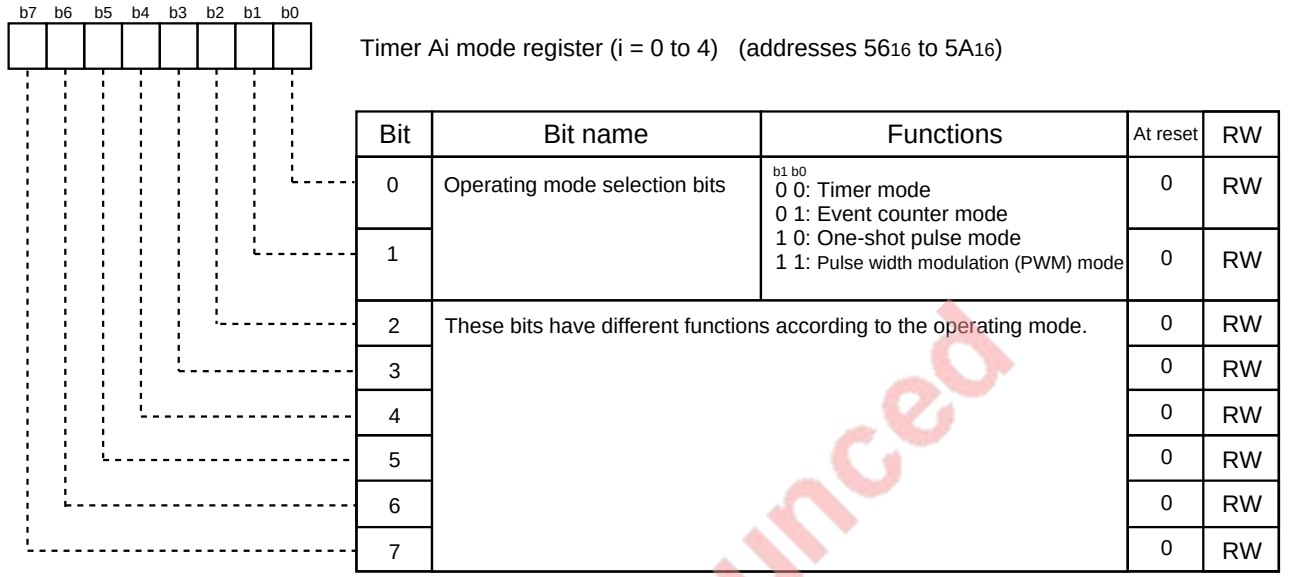
Fig. 6.2.2 Structure of count start flag

EOL announced

6.2 Block description

6.2.3 Timer Ai mode register

Figure 6.2.3 shows the structure of the timer Ai mode register. The operating mode selection bits are used to select an operating mode of timer Ai. Bits 7 to 2 have different functions according to the operating mode. These bits are described in a section of each operating mode.



Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

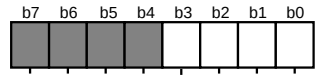
Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode 0 1: Event counter mode 1 0: One-shot pulse mode 1 1: Pulse width modulation (PWM) mode	0	RW
1			0	RW
2	These bits have different functions according to the operating mode.		0	RW
3			0	RW
4			0	RW
5			0	RW
6			0	RW
7			0	RW

Fig. 6.2.3 Structure of timer Ai mode register

EOL announced

6.2.4 Timer Ai interrupt control register

Figure 6.2.4 shows the structure of the timer Ai interrupt control register. For details about interrupts, refer to chapter **"4. INTERRUPTS."**



Timer Ai interrupt control register (i = 0 to 4) (addresses 75_{16} to 79_{16})

Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2 b1 b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 Priority is low. 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7 Priority is high.	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
7 to 4	Not implemented.		Undefined	—

Fig. 6.2.4 Structure of timer Ai interrupt control register

(1) Interrupt priority level selection bits (bits 2 to 0)

These bits select a timer Ai interrupt's priority level. When using timer Ai interrupts, select one priority level from levels 1 to 7. If a timer Ai interrupt request is generated, its priority level is compared with the processor interrupt priority level (IPL), and then the requested interrupt is enabled only when its priority level is higher than the IPL. (However, this is applied when the interrupt disable flag (I) = "0.") When disabling timer Ai interrupts, set these bits to "000_2" (Level 0).

(2) Interrupt request bit (bit 3)

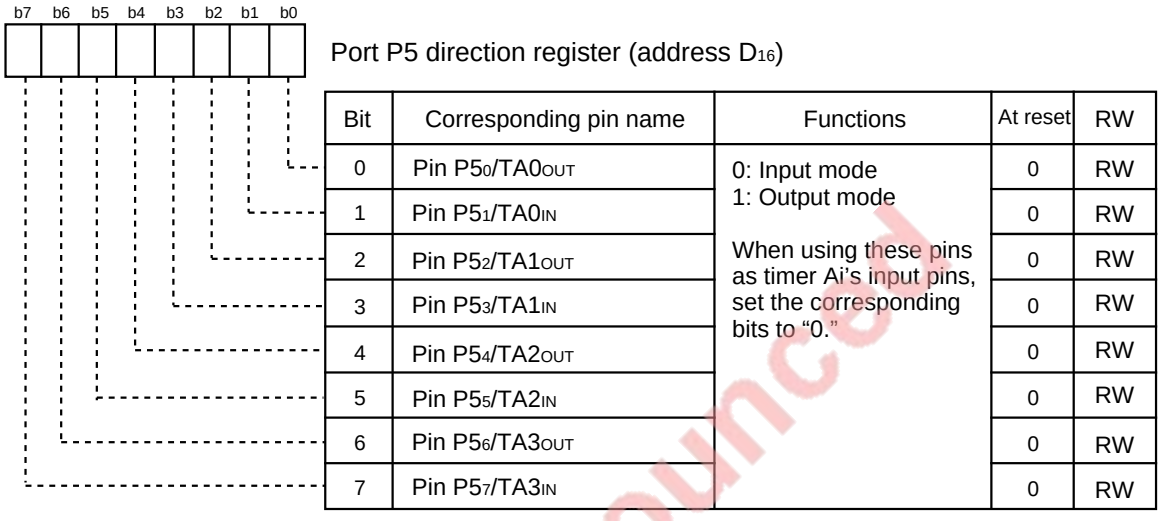
This bit is set to "1" when a timer Ai interrupt request is generated. This bit is automatically cleared to "0" when the timer Ai interrupt request is accepted. This bit can be set to "1" or cleared to "0" by software.

EOL announced

6.2 Block description

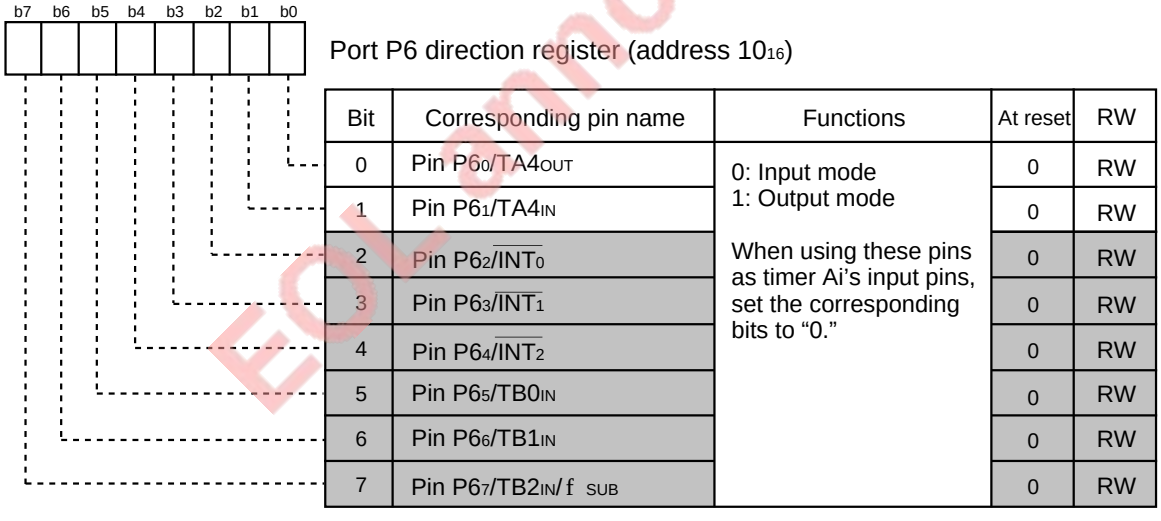
6.2.5 Port P5 and port P6 direction registers

I/O pins of timers A0 to A3 are multiplexed with port P5, and I/O pins of timer A4 are multiplexed with port P6. When using these pins as timer Ai's input pins, set the corresponding bits of the port P5 and port P6 direction registers to "0" in order to set these ports for the input mode. When using these pins as timer Ai's output pins, these pins are forcibly set to output pins of timer Ai independent of the direction registers' contents. Figure 6.2.5 shows the relationship between the port P5 and port P6 direction registers and the timer Ai's I/O pins.



Port P5 direction register (address D_{16})

Bit	Corresponding pin name	Functions	At reset	RW
0	Pin $P5_0$/$TA0_{OUT}$	0: Input mode 1: Output mode When using these pins as timer Ai's input pins, set the corresponding bits to "0."	0	RW
1	Pin $P5_1$/$TA0_{IN}$		0	RW
2	Pin $P5_2$/$TA1_{OUT}$		0	RW
3	Pin $P5_3$/$TA1_{IN}$		0	RW
4	Pin $P5_4$/$TA2_{OUT}$		0	RW
5	Pin $P5_5$/$TA2_{IN}$		0	RW
6	Pin $P5_6$/$TA3_{OUT}$		0	RW
7	Pin $P5_7$/$TA3_{IN}$		0	RW



Port P6 direction register (address 10_{16})

Bit	Corresponding pin name	Functions	At reset	RW
0	Pin $P6_0$/$TA4_{OUT}$	0: Input mode 1: Output mode When using these pins as timer Ai's input pins, set the corresponding bits to "0."	0	RW
1	Pin $P6_1$/$TA4_{IN}$		0	RW
2	Pin $P6_2$/$\overline{INT_0}$		0	RW
3	Pin $P6_3$/$\overline{INT_1}$		0	RW
4	Pin $P6_4$/$\overline{INT_2}$		0	RW
5	Pin $P6_5$/$TB0_{IN}$		0	RW
6	Pin $P6_6$/$TB1_{IN}$		0	RW
7	Pin $P6_7$/$TB2_{IN}$/f_{SUB}		0	RW

represents that bits 2 to 7 are not used for timer A.

EOL announced

Fig. 6.2.5 Relationship between port P5 and port P6 direction registers and timer Ai's I/O pins

6.3 Timer mode (Bits 1 and 0 of timer Ai mode register = "00$_2$")

In this mode, a count source internally generated is counted. (Refer to **Table 6.3.1.**) Figure 6.3.1 shows the structures of the timer Ai mode register and timer Ai register in the timer mode.

Table 6.3.1 Specifications of timer mode

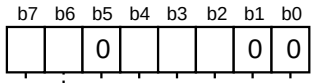
Item	Specifications
Count source	Clock f_2, f_{16}, f_{64}, or f_{512}
Count operation	● Countdown ● At an underflow, the reload register's contents is reloaded, and counting is continued.
Division ratio	$\frac{1}{(n+1)}$ n: Set value in the timer Ai register
Count start condition	When the count start flag is set to "1."
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	At an underflow
Pin TA_{iIN}'s function	Programmable I/O port or gate input
Pin TA_{iOUT}'s function	Programmable I/O port or pulse output
Read from timer	A counter value can be read out by reading the timer Ai register.
Write to timer	■ While counting is stopped When a value is written to the timer Ai register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer Ai register, it is written only to the reload register. (Transferred to the counter at the next reload time.)

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

EOL announced

TIMER A

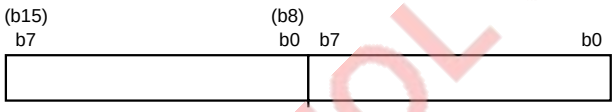
6.3 Timer mode



Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode	0	RW
1			0	RW
2	Pulse output function selection bit	0: No pulse is output. (Pin TAi_{OUT} functions as a programmable I/O port.) 1: Pulse is output. (Pin TAi_{OUT} functions as a pulse output pin.)	0	RW
3	Gate function selection bits	b4 b3 0 X: No gate function (Pin TAi_{IN} functions as a programmable I/O port.) 1 0: Counter counts only while pin TAi_{IN}'s input signal level is "L." 1 1: Counter counts only while pin TAi_{IN}'s input signal level is "H."	0	RW
4			0	RW
5	Must be fixed to "0" in the timer mode.		0	RW
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**



Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

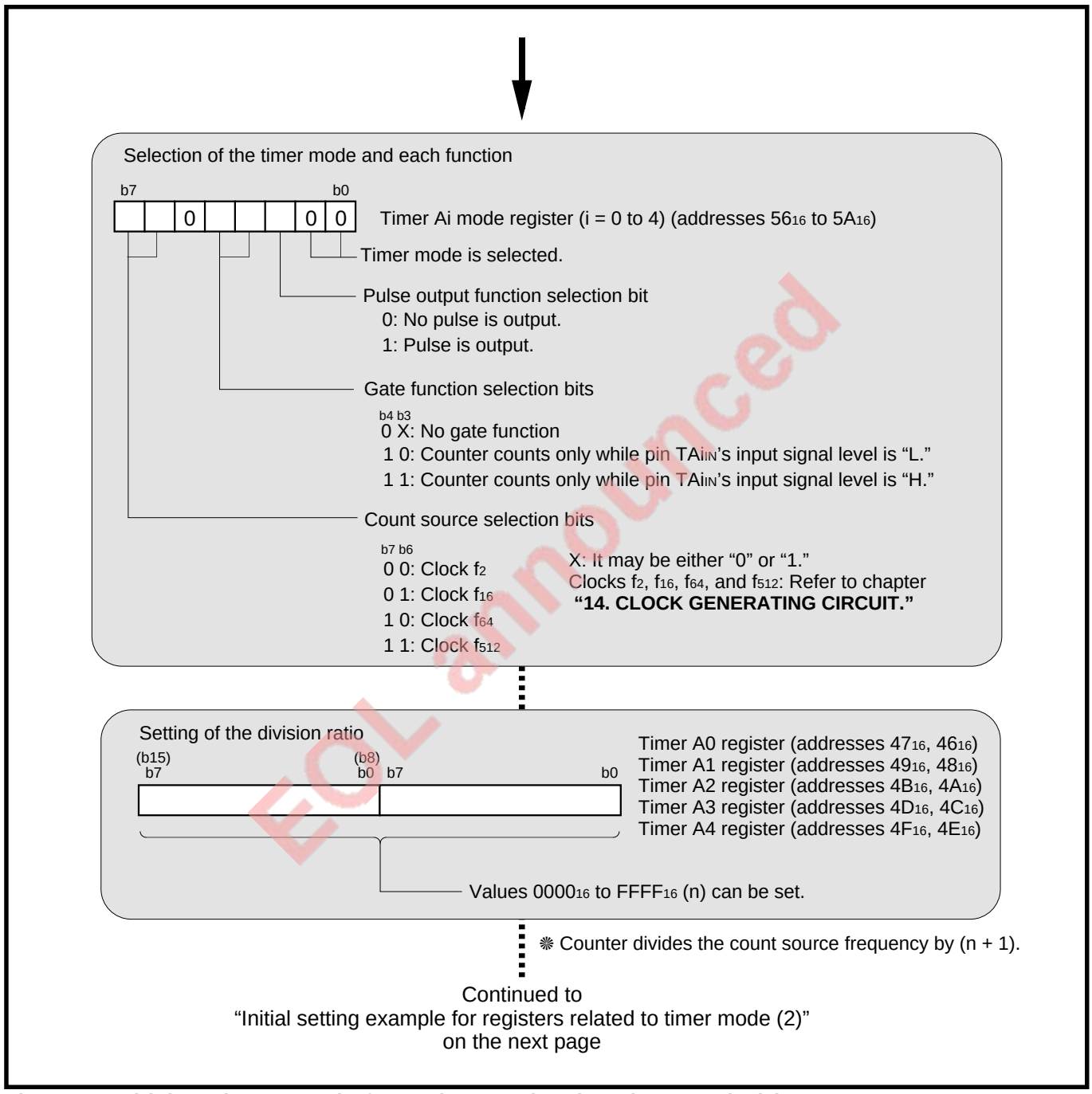
Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Undefined	RW

EOL announced

Fig. 6.3.1 Structures of timer Ai mode register and timer Ai register in timer mode

6.3.1 Setting for timer mode

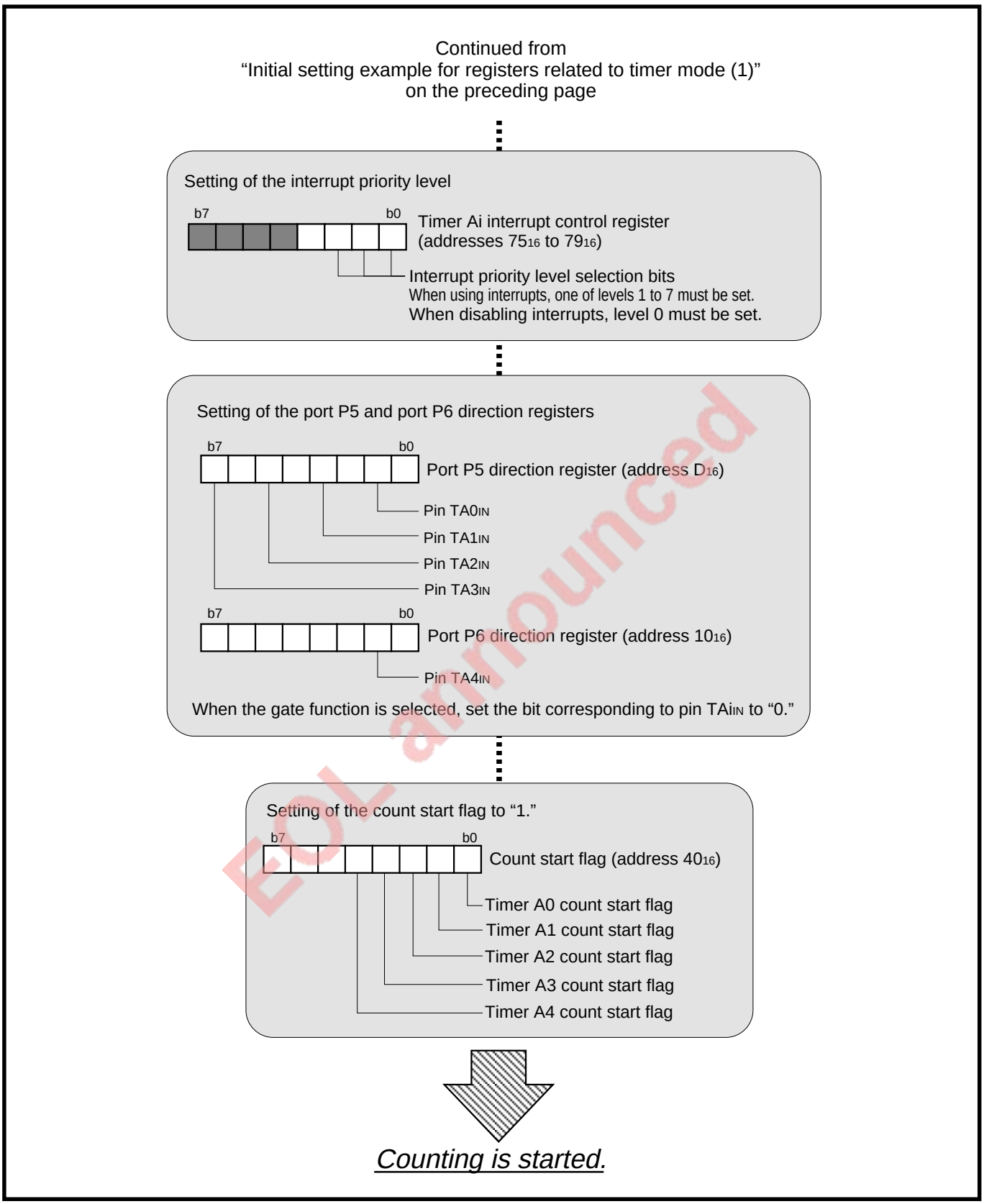
Figures 6.3.2 and 6.3.3 show an initial setting example for registers related to the timer mode.
Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**



ECL announced

Fig. 6.3.2 Initial setting example for registers related to timer mode (1)

6.3 Timer mode



EOL announced

Fig. 6.3.3 Initial setting example for registers related to timer mode (2)

6.3.2 Count source

In the timer mode, by the count source selection bits (bits 6 and 7 at addresses 56_{16} to $5A_{16}$), a count source can be selected. Table 6.3.2 lists the relationship between the count source selection bits and count source.

Table 6.3.2 Relationship between count source selection bits and count source

b7	b6	Count source	Frequency of count source		
			When system clock = 25 MHz	When system clock = 16 MHz	When system clock = 8 MHz
0	0	f_2	12.5 MHz	8 MHz	4 MHz
0	1	f_{16}	1.5625 MHz	1 MHz	500 kHz
1	0	f_{64}	390.625 kHz	250 kHz	125 kHz
1	1	f_{512}	48.8281 kHz	31.25 kHz	15.625 kHz

Clocks f_2, f_{16}, f_{64}, f_{512}, and system clock: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0" and the main clock division selection bit (bit 0 at address $6F_{16}$) = "0." (For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)

EOL announced

6.3 Timer mode

6.3.3 Operation in timer mode

① When the count start flag is set to “1,” the counter starts counting of the count source.
② When an underflow occurs, the reload register’s contents is reloaded, and then counting is continued.
③ The timer Ai interrupt request bit is set to “1” when the underflow occurs in ②.
After this, the interrupt request bit remains set to “1” until the interrupt request is accepted or the interrupt request bit is cleared to “0” by software.

Figure 6.3.4 shows an operation example in the timer mode.

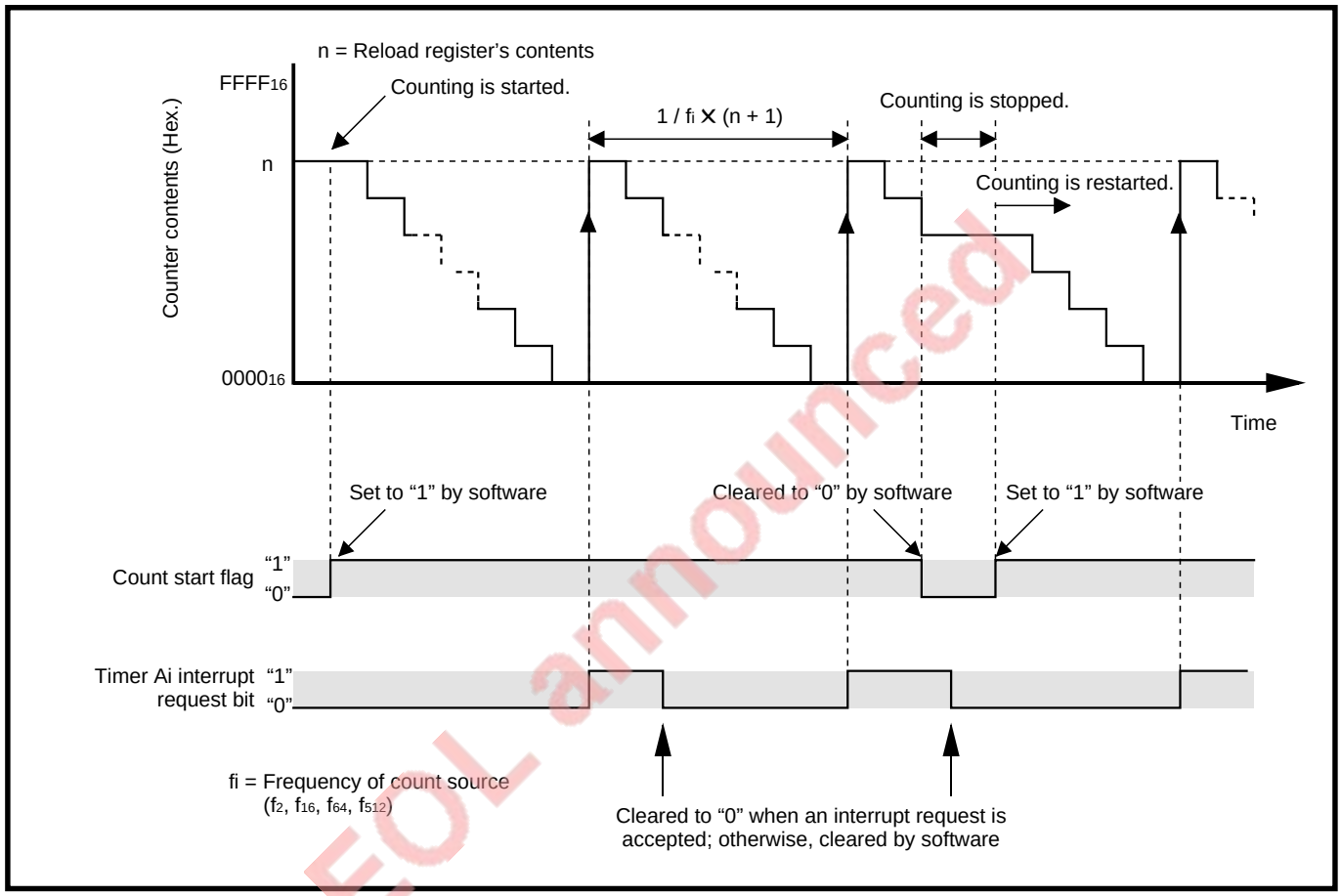


Fig. 6.3.4 Operation example in timer mode (without pulse output and gate functions)

EOL announced

6.3.4 Selectable functions

The gate and pulse output functions are described below.

(1) Gate function

The gate function is selected by setting the gate function selection bits (bits 4 and 3 at addresses 56_{16} to $5A_{16}$) to "10_2" or "11_2." When the gate function is selected, counting can be started or stopped by pin TAiIN's input signal. Table 6.3.3 lists the count valid levels. Figure 6.3.5 shows an operation example when the gate function is selected.

When selecting the gate function, set the port P5 and port P6 direction registers' bits which correspond to pin TAiIN for the input mode. Also make sure that pin TAiIN's input signal has a pulse width equal to or greater than two cycles of the count source.

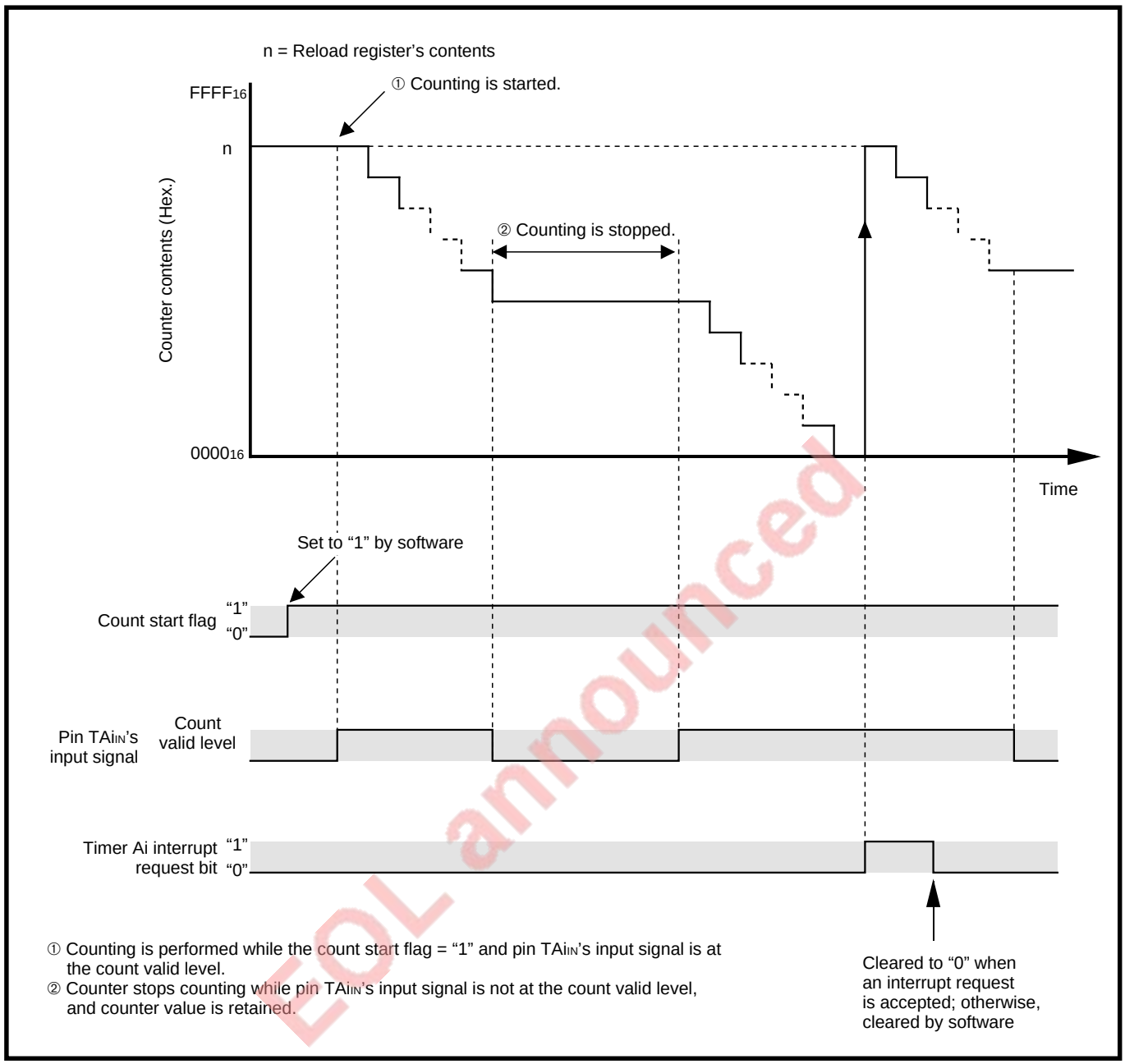
Table 6.3.3 Count valid levels

Gate function selection bits		Count valid level (Duration of counting)
b4	b3	
1	0	While pin TAiIN's input signal level is "L"
1	1	While pin TAiIN's input signal level is "H"

Note: The counter does not count while pin TAiIN's input signal is not at the count valid level.

EOL announced

6.3 Timer mode



EOL announced

Fig. 6.3.5 Operation example when gate function is selected

(2) Pulse output function

The pulse output function is selected by setting the pulse output function selection bit (bit 2 at addresses 56_{16} to $5A_{16}$) to "1." When this function is selected, pin TAiOUT is forcibly set as the pulse output pin independent of the corresponding bits of the port P5 and port P6 direction registers. And then, pin TAiOUT outputs the signal of which polarity is inverted each time an underflow occurs.

When the count start flag (address 40_{16}) = "0," in other words, when counting is stopped, pin TAiOUT outputs "L" level. Figure 6.3.6 shows an operation example when the pulse output function is selected.

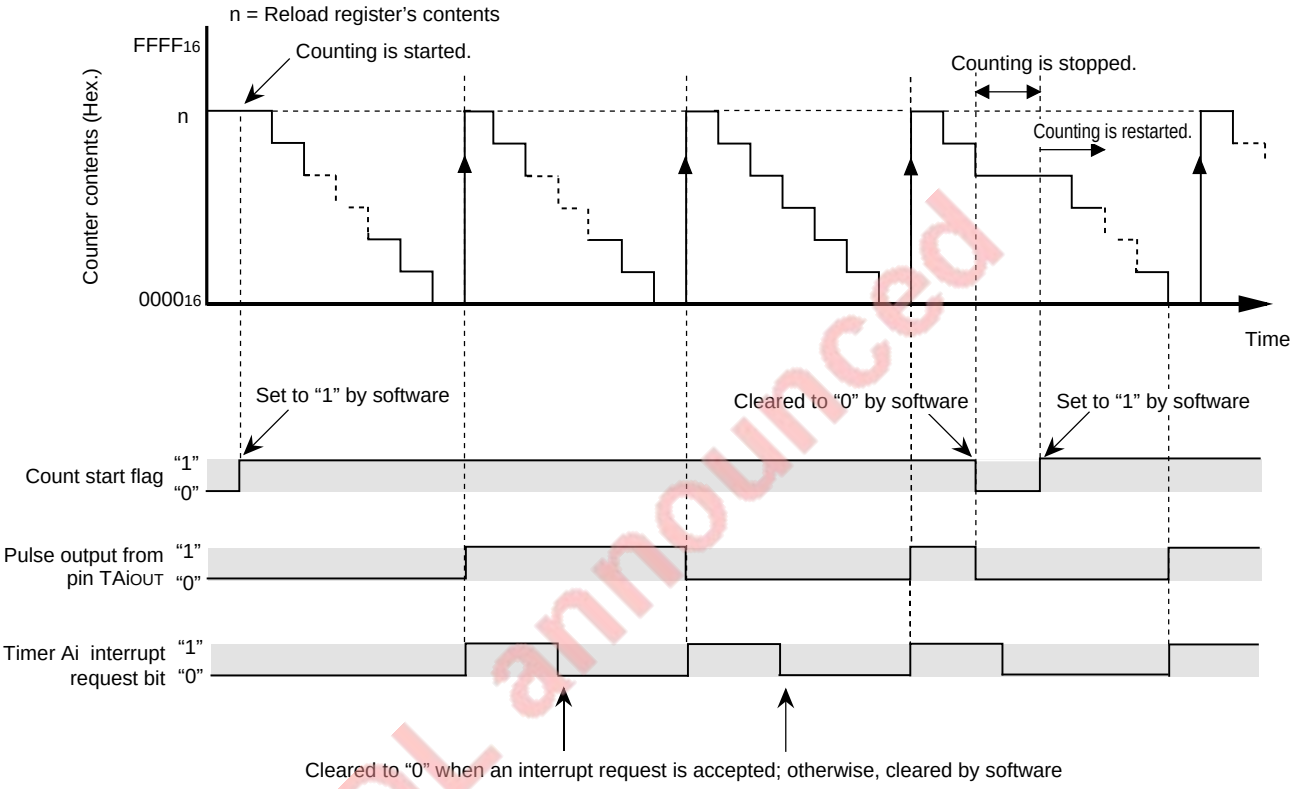


Fig. 6.3.6 Operation example when pulse output function is selected

EOL announced

TIMER A

6.3 Timer mode

[Precautions in timer mode]

While counting is in progress, by reading out the timer Ai register, the counter value can be read at an arbitrary timing. However, when reading is performed at the reload timing shown in Figure 6.3.7, value "FFFF$_{16}$" is read out. If reading is performed in the period from when a value is set into the timer Ai register with the counter stopped until the counter starts counting, the set value is correctly read out.

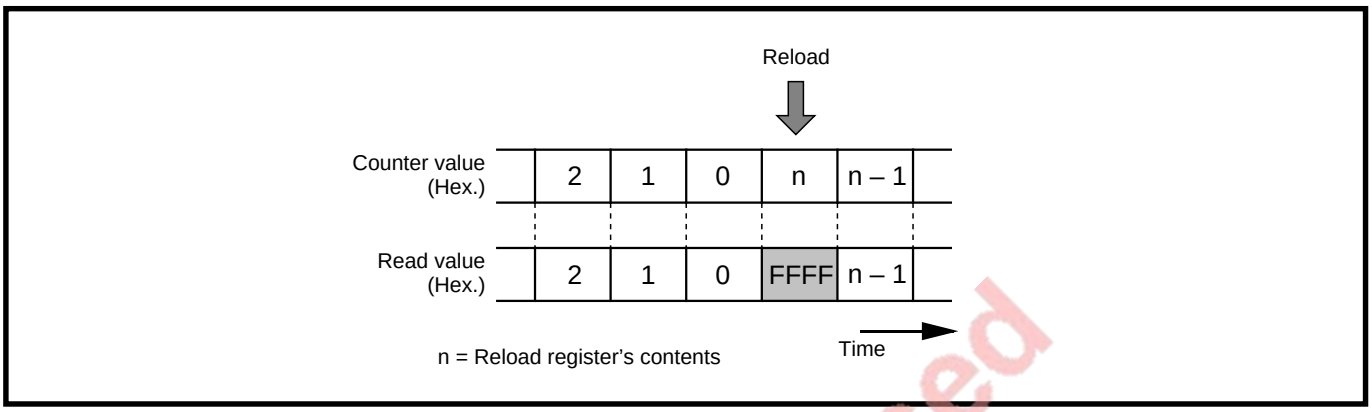


Fig. 6.3.7 Timer Ai register read out

EOL announced

6.4 Event counter mode (Bits 1 and 0 of timer Ai mode register = "01$_2$")

In this mode, an external signal is counted. (Refer to **Tables 6.4.1** and **6.4.2.**) Figures 6.4.1 and 6.4.2 show the structures of the timer Ai mode register and timer Ai register in the event counter mode.

Table 6.4.1 Specifications of event counter mode (when not using two-phase pulse signal processing function)

Item	Specifications
Count source	● External signal input to pin TAi$_{IN}$ ● "Falling edge" or "Rising edge" can be selected as the valid edge of the count source by software.
Count operation	● "Countup" or "countdown" can be selected by the external signal or software ● At an overflow or underflow, the reload register's contents is reloaded, and counting is continued **(Note)**.
Division ratio	< While counting down> $\frac{1}{(n + 1)}$ < While counting up> $\frac{1}{(FFFF_{16} - n + 1)}$ n: Set value in the timer Ai register
Count start condition	When the count start flag is set to "1."
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	At an overflow or underflow
Pin TAi$_{IN}$'s function	Count source input
Pin TAi$_{OUT}$'s function	Programmable I/O port, pulse output, or countup/countdown switch signal input
Read from timer	A counter value can be read out by reading the timer Ai register.
Write to timer	■ While counting is stopped When a value is written to the timer Ai register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer Ai register, it is written only to the reload register. (Transferred to the counter at the next reload time.)

Note: This is applied when not using the free-run count function.

EOL announced

6.4 Event counter mode

Table 6.4.2 Specifications of event counter mode (when using two-phase pulse signal processing function in timers A2, A3, and A4)

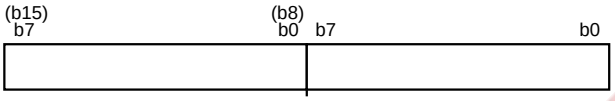
Item	Specifications
Count source	External signal (two-phase pulse) input to pin TAjIN or TAjOUT (j = 2 to 4)
Count operation	● "Countup" or "countdown" can be selected by the external signal (two-phase pulse). ● At an overflow or underflow, the reload register's contents is reloaded, and counting is continued. **(Note)**
Division ratio	< While counting down> $\frac{1}{(n + 1)}$ < While counting up> $\frac{1}{(FFFF_{16} - n + 1)}$ n: Set value in the timer Aj register
Count start condition	When the count start flag is set to "1."
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	At an overflow or underflow
Pin TAjIN, TAjOUT's (j = 2 to 4) function	Two-phase pulse input
Read from timer	A counter value can be read out by reading the timer A2, A3, or A4 register.
Write to timer	■ While counting is stopped When a value is written to the timer A2, A3, or A4 register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer A2, A3, or A4 register, it is written only to the reload register. (Transferred to the counter at the next reload time.)

Note: This is applied when not using the free-run count function.

EOL announced

Timer A0 mode register (address 56_{16})
Timer A1 mode register (address 57_{16})

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 1: Event counter mode	0	RW
1			0	RW
2	Pulse output function selection bit	0: No pulse is output. (Pin $TA0_{OUT}$ or $TA1_{OUT}$ functions as a programmable I/O port.) 1: Pulse is output. (Pin $TA0_{OUT}$ or $TA1_{OUT}$ functions as a pulse output pin.)	0	RW
3	Count polarity selection bit	0: Counts at falling edge of external signal 1: Counts at rising edge of external signal	0	RW
4	Up-down switching factor selection bit	0: Contents of the up-down flag 1: A signal which is input to pin $TA0_{OUT}$ or $TA1_{OUT}$	0	RW
5	Must be fixed to “0” in the event counter mode.		0	RW
6	These bits are ignored in the event counter mode.		0	RW
7			0	RW



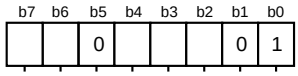
Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1) in down-counting, or by ($FFFF_{16}$ – n + 1) in up-counting. At reading this register, the counter value is read out.	Undefined	RW

EOL announced

Fig. 6.4.1 Structures of timer A0 and A1 mode registers and timer A0 and A1 registers in event counter mode

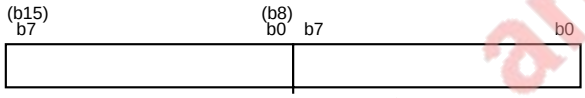
6.4 Event counter mode



Timer A2 mode register (address 58_{16})
Timer A3 mode register (address 59_{16})
Timer A4 mode register (address $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 1: Event counter mode	0	RW
1			0	RW
2	Pulse output function selection bit	0: No pulse is output. (Pin $TA2_{OUT}$, $TA3_{OUT}$, or $TA4_{OUT}$ functions as a programmable I/O port.) 1: Pulse is output. (Pin $TA2_{OUT}$, $TA3_{OUT}$, or $TA4_{OUT}$ functions as a pulse output pin.)	0	RW
3	Count polarity selection bit	0: Counting is performed at the falling edge of the external signal. 1: Counting is performed at the rising edge of the external signal.	0	RW
4	Up-down switching factor selection bit	0: Contents of the up-down flag 1: A signal which is input to pin $TA2_{OUT}$, $TA3_{OUT}$, or $TA4_{OUT}$	0	RW
5	Must be fixed to “0” in the event counter mode.		0	RW
6	Count type selection bit	0: Reload count type 1: Free-run count type	0	RW
7	Two-phase pulse signal processing type selection bit **(Note)**	0: Normal processing 1: Quadruple processing	0	RW

Note: This bit is valid only for the timer A3 mode register.
For the timer A2 and A4 mode registers, this bit is ignored. (It may be “0” or “1.”)



Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

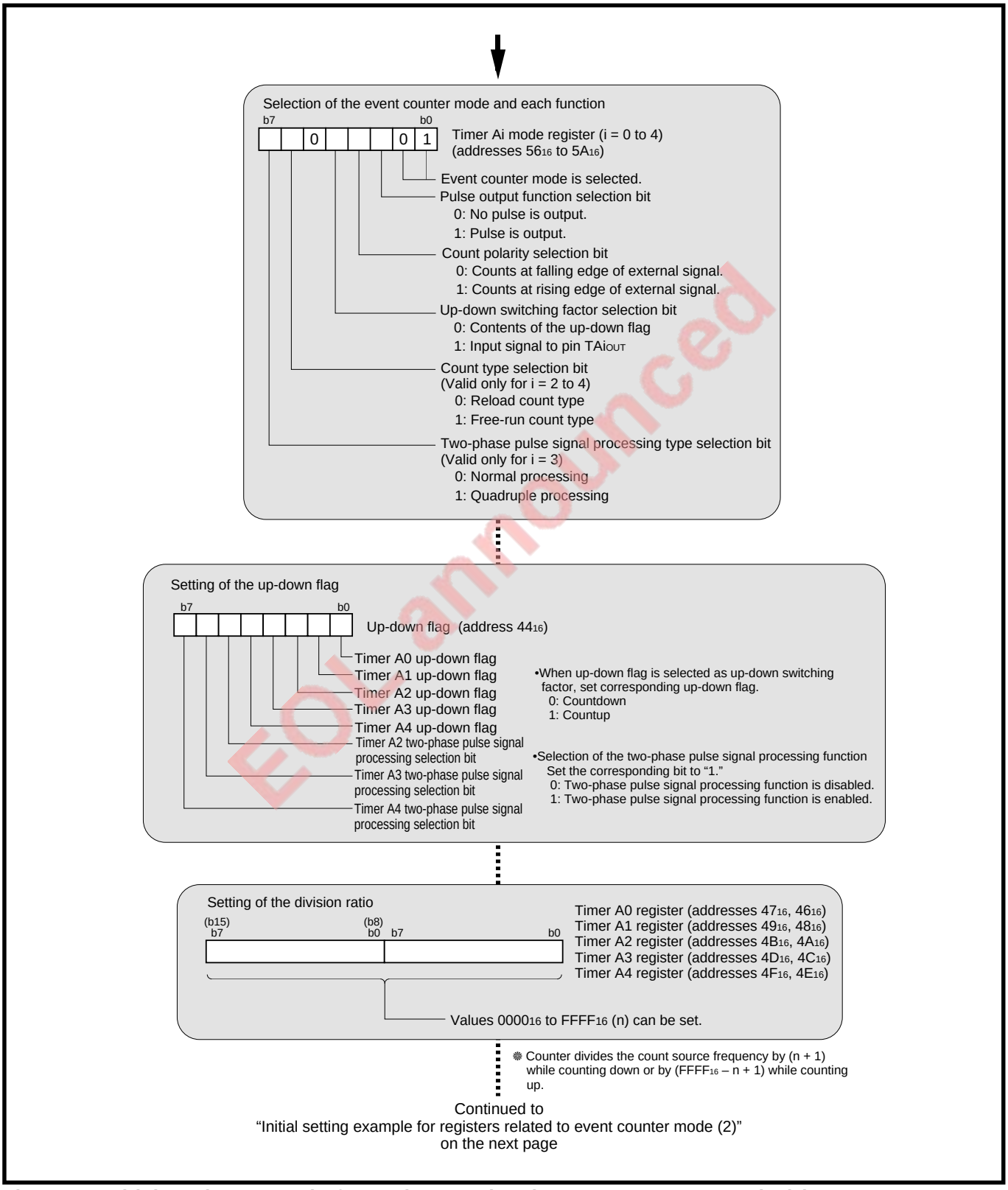
Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1) in down-counting, or by ($FFFF_{16}$ – n + 1) in up-counting. At reading this register, the counter value is read out.	Undefined	RW

EOL announced

Fig. 6.4.2 Structures of timer A2, A3, and A4 mode registers and timer A2, A3, and A4 registers in event counter mode

6.4.1 Setting for event counter mode

Figure 6.4.3 and 6.4.4 show an initial setting example for registers related to the event counter mode. Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**



EOL announced

Fig. 6.4.3 Initial setting example for registers related to event counter mode (1)

6.4 Event counter mode

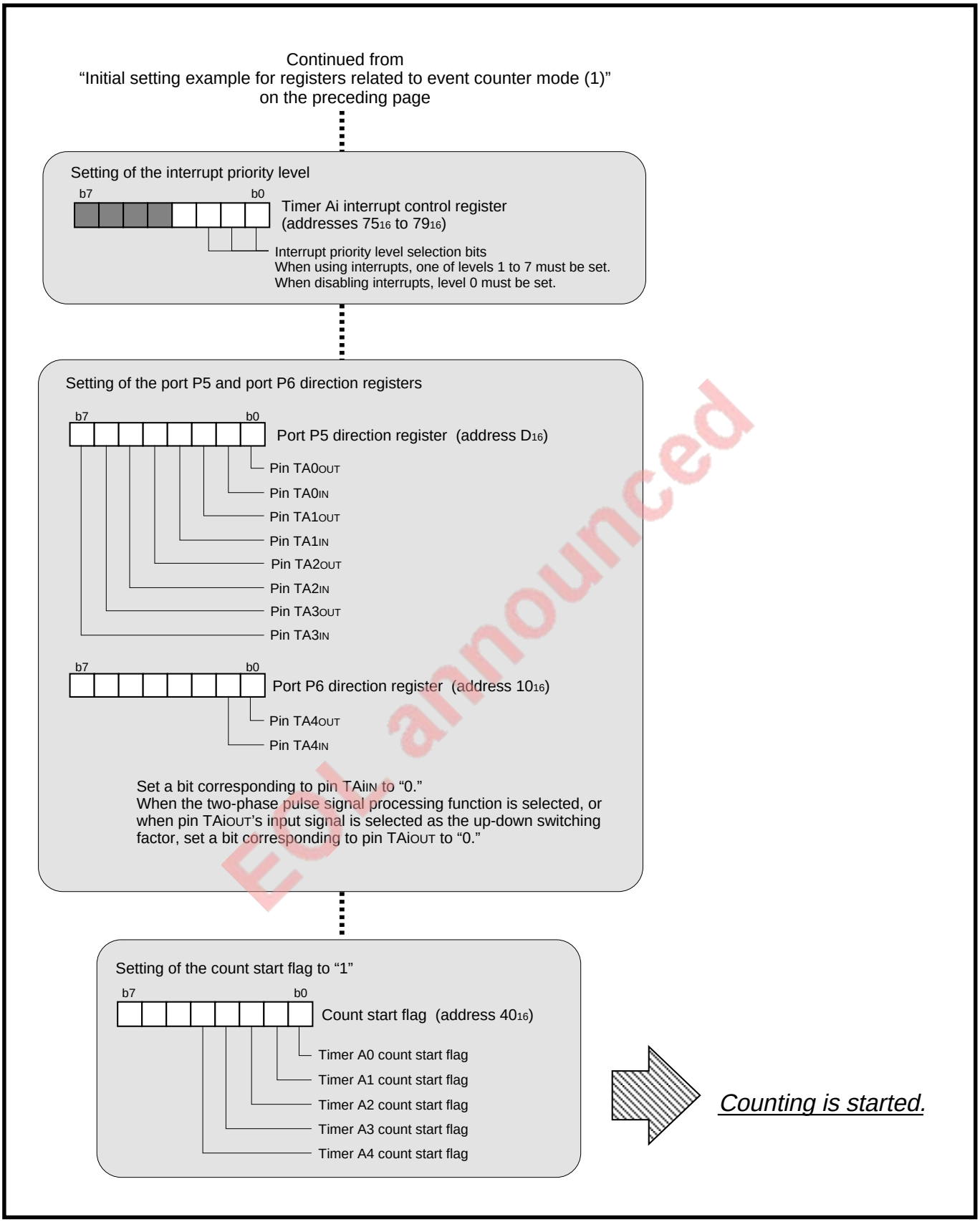


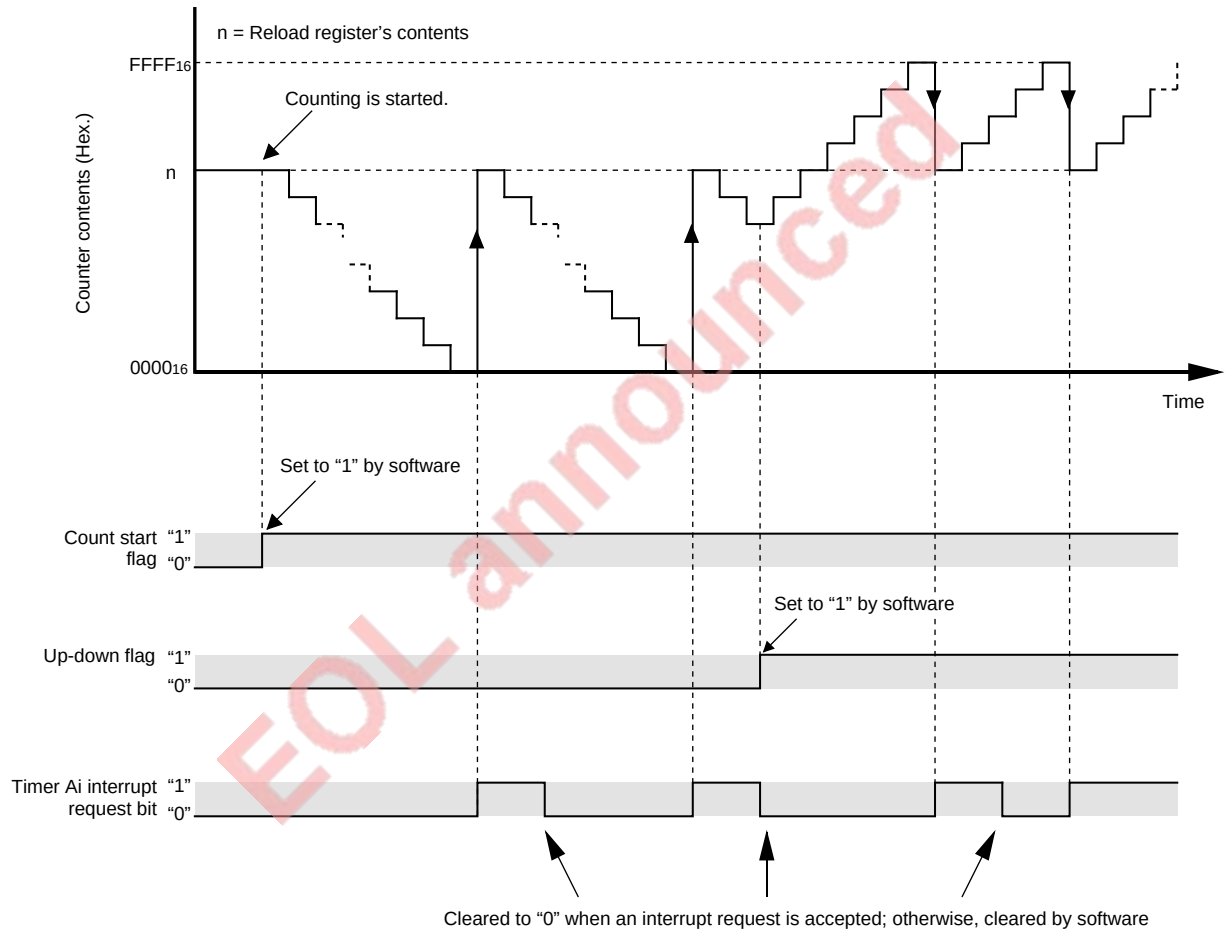
Fig. 6.4.4 Initial setting example for registers related to event counter mode (2)

EOL announced

6.4.2 Operation in event counter mode

① When the count start flag is set to “1,” the counter starts counting of the count source.
② The counter counts the count source’s valid edges.
③ When an underflow or overflow occurs, the reload register’s contents is reloaded, and then counting is continued.
④ The timer Ai interrupt request bit is set to “1” when the underflow or overflow occurs in ③.
After this, the interrupt request bit remains set to “1” until the interrupt request is accepted or the interrupt request bit is cleared to “0” by software.

Figure 6.4.5 shows an operation example in the event counter mode.



❋ The above is applied when the up-down flag’s content is selected as the up-down switching factor (i.e., up-down switching factor selection bit = “0”).

Fig. 6.4.5 Operation example in event counter mode (without free-run count function, pulse output function, and two-phase pulse signal processing function)

EOL announced

6.4 Event counter mode

(1) Switching between countup and countdown

A register named “up-down flag” (address 44_{16}) or pin TAiOUT’s input signal switches countup from and to countdown. This switching is performed by an up-down flag when the up-down switching factor selection bit (bit 4 at addresses 56_{16} to $5A_{16}$) = “0” and by pin TAiOUT’s input signal when the up-down switching factor selection bit = “1.”

When the switching between countup and countdown is set while counting is in progress, this switching is realized at the next valid edge of the count source.

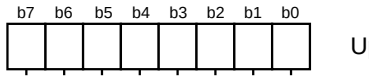
■ When switching by up-down flag

Countdown is performed when the up-down flag = “0,” and countup is performed when the up-down flag = “1.” Figure 6.4.6 shows the structure of the up-down flag.

■ When switching by pin TAiOUT’s input signal

Countdown is performed when pin TAiOUT’s input signal level is “L” and countup is performed when it is “H.”

When switching countup from and to countdown by pin TAiOUT’s input signal, set a port P5 or P6 direction register’s bit which corresponds to pin TAiOUT for the input mode.



Up-down flag (address 44_{16})

Bit	Bit name	Functions	At reset	RW
0	Timer A0 up-down flag	0: Countdown 1: Countup This bits is valid when the contents of the up-down flag is selected as the up-down switching factor.	0	RW
1	Timer A1 up-down flag		0	RW
2	Timer A2 up-down flag		0	RW
3	Timer A3 up-down flag		0	RW
4	Timer A4 up-down flag		0	RW
5	Timer A2 two-phase pulse signal processing selection bit	0: Two-phase pulse signal processing function is disabled. 1: Two-phase pulse signal processing function is enabled. When not using the two-phase pulse signal processing function, be sure to set this bit to “0.” This bit is “0” at reading.	0	WO
6	Timer A3 two-phase pulse signal processing selection bit		0	WO
7	Timer A4 two-phase pulse signal processing selection bit		0	WO

Note: When writing to bits 5 to 7, use the **LDM** or **STA** instruction.

EOL announced

Fig. 6.4.6 Structure of up-down flag

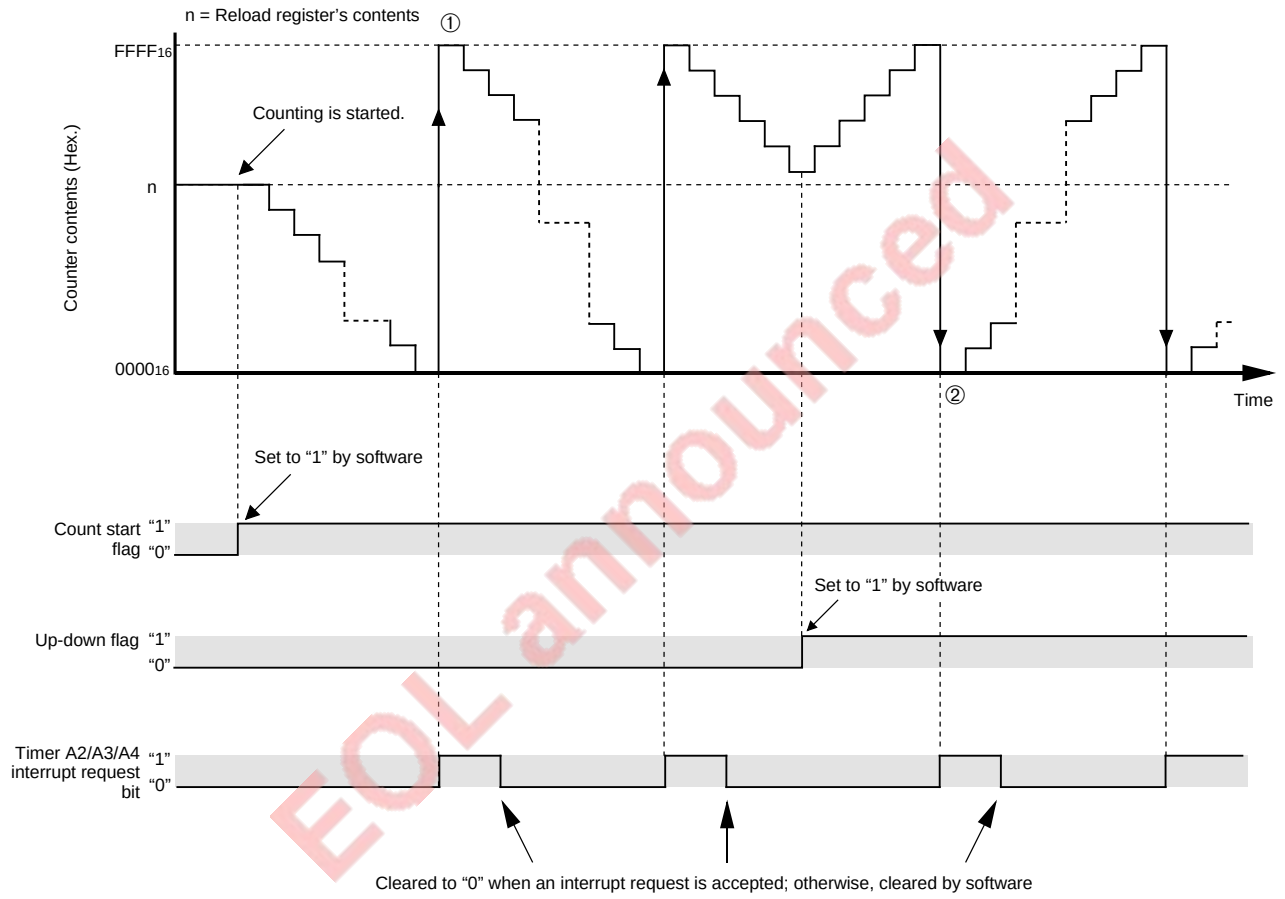
6.4.3 Selectable functions

The free-run count, pulse output, and two-phase pulse signal processing functions are described below.

(1) Free-run count function (Timers A2 to A4)

For timers A2 to A4, when the count type selection bit (bit 6 at addresses 58_{16} to $5A_{16}$) is set to "1," the free-run count function is selected. When the free-run count function is selected, although a timer A2/A3/A4 interrupt request is generated at an overflow or underflow, the reload register's contents is not reloaded into the counter.

Figure 6.4.7 shows an operation example when the free-run count function is selected.



① After an underflow, counter starts counting from $FFFF_{16}$.
② After an overflow, counter starts counting from 0000_{16}.

✺ The above is applied when the up-down flag's contents is selected as the up-down switching factor (i.e., up-down switching factor selection bit = "0").

Fig. 6.4.7 Operation example when free-run count function is selected (without pulse output function and two-phase pulse signal processing function)

EOL announced

6.4 Event counter mode

(2) Pulse output function

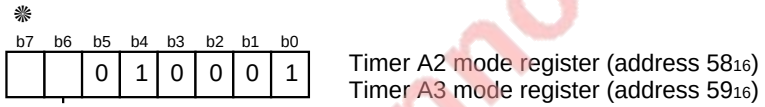
The pulse output function is selected by setting the pulse output function selection bit (bit 2 at addresses 56_{16} to $5A_{16}$) to "1." When this function is selected, pin TAiOUT is forcibly set as the pulse output pin independent of the corresponding bit of the port P5 or port P6 direction register. And then, pin TAiOUT outputs a signal of which polarity is inverted each time an underflow or overflow occurs (Refer to **Figure 6.3.6**).

When the count start flag (address 40_{16}) = "0," in other words, when counting is stopped, pin TAiOUT outputs "L" level.

(3) Two-phase pulse signal processing function (Timers A2 to A4)

For timers A2 to A4, the two-phase pulse signal processing function is selected by setting the two-phase pulse signal processing selection bits (bits 5 to 7 at address 44_{16}) to "1." (Refer to **Figure 6.4.6.**) Figure 6.4.8 shows the timer A2, A3, and A4 mode registers when the two-phase pulse signal processing function is selected.

In a timer with the two-phase pulse signal processing function selected, two kinds of pulses of which phases differ by 90 degrees are counted. There are two types of the two-phase pulse signal processing: normal processing and quadruple processing. In timer A2, normal processing is performed; in timer A4, quadruple processing is performed. In timer A3, either normal processing or quadruple processing can be selected by the two-phase pulse signal processing type selection bit (bit 7 at address 59_{16}). Some bits of the port P5 and P6 direction registers correspond to pins used for the two-phase pulse input. Set these bits for the input mode.



✵: Bit 7 of the timer A3 mode register is used to select the two-phase pulse signal processing type of timer A3.
Normal processing is selected when this bit = "0," and quadruple processing is selected when this bit = "1."
Bit 7 of the timer A2/A4 mode register is ignored. (It may be "0" or "1.")

Not announced

Fig. 6.4.8 Timer A2, A3, and A4 mode registers when two-phase pulse signal processing function is selected

■ Normal processing

Countup is performed at the rising edges of pin TAkIN (k = 2 and 3) if the phase relationship is such that pin TAkIN's input signal level changes from "L" to "H" while pin TAkOUT's input signal level is "H."

Countdown is performed at the falling edges of pin TAkIN if the phase relationship is such that pin TAkIN's input signal level changes from "H" to "L" while pin TAkOUT's input signal level is "H." (Refer to **Figure 6.4.9**.)

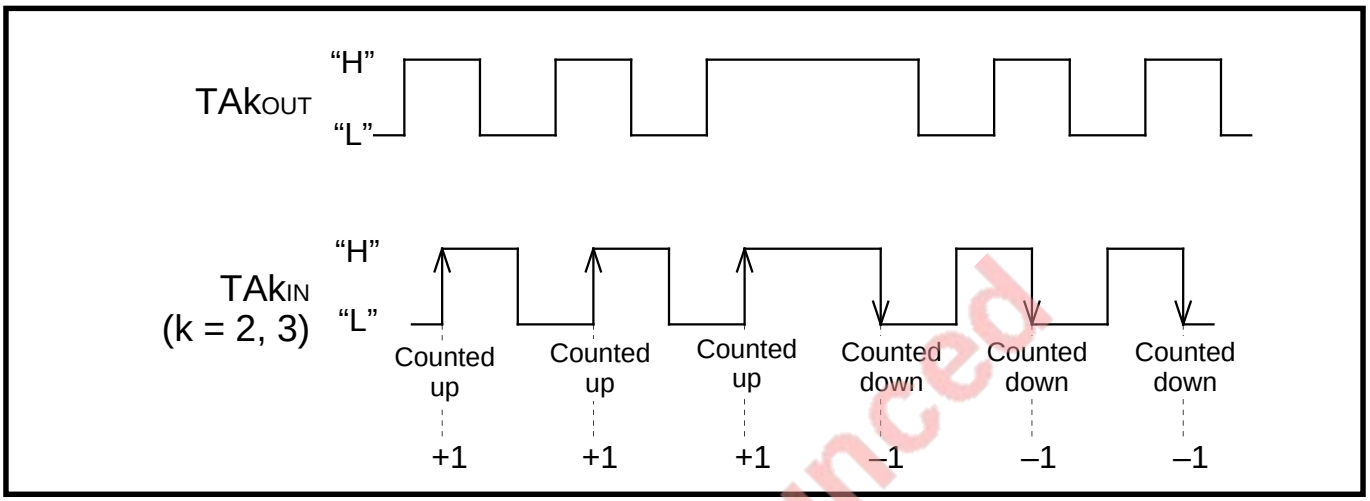


Fig. 6.4.9 Normal processing

■ Quadruple processing

Countup is performed at the rising and falling edges of pins TAlOUT (l = 3 and 4) and TAlIN if the phase relationship is such that pin TAlIN's input signal level changes from "L" to "H" while pin TAlOUT's input signal level is "H."

Countdown is performed at the rising and falling edges of pins TAlOUT and TAlIN if the phase relationship is such that pin TAlIN's input signal level changes from "H" to "L" while pin TAlOUT's input signal level is "H." (Refer to **Figure 6.4.10**.)

Table 6.4.3 lists input signals of pins TAlOUT and TAlIN when the quadruple processing is selected.

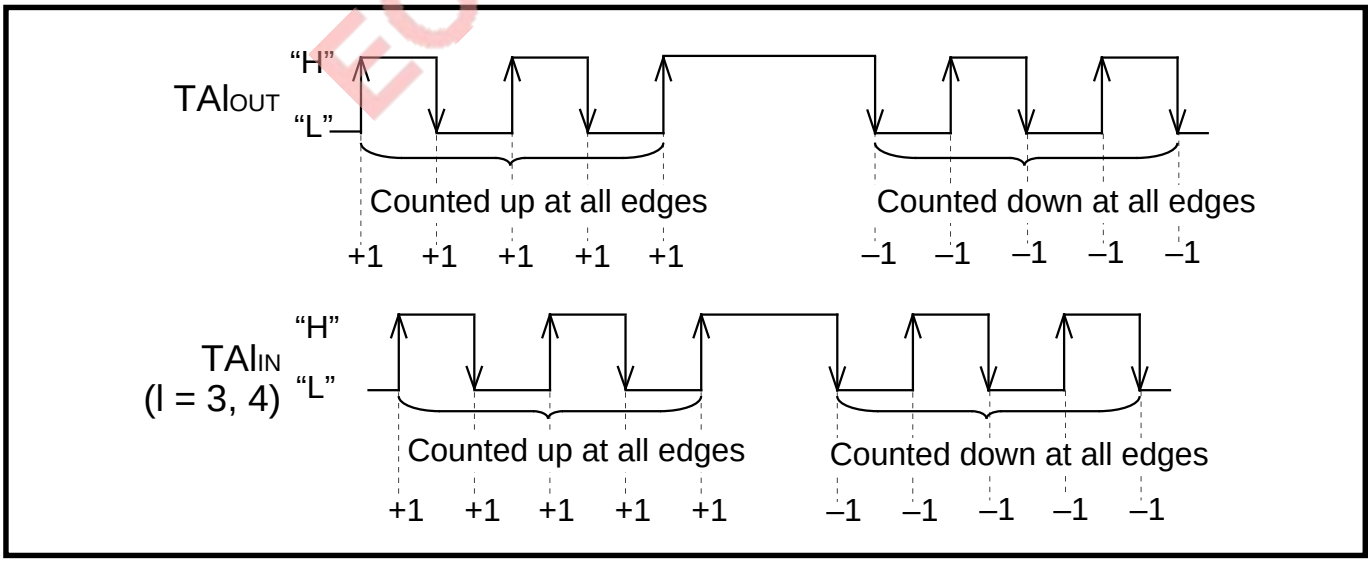


Fig. 6.4.10 Quadruple processing

EOL announced

6.4 Event counter mode

Table 6.4.3 Pin TAIOUT and TAIIN's input signals when quadruple processing is selected

	Input signal of pin TAIOUT	Input signal of pin TAIIN
Countup	"H" level	Rising edge
	"L" level	Falling edge
	Rising edge	"L" level
	Falling edge	"H" level
Countdown	"H" level	Falling edge
	"L" level	Rising edge
	Rising edge	"H" level
	Falling edge	"L" level

EOL announced

[Precautions in event counter mode]

1. While counting is in progress, by reading out the timer Ai register, the counter value can be read at an arbitrary timing. However, when reading is performed at the reload timing shown in Figure 6.4.11, value "FFFF$_{16}$" is read out at an underflow and value "0000$_{16}$" is read out at an overflow. If reading is performed in the period from when a value is set into the timer Ai register with the counter stopped until the counter starts counting, the set value is correctly read out.

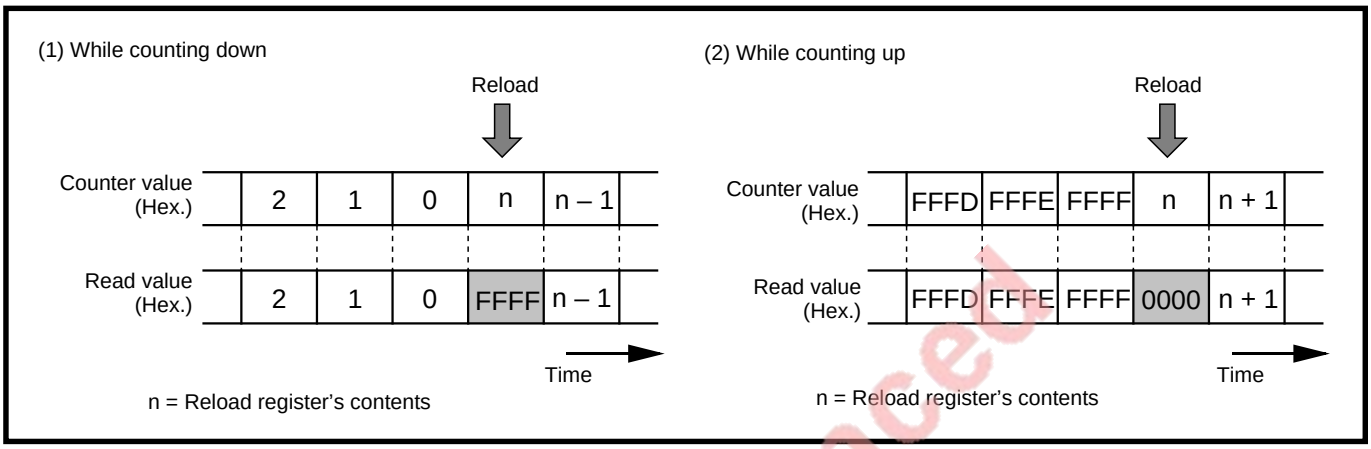


Fig. 6.4.11 Timer Ai register read out

2. Pin TAiOUT is used for all functions listed below. Therefore, only one of the following functions can be used for one timer.
   - Switching between countup and countdown by pin TAiOUT's input signal
   - Pulse output function
   - Two-phase pulse signal processing function (Timers A2 to A4)

EOL announced

6.5 One-shot pulse mode (Bits 1 and 0 of timer Ai mode register = "10_2")

In this mode, a pulse which has an arbitrary width is output once. (Refer to **Table 6.5.1**.) After a trigger occurs, "H" level is output from pin TAiOUT for an arbitrary time. Figure 6.5.1 shows the structures of the timer Ai mode register and timer Ai register in the one-shot pulse mode.

Table 6.5.1 Specifications of one-shot pulse mode

Item	Specifications
Count source	Clock f_2, f_{16}, f_{64}, or f_{512}
Count operation	● Countdown ● When the counter value reaches "0000_{16}," the reload register's contents is reloaded, and counting stops. ● When a trigger occurs while counting is in progress, the reload register's contents is reloaded, and counting is continued.
Output pulse width ("H")	$\frac{n}{fi}$ [s] n: Set value in the timer Ai register
Count start condition	● When a trigger occurs. (**Note**) ● Internal or external trigger can be selected by software.
Count stop condition	● When the counter value reaches "0000_{16}." ● When the count start flag is cleared to "0."
Interrupt request occurrence timing	When counting stops.
Pin TAiIN's function	Programmable I/O port or trigger input
Pin TAiOUT's function	One-shot pulse output
Read from timer	An undefined value is read out by reading the timer Ai register.
Write to timer	■ While counting is stopped When a value is written to the timer Ai register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer Ai register, it is written only to the reload register. (Transferred to the counter at the next reload time.)

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**
Note: A trigger occurs when the count start flag = "1."

EOL announced

b7	b6	b5	b4	b3	b2	b1	b0
		0			1	1	0

Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 1 0: One-shot pulse mode	0	RW
1			0	RW
2	Must be fixed to “1” in the one-shot pulse mode.		0	RW
3	Trigger selection bits	b4 b3 0 X: Writing “1” to the one-shot start flag (Pin TAi_{IN} functions as a programmable I/O port.) 1 0: Falling edge of the pin TAi_{IN}’s input signal 1 1: Rising edge of the pin TAi_{IN}’s input signal	0	RW
4			0	RW
5	Must be fixed to “0” in the one-shot pulse mode.		0	RW
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **“14. CLOCK GENERATING CIRCUIT.”**

(b15) b7 (b8) b0 b7 b0

Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, “H” level width of the one-shot pulse output from pin TAi_{OUT} is n/fi.	Undefined	WO

fi: Frequency of the count source (f_2, f_{16}, f_{64}, or f_{512})

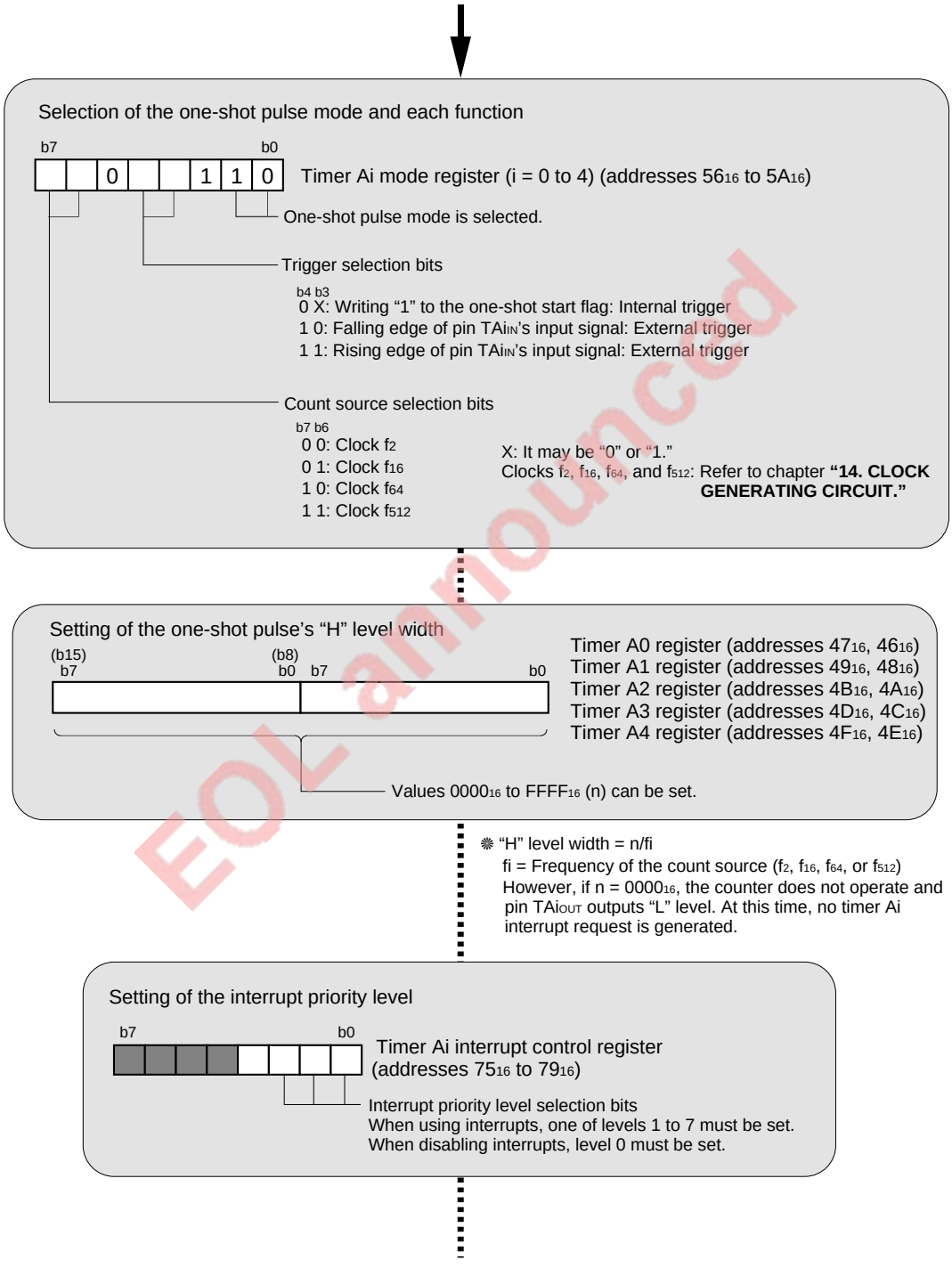
EOL announced

Fig. 6.5.1 Structures of timer Ai mode register and timer Ai register in one-shot pulse mode

6.5 One-shot pulse mode

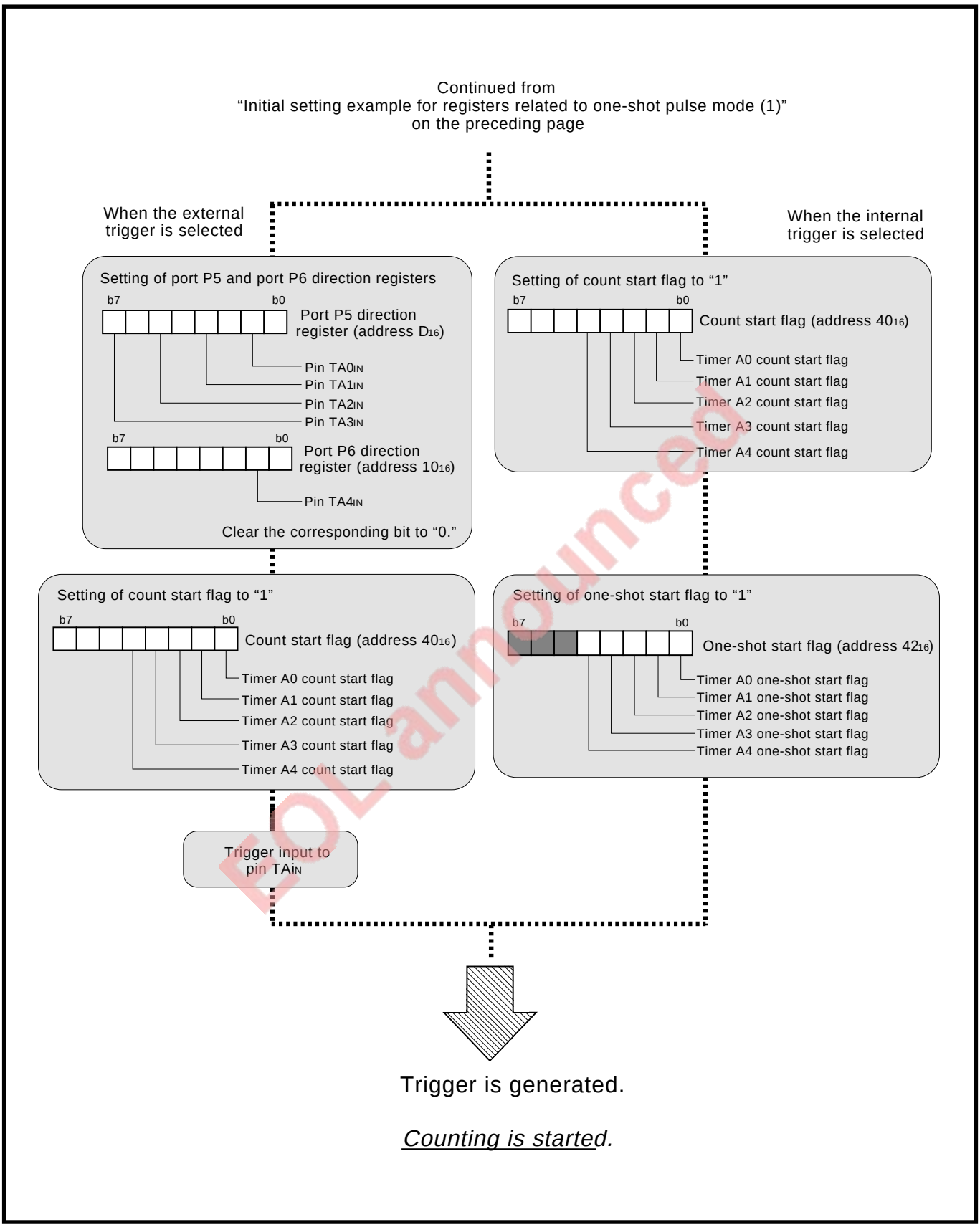
6.5.1 Setting for one-shot pulse mode

Figures 6.5.2 and 6.5.3 show an initial setting example for registers related to the one-shot pulse mode. Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**



EOL announced

Fig. 6.5.2 Initial setting example for registers related to one-shot pulse mode (1)



EOL announced

Fig. 6.5.3 Initial setting example for registers related to one-shot pulse mode (2)

6.5 One-shot pulse mode

6.5.2 Count source

In the one-shot pulse mode, by the count source selection bits (bits 7 and 6 at addresses 56_{16} to $5A_{16}$), a count source can be selected. Table 6.5.2 lists the relationship between the count source selection bits and count source.

Table 6.5.2 Relationship between count source selection bits and count source

b7	b6	Count source	Frequency of count source		
			When system clock = 25 MHz	When system clock = 16 MHz	When system clock = 8 MHz
0	0	f_2	12.5 MHz	8 MHz	4 MHz
0	1	f_{16}	1.5625 MHz	1 MHz	500 kHz
1	0	f_{64}	390.625 kHz	250 kHz	125 kHz
1	1	f_{512}	48.8281 kHz	31.25 kHz	15.625 kHz

Clocks f_2, f_{16}, f_{64}, f_{512} and system clock: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0" and the main clock division selection bit (bit 0 at address $6F_{16}$) = "0." (For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)

EOL announced

6.5.3 Trigger

The counter enters the count enable state when the count start flag (address 40_{16}) is set to "1." And then, the counter starts counting when a trigger occurs. An internal or external trigger can be selected as this trigger.

An internal trigger is selected when the trigger selection bits (bits 4 and 3 at addresses 56_{16} to $5A_{16}$) are "00_2" or "01_2"; an external trigger is selected when the trigger selection bits are "10_2" or "11_2."

When a trigger occurs during counting, the reload register's contents is reloaded and the counter continues counting. When generating a trigger during counting, make sure that a certain time which is equivalent to two cycles of the timer's count source or more has passed between the trigger previously generated and a new trigger.

(1) When internal trigger is selected

A trigger is generated when the one-shot start flag (address 42_{16}) is set to "1." Figure 6.5.4 shows the structure of the one-shot start flag.

(2) When external trigger is selected

A trigger is generated at the falling edge of pin TAiIN's input signal when bit 3 at addresses 56_{16} to $5A_{16}$ = "0" or at the rising edge of pin TAiIN's input signal when bit 3 = "1."

When using an external trigger, set the port P5 or P6 direction register's bit which corresponds to pin TAiIN's for the input mode.

EOL announced

One-shot start flag (address 42_{16})

Bit	Bit name	Functions	At reset	RW
0	Timer A0 one-shot start flag	1: One-shot pulse output is started. (Valid when the internal trigger is selected). "0" at reading.	0	WO
1	Timer A1 one-shot start flag		0	WO
2	Timer A2 one-shot start flag		0	WO
3	Timer A3 one-shot start flag		0	WO
4	Timer A4 one-shot start flag		0	WO
7 to 5	Not implemented.		Undefined	–

Fig. 6.5.4 Structure of one-shot start flag

6.5 One-shot pulse mode

6.5.4 Operation in one-shot pulse mode

① When the one-shot pulse mode is selected by the operating mode selection bits, pin TAiOUT outputs "L" level.

② When the count start flag is set to "1," the counter enters the count enable state, and then it starts counting if a trigger occurs.

③ When the counter starts counting, pin TAiOUT's output level becomes "H." (However, if value "0000_{16}" is set in the timer Ai register, the counter does not operate and the output level of pin TAiOUT remains "L." Nor is a timer Ai interrupt request generated.)

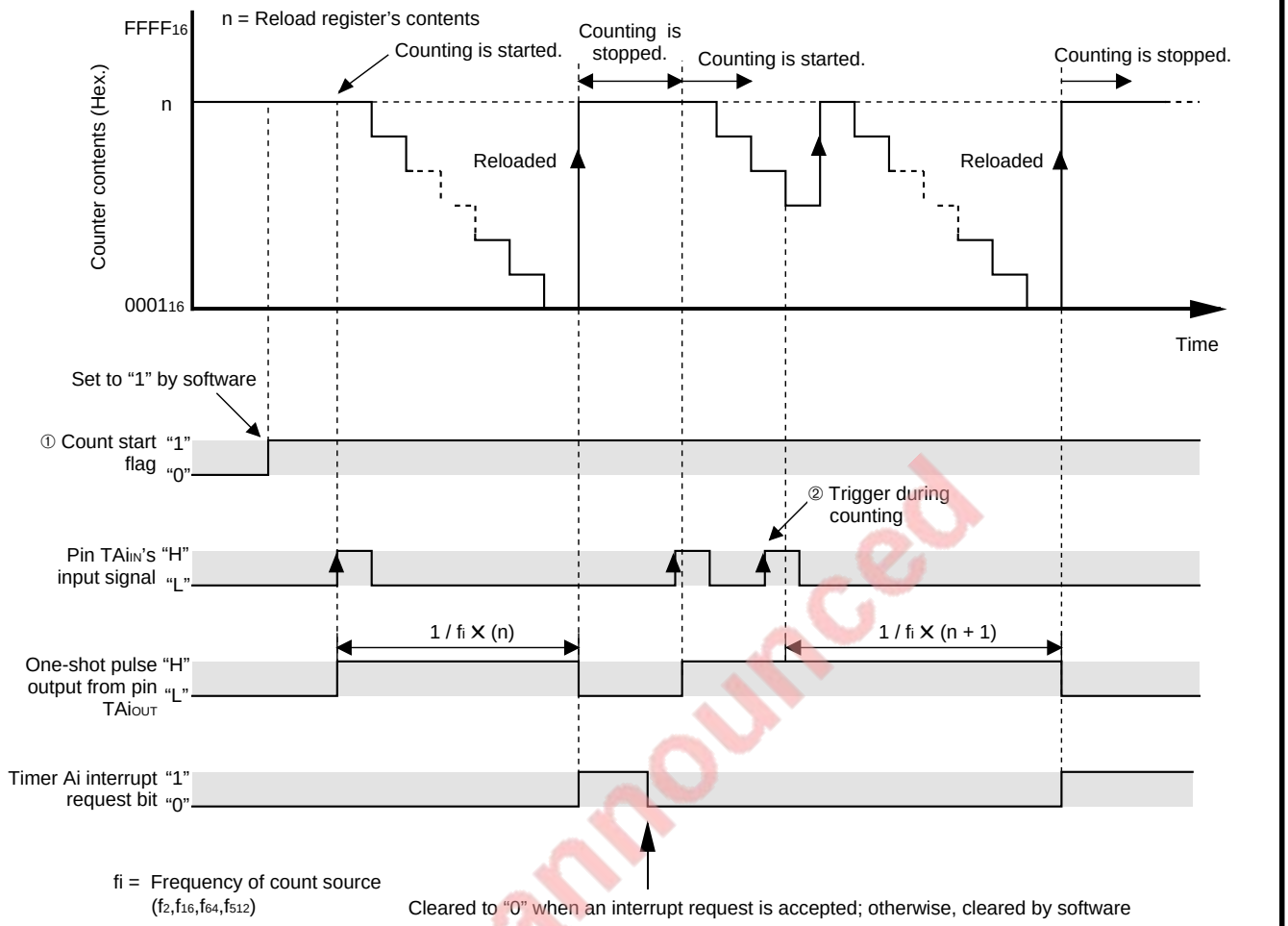
④ When the counter value reaches "0000_{16}," the output level of pin TAiOUT becomes "L." And then, the reload register's contents is reloaded, and the counter stops counting.

⑤ Simultaneously with ④, a timer Ai interrupt request bit is set to "1."
After this, the interrupt request bit remains set to "1" until the interrupt request is accepted or the interrupt request bit is cleared to "0" by software.

Figure 6.5.5 shows an operation example in the one-shot pulse mode.
When a trigger occurs after ④ above, the counter and pin TAiOUT perform the same operations beginning from ② again. When a trigger occurs during counting, the counter down-counts once after this new trigger occurs. And then, the reload register's contents is reloaded and counting is continued. When generating a trigger during counting, make sure that a certain time which is equivalent to two cycles of the timer's count source or more has passed between the trigger previously generated and a new trigger.

The one-shot pulse output from pin TAiOUT can be disabled by clearing the timer Ai mode register's bit 2 to "0." Therefore, timer Ai can be used as an internal one-shot timer that does not output the pulse. (In this case, pin TAiOUT functions as a programmable I/O port.)

EOL announced



EOL announced

Fig. 6.5.5 Operation example in one-shot pulse mode (when external trigger selected)

6.5 One-shot pulse mode

[Precautions in one-shot pulse mode]

1. When the count start flag is cleared to “0” during counting, the followings are performed.
   •The counter stops counting, and the reload register’s contents is reloaded.
   •Pin TAiOUT’s output level becomes “L.”
   •An interrupt request is generated, and a timer Ai interrupt request bit is set to “1.”

2. A one-shot pulse is output synchronously with an internally generated count source. Therefore, when an external trigger is selected, in the period from when a trigger is input to pin TAiIN until a one-shot pulse is output, there will be a delay equivalent to one cycle of the count source at maximum.

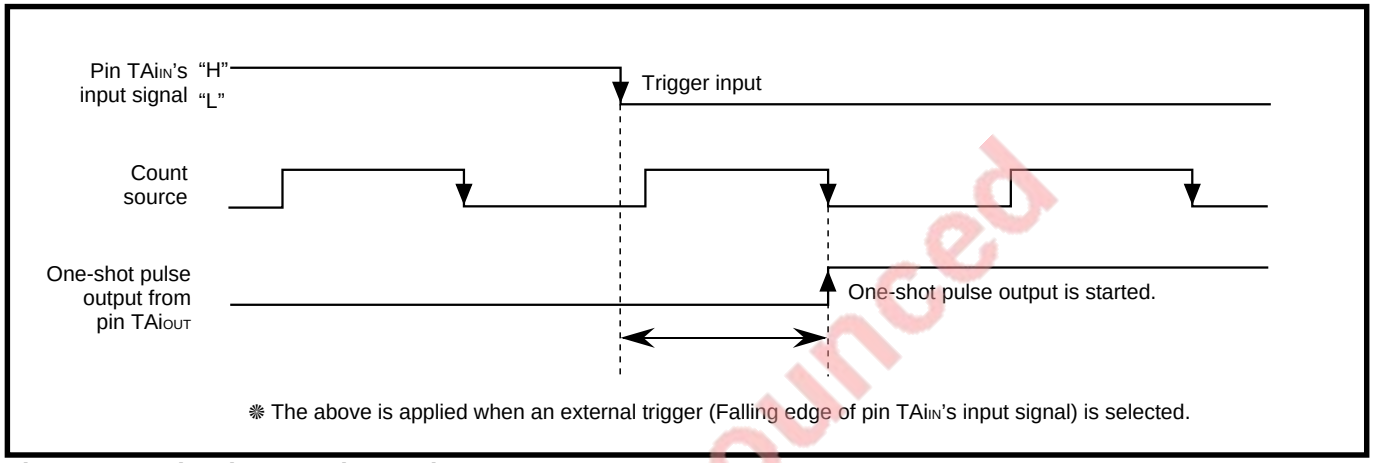


Fig. 6.5.6 Delay in one-shot pulse output

3. When a timer’s operating mode is set by the procedure listed below, a timer Ai interrupt request bit is set to “1.”
   - When the one-shot pulse mode is selected after reset
   - When the operating mode is switched from the timer mode to the one-shot pulse mode
   - When the operating mode is switched from the event counter mode to the one-shot pulse mode

   Therefore, when using a timer Ai interrupt (Interrupt request bit), be sure to clear the timer Ai interrupt request bit to “0” after setting the above.

EOL announced

6.6 Pulse width modulation (PWM) mode (Bits 1 and 0 of timer Ai mode register = "11_2")

In this mode, a pulse which has an arbitrary width is output in succession. (Refer to **Table 6.6.1.**) Figure 6.6.1 shows the structures of the timer Ai mode register and timer Ai register in the PWM mode.

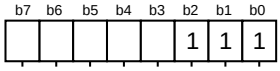
Table 6.6.1 Specifications of PWM mode

Item	Specifications
Count source	Clock f_2, f_{16}, f_{64}, or f_{512}
Count operation	● Countdown (Operates as an 8-bit or 16-bit pulse width modulator) ● Reload register's contents is reloaded at the rising edge of PWM pulse, and counting is continued. ● A trigger generated during counting does not affect the counting.
PWM period and "H" level width	<16-bit pulse width modulator> Period = $\frac{2^{16} - 1}{fi}$ [s] "H" level width = $\frac{K}{fi}$ [s] K: Set value in the timer Ai register <8-bit pulse width modulator> Period = $\frac{(m + 1)(2^8 - 1)}{fi}$ [s] "H" level width = $\frac{n(m + 1)}{fi}$ [s] m: Set value in the low-order 8 bits of the timer Ai register n: Set value in the high-order 8 bits of the timer Ai register
Count start condition	● When a trigger occurs. ● Internal or external trigger can be selected by software.
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	At the falling edge of PWM pulse
Pin TAi_{IN}'s function	Programmable I/O port or trigger input
Pin TAi_{OUT}'s function	PWM pulse output
Read from timer	An undefined value is read out by reading the timer Ai register.
Write to timer	■ While counting is stopped When a value is written to the timer Ai register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer Ai register, it is written only to the reload register.

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

EOL announced

6.6 Pulse width modulation (PWM) mode

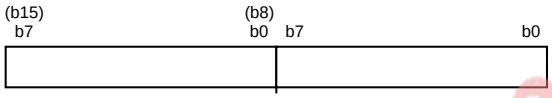


Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 1 1: PWM mode	0	RW
1			0	RW
2	Must be fixed to "1" in the PWM mode.		0	RW
3	Trigger selection bits	b4 b3 0 X: Writing "1" to the count start flag (Pin TAi_{IN} functions as a programmable I/O port.) 1 0: Falling edge of the pin TAi_{IN}'s input signal 1 1: Rising edge of the pin TAi_{IN}'s input signal	0	RW
4			0	RW
5	16/8-bit PWM mode selection bit	0: The counter operates as a 16-bit pulse width modulator. 1: The counter operates as an 8-bit pulse width modulator.	0	RW
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

■ When operating as a 16-bit pulse width modulator

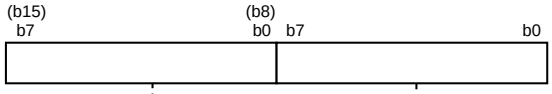


Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFE_{16}$ can be set. Assuming that the set value = n, "H" level width of the PWM pulse which is output from pin TAi_{OUT} is n/fi.	Un-defined	WO

fi: Frequency of the count source (f_2, f_{16}, f_{64}, or f_{512})

■ When operating as an 8-bit pulse width modulator



Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
7 to 0	Values 00_{16} to FF_{16} can be set. Assuming that the set value = m, period of the PWM pulse which is output from pin TAi_{OUT} is $(m + 1)(2^8 - 1)$/fi.	Un-defined	WO
15 to 8	Values 00_{16} to FE_{16} can be set. Assuming that the set value = n, "H" level width of the PWM pulse which is output from pin TAi_{OUT} is n(m +1)/fi.	Un-defined	WO

fi: Frequency of the count source (f_2, f_{16}, f_{64}, or f_{512})

EOL announced

Fig. 6.6.1 Structures of timer Ai mode register and timer Ai register in PWM mode

6.6.1 Setting for PWM mode

Figures 6.6.2 and 6.6.3 show an initial setting example for registers related to the PWM mode.
Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**

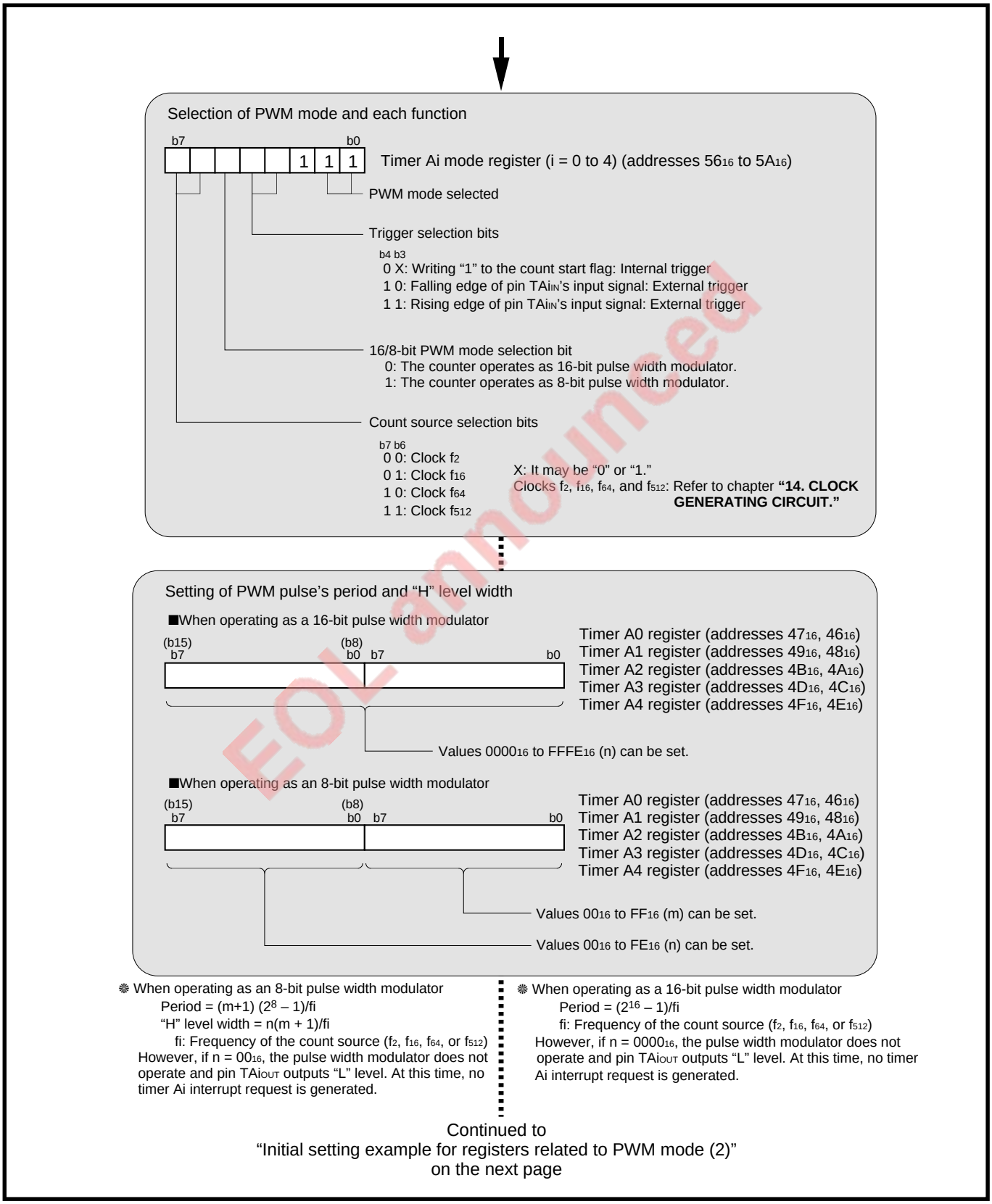


Fig. 6.6.2 Initial setting example for registers related to PWM mode (1)

EOL announced

6.6 Pulse width modulation (PWM) mode

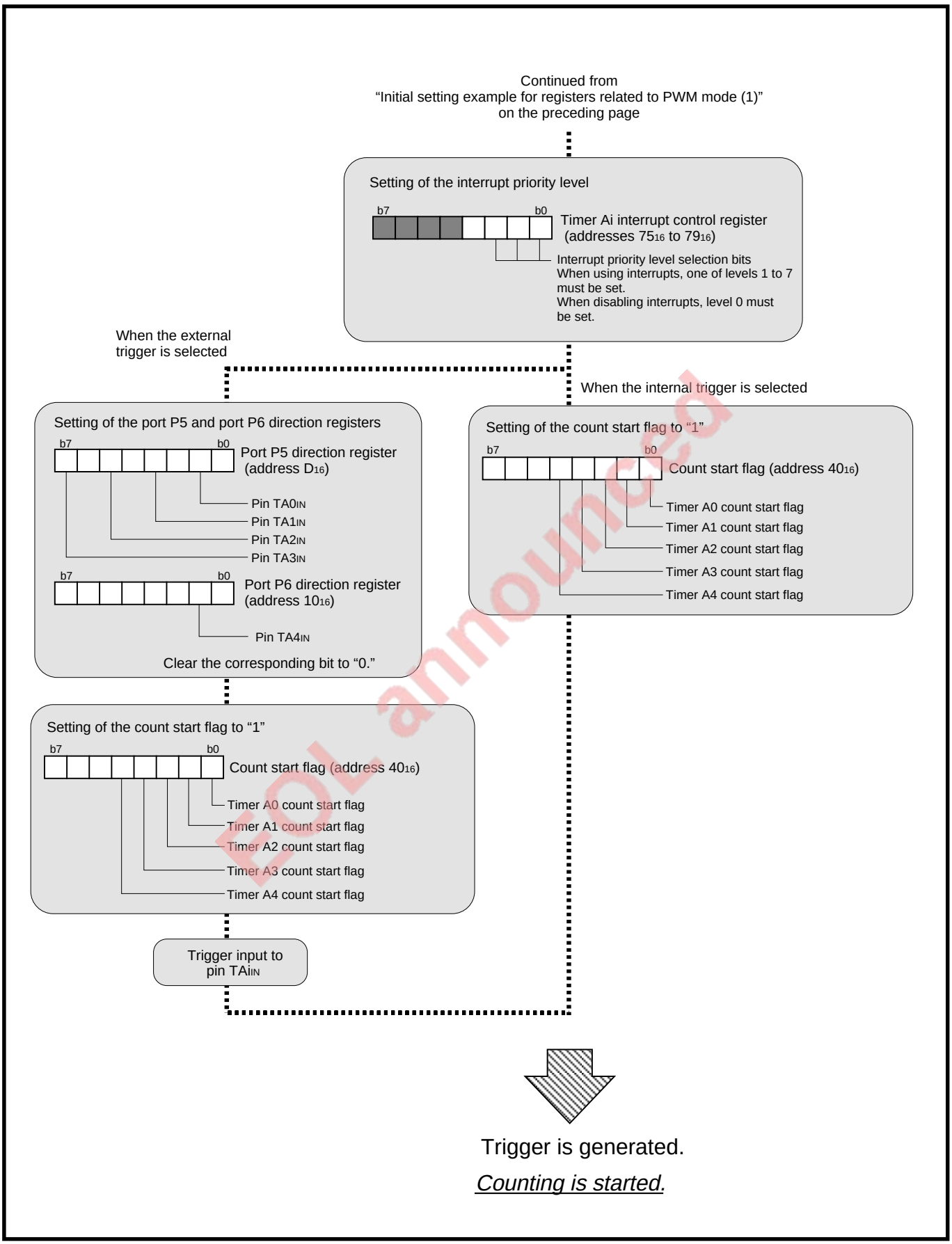


Fig. 6.6.3 Initial setting example for registers related to PWM mode (2)

FDL announced

6.6.2 Count source

In the PWM mode, by the count source selection bits (bits 7 and 6 at addresses 56_{16} to $5A_{16}$), a count source can be selected. Table 6.6.2 lists the relationship between the count source selection bits and count source.

Table 6.6.2 Relationship between count source selection bits and count source

b7	b6	Count source	Frequency of count source		
			When system clock = 25 MHz	When system clock = 16 MHz	When system clock = 8 MHz
0	0	f_2	12.5 MHz	8 MHz	4 MHz
0	1	f_{16}	1.5625 MHz	1 MHz	500 kHz
1	0	f_{64}	390.625 kHz	250 kHz	125 kHz
1	1	f_{512}	48.8281 kHz	31.25 kHz	15.625 kHz

Clocks f_2, f_{16}, f_{64}, f_{512}, and system clock: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0" and the main clock division selection bit (bit 0 at address $6F_{16}$) = "0." (For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)

EOL announced

6.6 Pulse width modulation (PWM) mode

6.6.3 Trigger

When a trigger occurs, pin TAiOUT starts the PWM pulse output. An internal or external trigger can be selected as this trigger.

An internal trigger is selected when the trigger selection bits (bits 4 and 3 at addresses 56_{16} to $5A_{16}$) are "00_2" or "01_2"; an external trigger is selected when the trigger selection bits are "10_2" or "11_2."

A trigger generated during PWM pulse output is invalid and does not affect the pulse output operation.

(1) When internal trigger is selected

A trigger is generated when the count start flag (address 40_{16}) is set to "1."

(2) When external trigger is selected

A trigger is generated at the falling edge of the pin TAiIN's input signal when bit 3 at addresses 56_{16} to $5A_{16}$ = "0" or at the rising edge of the pin TAiIN's input signal when bit 3 = "1." However, a trigger input is accepted only when the count start flag = "1."

When using an external trigger, set the port P5 or P6 direction register's bit which corresponds to pin TAiIN for the input mode.

EOL announced

6.6.4 Operation in PWM mode

① When the PWM mode is selected by the operating mode selection bits, pin TAiOUT outputs "L" level.
② When a trigger occurs, the counter (Pulse width modulator) starts counting and pin TAiOUT outputs a PWM pulse (**Notes 1 and 2**).
③ A timer Ai interrupt request bit is set to "1" each time the PWM pulse level changes from "H" to "L." After this, the interrupt request bit remains set to "1" until the interrupt request is accepted or the interrupt request bit is cleared to "0" by software.
④ Each time a PWM pulse is output for one period, the reload register's contents is reloaded and counting is continued.

Operation of the pulse width modulator is described below.

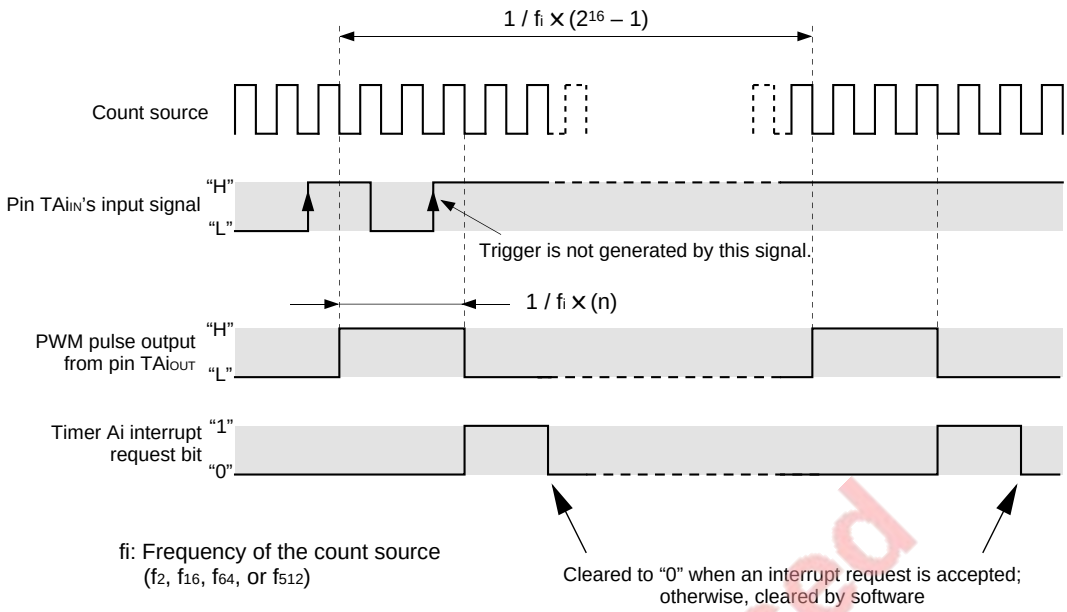
[16-bit pulse width modulator]
When the 16/8-bit PWM mode selection bit is set to "0," the counter operates as a 16-bit pulse width modulator. Each of Figures 6.6.4 and 6.6.5 shows an operation example of the 16-bit pulse width modulator.

[8-bit pulse width modulator]
When the 16/8-bit PWM mode selection bit is set to "1," the counter is divided into 8-bit halves. Then, the high-order 8 bits operate as an 8-bit pulse width modulator, and the low-order 8 bits operate as an 8-bit prescaler. Each of Figures 6.6.6 and 6.6.7 shows an operation example of the 8-bit pulse width modulator.

Notes 1: If a value of "0000_{16}" is set in the timer Ai register when the counter operates as a 16-bit pulse width modulator, the pulse width modulator does not operate and the output level of pin TAiOUT remains "L." Nor is a timer Ai interrupt request generated. These operations are also applied to the case where a value of "00_{16}" is set in high-order 8 bits of the timer Ai register when the counter operates as an 8-bit pulse width modulator.
2: When the counter operates as an 8-bit pulse width modulator, after a trigger occurs, pin TAiOUT outputs "L" level of which width is the same as the PWM pulse's "H" level width which was set. And then, pin TAiOUT starts the PWM pulse output.

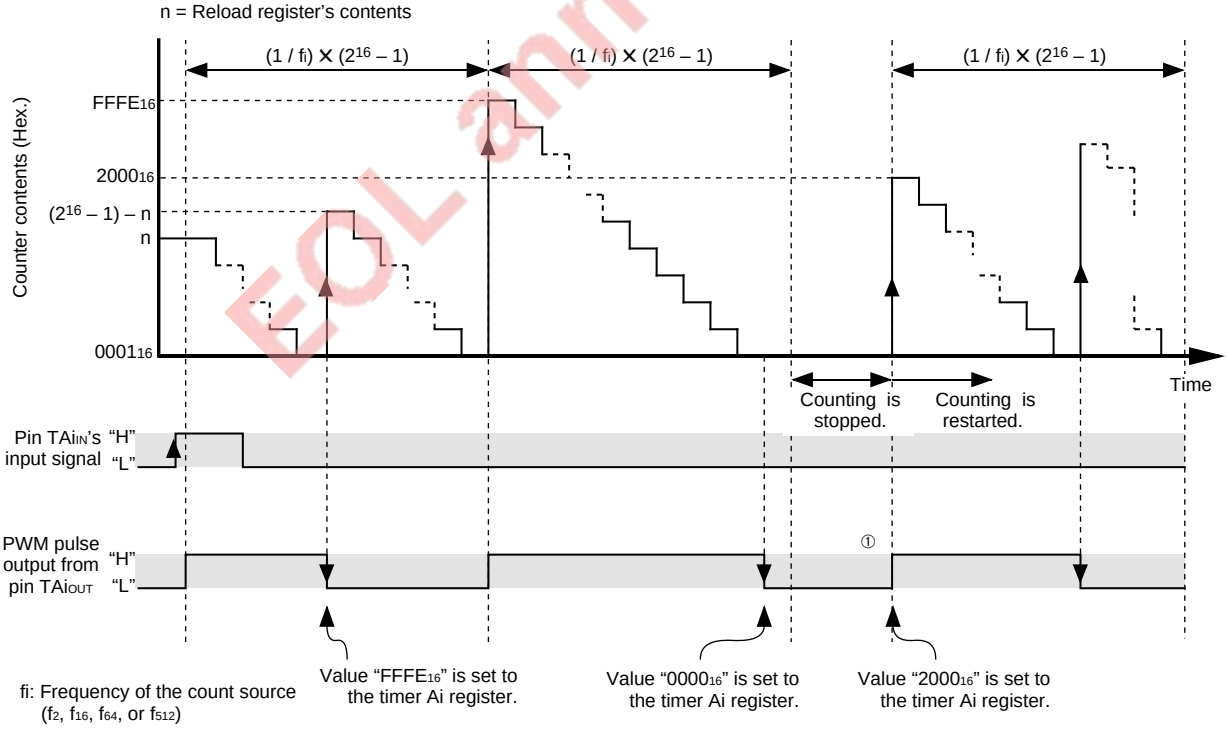
EOL announced

6.6 Pulse width modulation (PWM) mode



✵ The above is applied when the reload register = 0003_{16} and an external trigger (Rising edge of pin TAiIN's input signal) is selected.

Fig. 6.6.4 Operation example of 16-bit pulse width modulator



① When an arbitrary value is reset to the timer Ai register after value "0000_{16}" is set to it, the rising timing of PWM pulse depends on this reset timing.

✵ The above is applied when an external trigger (Rising edge of pin TAiIN's input signal) is selected.

Fig. 6.6.5 Operation example of 16-bit pulse width modulator (when counter value is updated during pulse output)

EOL announced

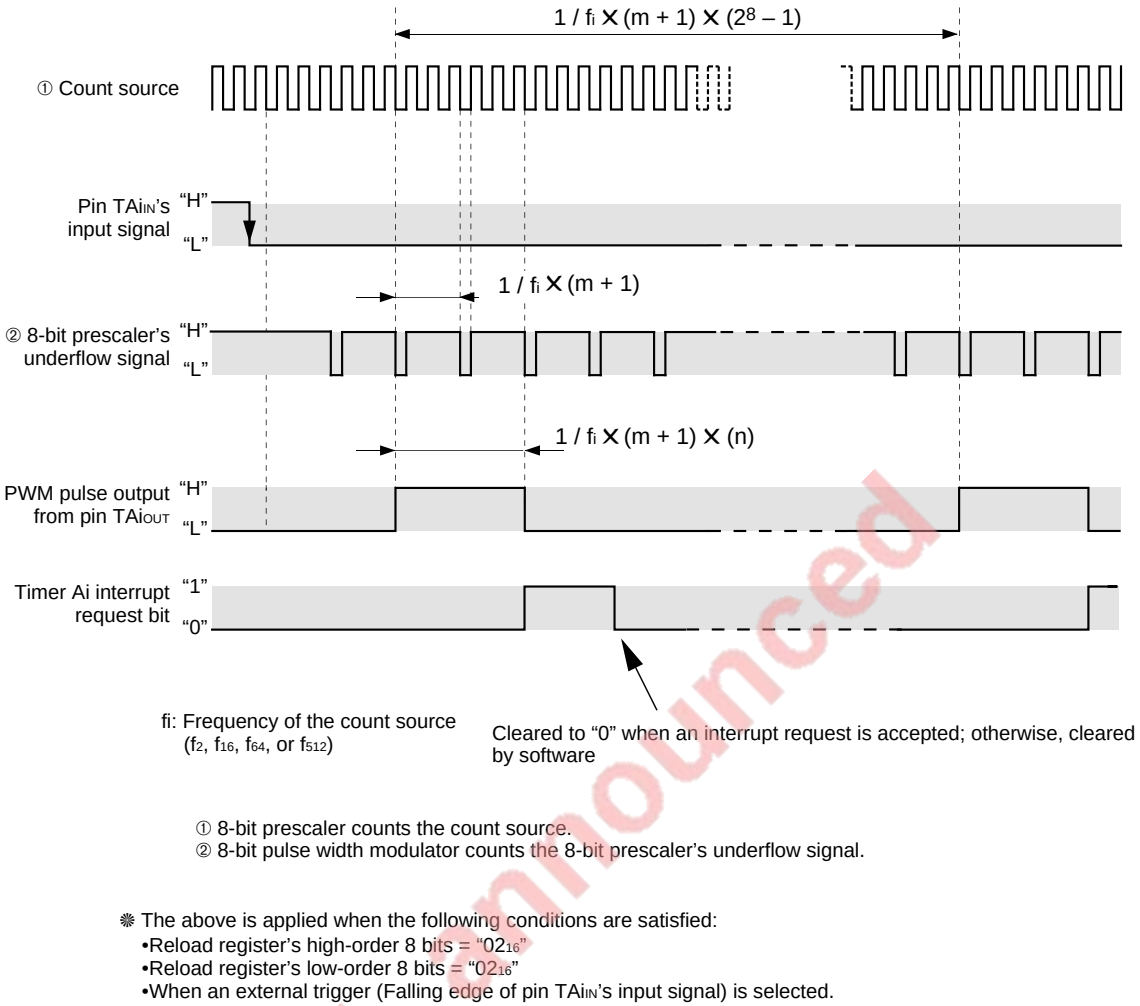
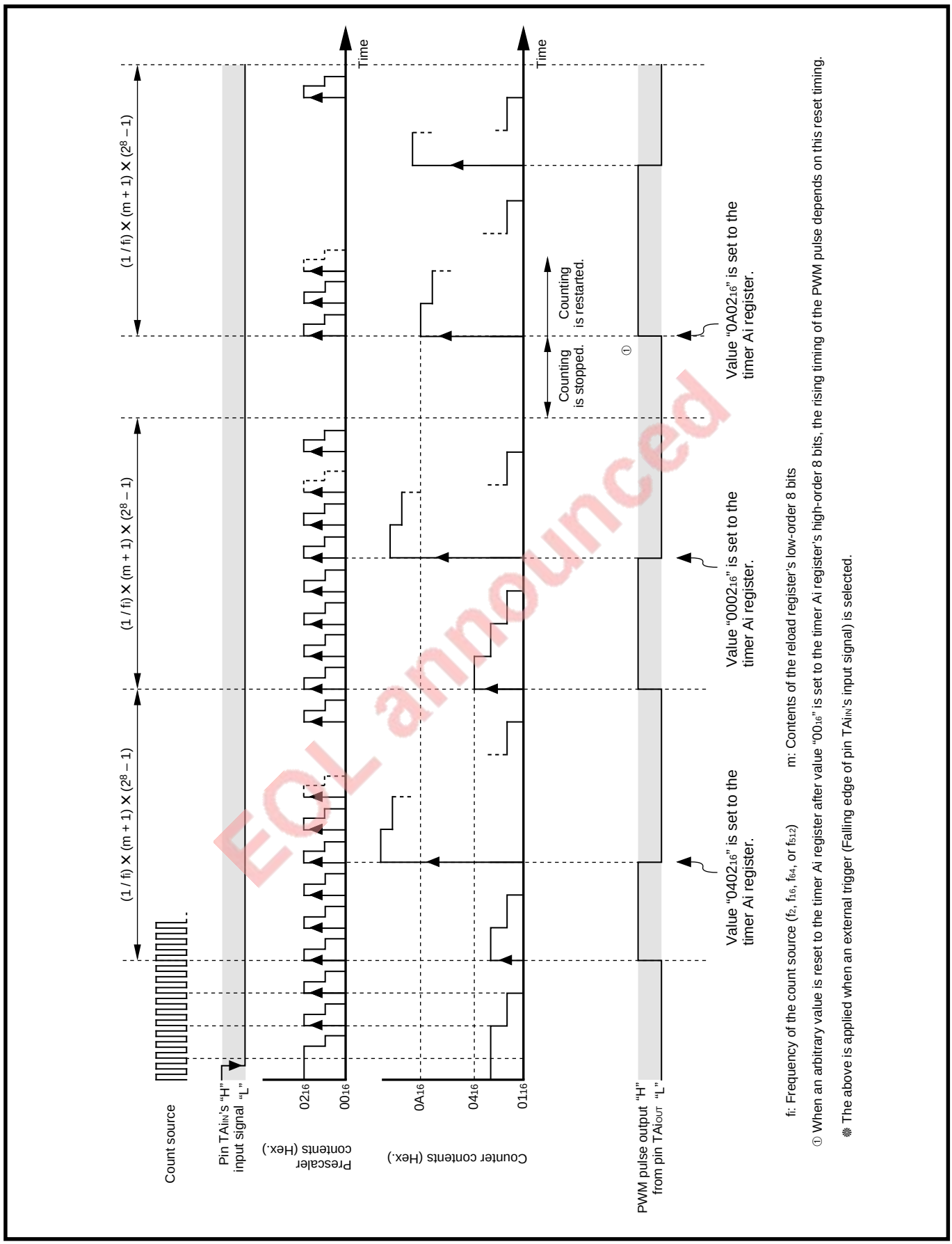


Fig. 6.6.6 Operation example of 8-bit pulse width modulator

EOL announced

6.6 Pulse width modulation (PWM) mode



EOL announced

Fig. 6.6.7 Operation example of 8-bit pulse width modulator (when counter value is updated during pulse output)

[Precautions in PWM mode]

1. When the count start flag is cleared to “0” while a PWM pulse is output, the counter stops counting. At this time, if pin TAiOUT outputs “H” level, the output level becomes “L” and a timer Ai interrupt request bit is set to “1.” If pin TAiOUT outputs “L” level, the output level does not change and a timer Ai interrupt request is not generated.

2. When a timer’s operating mode is set by the procedure listed below, a timer Ai interrupt request bit is set to “1.”
   - When the PWM mode is selected after reset
   - When the operating mode is switched from the timer mode to the PWM mode
   - When the operating mode is switched from the event counter mode to the PWM mode

   Therefore, when using a timer Ai interrupt (Interrupt request bit), be sure to clear the timer Ai interrupt request bit to “0” after setting the above.

EOL announced

MEMO

EOL announced

CHAPTER 7

TIMER B

7.1 Overview
7.2 Block description
7.3 Timer mode
7.4 Event counter mode
7.5 Pulse period/Pulse width measurement mode
7.6 Clock timer

EOL announced

TIMER B

7.1 Overview

Timer B consists of three counters (Timers B0 to B2), and each has a 16-bit reload function. Timers B0 to B2 operate independently of each other.

Timer Bi (i = 0 to 2) has three operating modes listed below. Furthermore, timer B2 can function as a clock timer. Except that timer B2 functions as a clock timer and timer B1 has an internal connect function, timers B0 to B2 have the same functions.

■ Timer mode
Timer B counts a count source internally generated.

■ Event counter mode
Timer B counts an external signal, and the following functions can be used:
● Internal connect function (Timer B1 only)

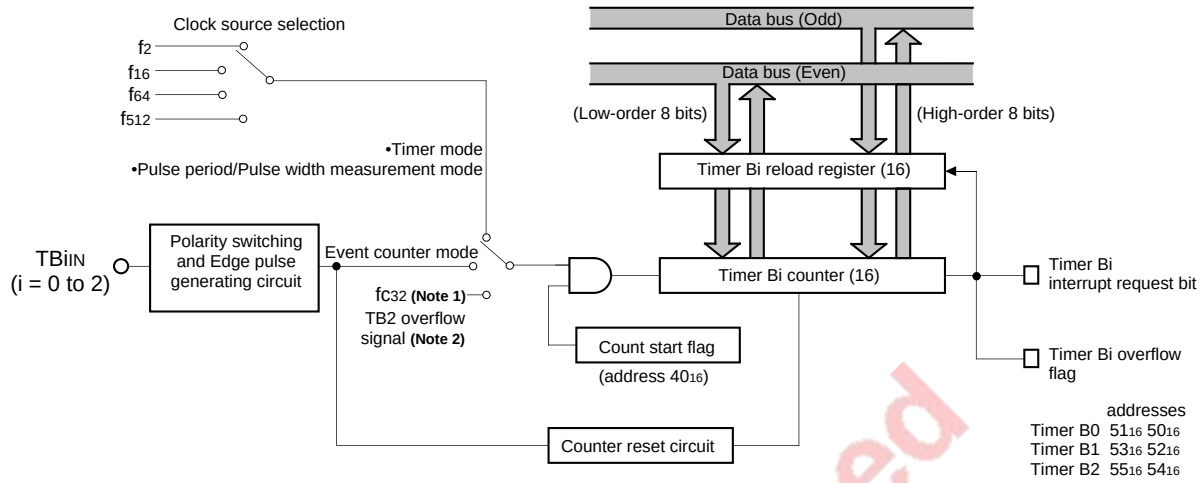
■ Pulse period/Pulse width measurement mode
Timer B measures an external signal's pulse period/pulse width.

■ Clock timer (Timer B2)

EOL announced

7.2 Block description

Figure 7.2.1 shows the timer B block diagram. Registers related to timer B are described below.



Notes 1: Clock source for clock timer
Can be selected only for TB2 (Refer to **Figure 14.3.1.**)
2: Can be selected only for TB1 (Internal connect mode)

Clocks f_2, f_{16}, f_{64}, and f_{512} : Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Fig. 7.2.1 Timer B block diagram

EOL announced

TIMER B

7.2 Block description

7.2.1 Counter and Reload register (Timer Bi register)

Each of timer Bi counter and its reload register consists of 16 bits and has the following functions.

(1) Functions in timer mode, event counter mode, and clock timer

The counter performs countdown each time a count source is input. The reload register is used to memorize the initial value of a counter. When an underflow occurs in the counter, the reload register's contents is reloaded into the counter.

Values are set to the counter and reload register by writing the values to the timer Bi register. Table 7.2.1 lists the memory allocation of the timer Bi register.

A value written into the timer Bi register while counting is stopped is set to the counter and reload register. A value written into the timer Bi register while counting is in progress is set only to the reload register. In this case, the reload register's updated contents is transferred to the counter when the next underflow occurs. A value obtained by reading out the timer Bi register is the counter value.

Note: Perform reading or writing from/to the timer Bi register by the 16 bits. For a value read from the timer Bi register, refer to **"Precautions in timer mode"** and **"Precautions in event counter mode."**

(2) Functions in pulse period/pulse width measurement mode

The counter performs countup each time a count source is input. The reload register is used to hold the pulse period or pulse width measurement result. When a valid edge is input to pin TBi_{IN}, the counter value is transferred to the reload register. In this mode, a value obtained by reading out the timer Bi register is the reload register's contents, and the measurement result can be obtained.

Note: Perform reading from the timer Bi register by the 16 bits.

Table 7.2.1 Memory allocation of timer Bi register

Timer Bi register	High-order byte	Low-order byte
Timer B0 register	Address 51_{16}	Address 50_{16}
Timer B1 register	Address 53_{16}	Address 52_{16}
Timer B2 register	Address 55_{16}	Address 54_{16}

Note: At reset, the contents of the timer Bi register is undefined.

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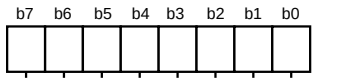
7.2.2 Count start flag

This register is used to start or stop counting. Each bit of this register corresponds to each timer, respectively. Figure 7.2.2 shows the structure of the count start flag.



Count start flag (address 40_{16})

Bit	Bit name	Functions	At reset	RW
0	Timer A0 count start flag	0: Counting is stopped. 1: Counting is started.	0	RW
1	Timer A1 count start flag		0	RW
2	Timer A2 count start flag		0	RW
3	Timer A3 count start flag		0	RW
4	Timer A4 count start flag		0	RW
5	Timer B0 count start flag		0	RW
6	Timer B1 count start flag		0	RW
7	Timer B2 count start flag		0	RW

represents that bits 0 to 4 are not used for timer B.

Fig. 7.2.2 Structure of count start flag

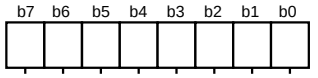
EOL announced

TIMER B

7.2 Block description

7.2.3 Timer Bi mode register

Figure 7.2.3 shows the structure of the timer Bi mode register. The operating mode selection bits are used to select an operating mode of timer Bi. Bits 7 to 5 and bits 3 and 2 have different functions according to the operating mode. These bits are described in a section of each operating mode.



Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode 0 1: Event counter mode 1 0: Pulse period/Pulse width measurement mode 1 1: Do not select.	0	RW
1			0	RW
2	These bits have different functions according to the operating mode.		0	RW
3			0	RW
4	Must be fixed to “0” (i = 0).		0	RW
	Not implemented (i = 1, 2).		Un-defined	—
5	These bits have different functions according to the operating mode.		Un-defined	RO **(Note)**
6			0	RW
7			0	RW

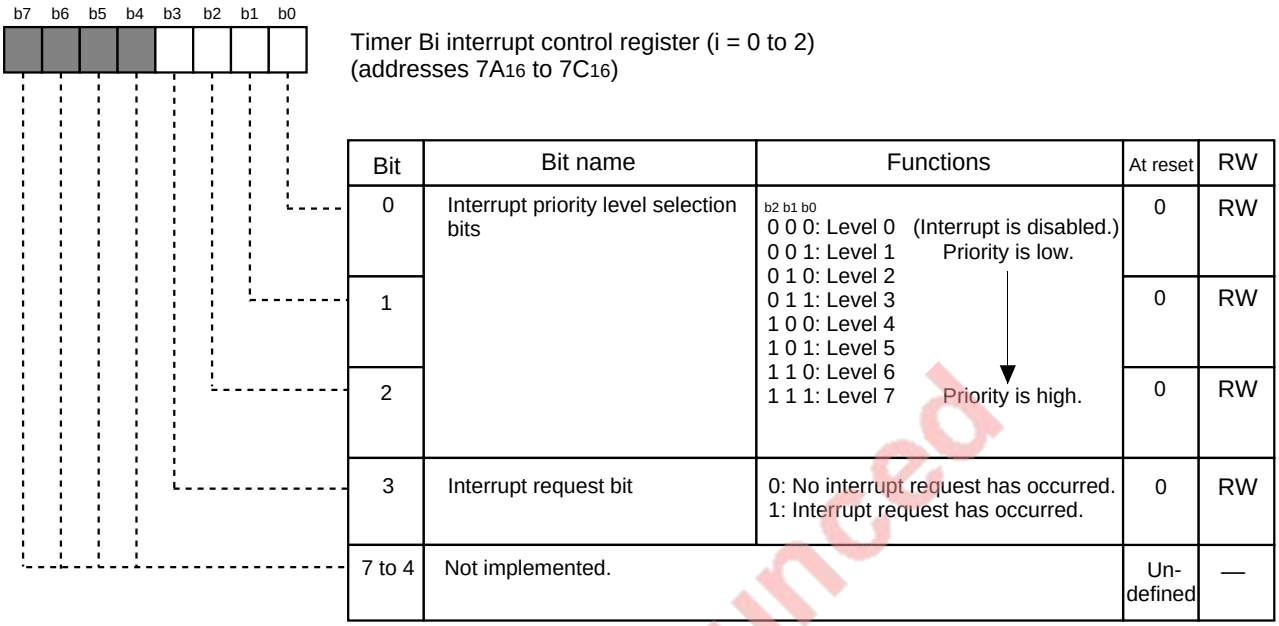
Note: In the timer and event counter modes, bit 5 is ignored and undefined at reading.

Fig. 7.2.3 Structure of timer Bi mode register

EOL announced

7.2.4 Timer Bi interrupt control register

Figure 7.2.4 shows the structure of the timer Bi interrupt control register. For details about interrupts, refer to chapter **"4. INTERRUPTS"**



Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2 b1 b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 Priority is low. 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7 Priority is high.	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
7 to 4	Not implemented.		Un-defined	—

Fig. 7.2.4 Structure of timer Bi interrupt control register

(1) Interrupt priority level selection bits (bits 2 to 0)

These bits select a timer Bi interrupt's priority level. When using timer Bi interrupts, select one priority level from levels 1 to 7. If a timer Bi interrupt request is generated, its priority level is compared with the processor interrupt priority level (IPL), and then the requested interrupt is enabled only when its priority level is higher than the IPL. (However, this is applied when the interrupt disable flag (I) = "0.") When disabling timer Bi interrupts, set these bits to "000_2" (Level 0).

(2) Interrupt request bit (bit 3)

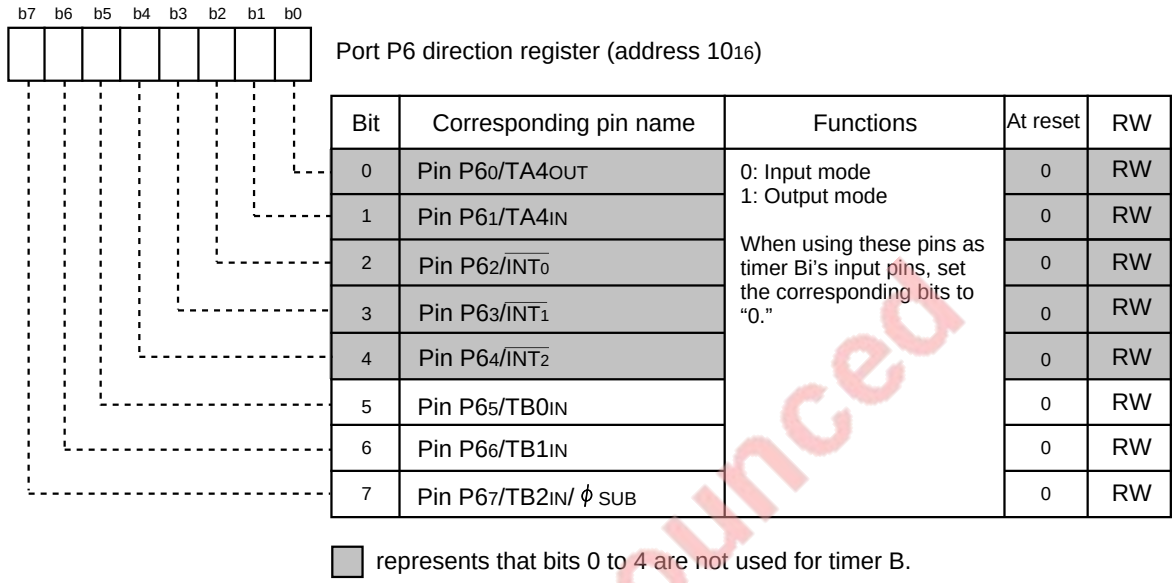
This bit is set to "1" when a timer Bi interrupt request is generated. This bit is automatically cleared to "0" when the timer Bi interrupt request is accepted. This bit can be set to "1" or cleared to "0" by software.

EOL announced

7.2 Block description

7.2.5 Port P6 direction register

I/O pins of timer Bi are multiplexed with port P6. When using these pins as timer Bi's input pins, set the corresponding bits of the port P6 direction register to "0" in order to set these ports for the input mode. Figure 7.2.5 shows the relationship between the port P6 direction register and the timer Bi's input pins.



Port P6 direction register (address 10_{16})

Bit	Corresponding pin name	Functions	At reset	RW
0	Pin $P6_0$/$TA4_{OUT}$	0: Input mode 1: Output mode When using these pins as timer Bi's input pins, set the corresponding bits to "0."	0	RW
1	Pin $P6_1$/$TA4_{IN}$		0	RW
2	Pin $P6_2$/$\overline{INT_0}$		0	RW
3	Pin $P6_3$/$\overline{INT_1}$		0	RW
4	Pin $P6_4$/$\overline{INT_2}$		0	RW
5	Pin $P6_5$/$TB0_{IN}$		0	RW
6	Pin $P6_6$/$TB1_{IN}$		0	RW
7	Pin $P6_7$/$TB2_{IN}$/ ϕ_{SUB}		0	RW

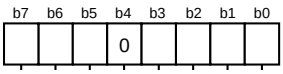
: represents that bits 0 to 4 are not used for timer B.

Fig. 7.2.5 Relationship between port P6 direction register and timer Bi's input pins

EOL announced

7.2.6 Port function control register

Figure 7.2.6 shows the structure of the port function control register.



Port function control register (address $6D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Standby state selection bit	0: Pins P0 to P3 are used for the external bus output. 1: Pins P0 to P3 are used for the port output.	0	RW
1	Sub-clock output selection bit/ Timer B2 clock source selection bit	•Port-Xc selection bit* = "0" (when the sub clock is not used) Timer B2 (event counter mode) clock source selection **(Note 1)** 0: $TB2_{IN}$ input (event counter mode) 1: Main clock divided by 32 (clock timer) •Port-Xc selection bit = "1" (when the sub clock is used) Sub-clock output selection 0: Pin $P6_7/TB2_{IN}/\phi_{SUB}$ functions as a programmable I/O port. 1: Sub clock ϕ_{SUB} is output from pin $P6_7/TB2_{IN}/\phi_{SUB}$.	0	RW
2	Timer B1 internal connect selection bit **(Note 2)**	0: No internal connection 1: Internal connection with timer B2	0	RW
3	Port P6 pull-up selection bit 0	0: No pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$ 1: With pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$	0	RW
4	Must be fixed to "0."		0	RW
5	Port P6 pull-up selection bit 1	•Key input interrupt selection bit = "0" 0: No pull-up for pin $P6_4/\overline{INT_2}$ 1: With pull-up for pin $P6_4/\overline{INT_2}$ •Key input interrupt selection bit = "1" 0: Pin $P6_4/\overline{INT_2}$ is a port with no pull-up. 1: Pin $P6_4/\overline{INT_2}$ is an input pin with pull-up and is used for the key input interrupt.	0	RW
6	Port P5 pull-up selection bit	0: No pull-up for pins $P5_4/TA2_{OUT}/\overline{KI_0}$ to $P5_7/TA3_{IN}/\overline{KI_3}$ 1: With pull-up for pins $P5_4/TA2_{OUT}/\overline{KI_0}$ to $P5_7/TA3_{IN}/\overline{KI_3}$	0	RW
7	Key input interrupt selection bit	0: $\overline{INT_2}$ interrupt ($TA2_{IN}$ and $TA3_{IN}$ inputs are assigned to pins $P5_5$ and $P5_7$.) 1: Key input interrupt ($TA2_{IN}$ and $TA3_{IN}$ inputs are assigned to pins $P7_2$ and $P7_3$.)	0	RW

Port-Xc selection bit* : Bit 4 of the oscillation circuit control register 0 (address $6C_{16}$)

Notes 1: When the port-Xc selection bit = "0" and timer B2 operates in the timer mode or the pulse period /pulse width measurement mode, bit 1 is invalid.
2: When timer B1 operates in the event counter mode, bit 2 is valid.
3: ☐ represents that bits 0 and 3 to 7 are not used for timer B.

Fig. 7.2.6 Structure of port function control register

EOL announced

7.3 Timer mode (Bits 1 and 0 of timer Bi mode register = "00$_2$")

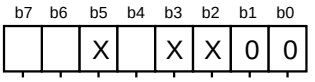
In this mode, a count source internally generated is counted. (Refer to **Table 7.3.1.**) Figure 7.3.1 shows the structures of the timer Bi mode register and timer Bi register in the timer mode.

Table 7.3.1 Specifications of timer mode

Item	Specifications
Count source	Clock f_2, f_{16}, f_{64}, or f_{512}
Count operation	● Countdown ● At an underflow, the reload register's contents is reloaded, and counting is continued.
Division ratio	$\frac{1}{(n+1)}$ n: Set value in the timer Bi register
Count start condition	When the count start flag is set to "1."
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	At an underflow
Pin TBi_{IN}'s function	Programmable I/O port (Pin $TB2_{IN}$ is a programmable I/O port or ϕ_{SUB} output pin.)
Read from timer	A counter value can be read out by reading the timer Bi register.
Write to timer	■ While counting is stopped When a value is written to the timer Bi register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer Bi register, it is written only to the reload register. (Transferred to the counter at the next reload time.)

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter "**14. CLOCK GENERATING CIRCUIT.**"

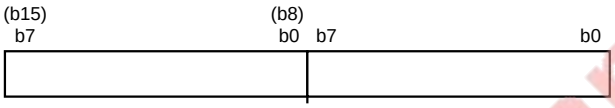
EOL announced



Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode	0	RW
1			0	RW
2	These bits are ignored in the timer mode.		0	RW
3			0	RW
4	•Timer B0 mode register Must be fixed to "0."		0	RW
	•Timer B1 and B2 mode registers Not implemented.		Un-defined	—
5	This bit is ignored in the timer mode and is undefined at reading.		Un-defined	RO
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**



Timer B0 register (addresses 51_{16}, 50_{16})
Timer B1 register (addresses 53_{16}, 52_{16})
Timer B2 register (addresses 55_{16}, 54_{16})

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Un-defined	RW

EOL announced

Fig. 7.3.1 Structures of timer Bi mode register and timer Bi register in timer mode

TIMER B

7.3 Timer mode

7.3.1 Setting for timer mode

Figure 7.3.2 shows an initial setting example for registers related to the timer mode.
Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**

EOL announced

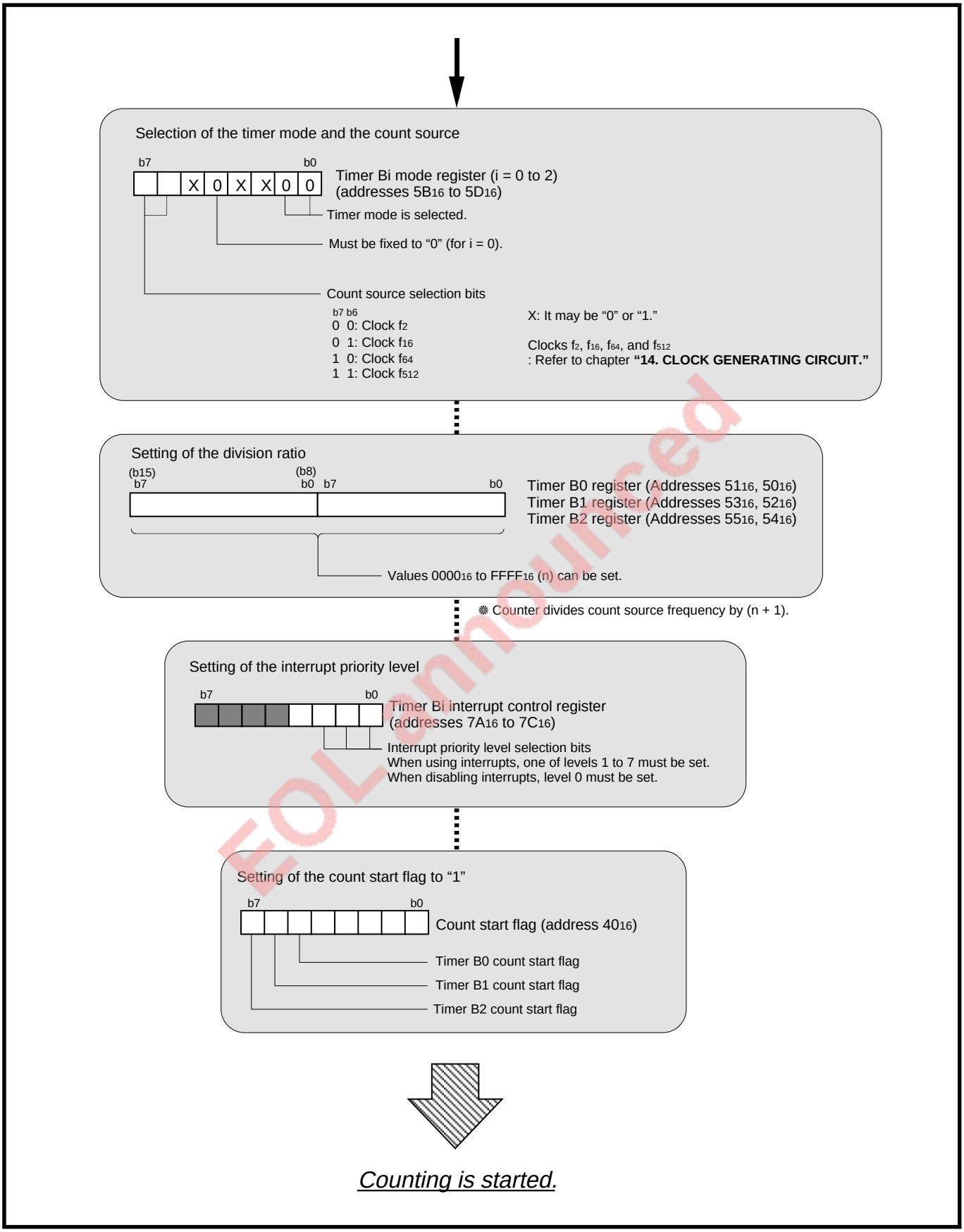


Fig. 7.3.2 Initial setting example for registers related to timer mode

EOL announced

7.3 Timer mode

7.3.2 Count source

In the timer mode, by the count source selection bits (bits 7 and 6 at addresses $5B_{16}$ to $5D_{16}$), a count source can be selected. Table 7.3.2 lists the relationship between the count source selection bits and count source.

Table 7.3.2 Relationship between count source selection bits and count source

b7	b6	Count source	Frequency of count source		
			When system clock = 25 MHz	When system clock = 16 MHz	When system clock = 8 MHz
0	0	f_2	12.5 MHz	8 MHz	4 MHz
0	1	f_{16}	1.5625 MHz	1 MHz	500 kHz
1	0	f_{64}	390.625 kHz	250 kHz	125 kHz
1	1	f_{512}	48.8281 kHz	31.25 kHz	15.625 kHz

Clocks f_2, f_{16}, f_{64}, f_{512}, and system clock: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0" and the main clock division selection bit (bit 0 at address $6F_{16}$) = "0." (For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)

EOL announced

7.3.3 Operation in timer mode

① When the count start flag is set to “1,” the counter starts counting of the count source.
② When an underflow occurs, the reload register’s contents is reloaded, and then counting is continued.
③ The timer Bi interrupt request bit is set to “1” when the underflow occurs in ②.
After this, the interrupt request bit remains set to “1” until the interrupt request is accepted or the interrupt request bit is cleared to “0” by software.

Figure 7.3.3 shows an operation example in the timer mode.

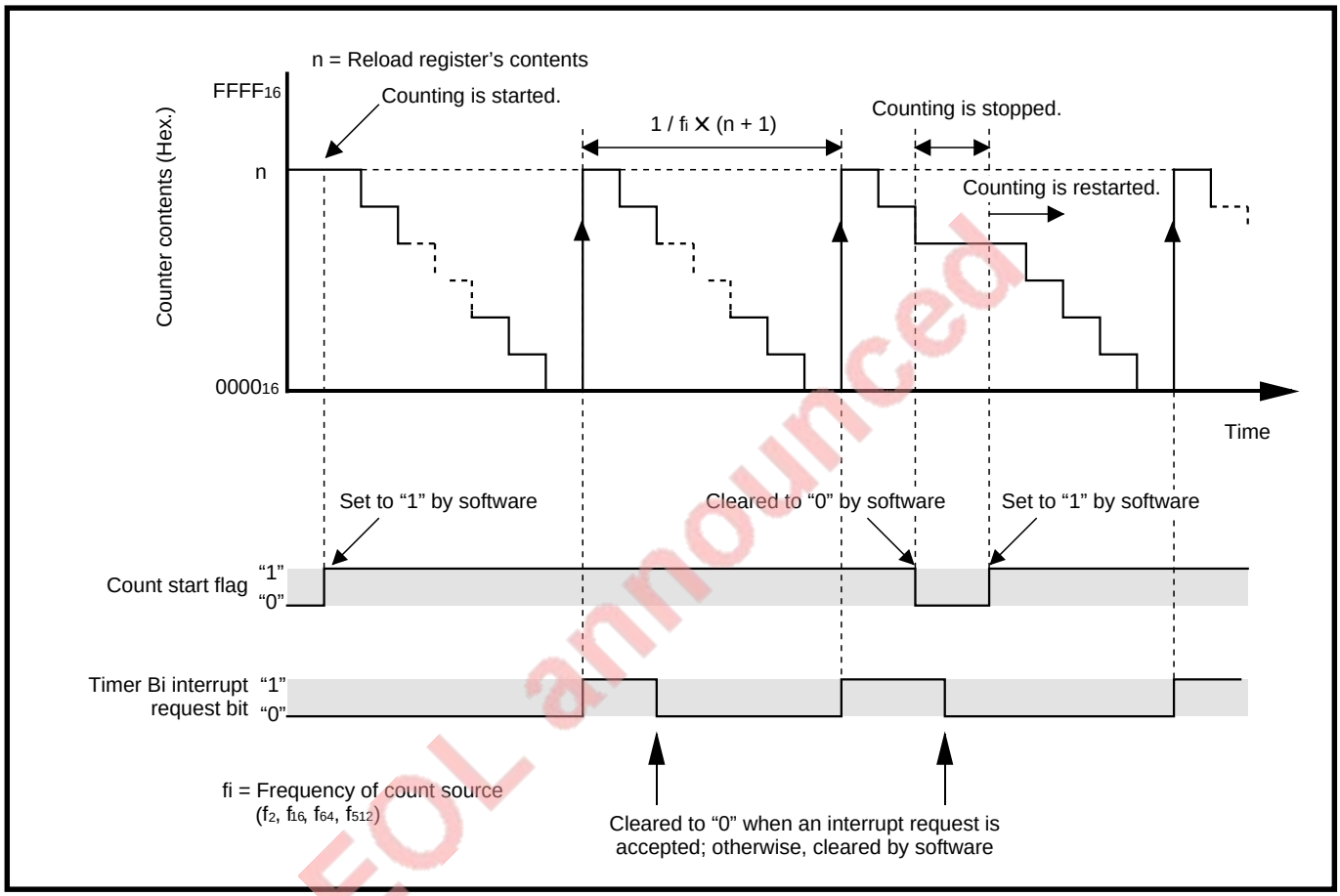


Fig. 7.3.3 Operation example in timer mode

EOL announced

7.3 Timer mode

[Precautions in timer mode]

While counting is in progress, by reading out the timer Bi register, the counter value can be read at an arbitrary timing. However, when reading is performed at the reload timing shown in Figure 7.3.4, value "FFFF$_{16}$" is read out. If reading is performed in the period from when a value is set into the timer Bi register with the counter stopped until the counter starts counting, the set value is correctly read out.

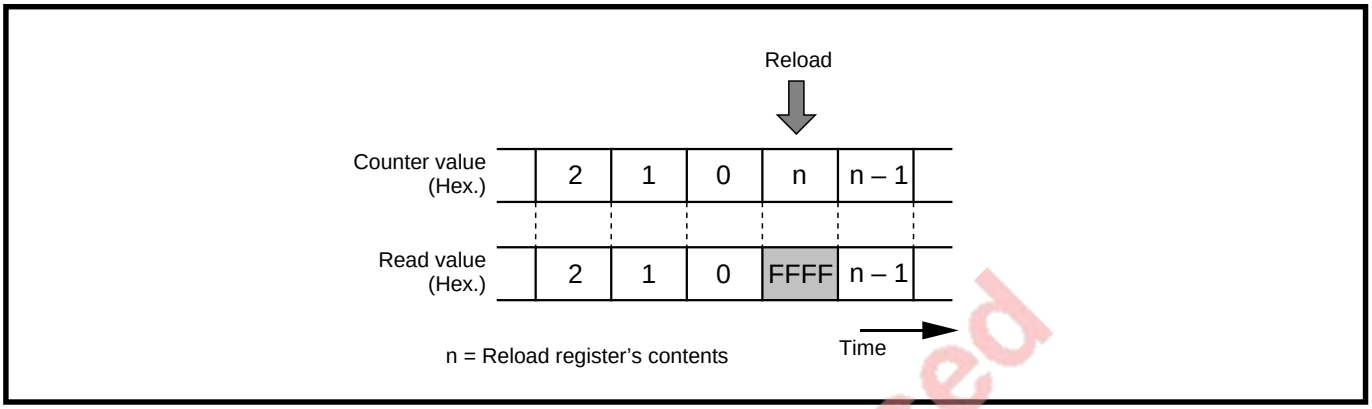


Fig. 7.3.4 Timer Bi register read out

EOL announced

7.4 Event counter mode (Bits 1 and 0 of timer Bi mode register = "012")

In this mode, an external signal is counted. (Refer to **Table 7.4.1.**) Figure 7.4.1 shows the structures of the timer Bi mode register and timer Bi register in the event counter mode.

Table 7.4.1 Specifications of event counter mode

Item	Specifications
Count source	● External signal input to pin TBiIN **(Notes 1 and 2)**. ● "Falling edge," "Rising edge," or "Falling and Rising edges" can be selected as the valid edge of the count source by software.
Count operation	● Countdown ● At an underflow, the reload register's contents is reloaded, and counting is continued.
Division ratio	$\frac{1}{(n+1)}$ n: Set value in the timer Bi register
Count start condition	When the count start flag is set to "1."
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	At an underflow
Pin TBiIN's function	Count source input
Read from timer	A counter value can be read out by reading the timer Bi register.
Write to timer	■ While counting is stopped When a value is written to the timer Bi register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer Bi register, it is written only to the reload register. (Transferred to the counter at the next reload time.)

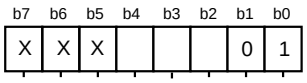
Notes 1: When the timer B1 internal connect selection bit (bit 2 at address $6D_{16}$) = "1," timer B1 counts the timer B2's underflow signal. (Refer to section **"7.4.3 Selectable functions."**)

2: When using timer B2 in the event counter mode, set both of the port-Xc selection bit (bit 4 at address $6C_{16}$) and the sub-clock output selection bit/Timer B2 clock source selection bit (bit 1 at address $6D_{16}$) to "0." When one of or both of these bits = "1," timer B2 functions as a clock timer. (Refer to section **"7.6 Clock timer."**)

ED-announced

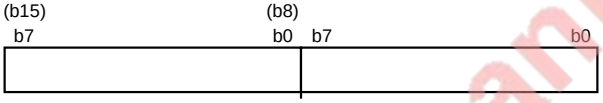
TIMER B

7.4 Event counter mode



Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 1: Event counter mode	0	RW
1			0	RW
2	Count polarity selection bits	b3 b2 0 0: Counting is performed at the falling edge of the external signal. 0 1: Counting is performed at the rising edge of the external signal. 1 0: Counting is performed at both falling and rising edges of the external signal. 1 1: Do not select.	0	RW
3			0	RW
4	•Timer B0 mode register Must be fixed to "0."		0	RW
	•Timer B1 and B2 mode registers Not implemented.		Un-defined	—
5	This bit is ignored in the event counter mode and is undefined at reading.		Un-defined	RO
6	These bits are ignored in the event counter mode.		0	RW
7			0	RW



Timer B0 register (addresses 51_{16}, 50_{16})
Timer B1 register (addresses 53_{16}, 52_{16})
Timer B2 register (addresses 55_{16}, 54_{16})

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Un-defined	RW

EOL announced

Fig. 7.4.1 Structures of timer Bi mode register and timer Bi register in event counter mode

7.4.1 Setting for event counter mode

Figure 7.4.2 shows an initial setting example for registers related to the event counter mode.
Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**

EOL announced

7.4 Event counter mode

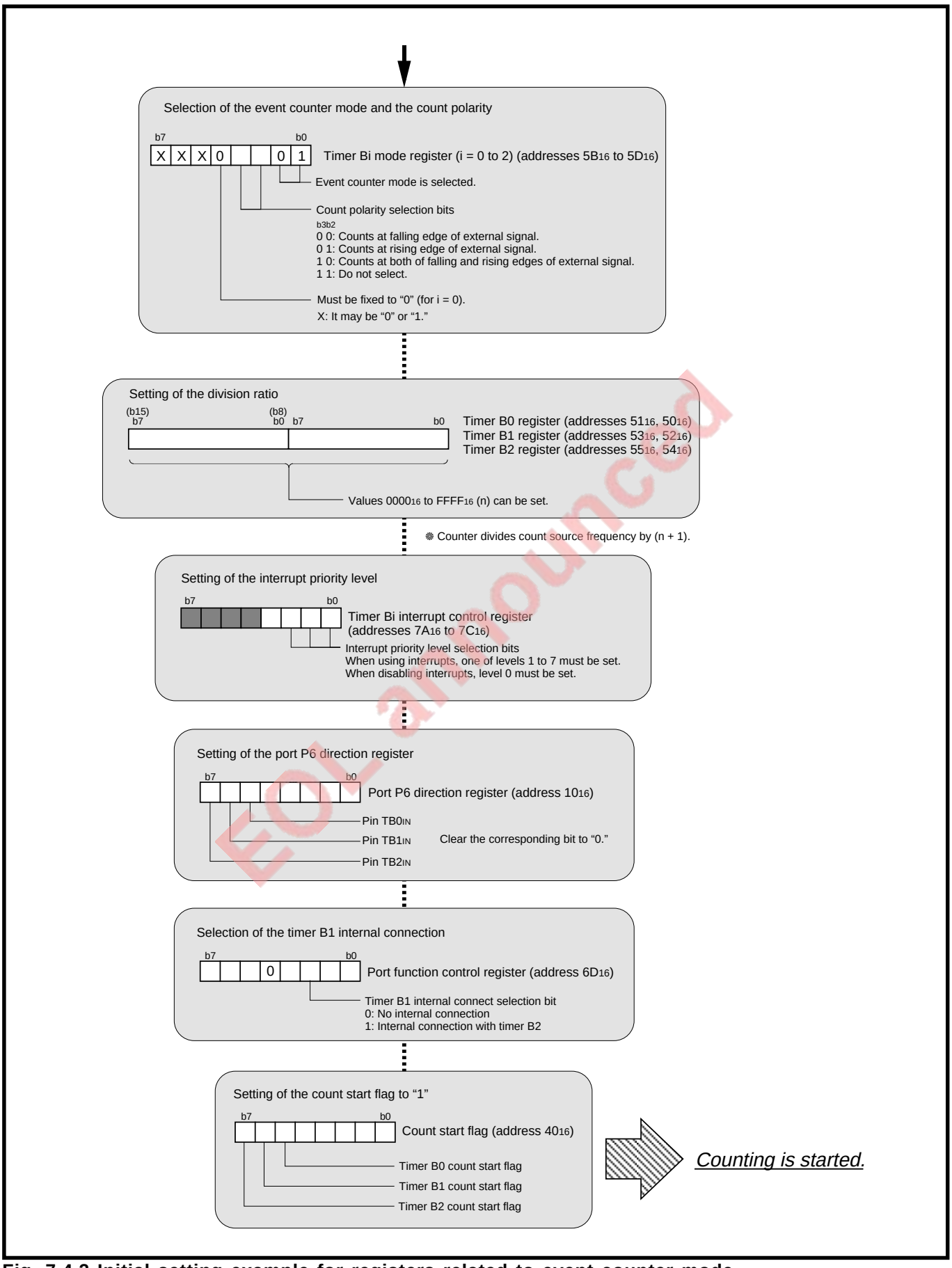


Fig. 7.4.2 Initial setting example for registers related to event counter mode

EOL announced

7.4.2 Operation in event counter mode

① When the count start flag is set to “1,” the counter starts counting of the count source.
② The counter counts the count source’s valid edges.
③ When an underflow occurs, the reload register’s contents is reloaded, and then counting is continued.
④ The timer Bi interrupt request bit is set to “1” when the underflow occurs in ③.
After this, the interrupt request bit remains set to “1” until the interrupt request is accepted or the interrupt request bit is cleared to “0” by software.

Figure 7.4.3 shows an operation example in the event counter mode.

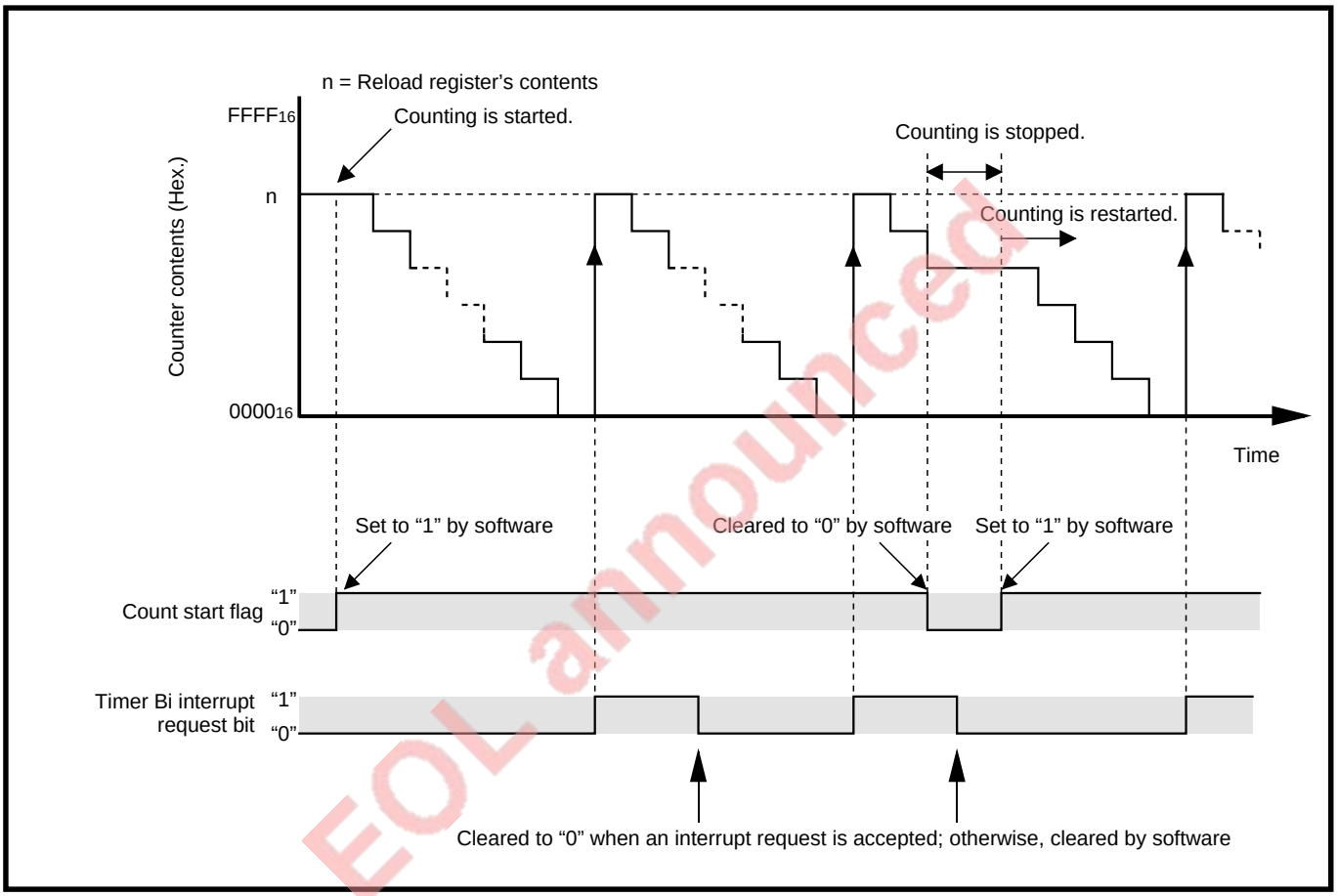


Fig. 7.4.3 Operation example in event counter mode

EOL announced

7.4 Event counter mode

7.4.3 Selectable functions

Timer B1 internal connection is described below.

(1) Timer B1 internal connection

When the timer B1 internal connect selection bit (bit 2 at address $6D_{16}$) is set to "1," timer B1 is internally connected to timer B2 and counts the timer B2's underflow signal. Accordingly, timers B2 and B1 function as a 32-bit (16 bits + 16 bits) timer and counts the timer B2's count source.

This function can be used when timer B2 operates in the timer or event counter mode, or as a clock timer.

Figure 7.4.4 shows connection between timers B2 and B1 when timer B1 internal connection is selected. Figure 7.4.5 shows structures of the timer B1 mode register and port function control register when timer B1 internal connection is selected. Figure 7.4.6 shows an operation example when timer B1 internal connection is selected.

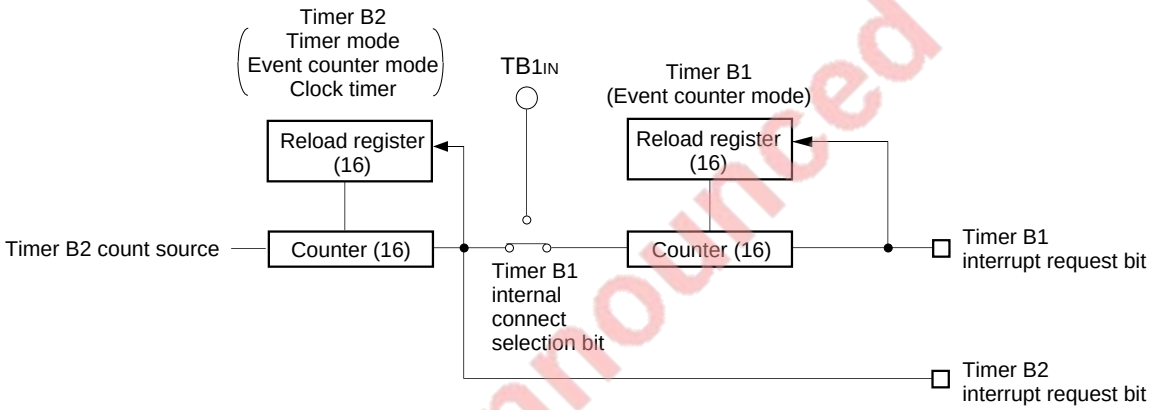


Fig. 7.4.4 Connection between timers B2 and B1 when timer B1 internal connection is selected

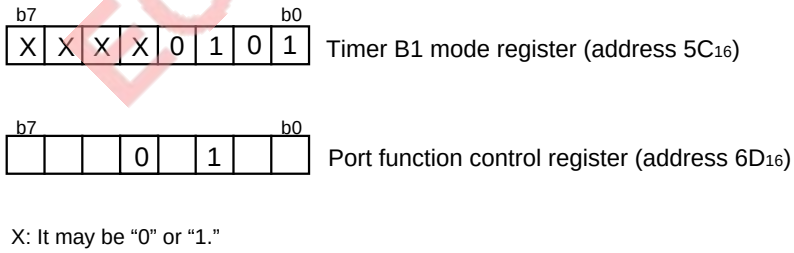
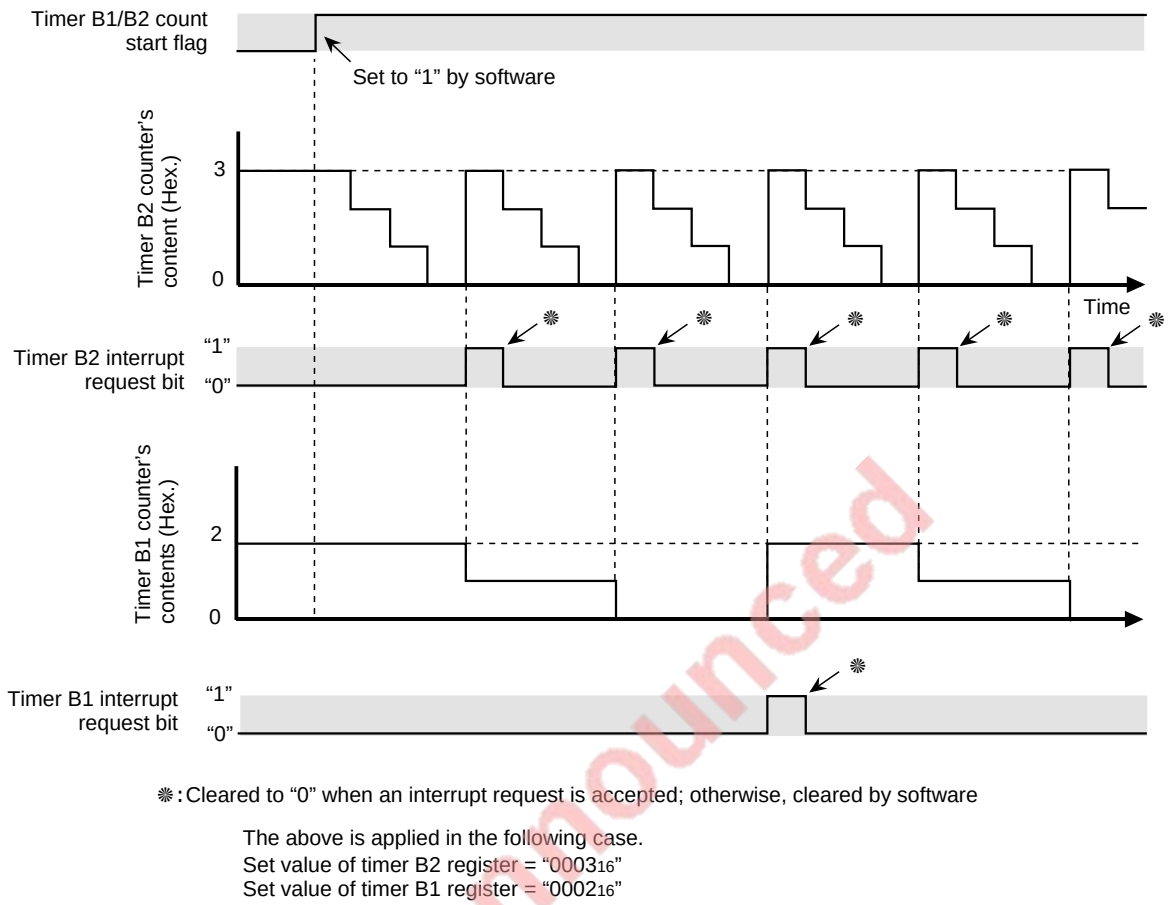


Fig. 7.4.5 Structures of timer B1 mode register and port function control register when timer B1 internal connection is selected

EOL announced



❋ : Cleared to “0” when an interrupt request is accepted; otherwise, cleared by software

The above is applied in the following case.
Set value of timer B2 register = “0003_{16}”
Set value of timer B1 register = “0002_{16}”

Fig. 7.4.6 Operation example when timer B1 internal connection is selected

EOL announced

TIMER B

7.4 Event counter mode

[Precautions in event counter mode]

1. While counting is in progress, by reading out the timer Bi register, the counter value can be read at an arbitrary timing. However, when reading is performed at the reload timing shown in Figure 7.4.7, value "FFFF$_{16}$" is read out. If reading is performed in the period from when a value is set into the timer Bi register with the counter stopped until the counter starts counting, the set value is correctly read out.

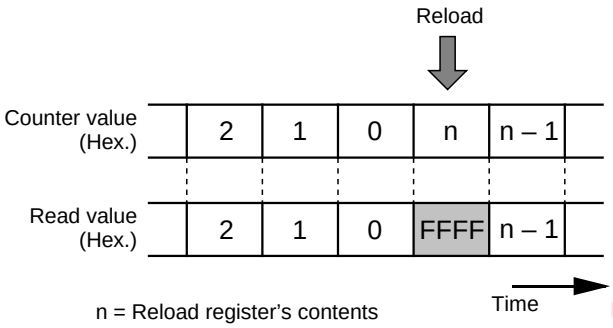


Fig. 7.4.7 Timer Bi register read out

2. The internal connect function between timer B2 and timer B1 can be used when timer B2 operates in the timer or event counter mode, or as a clock timer. Do not use this function in the pulse period/pulse width measurement mode.

EOL announced

7.5 Pulse period/Pulse width measurement mode (Bits 1 and 0 of timer Bi mode register = "10$_2$")

In this mode, an external signal's pulse period or pulse width is measured. (Refer to **Table 7.5.1.**) Figure 7.5.1 shows the structures of the timer Bi mode register and timer Bi register in the pulse period/pulse width measurement mode.

■ Pulse period measurement
The pulse period of an external signal which is input to pin TBi$_{IN}$ is measured.

■ Pulse width measurement
The pulse width ("L" level width and "H" level width) of an external signal which is input to pin TBi$_{IN}$ is measured.

Note: When the port-Xc selection bit (bit 4 at address 6C$_{16}$) = "1," timer B2 functions as a clock timer. Accordingly, pulse period/pulse width measurement cannot be performed.

Table 7.5.1 Specifications of pulse period/pulse width measurement mode

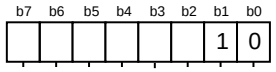
Item	Specifications
Count source	Clock f_2, f_{16}, f_{64}, or f_{512}
Count operation	● Countup ● When valid edge of the measurement pulse is input, the counter value is transferred to the reload register. And then, the counter value is cleared to "0000$_{16}$," and counting is continued.
Count start condition	When the count start flag is set to "1."
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	● When the valid edge of the measurement pulse is input (**Note 1**). ● At an overflow (Simultaneously, the overflow flag is set to "1.")
Pin TBi$_{IN}$'s function	Measurement pulse input
Read from timer	By reading the timer Bi register, the reload register's contents (Measurement result) is read out (**Note 2**).
Write to timer	Ignored

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**
Overflow flag: A flag used to identify the source of an interrupt request occurrence.
Notes 1: An interrupt request is not generated when the first valid edge is input after counting starts.
2: From when counting starts until the second valid edge is input, a value obtained by reading the timer Bi register is undefined.

FOR Announced

TIMER B

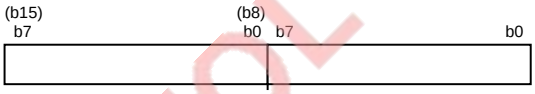
7.5 Pulse period/Pulse width measurement mode



Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 1 0: Pulse period/pulse width measurement mode	0	RW
1			0	RW
2	Measurement mode selection bits	b3 b2 0 0: Pulse period measurement (interval between falling edges of the measurement pulse) 0 1: Pulse period measurement Interval between rising edges of the measurement pulse) 1 0: Pulse width measurement (Interval from a falling edge to a rising edge, and from a rising edge to a falling edge of the measurement pulse) 1 1: Do not select.	0	RW
3			0	RW
4	•Timer B0 mode register Must be fixed to "0."		0	RW
	•Timer B1 and B2 mode registers Not implemented.		Un-defined	—
5	Timer Bi overflow flag **(Note)**	0: No overflow 1: Overflow	1	RO
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**
Note: Timer Bi overflow flag is cleared to "0" when writing to the timer Bi mode register is performed with the count start flag = "1." This flag cannot be set to "1" by software.



Timer B0 register (addresses 51_{16}, 50_{16})
Timer B1 register (addresses 53_{16}, 52_{16})
Timer B2 register (addresses 55_{16}, 54_{16})

Bit	Functions	At reset	RW
15 to 0	The result of the pulse period or pulse width measurement is read out.	Un-defined	RO

EOL announced

Fig. 7.5.1 Structures of timer Bi mode register and timer Bi register in pulse period/pulse width measurement mode

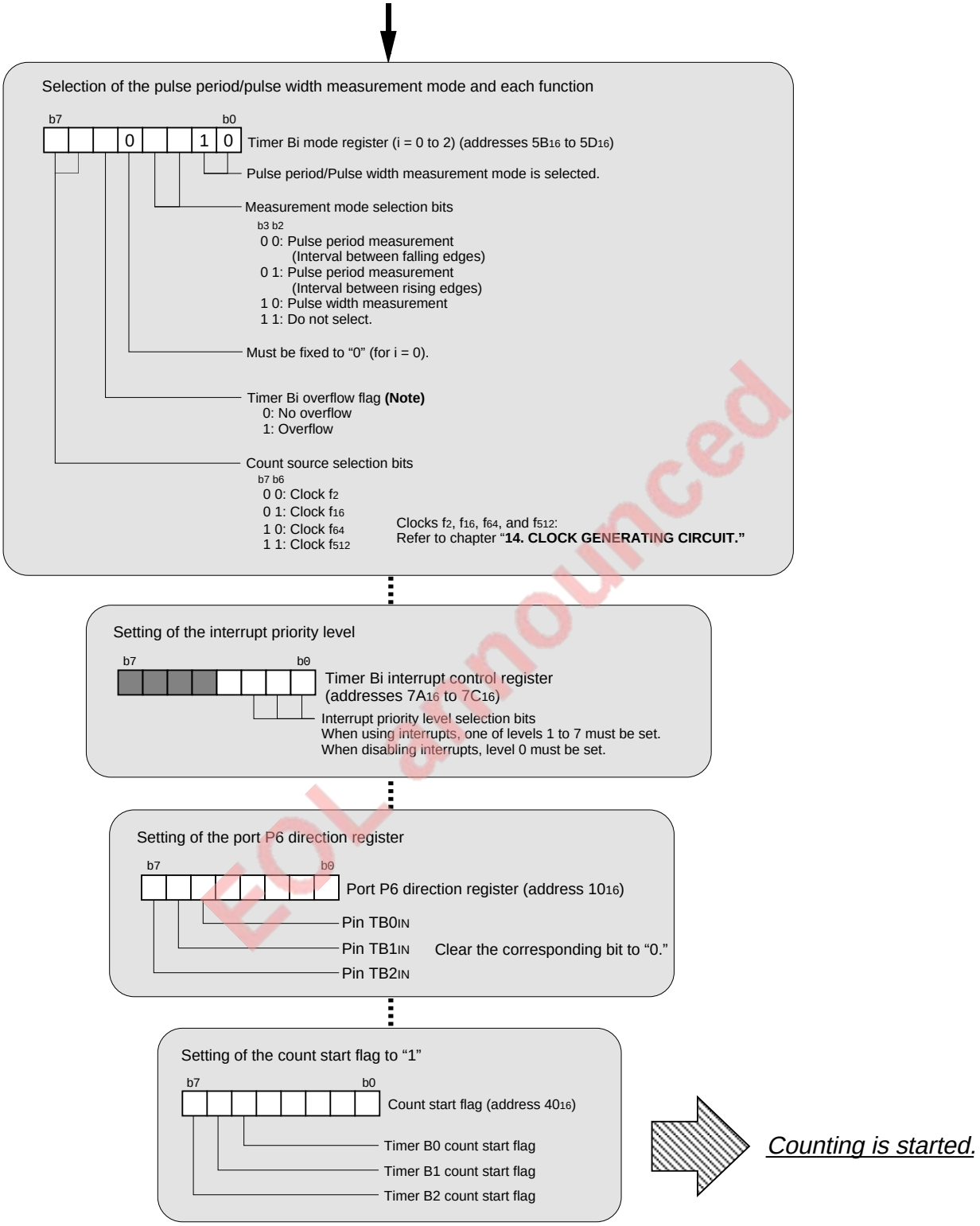
7.5.1 Setting for pulse period/pulse width measurement mode

Figure 7.5.2 shows an initial setting example for registers related to the pulse period/pulse width measurement mode.

Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**

EOL announced

7.5 Pulse period/Pulse width measurement mode



Note: The timer Bi overflow flag is a read-only flag. This flag is cleared to "0" when writing to timer Bi mode register is performed with the count start flag = "1."

Fig. 7.5.2 Initial setting example for registers related to pulse period/pulse width measurement mode

EOL announced

7.5.2 Count source

In the pulse period/pulse width measurement mode, by the count source selection bits (bits 7 and 6 at addresses $5B_{16}$ to $5D_{16}$), a count source can be selected. Table 7.5.2 lists the relationship between the count source selection bits and count source.

Table 7.5.2 Relationship between count source selection bits and count source

b7	b6	Count source	Frequency of count source		
			When system clock = 25 MHz	When system clock = 16 MHz	When system clock = 8 MHz
0	0	f_2	12.5 MHz	8 MHz	4 MHz
0	1	f_{16}	1.5625 MHz	1 MHz	500 kHz
1	0	f_{64}	390.625 kHz	250 kHz	125 kHz
1	1	f_{512}	48.8281 kHz	31.25 kHz	15.625 kHz

Clocks f_2, f_{16}, f_{64}, f_{512}, and system clock: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0" and the main clock division selection bit (bit 0 at address $6F_{16}$) = "0." (For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)

EOL announced

7.5 Pulse period/Pulse width measurement mode

7.5.3 Operation in pulse period/pulse width measurement mode

① When the count start flag is set to "1," the counter starts counting of the count source.
② When a valid edge of the measurement pulse is input, the counter value is transferred to the reload register. (Refer to **"(1) Pulse period/Pulse width measurement."**)
③ After a transfer in ②, the counter value becomes "0000_{16}," and the counter continues counting.
④ The timer Bi interrupt request bit is set to "1" when the counter value becomes "0000_{16}" in ③,(**Note**). After this, the interrupt request bit remains set to "1" until the interrupt request is accepted or the interrupt request bit is cleared to "0" by software.
⑤ Operations ② to ④ are repeated.

Note: Timer Bi interrupt request is not generated when the first valid edge is input after counting starts.

(1) Pulse period/Pulse width measurement

Whether to measure the pulse period or the pulse width of an external signal can be selected by the measurement mode selection bits (bits 3 and 2 at addresses $5B_{16}$ to $5D_{16}$). Table 7.5.3 lists the relationship between the measurement mode selection bits and the pulse period/pulse width measurement. Make sure that the measurement interval from the falling edge to the rising edge and that of from the rising edge to the falling edge are two cycles of the count source or more. When measuring pulse width of a signal whose duty ratio is not 50%, identify whether the measurement result is the "H" level width or the "L" level width by software.

Table 7.5.3 Relationship between measurement mode selection bits and pulse period/pulse width measurement

b3	b2	Pulse period/Pulse width measurement	Measurement interval (Valid edge)
0	0	Pulse period measurement	From falling edge to falling edge (Falling edge)
0	1		From rising edge to rising edge (Rising edge)
1	0	Pulse width measurement	From falling edge to rising edge, and from rising edge to falling edge (Falling and Rising edges)

EOL announced

(2) Timer Bi overflow flag

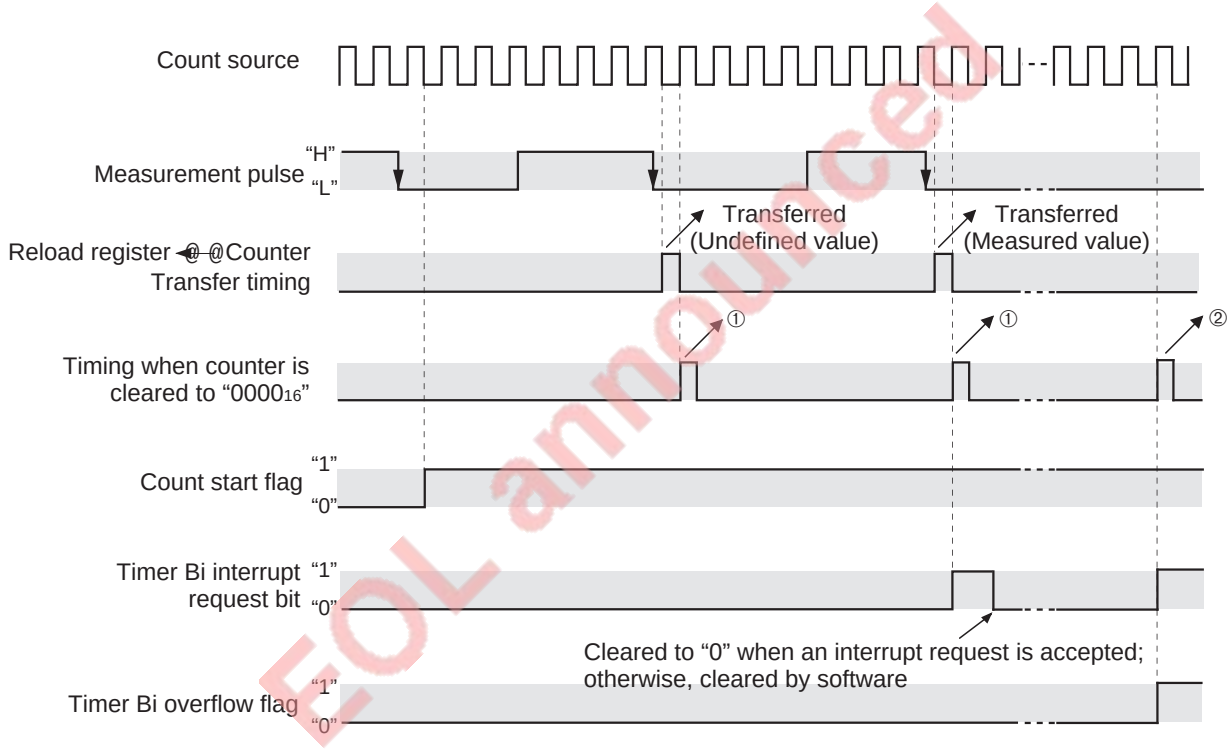
When a measurement pulse's valid edge is input or an overflow occurs, a timer Bi interrupt request is generated. The timer Bi overflow flag is used to identify the cause of an interrupt request occurrence, in other words, determine whether it is an overflow or a valid edge input.

When an overflow occurs, the timer Bi overflow flag is set to "1." Therefore, the source of the interrupt request occurrence can be identified by checking the timer Bi overflow flag's state in the interrupt routine. The timer Bi overflow flag is cleared to "0" at the next count timing of the count source when a value is written to the timer Bi mode register with the count start flag = "1."

The timer Bi overflow flag is a read-only flag.

Do not use this flag for detection of overflow timing.

Figure 7.5.3 shows the operation during pulse period measurement. Figure 7.5.4 shows the operation during pulse width measurement.



① Initialization of the counter because of measurement completion
② Overflow

❋ The above is applied when measurement is performed from one falling edge of the measurement pulse until the next falling edge of that.

Fig. 7.5.3 Operation during pulse period measurement

EOL announced

TIMER B

7.5 Pulse period/Pulse width measurement mode

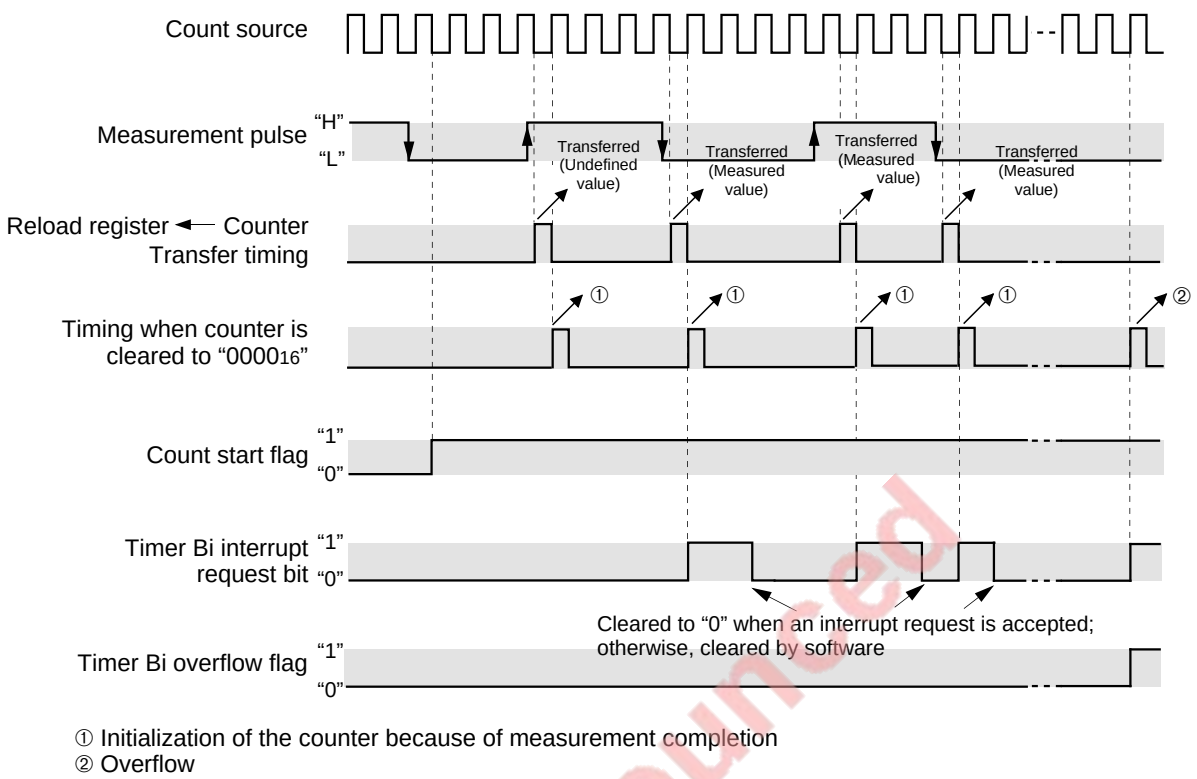


Fig. 7.5.4 Operation during pulse width measurement

EOL announced

[Precautions in pulse period/pulse width measurement mode]

1. A timer Bi interrupt request is generated by the following sources:
   - The measurement pulse's valid edge which is input
   - An overflow

   The interrupt request source shown above can be determined by the timer Bi overflow flag.

2. At reset, the timer Bi overflow flag is set to "1." This flag can be cleared to "0" by performing writing to the timer Bi mode register with the count start flag = "1."

3. When the first valid edge is input after counting starts, an undefined value is transferred to the reload register. At this time, a timer Bi interrupt request is not generated.

4. At start of counting, the counter value is undefined. Therefore, there is a possibility that a timer Bi interrupt request is generated by an overflow which occurs immediately after counting starts.

5. When the measurement mode selection bits are changed after counting starts, the timer Bi interrupt request bit is set to "1." Note that the timer Bi interrupt request bit does not change if the same value as before is written to the measurement mode selection bits.

6. When an input signal to pin TBiIN is affected by noise or others, there is a possibility that the counter cannot perform the exact measurement. We recommend to verify, by software, that the measurement values are within a constant range.

EOL announced

7.6 Clock timer

Timer B2 functions as a clock timer on the following condition (Refer to **Table 7.6.1.**):

- When the port-Xc selection bit (bit 4 at address $6C_{16}$) = "1"
- When the port-Xc selection bit = "0" and the timer B2 clock source selection bit (bit 1 at address $6D_{16}$) = "1"

Figure 7.6.1 shows the structures of the timer B2 mode register and timer B2 register when a clock timer is used.

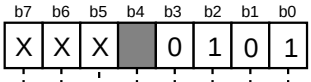
Table 7.6.1 Specifications of clock timer

Item	Specifications
Count source	f_{C32} (Sub clock divided by 32: $f(X_{CIN})/32$), or Main clock divided by 32: $f(X_{IN})/32$)
Count operation	● Countdown ● At an underflow, the reload register's contents is reloaded, and counting is continued.
Division ratio	$\frac{1}{(n+1)}$ n: Set value in the timer B2 register
Count start condition	When the count start flag is set to "1."
Count stop condition	When the count start flag is cleared to "0."
Interrupt request occurrence timing	At an underflow
Pin $TB2_{IN}$'s function	Programmable I/O port or ϕ_{SUB} output pin
Read from timer	A counter value can be read out by reading the timer B2 register.
Write to timer	■ While counting is stopped When a value is written to the timer B2 register, it is written to both of the reload register and counter. ■ While counting is in progress When a value is written to the timer B2 register, it is written only to the reload register. (Transferred to the counter at the next reload time.)

Clocks f_{C32} and $f(X_{CIN})$: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

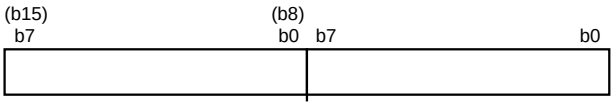
Either of $f(X_{CIN})/32$ or $f(X_{IN})/32$ can be selected as the clock timer's count source, f_{C32}.
The way to generate $f(X_{CIN})/32$ is different from that for clocks whose source is the system clock (e.g., internal clock ϕ, clocks f_2 to f_{512}, and so on). (Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**) $f(X_{CIN})/32$ is not affected by the system clock selection bit and system clock stop bit at wait state (bits 3 and 5 at address $6C_{16}$). Therefore, in the wait mode, (Refer to chapter **"11. STOP AND WAIT MODES."**) only the clock timer can operate by itself. In other words, it is possible to supply f_{C32} only.
Oppositely, the way to generate $f(X_{IN})/32$ is the same as that for the system clock. Therefore, when the system clock stop bit at wait state = "1," f_{C32} is not supplied in the wait mode.
Figure 7.6.2 shows the structure of the clock timer.

EOL announced



Timer B2 mode register (address 5D16)

Bit	Functions	At reset	RW
0	Must be fixed to “1” for the clock timer.	0	RW
1	Must be fixed to “0” for the clock timer.	0	RW
2	Must be fixed to “1” for the clock timer.	0	RW
3	Must be fixed to “0” for the clock timer.	0	RW
4	Not implemented.	Un-defined	—
5	This bit is ignored for the clock timer.	Un-defined	RO
6	These bits are ignored for the clock timer.	0	RW
7		0	RW



Timer B2 register (addresses 5516 and 5416)

Bit	Functions	At reset	RW
15 to 0	Values 000016 to FFFF16 can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Un-defined	RW

EOL announced

Fig. 7.6.1 Structures of timer B2 mode register and timer B2 register when clock timer is used

TIMER B

7.6 Clock timer

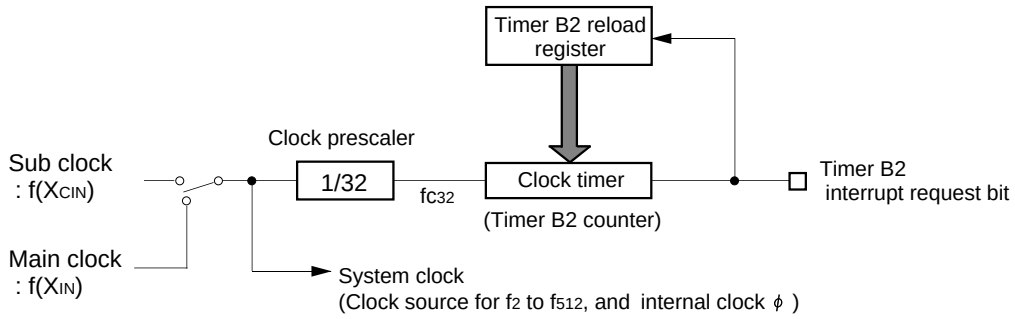
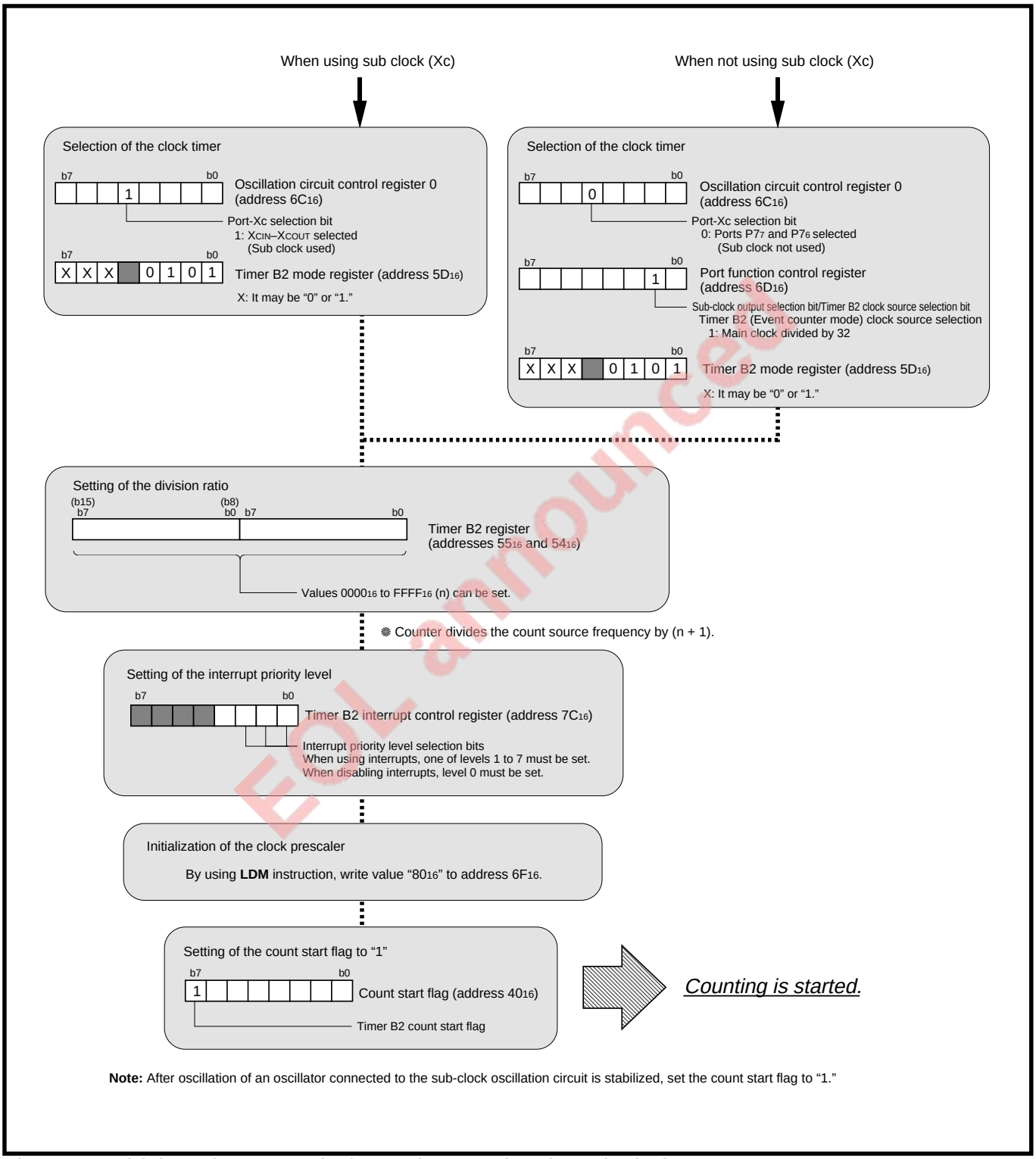


Fig. 7.6.2 Structure of clock timer

EOL announced

7.6.1 Setting for clock timer

Figure 7.6.3 shows an initial setting example for registers related to the clock timer.
Note that when using interrupts, setting for enabling interrupts is required. For details, refer to chapter **"4. INTERRUPTS."**



Note: After oscillation of an oscillator connected to the sub-clock oscillation circuit is stabilized, set the count start flag to "1."

Fig. 7.6.3 Initial setting example for registers related to clock timer

7.6 Clock timer

7.6.2 Operation of clock timer

① When the count start flag is set to “1,” the counter starts counting of the count source.
② When an underflow occurs, the reload register’s contents is reloaded, and then counting is continued.
③ The timer B2 interrupt request bit is set to “1” when the underflow occurs in ②.
After this, the interrupt request bit remains set to “1” until the interrupt request is accepted or the interrupt request bit is cleared to “0” by software.

For example, if f(XCIN) = 32.768 kHz, a timer B2 interrupt request can be issued every second when value “3FF16” is set into the timer B2 register (addresses 5416 and 5516) and every minute when value “EFFF16” is set into the register. Figure 7.6.4 shows an operation example of clock timer.

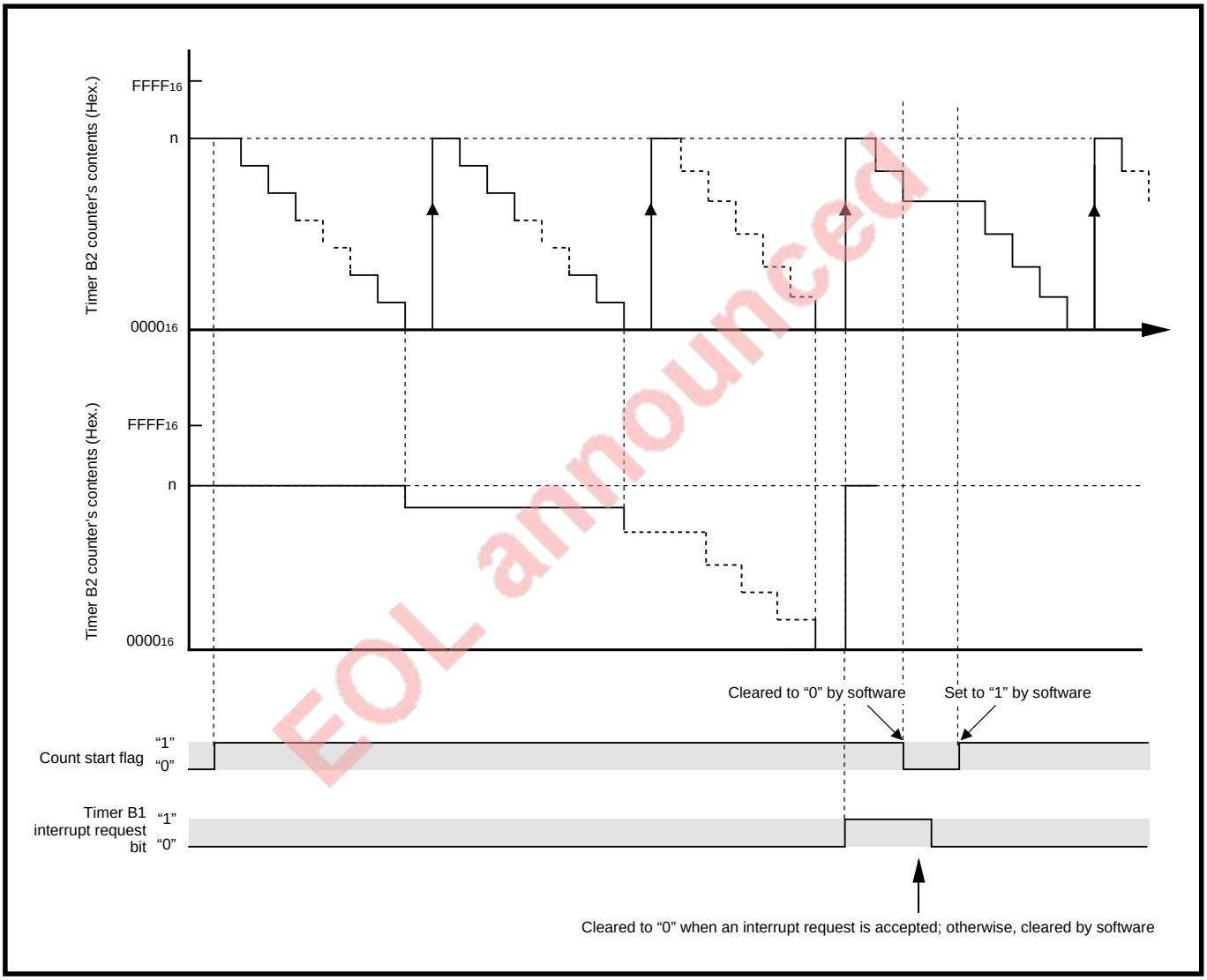


Fig. 7.6.4 Operation example of clock timer

EOL announced

[Precautions for clock timer]

1. While counting is in progress, by reading out the timer B2 register, the counter value can be read at an arbitrary timing. However, when reading is performed at the reload timing shown in Figure 7.6.5, value "FFFF$_{16}$" is read out. If reading is performed in the period from when a value is set into the timer B2 register with the counter stopped until the counter starts counting, the set value is correctly read out.

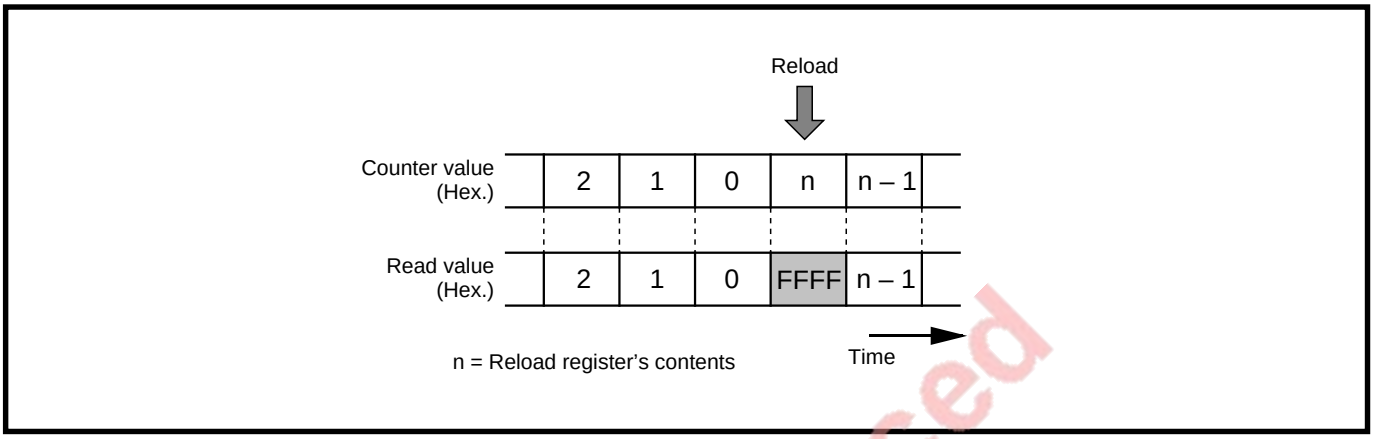


Fig. 7.6.5 Timer B2 register read out

2. For the clock prescaler reset, refer to section **"14.3.4 Clock prescaler reset."**

EOL announced

MEMO

EOL announced

CHAPTER 8

SERIAL I/O

8.1 Overview
8.2 Block description
8.3 Clock synchronous serial I/O mode
8.4 Clock asynchronous serial I/O (UART) mode

EOL announced

SERIAL I/O

8.1 Overview

The serial I/O consists of 3 channels: UART0, UART1 and UART2. They each have a dedicated timer for generating a transfer clock and can operate independently.

8.1 Overview

UARTi (i = 0 to 2) has the following two operating modes: clock synchronous serial I/O and clock asynchronous serial I/O (UART) modes. Except for a few functions in the clock synchronous serial I/O mode, UART0, UART1 and UART2 have the same functions.

- **Clock synchronous serial I/O mode**
  Transmitter and receiver use the same clock as a transfer clock. Transfer data has a length of 8 bits.

- **Clock asynchronous serial I/O (UART) mode**
  Transfer rate and transfer data format can arbitrarily be set. The transfer data length can be selected from the following three types: 7 bits, 8 bits, and 9 bits.

Figure 8.1.1 shows the transfer data formats in each operating mode. Table 8.1.1 shows the differences between UART0, UART1 and UART2.

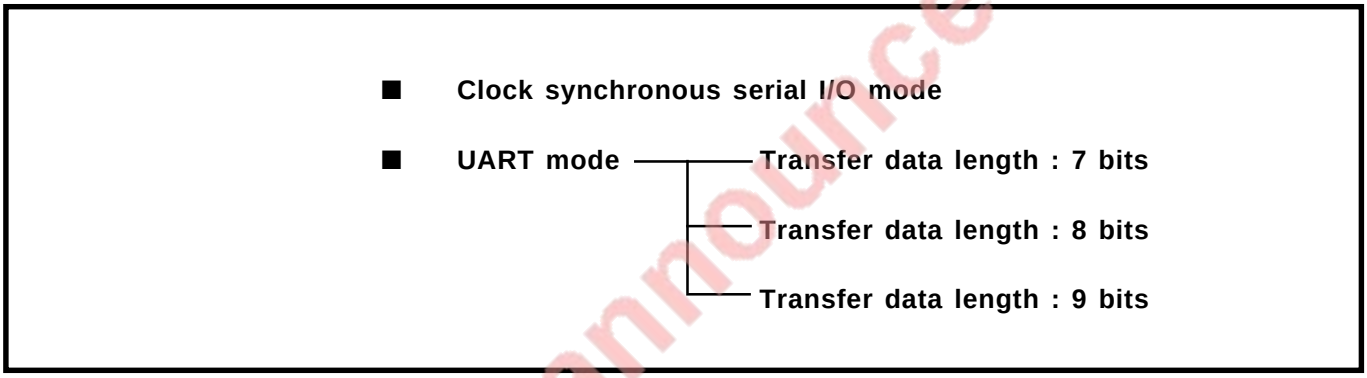


Fig. 8.1.1 Transfer data formats in each operating mode

EOL announced

Table 8.1.1 Differences between UART0, UART1 and UART2

	Communication	$\overline{CTS}$ input/ $\overline{RTS}$ output function	Interrupt function	Data output/CLK polarity/transfer format select function	Multiple clocks output function	Sleep function
UART0	Clock synchronous or asynchronous (UART) mode is selectable.	Both functions are available.	•UART0 transmission •UART0 reception (2 systems)	Available	Available	Available
UART1	Clock synchronous or asynchronous (UART) mode is selectable.	Both functions are available.	•UART1 transmission •UART1 reception (2 systems)	Available	Not available	Available
UART2	Clock synchronous or asynchronous (UART) mode is selectable.	Only $\overline{CTS}$ input function is available.	•UART2 transmission /reception **(Note 1)** (1 system)	Not available (**Note 2**)	Not available	Not available

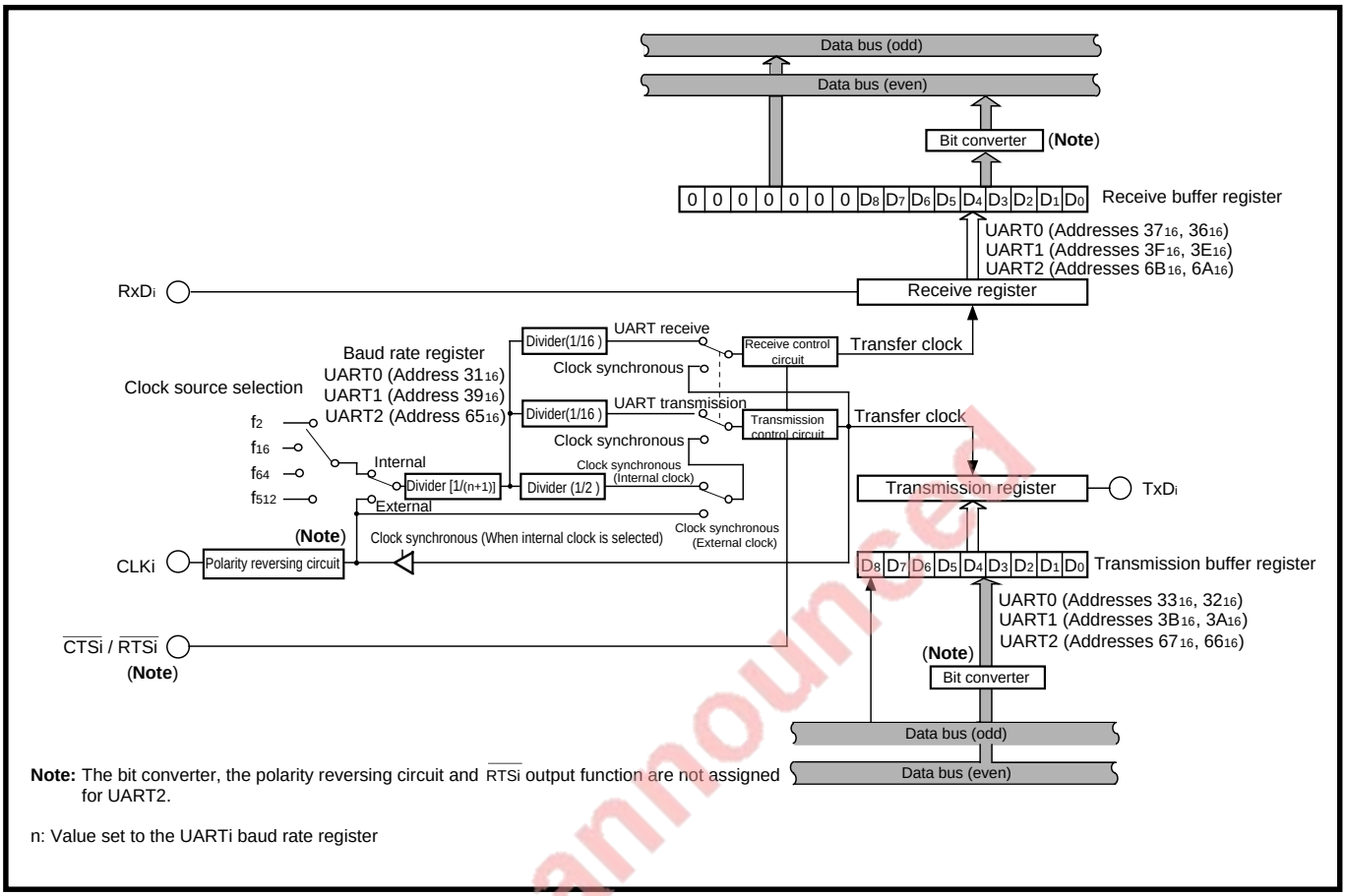
Notes 1: The A-D conversion interrupt and UART2 transmission/reception interrupt share the interrupt vector addresses and the interrupt control register.
When the UART2 mode is selected by specifying bits 2 to 0 of the UART2 transmit/receive mode register (address 64_{16}), the A-D conversion interrupt function cannot be used.

2: UART2 is fixed as follows.
- Data output (TxD_2 pin): CMOS output
- Polarity of CLK_2: Transmit data is output at the falling edge of the transfer clock.
  Receive data is input at the rising edge of the transfer clock.
  When not transferring, CLK_2 pin's level is "H."
  (Used in the clock synchronous serial I/O mode)
- Transfer format: LSB (the least significant bit) first

EOL announced

8.2 Block description

Figure 8.2.1 shows the block diagram for serial I/O. Registers related to serial I/O are described below.



Note: The bit converter, the polarity reversing circuit and $\overline{\text{RTSi}}$ output function are not assigned for UART2.

n: Value set to the UARTi baud rate register

Fig. 8.2.1 Block diagram for serial I/O

EOL announced

8.2.1 UARTi transmit/receive mode register

Figures 8.2.2 and 8.2.3 show the structure of UARTi transmit/receive mode register. The serial I/O mode selection bits are used to select a UARTi's operating mode. For bits 4 to 6, refer to section **"8.4.2 Transfer data format."** For bit 7, refer to section **"8.4.8 Sleep mode."**

UART0 transmit/receive mode register (address 30_{16})
UART1 transmit/receive mode register (address 38_{16})

Bit	Bit name	Functions	At reset	RW
0	Serial I/O mode selection bits	b2 b1 b0 0 0 0: Serial I/O is disabled. (P8 functions as a programmable I/O port.) 0 0 1: Clock synchronous serial I/O mode 0 1 0: Do not select. 0 1 1: Do not select. 1 0 0: UART mode (Transfer data length = 7 bits) 1 0 1: UART mode (Transfer data length = 8 bits) 1 1 0: UART mode (Transfer data length = 9 bits) 1 1 1: Do not select.	0	RW
1			0	RW
2			0	RW
3	Internal/External clock selection bit	0: Internal clock 1: External clock	0	RW
4	Stop bit length selection bit (Valid in the UART mode.) **(Note)**	0: One stop bit 1: Two stop bits	0	RW
5	Odd/Even parity selection bit (Valid in the UART mode when the parity enable bit = "1.") **(Note)**	0: Odd parity 1: Even parity	0	RW
6	Parity enable bit (Valid in the UART mode.) **(Note)**	0: Parity is disabled. 1: Parity is enabled.	0	RW
7	Sleep selection bit (Valid in the UART mode.) **(Note)**	0: The sleep mode is terminated. (Ignored.) 1: The sleep mode is selected.	0	RW

Note: Bits 4 to 6 are ignored in the clock synchronous serial I/O mode. (They may be "0" or "1.") Fix bit 7 to "0."

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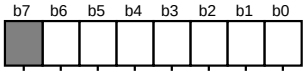
Fig. 8.2.2 Structure of UARTi transmit/receive mode register (1)

8.2 Block description



UART2 transmit/receive mode register (address 64 16)

Bit	Bit name	Functions	At reset	RW
0	Serial I/O mode selection bits **(Note 1)**	b2 b1 b0 0 0 0: Serial I/O is ignored. (P7 functions as a programmable I/O port) 0 0 1: Clock synchronous serial I/O mode 0 1 0: } Do not select. 0 1 1: } 1 0 0: UART mode (Transfer data length = 7 bits) 1 0 1: UART mode (Transfer data length = 8 bits) 1 1 0: UART mode (Transfer data length = 9 bits) 1 1 1: Do not select.	0	RW
1			0	RW
2			0	RW
	Internal/External clock selection bit	0: Internal clock 1: External clock	0	RW
4	Stop bit length selection bit (Valid in the UART mode.) **(Note 2)**	0: One stop bit 1: Two stop bits	0	RW
5	Odd/Even Parity selection bit (Valid in the UART mode when the parity enable bit = "1".) **(Note 2)**	0: Odd parity 1: Even parity	0	RW
6	Parity enable bit (Valid in the UART mode.) **(Note 2)**	0: Parity is disabled. 1: Parity is enabled.	0	RW
7	Not implemented.		Un-defined	—

Notes 1: By specifying these bits, an A-D conversion interrupt or a UART2 transmit/receive interrupt is selected.
When bits 2 to 0 = "000$_2$," an A-D conversion interrupt is selected. When bits 2 to 0 = "001 $_2$" or "100$_2$ to 111$_2$," a UART2 transmit/receive interrupt is selected.
2: In the clock synchronous serial I/O mode, bits 4 to 6 are ignored. (They may be "0" or "1.")

Fig. 8.2.3 Structure of UARTi transmit/receive mode register (2)

EOL announced

(1) Internal/External clock selection bit (bit 3)

● Clock synchronous serial I/O mode

When an internal clock is selected by clearing this bit to "0," a clock which is specified with the BRG count source selection bits (bits 1 and 0 at addresses 34_{16}, $3C_{16}$ and 68_{16}) becomes the count source of BRGi (described later). At this time, the BRGi's output divided by 2 is the transfer clock. The transfer clock is output from the CLKi pin (**Note**).

When an external clock is selected by setting this bit to "1," a clock input to the CLKi pin becomes the transfer clock.

Note : When selecting an internal clock and performing only transmission in UART0, the number of the transfer clock output pins varies according to the contents of the transmit clock output pin selection bits (bits 5 and 4 at address $6E_{16}$). (Refer to section **"8.3.1 Transfer clock."**)

● UART mode

When an internal clock is selected by clearing this bit to "0," a clock which is specified with the BRG count source selection bits (bits 1 and 0 at addresses 34_{16}, $3C_{16}$ and 68_{16}) becomes the count source of the BRGi (described later). At this time, the CLKi pin functions as a programmable I/O port.

When an external clock is selected by setting this bit to "1," a clock input to the CLKi pin becomes the count source of BRGi .

Note that, in the UART mode, the BRGi's output divided by 16 is always the transfer clock.

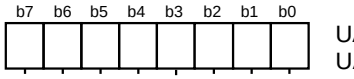
BRGi: UARTi baud rate register (Refer to section "**8.2.7 UARTi baud rate register (BRGi).**")

EOL announced

8.2 Block description

8.2.2 UARTi transmit/receive control register 0

Figures 8.2.4 and 8.2.5 show the structure of UARTi transmit/receive control register 0. For bits 1 and 0, refer to section **"(1) Internal/External clock selection bit"** in page 8-7. For bits 7 to 4, refer to the description of each operating mode.



UART0 transmit/receive control register 0 (address $3\,4_{16}$)
UART1 transmit/receive control register 0 (address $3C_{16}$)

Bit	Bit name	Functions	At reset	RW
0	BRG count source selection bits	b1 b0 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
1			0	RW
2	$\overline{CTS}/\overline{RTS}$ function selection bit (Valid when the $\overline{CTS}/\overline{RTS}$ enable bit is "0.")	0: The $\overline{CTS}$ function is selected. 1: The $\overline{RTS}$ function is selected.	0	RW
3	Transmission register empty flag	0: Data is present in the transmission register. (Transmission is in progress.) 1: No data is present in the transmission register. (Transmission is completed.)	1	RO
4	$\overline{CTS}/\overline{RTS}$ enable bit	0: The $\overline{CTS}/\overline{RTS}$ function is enabled. 1: The $\overline{CTS}/\overline{RTS}$ function is disabled. ($P8_0$ and $P8_4$ function as programmable I/O ports.)	0	RW
5	Data output selection bit	0: Pin TxD_i is set for CMOS output. 1: Pin TxD_i is set for N-channel open-drain output.	0	RW
6	CLK polarity selection bit (This bit is used in the clock synchronous serial I/O mode.) **(Note)**	0: At the falling edge of the transfer clock, transmit data is output; at the rising edge of the transfer clock, receive data is input. When not in transferring, pin CLK_i's level is "H." 1: At the rising edge of the transfer clock, transmit data is output; at the falling edge of the transfer clock, receive data is input. When not in transferring, pin CLK_i's level is "L."	0	RW
7	Transfer format selection bit (This bit is used in the clock synchronous serial I/O mode.) **(Note)**	0: LSB (Least Significant Bit) first 1: MSB (Most Significant Bit) first	0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**
Note: Fix bits 6 and 7 to "0" in the UART mode.

EOL announced

Fig. 8.2.4 Structure of UARTi transmit/receive control register 0 (1)

UART2 transmit/receive control register 0 (address 68_{16})

Bit	Bit name	Functions	At reset	RW
0	BRG count source selection bits	b1 b0 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
1			0	RW
2	$\overline{CTS}$ enable bit	0: The $\overline{CTS}$ function is enabled. 1: The $\overline{CTS}$ function is disabled. ($P8_0$ and $P8_4$ function as programmable I/O ports.)	0	RW
3	Transmission register empty flag	0: Data is present in the transmission register. (Transmission is in progress.) 1: No data is present in the transmission register. (Transmission is completed.)	1	RO
7 to 4	Not implemented.		Un-defined	

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Fig. 8.2.5 Structure of UARTi transmit/receive control register 0 (2)

(1) $\overline{CTS}/\overline{RTS}$ function selection bit (bit 2) (UART0, UART1)

This bit becomes valid when the $\overline{CTS}/\overline{RTS}$ enable bit (bit 6) is cleared to "0."

When this bit is cleared to "0" in order to select the $\overline{CTS}$ function, the $P8_0$ and $P8_4$ pins function as $\overline{CTS}$ input pins. At this time, a "L"-level signal input to the $\overline{CTS}$ pin is one of the transmit conditions. When this bit is set to "1" in order to select the $\overline{RTS}$ function, the $P8_0$ and $P8_4$ pins function as $\overline{RTS}$ output pins. When the receive enable bit (bit 2 at addresses 35_{16}, $3D_{16}$) is "0" (in other words, reception is disabled.), the $\overline{RTS}$ pin outputs "H" level.

In the clock synchronous serial I/O mode, the output level of $\overline{RTS}$ pin becomes "L" when receive conditions are satisfied; it becomes "H" when reception is started. Note that, when an internal clock is selected (bit 3 at addresses 30_{16}, 38_{16} = "0"), the $\overline{RTS}$ function is ignored.

In the clock asynchronous serial I/O mode, the output level of the $\overline{RTS}$ pin becomes "L" when receive enable bit is set to "1"; it becomes "H" when reception is started; it becomes "L" when the reception is completed.

(2) $\overline{CTS}$ enable bit (bit 2) (UART2)

$\overline{CTS}$ input pin is valid when this bit is set to "0."

A "L"-level signal input to the $\overline{CTS}$ pin is one of the transmit conditions.

(3) Transmission register empty flag (bit 3)

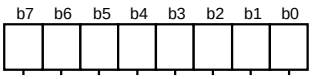
This flag is cleared to "0" when the contents of the UARTi transmission buffer register is transferred to the UARTi transmission register. When transmission is completed and the UARTi transmission register becomes empty, this flag is set to "1."

Eol announced

8.2 Block description

8.2.3 UARTi transmit/receive control register 1

Figure 8.2.6 shows the structure of UARTi transmit/receive control register 1. For bits 7 to 4, refer to the description of each operating mode.



UART0 transmit/receive control register 1 (address 35 16)
UART1 transmit/receive control register 1 (address 3D 16)
UART2 transmit/receive control register 1 (address 69 16)

Bit	Bit name	Functions	At reset	RW
0	Transmit enable bit	0: Transmission is disabled. 1: Transmission is enabled.	0	RW
1	Transmission buffer empty flag	0: Data is present in the transmission buffer register. 1: No data is present in the transmission buffer register.	1	RO
2	Receive enable bit	0: Reception is disabled. 1: Reception is enabled.	0	RW
3	Receive completion flag	0: No data is present in the receive buffer register. 1: Data is present in the receive buffer register.	0	RO
4	Overrun error flag **(Note 1)**	0: No overrun error is detected. 1: Overrun error is detected.	0	RO
5	Framing error flag **(Notes 1 and 2)** (Valid in the UART mode.)	0: No framing error is detected. 1: Framing error is detected.	0	RO
6	Parity error flag **(Notes 1 and 2)** (Valid in the UART mode.)	0: No parity error is detected. 1: Parity error is detected.	0	RO
7	Error sum flag **(Notes 1 and 2)** (Valid in the UART mode.)	0: No error is detected. 1: Error is detected.	0	RO

Notes 1: Bits 4 to 7 are cleared to "0" when the serial I/O mode selection bits (bits 2 to 0 at addresses 3016, 3816) are cleared to "0002" or when the receive enable bit is cleared to "0." (Bit 7 is cleared to "0" when all of bits 4 to 6 are "0.")
Note also that bits 5 and 6 are cleared to "0" when the low-order byte of the UARTi receive buffer register (addresses 36 16, 3E16, 6A16) is read out.
2: Bits 5 to 7 are ignored in the clock synchronous serial I/O mode.

Fig. 8.2.6 Structure of UARTi transmit/receive control register 1

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(1) Transmit enable bit (bit 0)

When this bit is set to “1,” UARTi enters the transmit enable state.

When this bit is cleared to “0” during transmission, UARTi enters the transmit disable state after the transmission which is in progress at this clearing is completed.

(2) Transmission buffer empty flag (bit 1)

This flag is set to “1” when data is transferred from the UARTi transmission buffer register to the UARTi transmission register.

This flag is cleared to “0” when data is set to the UARTi transmission buffer register.

(3) Receive enable bit (bit 2)

When this bit is set to “1,” UARTi enters the receive enable state.

When this bit is cleared to “0” during reception, UARTi quits the reception immediately and enters the receive disable state.

(4) Receive completion flag (bit 3)

This flag is set to “1” in the following case;

- when data is ready in the UARTi receive register and is transferred to the UARTi receive buffer register (in other words, when reception is completed).

This flag is cleared to “0” in one of the following cases;

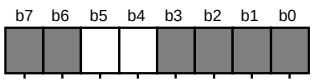
- when the low-order byte of the UARTi receive buffer register is read out,
- when the receive enable bit (bit 2) is cleared to “0,”
- when port P8 is used as a programmable I/O port by clearing the serial I/O mode selection bits (bits 2 to 0 at addresses 30_{16}, 38_{16} and 64_{16}) to “000_2”

EOL announced

8.2 Block description

8.2.4 Serial transmit control register

Figure 8.2.7 shows the structure of the serial transmit control register. The transmission clock output pin selection bits are valid only for UART0. For these bits, refer to section **"8.3.1 Transfer clock."**



Serial transmit control register (address 6E 16)

Bit	Bit name	Functions	At reset	RW
3 to 0	Not implemented.		Un-defined	—
4	Transmission clock output pin selection bits (Valid only in the clock synchronous serial I/O mode.) **(Note)**	b5 b4 0 0: One transfer clock output pin (CLK0) 0 1: } Multiple transfer clock output pins 1 0: } 1 1: }	0	RW
5			0	RW
7, 6	Not implemented. Value "0" is read out from here.		0	—

✺ When using multiple transfer clock output pins, satisfy the following conditions:

- Serial I/O mode selection bits (bits 2 to 0 at address 30 16) = "001 2"
- Internal/external clock selection bit (bit 3 at address 30 16) = "0"
- $\overline{\text{CTS}}/\overline{\text{RTS}}$ enable bit (bit 4 at address 34 16) = "1"
- Receive enable bit (bit 2 at address 35 16) = "0" (for cases ① and ② in Table 8.3.4)
- Transmission clock output pin selection bits = "01 2", "10 2", or "11 2" (Refer to **Table 8.3.3**.)

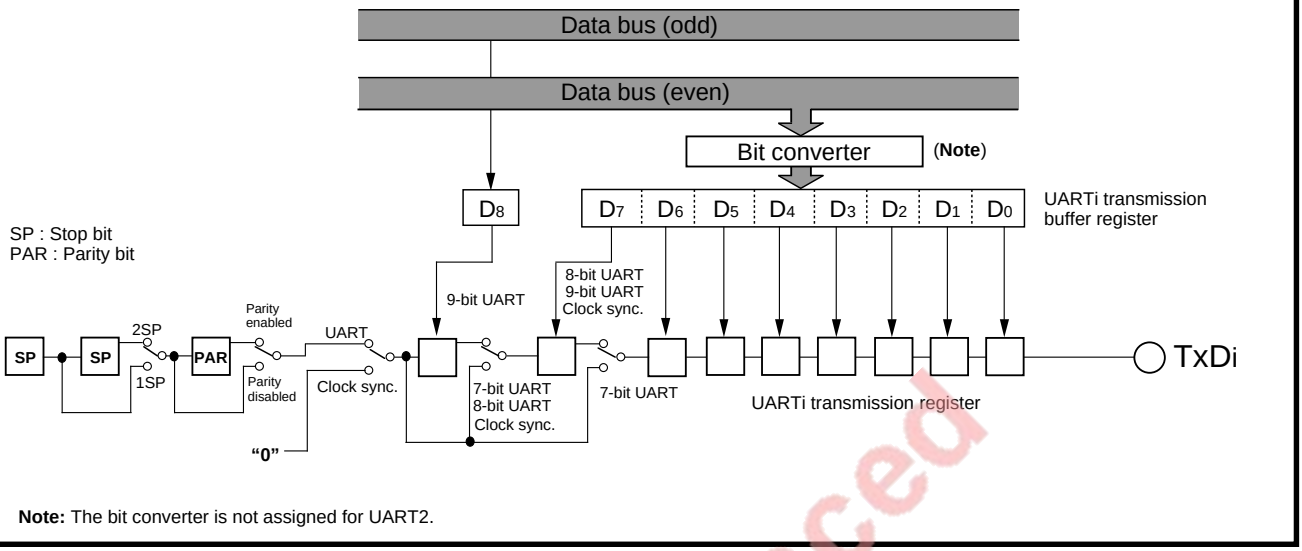
Note: Bits 4 and 5 are ignored in the UART mode. (They may be "0" or "1.")

Fig. 8.2.7 Structure of serial transmit control register

EOL announced

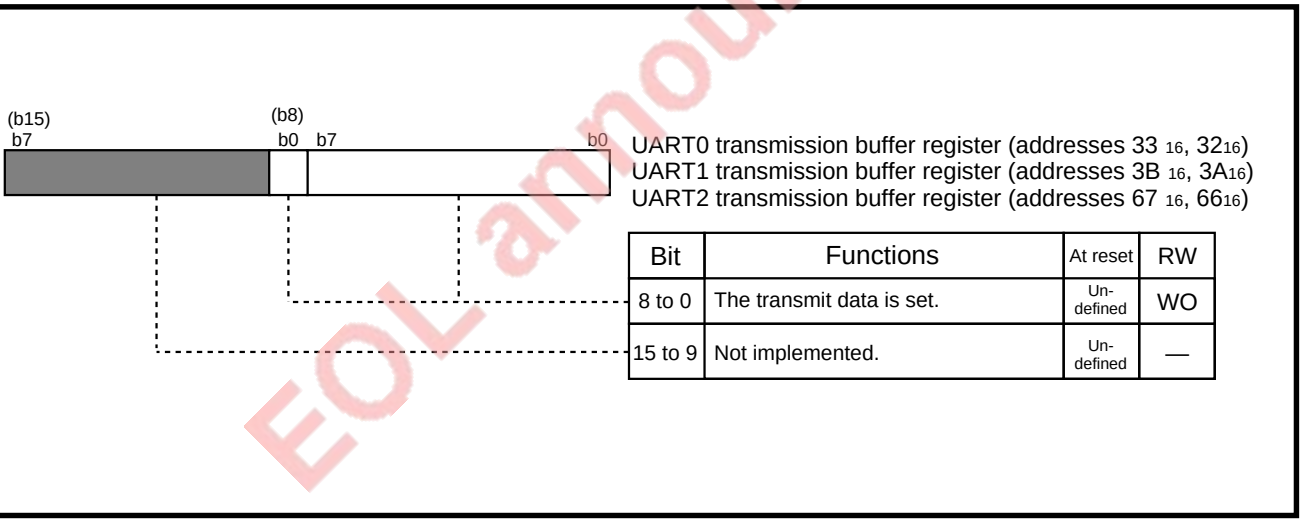
8.2.5 UARTi transmission register and UARTi transmission buffer register

Figure 8.2.8 shows the block diagram for the transmitter. Figure 8.2.9 shows the structure of the UARTi transmission buffer register.



Note: The bit converter is not assigned for UART2.

Fig. 8.2.8 Block diagram for transmitter



UART0 transmission buffer register (addresses 33 16, 3216)
UART1 transmission buffer register (addresses 3B 16, 3A16)
UART2 transmission buffer register (addresses 67 16, 6616)

Bit	Functions	At reset	RW
8 to 0	The transmit data is set.	Un-defined	WO
15 to 9	Not implemented.	Un-defined	—

Fig. 8.2.9 Structure of UARTi transmission buffer register

EOL announced

8.2 Block description

Transmit data is set into the UARTi transmission buffer register.
When the microcomputer operates in the clock synchronous serial I/O mode or when 7-bit or 8-bit length is selected as the transfer data's length in the UART mode, the transmit data is set into the low-order byte of this register. When 9-bit length is selected as the transfer data's length in the UART mode, the transmit data is set into the UARTi transmission buffer register as follows.

- Bit 8 of the transmit data is set into bit 0 of the high-order byte of the UARTi transmission buffer register.
- Bits 7 to 0 of the transmit data are set into the low-order byte of the UARTi transmission buffer register.

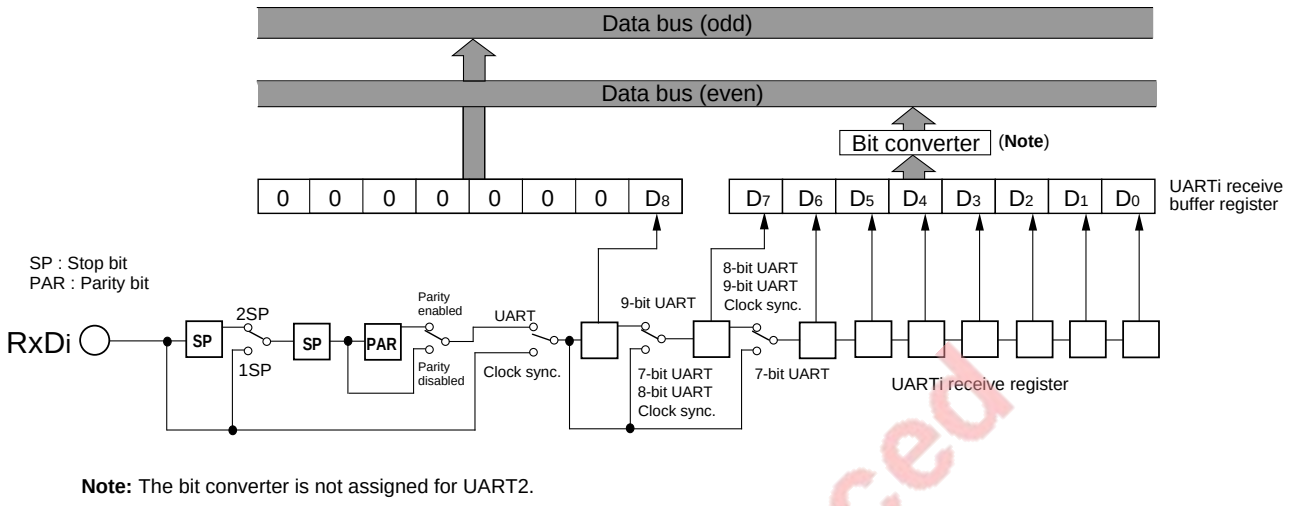
When transmit conditions are satisfied, the transmit data which is set in the UARTi transmission buffer register is transferred to the UARTi transmission register, and then it is output from the TxDi pin synchronously with the transfer clock. The UARTi transmission buffer register becomes empty when data which is set in this register is transferred to the UARTi transmission register, so the next transmit data can be set.
When the "MSB first" is selected in the clock synchronous serial I/O mode, bit position of set data is reversed, and then this data is written into the UARTi transmission buffer register as the transmit data. (Refer to section **"8.3.2 Transfer data format."**) Transmit operation itself is the same whichever format is selected, "LSB first" or "MSB first."
When quitting the transmission which is in progress and setting the UARTi transmission buffer register again, follow the procedure described below.

① Clear the serial I/O mode selection bits (bits 2 to 0 at addresses 30_{16}, 38_{16} and 64_{16}) to "000_2." (Serial I/O is ignored.)
② Set the serial I/O mode selection bits again.
③ Set the transmit enable bit (bit 0 at addresses 35_{16}, $3D_{16}$ and 69_{16}) to "1" (in other words, transmission is enabled.) and set the transmit data into the UARTi transmission buffer register.

EOL announced

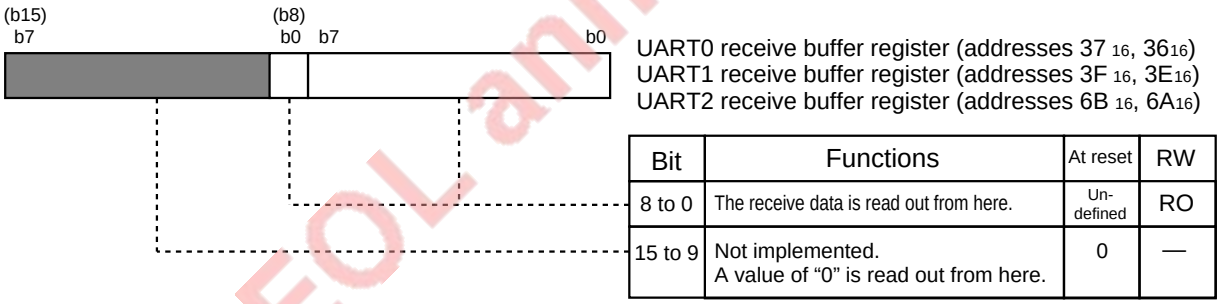
8.2.6 UARTi receive register and UARTi receive buffer register

Figure 8.2.10 shows the block diagram for the receiver. Figure 8.2.11 shows the structure of the UARTi receive buffer register.



Note: The bit converter is not assigned for UART2.

Fig. 8.2.10 Block diagram for receiver



UART0 receive buffer register (addresses 37_{16}, 36_{16})
UART1 receive buffer register (addresses $3F_{16}$, $3E_{16}$)
UART2 receive buffer register (addresses $6B_{16}$, $6A_{16}$)

Bit	Functions	At reset	RW
8 to 0	The receive data is read out from here.	Un-defined	RO
15 to 9	Not implemented. A value of "0" is read out from here.	0	—

Fig. 8.2.11 Structure of UARTi receive buffer register

EOL announced

8.2 Block description

The UARTi receive register is used to convert serial data, which is input from the RxDi pin, into parallel data. This register takes a signal which is input from the RxDi pin by the 1 bit synchronously with the transfer clock.

The UARTi receive buffer register is used to read receive data. When reception is completed, the receive data which is taken into the UARTi receive register is automatically transferred to the UARTi receive buffer register. Note that the contents of the UARTi receive buffer register is updated when the next data is ready in the UARTi receive register before data which has been transferred to the UARTi receive buffer register is read out (in other words, when an overrun error occurs).

When “MSB first” is selected in the clock synchronous serial I/O mode, bit position of data in the UARTi receive buffer register is reversed, and then this data is read out as the receive data. (Refer to section **“8.3.2 Transfer data format.”**) Receive operation itself is the same whichever format is selected, “LSB first” or “MSB first.”

The UARTi receive buffer register is initialized when the receive enable bit (bit 2 at addresses 35_{16}, $3D_{16}$ and 69_{16}) is set to “1” after clearing it to “0.”

Figure 8.2.12 shows the contents of the UARTi receive buffer register when reception is completed.

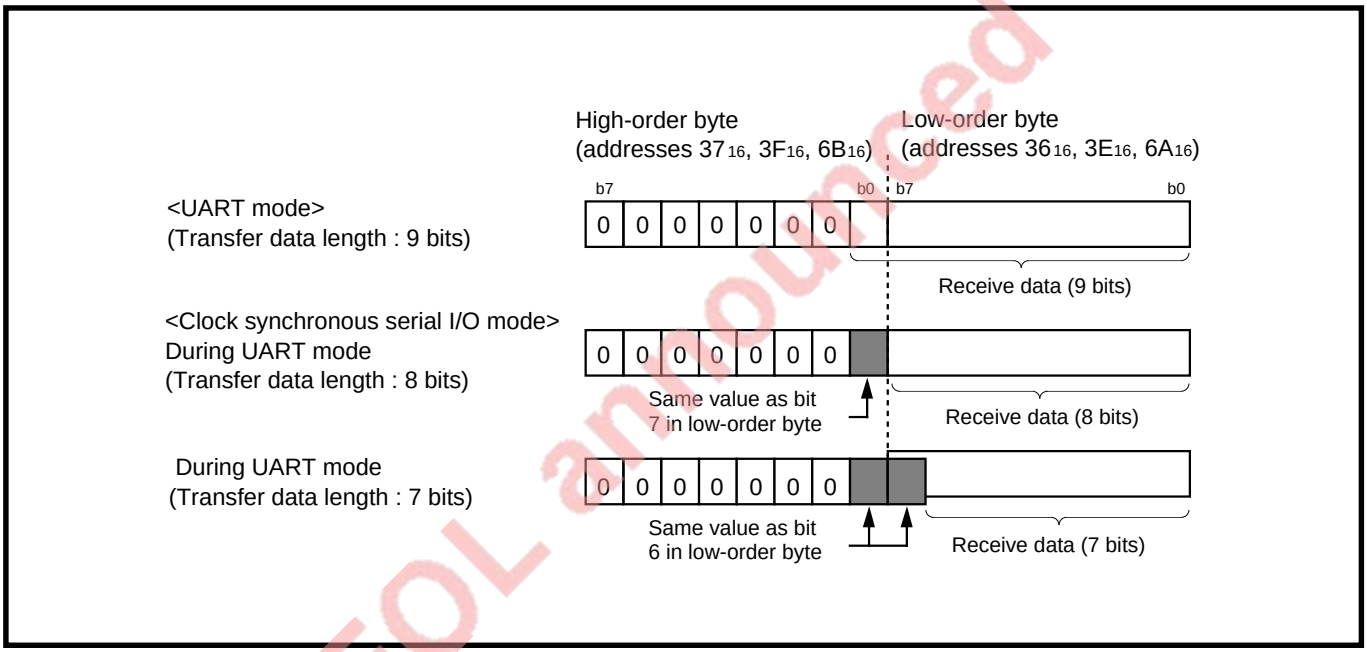


Fig. 8.2.12 Contents of UARTi receive buffer register when reception is completed

EOL announced

8.2.7 UARTi baud rate register (BRGi)

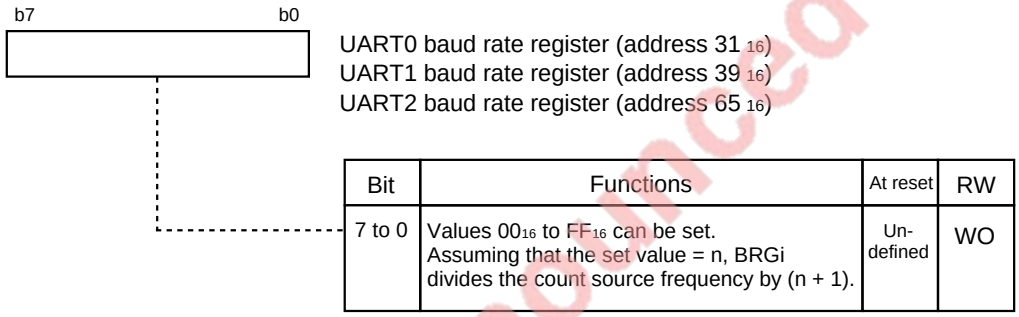
The UARTi baud rate register (BRGi) is an 8-bit timer used only for UARTi. It generates a transfer clock and has a reload register. Assuming that a value set in BRGi is “n” (n = 00_{16} to FF_{16}), the BRGi divides the count source frequency by (n + 1).

In the clock synchronous serial I/O mode, BRGi is valid when an internal clock is selected. At this time, the BRGi’s output divided by 2 is the transfer clock.

In the UART mode, the BRGi is always valid. At this time, the BRGi’s output divided by 16 is the transfer clock.

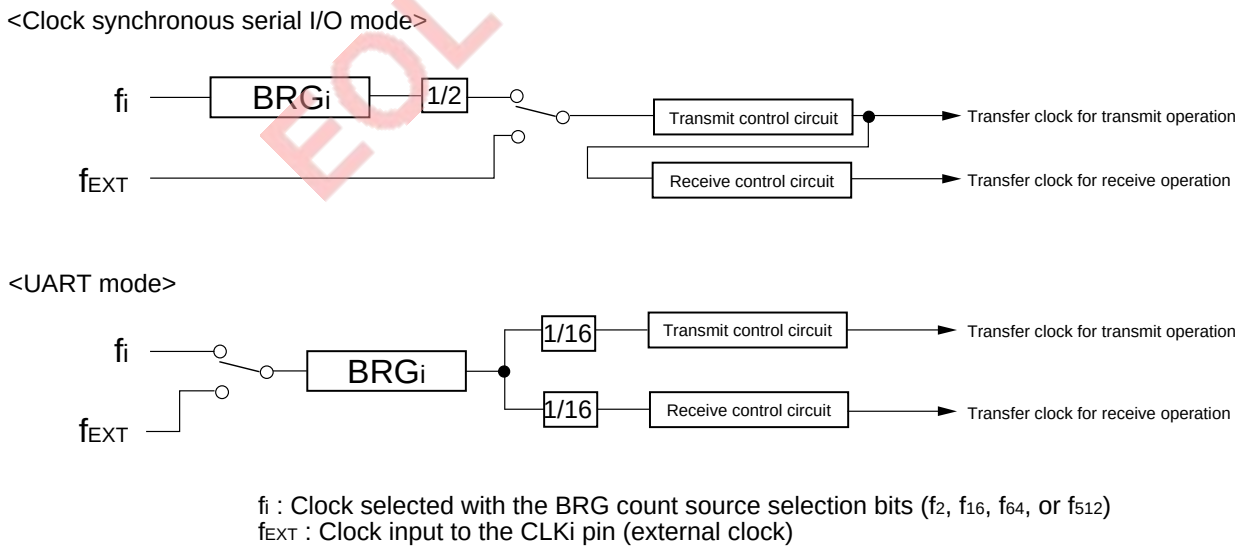
When a value is written to addresses 31_{16}, 39_{16}, and 65_{16}, the value is also written to the timer and the reload register whether transmission/reception is in progress or stopped. Therefore, when writing a value to these addresses, be sure to perform it while transmission/reception is stopped.

Figure 8.2.13 shows the structure of BRGi and Figure 8.2.14 shows the block diagram of transfer clock generating section.



Bit	Functions	At reset	RW
7 to 0	Values 00_{16} to FF_{16} can be set. Assuming that the set value = n, BRGi divides the count source frequency by (n + 1).	Un-defined	WO

Fig. 8.2.13 Structure of UARTi baud rate register (BRGi)



fi : Clock selected with the BRG count source selection bits (f_2, f_{16}, f_{64}, or f_{512})
f_{EXT} : Clock input to the CLKi pin (external clock)

Fig. 8.2.14 Block diagram of transfer clock generating section

EOL announced

8.2 Block description

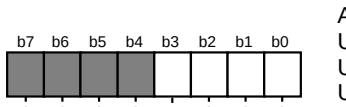
8.2.8 Interrupt control register related to UARTi

When UARTi is used, the following interrupts can be used: UARTi transmission interrupt and UARTi reception interrupt. Each interrupt has its corresponding interrupt control register. However, in UART2, an interrupt for transmission and an interrupt for reception are controlled with the same register. Figure 8.2.15 shows the structure of interrupt control registers related to UARTi.

For details about interrupts, refer to chapter **"4 Interrupts."**

The UART2 transmission/reception interrupt and the A-D conversion interrupt share the same interrupt vector addresses and interrupt control register.

Switching between the A-D conversion interrupt and the UART2 transmission/reception interrupt is performed with bits 2 to 0 of the UART2 transmission/reception mode register. (Refer to **Figure 8.2.3.**)



A-D/UART2 trans./rece. interrupt control register (address 70 16)
UART0 transmission interrupt control register (address 71 16)
UART0 receive interrupt control register (address 72 16)
UART1 transmission interrupt control register (address 73 16)
UART1 receive interrupt control register (addresses 74 16)

Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2 b1 b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 Priority is low. 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7 Priority is high.	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit	0: No interrupt has occurred. 1: Interrupt has occurred.	0 **(Note)**	RW
7 to 4	Not implemented.		Un-defined	—

Note: When the UART2 function is selected, bit 3 of the A-D conversion/UART2 trans./rece. interrupt control register is set to "1."
Accordingly, before enabling interrupts, write value "0" to this bit.

Fig. 8.2.15 Structure of interrupt control registers related to UARTi

EOL announced

(1) Interrupt priority level selection bits (bits 2 to 0)

These bits are used to select the priority level of the UARTi transmission interrupt or UARTi reception interrupt. When using the UARTi transmission/reception interrupt, select one of priority levels 1 to 7. When a UARTi transmission/reception interrupt request occurs, its priority level is compared with the processor interrupt priority level (IPL) and the requested interrupt is enabled only when its priority level is higher than the IPL. (Note that this is applied when the interrupt disable flag (I) = "0.") When these bits are set to "000_2" (level 0), the UARTi transmission/reception interrupt is disabled.

(2) Interrupt request bit (bit 3)

The UARTi transmission interrupt request bit is set to "1" when data is transferred from the UARTi transmission buffer register to the UARTi transmission register.

The UARTi reception interrupt request bit is set to "1" when data is transferred from the UARTi receive register to the UARTi receive buffer register. Note that these bits do not change when an overrun error occurs.

When each interrupt request is accepted, the corresponding interrupt request bit is automatically cleared to "0." Note that each bit can be set to "1" or cleared to "0" by software.

EOL announced

8.2 Block description

8.2.9 Ports P7 and P8 direction registers

I/O pins of UARTi are multiplexed with ports P7 and P8. When using the $P7_4$, $P8_2$ and $P8_6$ pins as serial data input pins (RxDi), set the corresponding bits of the ports P7 and P8 direction registers to "0" to set these ports for the input mode. When using the $P7_2$ pin as the $\overline{CTS_2}$ input pin, set bit 2 of the port P7 direction register to "0" to set this port for the input mode. When using the $P7_3$, $P7_5$, $P8_0$, $P8_1$, $P8_3$–$P8_5$, and $P8_7$ pins as UARTi's I/O pins ($\overline{CTSi}$/$\overline{RTSi}$, CLKi, TxDi), these pins are forcibly set as the UARTi's I/O pins, regardless of the ports P7 and P8 direction register's contents. Also, as for $CLKS_0$ and $CLKS_1$, refer to section **"8.3.1 (4) Number of transfer clock output pins (UART0)."** Figure 8.2.16 shows the relationship between the ports P7, P8 direction registers and UARTi's I/O pins.

Note that the functions of the UARTi's I/O pins can be switched by software. For details, refer to the description of each operating mode.

b7 b6 b5 b4 b3 b2 b1 b0

Port P7 direction register (address 11_{16})

Bit	Corresponding pin name	Functions	At reset	RW
0	Pin $P7_0$/AN_0	0: Input mode 1: Output mode When using pin $P7_2$ as the $\overline{CTS_2}$ input pin and using pin $P7_4$ as serial data's input pin (RxD_2), set the corresponding bit to "0."	0	RW
1	Pin $P7_1$/AN_1		0	RW
2	Pin $P7_2$/AN_2/$\overline{CTS_2}$		0	RW
3	Pin $P7_3$/AN_3/CLK_2		0	RW
4	Pin $P7_4$/AN_4/RxD_2		0	RW
5	Pin $P7_5$/AN_5/$\overline{ADTRG}$/TxD_2		0	RW
6	Pin $P7_6$/AN_6/$XCOUT$		0	RW
7	Pin $P7_7$/AN_7/$XCIN$		0	RW

b7 b6 b5 b4 b3 b2 b1 b0

Port P8 direction register (address 14_{16})

Bit	Corresponding pin name	Functions	At reset	RW
0	Pin $P8_0$/$\overline{CTS_0}$/$\overline{RTS_0}$/$CLKS_1$	0: Input mode 1: Output mode When using pins $P8_2$ and $P8_6$ as serial data's input pins (RxD_0, RxD_1), set the corresponding bits to "0."	0	RW
1	Pin $P8_1$/CLK_0		0	RW
2	Pin $P8_2$/RxD_0/$CLKS_0$		0	RW
3	Pin $P8_3$/TxD_0		0	RW
4	Pin $P8_4$/$\overline{CTS_1}$/$\overline{RTS_1}$		0	RW
5	Pin $P8_5$/CLK_1		0	RW
6	Pin $P8_6$/RxD_1		0	RW
7	Pin $P8_7$/TxD_1		0	RW

Note: For pins $CLKS_0$ and $CLKS_1$, refer to section **"8.3.1 (4) Number of transfer clock output pins (UART0)."**

: Not used for serial I/O

EOL announced

Fig. 8.2.16 Relationship between ports P7, P8 direction register and UARTi's I/O pins

8.3 Clock synchronous serial I/O mode

Table 8.3.1 lists the performance overview in the clock synchronous serial I/O mode and Table 8.3.2 lists the functions of I/O pins in this mode.

Table 8.3.1 Performance overview in clock synchronous serial I/O mode

Item		Functions
Transfer data format		Transfer data has a length of 8 bits. LSB first or MSB first is selected by software.
Transfer rate	When internal clock is selected	BRGi's output divided by 2
	When external clock is selected	Maximum of 5 Mbps
Transmit/Receive control		$\overline{CTS}$ function or $\overline{RTS}$ function is selected by software (**Note**).

Note: The $\overline{RTS}$ function is not assigned for UART2.

Table 8.3.2 Functions of I/O pins in clock synchronous serial I/O mode

Pin name	Functions	Method of selection
TxDi ($P8_3$, $P8_7$, $P7_5$)	Serial data output	—————— (They output dummy data when only reception is performed.)
RxDi ($P8_2$, $P8_6$, $P7_4$)	Serial data input	Ports P7 and P8 direction registers' corresponding bits ="0" (They can be used as input ports when only transmission is performed.)
CLKi ($P8_1$, $P8_5$, $P7_3$)	Transfer clock output	Internal/External clock selection bit = "0"
	Transfer clock input	Internal/External clock selection bit = "1"
$\overline{CTS_0}/\overline{RTS_0}$ ($P8_0$), $\overline{CTS_1}/\overline{RTS_1}$ ($P8_4$) (**Note 1**)	$\overline{CTS}$ input	$\overline{CTS}/\overline{RTS}$ enable bit = "0" $\overline{CTS}/\overline{RTS}$ function selection bit = "0"
	$\overline{RTS}$ output	$\overline{CTS}/\overline{RTS}$ enable bit = "0" $\overline{CTS}/\overline{RTS}$ function selection bit = "1"
	Programmable I/O port	$\overline{CTS}/\overline{RTS}$ enable bit = "1"
$\overline{CTS_2}$ ($P7_2$)	$\overline{CTS}$ input	$\overline{CTS}$ enable bit = "0"
	Programmable I/O port	$\overline{CTS}$ enable bit = "1"

Port P7 direction register: Address 11_{16}
Port P8 direction register: Address 14_{16}
Internal/External clock selection bit: Bit 3 at addresses 30_{16}, 38_{16}, and 64_{16}
$\overline{CTS}/\overline{RTS}$ enable bit: Bit 4 at addresses 34_{16} and $3C_{16}$
$\overline{CTS}/\overline{RTS}$ function selection bit: Bit 2 at addresses 34_{16} and $3C_{16}$
$\overline{CTS}$ enable bit: Bit 2 at address 68_{16}

❋ The TxDi pin outputs "H" level from when a UARTi's operating mode is selected until transfer starts. (The TxDi pin is in a floating state when N-channel open-drain output is selected.)
❋ In UART0, multiple transfer clock output pins can be used. (Refer to **Table 8.3.3.**)

Notes 1: The $\overline{RTS}$ function is not assigned for UART2.
2: As for $CLKS_0$ and $CLKS_1$, refer to section **"8.3.1 (4) Number of transfer clock output pins (UART0)."**

EOL announced

8.3 Clock synchronous serial I/O mode

8.3.1 Transfer clock (sync clock)

Data is transferred synchronously with the transfer clock. For the transfer clock, the following items can be specified:

- Whether to generate the transfer clock internally or to input it from the external.
- Polarity of a clock which is output from the CLKi pin (UART0, UART1)
- Number of transfer clock output pins (UART0).

Note that the transfer clock is generated while the transmit control circuit is operating. Therefore, even when performing only reception, set the transmit enable bit to "1" and make the transmit control circuit operate by setting dummy data into the UARTi transmission buffer register.

(1) How to generate transfer clock internally

A count source is selected with the BRG count source selection bits. The count source is divided in the BRGi, and then the BRGi's output is further divided by 2. (In this way, the transfer clock is generated.) This transfer clock is output from the CLKi pin.

[Setting for related registers]

- An internal clock is selected (bit 3 at addresses 30_{16}, 38_{16}, and 64_{16} = "0").
- The BRGi's count source is selected (bits 1 and 0 at addresses 34_{16}, $3C_{16}$, and 68_{16}).
- A value of "divide value – 1" (= n: 00_{16} to FF_{16}) is set into the BRGi (addresses 31_{16}, 39_{16}, and 65_{16}).

$$\text{Transfer clock's frequency} = \frac{fi}{2\ (n+1)}$$ fi: BRGi's count source frequency (f_2, f_{16}, f_{64}, and f_{512})

- Transmission is enabled (bit 0 at addresses 35_{16}, $3D_{16}$, and 69_{16} = "1").
- Data is set into the UARTi transmission buffer register (addresses 32_{16}, $3A_{16}$, and 66_{16})

[Pin status]

- Transfer clock is output from the CLKi pin.
- Serial data is output from the TxDi pin. (Dummy data is output when only reception is performed.)

(2) How to input transfer clock from the external

A clock which is input from the CLKi pin is the transfer clock.

[Setting related registers]

- An external clock is selected (bit 3 at addresses 30_{16}, 38_{16}, and 64_{16} = "1").
- Transmission is enabled (bit 0 at addresses 35_{16}, $3D_{16}$, and 69_{16} = "1").
- Data is set into the UARTi transmission buffer register (addresses 32_{16}, $3A_{16}$, 66_{16}).

[Pin status]

- Transfer clock is input from the CLKi pin.
- Serial data is output from the TxDi pin. (Dummy data is output when only reception is performed.)

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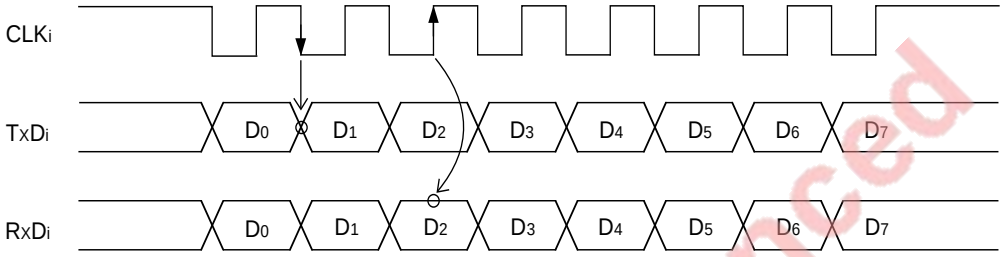
(3) How to select polarity of transfer clock

The polarity of a clock which is output from the CLKi pin can be selected with the CLK polarity selection bit (UART0, UART1) as shown in Figure 8.3.1. The CLK polarity select bit is not implemented for UART2. The CLK_2 pin outputs the transmit data at the fall of the transfer clock; this pin inputs the receive data at the rise of the transfer clock.

[Setting for related registers]

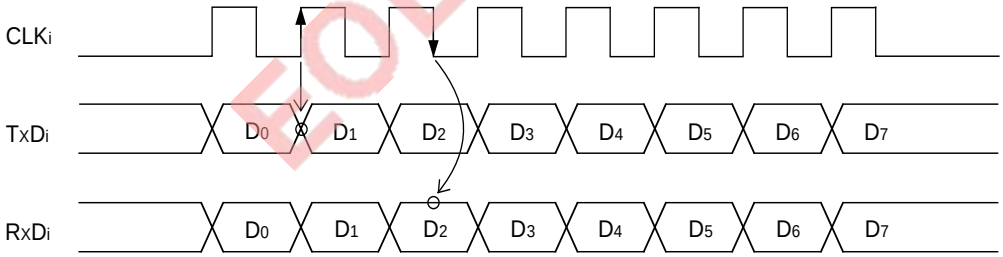
● The CLK polarity is selected (bit 6 at addresses 34_{16}, $3C_{16}$).

■ When CLK polarity selection bit = "0."



❋ The transmit data is output to the TxDi pin at the falling edge of the transfer clock; the receive data is input from the RxDi pin at the rising edge of the transfer clock.
When not transferring, the CLKi pin's level is "H."

■ When CLK polarity selection bit = "1."



❋ The transmit data is output to the TxDi pin at the rising edge of the transfer clock; the receive data is input from the RxDi pin at the falling edge of the transfer clock.
When not transferring, the CLKi pin's level is "L."

Fig. 8.3.1 Polarity of transfer clock

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8.3 Clock synchronous serial I/O mode

(4) Number of transfer clock output pins (UART0)

Only in UART0, when an internal clock is selected, one pin can be selected as the transfer clock output pin from the following pins: CLK_0, $CLKS_0$ (in common with RxD_0), and $CLKS_1$ (in common with $\overline{CTS_0}/\overline{RTS_0}$).

By this selection, data can be transmitted to the maximum of three external receiving devices. (Refer to ① in **Table 8.3.4**). In this case, since the RxD_0 and $\overline{CTS_0}/\overline{RTS_0}$ pins function as the transfer clock output pins (CLK_0, $CLKS_1$), the $\overline{CTS}/\overline{RTS}$ function and reception are disabled.

When only the CLK_0 and $CLKS_0$ pins are used as the transfer clock output pins, the $P8_0$ ($\overline{CTS_0}/\overline{RTS_0}$/$CLKS_1$) pin can be used as a programmable I/O port. (Refer to ② in **Table 8.3.4.**)

Also, when the CLK_0 and $CLKS_1$ pins are used as the transfer clock output pins and bit 2 of the port P8 direction register is set to "0," data can be received from the RxD_0 pin. (Refer to ③ in **Table 8.3.4.**)

[Setting for related registers]

- An internal clock is selected (bit 3 at address 30_{16} = "0").
- The $\overline{CTS}/\overline{RTS}$ function is disabled (bit 4 at address 34_{16} = "1").
- Reception is disabled (bit 2 at address 35_{16} = "0"). (Refer to ① and ② in **Table 8.3.4.**)
- Number of transfer clock output pins is selected. (bits 5 and 4 at address $6E_{16}$; Refer to **Table 8.3.3.)**
- Conditions for "output when not transferring" (described later) are set.
  ($CLKS_0$: bit 2 at address 14_{16} = "1":
  $CLKS_1$: bit 0 at address 14_{16} = "1," bit 0 at address 12_{16} = level at "output when not transferring")

[Pin status]

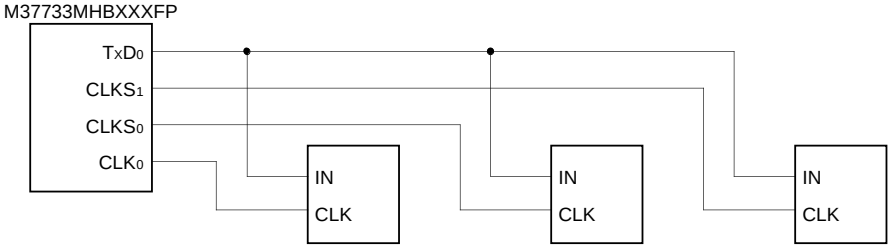
Refer to **Table 8.3.3**.

Table 8.3.3 Pin functions when one transfer clock output pin is selected

Transfer clock output pin selection bits		Number of pins from which one transfer clock output pin is selected	Functions			
b5	b4		$\overline{CTS_0}/\overline{RTS_0}/CLKS_1$ ($P8_0$)	CLK_0 ($P8_1$)	$RxD_0/CLKS_0$ ($P8_2$)	TxD_0 ($P8_3$)
0	0	1	Programmable I/O port	Outputs transfer clock.	Programmable I/O port	Outputs serial data.
0	1	Selectable	Programmable I/O port	Outputs transfer clock.	❋	
1	0		Programmable I/O port	Output when not transferring*	Outputs transfer clock.	
1	1		Outputs transfer clock.	Output when not transferring*	❋	

Output when not transferring*: When the CLK polarity selection bit (bit 6 at address 34_{16}) = "0," the CLK_0 pin outputs "H" level; when this bit = "1," the CLK_0 pin outputs "L" level.

❋ When bit 2 at address 14_{16} (port P8 direction register) = "0," the $RxD_0/CLKS_0$ pin is in a floating state; when this bit = "1," the $RxD_0/CLKS_0$ pin do the processing of "output when not transferring."



Note: This is applied when the following conditions are satisfied:
- Only transmission is performed.
- Clock synchronous serial I/O mode is selected.
- An internal clock is selected.

Fig. 8.3.2 Connection example when one transfer clock output pin is selected from three pins

ECU announced

[Switching of transfer clock output pin]
When the transfer clock output pin is switched while transmission is enabled, follow the procedure described below. Transmission starts when step ③ is executed:

① Check whether the previous transfer is completed or not. (Refer to **Figure 8.3.6.**)
② If the previous transfer has been completed, change the contents of the transmit clock output pin selection bit.
③ Set the transmit data.

For usage examples, refer to section **"17.2.2 Examples of transmission for several peripheral ICs (Clock synchronous serial I/O mode)."**

Table 8.3.4 Number of channels for serial I/O transmission/reception for the case where multiple transfer clock output pins are used

Pin	Setting example		
	①	②	③
$\overline{CTS_0}/\overline{RTS_0}/CLKS_1$ ($P8_0$)	Outputs transfer clock.	Programmable I/O port	Outputs transfer clock.
CLK_0 ($P8_1$)	Outputs transfer clock.	Outputs transfer clock.	Outputs transfer clock.
$RxD_0/CLKS_0$ ($P8_2$)	Outputs transfer clock.	Outputs transfer clock.	Receives data.
TxD_0 ($P8_3$)	Transmits data.	Transmits data.	Transmits data.
•Number of channels for serial I/O transmission/ reception •Status of transmit clock output pin selection bits (b5, b4)	3 channels for transmission {$CLKS_1$, TxD_0} (1, 1) {CLK_0, TxD_0} (0, 1) {$CLKS_0$, TxD_0} (1, 0)	2 channels for transmission {CLK_0, TxD_0} (0, 1) {$CLKS_0$, TxD_0} (1, 0)	1 channel for transmission {$CLKS_1$, TxD_0} (1, 1) 1 channel for transmission/reception {CLK_0, RxD_0, TxD_0} (0, 1)

Note: Set bit 2 at address 14_{16} (port P8 direction register) to "0."

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8.3 Clock synchronous serial I/O mode

8.3.2 Transfer data format

LSB-first or MSB-first can be selected (UART0, UART1). Table 8.3.5 lists the relationship between the transfer data format and the way to write/read to and from the UARTi transmission/receive buffer register. By setting the transfer format selection bit (bit 7 at addresses 34_{16}, $3C_{16}$), transfer data format can be selected.

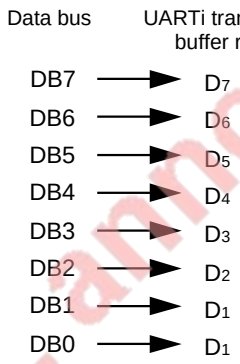
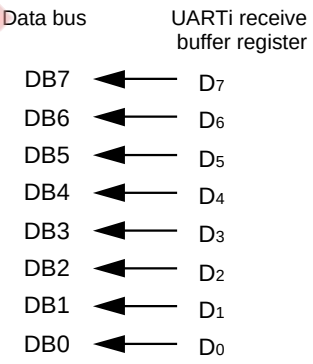
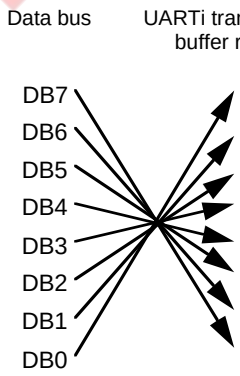
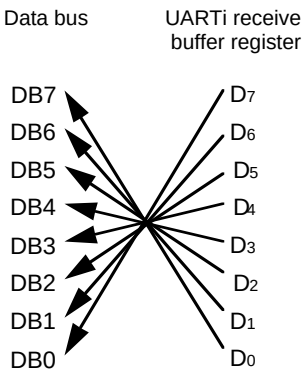
When this bit is cleared to "0," the set data is written to the UARTi transmission buffer register as the transmit data. Similarly, the data in the UARTi receive buffer register is read out as the receive data. (Refer to **the upper row in Table 8.3.5.**)

When this bit is set to "1," each bit's position of the set data is reversed, and then this data is written to the UARTi transmission buffer register as the transmit data. Similarly, each bit's position of data in the UARTi receive buffer register is reversed, and then this data is read out as the receive data. (Refer to **the lower row in Table 8.3.5.**)

Note that only the way to write/read to and from the UARTi transmission/receive buffer register is affected by the transfer data format. The transmit/receive operation is unaffected.

The transfer data format for UART2 is fixed to "LSB-first."

Table 8.3.5 Relationship between transfer data format and way to write/read to and from UARTi transmission/receive buffer register

Transfer format selection bit	Transfer data format	When data is written to UARTi transmission buffer register	When data is read from UARTi receive buffer register
0	LSB (Least Significant Bit) first		
1	MSB (Most Significant Bit) first		

EOL announced

8.3.3 Method of transmission

Figures 8.3.3 and 8.3.4 show initial setting examples for related registers when transmitting. Transmission is started when all of the following conditions (① to ③) are satisfied. When an external clock is selected, satisfy conditions ① to ③ with the following preconditions satisfied.

[Preconditions for UART0 and UART1]

- The CLKi pin's input is at "H" level.
  (When an external clock is selected and the CLK polarity selection bit = "0.")
- The CLKi pin's input is at "L" level.
  (When an external clock is selected and the CLK polarity selection bit = "1.")

Note: When an internal clock is selected, the above preconditions are ignored.

[Preconditions for UART2]

- The CLKi pin's input is at "H" level.
  (When an external clock is selected)

Note: When an internal clock is selected, the above precondition is ignored.

① Transmit enable state (transmit enable bit = "1")
② Transmit data is present in the UARTi transmission buffer register (transmission buffer empty flag = "0").
③ The $\overline{\text{CTSi}}$ pin's input is at "L" level (when the $\overline{\text{CTS}}$ function is selected)

Note: When the $\overline{\text{CTS}}$ function is not selected or in UART2, this condition is ignored.

By connecting the $\overline{\text{RTSi}}$ pin (receiver side) and $\overline{\text{CTSi}}$ pin (transmitter side), the timing of transmission and that of reception can be matched (UART0, UART1). For details, refer to section **"8.3.6 Receive operation."** When using interrupts, settings for enabling interrupts are required. For details, refer to chapter **"4. Interrupts."**

Figure 8.3.5 shows how to write data after transmission is started and Figure 8.3.6 shows how to detect the transmit completion.

EOL announced

8.3 Clock synchronous serial I/O mode

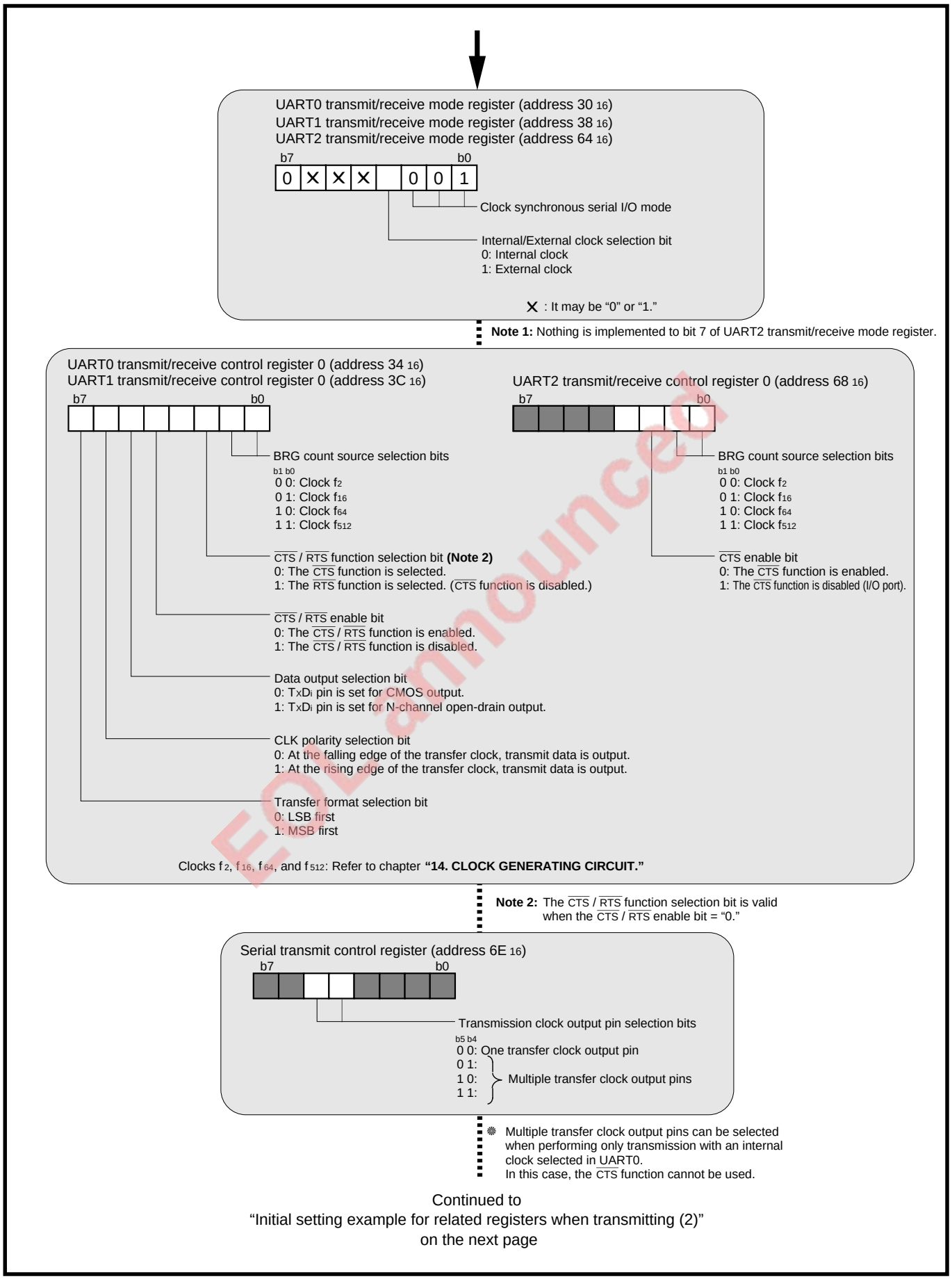


Fig. 8.3.3 Initial setting example for related registers when transmitting (1)

Pre-announced EOL

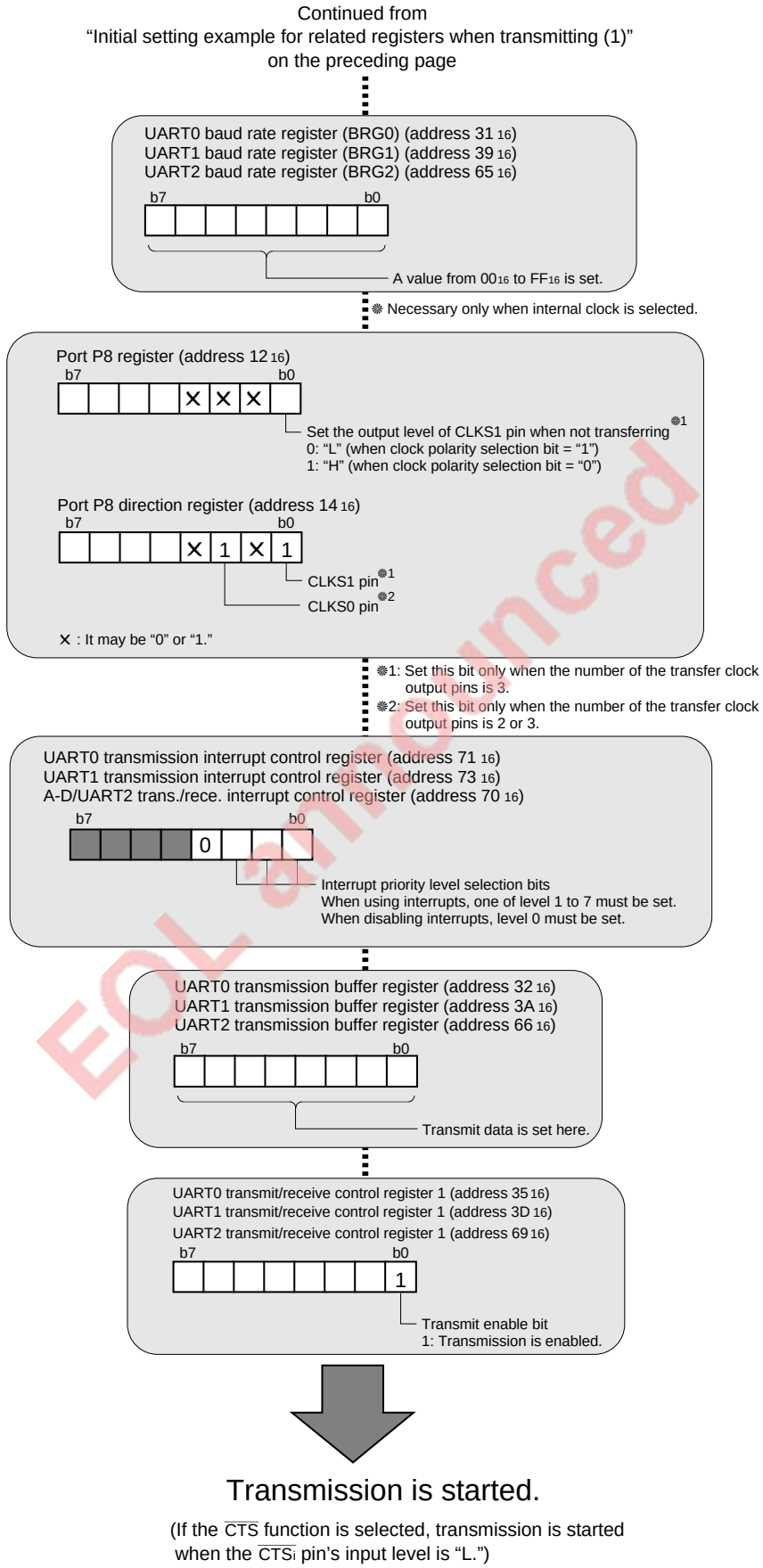


Fig. 8.3.4 Initial setting example for related registers when transmitting (2)

EOL announced

8.3 Clock synchronous serial I/O mode

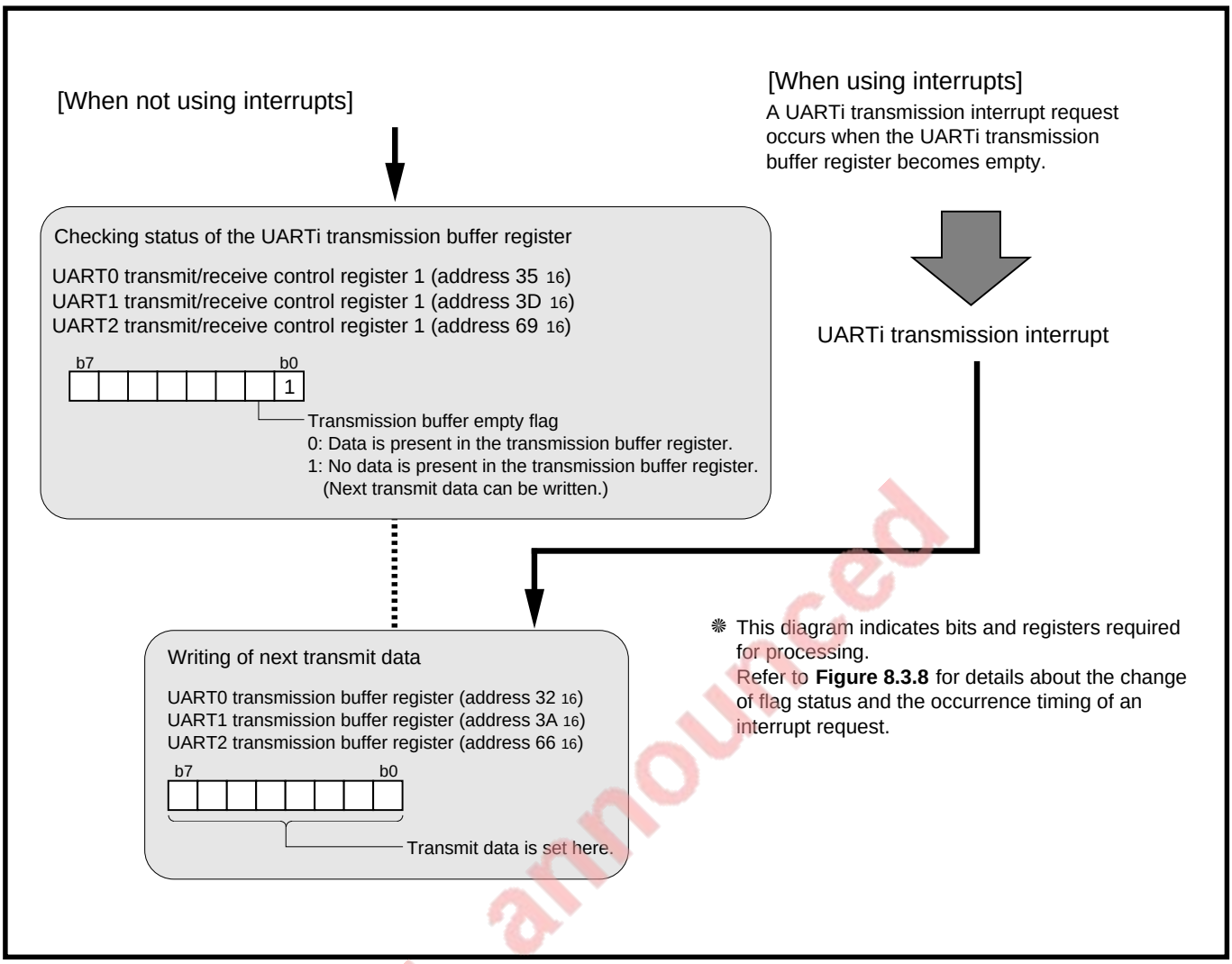


Fig. 8.3.5 How to write data after transmission is started

EOL announced

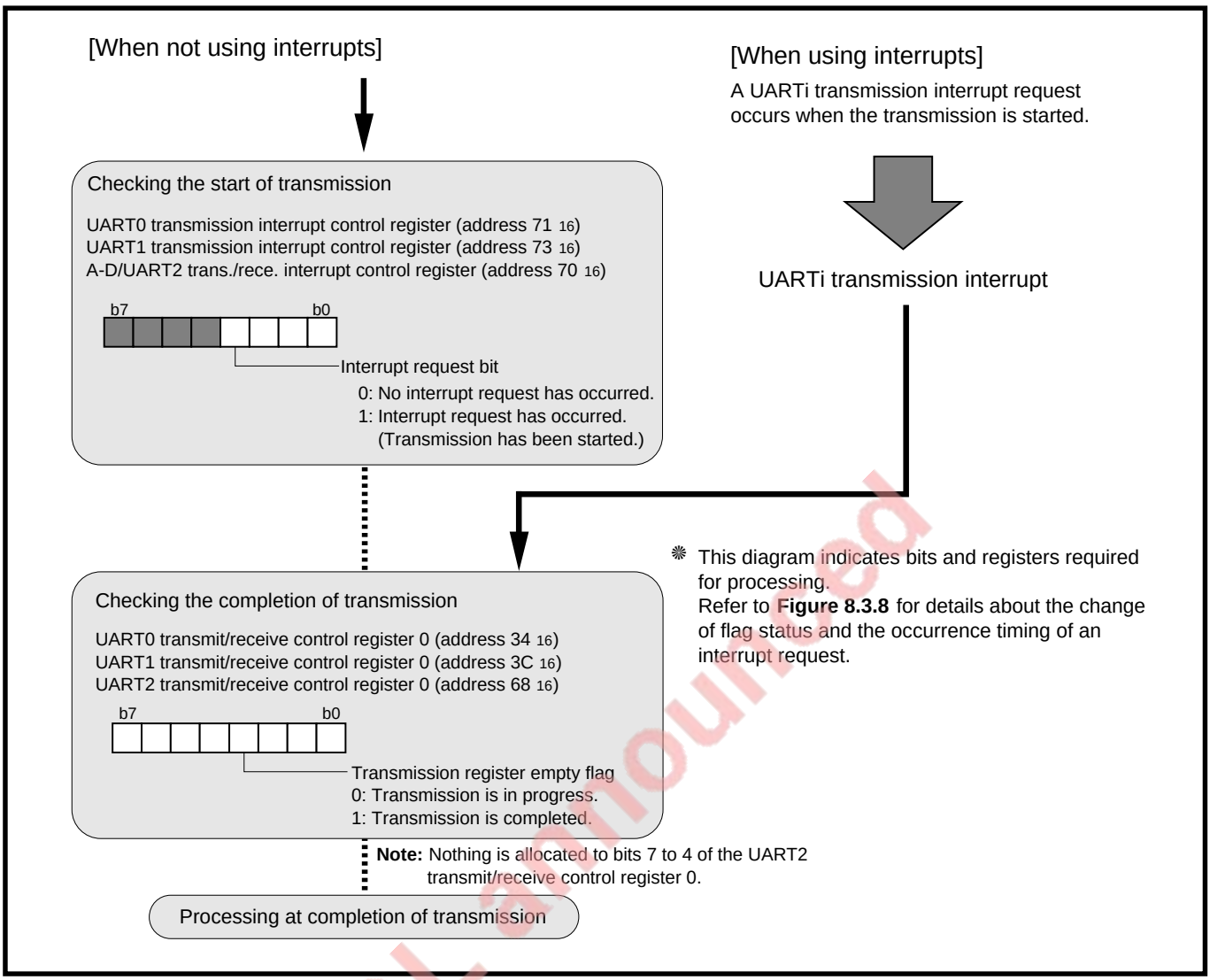


Fig. 8.3.6 How to detect of transmit completion

EOL announced

8.3 Clock synchronous serial I/O mode

8.3.4 Transmit operation

When the transmit conditions described in section **"8.3.3 Method of transmission"** are satisfied while an internal clock is selected, the transfer clock is generated. And then, the following operations are automatically performed after one cycle of the transfer clock has passed.
When the transmit conditions are satisfied and the external clock is input to the CLKi pin while the external clock is selected, the following operations are automatically performed.

- The UARTi transmission buffer register's contents is transferred to the UARTi transmission register.
- The transmission buffer empty flag is set to "1."
- The transmission register empty flag is cleared to "0."
- A UARTi transmission interrupt request occurs and the interrupt request bit is set to "1."
- Eight transfer clocks are generated (when an internal clock is selected).

The transmit operation is described below.

① Data in the UARTi transmission register is transmitted from the TxDi pin synchronously with the valid edge* of the CLKi pin's clock.
② This data is transmitted bit by bit sequentially beginning with the least significant bit (LSB).
③ When one byte of data has been transmitted, the transmission register empty flag is set to "1." This indicates the completion of transmission.

Valid edge*: In UART0 and UART1, this means the falling edge when the CLK polarity selection bit = "0" and the rising edge when the CLK polarity selection bit = "1"; in UART2, this means the rising edge.

Figure 8.3.7 shows the transmit operation.
When an internal clock is selected, if the transmit conditions for the next data are satisfied at completion of transmission, the next transfer clock is generated immediately. Accordingly, when performing transmission in succession, set the next transmit data to the UARTi transmission buffer register during transmission (when the transmission register empty flag = "0"). When the transmit conditions for the next data are not satisfied, the transfer clock stops at "H" level when the CLK polarity selection bit = "0," and it stops at "L" level when the CLK polarity selection bit = "1."
Figure 8.3.8 shows an example of transmit timing (when an internal clock and the $\overline{\text{CTS}}$ function are selected).
4

EOL announced

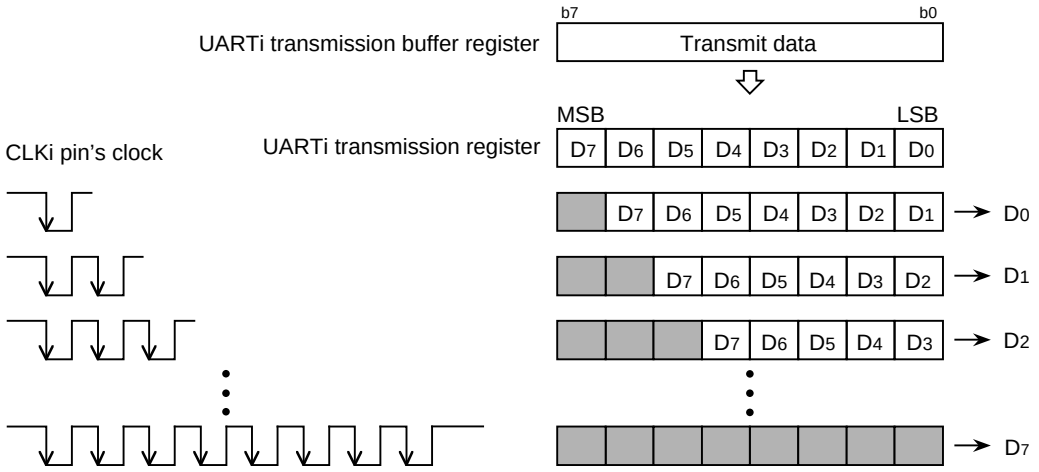


Fig. 8.3.7 Transmit operation

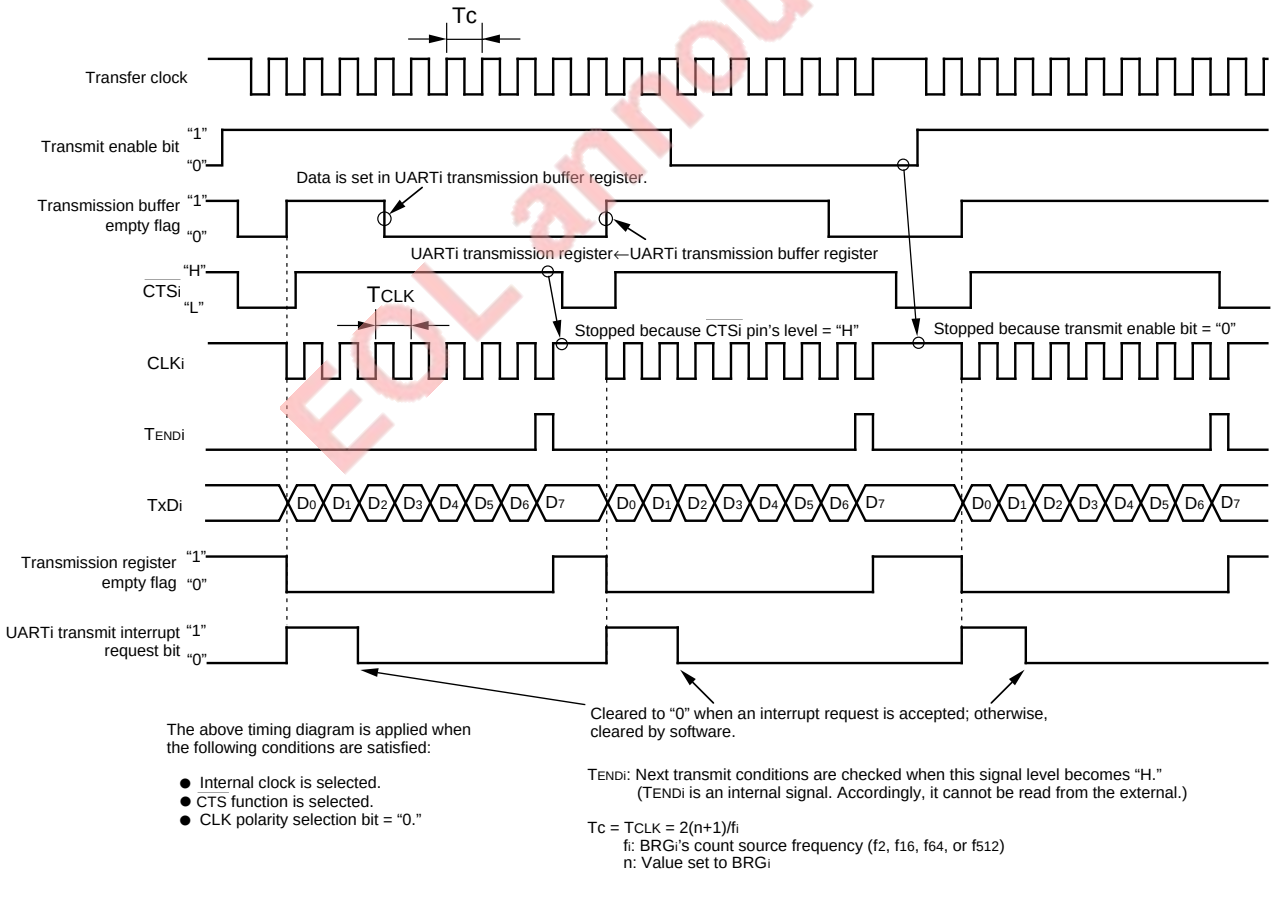


Fig. 8.3.8 Example of transmit timing (when internal clock and CTS function are selected)

EOL announced

8.3 Clock synchronous serial I/O mode

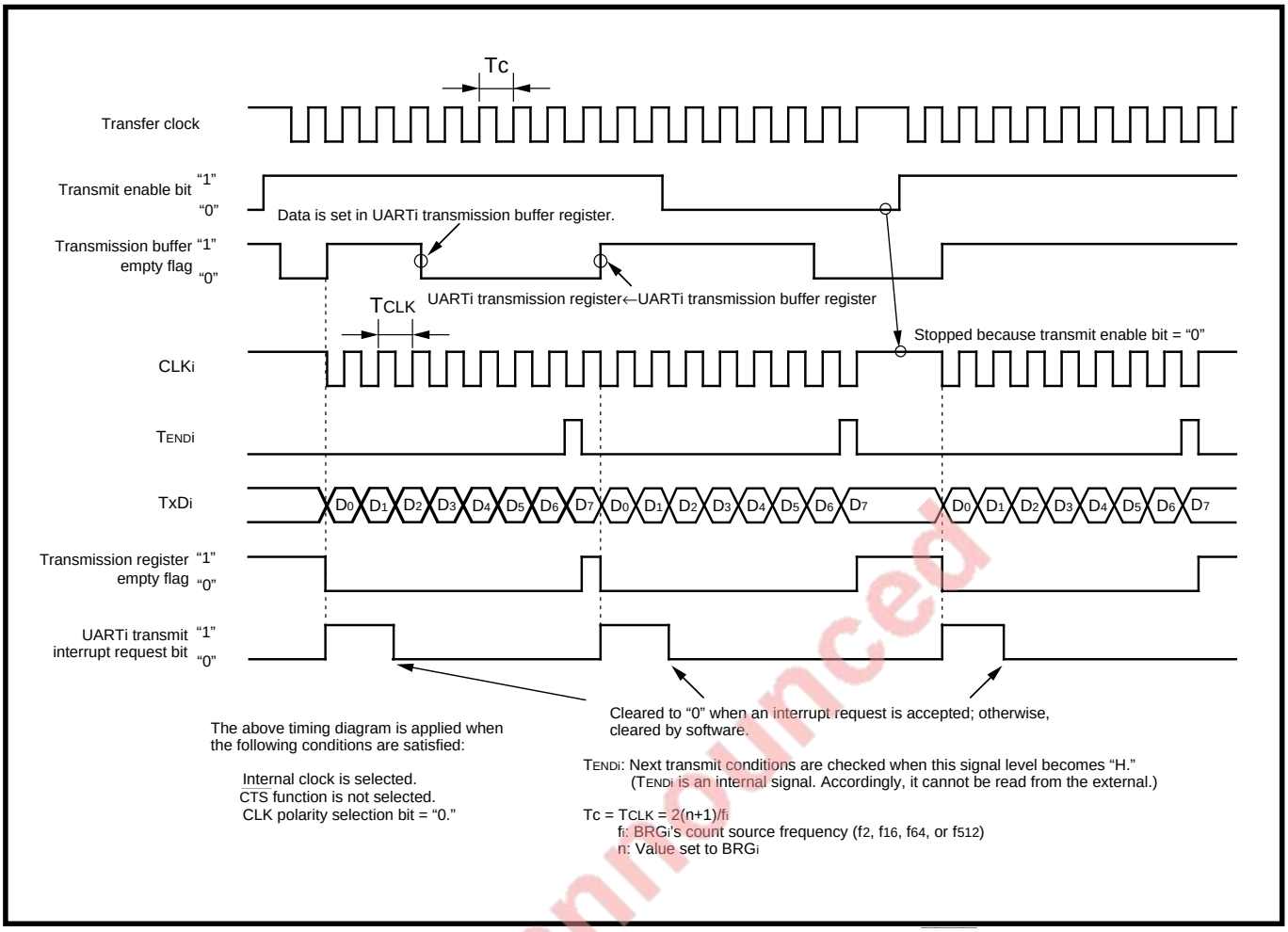


Fig. 8.3.9 Example of transmit timing (when internal clock is selected and CTS function is not selected)

EOL announced

8.3.5 Method of reception

Figures 8.3.10 and 8.3.11 show initial setting examples for related registers when receiving. Reception is started when all of the following conditions (① to ③) are satisfied. When an external clock is selected, satisfy conditions ① to ③ with the following preconditions satisfied.

[Preconditions for UART0 and UART1]

- The CLKi pin's input is at "H" level.
  (When an external clock is selected and the CLK polarity selection bit = "0.")
- The CLKi pin's input is at "L" level.
  (When an external clock is selected and the CLK polarity selection bit = "1.")

Note: When an internal clock is selected, the above preconditions are ignored.

[Preconditions for UART2]

- The CLKi pin's input is at "H" level.
  (When an external clock is selected)

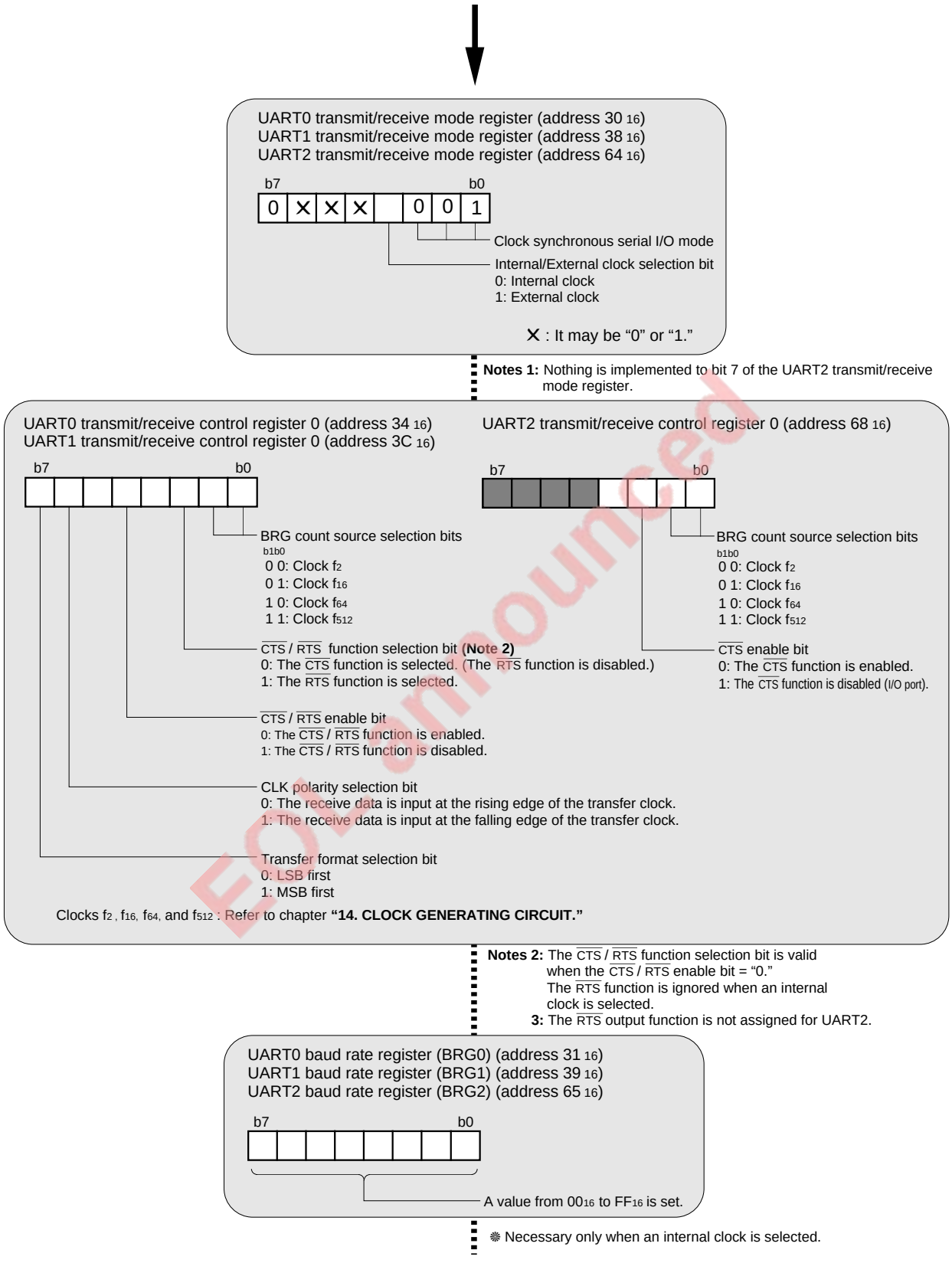
Note: When an internal clock is selected, the above precondition is ignored.

① Receive enable state (receive enable bit = "1")
② Transmit enable state (transmit enable bit = "1")
③ Dummy data is present in the UARTi transmission buffer register (transmission buffer empty flag = "0").

By connecting the $\overline{\text{RTSi}}$ pin (receiver side) and $\overline{\text{CTSi}}$ pin (transmitter side), the timing of transmission and that of reception can be matched (UART0, UART1). For details, refer to section **"8.3.6 Receive operation."** When using interrupts, settings for enabling interrupts are required. For details, refer to chapter **"4. Interrupts."**
Figure 8.3.12 shows the processing after reception is completed.

EOL announced

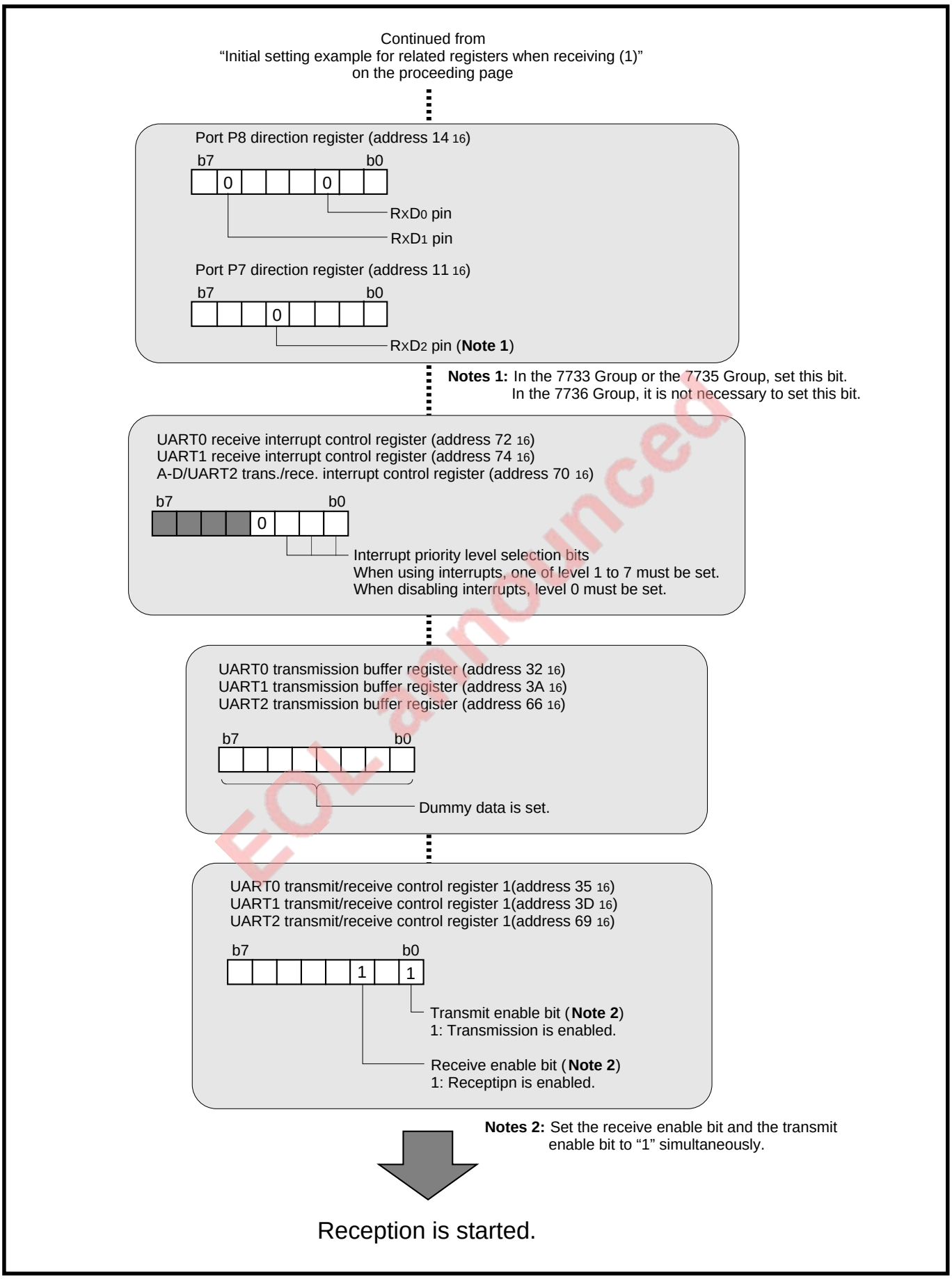
8.3 Clock synchronous serial I/O mode



Continued to
"Initial setting example for related registers when receiving (2)"
on the next page

Fig. 8.3.10 Initial setting example for related registers when receiving (1)

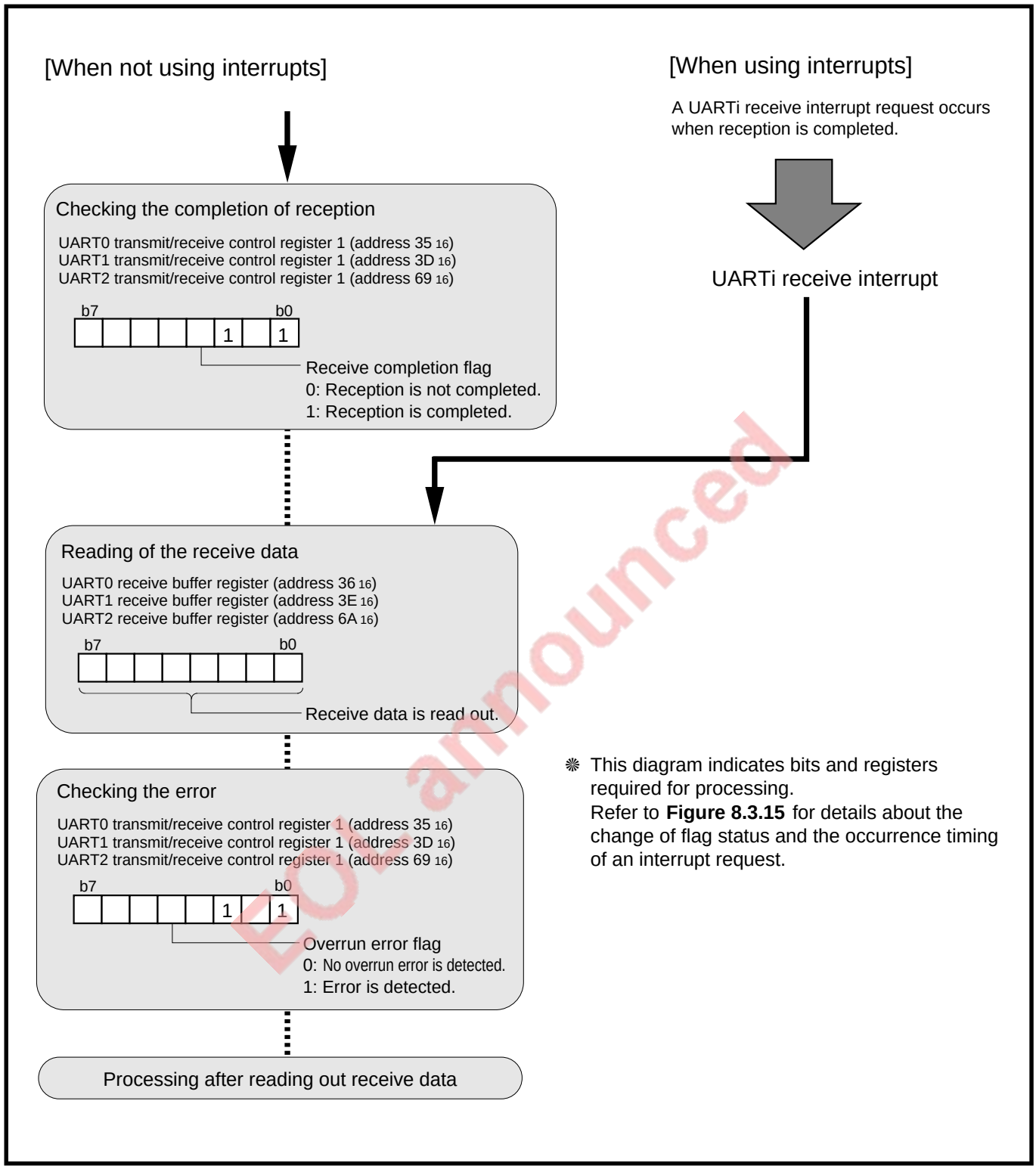
Engineering Announced



EOL announced

Fig. 8.3.11 Initial setting example for related registers when receiving (2)

8.3 Clock synchronous serial I/O mode



EOT announced

Fig. 8.3.12 Processing after reception is completed

8.3.6 Receive operation

When the receive conditions described in section **"8.3.5 Method of reception"** are satisfied while an internal clock is selected, the transfer clock is generated. And then, the receive is started after one cycle of the transfer clock has passed.
When the receive conditions are satisfied while the external clock is selected, UARTi is in the reception enabled state. Then, the external clock is input to the CLKi pin and reception is started.
In UART0 and UART1, when the $\overline{\text{RTS}}$ function is selected with an external clock selected, the $\overline{\text{RTSi}}$ pin's output level is "L," and the microcomputer informs the transmitter side that reception is enabled. When reception is started, the $\overline{\text{RTSi}}$ pin's output level is "H." Accordingly, by connecting the $\overline{\text{RTSi}}$ pin to the $\overline{\text{CTSi}}$ pin of the transmitter side, the timing of transmission and that of reception can be matched.
When an internal clock is selected, do not use the $\overline{\text{RTS}}$ function because the $\overline{\text{RTSi}}$ output is undefined.
Figure 8.3.13 shows a connection example.
The $\overline{\text{RTS}}$ output function is not assigned for UART2.

The receive operation is described below.

① The signal which is input from the RxDi pin is taken in the most significant bit of the UARTi receive register synchronously with the valid edge* of the clock which is output from the CLKi pin or input to the CLKi pin.
② The contents of the UARTi receive register is shifted by 1 bit to the right.
③ Operations ① and ② are repeated at each valid edge of the clock which is output from the CLKi pin or input to the CLKi pin.
④ When one byte of data is prepared in the UARTi receive register, the contents of this register is transferred to the UARTi receive buffer register.
⑤ Simultaneously with ④, the receive completion flag is set to "1." At this time, a receive interrupt request occurs, and then an interrupt request bit is set to "1."

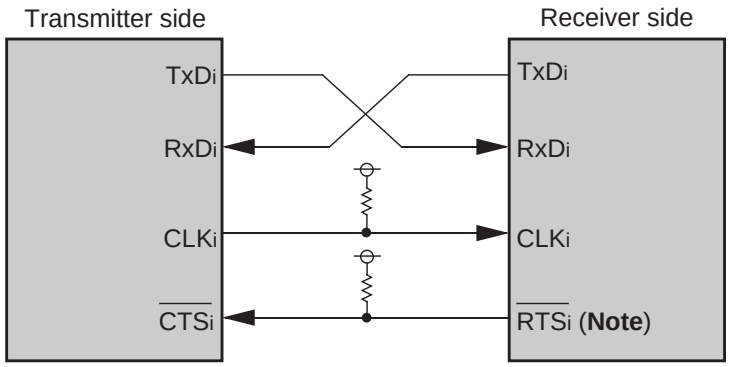
Valid edge* : In UART0 and UART1, this means the rising edge when the CLK polarity selection bit = "0" and the falling edge when the CLK polarity selection bit = "1"; in UART2, this means the rising edge.

The receive completion flag is cleared to "0" when the low-order byte of the UARTi receive buffer register is read out. The $\overline{\text{RTSi}}$ pin continues to output "H" level until the receive conditions are next satisfied (when the $\overline{\text{RTS}}$ function is selected). Figure 8.3.14 shows the receive operation and Figure 8.3.15 shows an example of receive timing (when an external clock is selected).
When the contents of the UARTi receive buffer register is read out with the transfer format selection bit = "1" (MSB first), each bit's position of this register's contents is reversed and the resultant data is read out (UART0, UART1).

EOL announced

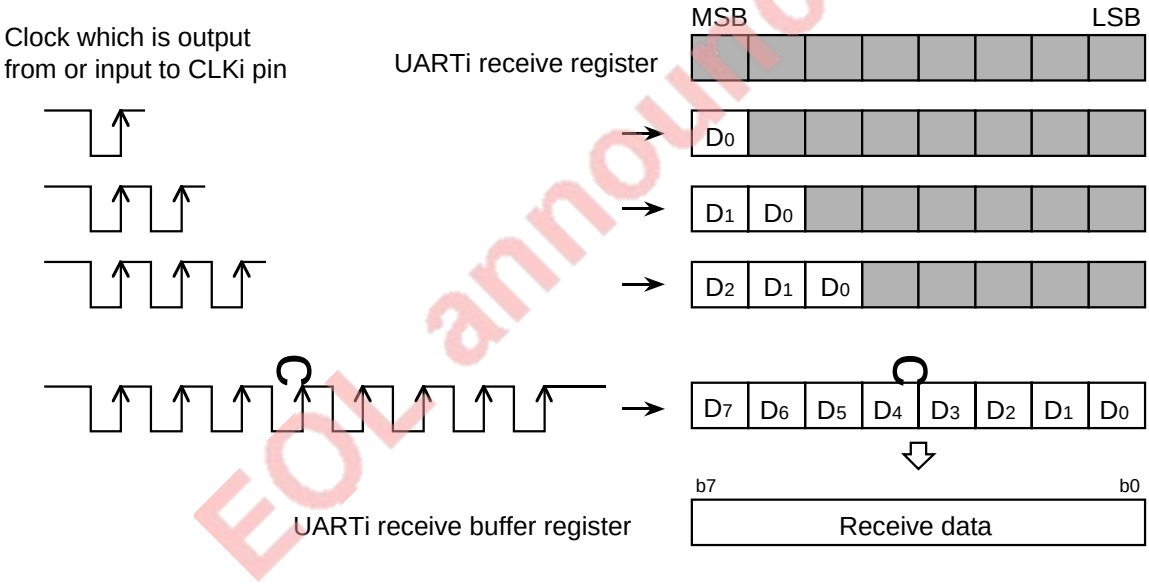
SERIAL I/O

8.3 Clock synchronous serial I/O mode



Note: The $\overline{\text{RTSi}}$ output function is not assigned for

Fig. 8.3.13 Connection example



❋ This is applied when the CLK polarity selection bit = "0."
When the CLK polarity selection bit = "1," data is shifted at the falling edge of the clock which is output from or input to the CLKi pin.

Fig. 8.3.14 Receive operation

EOL announced

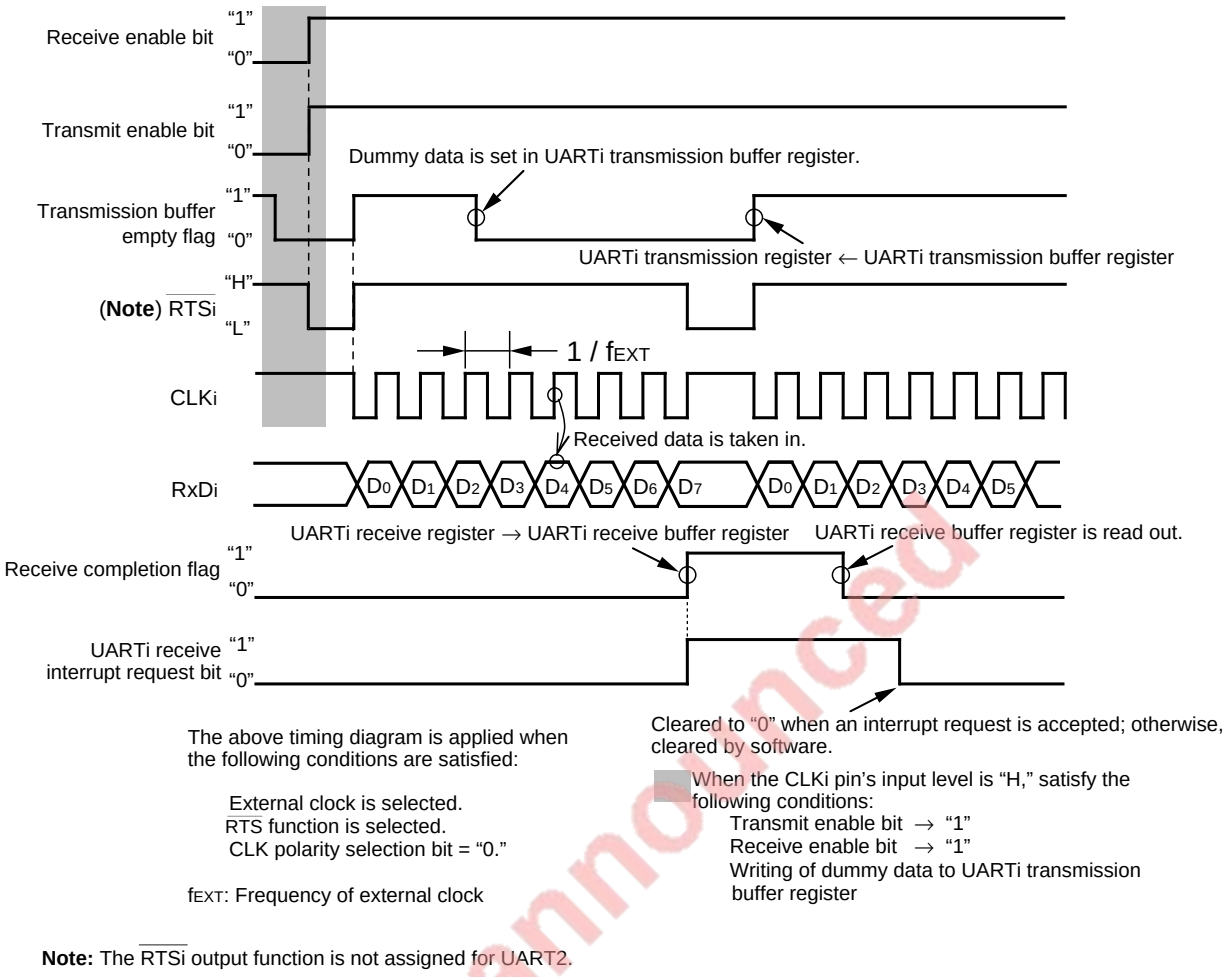


Fig. 8.3.15 Example of receive timing (when external clock is selected)

EOL announced

8.3 Clock synchronous serial I/O mode

8.3.7 Processing when an overrun error is detected

In the clock synchronous serial I/O mode, an overrun error can be detected.

An overrun error occurs when the next data is prepared in the UARTi receive register with the receive completion flag = “1” (in other words, data is present in the UARTi receive buffer register), and then the next data is transferred to the receive buffer register. In other words, when the next data is prepared before the contents of the UARTi receive buffer register is read out, an overrun error occurs. When an overrun error occurs, the next data is written into the UARTi receive buffer register. At this time, the UARTi receive interrupt request bit does not change.

An overrun error is detected when data is transferred from the UARTi receive register to the UARTi receive buffer register. At this time, the overrun error flag is set to “1.” The overrun error flag is cleared to “0” when the serial I/O mode selection bits are cleared to “000_2” or when the receive enable bit is cleared to “0.”

When an overrun error occurs during reception, initialize the overrun error flag and the UARTi receive buffer register, and then perform reception again. When it is necessary to perform transmission owing to an overrun error which occurs in the receiver side, set the UARTi transmission buffer register again, and then starts transmission again.

The method of initializing the UARTi receive buffer register and that of setting the UARTi transmission buffer register again are described below.

(1) Method of Initializing UARTi receive buffer register

① Clear the receive enable bit to “0.” (Reception is disabled.)

② Set the receive enable bit to “1” again. (Reception is enabled.)

(2) Method of setting UARTi transmission buffer register again

① Clear the serial I/O mode selection bits to “000_2.” (Serial I/O is ignored.)

② Set the serial I/O mode selection bits to “001_2” again.

③ Set the transmit enable bit to “1.” (Transmission is enabled.) And set the transmit data to the UARTi transmission buffer register.

EOL announced

8.3.8 Precautions for clock synchronous serial I/O

1. The transfer clock is generated by the operation of the transmit control circuit. Accordingly, even when performing only reception, the transmit operation (setting for transmission) must be performed. In this case, dummy data is output from the TxDi pin to the external.

2. When an internal clock is selected during reception, the transfer clock is generated if the following conditions are satisfied:
   •The transmit enable bit is set to "1." (Transmission is enabled.)
   •Dummy data is set to the UARTi transmission buffer register.
   When an external clock is selected during reception, the transfer clock is generated if the following conditions are satisfied:
   •The transmit enable bit is set to "1."
   •A clock is input to the CLKi pin after dummy data is set to the UARTi transmission buffer register.

3. When an external clock is selected, make sure that the following conditions are satisfied with the CLKi pin's input level = "H" if the CLK polarity selection bit = "0" or with the CLKi pin's input level = "L" if the CLK polarity selection bit = "1":

   [At transmitting]
   ① Set the transmit enable bit to "1."
   ② Write the transmit data to the UARTi transmission buffer register.
   ③ Input "L" level to the $\overline{\text{CTSi}}$ pin (when $\overline{\text{CTS}}$ function is selected).

   [At receiving]
   ① Set the receive enable bit to "1."
   ② Set the transmit enable bit to "1."
   ③ Write dummy data to the UARTi transmission buffer register.

4. When receiving data in succession, set dummy data to the low-order byte of the UARTi transmission buffer register each time when 1-byte data is received.

5. For performing the transmission and the reception simultaneously, UART2 does not distinguish the transmission interrupt from the reception interrupt. The UART2 transmission/reception interrupt request occurs when either interrupt request occurs. Accordingly, in the system which performs the transmission and reception simultaneously for UART2, not use the UART2 transmission/reception interrupt but use the method of poling the transmission buffer empty flag and the receive completion flag by software.

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

Table 8.4.1 lists the performance overview in the UART mode and Table 8.4.2 lists the functions of I/O pins in this mode.

Table 8.4.1 Performance overview in UART mode

Item		Functions
Transfer data format	Start bit	1 bit
	Character bit (Transfer data)	7 bits, 8 bits, or 9 bits
	Parity bit	0 bit or 1 bit (Odd or Even can be selected.)
	Stop bit	1 bit or 2 bits
Transfer rate	When internal clock is selected	BRGi's output divided by 16 (Maximum of 781.25 kbps **(Note)**)
	When external clock is selected	Maximum of 312.5 kbps
Error detection		4 types (Overrun, Framing, Parity, and Summing) Presence of error can be detected only by checking error sum flag.

Note: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0" and the system clock frequency = 25 MHz ($f(f_2)$ = 12.5 MHz). (For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Table 8.4.2 Functions of I/O pins in UART mode

Pin name	Functions	Method of selection
TxDi ($P8_3$, $P8_7$, $P7_5$)	Serial data output	(They cannot be used as programmable I/O ports.)
RxDi ($P8_2$, $P8_6$, $P7_4$)	Serial data input	Ports P7 and P8 direction register's corresponding bit = "0" (They can be used as input ports when only transmission is performed.)
CLKi ($P8_1$, $P8_5$, $P7_3$)	Programmable I/O port	Internal/External clock selection bit = "0"
	BRGi count source input	Internal/External clock selection bit = "1"
$\overline{CTS}i/\overline{RTS}i$ (**Note**) ($P8_0$, $P8_4$)	$\overline{CTS}$ input	$\overline{CTS}/\overline{RTS}$ enable bit = "0" $\overline{CTS}/\overline{RTS}$ function selection bit = "0"
	$\overline{RTS}$ output	$\overline{CTS}/\overline{RTS}$ enable bit = "0" $\overline{CTS}/\overline{RTS}$ function selection bit = "1"
	Programmable I/O port	$\overline{CTS}/\overline{RTS}$ enable bit = "1"
CTS_2 ($P7_2$)	$\overline{CTS}$ input	$\overline{CTS}$ enable bit = "0"
	Programmable I/O port	$\overline{CTS}$ enable bit = "1"

Port P7 direction register: Address 11_{16}
Port P8 direction register: Address 14_{16}
Internal/External clock selection bit: Bit 3 at addresses 30_{16}, 38_{16}, and 64_{16}
$\overline{CTS}/\overline{RTS}$ enable bit: Bit 4 at addresses 34_{16} and $3C_{16}$
$\overline{CTS}/\overline{RTS}$ function selection bit: Bit 2 at addresses 34_{16} and $3C_{16}$
$\overline{CTS}$ enable bit: Bit 2 at addresses 68_{16}

❋ The TxDi pin outputs "H" level while not transmitting after a UARTi's operating mode is selected. (The TxDi pin is in a floating state when N-channel open-drain output is selected.)

Note: The $\overline{RTS}i$ output function is not assigned for UART2.

EOL announced

8.4.1 Transfer rate (Baud rate: transfer clock frequency)

The transfer rate is determined by BRGi (addresses 31_{16}, 39_{16}, and 65_{16}).

When a value of "n" is set in BRGi (n = 00_{16} to FF_{16}), the count source is divided by (n + 1) in the BRGi, and then the BRGi's output is further divided by 16. (In this way, the transfer clock is generated.) Accordingly, assuming that the baud rate is B (bps), "n" is expressed by the following formula.

$$n = \frac{F}{16 \times B} - 1$$

F : BRGi's count source frequency

An internal clock or an external clock can be selected as the BRGi's count source by specifying the internal/external clock selection bit (bit 3 at addresses 30_{16}, 38_{16}, and 64_{16}). When an internal clock is selected, the clock selected by the BRG count source selection bits (bits 1 and 0 at addresses 34_{16}, $3C_{16}$, and 68_{16}) is the BRGi's count source. When an external clock is selected, the clock which is input to the CLKi pin is the BRGi's count source.

Tables 8.4.3 to 8.4.5 list examples of baud rate setting. Be sure to set the same baud rate for both transmitter and receiver sides.

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

Table 8.4.3 Example of baud rate setting (1)

Baud rate (bps)	BRGi's countsource	System clock: 14.7456 MHz		System clock: 19.6608 MHz	
		BRGi's set value: n	Actual time (bps)	BRGi's set value: n	Actual time (bps)
300	f_{16}	191 (BF_{16})	300.00	255 (FF_{16})	300.00
600	f_{16}	95 ($5F_{16}$)	600.00	127 ($7F_{16}$)	600.00
1200	f_{16}	47 ($2F_{16}$)	1200.00	63 ($3F_{16}$)	1200.00
2400	f_2	191 (BF_{16})	2400.00	255 (FF_{16})	2400.00
4800	f_2	95 ($5F_{16}$)	4800.00	127 ($7F_{16}$)	4800.00
9600	f_2	47 ($2F_{16}$)	9600.00	63 ($3F_{16}$)	9600.00
19200	f_2	23 (17_{16})	19200.00	31 ($1F_{16}$)	19200.00
38400	f_2	11 ($0B_{16}$)	38400.00	15 (F_{16})	38400.00
57600	f_2	7 (07_{16})	57600.00		
115200	f_2	3 (03_{16})	115200.00		

System clock, and clocks f_2, f_{16}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."
For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Table 8.4.4 Example of baud rate setting (2)

Baud rate (bps)	BRGi's countsource	System clock: 24.576 MHz		System clock: 25 MHz	
		BRGi's set value: n	Actual time (bps)	BRGi's set value: n	Actual time (bps)
300	f_{64}	79 ($4F_{16}$)	300.00	80 (50_{16})	301.41
600	f_{16}	159 ($9F_{16}$)	600.00	162 ($A2_{16}$)	599.12
1200	f_{16}	79 ($4F_{16}$)	1200.00	80 (50_{16})	1205.63
2400	f_{16}	39 (27_{16})	2400.00	40 (28_{16})	2381.86
4800	f_2	159 ($9F_{16}$)	4800.00	162 ($A2_{16}$)	4792.94
9600	f_2	79 ($4F_{16}$)	9600.00	80 (50_{16})	9645.06
14400	f_2	52 (34_{16})	14490.57	53 (35_{16})	14467.59
19200	f_2	39 (27_{16})	19200.00	40 (28_{16})	19054.88
31250	f_2			24 (18_{16})	31250.00

System clock, and clocks f_2, f_{16}, f_{64}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."
For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Table 8.4.5 Example of baud rate setting (3)

Baud rate (bps)	BRGi's countsource	System clock: 11.0592 MHz		System clock: 12 MHz	
		BRGi's set value: n	Actual time (bps)	BRGi's set value: n	Actual time (bps)
300	f_{16}	143 ($8F_{16}$)	300.00	155 ($9B_{16}$)	300.48
600	f_{16}	71 (47_{16})	600.00	77 ($4D_{16}$)	600.96
1200	f_{16}	35 (23_{16})	1200.00	38 (26_{16})	1201.92
2400	f_2	143 ($8F_{16}$)	2400.00	155 ($9B_{16}$)	2403.85
4800	f_2	71 (47_{16})	4800.00	77 ($4D_{16}$)	4807.69
9600	f_2	35 (23_{16})	9600.00	38 (26_{16})	9615.38
14400	f_2	24 (18_{16})	14400.00	26 ($1A_{16}$)	14423.08
19200	f_2	17 (11_{16})	19200.00		
28800	f_2	12 ($0C_{16}$)	28800.00	13 ($0D_{16}$)	28846.15
31250	f_2			11 ($0B_{16}$)	31250.00

System clock, and clocks f_2, f_{16}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Note: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."
For details, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

EOL announced

8.4.2 Transfer data format

The transfer data format can be selected from three formats shown in Figure 8.4.1. By setting bits 6 to 4 at addresses 30_{16}, 38_{16} and 64_{16}, the transfer data format can be selected. (Refer to **Figures 8.2.2 and 8.2.3.**) Be sure to set the same transfer data format for both transmitter and receiver sides.
Figure 8.4.2 shows an example of transfer data format. Table 8.4.6 lists each bit in transmit data.

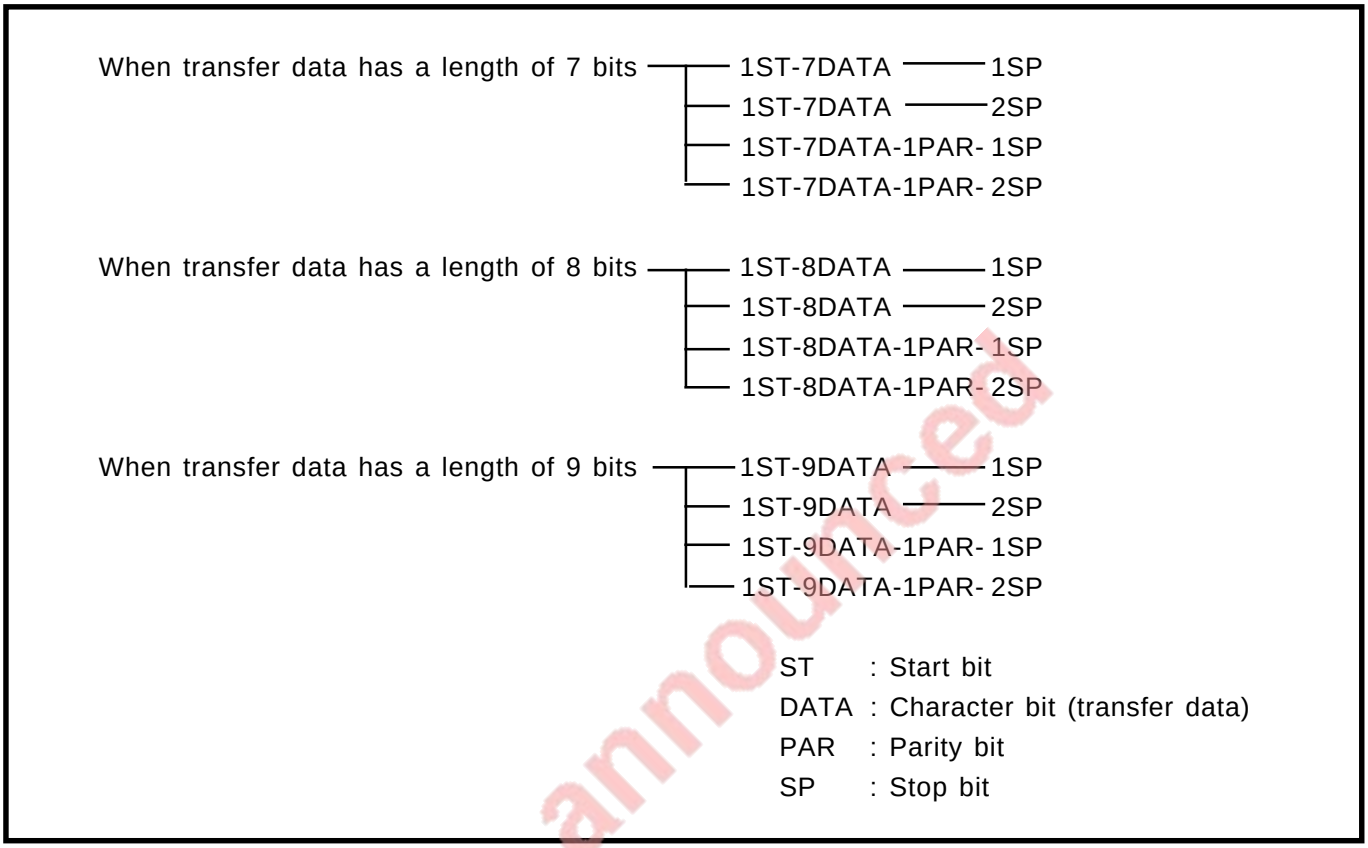


Fig. 8.4.1 Transfer data format

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

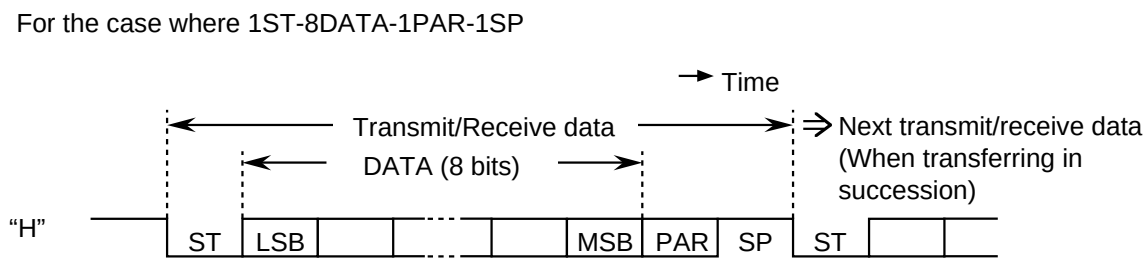


Fig. 8.4.2 Example of transfer data format

Table 8.4.6 Each bit in transmit data

Name	Functions
ST Start bit	"L" signal equivalent to 1 character bit which is added immediately before the character bits. It indicates start of data transmission.
DATA Character bit	Transmit data which is set in the UARTi transmission buffer register.
PAR Parity bit	A signal which is added immediately after the character bits in order to improve data reliability. The level of this signal changes depending on odd/even parity selection in such a way that the sum of "1"s in bits (this bit and character bits) is always an odd or even number.
SP Stop bit	"H" level signal equivalent to 1 or 2 character bits which is added immediately after the character bits (or parity bit when parity is enabled). It indicates end of data transmission.

EOL announced

8.4.3 Method of transmission

Figure 8.4.3 shows an initial setting example for related registers when transmitting.
The difference derived by selection of transfer data length (7 bits, 8 bits, or 9 bits) is only that data is transmitted in different lengths. When a 7/8-bit data length is selected, set the transmit data in the low-order byte of the UARTi transmission buffer register; when a 9-bit data length is selected, set the transmit data in the low-order byte and bit 0 of the high-order byte.
Transmission is started when the following conditions (① to ③) are satisfied:

① Transmit enable state (transmit enable bit = “1”)
② Transmit data is present in the UARTi transmission buffer register (transmission buffer empty flag = “0”)
③ The $\overline{\text{CTSi}}$ pin’s input is at “L” level (when the $\overline{\text{CTS}}$ function is selected)
Note: When the $\overline{\text{CTS}}$ function is not selected or in UART2, this condition is ignored.

By connecting the $\overline{\text{RTSi}}$ pin (receiver side) and $\overline{\text{CTSi}}$ pin (transmitter side), the timing of transmission and that of reception can be matched (UART0, UART1). For details, refer to section **“8.4.6 Receive operation.”**
When using interrupts, settings for enabling interrupts are required. For details, refer to chapter **“4. Interrupts.”**
Figure 8.4.4 shows how to write data after transmission is started and Figure 8.4.5 shows how to detect the transmit completion.

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

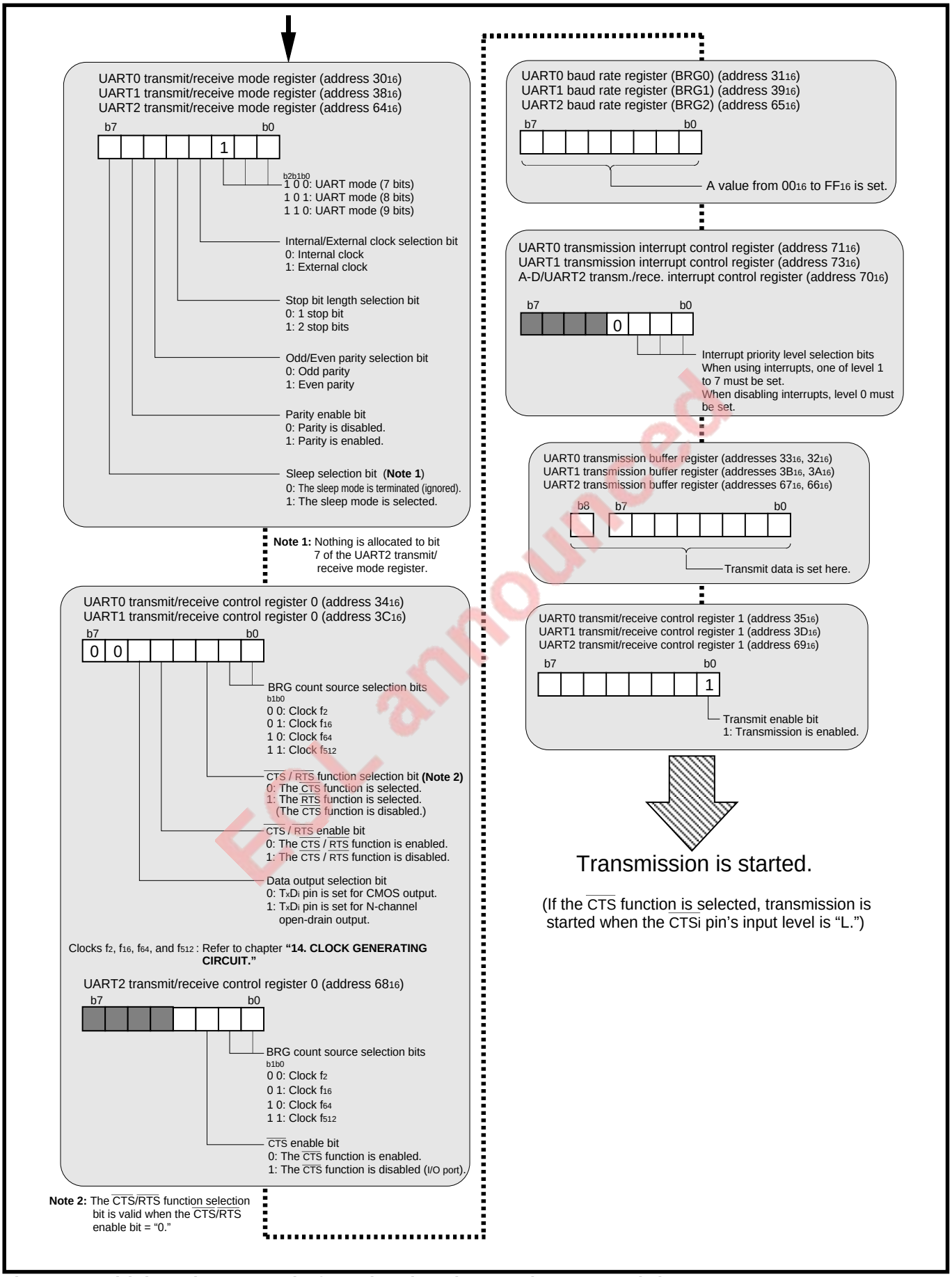


Fig. 8.4.3 Initial setting example for related registers when transmitting

E.L announced

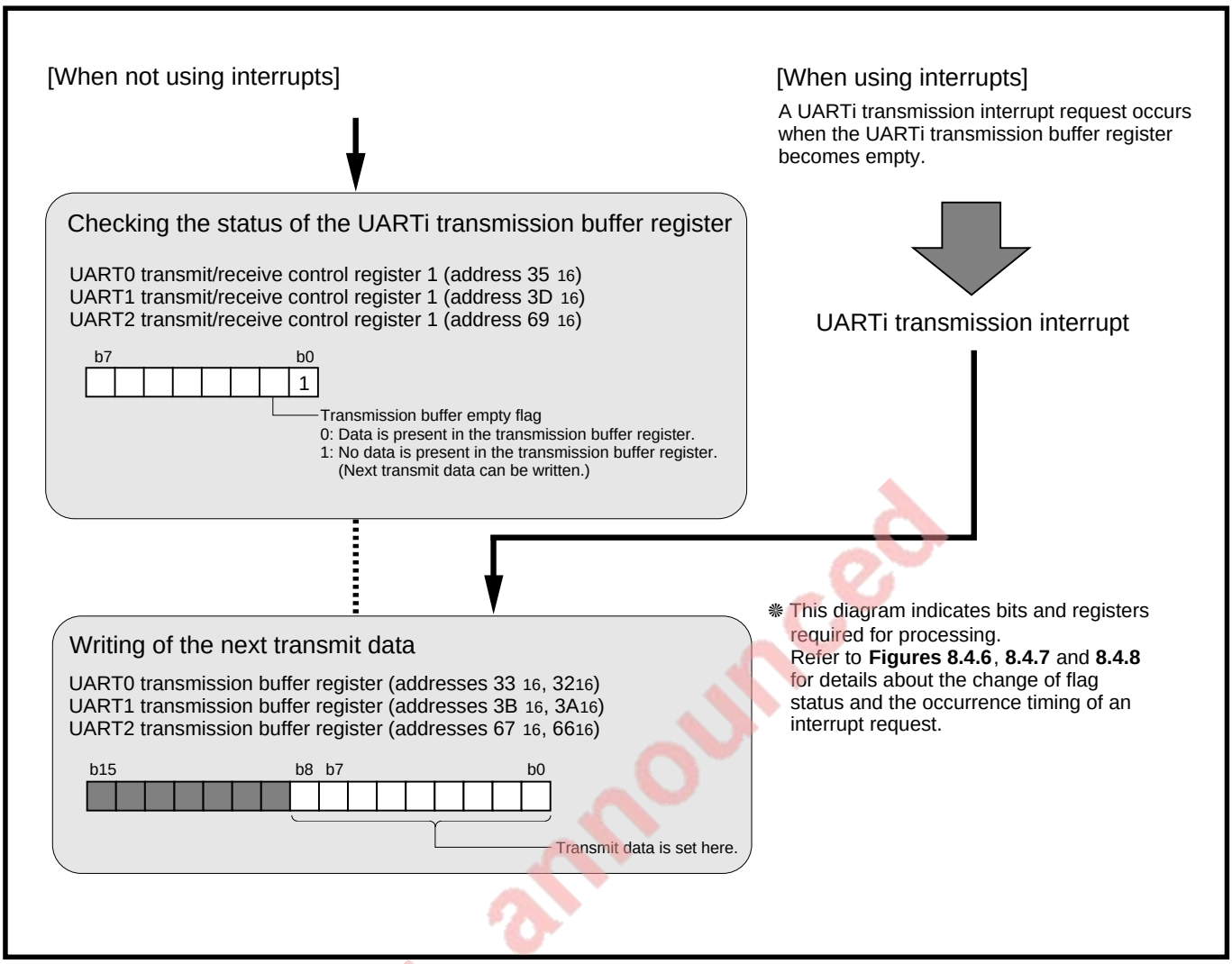


Fig. 8.4.4 How to write data after transmission is started

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

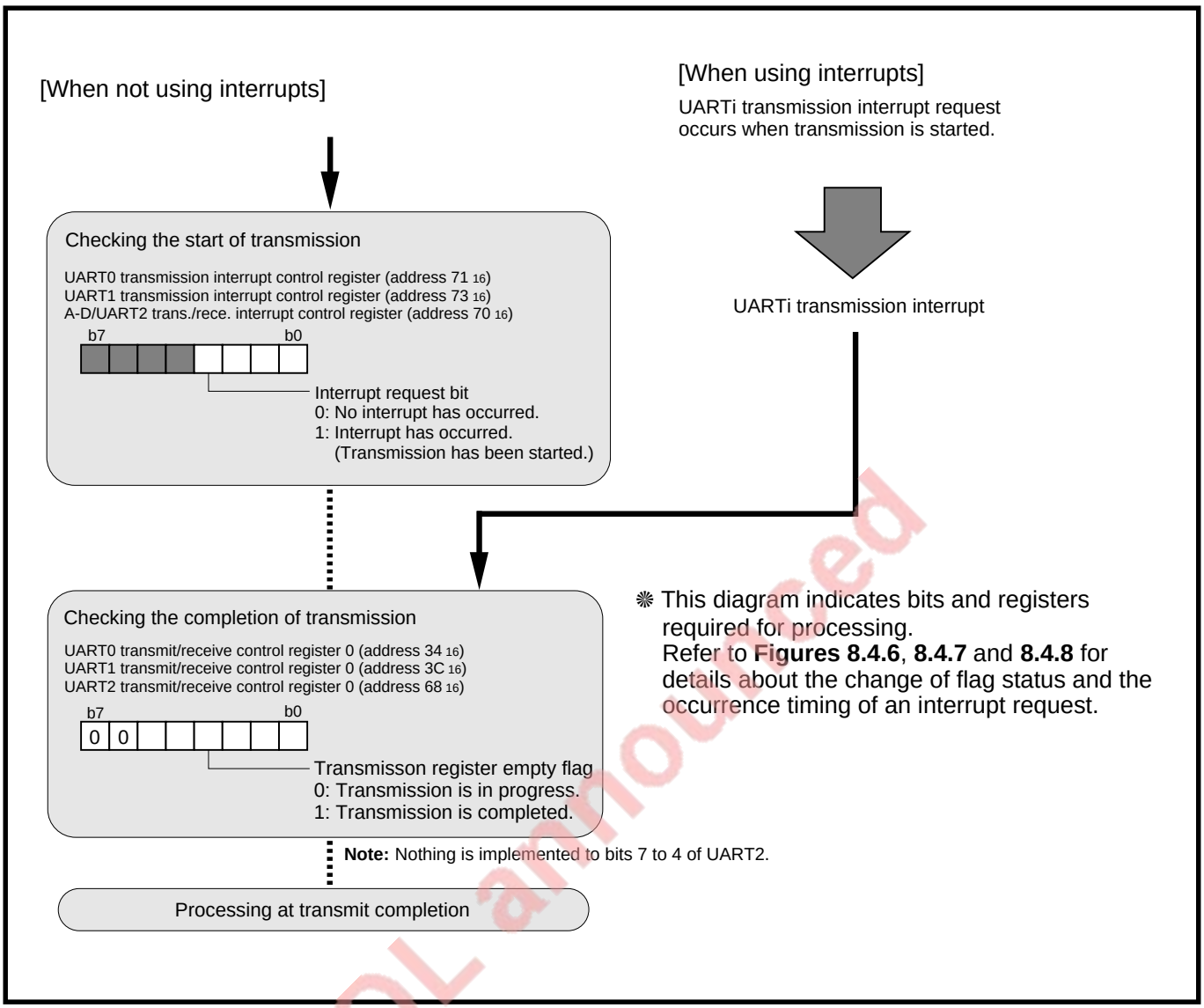


Fig. 8.4.5 How to detect transmit completion

EOL announced

8.4.4 Transmit operation

When the transmit conditions described in section **"8.4.3 Method of transmission"** are satisfied, the transfer clock is generated and the following operations are automatically performed after one cycle of the transfer clock has passed.

- The UARTi transmission buffer register's contents is transferred to the UARTi transmission register.
- The transmission buffer empty flag is set to "1."
- The transmission register empty flag is cleared to "0."
- A UARTi transmission interrupt request occurs and the interrupt request bit is set to "1."

The transmit operation is described below.

① Data in the UARTi transmission register is transmitted from the TxDi pin.
② This data is transmitted bit by bit sequentially in order of ST→DATA (LSB)→ ••• →DATA (MSB)→PAR →SP according to the transfer data format.
③ In the middle of the stop bit (the second stop bit when two stop bits are selected), the transmission register empty flag is set to "1." This indicates completion of transmission. Also, whether the transmit conditions for the next data are satisfied or not is checked.

When the transmit conditions for the next data are satisfied at completion of transmission in operation ③, a start bit is generated following the stop bit and the next data is transmitted. When performing transmission in succession, set the next transmit data in the UARTi transmission buffer register during transmission (when transmission register empty flag = "0").
When the transmit conditions for the next data are not satisfied, the TXDi pin outputs "H" level and the transfer clock is stopped.
Figure 8.4.6 shows an example of transmit timing when the transfer data length has a 8 bits. Figure 8.4.7 shows an example of transmit timing when the transfer data length has a 9 bits.

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

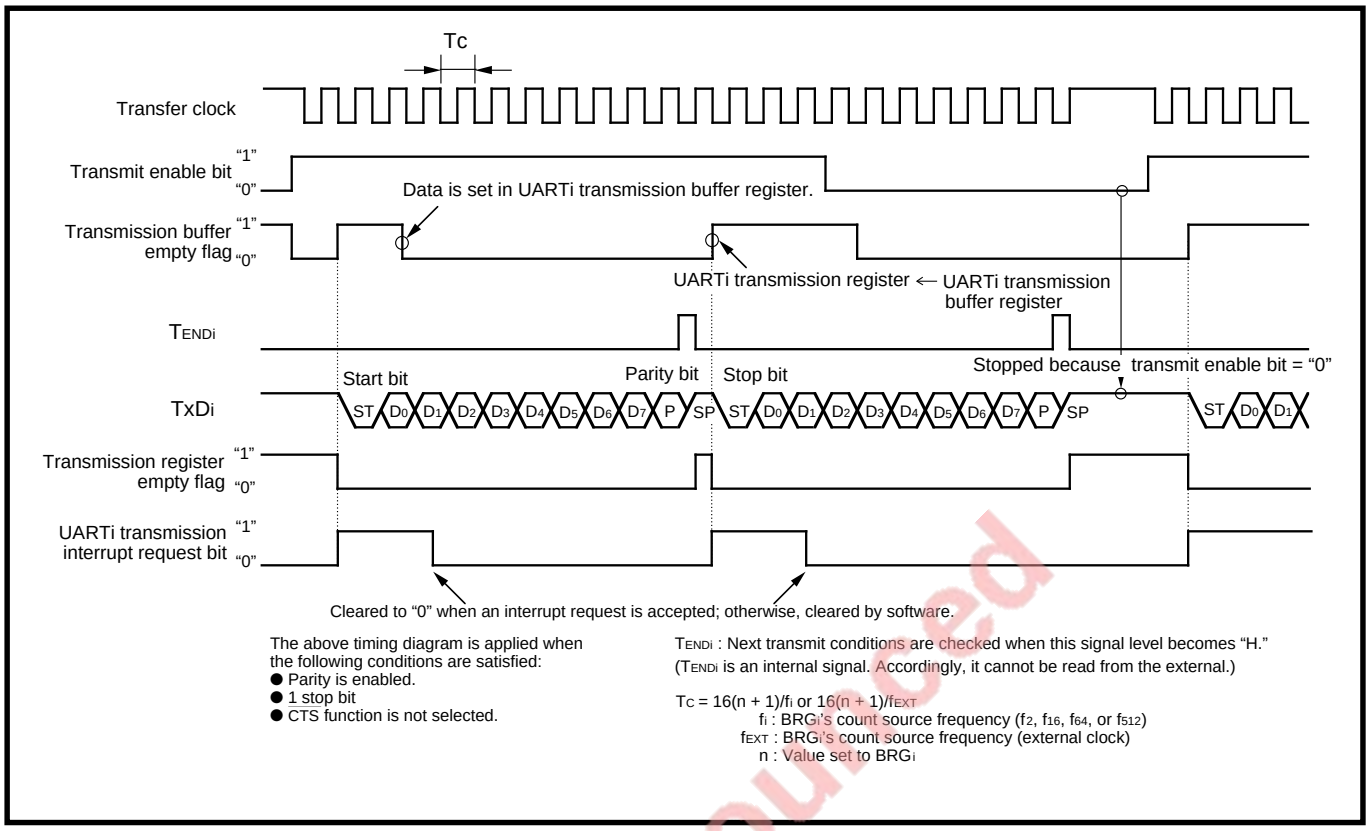


Fig. 8.4.6 Example of transmit timing when data is transferred in 8 bits (When parity is enabled, one stop bit, and $\overline{\text{CTS}}$ function is not selected)

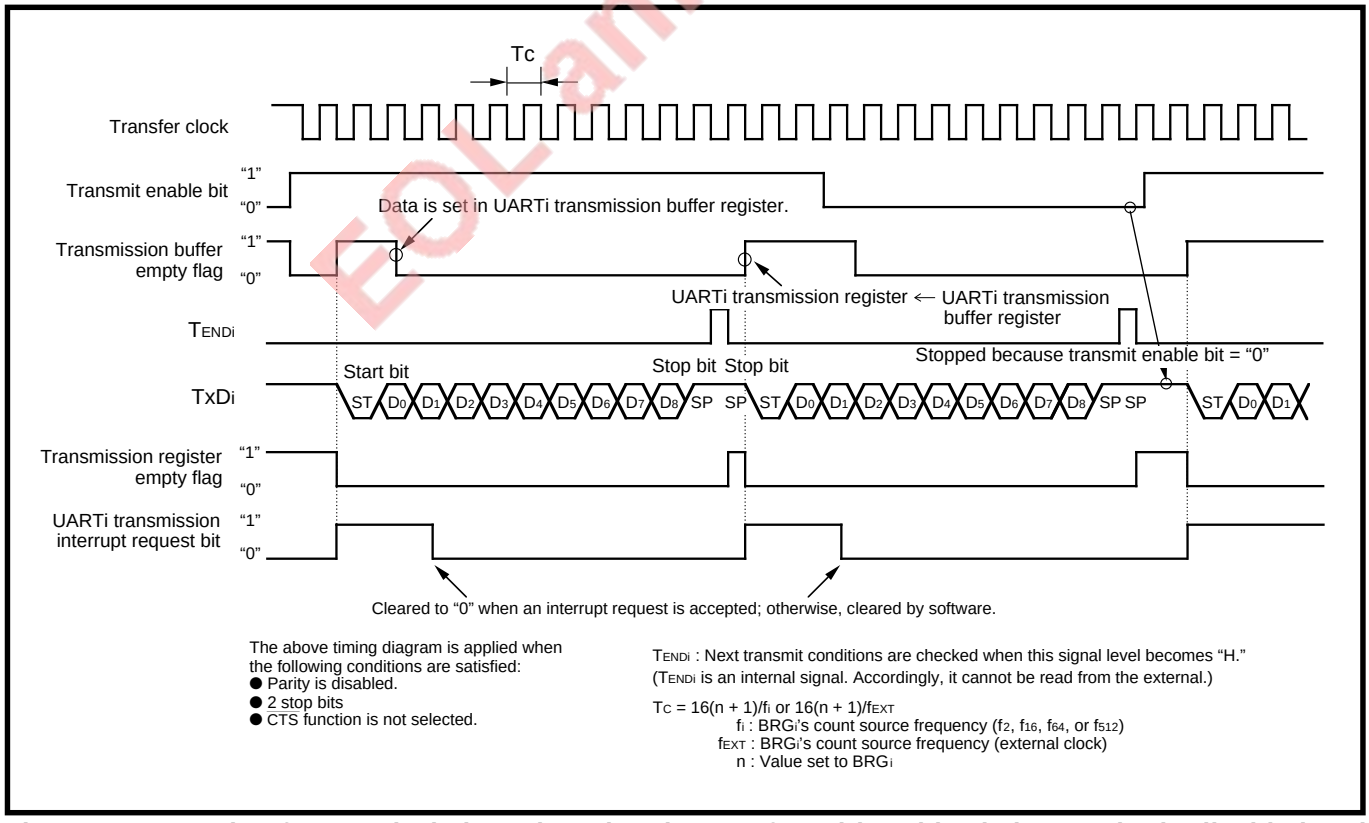
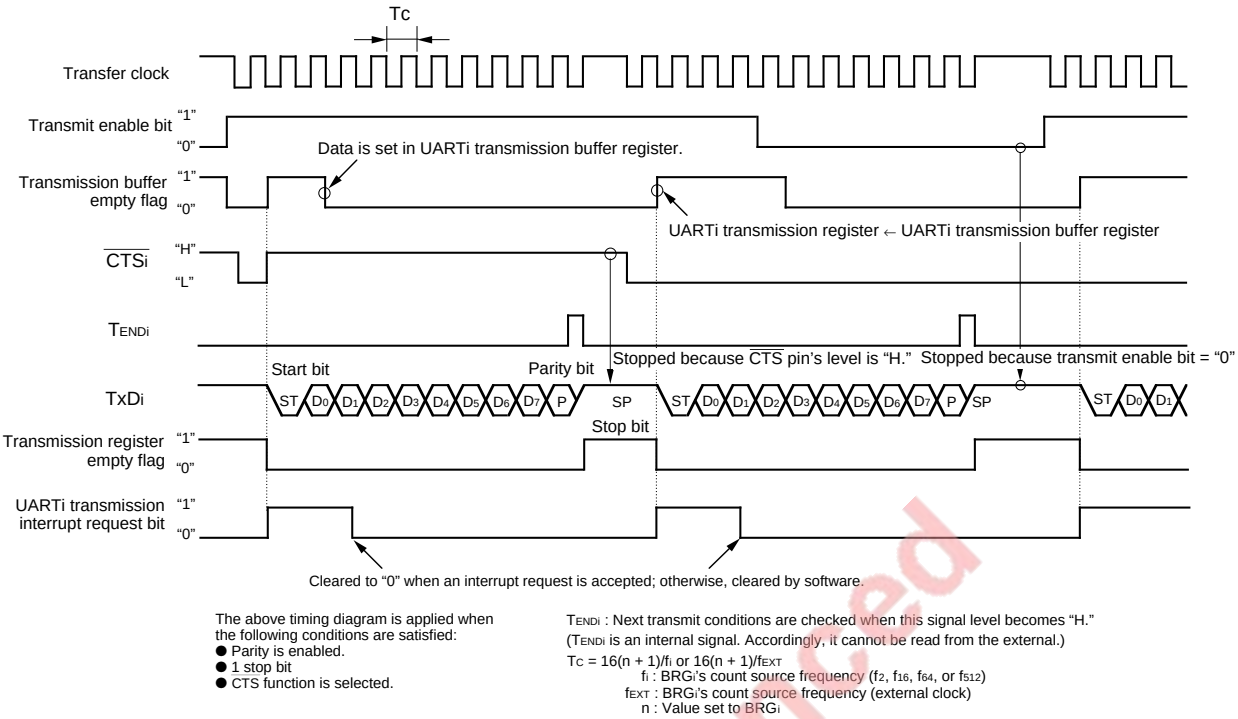


Fig. 8.4.7 Example of transmit timing when data is transferred in 9 bits (When parity is disabled and two stop bits)

EOL announced



The above timing diagram is applied when the following conditions are satisfied:
- Parity is enabled.
- 1 stop bit
- CTS function is selected.

T_{ENDi} : Next transmit conditions are checked when this signal level becomes "H."
(T_{ENDi} is an internal signal. Accordingly, it cannot be read from the external.)

$T_C = 16(n + 1)/f_i$ or $16(n + 1)/f_{EXT}$

f_i : BRGi's count source frequency (f_2, f_{16}, f_{64}, or f_{512})

f_{EXT} : BRGi's count source frequency (external clock)

n : Value set to BRGi

Fig. 8.4.8 Example of transmit timing when data is transferred in 8 bits (When parity is enabled, one stop bit, and CTS function is selected)

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

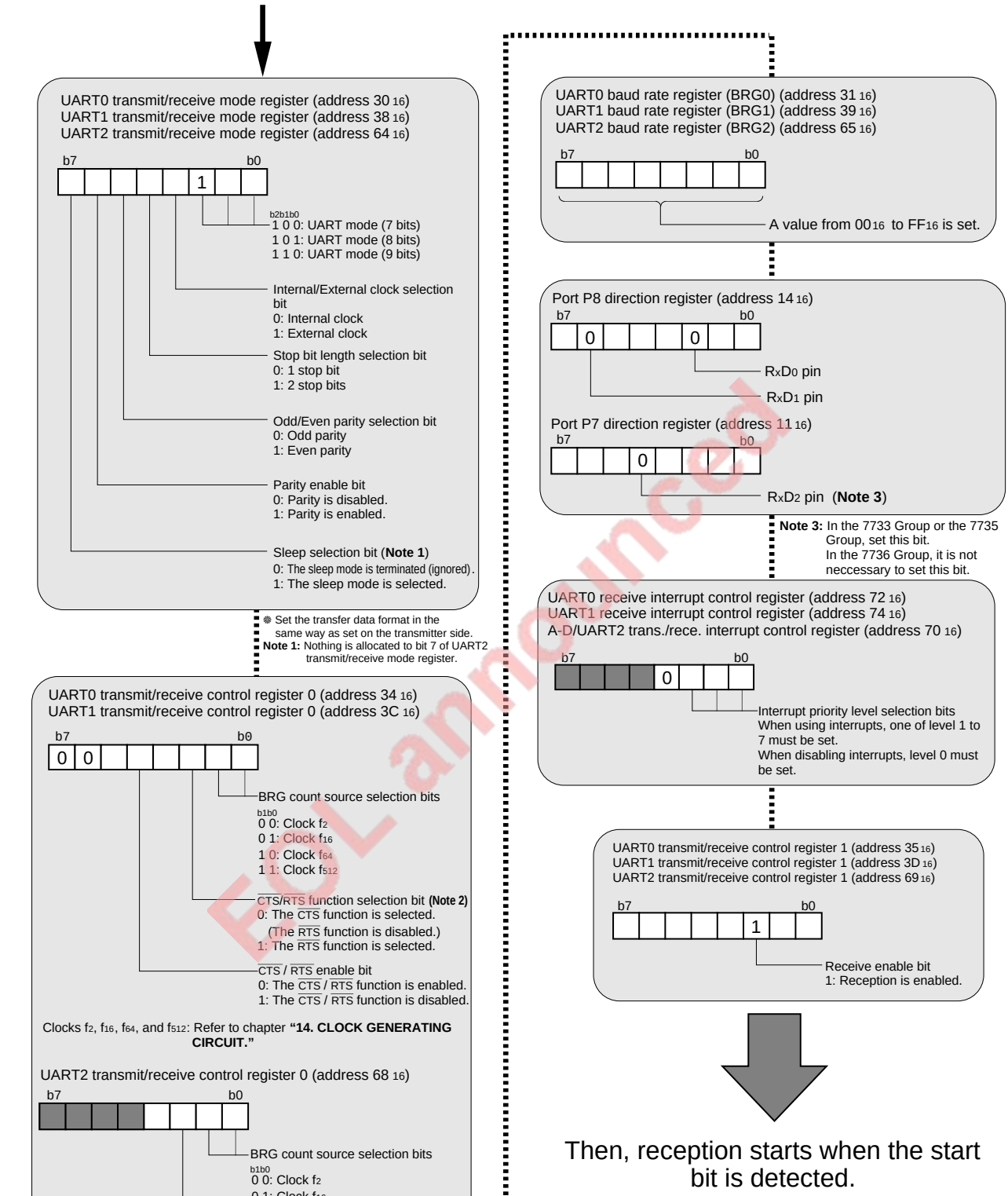
8.4.5 Method of reception

Figure 8.4.9 shows an initial setting example for related registers when receiving. Reception is started when the following conditions (① and ②) are satisfied.

① Receive enable state (receive enable bit = “1”).
② The start bit is detected.

By connecting the $\overline{\text{RTSi}}$ pin (receiver side) and $\overline{\text{CTSi}}$ pin (transmitter side), the timing of transmission and that of reception can be matched (UART0, UART1). For details, refer to section **“8.4.6 Receive operation.”** When using interrupts, settings for enabling interrupts are required. For details, refer to chapter **“4. Interrupts.”** Figure 8.4.10 shows the processing after reception is completed.

EOL announced



FCL announced

Fig. 8.4.9 Initial setting example for related registers when receiving

8.4 Clock asynchronous serial I/O (UART) mode

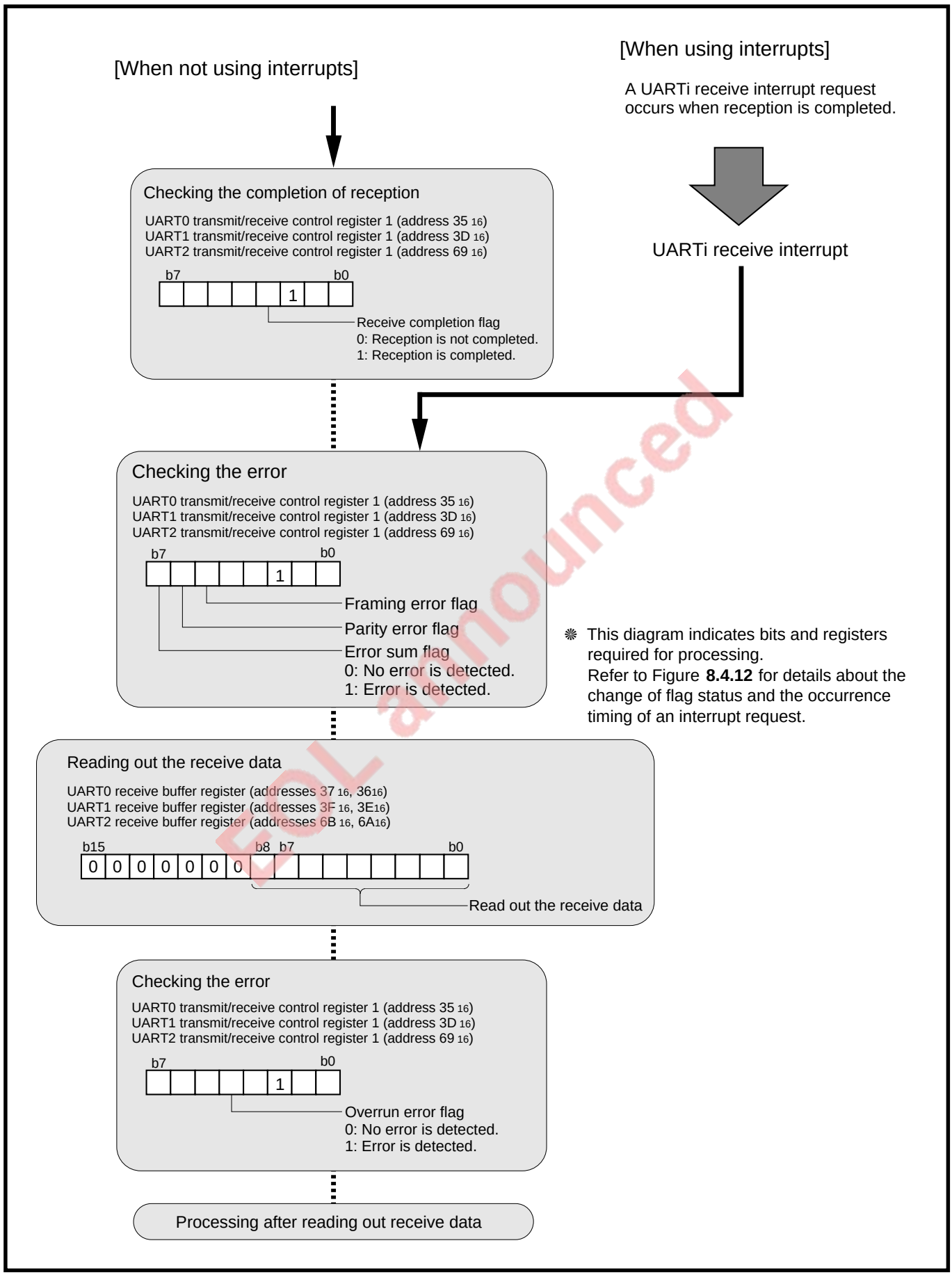


Fig. 8.4.10 Processing after reception is completed

8.4.6 Receive operation

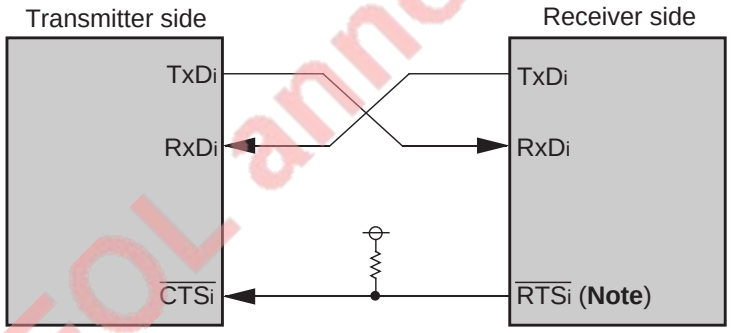
When the receive enable bit is set to “1,” the UARTi enters the receive enable state. And then, the transfer clock is generated when ST is detected, and reception is started.

When the $\overline{\text{RTS}}$ function is selected (UART0, UART1), the $\overline{\text{RTSi}}$ pin’s output level becomes “L” if the UARTi enters the receive enable state and the microcomputer informs the transmitter side that reception is enabled. When reception is started, the $\overline{\text{RTSi}}$ pin’s output level becomes “H.” Accordingly, by connecting the $\overline{\text{RTSi}}$ pin (receiver side) and the $\overline{\text{CTSi}}$ pin (transmitter side), the timing of transmission and that of reception can be matched. Figure 8.4.11 shows an connection example.

The receive operation is described below.

① The signal which is input from the RxDi pin is taken in the most significant bit of the UARTi receive register synchronously with the transfer clock’s rising edge.
② The contents of UARTi receive register is shifted by 1 bit to the right.
③ Operations ① and ② are repeated at each transfer clock’s rising edge.
④ When a set of data is prepared, in other words, when shifted several times depending on the specified data format, the UARTi receive register’s contents is transferred to the UARTi receive buffer register.
⑤ Simultaneously with ④, the receive completion flag is set to “1.” Furthermore, a UARTi receive interrupt request occurs and the interrupt request bit is set to “1.”

The receive completion flag is cleared to “0” when the low-order of the UARTi receive buffer register is read out. The $\overline{\text{RTSi}}$ pin’s output level becomes “L” simultaneously with ⑤ (when $\overline{\text{RTS}}$ function is selected). Figure 8.4.12 shows an example of receive timing when transfer data has a length of 8 bits.

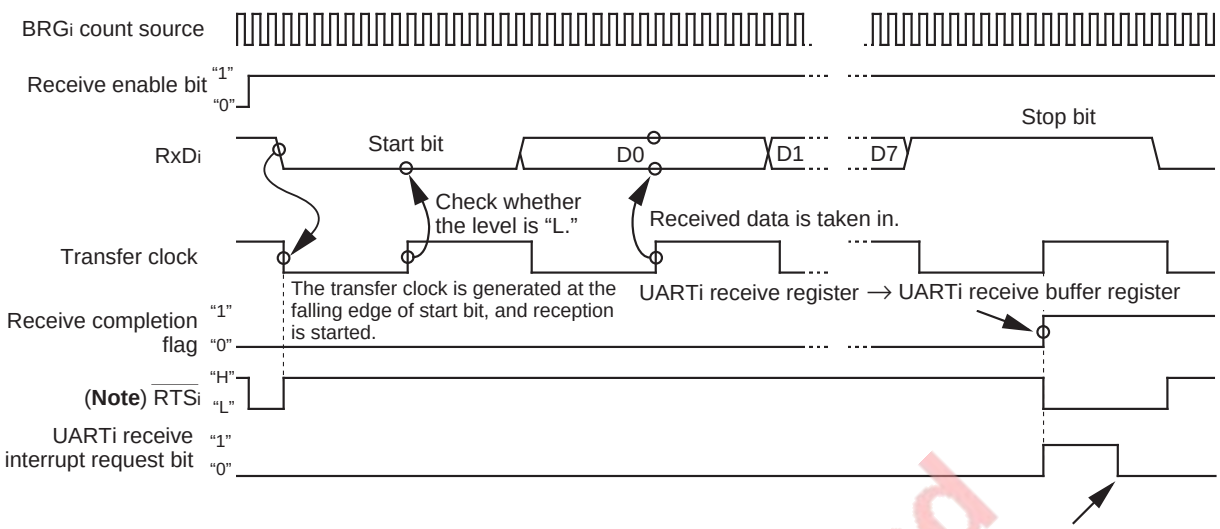


Note: The $\overline{\text{RTSi}}$ output function is not assigned for

Fig. 8.4.11 Connection example

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode



The above timing diagram is applied when the following conditions are satisfied:

- Parity is disabled.
- 1 stop bit
- RTS function is selected.

Note: The RTSi output function is not assigned for

Fig. 8.4.12 Example of receive timing when data is transferred in 8 bits (When parity is disabled and one stop bit)

EOL announced

8.4.7 Processing when error is detected

Errors listed below can be detected in the UART mode:

- **Overrun error**
  An overrun error occurs when the next data is prepared in the UARTi receive register with the receive completion flag = "1" (in other words, data is present in the UARTi receive buffer register), and then the next data is transferred to the UARTi receive buffer register. In other words, when the next data is prepared before the contents of the UARTi receive buffer register is read out. When an overrun error occurs, the next receive data is written into the UARTi receive buffer register. At this time, the UARTi receive interrupt request bit is not set to "1."

- **Framing error**
  A framing error occurs when the number of detected stop bits does not match the number which is set. (The UARTi interrupt request bit is set to "1.")

- **Parity error**
  A parity error occurs when the sum of "1"s in the parity bit and character bits does not match the number which is set. (The UARTi interrupt request bit is set to "1.")

Each error is detected when data is transferred from the UARTi receive register to the UARTi receive buffer register, and the corresponding error flag is set to "1." Furthermore, when any of the above errors occurs, the error sum flag is set to "1." Accordingly, the error sum flag informs whether any error has occurred or not.
Error flags are cleared to "0" when the serial I/O mode selection bits are cleared to "000_2" or when the receive enable bit is cleared to "0." (When all of the overrun, framing, and parity error flags are cleared to "0," the error sum flag is cleared to "0.") Note also that the framing and parity error flags are cleared to "0" when the low-order byte of the UARTi receive buffer register is read out.

When an error occurs during reception, initialize the error flags and the UARTi receive buffer register, and then perform reception again. When it is necessary to perform transmission again owing to an error which occurs in the receiver side, set the UARTi transmission buffer register again, and then starts transmission again.
The method of initializing the UARTi receive buffer register and that of setting the UARTi transmission buffer register again are described below.

(1) Method of initializing UARTi receive buffer register

① Clear the receive enable bit to "0." (Reception is disabled.)
② Set the receive enable bit to "1" again. (Reception is enabled.)

(2) Method of setting UARTi transmission buffer register again

① Clear the serial I/O mode selection bits to "000_2." (Serial I/O is ignored.)
② Set the serial I/O mode selection bits again.
③ Set the transmit enable bit to "1." (Transmission is enabled.) And set the transmit data to the UARTi transmission buffer register.

8.4.8 Precautions for UART

For performing the transmission and the reception simultaneously, UART2 does not distinguish the transmission interrupt from the reception interrupt. The UART2 transmission/reception interrupt request occurs when either interrupt request occurs. Accordingly, in the system which performs the transmission and reception simultaneously for UART2, not use the UART2 transmission/reception interrupt but use the method of poling the transmission buffer empty flag and the receive completion flag by software.

EOL announced

8.4 Clock asynchronous serial I/O (UART) mode

8.4.9 Sleep mode (UART0 and UART1)

This mode is used when data is transferred between the master microcomputer and one slave microcomputer, which is selected from multiple slave microcomputers connected to the master microcomputer using UARTi. The sleep mode is selected when the sleep selection bit (bit 7 at addresses 30_{16} and 38_{16}) is set to "1" at receiving.

In the sleep mode, the receive operation is performed when the MSB (D_8 when the transfer data has a length of 9 bits; D_7 when the transfer data has a length of 8 bits; D_6 when the transfer data has a length of 7 bits) of the receive data = "1." The receive operation is not performed when the MSB = "0." (The UARTi receive register's contents is not transferred to the UARTi receive buffer register. The receive completion flag and error flags do not change and a UARTi receive interrupt request does not occur, also.)

A usage example of the sleep mode when the transfer data has a length of 8 bits is described below.

① Set the same transfer data format for the master and slave microcomputers. Select the sleep mode for the slave microcomputer.
② Transmit the data, which has "1" in bit 7 and the address of the slave microcomputer to be communicated in bits 6 to 0, from the master microcomputer to all slave microcomputers.
③ All slave microcomputers receive data in operation ②. (At this time, a UARTi receive interrupt request occurs.)
④ For all slave microcomputers, check in the interrupt routine whether bits 6 to 0 in the receive data match their own addresses.
⑤ For the slave microcomputer whose address matches bits 6 to 0 in the receive data, terminate the sleep mode. (Do not terminate the sleep mode for the other slave microcomputers.)
By performing operations ② to ⑤, "the slave microcomputer which performs transmission" can be specified.
⑥ Transmit the data, which has "0" in bit 7, from the master microcomputer. (Only the microcomputer selected by operations ② to ⑤ receives this data. The other microcomputers do not receive this data.)
⑦ By repeating operation ⑥, data is transferred between two specific microcomputers in succession. Also, by performing operations ② to ⑤, another slave microcomputer can be specified.

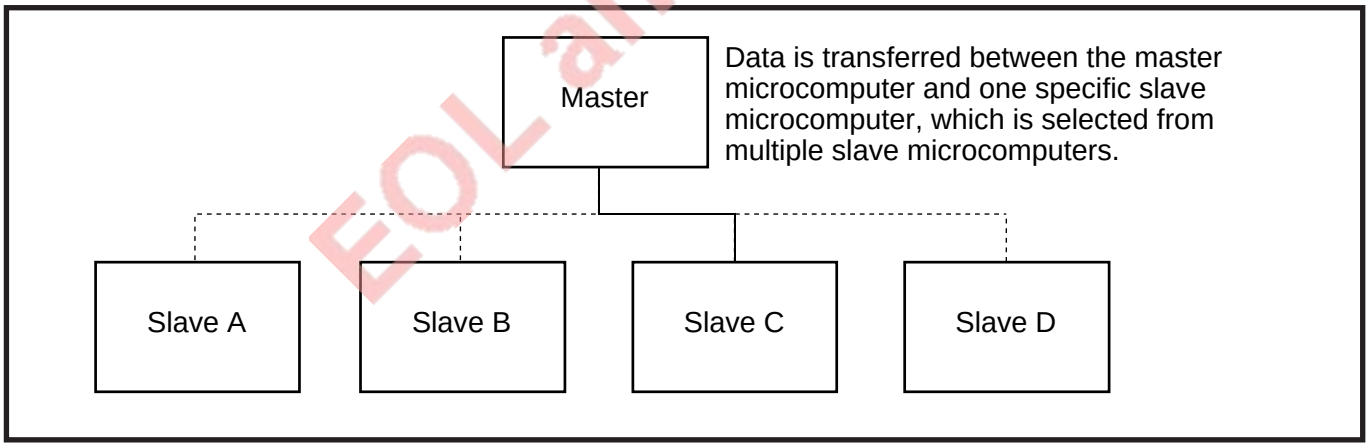


Fig. 8.4.13 Sleep mode

EOL announced

CHAPTER 9

A-D CONVERTER

9.1 Overview
9.2 Block description
9.3 A-D conversion method
9.4 Absolute accuracy and Differential non-linearity error
9.5 One-shot mode
9.6 Repeat mode
9.7 Single sweep mode
9.8 Repeat sweep mode
9.9 Precautions for A-D converter

EOL announced

A-D CONVERTER

9.1 Overview

The A-D converter is described below.
For this A-D converter, 8-bit resolution or 10-bit resolution can be selected. It's conversion method is the successive approximation method and has 8 analog input pins.

9.1 Overview

The performance overview is listed in Table 9.1.1.

Table 9.1.1 Performance overview

Item	Performance
A-D conversion method	Successive approximation method
Resolution	8/10 bits can be selected by software
Absolute accuracy	8-bit resolution: ±2 LSB
	10-bit resolution: ±3 LSB
Analog input pin	8 pins (AN_0 to AN_7)
Conversion rate per analog input pin	8-bit resolution: 49 ϕ_{AD}* cycles
	10-bit resolution: 59 ϕ_{AD}* cycles

ϕ_{AD}*: A-D converter's operating clock

The A-D convertor has the following four operation modes.

■ One-shot mode
A-D conversion is once performed for the input voltage of one analog input pin.

■ Repeat mode
A-D conversion is repeatedly performed for the input voltage of one analog input pin.

■ Single sweep mode
A-D conversion is performed for the input voltage of multiple analog input pins, one at a time.

■ Repeat sweep mode
A-D conversion is repeatedly performed for the input voltage of multiple analog input pins.

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9.2 Block description

Figure 9.2.1 shows the block diagram of the A-D converter. Registers related to the A-D converter are described below.

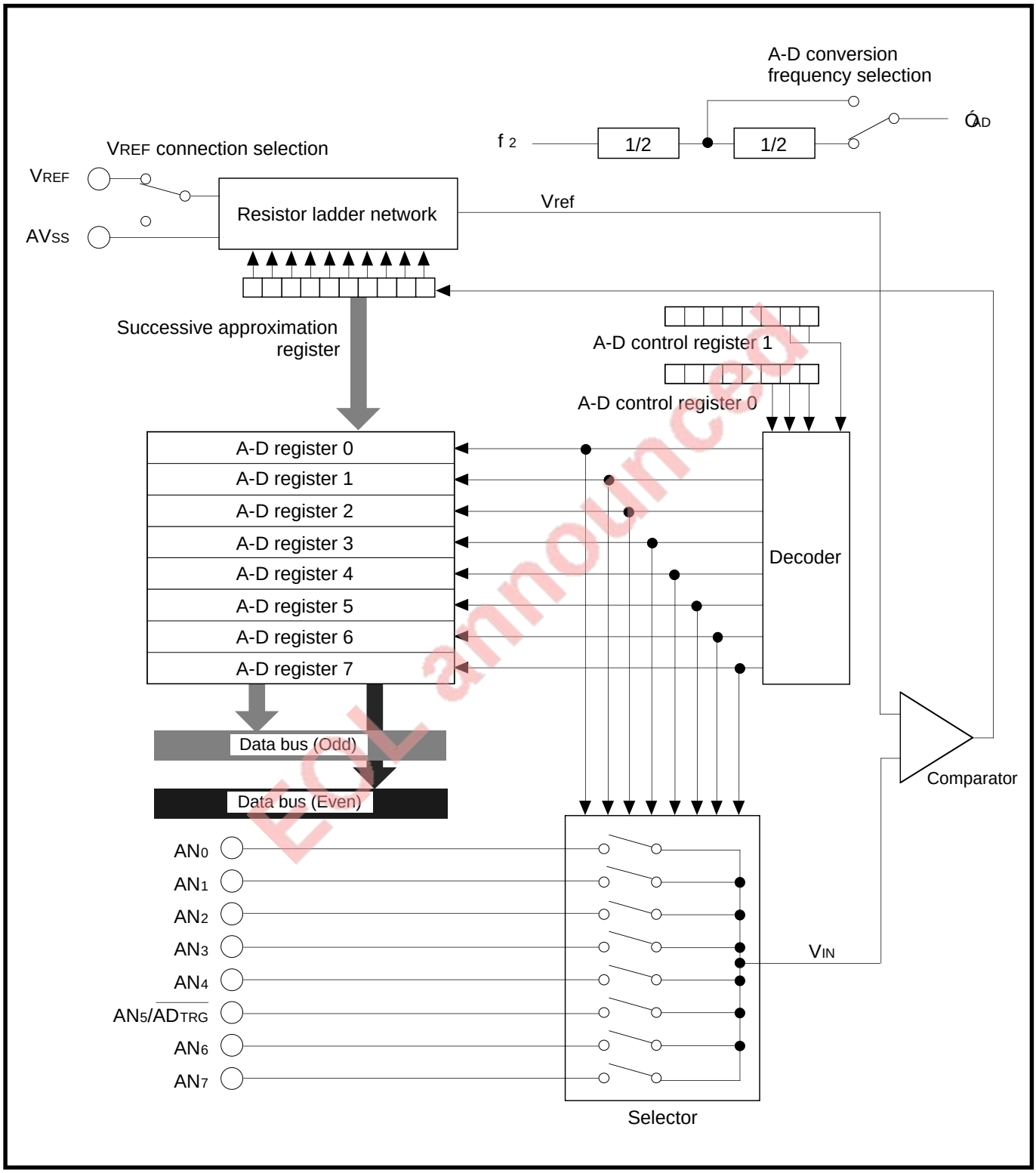


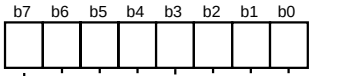
Fig. 9.2.1 Block diagram of A-D converter

A-D CONVERTER

9.2 Block description

9.2.1 A-D control register 0

Figure 9.2.2 shows the structure of A-D control register 0. A-D operation mode selection bits select an operation mode of A-D converter. The other bits are described below.



@A-D control register 0 (address 1E 16)

Bit	Bit name	Functions	At reset	RW
0	Analog input selection bits (Valid in the one-shot and repeat modes) **(Note 1)**	b2 b1 b0 0 0 0: AN0 is stopped. 0 0 1: AN1 is stopped. 0 1 0: AN2 is stopped. 0 1 1: AN3 is stopped. 1 0 0: AN4 is stopped. 1 0 1: AN5 is stopped. **(Note 2)** 1 1 0: AN6 is stopped. 1 1 1: AN7 is stopped.	Undefined	RW
1 @			Undefined	RW
2 @			Undefined	RW
3	A-D operation mode selection bits	b4b3 00: One-shot mode 01: Repeat mode 10: Single sweep mode 11: Repeat sweep mode	0	RW
4 @			0	RW
5	Trigger selection bit	0: Internal trigger 1: External trigger	0	RW
6	A-D conversion start flag	0: A-D conversion is stopped. 1: A-D conversion is started.	0	RW
7	A-D conversion frequency (AD) selection flag	0: f2/4* 1: f2/2	0	RW

f2*: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Notes 1: These bits are ignored in the single sweep and repeat sweep modes. (They may be "0" or "1.")
2: When an external trigger is selected, pin AN 5 cannot be used as an analog input pin.
3: Writing to each bit (except bit 6) of the A-D control register 0 must be performed while the A-D converter stops operating.

Fig. 9.2.2 Structure of A-D control register 0

EOL announced

(1) Analog input selection bits (bits 2 to 0)

These bits are used to select an analog input pin in the one-shot and repeat modes. (Refer to section **"9.2.5 Port P7 direction register."**)

When switching the operating mode to the one-shot or repeat mode after A-D conversion is once performed in the single sweep or repeat sweep mode, set these bits again.

(2) Trigger selection bit (bit 5)

This bit selects a trigger occurrence source. (Refer to **"(3) A-D conversion start flag."**)

(3) A-D conversion start flag (bit 6)

When internal trigger is selected

When this bit is set to "1," a trigger occurs, and then the A-D converter starts operating. When this bit is cleared to "0," the A-D converter stops operating.

In the one-shot or single sweep mode, this bit is cleared to "0" after A-D conversion is completed. In the repeat or repeat sweep mode, the A-D converter continues operating until this bit is cleared to "0" by software.

When external trigger is selected

If the $\overline{\text{ADTRG}}$ pin level goes from "H" to "L" when this bit = "1," a trigger occurs, and then the A-D converter starts operating. The A-D converter stops operating when this bit is cleared to "0." In the one-shot or single sweep mode, this bit remains set to "1" even after A-D conversion is completed. In the repeat or repeat sweep mode, the A-D converter continues operating until this bit is cleared to "0" by software.

(4) A-D conversion frequency (ϕAD) selection flag (bit 7)

Conversion time varies according to the A-D converter's operating clock (ϕAD) selected by this bit as listed in Table 9.2.1. Since the A-D converter's comparator consists of capacity coupling amplifiers, keep that ϕAD ≥ 250 kHz during A-D conversion.

Table 9.2.1 Conversion time per one analog input pin (Unit: μs)

A-D conversion frequency (ϕAD) selection flag		0	1
ϕAD		f2 divided by 4	f2 divided by 2
Conversion time	Resolution : 8 bits	15.68	7.84
•System clock = 25 MHz **(Note)**	Resolution : 10 bits	18.88	9.44

Note: This is applied when the following conditions are satisfied;

•f(XIN) = 25 MHz

•The main clock is selected as the system clock.

•Main clock divided by 2 is available.

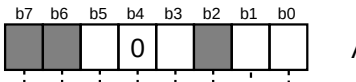
EOL announced

A-D CONVERTER

9.2 Block description

9.2.2 A-D control register 1

Figure 9.2.3 shows the structure of A-D control register 1.



A-D control register 1 (address 1F 16)

Bit	Bit name	Functions	At reset	RW
0	A-D sweep pin selection bits (Valid in the single sweep and repeat sweep modes.) **(Note 1)**	b1 b0 0 0: Pins AN_0 and AN_1 (2 pins) 0 1: Pins AN_0 to AN_3 (4 pins) 1 0: Pins AN_0 to AN_5 (6 pins) **(Note 2)** 1 1: Pins AN_0 to AN_7 (8 pins)	1	RW
1			1	RW
2	Not implemented.		Undefined	_
3	8/10-bit mode selection bit	0: 8-bit resolution 1: 10-bit resolution	0	RW
4	Must be fixed to "0."		0	RW
5	V_{REF} connection selection bit **(Note 4)**	0: Pin V_{REF} is connected. 1: Pin V_{REF} is disconnected. (High impedance)	0	RW
6	Not implemented.		Undefined	_
7				

Notes 1: These bits are ignored in the one-shot and repeat modes. (They may be "0" or "1.")
2: When an external trigger is selected, pin AN_5 cannot be used as an analog input pin.
3: Writing to each bit of the A-D control register 1 must be performed while the A-D converter stops operating.
4: When the V_{REF} connection selection bit is cleared from "1" to "0," wait for an interval of 1 µs or more passed, and then start A-D conversion.

Fig. 9.2.3 Structure of A-D control register 1

(1) A-D sweep pin selection bits (bits 1 and 0)

These bits are used to select analog input pins in the single sweep and repeat sweep modes. Refer to section **"9.2.5 Port P7 direction register."**

(2) V_{REF} connection selection bit (bit 5)

This bit is used to disconnect the A-D converter's resistor ladder network from the reference voltage input pin (V_{REF}) when not using the A-D converter.

When pin V_{REF} is disconnected from the resistor ladder network, no current flows from pin V_{REF} to the resistor ladder network.

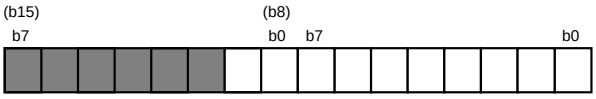
EOL announced

9.2.3 A-D register i (i = 0 to 7)

Figure 9.2.4 shows the structure of A-D register i. When A-D conversion is completed, the conversion result (in other words, the contents of the successive approximation register) is stored into this register. Each A-D register i corresponds to an analog input pin (ANi), one for one. Table 9.2.2 lists the correspondence of an analog input pin to A-D register i.

●When resolution = 8 bits

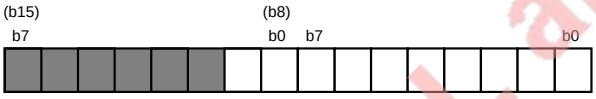
A-D register 0 (addresses 21 16 and 20 16)
A-D register 1 (addresses 23 16 and 22 16)
A-D register 2 (addresses 25 16 and 24 16)
A-D register 3 (addresses 27 16 and 26 16)
A-D register 4 (addresses 29 16 and 28 16)
A-D register 5 (addresses 2B 16 and 2A 16)
A-D register 6 (addresses 2D 16 and 2C 16)
A-D register 7 (addresses 2F 16 and 2E 16)



Bit	Functions	At reset	RW
7 to 0	The A-D conversion result is read out.	Undefined	RO
15 to 8	"0" at reading.	0	RO

●When resolution = 10 bits

A-D register 0 (addresses 21 16 and 20 16)
A-D register 1 (addresses 23 16 and 22 16)
A-D register 2 (addresses 25 16 and 24 16)
A-D register 3 (addresses 27 16 and 26 16)
A-D register 4 (addresses 29 16 and 28 16)
A-D register 5 (addresses 2B 16 and 2A 16)
A-D register 6 (addresses 2D 16 and 2C 16)
A-D register 7 (addresses 2F 16 and 2E 16)



Bit	Functions	At reset	RW
9 to 0	The A-D conversion result is read out.	Undefined	RO
15 to 10	"0" at reading.	0	RO

EOL announced

Fig. 9.2.4 Structure of A-D register i

Table 9.2.2 Correspondence of analog input pin and A-D register i

Analog input pin	A-D register i where conversion result is stored
Pin AN0	A-D register 0
Pin AN1	A-D register 1
Pin AN2	A-D register 2
Pin AN3	A-D register 3
Pin AN4	A-D register 4
Pin AN5	A-D register 5
Pin AN6	A-D register 6
Pin AN7	A-D register 7

A-D CONVERTER

9.2 Block description

9.2.4 A-D/UART2 trans./rece. interrupt control register

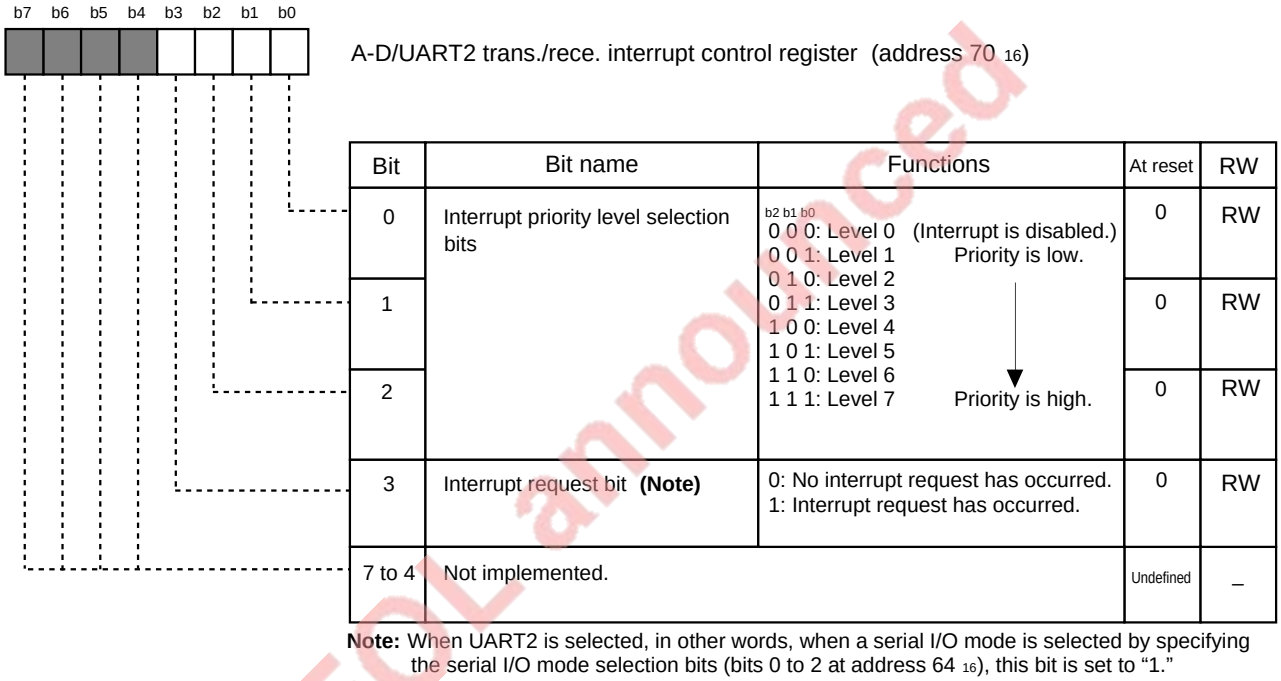
Figure. 9.2.5 shows the structure of the A-D/UART2 trans./rece. control register.

The A-D conversion interrupt and UART2 transmission/reception interrupt share the same interrupt control register and interrupt vector addresses.

When UART2 is selected, the A-D/UART2 trans./rece. interrupt control register functions as an register which control the UART2 transmission/reception interrupt. At this time, the A-D conversion interrupt cannot be used.

For details on interrupts, refer to chapter **"4. INTERRUPTS."** For details on UART2, refer to chapter **"8. SERIAL I/O."**

The case where this register is used as the A-D conversion interrupt control register is described below.



Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2 b1 b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 Priority is low. 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7 Priority is high.	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit **(Note)**	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
7 to 4	Not implemented.		Undefined	–

Note: When UART2 is selected, in other words, when a serial I/O mode is selected by specifying the serial I/O mode selection bits (bits 0 to 2 at address 64 16), this bit is set to "1."

EOL announced

Fig. 9.2.5 Structure of A-D/UART2 trans./rece. interrupt control register

(1) Interrupt priority level selection bits (bits 2 to 0)

These bits select an A-D conversion interrupt's priority level. When using A-D conversion interrupts, select one priority level from levels 1 to 7. If an A-D conversion interrupt request occurs, its priority level is compared with the processor interrupt priority level (IPL), and the requested interrupt is enabled only when its priority level is higher than the IPL. (Note that this is applied to the case where the interrupt disable flag (I) = "0.") When disabling A-D conversion interrupts, set these bits to "000_2" (Level 0).

(2) Interrupt request bit (bit 3)

This bit is set to "1" when an A-D conversion interrupt request occurs. This bit is automatically cleared to "0" when the A-D conversion interrupt request is accepted.

Note that this bit can be set to "1" or cleared to "0" by software.

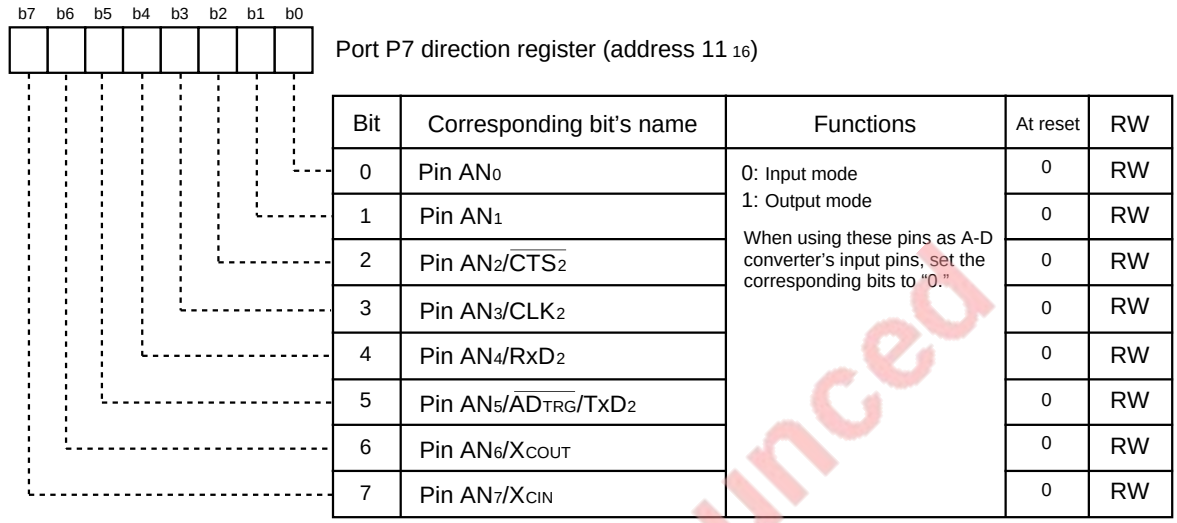
EOL announced

A-D CONVERTER

9.2 Block description

9.2.5 Port P7 direction register

Input pins of the A-D converter are multiplexed with port P7. When using these pins as A-D converter's input pins, set the corresponding bits of the port P7 direction register to "0" to set these ports for the input mode. Figure 9.2.6 shows the relationship between the port P7 direction register and I/O pins of the sub-clock oscillation circuit and peripheral functions.



Port P7 direction register (address 11_{16})

Bit	Corresponding bit's name	Functions	At reset	RW
0	Pin AN_0	0: Input mode 1: Output mode When using these pins as A-D converter's input pins, set the corresponding bits to "0."	0	RW
1	Pin AN_1		0	RW
2	Pin $AN_2/\overline{CTS_2}$		0	RW
3	Pin AN_3/CLK_2		0	RW
4	Pin AN_4/RxD_2		0	RW
5	Pin $AN_5/\overline{ADTRG}/TxD_2$		0	RW
6	Pin AN_6/X_{COUT}		0	RW
7	Pin AN_7/X_{CIN}		0	RW

Fig. 9.2.6 Relationship between port P7 direction register and I/O pins of sub-clock oscillation circuit and peripheral functions

Analog input pins function as the port P7's I/O pins and also function as I/O pins of the sub-clock oscillation circuit and UART2. For pins which are forcedly set to the output mode when the function for the sub-clock oscillation circuit or UART2 is selected, analog input is disabled. (Refer to **"Table 9.2.3."**)

Table 9.2.3 Port P7's pin which is forcedly set to output mode

Pin	Conditions where pin is forcedly set to output mode
$P7_3/AN_3/CLK_2$	Clock synchronous serial I/O mode is selected and an internal clock is used. (bits 3 to 0 at address 64_{16} = "0001_2")
$P7_5/AN_5/\overline{ADTRG}/TxD_2$	Serial I/O mode is selected. (bits 2 to 0 at address 64_{16} = "001_2," "100_2," "101_2," or "110_2")
$P7_6/AN_6/X_{COUT}$	Sub-clock oscillation circuit is operating by itself. (bit 4 at address $6C_{16}$ = "1" and bit 2 at address $6F_{16}$ = "0")

EOL announced

9.3 A-D conversion method

The A-D converter compares the comparison voltage (V_{ref}), which is internally generated according to the contents of the successive approximation register, and the analog input voltage (V_{IN}), which is input from the analog input pin. By reflecting the comparison result on the successive approximation register, V_{IN} is converted into a digital value (successive approximation method). When a trigger occurs, the A-D converter performs the following processing:

① Determination of successive approximation register's bit 9
The A-D converter compares V_{ref} and V_{IN}. At this time, contents of the successive approximation register is "1000000000_2" (Initial value).
Bit 9 of the successive approximation register changes according to the comparison result as follows:
If $V_{ref} < V_{IN}$, bit 9 = "1"
If $V_{ref} > V_{IN}$, bit 9 = "0"

② Determination of successive approximation register's bit 8
After setting bit 8 of the successive approximation register to "1," the A-D converter compares V_{ref} and V_{IN}. Bit 8 changes according to the comparison result as follows:
If $V_{ref} < V_{IN}$, bit 8 = "1"
If $V_{ref} > V_{IN}$, bit 8 = "0"

③ Determination of successive approximation register's bits 7 to LSB
When resolution = 8 bits ..... For bits 7 to 2, perform operation ②.
When resolution = 10 bits ..... For bits 7 to 0, perform operation ②.

When the LSB is determined, the contents of the successive approximation register, in other words, the conversion result is transferred to the A-D register i.

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V_{ref} is generated according to the latest contents of the successive approximation register. Table 9.3.1 lists the relationship between the successive approximation register's contents and V_{ref}. Tables 9.3.2 and 9.3.3 list changes of the successive approximation register and V_{ref} during A-D conversion. Figure 9.3.1 shows theoretical A-D conversion characteristics when resolution = 10 bits.

Table 9.3.1 Relationship between successive approximation register's contents and Vref

Successive approximation register's contents: n	V_{ref} (V)
0	0
1 to 1023	$\frac{V_{REF}^*}{1024} \times (n - 0.5)$

V_{REF}*: Reference voltage

A-D CONVERTER

9.3 A-D conversion method

Table 9.3.2 Change of successive approximation register and Vref during A-D conversion (when resolution = 8 bits)

	Successive approximation register	Vref
A-D converter stopped	b9 b0 1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$ [V]
1st comparison	1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} - \frac{V_{REF}}{2048}$ [V]
2nd comparison	n9 1 0 0 0 0 0 0 0 0 1st comparison result	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} - \frac{V_{REF}}{2048}$ [V] (•When $n_9 = 1$, $+\frac{V_{REF}}{4}$ •When $n_9 = 0$, $-\frac{V_{REF}}{4}$)
3rd comparison	n9 n8 1 0 0 0 0 0 0 0 2nd comparison result	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} - \frac{V_{REF}}{2048}$ [V] (•When $n_8 = 1$, $+\frac{V_{REF}}{8}$ •When $n_8 = 0$, $-\frac{V_{REF}}{8}$)
⋮	⋮	⋮
8th comparison	n9 n8 n7 n6 n5 n4 n3 1 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} \pm \cdots\cdots \pm \frac{V_{REF}}{256} - \frac{V_{REF}}{2048}$ [V]
Conversion complete	n9 n8 n7 n6 n5 n4 n3 n2 0 0	

Table 9.3.3 Change of successive approximation register and Vref during A-D conversion (when resolution = 10 bits)

	Successive approximation register	Vref
A-D converter stopped	b9 b0 1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$ [V]
1st comparison	1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} - \frac{V_{REF}}{2048}$ [V]
2nd comparison	n9 1 0 0 0 0 0 0 0 0 1st comparison result	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} - \frac{V_{REF}}{2048}$ [V] (•When $n_9 = 1$, $+\frac{V_{REF}}{4}$ •When $n_9 = 0$, $-\frac{V_{REF}}{4}$)
3rd comparison	n9 n8 1 0 0 0 0 0 0 0 2nd comparison result	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} - \frac{V_{REF}}{2048}$ [V] (•When $n_8 = 1$, $+\frac{V_{REF}}{8}$ •When $n_8 = 0$, $-\frac{V_{REF}}{8}$)
⋮	⋮	⋮
10th comparison	n9 n8 n7 n6 n5 n4 n3 n2 n1 1	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8} \pm \cdots\cdots \pm \frac{V_{REF}}{1024} - \frac{V_{REF}}{2048}$ [V]
Conversion complete	n9 n8 n7 n6 n5 n4 n3 n2 n1 n0	

Not announced

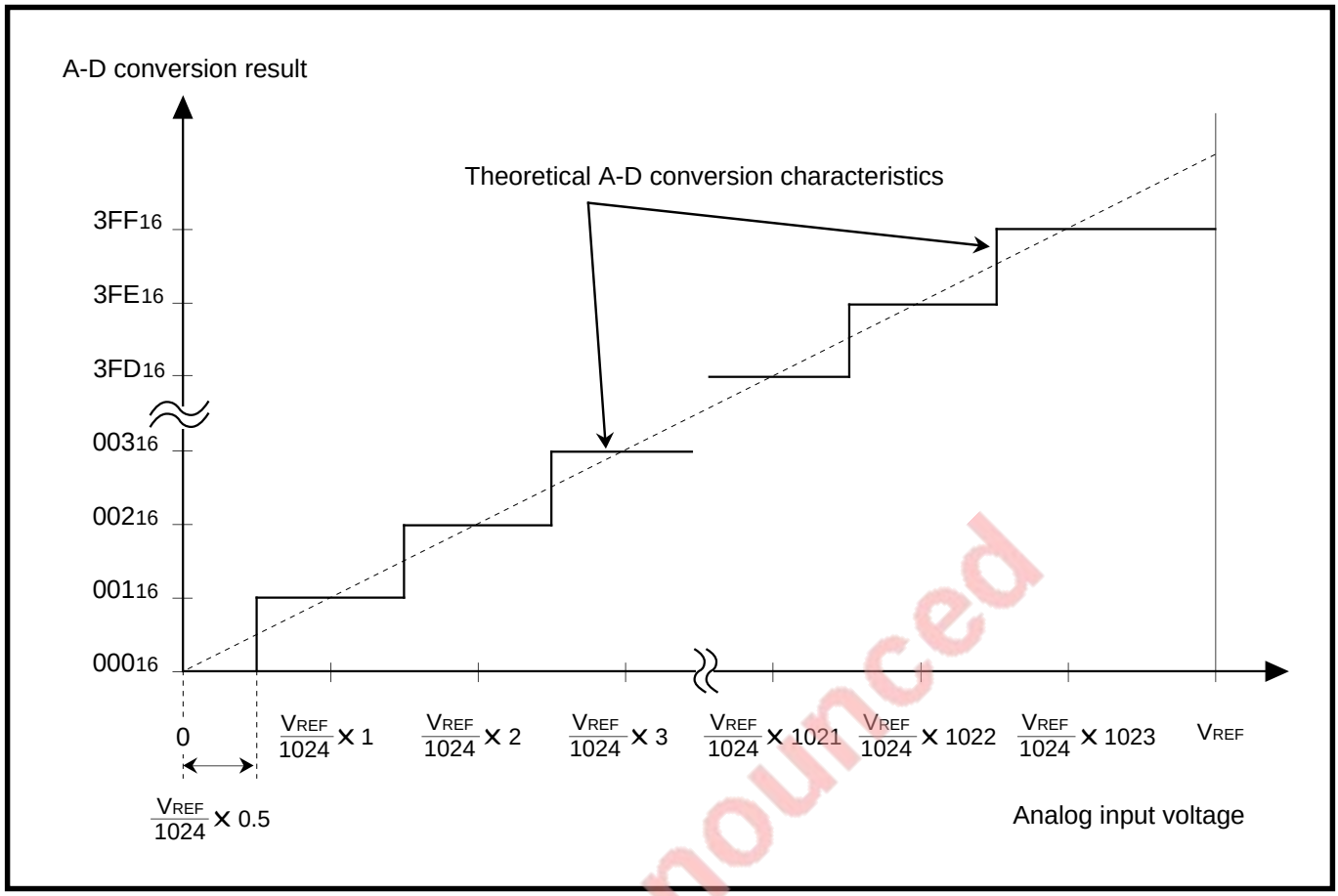

Fig. 9.3.1 Theoretical A-D conversion characteristics when resolution = 10 bits

EOL announced

9.4 Absolute accuracy and Differential non-linearity error

The A-D conversion's accuracy is described below.

9.4.1 Absolute accuracy

The absolute accuracy is the difference expressed in the LSB between the actual A-D conversion result and the output code of an A-D converter with ideal characteristics. The analog input voltage when measuring the accuracy is assumed to be the mid point of the input voltage width that outputs the same output code from an A-D converter with ideal characteristics. For example, in the case of the 10-bit resolution, when V_{REF} = 5.12 V, 1-LSB width is 5 mV, and 0 mV, 5 mV, 10 mV, 15 mV, 20 mV, ... are selected as the analog input voltages.

The absolute accuracy = ±3 LSB when the analog input voltage = 25 mV indicates that the output code expected from an ideal A-D conversion characteristics is "005_{16}" but the actual A-D conversion result is between "002_{16}" to "008_{16}."

The absolute accuracy includes the zero error and the full-scale error.

The absolute accuracy degrades when V_{REF} is lowered. The output codes for analog input voltages between V_{REF} and AV_{CC} are "$3FF_{16}$."

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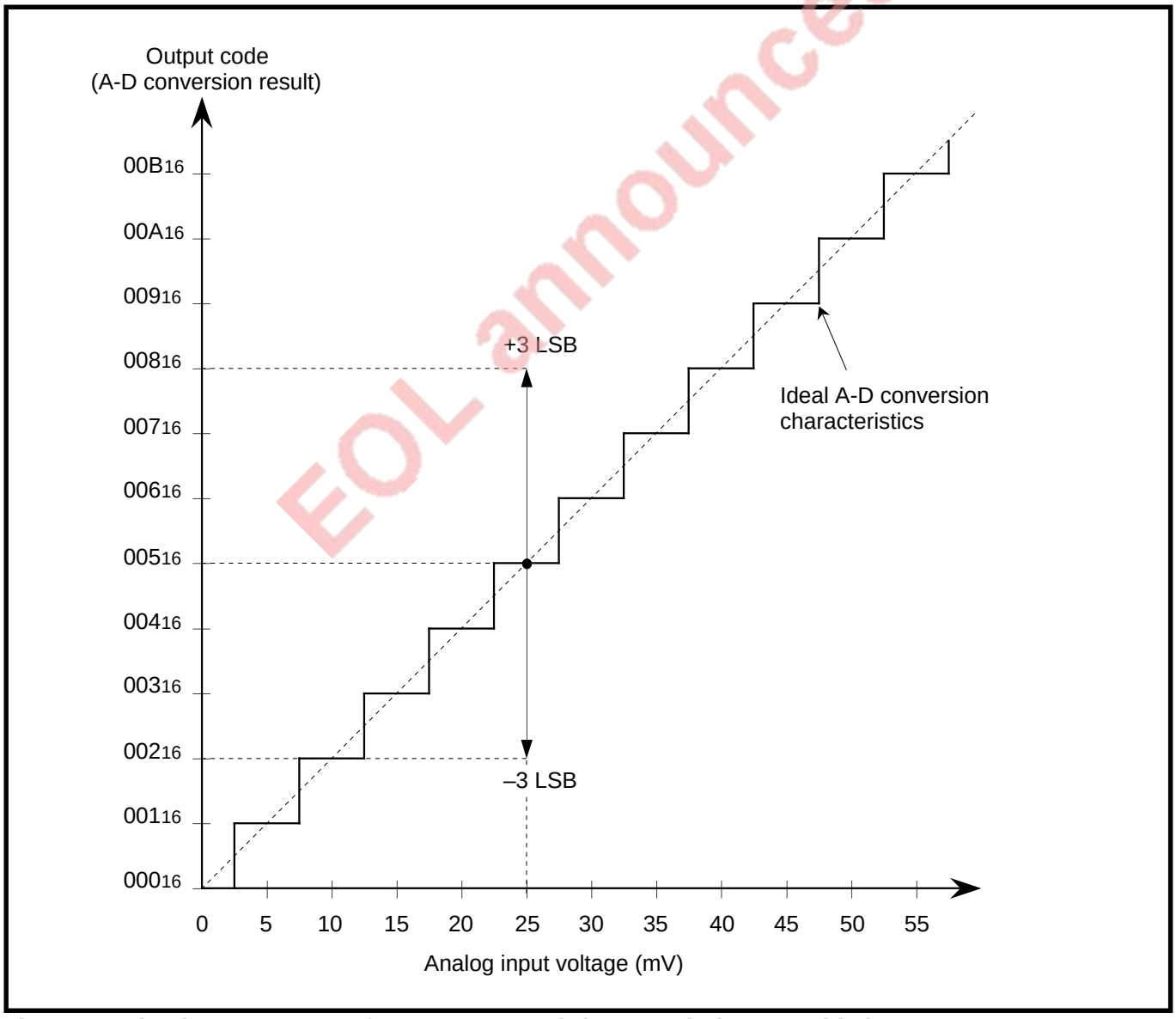
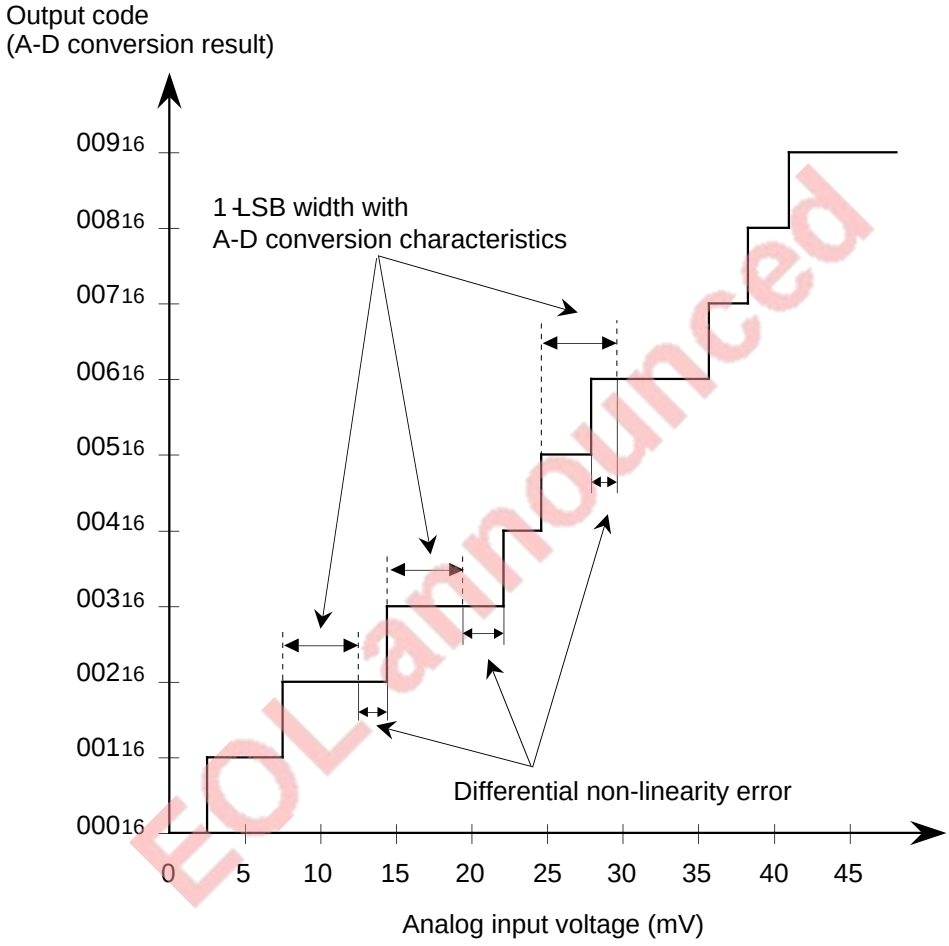


Fig. 9.4.1 Absolute accuracy of A-D converter (when resolution = 10 bits)

9.4.2 Differential non-linearity error

The differential non-linearity error indicates the difference between the 1-LSB step width (the ideal analog input voltage width while the same output code is expected to output) of an A-D converter with ideal characteristics and the actual measured step width (the actual analog input voltage width while the same output code is output). For example, in the case of the 10-bit mode, when V_{REF} = 5.12 V, the 1-LSB width of an A-D converter with ideal characteristics is 5 mV, but if the differential non-linearity error is ±1 LSB, the actual measured 1-LSB width is 0 to 10 mV. (Refer to section **"16.1.4 A-D converter standard characteristics."**)



EOL announced

Fig. 9.4.2 Differential non-linearity error (when resolution = 10 bits)

A-D CONVERTER

9.4 Absolute accuracy and Differential non-linearity error

9.4.3 Comparison voltage when resolution = 8 bits

When 8-bit resolution is selected in the M37733MHBXXXFP, the high-order 8 bits of the 10-bit successive approximation register is the conversion result.

Accordingly, when compared with the 8-bit A-D converter, the comparison reference voltage is different by $3V_{REF}/2048$ (refer to the underlined portions in the Table 9.4.1). The difference of the output code change point is generated as shown in Figure 9.4.3.

Table 9.4.1 Compare reference voltage

	M37733MHBXXXFP (When resolution = 8 bits)	8-bit A-D converter
Comparison reference voltage V_{ref}	V_{REF}*1/2^8 × n*2 – $\underline{V_{REF}/2^{10} \times 0.5}$	$V_{REF}/2^8$ × n – $\underline{V_{REF}/2^8 \times 0.5}$

V_{REF}*1: Reference voltage

n*2: Contents of successive approximation register

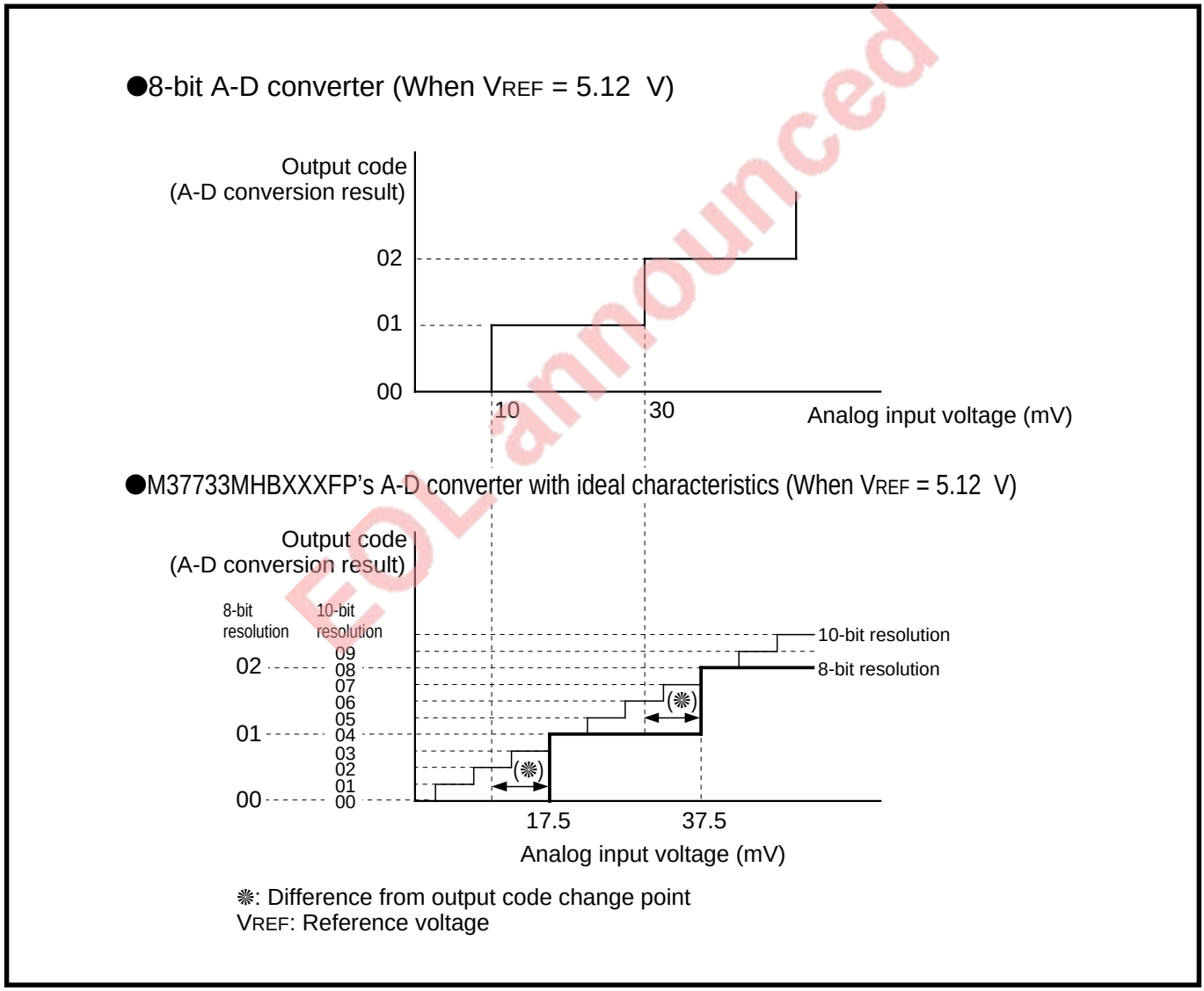


Fig. 9.4.3 Difference of output code change point

EOL announced

9.5 One-shot mode

•A-D operation mode selection bits (bits 4 and 3 at address $1E_{16}$) = “00_2”

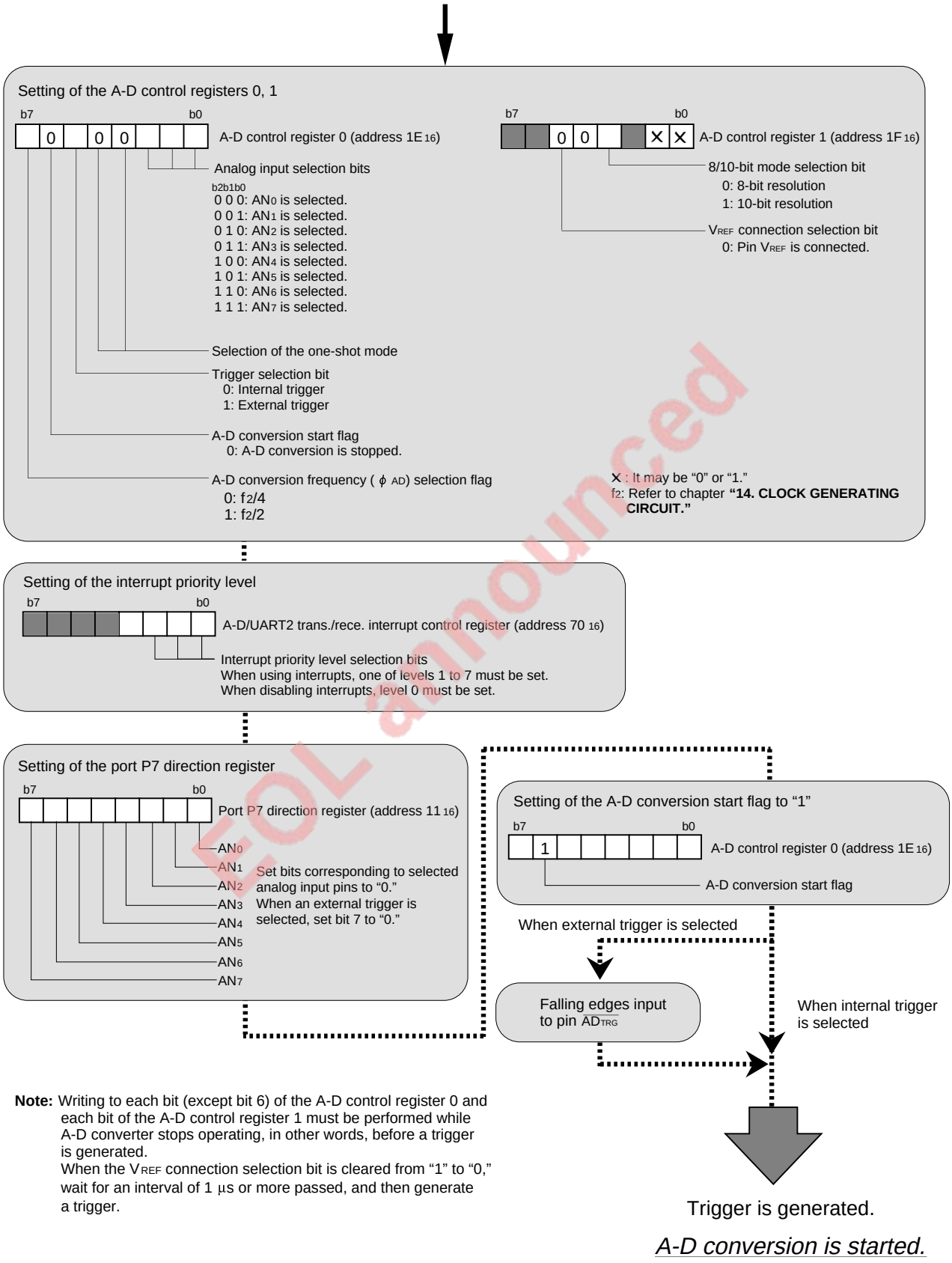
In this mode, A-D conversion is once performed for the input voltage of one analog input pin. An A-D conversion interrupt request occurs when the A-D conversion is completed. Note that an A-D conversion interrupt cannot be used when the UART2 transmission/reception interrupt is used.

9.5.1 Setting for one-shot mode

Figure 9.5.1 shows an initial setting example for registers related to the one-shot mode.
When using interrupts, settings for enabling interrupts are required. For details, refer to chapter **“4. INTERRUPTS.”**

EOL announced

9.5 One-shot mode



Note: Writing to each bit (except bit 6) of the A-D control register 0 and each bit of the A-D control register 1 must be performed while A-D converter stops operating, in other words, before a trigger is generated.
When the V_{REF} connection selection bit is cleared from "1" to "0," wait for an interval of 1 µs or more passed, and then generate a trigger.

Fig. 9.5.1 Initial setting example for registers related to one-shot mode

9.5.2 Operation in one-shot mode

Figure 9.5.2 shows the conversion operation in the one-shot mode.

(1) When internal trigger is selected

① By setting the A-D conversion start flag to "1," the A-D converter starts operating.

② The A-D conversion is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register i.

- 49 cycles of ϕ_{AD} have passed when resolution = 8 bits
- 59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ When a UART2 trans./rece. interrupt is not used, the A-D conversion interrupt request bit is set to "1" simultaneously with ②.

④ The A-D conversion start flag is cleared to "0," and then the A-D converter stops operating.

(2) When external trigger is selected

① If pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L" when the A-D conversion start flag = "1," the A-D converter starts operating.

② The A-D conversion is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register i.

- 49 cycles of ϕ_{AD} have passed when resolution = 8 bits
- 59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ When a UART2 trans./rece. interrupt is not used, the A-D conversion interrupt request bit is set to "1" simultaneously with ②.

④ The A-D converter stops operating.

The A-D conversion start flag remains set to "1" after the A-D converter stops operating. Accordingly, when pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L", the A-D converter restarts conversion from ①. Note that when pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L" during A-D conversion, the converter quits the conversion which is performed at that time and restarts it from ①.

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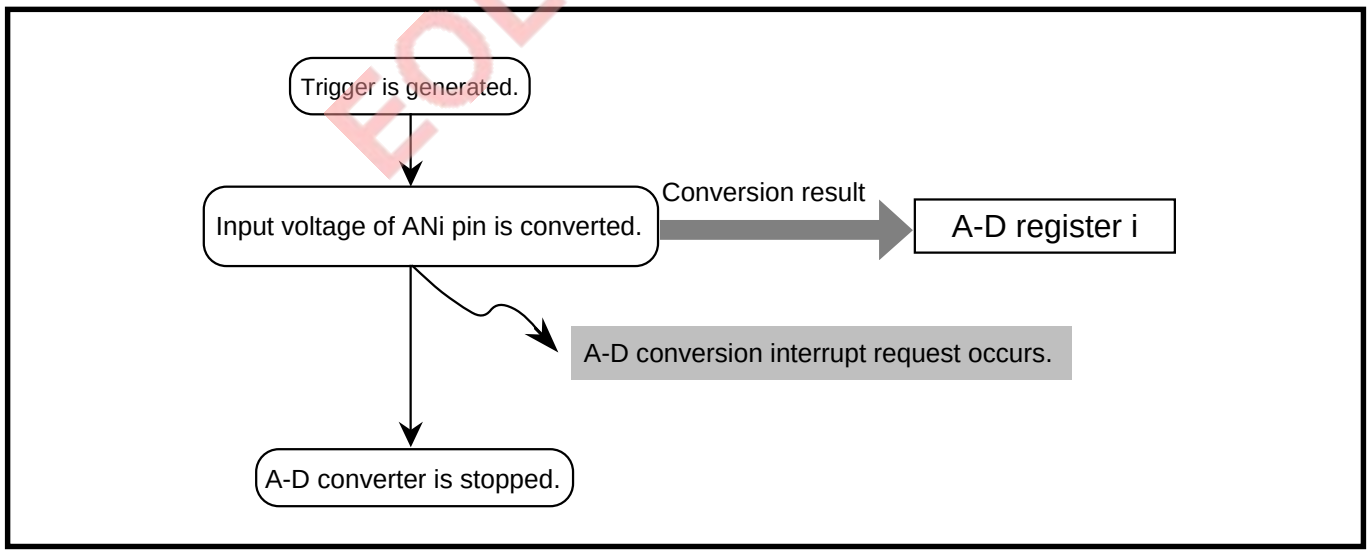


Fig. 9.5.2 Conversion operation in one-shot mode

9.6 Repeat mode

•A-D operation mode selection bits (bits 4 and 3 at address $1E_{16}$) = “01_2”

In this mode, A-D conversion is repeatedly performed for the input voltage of one analog input pin. No A-D conversion interrupt request occurs in this mode. The A-D conversion start flag (bit 6 at address $1E_{16}$) remains set to “1” until it is cleared to “0” by software. While the A-D conversion start flag = “1,” the A-D converter repeats A-D conversion without a stop.

9.6.1 Setting for repeat mode

Figure 9.6.1 shows an initial setting example for registers related to the repeat mode.

EOL announced

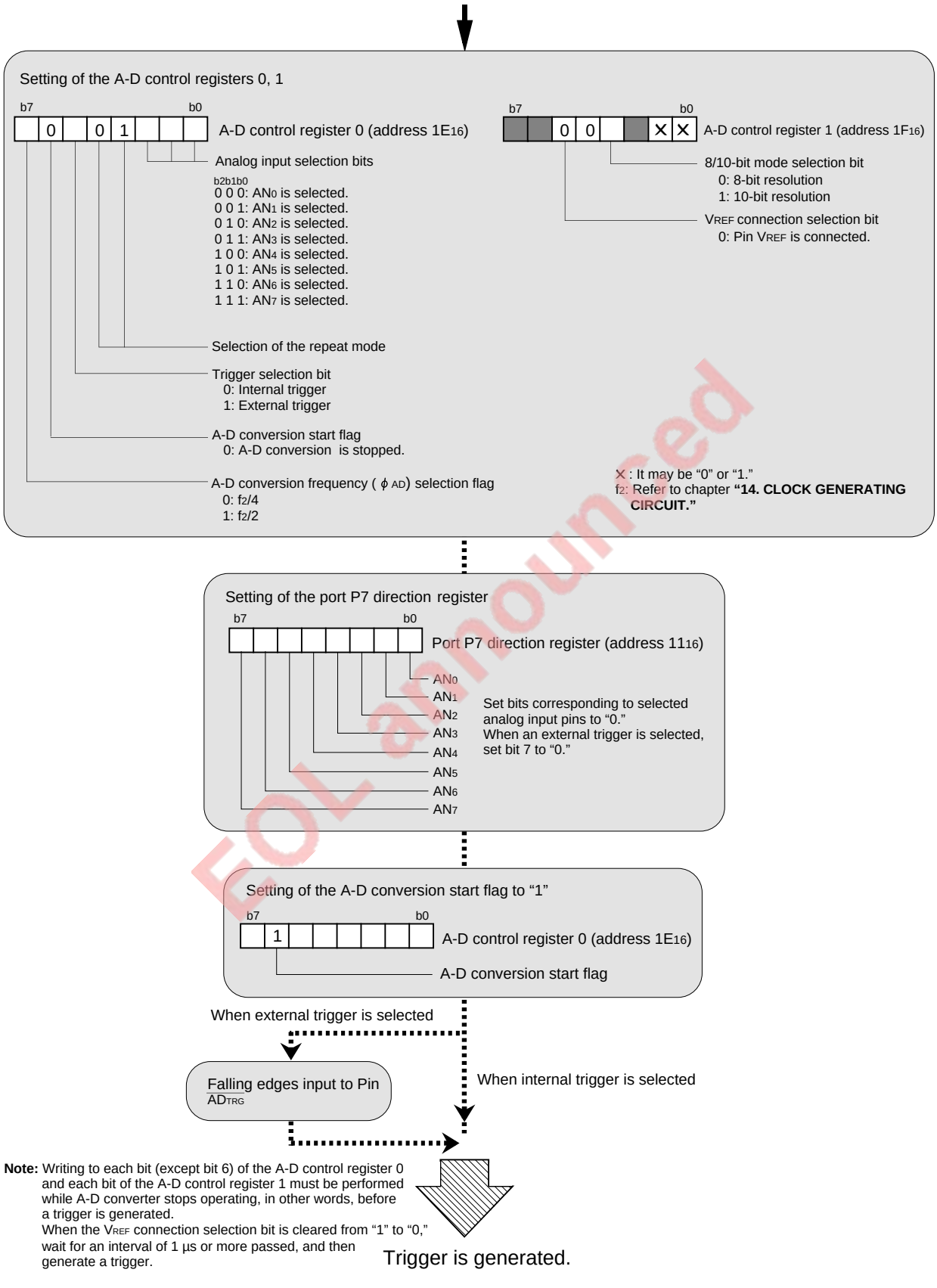


Fig. 9.6.1 Initial setting example for registers related to repeat mode

EOL announced

A-D CONVERTER

9.6 Repeat mode

9.6.2 Operation in repeat mode

Figure 9.6.2 shows the conversion operation in the repeat mode.

(1) When internal trigger is selected

① When the A-D conversion start flag is set to "1," the A-D converter starts operating.

② The first A-D conversion is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register i.

- 49 cycles of ϕ_{AD} have passed when resolution = 8 bits
- 59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ The A-D converter continues operating until the A-D conversion start flag is cleared to "0" by software. Each time A-D conversion is completed, the conversion result is transferred to the A-D register i.

(2) When external trigger is selected

① If pin $\overline{ADTRG}$'s level goes from "H" to "L" when the A-D conversion start flag = "1," the A-D converter starts operating.

② The first A-D conversion is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register i.

- 49 cycles of ϕ_{AD} have passed when resolution = 8 bits
- 59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ The A-D converter continues operating until the A-D conversion start flag is cleared to "0" by software. Each time A-D conversion is completed, the conversion result is transferred to the A-D register i.

Note that when pin $\overline{ADTRG}$'s level goes from "H" to "L" during A-D conversion, the A-D converter quits the conversion which is performed at that time and restarts it from ①.

EOL announced

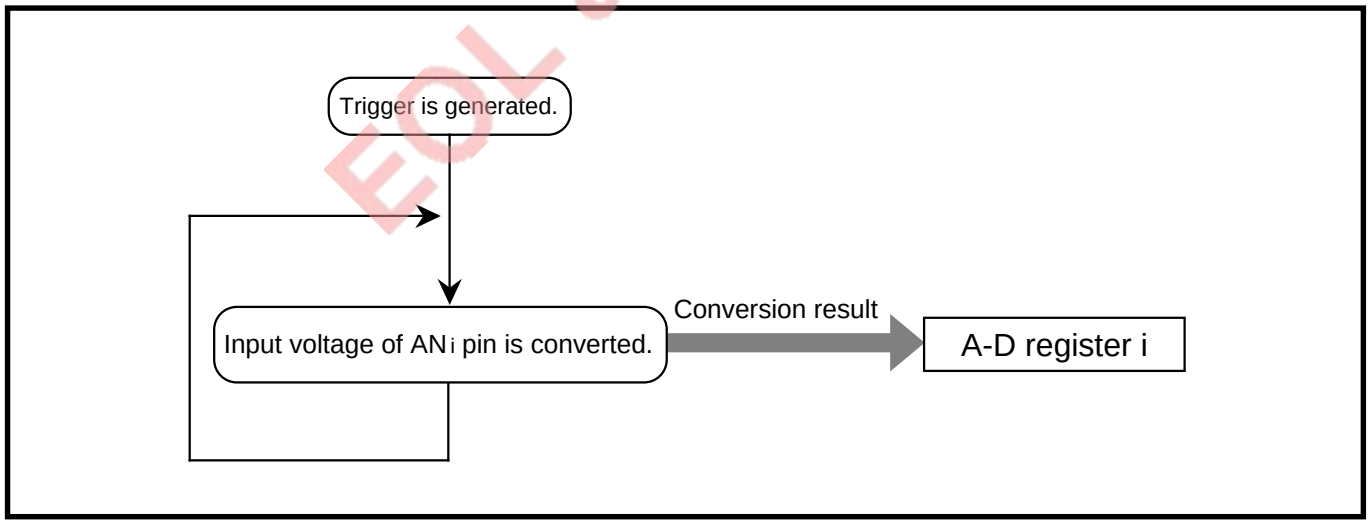


Fig. 9.6.2 Conversion operation in repeat mode

9.7 Single sweep mode

•A-D operation mode selection bits (bits 4 and 3) = “10_2”

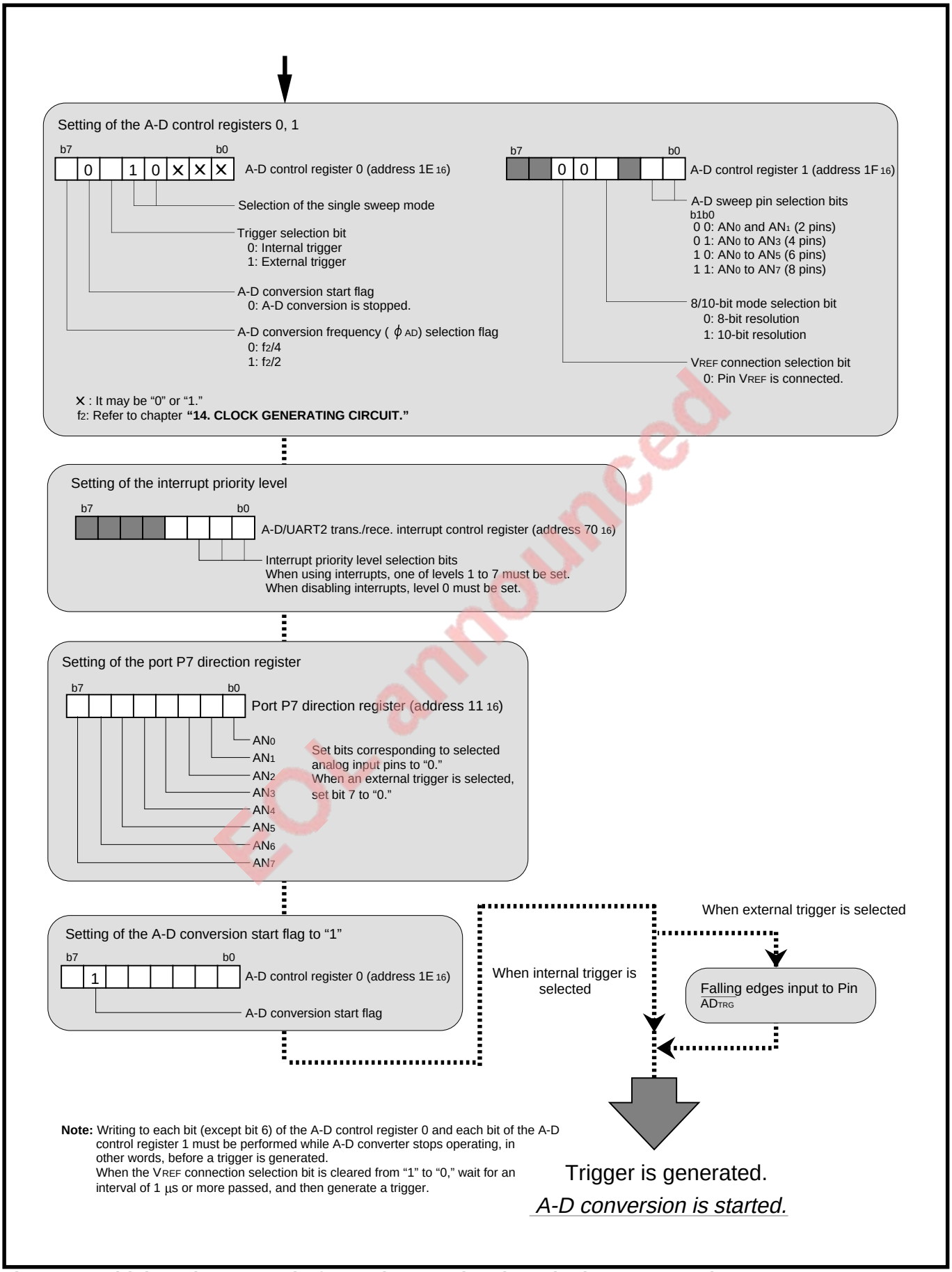
In this mode, A-D conversion is performed for the input voltage of multiple analog input pins, one at a time. A-D conversion is performed in order of AN_0, AN_1, AN_2, ... An A-D conversion interrupt request occurs when A-D conversions are completed for all analog input pins selected.

9.7.1 Setting for single sweep mode

Figure 9.7.1 shows an initial setting example for registers related to the single sweep mode.
When using interrupts, settings for enabling interrupts are required. For details, refer to chapter **“4. INTERRUPTS.”**

EOL announced

9.7 Single sweep mode



Note: Writing to each bit (except bit 6) of the A-D control register 0 and each bit of the A-D control register 1 must be performed while A-D converter stops operating, in other words, before a trigger is generated.
When the VREF connection selection bit is cleared from "1" to "0," wait for an interval of 1 μs or more passed, and then generate a trigger.

Fig. 9.7.1 Initial setting example for registers related to single sweep mode

EOL announced

9.7.2 Operation in single sweep mode

Figure 9.7.2 shows the conversion operation in the single sweep mode.

(1) When internal trigger is selected

① When the A-D conversion start flag is set to "1," the A-D converter starts A-D conversion for an input voltage of pin AN0.

② The A-D conversion for pin AN0 is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register 0.

- 49 cycles of ϕ_{AD} have passed when resolution = 8 bits
- 59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ A-D conversion is performed for all analog input pins selected. Each time A-D conversion is completed for a pin, the conversion result is transferred to the A-D register i which corresponds to the pin.

④ When a UART2 trans./rece. interrupt is not used, the A-D conversion interrupt request bit is set to "1" at completion of ③.

⑤ The A-D conversion start flag is cleared to "0," and the A-D converter stops operating.

(2) When external trigger is selected

① If pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L" when the A-D conversion start flag = "1," the A-D converter starts A-D conversion for the input voltage of pin AN0.

② The A-D conversion for pin AN0 is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register 0.

- 49 cycles of ϕ_{AD} have passed when resolution = 8 bits
- 59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ A-D conversion is performed for all analog input pins selected. Each time A-D conversion is completed for a pin, the conversion result is transferred to the A-D register i which corresponds to the pin.

④ When a UART2 trans./rece. interrupt is not used, the A-D conversion interrupt request bit is set to "1" at completion of ③.

⑤ The A-D converter stops operating.

The A-D conversion start flag remains set to "1" after this. Accordingly, when pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L," the A-D converter restarts conversion from ①. Note that if pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L" during A-D conversion, the A-D converter quits the conversion which is performed at that time and restarts it from ①.

EOL announced

9.7 Single sweep mode

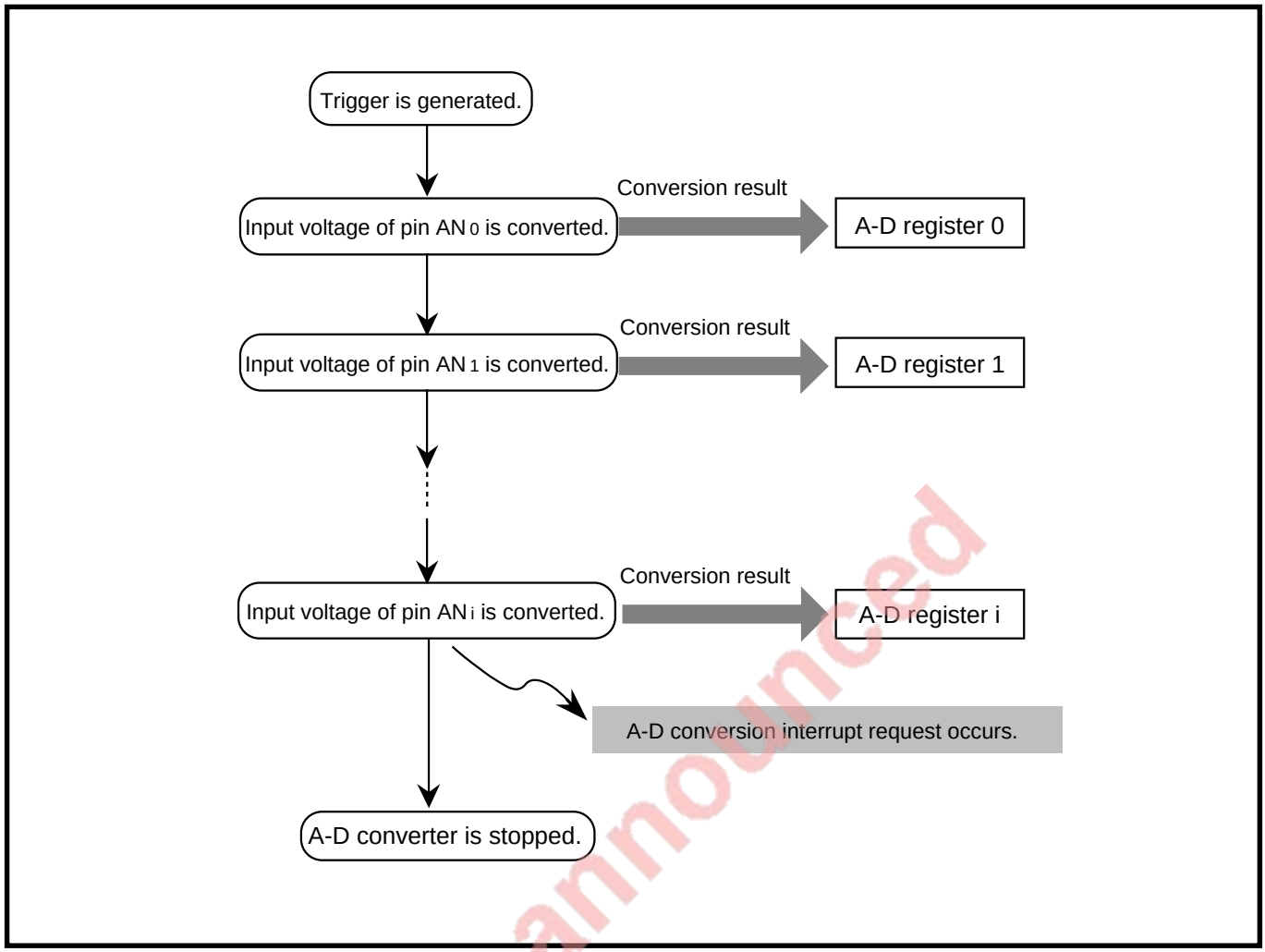


Fig. 9.7.2 Conversion operation in single sweep mode

EOL announced

9.8 Repeat sweep mode

•A-D operation mode selection bits (bits 4 and 3 at address $1E_{16}$) = “11_2”

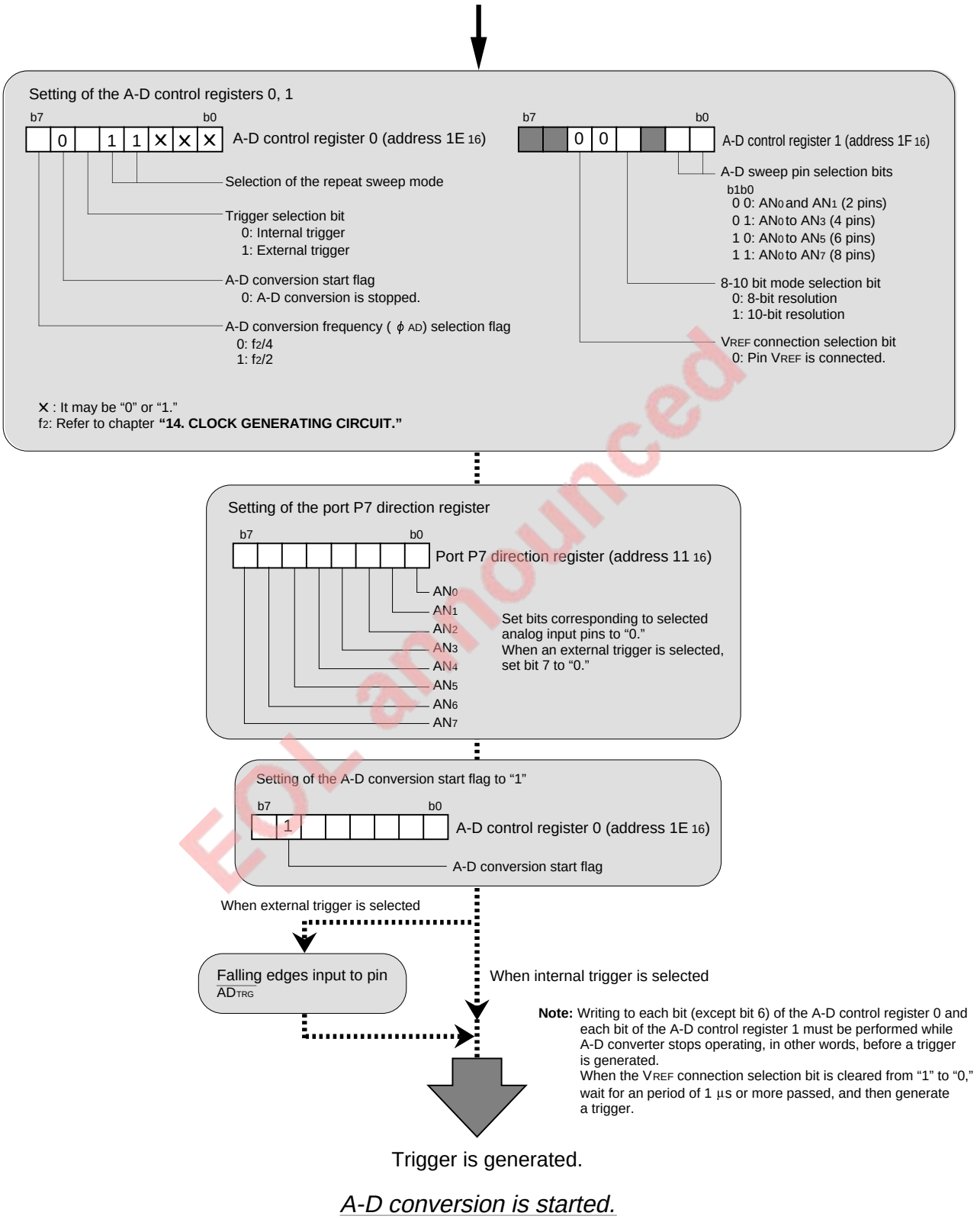
In this mode, A-D conversion is repeatedly performed for the input voltage of multiple analog input pins. A-D conversion is performed in order of AN_0, AN_1, AN_2, ...
No A-D conversion interrupt request occurs in this mode.
The A-D conversion start flag (bit 6 at address $1E_{16}$) remains set to “1” until it is cleared to “0” by software. While the A-D conversion start flag is “1,” the A-D converter repeats A-D conversion without a stop.

9.8.1 Setting for repeat sweep mode

Figure 9.8.1 shows an initial setting example for registers related to the repeat sweep mode.

EOL announced

9.8 Repeat sweep mode



EOL announced

Fig. 9.8.1 Initial setting example for registers related to repeat sweep mode

9.8.2 Operation in repeat sweep mode

Figure 9.8.2 shows the conversion operation in the repeat sweep mode.

(1) When internal trigger is selected

① When the A-D conversion start flag is set to "1," the A-D converter starts A-D conversion for an input voltage of pin AN0.

② The A-D conversion for pin AN0 is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register 0.

•49 cycles of ϕ_{AD} have passed when resolution = 8 bits

•59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ A-D conversion is performed for all analog input pins selected. Each time A-D conversion is completed for a pin, the conversion result is transferred to the A-D register i which corresponds to the pin.

④ A-D conversion is repeatedly performed for all analog input pins selected.

⑤ The A-D converter continues operating until the A-D conversion start flag is cleared to "0" by software.

(2) When external trigger is selected

① If pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L" when the A-D conversion start flag = "1," the A-D converter starts A-D conversion for the input voltage of pin AN0.

② The A-D conversion for pin AN0 is completed when one of the following conditions is satisfied, and then the contents of the successive approximation register (in other words, the conversion result) is transferred to the A-D register 0.

•49 cycles of ϕ_{AD} have passed when resolution = 8 bits

•59 cycles of ϕ_{AD} have passed when resolution = 10 bits

③ A-D conversion is performed for all analog input pins selected. Each time A-D conversion is completed for a pin, the conversion result is transferred to the A-D register i which corresponds to the pin.

④ A-D conversion is repeatedly performed for all analog input pins selected.

⑤ The A-D converter continues operating until the A-D conversion start flag is cleared to "0" by software.

Note that when pin $\overline{\text{ADTRG}}$'s level goes from "H" to "L" during A-D conversion, the A-D converter quits the conversion which is performed at that time and restarts it from ①.

EOL announced

9.8 Repeat sweep mode

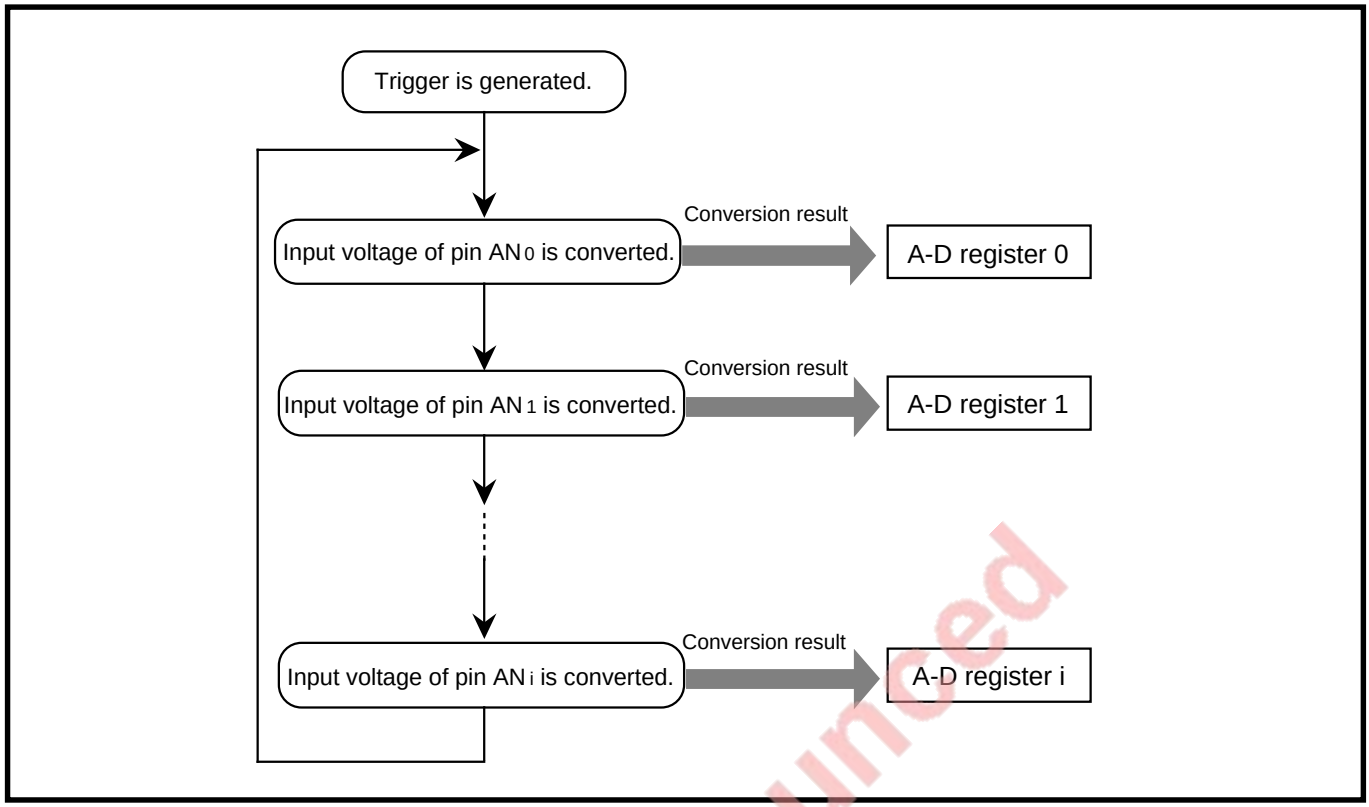


Fig. 9.8.2 Conversion operation in repeat sweep mode

EOL announced

9.9 Precautions for A-D converter

1. Writing to each bit (except bit 6) of the A-D control register 0 and each bit of the A-D control register 1 must be performed while the A-D converter stops operating, in other words, before a trigger is generated.

   When the V_{REF} connection selection bit is cleared from “1” to “0,” in other words, when pin V_{REF} is disconnected from the resistor ladder network, wait for an period of 1 μs or more, and then generate a trigger.

2. When an external trigger is selected, pin AN_5 cannot be used as an analog input pin because this pin is disconnected from the comparator. If pin AN_5 is selected as an analog input pin when an external trigger is selected, the A-D converter operates, but an undefined value is stored into the A-D register 5.

3. When using the A-D converter, refer to section **“Appendix 8. Countermeasures against noise,”** also.

EOL announced

9.9 Precautions for A-D converter

MEMO

EOL announced

CHAPTER 10
WATCHDOG TIMER

10.1 Block description
10.2 Operation description
10.3 Precautions for watchdog timer

EOL announced

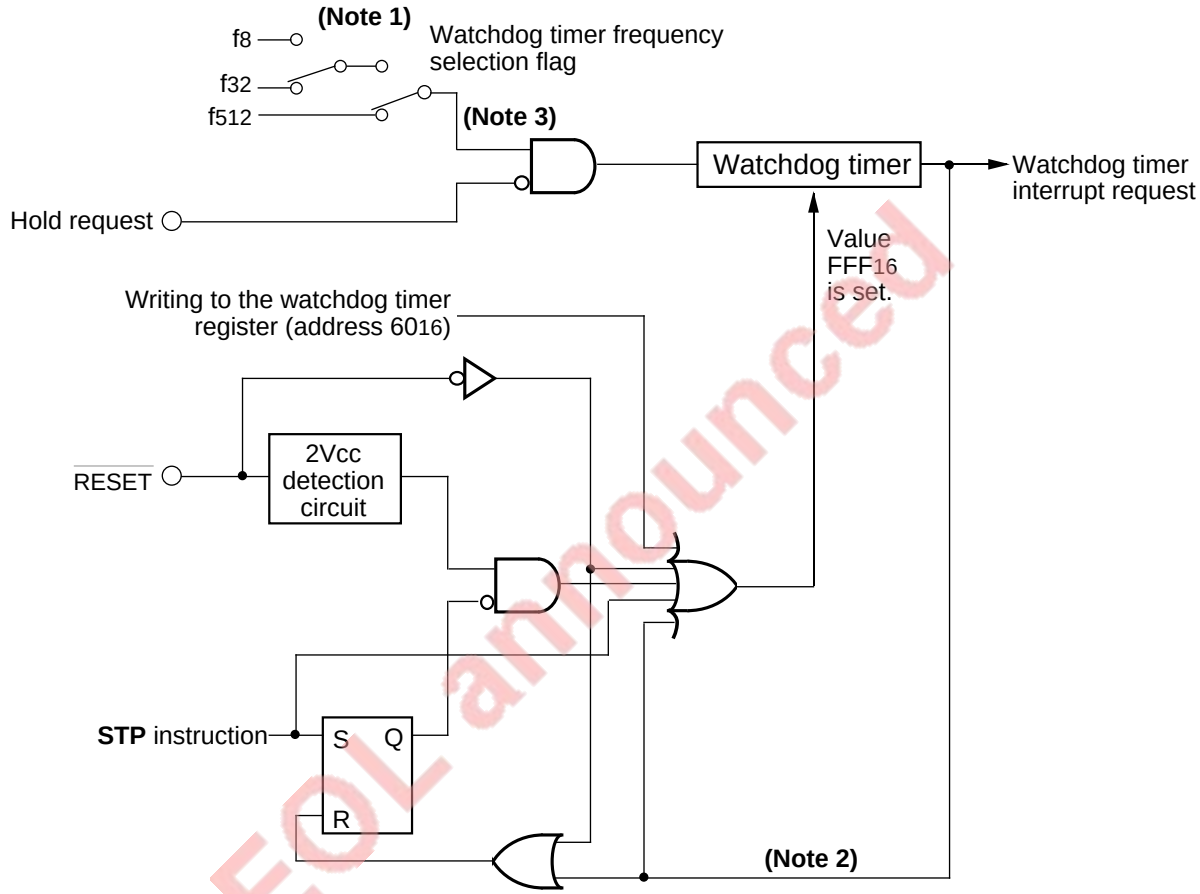
WATCHDOG TIMER

10.1 Block description

The watchdog timer is described below and functions as follows:
- Detects a program runaway.
- Measures a certain time from when oscillation starts at termination of the stop mode. (Refer to chapter **"11. STOP AND WAIT MODES."**)

10.1 Block description

Figure 10.1.1 shows the block diagram of the watchdog timer.



EOL announced

Clocks f8, f32, f512 : Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Notes 1: Only when the system clock selection bit (bit 3 at address 6C16) = "1" and the stop mode is terminated by an interrupt request generated, the watchdog timer is connected to clock f8.

2: Clock f16 is input when one of the following conditions is satisfied;
- The port-Xc selection bit = "0" and the main clock external input selection bit = "1"
- The system clock selection bit = "0" and the main clock external input selection bit = "1"
- The port-Xc selection bit = "1," the system clock selection bit = "1" and the sub clock external input selection bit = "1"

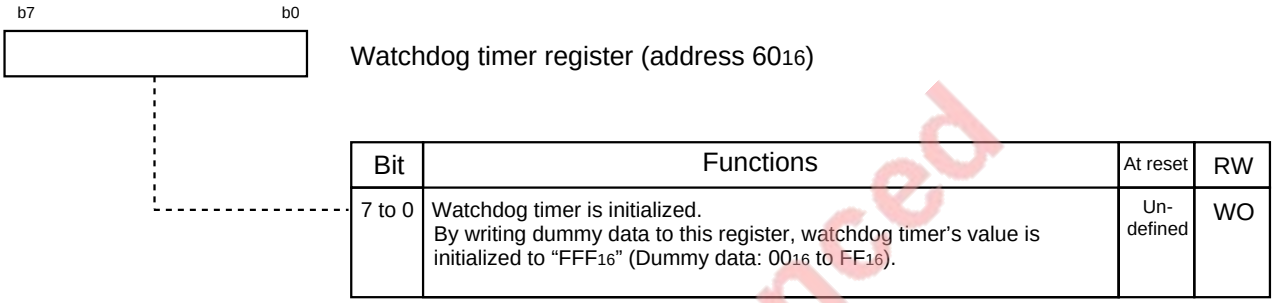
3: When the **STP** instruction is executed, the watchdog timer is connected as follows;
- Connected to clock f32 when the system clock selection bit = "0"
- Connected to clock f8 when the system clock selection bit = "1"

Fig. 10.1.1 Block diagram of watchdog timer

10.1.1 Watchdog timer

The watchdog timer is a 12-bit counter that down-counts a count source which is selected by the watchdog timer frequency selection flag (bit 0 at address 61_{16}). Value "FFF_{16}" is automatically set in the watchdog timer in the following cases. Note that an arbitrary value cannot be set in the watchdog timer.

- When dummy data is written to the watchdog timer register (Refer to **Figure 10.1.2.**)
- When the most significant bit of the watchdog timer becomes "0"
- When the **STP** instruction is executed (Refer to chapter **"11. STOP AND WAIT MODES."**)
- At reset



Watchdog timer register (address 60_{16})

Bit	Functions	At reset	RW
7 to 0	Watchdog timer is initialized. By writing dummy data to this register, watchdog timer's value is initialized to "FFF_{16}" (Dummy data: 00_{16} to FF_{16}).	Un-defined	WO

Fig. 10.1.2 Structure of watchdog timer register

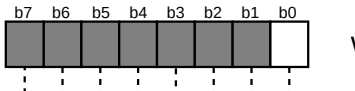
EOL announced

WATCHDOG TIMER

10.1 Block description

10.1.2 Watchdog timer frequency selection flag

This is used to select a watchdog timer's count source. Figure 10.1.3 shows the structure of the watchdog timer frequency selection flag.



Watchdog timer frequency selection flag (address 61_{16})

Bit	Bit name	Functions	At reset	RW
0	Watchdog timer frequency selection flag	0 : Clock f_{512} 1 : Clock f_{32}	0	RW
7 to 1	Not implemented.		Un-defined	—

Clocks f_{32}, f_{512} : Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Fig. 10.1.3 Structure of watchdog timer frequency selection flag

EOL announced

10.2 Operation description

The watchdog timer's operation is described below.
For its operation in the stop and wait modes, refer to chapter **"11. STOP AND WAIT MODES."**

10.2.1 Basic operation

①The watchdog timer starts counting down from "FFF_{16}."
②When the watchdog timer's most significant bit becomes "0," in other words, when the countdown has been performed 2048 times, a watchdog timer interrupt request occurs. (Refer to **Table 10.2.1.**)
③When the interrupt request occurs (②), value "FFF_{16}" is set to the watchdog timer.

The watchdog timer interrupt is a non-maskable interrupt. When a watchdog timer interrupt request is accepted, the processor interrupt priority level (IPL) is set to "111_2."

Table 10.2.1 Occurrence interval of watchdog timer interrupt request

Watchdog timer's count source	Occurrence interval of watchdog timer interrupt request		
	When system clock = 25 MHz (**Note 1**)	When system clock = 12 MHz (**Note 1**)	When system clock = 32 kHz (**Note 2**)
f_{512}	41.9 ms	87.4 ms	32768 ms
f_{32}	2.62 ms	5.46 ms	2048 ms

Clocks f_{32}, f_{512}, and system clock: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Notes 1: This is applied when the system clock selection bit (bit 3 at address $6C_{16}$; Refer to **Figure 10.2.1.**) = "0" and the main clock division selection bit (bit 0 at address $6F_{16}$; Refer to **Figure 10.2.2.**) = "0."
2: This is applied when the port-Xc selection bit (bit 4 at address $6C_{16}$; Refer to **Figure 10.2.1.**) = "1" and the system clock selection bit = "1."

Make sure that dummy data must be written to address 60_{16} (Watchdog timer register) by software before the most significant bit of the watchdog timer becomes "0."
If writing to address 60_{16} is not performed because of a program runaway and the most significant bit of the watchdog timer becomes "0," a watchdog timer interrupt request occurs. This means that a program runaway has occurred.
When resetting the microcomputer after detecting a program runaway, write "1" to the software reset bit (bit 3 at address $5E_{16}$) in the watchdog timer interrupt routine. (Make sure that writing "1" to the software reset bit must be performed on the condition that the main clock is stably supplied.) (For details, refer to chapter **"13. RESET"** and section **"17.3 Watchdog timer."**)

EOL announced

WATCHDOG TIMER

10.2 Operation description

10.2.2 Operation in stop mode

In the stop mode, the watchdog timer stops operating. Immediately after the stop mode is terminated, the watchdog timer operates as follows.

(1) When stop mode is terminated by a hardware reset

Supply of internal clock ϕ starts immediately after the stop mode is terminated, and the microcomputer performs the "operation after reset." (Refer to chapter **"13. RESET."**) The watchdog timer frequency selection flag becomes "0," and the watchdog timer starts counting of the main clock*1 divided by 512 from "FFF_{16}."

Main clock*1: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

(2) When stop mode is terminated by an interrupt request generated

According to bit state listed in Table 10.2.2, the watchdog timer operates as "a" or "b" described below.

a. Supply of internal clock ϕ starts immediately after the stop mode is terminated, and the routine of the interrupt which is used to terminate the stop mode is executed. From "FFF_{16}," the watchdog timer restarts counting of a count source which was counted just before the **STP** instruction is executed **(Note 1)**.

b. Immediately after the stop mode is terminated, the watchdog timer starts counting of a count source **(Note 2)** from "FFF_{16}." Supply of internal clock ϕ starts when the watchdog timer's most significant bit becomes "0." (At this time, a watchdog timer interrupt request is not generated.)
When supply of internal clock ϕ starts, the microcomputer executes the routine of the interrupt which is used to terminate the stop mode. From "FFF_{16}," the watchdog timer restarts counting of a count source which was counted just before the **STP** instruction is executed **(Note 1)**.

Notes 1: Clock f_{32} or f_{512} is counted.
2: When the system clock selection bit = "0," clock f_{32} is counted. When the system clock selection bit = "1" and the port-Xc selection bit = "0," clock f_8 is counted.

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Table 10.2.2 Watchdog timer's operation and bit state related to oscillation circuit control

Bit state related to oscillation circuit control				Watchdog timer's operation
Port-Xc selection bit (Bit 4 at address $6C_{16}$)	System clock selection bit (Bit 3 at address $6C_{16}$)	Main clock external input selection bit (Bit 1 at address $6F_{16}$)	Sub clock external input selection bit (Bit 2 at address $6F_{16}$)	
0	0	0	0	b
			1	
		1	0	a
			1	
	1	0	0	b
			1	
		1	0	a
			1	
1	0	0	0	b
			1	
		1	0	a
			1	
	1	0	0	b
			1	a
		1	0	b
			1	a

Note: For each bit's function, refer to **Figures 10.2.1 and 10.2.2**. For the procedure of writing to the main clock external input selection bit and the sub clock external input selection bit, refer to **Figure 10.2.3.**

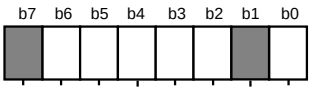
10.2.3 Operation in wait mode

When the system clock stop bit at wait state (bit 5 at address $6C_{16}$; Refer to **Figure 10.2.1.**) = "1," the watchdog timer stops operating in the wait mode. Furthermore, after the wait mode is terminated, the watchdog timer restarts counting from the same state as that before the watchdog timer stops.
When the system clock stop bit at wait state = "0," the watchdog timer does not stop.

EOL announced

10.2.4 Operation in hold state

The watchdog timer stops operating in the hold state. (Refer to section **"12.4 Hold function."**) When the hold state is terminated, the watchdog timer restarts counting from the same state as that before the watchdog timer stops.



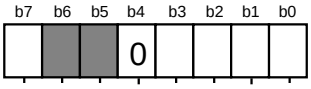
Oscillation circuit control register 0 (address $6C_{16}$)

Bit	Bit name	Functions	At reset	RW
0	X_{COUT} drivability selection bit	0: Drivability "LOW" 1: Drivability "HIGH"	1	RW (**Note 1**)
1	Not implemented.		Un-defined	—
2	Main clock stop bit	0: Main clock oscillation or external clock input is available. 1: Main clock oscillation or external clock input is stopped.	0	RW (**Note 1**)
3	System clock selection bit	When the port-Xc selection bit = "0," 0: Main clock 1: Main clock divided by 8 When the port-Xc selection bit = "1," 0: Main clock 1: Sub clock	0	RW (**Note 2**)
4	Port-Xc selection bit	0: Operate as I/O ports ($P7_7$, $P7_6$). 1: Operate as pins X_{CIN} and X_{COUT}.	0	RW (**Notes 2 and 3**)
5	System clock stop bit at wait state	0: Operates in the wait mode. 1: Stopped in the wait mode.	0	RW
6	Signal output disable selection bit	0: Output is enabled. (Refer to **Tables 12.1.2 and 12.1.5**) 1: Output is disabled.	0	RW
7	Not implemented.		Un-defined	—

Notes 1: Nothing can be written to this bit after reset. Writing to this bit is enabled when the port-Xc selection bit = "1."
2: When selecting the sub clock as the system clock, set bit 3 to "1" after setting bit 4 to "1." If the above settings are performed simultaneously, in other words, performed by executing only one instruction, only bit 3 is set to "1."
3: Although this bit can be set to "1," it cannot be cleared to "0" after this bit is once set to "1."
4: ☐ represents that bits 0 to 2 and bit 7 are not used for the watchdog timer.

EOL announced

Fig. 10.2.1 Structure of oscillation circuit control register 0



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin XCOUT. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 3)**	Ignored in the mask ROM and external ROM versions.		0	RW
	Must be fixed to "1" in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to "0" **(Note 2)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing "1" to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 10.2.3.
2: The case where data "01010101_2" is written with the procedure shown in Figure 10.2.3 is not included.
3: In the 7735 Group, fix this bit to "0."
4: ☐ represents that bits 3 to 7 are not used for the watchdog timer.

EOL announced

Fig. 10.2.2 Structure of oscillation circuit control register 1

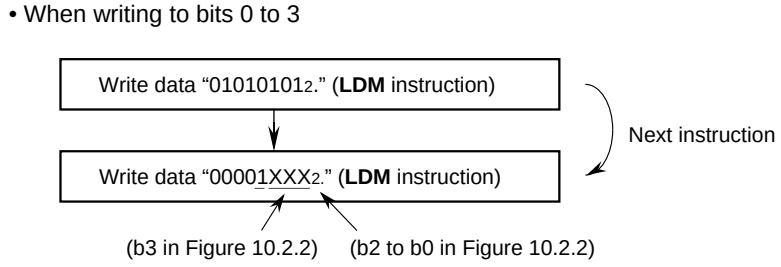


Fig. 10.2.3 Procedure for writing data to oscillation circuit control register 1

10.3 Precautions for watchdog timer

1. If dummy data is written to address 60_{16} when the data length flag (m) is "0," writing to address 61_{16} is simultaneously performed. Accordingly, when a change of the watchdog timer frequency selection flag's value (bit 0 at address 61_{16}) is not required, write the same value that is set.

2. In order to stop the watchdog timer in the hold state, the count source which is actually counted by the watchdog timer is the logical product of two signals. One is the inverted signal input from pin $\overline{\text{HOLD}}$, and the other is a count source which is selected by the watchdog timer frequency selection flag (clock f_{32} or f_{512}). (Refer to **Figure 10.1.1.**) Accordingly, there is a possibility that counting is performed when pin $\overline{\text{HOLD}}$'s input signal level changes during a duration which is shorter than 1 cycle of the selected count source (clock f_{32} or f_{512}).

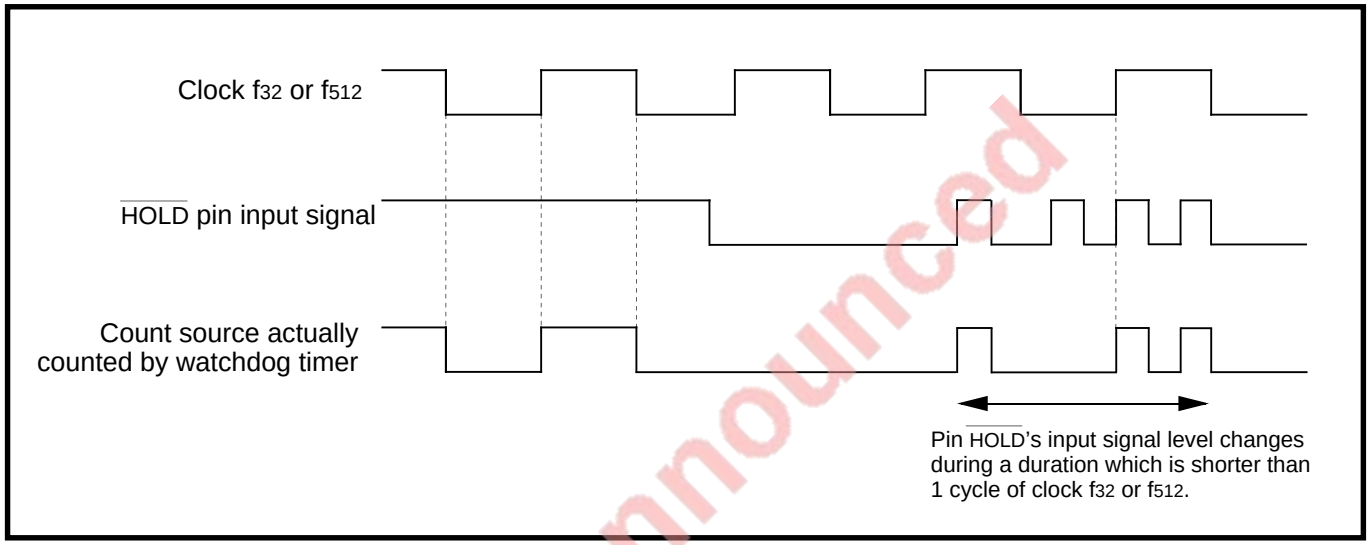


Fig. 10.3.1 Watchdog timer's count source

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3. When the main clock is not stably supplied, do not use the software reset (that is, writing "1" to the software reset bit) as a means to reset the microcomputer at a program runaway.

4. When the **STP** instruction (Refer to chapter **"11. STOP AND WAIT MODES"**) is executed, the watchdog timer stops operating. For the system where the watchdog timer is used to detect a program runaway, select "**STP** instruction disabled" with "**STP** instruction option" on "MASK ROM ORDER CONFIRMATION FORM."

CHAPTER 11

STOP AND WAIT MODES

11.1 Overview
11.2 Clock generating circuit
11.3 Stop mode
11.4 Wait mode

EOL announced

STOP AND WAIT MODES

11.1 Overview

The stop and wait modes are described below.
When there is no need for operation of the central processing unit (CPU), the stop and wait modes are used to stop oscillation or internal clock ϕ. The microcomputer enters the stop mode when the **STP** instruction is executed; the microcomputer enters the wait mode when the **WIT** instruction is executed.

11.1 Overview

Table 11.1.1 lists the differences between the stop and wait modes.
The stop state of oscillation or internal clock ϕ can be terminated by an interrupt request occurrence or hardware reset.

Table 11.1.1 Differences between stop and wait modes

<table>
<tr><td colspan="2" rowspan="2">Item</td><td colspan="4">State/Operation</td></tr>
<tr><td colspan="2">Stop mode</td><td colspan="2">Wait mode</td></tr>
<tr><td rowspan="4">State in each mode</td><td>Oscillation</td><td colspan="2" rowspan="4">Stopped</td><td colspan="2">Operating (Note 1)</td></tr>
<tr><td>Internal clock ϕ</td><td colspan="2">Stopped</td></tr>
<tr><td>Clock timer*1</td><td colspan="2">Operating</td></tr>
<tr><td>Clocks f2 to f512, clock ϕ1*2</td><td>Stopped</td><td>Operating</td></tr>
<tr><td rowspan="2">Operation after each mode is terminated</td><td>When terminated by interrupt request occurrence</td><td>Supply of internal clock ϕ starts after measuring a certain time by watchdog timer.</td><td>Supply of internal clock ϕ starts after f2 x 7 cycles.</td><td colspan="2">Supply of internal clock ϕ starts immediately after termination of the wait mode.</td></tr>
<tr><td>When terminated by hardware reset</td><td colspan="4">Operation after hardware reset</td></tr>
<tr><td rowspan="4">Features</td><td>Current consumption</td><td colspan="2">Less than that in the wait mode</td><td>Less than that when clocks f2 to f512 operate</td><td>Less than that when CPU operates</td></tr>
<tr><td>Internal peripheral devices</td><td colspan="3">Functions using the external clock are enabled.
Functions using clocks f2 to f512 are disabled.</td><td>Operating enabled</td></tr>
<tr><td>Interval from termination of each mode until execution of instruction</td><td>Long</td><td colspan="3">Short</td></tr>
<tr><td>Condition</td><td>———</td><td>From the external, a clock must stably be input to a clock input pin (Note 2).</td><td colspan="2">———————————</td></tr>
</table>

Clock timer*1 : Refer to section **"7.6 Clock timer."**
Clocks f2 to f512, clock ϕ1*2 : Refer to **Figure 11.2.1.**

Note 1: When the main clock external input selection bit = "1," the main-clock oscillation circuit stops operating; when the sub clock external input selection bit = "1," the sub-clock oscillation circuit stops operating. (Note that, in this case, an external clock can be input.)
2: When the main clock is the system clock, pin XIN is used; when the sub clock is the system clock, pin XCIN is used.

EOL announced

11.2 Clock generating circuit

Figure 11.2.1 shows the block diagram of the clock generating circuit (with the **STP** and **WIT** instructions). Figures 11.2.2 and 11.2.3 show the structures of the oscillation circuit control register 0 and oscillation circuit control register 1, respectively.

Figure 11.2.4 shows the procedure for writing data to the oscillation circuit control register 1.

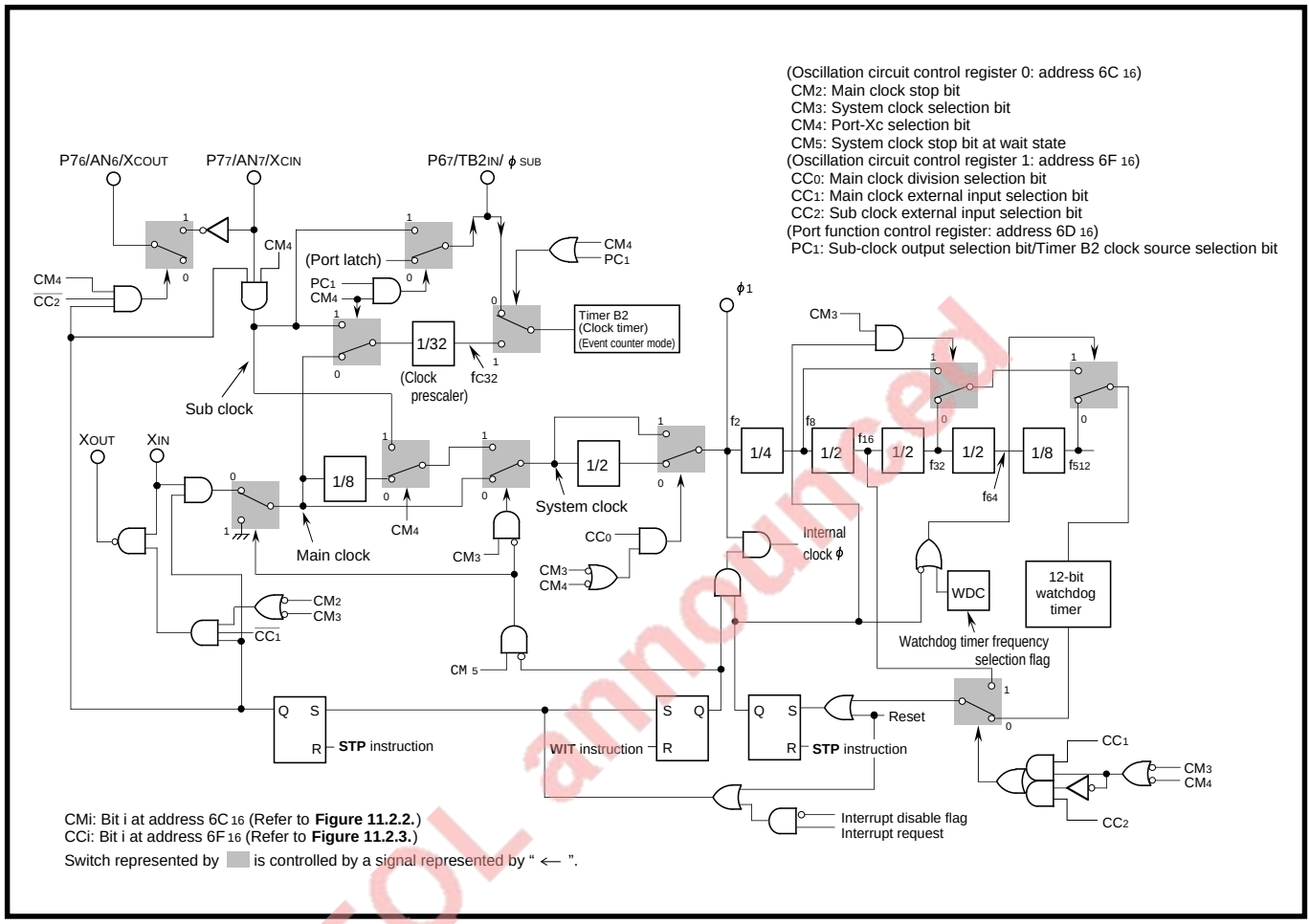
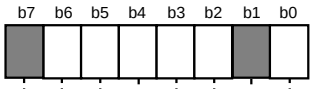


Fig. 11.2.1 Block diagram of clock generating circuit (with STP and WIT instructions)

EOL announced

11.2 Clock generating circuit



Oscillation circuit control register 0 (address 6C 16)

Bit	Bit name	Functions	At reset	RW
0	XCOUT drivability selection bit	0: Drivability "LOW" 1: Drivability "HIGH"	1	RW (**Note 1**)
1	Not implemented.		Un-defined	–
2	Main clock stop bit	0: Main clock oscillation or external clock input is available. 1: Main clock oscillation or external clock input is stopped.	0	RW (**Note 1**)
3	System clock selection bit	When the port-Xc selection bit = "0," 0: Main clock 1: Main clock divided by 8 When the port-Xc selection bit = "1," 0: Main clock 1: Sub clock	0	RW (**Note 2**)
4	Port-Xc selection bit	0: Operate as I/O ports (P77, P76). 1: Operate as pins XCIN and XCOUT.	0	RW (**Notes 2 and 3**)
5	System clock stop bit at wait state **(Note 4)**	0: Operates in the wait mode. 1: Stopped in the wait mode.	0	RW
6	Signal output disable selection bit	0: Output is enabled. (Refer to **Tables 12.1.2 and 12.1.5**) 1: Output is disabled.	0	RW
7	Not implemented.		Un-defined	–

Notes 1: Nothing can be written to this bit after reset. Writing to this bit is enabled when the port-Xc selection bit = "1."

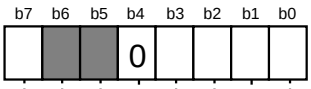
2: When selecting the sub clock as the system clock, set bit 3 to "1" after setting bit 4 to "1." If the above settings are performed simultaneously, in other words, performed by executing only one instruction, only bit 3 is set to "1."

3: Although this bit can be set to "1," it cannot be cleared to "0" after this bit is once set to "1."

4: When setting the system clock stop bit at wait state to "1," perform it immediately before the **WIT** instruction is executed. Furthermore, clear this bit to "0" immediately after the wait mode is terminated.

Announced

Fig. 11.2.2 Structure of oscillation circuit control register 0



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 3)**	Ignored in the mask ROM and external ROM versions.		0	RW
	Must be fixed to "1" in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to "0" **(Note 2)**		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing "1" to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 11.2.4.
2: The case where data "01010101_2" is written with the procedure shown in Figure 11.2.4 is not included.
3: In the 7735 Group, fix this bit to "0."
4: ▨ represents that bits 3 to 7 are not used for the stop and wait modes.

EOL announced

Fig. 11.2.3 Structure of oscillation circuit control register 1

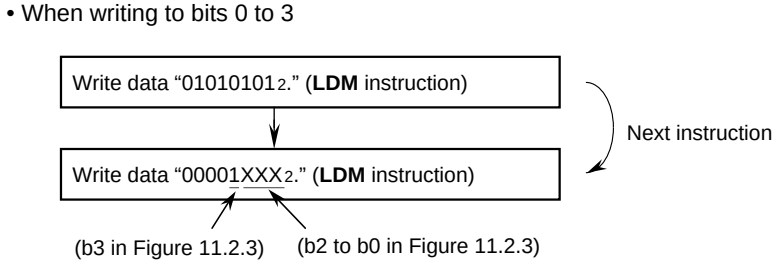


Fig. 11.2.4 Procedure for writing data to oscillation circuit control register 1

11.3 Stop mode

When the **STP** instruction is executed, the main-clock and sub-clock oscillation circuits stop operating. This state is called “stop mode.”

In the stop mode, even when oscillation stops, the contents of the internal RAM can be retained if there is 2 V of Vcc (power source voltage) or more. Furthermore, because the CPU and all internal peripheral devices which use clocks f_2 to f_{512}[*1] stop operating, power consumption is lowered. Refer to section **“17.4 Power saving”** for lowering the power consumption.

Table 11.3.1 lists the microcomputer’s state/operation in the stop mode and after the stop mode is terminated. Table 11.3.2 lists the pin state in the stop mode.

Table 11.3.1 Microcomputer’s state/operation in stop mode and after stop mode is terminated

Item				State/Operation	
				Watchdog timer is used when terminating the stop mode	Watchdog timer is not used when terminating the stop mode
State in stop mode	Oscillation			Stopped	
	Internal clock ϕ				
	Clocks f_2 to f_{512}[*1], clock ϕ_1[*2]				
	Internal peripheral devices	Clock timer[*3]	f(XIN)/32	Stopped	
			f(XCIN)/32		
		Timer A, Timer B		Operating enabled only in the event counter mode	
		Serial I/O		Operating enabled only when the external clock is selected	
		A-D converter		Stopped	
		Watchdog timer		Stopped	
		Pins		Refer to **Table 11.3.2**	
Operation after stop mode is terminated	When terminated by interrupt request occurrence			Supply of internal clock ϕ starts after measuring a certain time by watchdog timer.	Supply of internal clock ϕ starts after f_2 x 7 cycles.
	When terminated by hardware reset			Operation after hardware reset	
Condition				———	From the external, a clock must stably be input to a clock input pin[*4].

Clocks f_2 to f_{512}[*1], clock ϕ_1[*2] : Refer to **Figure 11.2.1.**

Clock timer[*3] : Refer to section **“7.6 Clock timer.”**

Clock input pin[*4] : When the system clock is the main clock, pin XIN is used; when the system clock is the sub clock, pin XCIN is used.

❋ In order to select whether to use the watchdog timer or not when terminating the stop mode, specify the main clock external input selection bit (bit 1 at address $6F_{16}$; when the main clock is used) or the sub clock external input selection bit (bit 2 at address $6F_{16}$; when the sub clock is used).

(Refer to **Figure 11.2.3,** sections **“11.3.2 Stop mode terminating operation by interrupt request occurrence (when using watchdog timer)”** and **“11.3.3 Stop mode terminating operation by interrupt request occurrence (when not using watchdog timer).”**

EOL announced

Table 11.3.2 Pin state in stop mode

Pins	State			
	Single-chip mode	Memory expansion mode	Microprocessor mode	
			When the standby state selection bit*1 = "0"	When the standby state selection bit*1 = "1"
$\overline{E}$	■ When the signal output disable selection bit = "0," "H" level is output ■ When the signal output disable selection bit = "1," "L" level is output.	Same as in the microprocessor mode	"H" level is output.	■ When the signal output disable selection bit = "0," "H" level is output. ■ When the signal output disable selection bit = "1," "L" level is output.
R/$\overline{W}$, $\overline{BHE}$, $\overline{HLDA}$				Output levels can be set. (Refer to section **"11.3.1 Output levels of external bus and bus control signals in stop mode."**)
ALE			"L" level is output.	
A_0–A_7, A_8/D_8–A_{15}/D_{15}, A_{16}/D_0–A_{23}/D_7			Retains the same state in which the **STP** instruction is executed.	
$P4_2/\phi_1$	■ When the clock ϕ_1 output selection bit*2 = "1" ϕ_1: "L" level is output. ■ When the clock ϕ_1 output selection bit = "0" $P4_2$: Retains the same state in which the **STP** instruction is executed.		■ When the signal output disable selection bit*3 = "0" ϕ_1: "L" level is output. ■ When the signal output disable selection bit = "1" $P4_2$: Bit 2's value of the port P4 register is output **(Note)**.	
Ports	P0 to P8 (not including $P4_2$) : Retains the same state in which the **STP** instruction is executed.	$P4_3$ to $P4_7$, P5 to P8 :Retains the same state in which the **STP** instruction is executed.		

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Standby state selection bit*1: Bit 0 at address $6D_{16}$ (Refer to **Figure 11.3.1.**)
Clock ϕ_1 output selection bit*2: Bit 7 at address $5E_{16}$
(Refer to section **"12.1 Signals required for accessing external devices."**)
Signal output disable selection bit*3: Bit 6 at address $6C_{16}$
(Refer to section **"12.1 Signals required for accessing external devices."**)

Note: Make sure to set bit 2 of the port P4 direction register to "1."

11.3.1 Output levels of external bus and bus control signals in stop mode

In the memory expansion or microprocessor mode, the output levels of the external bus and bus control signals in the stop mode can be set by software. By setting the standby state selection bit (bit 0 at address $6D_{16}$) to "1," these output levels become levels set by software. Figure 11.3.1 shows an output level setting example in the stop mode.
In the single-chip mode, do not set the standby state selection bit to "1."

11.3 Stop mode

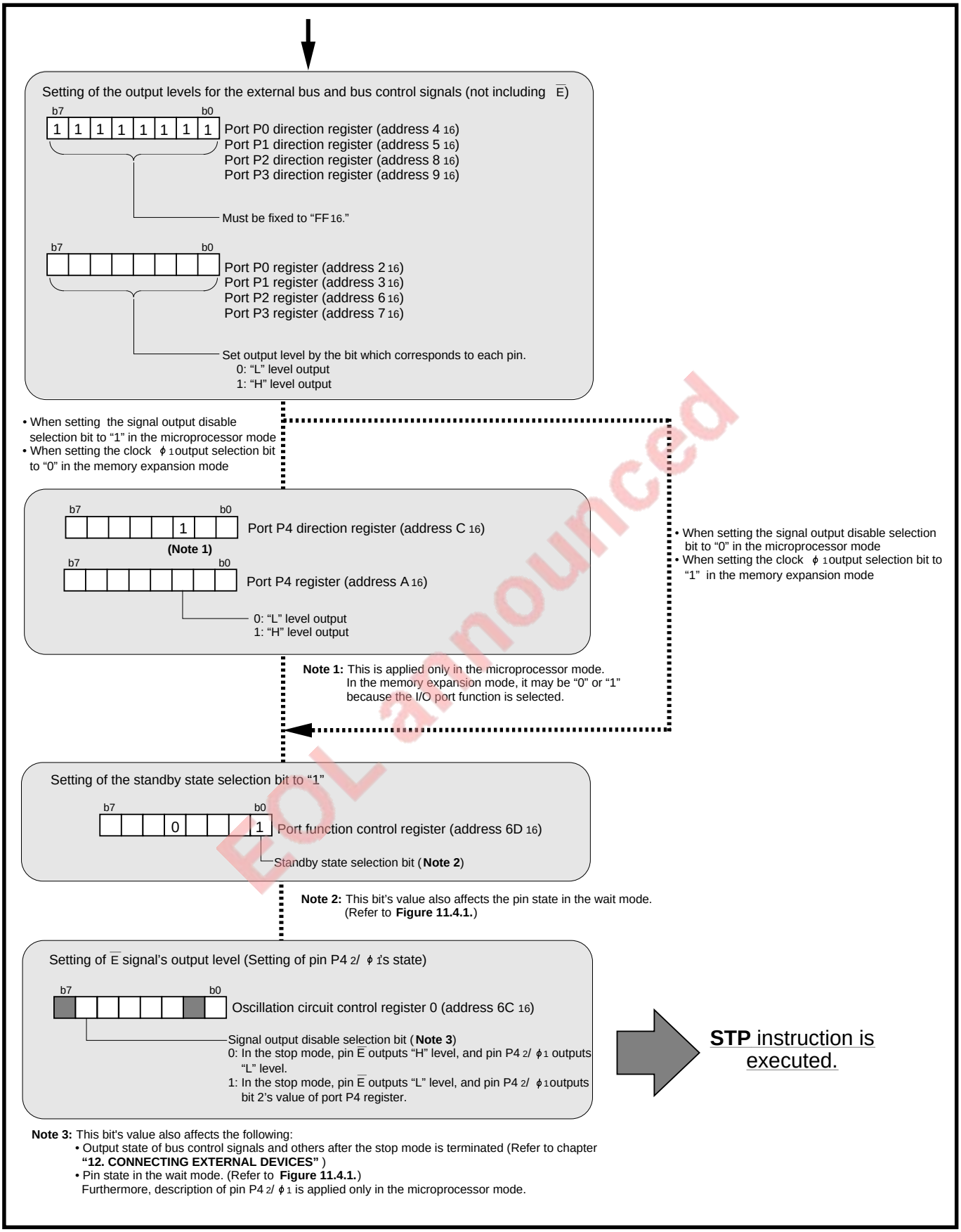


Fig. 11.3.1 Output level setting example in stop mode (Memory expansion or Microprocessor mode)

EOL announced

11.3.2 Stop mode terminating operation by interrupt request occurrence (when using watchdog timer)
When there is little possibility that a clock is stably supplied from an oscillation circuit **(Note 1)** in returning from the stop mode, instruction execution can be started after a certain time **(Note 2)** measured by the watchdog timer.

Notes 1: A clock is supplied in one of the following ways:
- An oscillation circuit operates by itself.
- An external clock is input.

2: "a certain time" means an interval from occurrence of an interrupt request until stabilization of clock supply.

① When an interrupt request occurs, an oscillator starts oscillating. Simultaneously, supply of clocks f_2 to f_{512} starts.
② By start of oscillation, the watchdog timer starts counting. The watchdog timer counts f_{32} when the system clock selection bit (bit 3 at address $6C_{16}$; Refer to **Figure 11.2.2.**) = "0" or f_8 when the system clock selection bit = "1."
③ When the watchdog timer's MSB becomes "0," supply of internal clock ϕ starts. At the same time, the watchdog timer's count source returns to a count source (clock f_{32} or f_{512}) which is selected by the watchdog timer frequency selection flag (bit 0 at address 61_{16}).
④ The interrupt request which occurs in ① is accepted.

Table 11.3.3 lists interrupts which can be used for termination of the stop mode.

Table 11.3.3 Interrupts which can be used for termination of stop mode

Interrupt	Conditions for each function which generates interrupt request
Key input interrupt	When the key input interrupt function is selected
$\overline{INT_i}$ interrupt (i = 0 to 2)	$\overline{INT_2}$ interrupt: When the key input interrupt function is invalid.
Timer Ai interrupt (i = 0 to 4)	In the event counter mode
Timer Bi interrupt (i = 0 to 2)	
UARTi transmission interrupt (i = 0, 1)	When the external clock is selected
UARTi reception interrupt (i = 0, 1)	
UART2 transmission/reception interrupt	

Note 1: Because an oscillator has stopped oscillating, each function is available only in the conditions listed in Table 11.3.3. Note that the A-D converter and clock timer (Refer to section **"7.6 Clock timer"**) do not operate, also.

2: Because an oscillator has stopped oscillating, interrupts not listed in Table 11.3.3 cannot be used.

3: For each interrupt, refer to chapters **"4. INTERRUPTS," "5. KEY INPUT INTERRUPT FUNCTION," "6. TIMER A," "7. TIMER B,"** and **"8. SERIAL I/O."**

EOL announced

11.3 Stop mode

When using the watchdog timer in termination of the stop mode, make sure to set as follows before executing the **STP** instruction.

■ Enable an interrupt which is used for termination.
Also, make sure that the interrupt priority level of an interrupt which is used for termination is higher than the processor interrupt priority level (IPL) of a routine where the **STP** instruction is executed. Furthermore, when multiple interrupts in Table 11.3.3 are enabled, the stop mode is terminated by the interrupt request which occurs first.
After oscillation starts (①), there is a possibility that an interrupt request occurs until the supply of internal clock ϕ starts (③). Interrupt requests which occur during this period are accepted in order of priority after the watchdog timer's MSB becomes "0." For interrupts which have no need to be accepted, set their interrupt priority levels to "0" (Interrupt disabled) before executing the **STP** instruction.

■ When the system clock is the main clock or the main clock divided by 8, set the main clock external input selection bit (bit 1 at address $6F_{16}$; Refer to **Figure 11.2.3.**) to "0." When the system clock is the sub clock, set the sub clock external input selection bit (bit 2 at address $6F_{16}$) to "0."

11.3.3 Stop mode terminating operation by interrupt request occurrence (when not using watchdog timer)
When a clock is stably input from the external to a clock input pin (Refer to **Figures 14.2.2 and 14.2.4.**), instruction execution can be started immediately after the termination of the stop mode.

① When an interrupt request occurs, clock input from pin X_{IN} starts. Simultaneously, supply of clocks f_2 to f_{512} starts.
② Supply of internal clock ϕ starts after 7 cycles of f_2.
③ The interrupt request which occurs in ① is accepted.

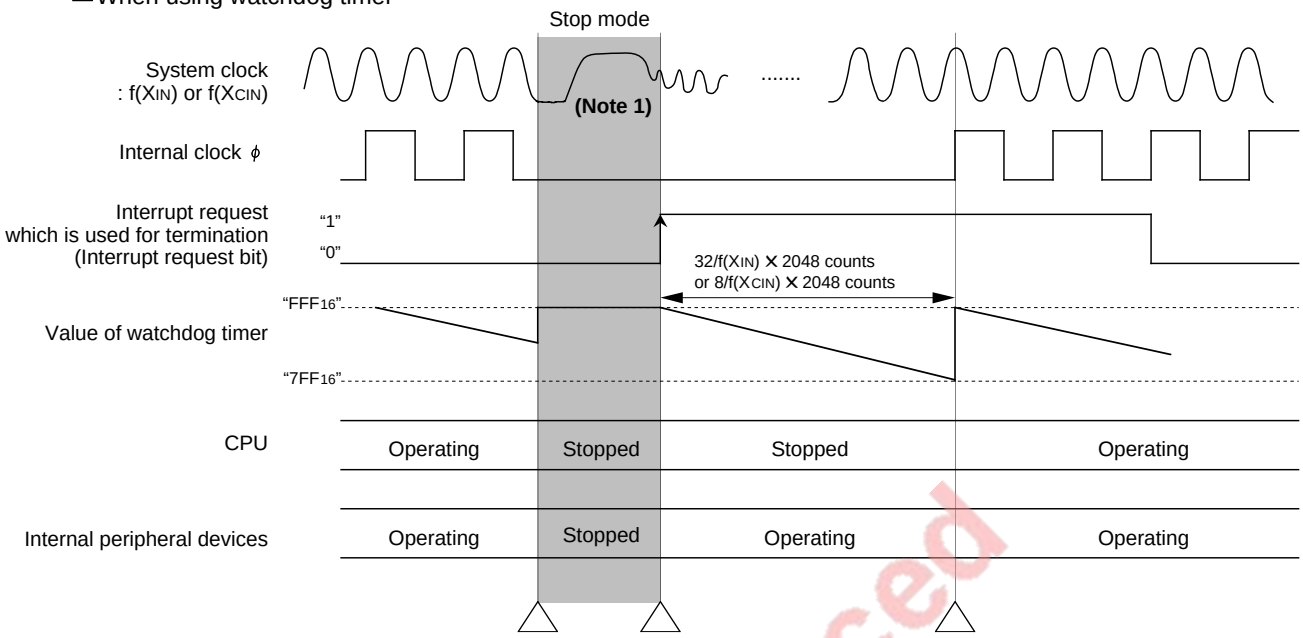
Table 11.3.3 lists interrupts which can be used for termination.
When not using the watchdog timer in termination of the stop mode, make sure to set as follows before executing the **STP** instruction.

■ Enable an interrupt which is used for termination.
Also, make sure that the interrupt priority level of an interrupt which is used for termination is higher than the processor interrupt priority level (IPL) of a routine where the **STP** instruction is executed. Furthermore, when multiple interrupts in Table 11.3.3 are enabled, the stop mode is terminated by the interrupt request which occurs first.

■ When the system clock is the main clock or the main clock divided by 8, set the main clock external input selection bit (bit 1 at address $6F_{16}$; Refer to **Figure 11.2.3.**) to "1." When the system clock is the sub clock, set the sub clock external input selection bit (bit 2 at address $6F_{16}$) to "1."

EOL announced

■When using watchdog timer



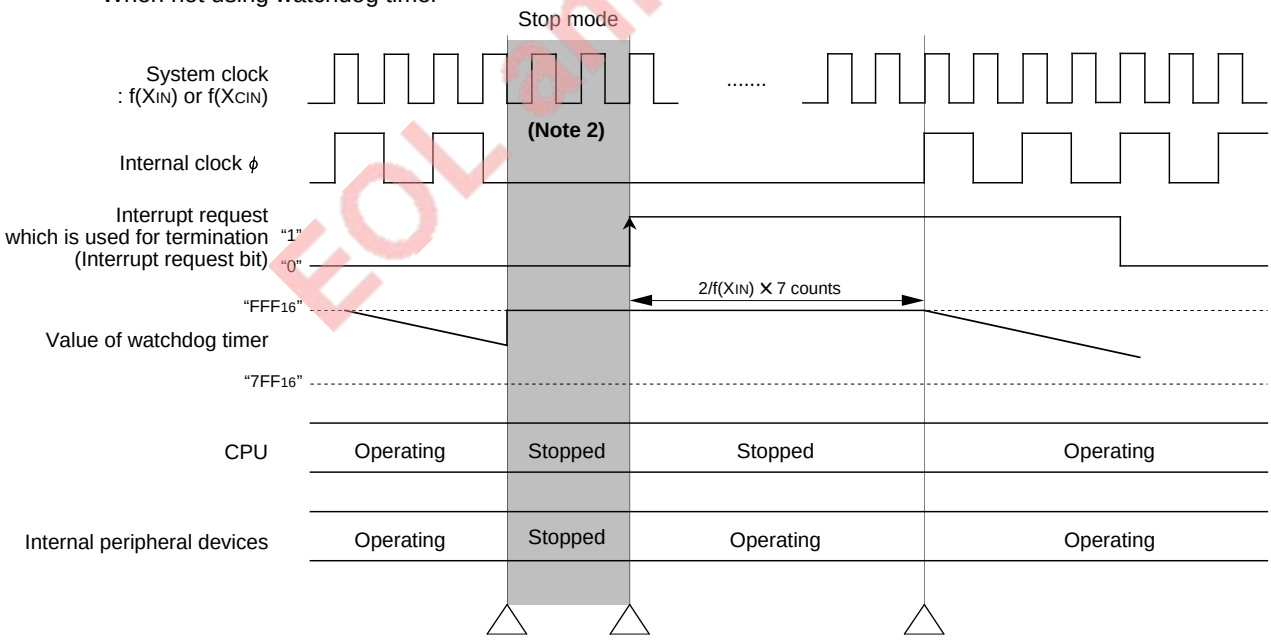
●**STP** instruction is executed

●Interrupt request which is used for termination occurs.
●Oscillation starts. (When an external clock is input from pin XIN, clock input starts.)
●Watchdog timer starts counting.

●Watchdog timer's MSB = "0" (However, watchdog timer interrupt request does not occur.)
●Supply of ϕ CPU (internal clock ϕ) starts.
●Interrupt request which was used for termination is accepted.

Note 1: Sub clock (f(XCIN)) is stopped at "L" level in the stop mode.

■When not using watchdog timer



●**STP** instruction is executed

●Interrupt request which is used for termination occurs.
●Clock input from pin XIN or XCIN starts.

●Watchdog timer starts counting.
●Supply of ϕ CPU (internal clock ϕ) starts.
●Interrupt request which was used for termination is accepted.

Note 2: In the stop mode, clock input can be stopped.
In order to stop clock input, be sure to generate an interrupt request after a clock is stably supplied when returning from the stop mode.

Fig. 11.3.2 Stop mode terminating sequence by interrupt request occurrence

EOL announced

11.3 Stop mode

11.3.4 Stop mode terminating operation by hardware reset

When terminating the stop mode by hardware reset, input "L" level to pin $\overline{\text{RESET}}$ from the external circuit until oscillation of an oscillator which is connected to the main-clock oscillation circuit is stabilized.
The CPU and SFR area are initialized in the same way as at system reset. However, the internal RAM area retains the same contents as that before the **STP** instruction was executed. The terminating sequence is the same as the internal processing sequence after reset.
When determining whether hardware reset was applied for termination of the stop mode or system reset was applied, use software after reset.
For reset, refer to chapter **"13. RESET."**

11.3.5 Precautions for stop mode

1. In the mask ROM version, select "**STP** instruction enabled" with "**STP** instruction option" on "MASK ROM ORDER CONFIRMATION FORM." (In the built-in PROM and external ROM versions, **STP** instruction is always enabled.)

2. "Stop mode terminating operation by an interrupt request occurrence (when not using watchdog timer)" can be selected only when an external clock is stably input to a clock input pin for a clock which is selected as the system clock.
   In one of the following cases, select "Stop mode terminating operation by an interrupt request occurrence (when using watchdog timer)":
   - When an oscillator is connected between input and output pins for a clock which is selected as the system clock
   - When there is a possibility that the above external clock is temporarily unstable in termination of the stop mode

EOL announced

11.4 Wait mode

When the **WIT** instruction is executed, internal clock ϕ stops. (The oscillator does not stop oscillating.) This state is called "wait mode."
In the wait mode, power consumption can be lowered with Vcc (power source voltage) retained. Refer to section **"17.4 Power saving"** for lowering the power consumption.
Table 11.4.1 lists the microcomputer's state/operation in the wait mode and after the wait mode is terminated. Table 11.4.2 lists the pin state in the wait mode.

Table 11.4.1 Microcomputer's state/operation in wait mode and after wait mode is terminated

Item				State/Operation	
				When clocks f_2 to f_{512} are stopped	When clocks f_2 to f_{512} are not stopped
State in wait mode	Oscillation			Operating	
	Internal clock ϕ			Stopped	
	Clocks f_2 to f_{512}[*1], clock ϕ_1[*2]			Stopped	Operating
	Internal peripheral devices	Clock timer[*3]	f(XIN)/32	Stopped	Operating
			f(XCIN)/32	Operating	
		Timer A, Timer B		Operating enabled only in the event counter mode.	Operating
		Serial I/O		Operating enabled only when the external clock is selected.	Operating
		A-D converter		Stopped	Operating
		Watchdog timer		Stopped	Operating
		Pins		Refer to **Table 11.4.2.**	
Operation after wait mode is terminated	When terminated by interrupt request occurrence			Supply of internal clock ϕ starts immediately after termination.	
	When terminated by hardware reset			Operation after hardware reset	

Clocks f_2 to f_{512}[*1], clock ϕ_1[*2]: Refer to **Figure 11.2.1.**

Clock timer[*3]: Refer to section **"7.6 Clock timer."**

❋ In order to select the state of clocks f_2 to f_{512} in the wait mode, specify the system clock stop bit at wait state (bit 5 at address $6C_{16}$). (Refer to **Figure 11.2.2** and section **"11.4.1 State of clocks f_2 to f_{512} in wait mode."**)

EOL announced

STOP AND WAIT MODES

11.4 Wait mode

Table 11.4.2 Pin state in wait mode

<table>
<tr><th rowspan="3">Pins</th><th colspan="4">State</th></tr>
<tr><th rowspan="2">Single-chip mode</th><th rowspan="2">Memory expansion mode</th><th colspan="2">Microprocessor mode</th></tr>
<tr><th>When the standby state selection bit*1 = “0”</th><th>When the standby state selection bit*1 = “1”</th></tr>
<tr><td>$\overline{E}$</td><td>■ When the signal output disable selection bit = “0,” “H” level is output.
■ When the signal output disable selection bit = “1,” “L” level is output.</td><td>Same as in the microprocessor mode</td><td>“H” level is output.</td><td>■ When the signal output disable selection bit = “0,” “H” level is output.
■ When the signal output disable selection bit = “1,” “L” level is output.</td></tr>
<tr><td>R/$\overline{W}$,
$\overline{BHE}$,
$\overline{HLDA}$</td><td rowspan="3"></td><td rowspan="3"></td><td rowspan="2"></td><td rowspan="3">Output levels can be set. (Refer to section “11.4.2 Output levels of external bus and bus control signals in wait mode”)</td></tr>
<tr><td>ALE</td><td>“L” level is output.</td></tr>
<tr><td>A0–A7,
A8/D8–A15/D15,
A16/D0–A23/D7</td><td>Retains the same state in which the WIT instruction is executed.</td></tr>
<tr><td>P42/ϕ1</td><td colspan="3">■ When the clock ϕ1 output selection bit*2 = “1”
ϕ1: Operating when the system clock stop bit at wait state*4 = “0.”
“L” level is output when the system clock stop bit at wait state = “1.”
■ When the clock ϕ1 output selection bit = “0”
P42: Retains the same state in which the WIT instruction is executed.</td><td>■ When the signal output disable selection bit*3 = “0”
ϕ1: Operating when the system clock stop bit at wait state = “0.”
“L” level is output when the system clock stop bit at wait state = “1.”
■ When the signal output disable selection bit = “1”
P42: Bit 2’s value of port P4 register is output (Note).</td></tr>
<tr><td>Ports</td><td colspan="2">P0 to P8 (not including P42) : Retains the same state in which the WIT instruction is executed.</td><td colspan="2">P43 to P47, P5 to P8 : Retains the same state in which the WIT instruction is executed.</td></tr>
</table>

Standby state selection bit*1: Bit 0 at address 6D16 (Refer to **Figure 11.4.1.**)
Clock ϕ1 output selection bit*2: Bit 7 at address 5E16
(Refer to section **“12.1 Signals required for accessing external devices.”**)
Signal output disable selection bit*3: Bit 6 at address 6C16
(Refer to section **“12.1 Signals required for accessing external devices.”**)
System clock stop bit at wait state*4: Bit 5 at address 6C16
(Refer to section **“11.4.1 State of clocks f2 to f512 in wait mode.”**)

Note: Make sure to set bit 2 of the port P4 direction register to “1.”

EOL announced

11.4.1 State of clocks f_2 to f_{512} in wait mode

The state of clocks f_2 to f_{512} in the wait mode can be selected by the system clock stop bit at wait state (bit 5 at address $6C_{16}$: Refer to **Figure 11.2.2**.). When supply of clocks f_2 to f_{512} is stopped in the wait mode, power consumption can further be lowered.

When supply of clocks f_2 to f_{512} is stopped, internal peripheral devices which use clocks f_2 to f_{512} stop operating as in the stop mode. Furthermore, when pin $P4_2/\phi_1$ functions as a clock ϕ_1 output pin, this pin outputs "L" level. (Refer to **Table 11.4.2.**)

When supply of clocks f_2 to f_{512} is not stopped, both of the internal peripheral devices' operation and clock ϕ_1 output do not stop. Note that, in the microprocessor mode, clock ϕ_1 output stops when the signal output disable selection bit = "1."

In both cases, internal clock ϕ stops, so that the CPU does not operate. Furthermore, because clock fc_{32} does not stop operating, the clock timer continues operating. (Refer to **Table 11.4.3.**)

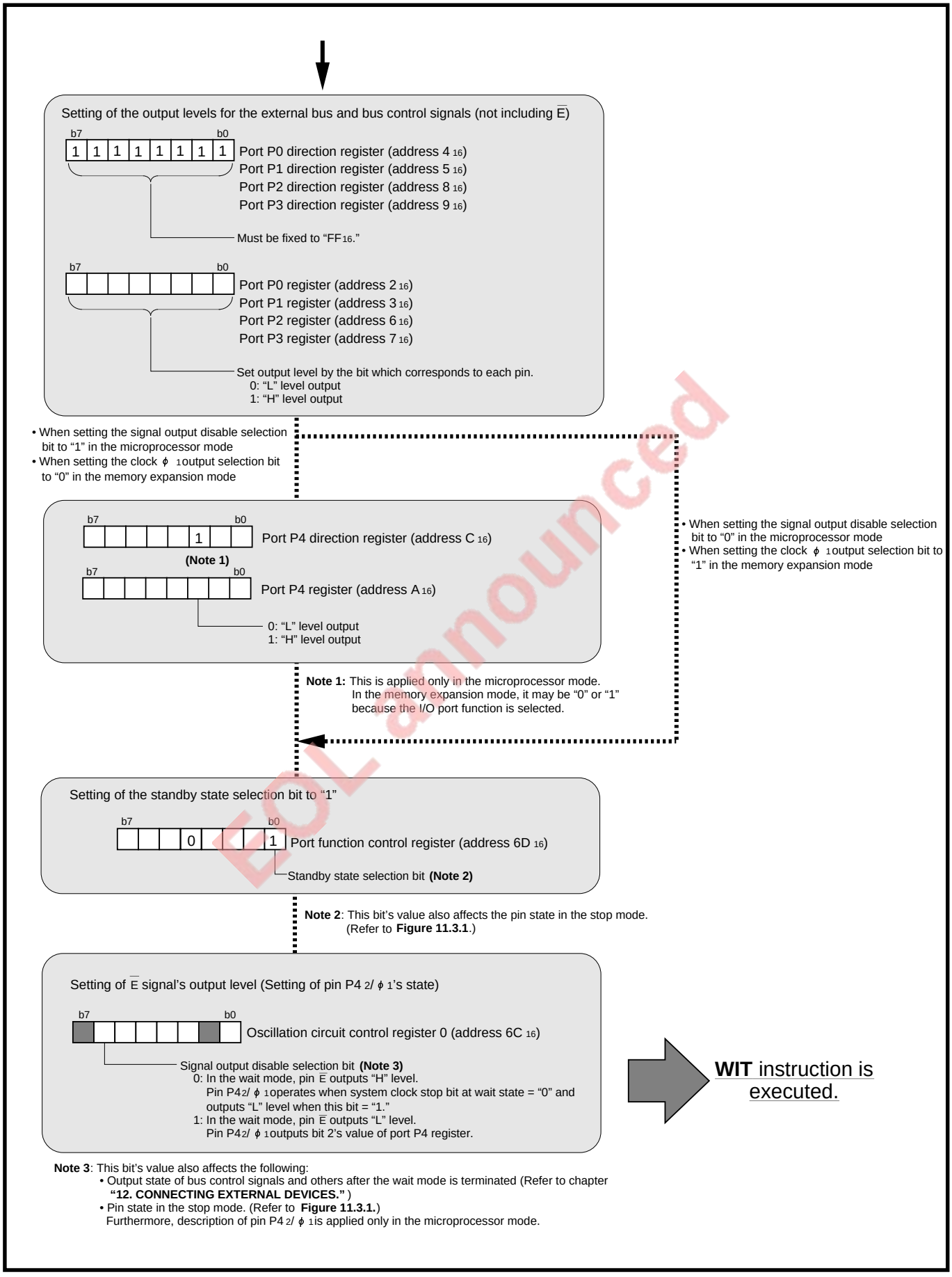
11.4.2 Output levels of external bus and bus control signals in wait mode

In the memory expansion or microprocessor mode, the output levels of the external bus and bus control signals in the wait mode can be set by software. By setting the standby state selection bit (bit 0 at address $6D_{16}$) to "1," these output levels become levels set by software. Figure 11.4.1 shows an output level setting example in the wait mode.

In the single-chip mode, do not set the standby state selection bit to "1." (Fix this bit to "0.")

EOL announced

11.4 Wait mode



EOL announced

Fig. 11.4.1 Output level setting example in wait mode (Memory expansion or Microprocessor mode)

11.4.3 Wait mode terminating operation by interrupt request occurrence

① When an interrupt request occurs with supply of clocks f_2 to f_{512} stopped, the clock supply restarts.
② Supply of internal clock ϕ starts.
③ The interrupt request which occurs in ① is accepted.

An interrupt which can be used for termination depends on the state of clocks f_2 to f_{512} in the wait mode. (Refer to **Table 11.4.3.**)

Table 11.4.3 Interrupts which can be used for termination of wait mode

Interrupt		Conditions for each function which generates interrupt request	
		When clocks f_2 to f_{512} are stopped	When clocks f_2 to f_{512} are not stopped
Key input interrupt		When the key input interrupt function is selected	
$\overline{INT_i}$ interrupt (i = 0 to 2)		$\overline{INT_2}$ interrupt: When the key input interrupt function is invalid.	
Timer Ai interrupt (i = 0 to 4)		In the event counter mode	Enabled in all modes
Timer Bi interrupt (i = 0 to 2)			
UARTi transmission interrupt (i = 0 to 2)		Enabled only when the external clock is selected	Always enabled
UARTi reception interrupt (i = 0 to 2)			
Clock timer*	$f(X_{IN})/32$	Disabled	
(timer B2) interrupt	$f(X_{CIN})/32$	When timer B2 functions as the clock timer	
A-D conversion interrupt		Disabled	Enabled in one-shot mode and single sweep mode

Clock timer*: Refer to section **"7.6 Clock timer."**

❋ For each interrupt, refer to chapters **"4. INTERRUPTS," "5. KEY INPUT INTERRUPT FUNCTION," "6. TIMER A," "7. TIMER B," "8. SERIAL I/O,"** and **"9. A-D CONVERTER."**

Before executing the **WIT** instruction, be sure to enable an interrupt which is used for termination. Also make sure that the interrupt priority level of an interrupt which is used for termination is higher than the processor interrupt priority level (IPL) of a routine where the **WIT** instruction is executed. Furthermore, when multiple interrupts in Table 11.4.3 are enabled, the wait mode is terminated by the interrupt request which occurs first.

11.4.4 Wait mode terminating operation by hardware reset

The CPU and SFR area are initialized in the same way as at system reset. However, the internal RAM area retains the same contents as that before the **WIT** instruction was executed. The terminating sequence is the same as the internal processing sequence after reset.
When determining whether hardware reset was applied for termination of the wait mode or system reset was applied, use software after reset.
For reset, refer to chapter **"13. RESET."**

EOL announced

MEMO

EOL announced

CHAPTER 12

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices
12.2 Software wait
12.3 Ready function
12.4 Hold function

EOL announced

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

Functions and operations of signals required for accessing external devices are described below.

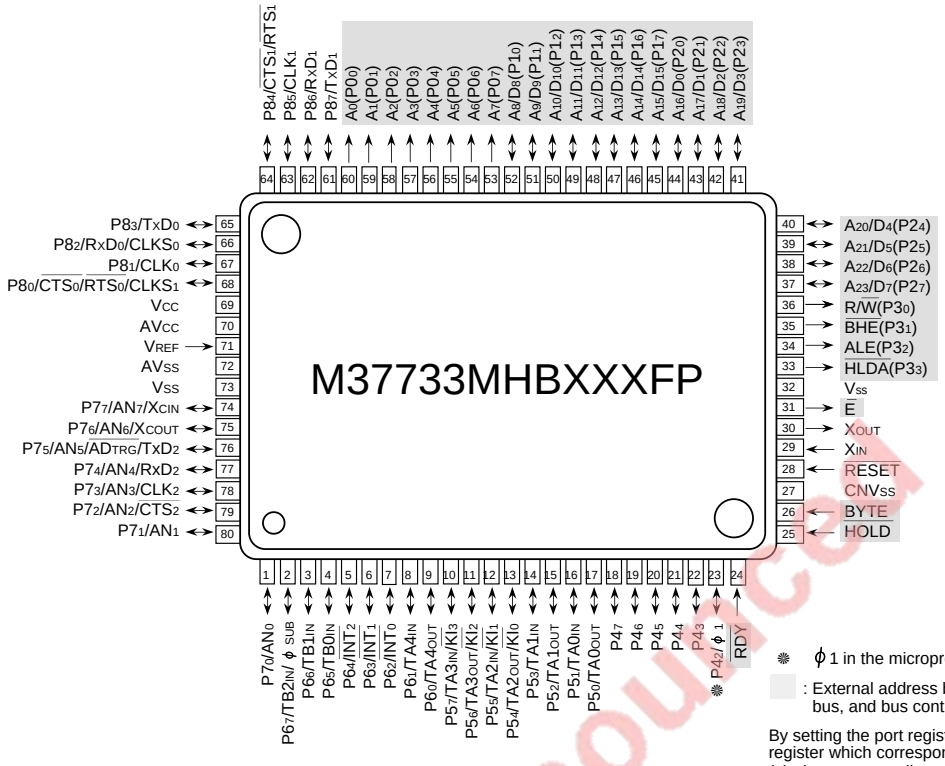
When connecting external devices which require a long access time, refer to sections **“12.2 Software wait,” “12.3 Ready function,”** and **“12.4 Hold function,”** also.

When connecting external devices, make sure that the microcomputer operates in the memory expansion or microprocessor mode. (Refer to section **“2.5 Processor modes.”**) When the microcomputer operates in these modes, ports P0 to P4 and pin $\overline{E}$ function as I/O pins of signals required for accessing external devices.

Figure 12.1.1 shows the pin configuration in the memory expansion or microprocessor mode. Table 12.1.1 lists the functions of ports P0 to P4 and pin $\overline{E}$ in the memory expansion or microprocessor mode.

EOL announced

When external data bus is 16 bits wide (BYTE = “L”)

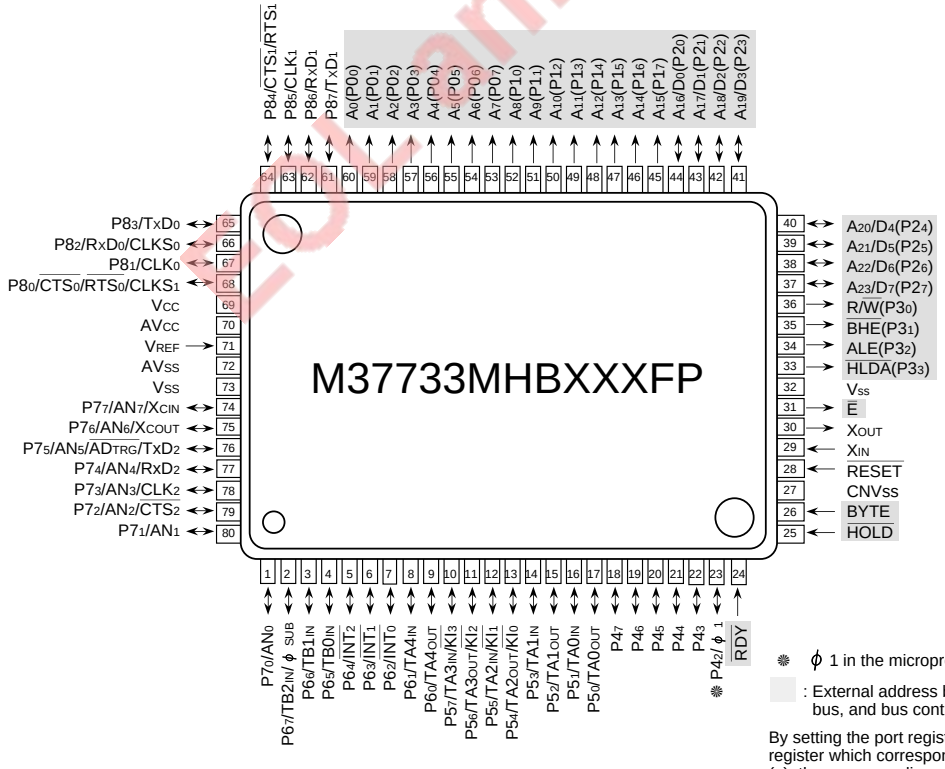


❋ ϕ 1 in the microprocessor mode

: External address bus, external data bus, and bus control signals

By setting the port register and port direction register which correspond to the port shown in ( ), the corresponding pin’s level can be fixed in the stop or wait mode.

When external data bus is 8 bits wide (BYTE = “H”)



❋ ϕ 1 in the microprocessor mode

: External address bus, external data bus, and bus control signals

By setting the port register and port direction register which correspond to the port shown in ( ), the corresponding pin’s level can be fixed in the stop or wait mode.

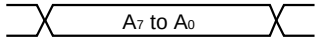
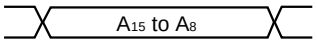
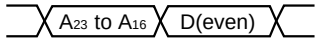
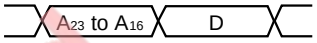
Fig. 12.1.1 Pin configuration in memory expansion or microprocessor mode (Top view)

Preliminary Announcement

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

Table 12.1.1 Functions of ports P0 to P4 and pin $\overline{E}$ in memory expansion or microprocessor mode

Pin name \ External data bus width	16 bits (BYTE = "L")	8 bits (BYTE = "H")
A_7 to A_0	A_7 to A_0 	
A_{15}/D_{15} to A_8/D_8	A_{15}/D_{15} to A_8/D_8 D(odd) : Data at odd address	A_{15} to A_8 
A_{23}/D_7 to A_{16}/D_0	A_{23}/D_7 to A_{16}/D_0  D(even) : Data at even address	A_{23}/D_7 to A_{16}/D_0  D : Data
$\overline{HLDA}$ ALE $\overline{BHE}$ R/$\overline{W}$	$\overline{HLDA}$ ALE $\overline{BHE}$ R/$\overline{W}$	
$P4_7$ to $P4_3$ ϕ 1 $\overline{RDY}$ $\overline{HOLD}$	$P4_7$ to $P4_3$ P : Functions as programmable I/O port ϕ1 **(Note 1)** $\overline{RDY}$ $\overline{HOLD}$	
$\overline{E}$	$\overline{E}$ **(Note 2)**	

Notes 1: In the memory expansion mode, this pin functions as a programmable I/O port. Furthermore, it can be switched to be a clock ϕ_1 output pin when selected by software. In the microprocessor mode, this pin is affected by the signal output disable selection bit (bit 6 at address $6C_{16}$). (Refer to **Table 12.1.5**.)

2: This signal is affected by the signal output disable selection bit (bit 6 at address $6C_{16}$). (Refer to **Table 12.1.2**.)

EOL announced

12.1.1 External bus (A_0 to A_7, A_8/D_8 to A_{15}/D_{15}, and A_{16}/D_0 to A_{23}/D_7)

The address is output from pins A_0 to A_{23} and specify the external area. Figure 12.1.2 shows the external area. Pins A_8 to A_{23} of the external address bus and pins D_0 to D_{15} of the external data bus share the same pins. When pin BYTE's level, which is described later, is "L," in other words, when the external data bus is 16 bits wide, pins A_8/D_8 to A_{15}/D_{15} and A_{16}/D_0 to A_{23}/D_7 perform address output and data input/output with the time-sharing method. When pin BYTE's level is "H," in other words, when the external data bus is 8 bits wide, pins A_{16}/D_0 to A_{23}/D_7 perform address output and data input/output with the time-sharing method and pins A_8 to A_{15} output the address.

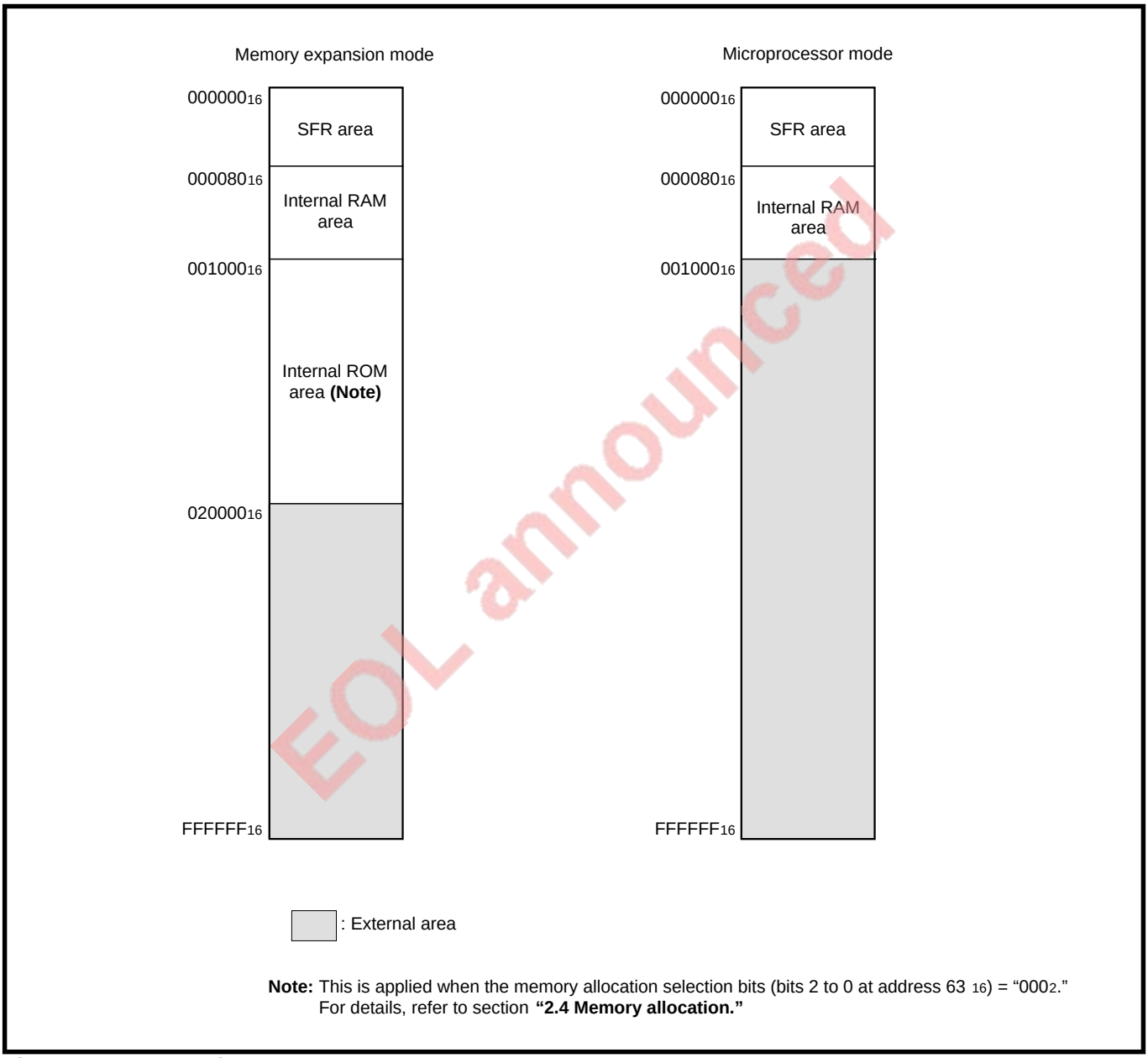


Fig. 12.1.2 External area

EOL announced

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

12.1.2 External data bus width selection signal (Pin BYTE's level)

This signal is used to select the external data bus width from 8 bits and 16 bits. When this signal level is "L," the external data bus is 16 bits wide; when this signal level is "H," the external data bus is 8 bits wide. (Refer to **Table 12.1.1.**) This signal level must be fixed to either "H" or "L."

This signal is valid only for the external areas. (When the internal area is accessed, the data bus is always 16 bits wide.)

12.1.3 Enable signal ($\overline{E}$)

When data is read or written, this signal level is "L." This signal is affected by the signal output disable selection bit (bit 6 at address $6C_{16}$). (Refer to **Table 12.1.2**.)

Table 12.1.2 $\overline{E}$ state

Processor mode	Conditions	Signal output disable selection bit	
		0	1
Memory expansion or Microprocessor mode	When the external area is accessed	Operating	
	When the internal area is accessed	Operating	Stopped at "H" level
	When the standby state selection bit = "1" in the stop or wait mode	Stopped at "H" level	Stopped at "L" level
	When the standby state selection bit = "0" in the stop or wait mode	Stopped at "H" level	
Single-chip mode	When not in the stop or wait mode	Operating	Stopped at "L" level
	When in the stop or wait mode	Stopped at "H" level	Stopped at "L" level

❋ For the stop and wait modes and the standby state selection bit, refer to chapter **"11. STOP AND WAIT MODES."**

: Not affected by the signal output disable selection bit.

12.1.4 Read/Write signal (R/$\overline{W}$)

This signal indicates data bus state. When data is written, this signal level is "L." Table 12.1.3 lists the data bus state indicated by signals $\overline{E}$ and R/$\overline{W}$.

Table 12.1.3 Data bus state

$\overline{E}$	R/$\overline{W}$	Data bus state
H	H	Not used
	L	
L	H	Read
	L	Write

EOL announced

12.1.5 Byte high enable signal ($\overline{BHE}$)

This signal indicates access to an odd address. This signal level is "L" when accessing only an odd address or when simultaneously accessing both an odd address and an even address.
This signal is used when connecting memory or I/O of which data bus is 8 bits wide with the 16-bit external data bus used. Table 12.1.4 lists the relationship between signal A_0 of the external address bus, signal $\overline{BHE}$, and access address.

Table 12.1.4 Relationship between signals A_0, $\overline{BHE}$ and access address

Access address	Even and Odd addresses (Simultaneous 2-byte access)	Even address (1-byte access)	Odd address (1-byte access)
A_0	L	L	H
$\overline{BHE}$	L	H	L

12.1.6 Address latch enable signal (ALE)

This signal is used to latch an address from a multiplexed signal. This multiplexed signal consists of the address and data and is input or output to or from pins A_8/D_8 to A_{15}/D_{15}, A_{16}/D_0 to A_{23}/D_7. When this signal level is "H," take the address into a latch and output it simultaneously. When this signal level is "L," retain the latched address.

12.1.7 Signal related to ready function ($\overline{RDY}$)

This signal is required to use the ready function. (Refer to section "**12.3 Ready function.**")

12.1.8 Signals related to hold function ($\overline{HOLD}$, $\overline{HLDA}$)

These signals are required to use the hold function. (Refer to section **"12.4 Hold function."**)

12.1.9 Clock ϕ_1

This signal has the same period as internal clock ϕ.
Whether to output or stop clock ϕ_1 can be selected by software. However, the method of this selection depends on the processor mode. Table 12.1.5 lists the method to select whether to output or stop clock ϕ_1. Figure 12.1.3 shows the clock ϕ_1 output start timing.

Table 12.1.5 Method to select whether to output or stop clock ϕ_1

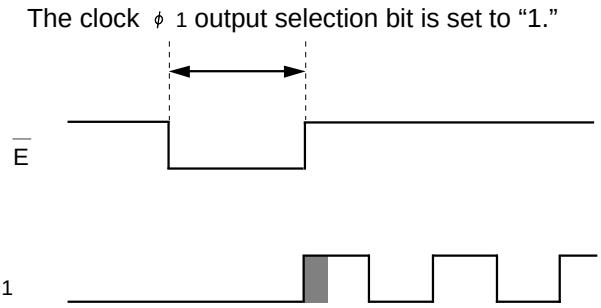
Processor mode	Single-chip or Memory expansion mode	Microprocessor mode
Clock ϕ_1 output	Set the clock ϕ_1 output selection bit[*1] to "1."	Clear the signal output disable selection bit[*2] to "0."
Clock ϕ_1 stopped	Clear the clock ϕ_1 output selection bit to "0." (Pin $P4_2$ functions as a programmable I/O port.)	Set the signal output disable selection bit to "1." **(Note)**
Remark	Clock ϕ_1 is stopped after reset. The signal output disable selection bit is ignored.	Clock ϕ_1 is output after reset. The clock ϕ_1 output selection bit is ignored.

Clock ϕ_1 output selection bit[*1]: Bit 7 at address $5E_{16}$
Signal output disable selection bit[*2]: Bit 6 at address $6C_{16}$ (Refer to **Table 12.1.2**.)
Note: In this case, make sure that bit 2 at address C_{16} (Port P4 direction register) is set to "1."
When bit 2 at address A_{16} (Port P4 register) = "0," "L" level is output: when this bit = "1," "H" level is output.

Not announced

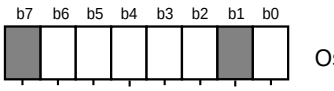
CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices



Notes 1: There is a possibility that the first cycle of clock ϕ1 output is not an exact square; the shaded section may be lost.
2: This is applied when “1” is written to the clock ϕ1 output selection bit while pin P4 2 outputs “L” level.

Fig. 12.1.3 Clock ϕ1 output start timing (when clock ϕ1 output selection bit is set from “0” to “1”)



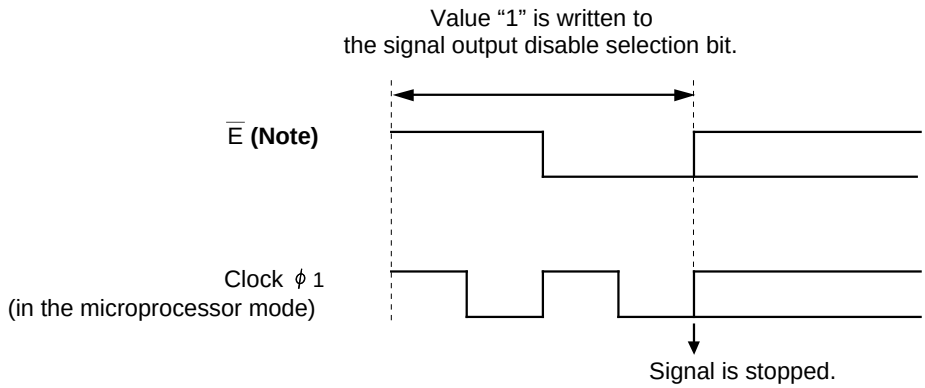
Oscillation circuit control register 0 (address $6C_{16}$)

Bit	Bit name	Functions	At reset	RW
0	X_{COUT} drivability selection bit	0: Drivability “LOW” 1: Drivability “HIGH”	1	RW (**Note 1**)
1	Not implemented.		Un-defined	–
2	Main clock stop bit	0: Main clock oscillation or external clock input is available. 1: Main clock oscillation or external clock input is stopped.	0	RW (**Note 1**)
3	System clock selection bit	When the port-Xc selection bit = “0,” 0: Main clock 1: Main clock divided by 8 When the port-Xc selection bit = “1,” 0: Main clock 1: Sub clock	0	RW (**Note 2**)
4	Port-Xc selection bit.	0: Operate as I/O ports ($P7_7$, $P7_6$). 1: Operate as pins X_{CIN} and X_{COUT}.	0	RW (**Notes 2 and 3**)
5	System clock stop bit at wait state **(Note 4)**	0: Operates in the wait mode. 1: Stopped in the wait mode.	0	RW
6	Signal output disable selection bit	0: Output is enabled. (Refer to **Tables 12.1.2 and 12.1.5**) 1: Output is disabled.	0	RW
7	Not implemented.		Un-defined	–

Notes 1: Nothing can be written to this bit after reset. Writing to this bit is enabled when the port-Xc selection bit = “1.”
2: When selecting the sub clock as the system clock, set bit 3 to “1” after setting bit 4 to “1.” If the above settings are performed simultaneously, in other words, performed by executing only one instruction, only bit 3 is set to “1.”
3: Although this bit can be set to “1,” it cannot be cleared to “0” after this bit is once set to “1.”
4: When setting the system clock stop bit at wait state to “1,” perform it immediately before the **WIT** instruction is executed. Furthermore, clear this bit to “0” immediately after the wait mode is terminated.
5: ▭ represents that bits 0 to 5 and 7 are not used for access control of external area. (Functions of these bits are valid.)

Fig. 12.1.4 Structure of oscillation circuit control register 0

EOL announced



Note: For conditions and signal levels, refer to **Tables 12.1.2 and 12.1.5.**

Fig. 12.1.5 Relationship between setting of signal output disable selection bit and stop timing of clock ϕ1 and $\overline{E}$

EOL announced

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

12.1.10 Operation of bus interface unit (BIU)

Figures 12.1.6 and 12.1.7 show operating waveform examples of signals which are input to or output from the external when accessing external devices. These waveforms are described in relation to the basic operating waveforms. (Refer to section **"2.2.3 Operation of bus interface unit (BIU)."**)

(1) When fetching an instruction into an instruction queue buffer

① When an instruction which is next fetched resides at an even address

When the external data bus is 16 bits wide, the BIU fetches two bytes of the instruction at a time with waveform (a). When the external data bus is 8 bits wide, the BIU fetches only one byte of the instruction with the first half of waveform (e).

② When an instruction which is next fetched resides at an odd address

When the external data bus is 16 bits wide, the BIU fetches only one byte of the instruction with waveform (d). When the external data bus is 8 bits wide, the BIU fetches only one byte of the instruction with the first half of waveform (f).

When branched to an odd address by executing a branch instruction or others with the 16-bit external data bus, at first, the BIU fetches one byte of an instruction with waveform (d) and then fetches instructions by the two bytes with waveform (a).

(2) When reading or writing data from or to memory • I/O

① When accessing 16-bit data which starts from an even address, waveform (a) or (e) is applied.
② When accessing 16-bit data which starts from an odd address, waveform (b) or (f) is applied.
③ When accessing 8-bit data which resides at an even address, waveform (c) or the first half of waveform (e) is applied.
④ When accessing 8-bit data which resides at an odd address, waveform (d) or the first half of waveform (f) is applied.

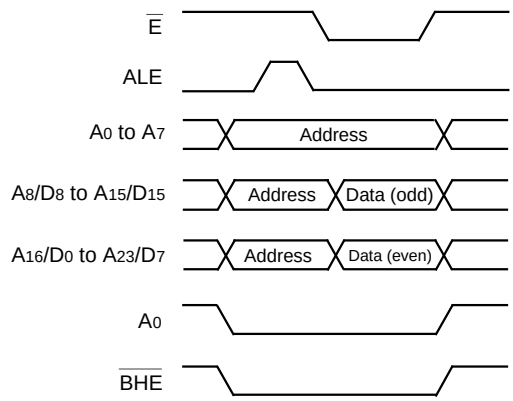
For instructions which are affected by data length flag (m) and index register length flag (x), an operation is applied as follows:
•When "m" or "x" = "0," operation ① or ② is applied.
•When "m" or "x" = "1," operation ③ or ④ is applied.
Settings of flags "m" and "x" and selection of the external data bus width do not affect each other.

EOL announced

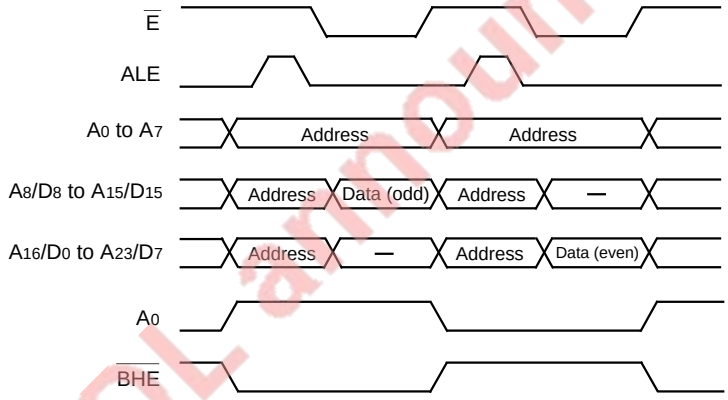
● When external data bus is 16 bits wide (BYTE = “L”)

<16-bit data access>

(a) Access starting from even address



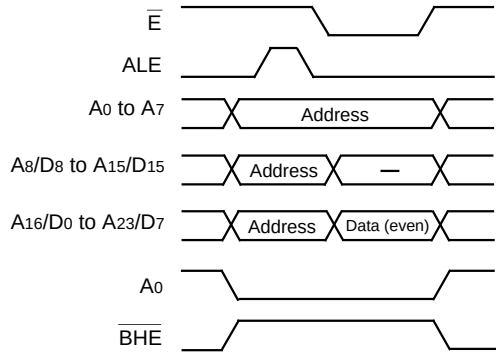
(b) Access starting from odd address



EOL announced

<8-bit data access>

(c) Access to even address



(d) Access to odd address

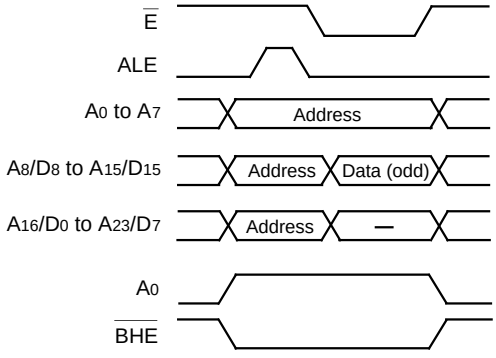


Fig. 12.1.6 Operating waveform examples of signals which are input to or output from the external (1)

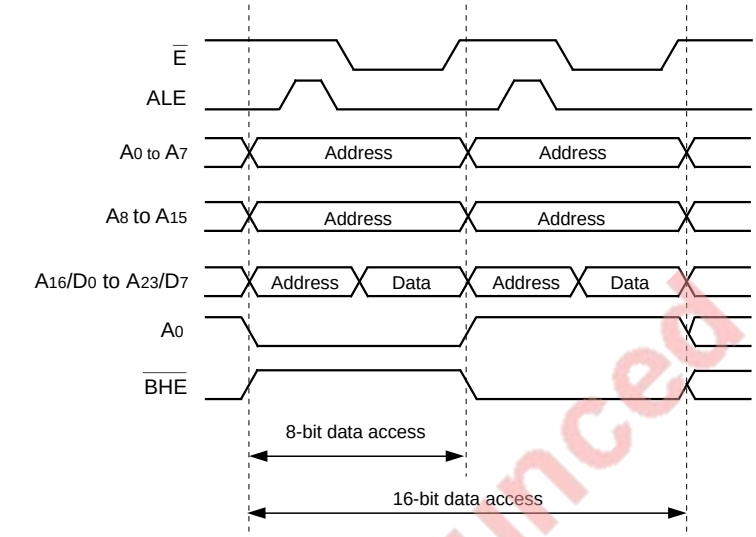
CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

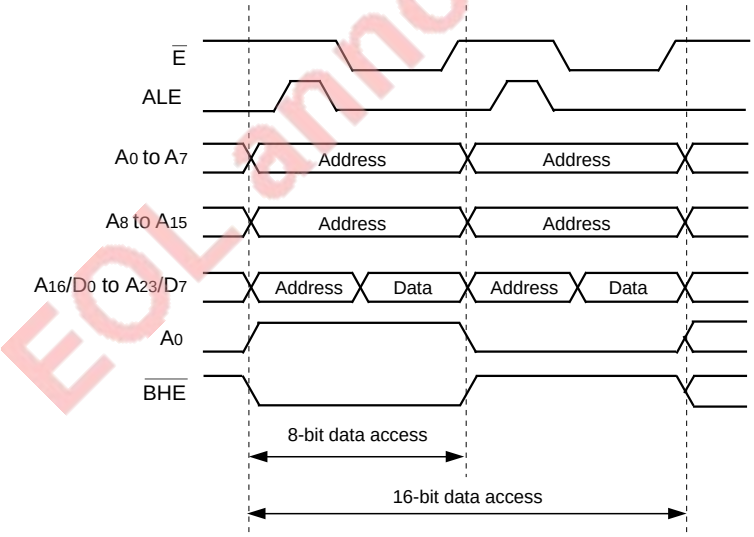
● When external data bus is 8 bits wide (BYTE = “H”)

<8/16-bit data access>

(e) Access starting from even address



(f) Access starting from odd address



Note: When 16-bit data is accessed, the low-order 8 bits of data are accessed first, and then, the high-order 8 bits are accessed.

Fig. 12.1.7 Operating waveform examples of signals which are input to or output from the external (2)

EOL announced

12.2 Software wait

The software wait facilitates access to external devices which require a long access time. There are two types of software waits: wait 0 and wait 1.

The software wait is set by the wait bit (bit 2 at address $5E_{16}$) and the wait selection bit (bit 0 at address $5F_{16}$). (Refer to **Table 12.2.1.**) Figure 12.2.1 shows the structures of the processor mode register 0 (address $5E_{16}$) and processor mode register 1 (address $5F_{16}$). Figure 12.2.2 shows bus timing examples when the software wait is used.

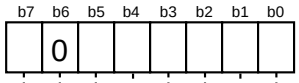
The software wait is valid only for the external area. (Access to the internal areas is always performed with no wait.)

Table 12.2.1 Setting method of software wait

Wait bit	Wait selection bit	Software wait	Bus cycle
1	0	Invalid (No wait)	Cycle of "internal clock ϕ divided by 2" (clock ϕ_1's cycle × 2)
0	0	Wait 0	"Cycle in the no-wait state" × 2 (clock ϕ_1's cycle × 4)
0	1	Wait 1	"Cycle in the no-wait state" × 1.5 (clock ϕ_1's cycle × 3)

EOL announced

12.2 Software wait



Processor mode register 0 (address 5E 16)

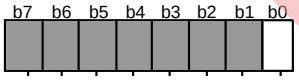
Bit	Bit name	Functions	At reset	RW
0	Processor mode bits	b1 b0 00: Single-chip mode 01: Memory expansion mode 10: Microprocessor mode 11: Do not select.	0	RW
1			0 **(Note 1)**	RW
2	Wait bit	0: Software wait is inserted when accessing external area. 1: No software wait is inserted when accessing external area.	0	RW
3	Software reset bit	Microcomputer is reset by setting this bit to "1." This bit is "0" at reading.	0	WO
4	Interrupt priority detection time selection bits	b5 b4 00: 7 cycles of ϕ 01: 4 cycles of ϕ 10: 2 cycles of ϕ 11: Do not select.	0	RW
5			0	RW
6	Must be fixed to "0."		0	RW
7	Clock ϕ_1 output selection bit **(Note 2)**	0: Clock ϕ_1 output is disabled. (P42 functions as a programmable /O port.) 1: Clock ϕ_1 output is enabled. (Port P42 functions as a clock ϕ_1 output pin.)	0	RW

Notes 1: When the Vcc-level voltage is applied to pin CNVss, this bit is set to "1" after reset. (At reading, this bit is always "1.")

2: This bit is ignored in the microprocessor mode. (It may be "0" or "1.")

3: ▭ represents that bits 3 to 6 are not used for access control of the external area. (Functions of these bits are valid.)

EOL announced

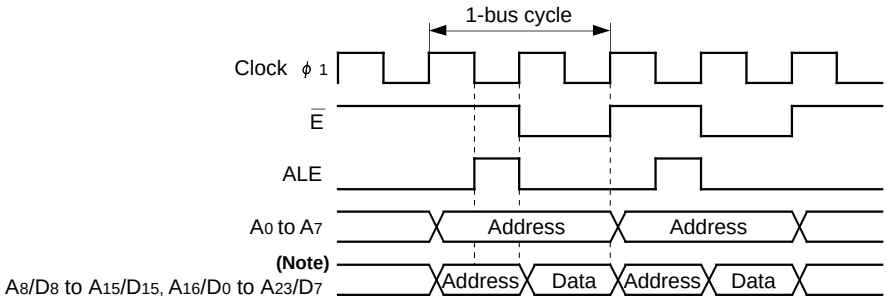


Processor mode register 1 (address 5F 16)

Bit	Bit name	Function	At reset	RW
0	Wait selection bit	0 : Wait 0 1 : Wait 1	0	RW
7 to1	Not implemented.		Un-defined	–

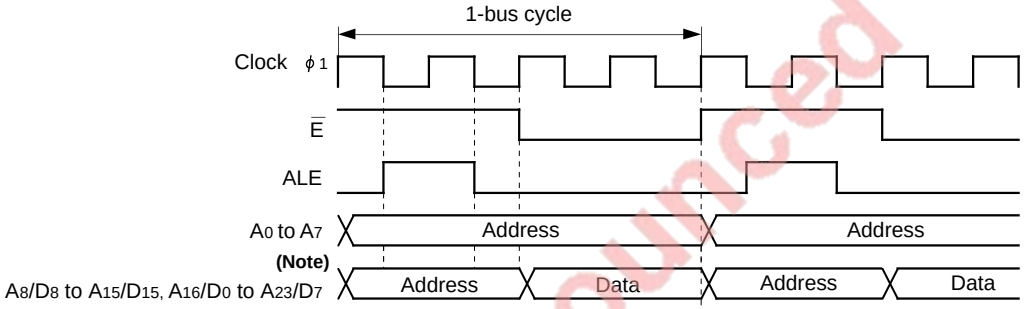
Fig. 12.2.1 Structures of processor mode register 0 and processor mode register 1

<<No wait>>

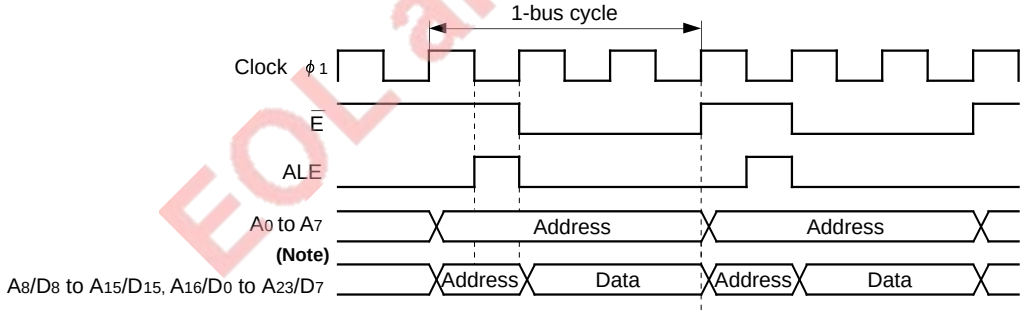


● This waveform is always applied when the internal area is accessed.

<<Wait 0>>



<<Wait 1>>



EOL announced

Note: When the external data bus is 8 bits wide (BYTE = "H"), operating waveform of A8/D8 to A15/D15 is the same as that of A0 to A7.

Fig. 12.2.2 Bus timing examples when software wait is used (BYTE = "L").

12.3 Ready function

The ready function facilitates access to external devices which require a long access time.
By applying "L" level to pin $\overline{RDY}$ in the memory expansion or microprocessor mode, the microcomputer enters the ready state. While pin $\overline{RDY}$'s level is "L," this state is retained. Table 12.3.1 lists the microcomputer's state in the ready state.
In the ready state, oscillation of the oscillator does not stop. Therefore, the internal peripheral devices can operate even in the ready state. The ready function is valid for the internal and external areas.

Table 12.3.1 Microcomputer's state in ready state

Item	State
Oscillation	Operating
ϕCPU	Stopped at "L" level
$\overline{HLDA}$, $\overline{E}$, R/$\overline{W}$, $\overline{BHE}$, ALE, A_0 to A_7, A_8/D_8 to A_{15}/D_{15}, A_{16}/D_0 to A_{23}/D_7, $P4_3$ to $P4_7$, $P5$ to $P8$	Retains the same state in which $\overline{RDY}$ was accepted.
$P4_2$/ϕ_1	In the memory expansion mode ■ When the clock ϕ_1 output selection bit[*1] = "1" Outputs clock ϕ_1. ■ When the clock ϕ_1 output selection bit = "0" Retains the same state in which $\overline{RDY}$ was accepted. In the microprocessor mode ■ When the signal output disable selection bit[*2] = "1" Retains the same state in which $\overline{RDY}$ was accepted. ■ When the signal output disable selection bit = "0" Outputs clock ϕ_1.
Timers A and B, Serial I/O, A-D converter, Watchdog timer	Operating

Clock ϕ_1 output selection bit[*1]: Bit 7 at address $5E_{16}$
Signal output disable selection bit[*2]: Bit 6 at address $6C_{16}$

Note: When "L" level which was input to pin $\overline{RDY}$ is sampled at one of the following timings, this signal is not accepted. (Note that ϕCPU is stopped at "L" level.)
- When the level of signal $\overline{E}$ is "H" while the bus is in use (Refer to ② **in Figure 12.3.1**.)
- Immediately before a wait generated by the software wait (Refer to ⑤ **in Figure 12.3.1.**)

EOL announced

12.3.1 Operation in ready state

When “L” level is input to pin $\overline{\text{RDY}}$, this signal is accepted at the falling edge of clock $\phi 1$ and the microcomputer enters the ready state. The ready state can be terminated by setting pin $\overline{\text{RDY}}$'s level to “H” again. When “H” level is input to pin $\overline{\text{RDY}}$, this signal is also accepted at the falling edge of clock $\phi 1$ and the ready state is terminated. Figure 12.3.1 shows timings when the ready state is accepted and terminated.

Refer to section **“17.1 Memory expansion”** for the way to use the ready function.

EOL announced

12.3 Ready function

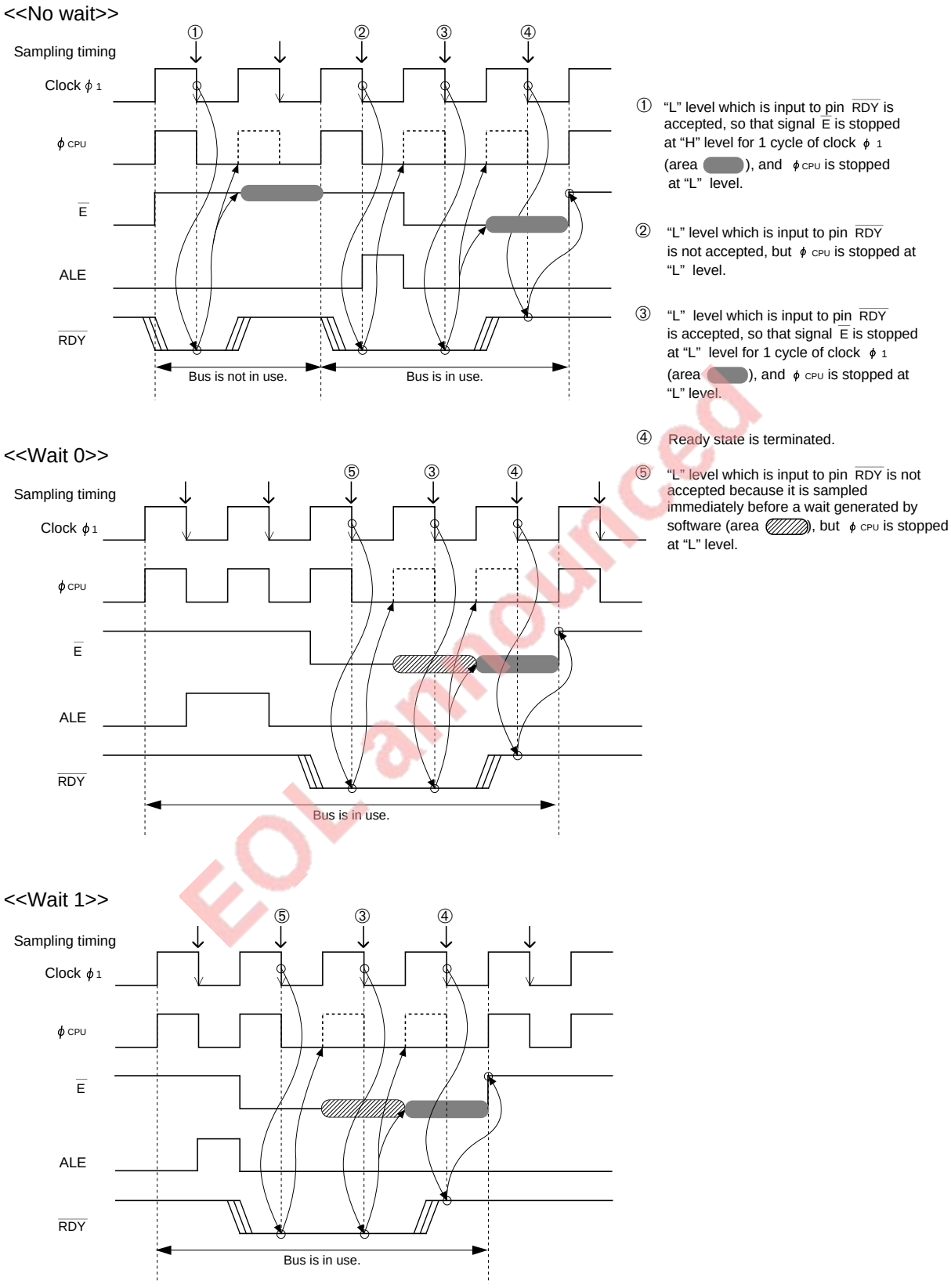


Fig. 12.3.1 Timings when ready state is accepted and terminated

EOL announced

12.4 Hold function

When an external circuit which accesses the bus without using the central processing unit (CPU), for example DMA, is used, it is necessary to generate a timing for transferring the right to use of the bus from the CPU to the external circuit. The hold function is used to generate this timing.

By applying "L" level to pin $\overline{HOLD}$ in the memory expansion or microprocessor mode, the microcomputer enters the hold state. While pin $\overline{HOLD}$'s level is "L," this state is retained. Table 12.4.1 lists the microcomputer's state in the hold state.

In the hold state, oscillation of the oscillator does not stop. Therefore, the internal peripheral devices can operate even in the hold state. (Note that the watchdog timer stops.)

Table 12.4.1 Microcomputer's state in hold state

Item	State
Oscillation	Operating
ϕCPU	Stopped at "L"
A_0 to A_7, A_8/D_8 to A_{15}/D_{15}, A_{16}/D_0 to A_{23}/D_7, R/$\overline{W}$, $\overline{BHE}$	Floating
$\overline{HLDA}$, ALE	Outputs "L" level.
$P4_2/\phi_1$	In the memory expansion mode ■ When the clock ϕ_1 output selection bit[*1] = "1" Outputs clock ϕ_1. ■ When the clock ϕ_1 output selection bit = "0" Retains the same state in which $\overline{HOLD}$ was accepted. In the microprocessor mode ■ When the signal output disable selection bit[*2]= "1" Retains the same state in which $\overline{HOLD}$ was accepted. ■ When the signal output disable selection bit = "0" Outputs clock ϕ_1.
$P4_3$ to $P4_7$, P5 to P8	Retains the same state in which $\overline{HOLD}$ was accepted.
Timers A and B, Serial I/O, A-D converter	Operating
Watchdog timer	Stopped

Clock ϕ_1 output selection bit[*1]: Bit 7 at address $5E_{16}$
Signal output disable selection bit[*2]: Bit 6 at address $6C_{16}$

EOL announced

12.4 Hold function

12.4.1 Operation in Hold state

When “L” level is input to pin $\overline{\text{HOLD}}$ while the bus is not in use, this signal is accepted at the falling edge of clock ϕ_1 in each bus cycle. When “L” level is input to pin $\overline{\text{HOLD}}$ while the bus is in use, this signal is accepted at the last falling edge of clock ϕ_1. (Refer to **Figures 12.4.2 to 12.4.6**.) When word data which starts from an odd address is accessed by the two bus cycles, determination is performed only in the second bus cycle. (Refer to **Figure 12.4.1.**)

When “L” level which was input to pin $\overline{\text{HOLD}}$ is accepted, ϕ_{CPU} is stopped at the next rising edge of clock ϕ_1. At this time, pin $\overline{\text{HLDA}}$ outputs “L” level, and so the external is informed that the microcomputer is in the hold state. After one cycle of clock ϕ_1 has passed since pin $\overline{\text{HLDA}}$’s level becomes “L,” pins R/$\overline{\text{W}}$, $\overline{\text{BHE}}$ and the external bus enter the floating state.

The hold state can be terminated by setting pin $\overline{\text{HOLD}}$’s level to “H” again. When “H” level is input to pin $\overline{\text{HOLD}}$, the signal is accepted at the falling edge of clock ϕ_1. When “H” level which was input to pin $\overline{\text{HOLD}}$ is accepted, pin $\overline{\text{HLDA}}$’s level goes from “L” to “H.” And then, the hold state is terminated after one cycle of clock ϕ_1 has passed.

Figures 12.4.2 to 12.4.6 show the timing when the hold state is accepted and terminated.

❋ In the ready state, determination of pin $\overline{\text{HOLD}}$’s input level is not performed.

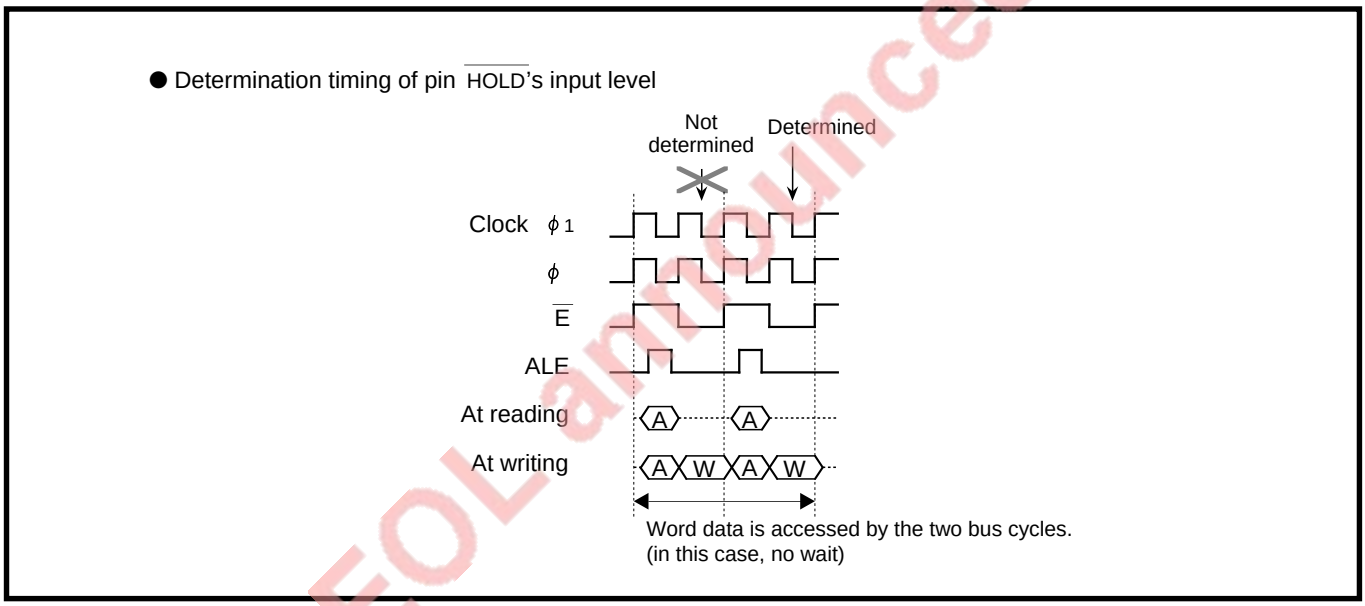


Fig.12.4.1 Determination when word data which starts from odd address is accessed by the two bus cycles

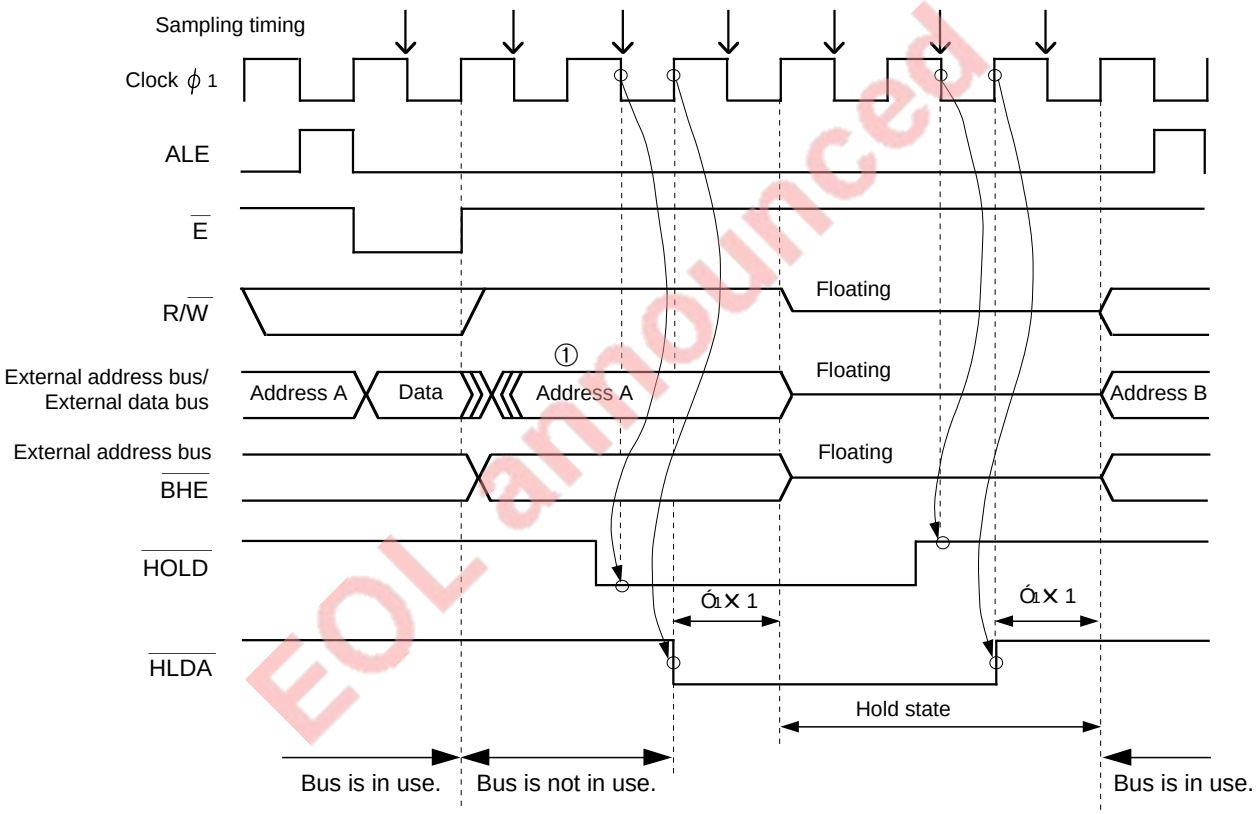
EOL announced

<<When “L” level is input to pin $\overline{\text{HOLD}}$ while bus is not in use>>

● State when “L” level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
Not in use	8	8, 16	No wait,
	16	8, 16	Wait 1, Wait 0

Note: The same operation is performed independent of the software wait (no wait, wait 0, or wait 1). This diagram shows the operation when no wait is selected.



EOL announced

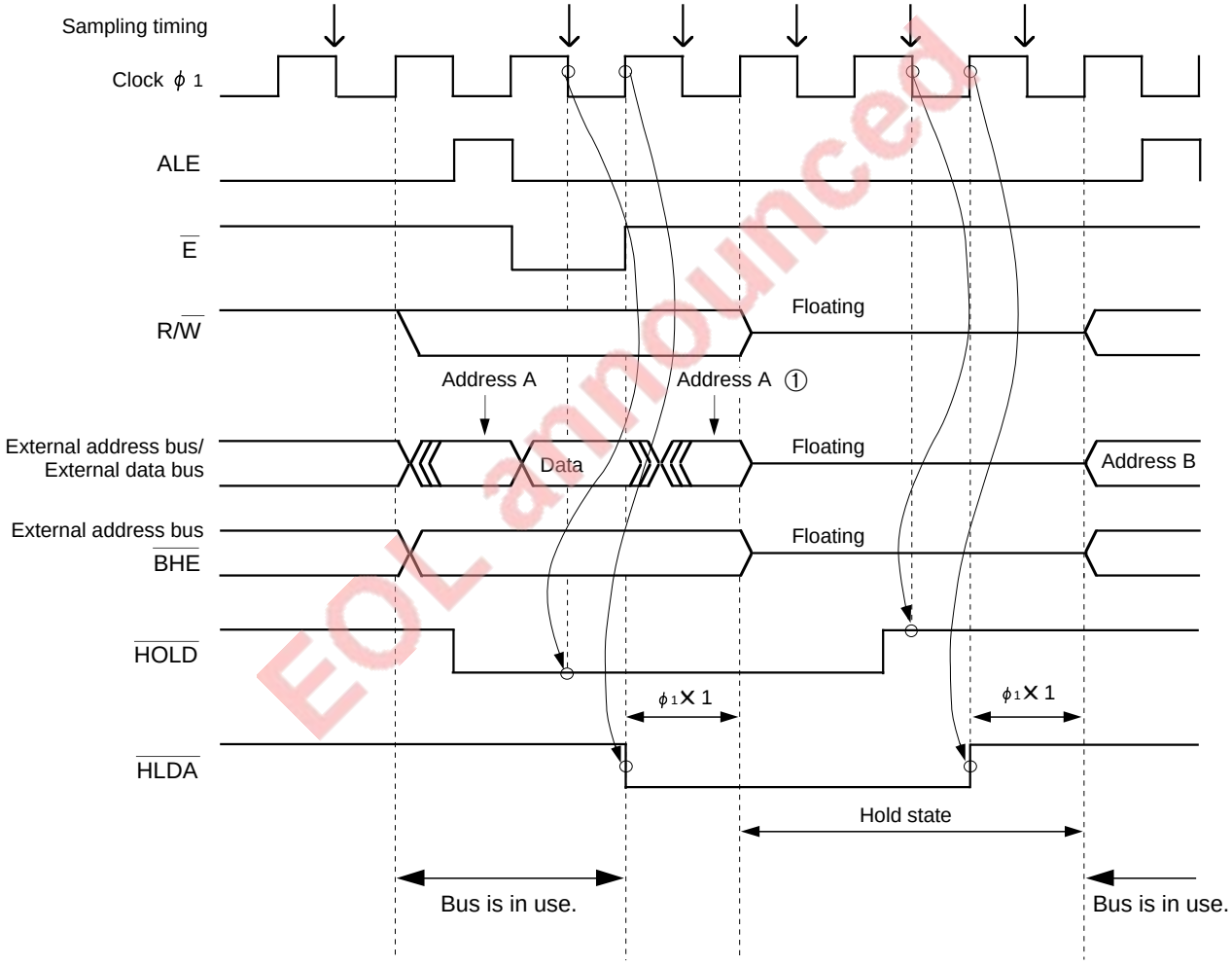
① Because the bus is not in use, the address which was output immediately before is output again, instead of a new address.

Fig. 12.4.2 Timing when hold state is accepted and terminated (1)

<<When “L” level is input to pin $\overline{\text{HOLD}}$ while bus is in use (1)>>

State when “L” level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	8	8,16	No wait
	16	16 (When accessed starting from even address)	



EOL announced

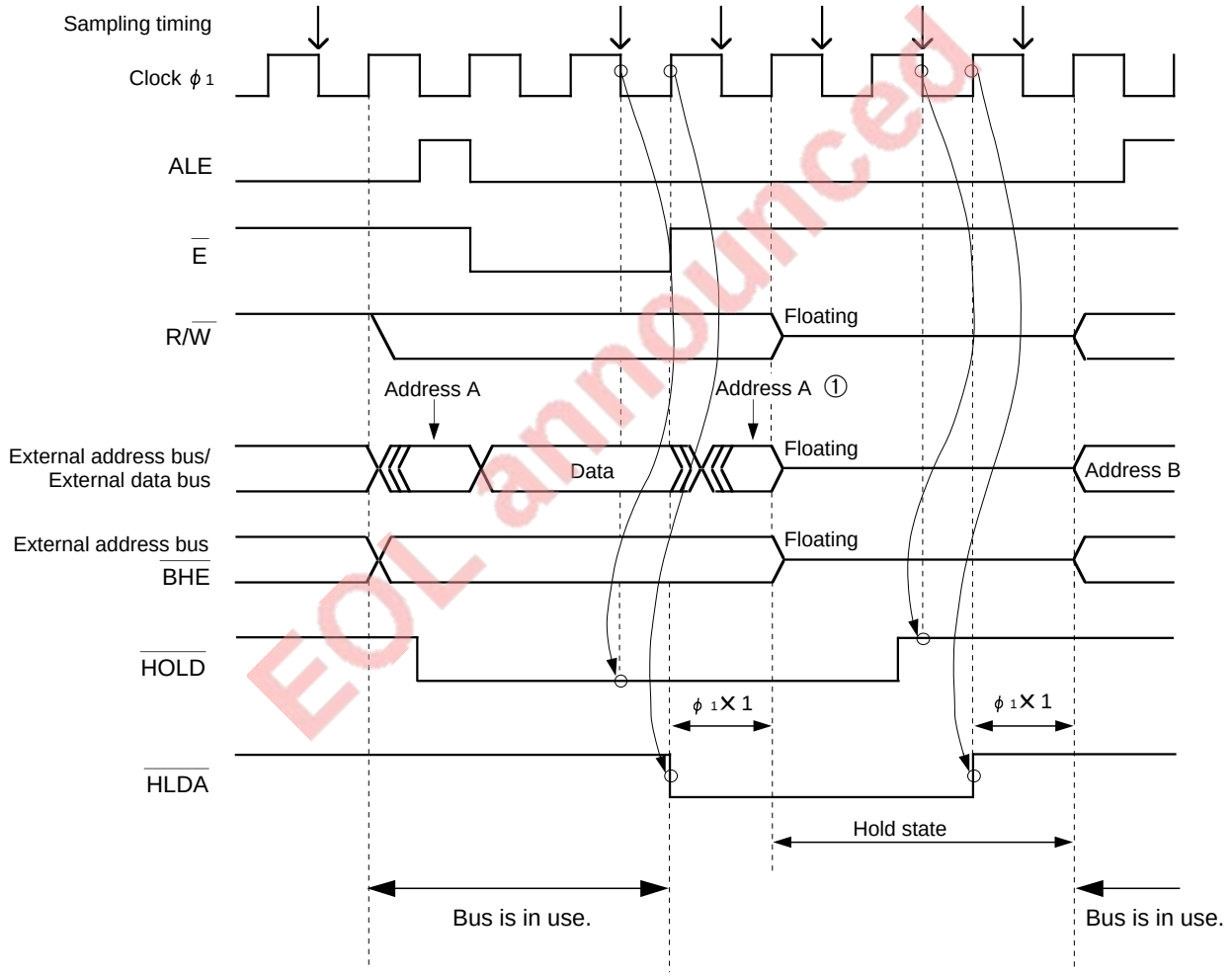
① When “L” level which is input to pin $\overline{\text{HOLD}}$ is accepted, the address which was output immediately before is output again, instead of a new address.

Fig. 12.4.3 Timing when hold state is accepted and terminated (2)

<<When "L" level is input to pin $\overline{\text{HOLD}}$ while bus is in use (2)>>

● State when "L" level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	8	8,16	Wait 1
	16	16 (When accessed starting from even address)	



EOL announced

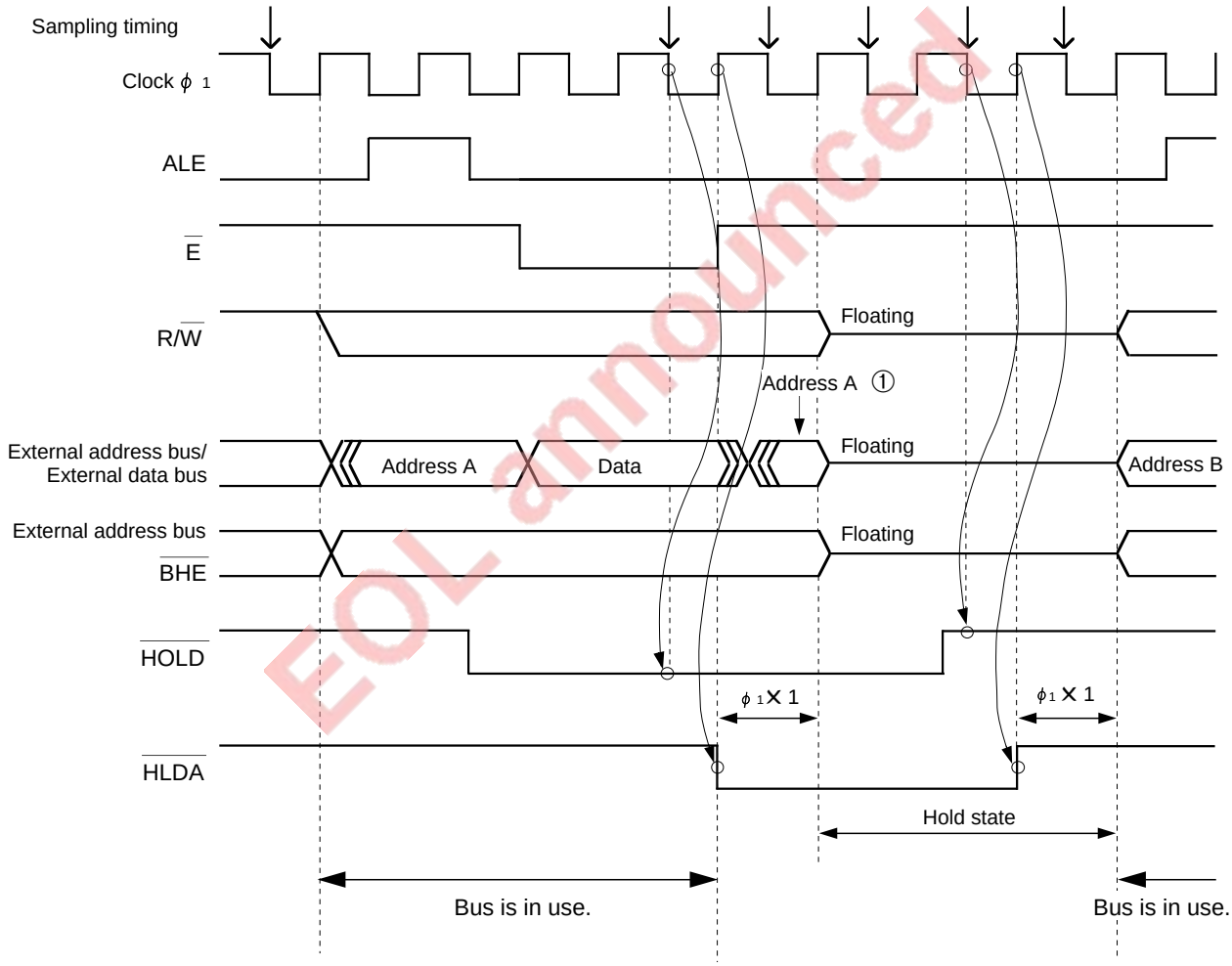
① When "L" level which is input to pin $\overline{\text{HOLD}}$ is accepted, the address which was output immediately before is output again, instead of a new address.

Fig. 12.4.4 Timing when hold state is accepted and terminated (3)

<<When "L" level is input to pin $\overline{\text{HOLD}}$ while bus is in use (3)>>

● State when "L" level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	8	8,16	Wait 0
	16	16 (When accessed starting from even address)	



EOL announced

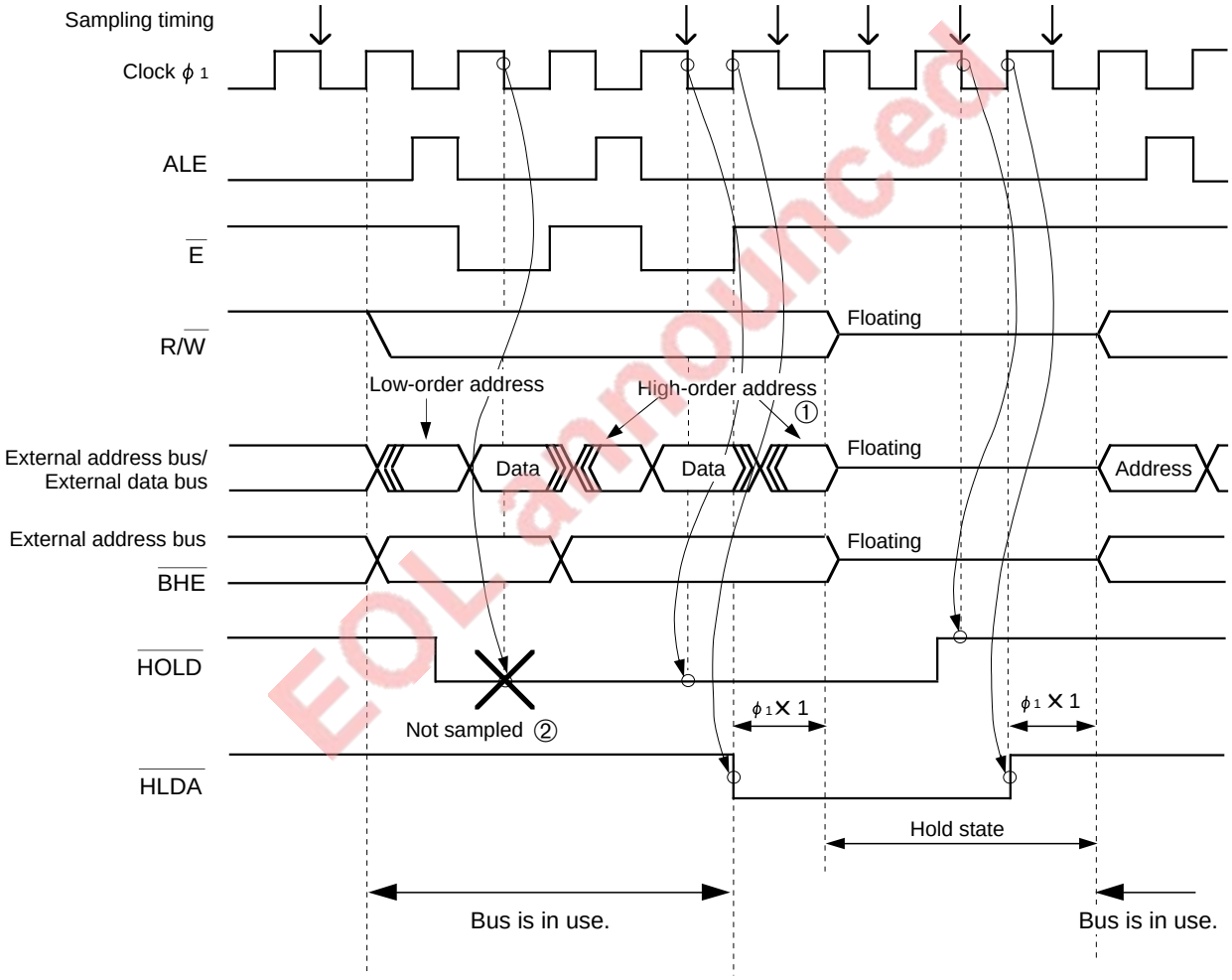
① When "L" level which is input to pin $\overline{\text{HOLD}}$ is accepted, the address which was output immediately before is output again, instead of a new address.

Fig. 12.4.5 Timing when hold state is accepted and terminated (4)

<<When "L" level is input to pin $\overline{\text{HOLD}}$ while bus is in use (4)>>

● State when "L" level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	16	8	No wait
		16 (When accessed starting from odd address)	



EOL announced

① When "L" level which is input to pin $\overline{\text{HOLD}}$ is accepted, the address which was output immediately before is output again, instead of a new address.
② Sampling is not performed until 16-bit data input/output is finished. ("L" level input to pin $\overline{\text{HOLD}}$ is not accepted.)

Fig. 12.4.6 Timing when hold state is accepted and terminated (5)

MEMO

EOL announced

CHAPTER 13
RESET

13.1 Hardware reset
13.2 Software reset

EOL announced

RESET

13.1 Hardware reset

How to reset the microcomputer is described below. There are two methods to reset the microcomputer: hardware reset and software reset.

13.1 Hardware reset

When the power source voltage satisfies the recommended operating conditions, the microcomputer is reset by applying “L” level to pin $\overline{\text{RESET}}$. (This is called “Hardware reset.”) Figure 13.1.1 shows an example of hardware reset timing.

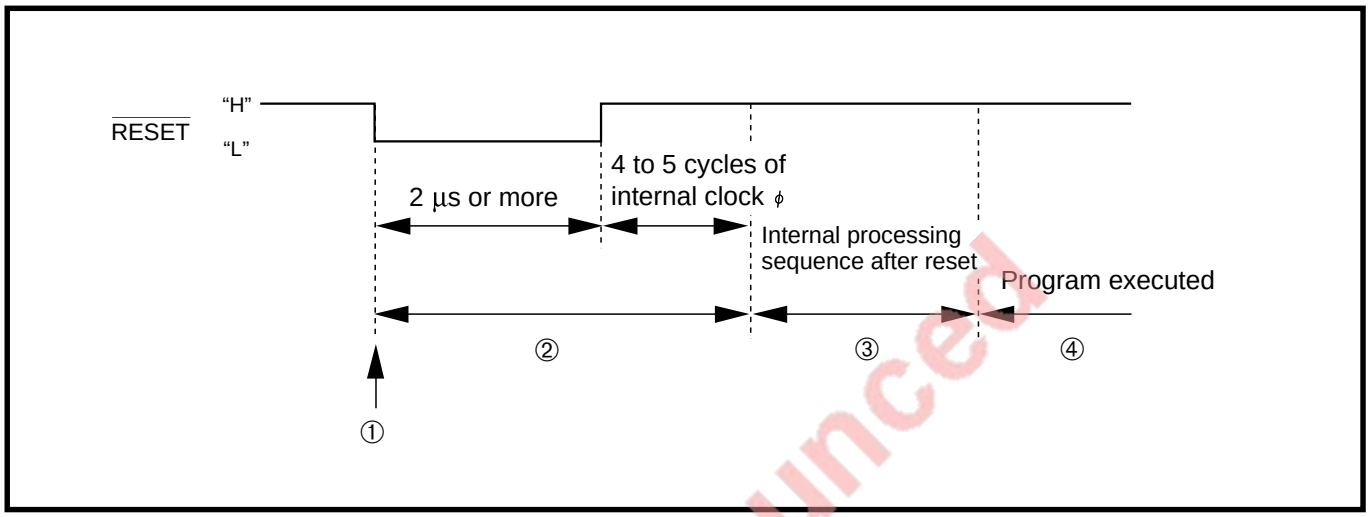


Fig. 13.1.1 Example of hardware reset timing (when main clock is stably supplied.)

The microcomputer’s operation during periods ① to ④ is described below.

① After “L” level is applied to pin $\overline{\text{RESET}}$, pins are initialized within a period of several ten ns. (Refer to **Table 13.1.1.**)

② While pin $\overline{\text{RESET}}$ is at “L” level or within a period of 4 to 5 cycles of internal clock ϕ after pin $\overline{\text{RESET}}$’s level changes from “L” to “H,” the central processing unit (CPU) and SFR area are initialized. At this time, the contents of the internal RAM area is undefined (except the cases where the stop or wait mode is terminated.). Refer to **Figures 13.1.2 to 13.1.6.**

③ After ②, “Internal processing sequence after reset” is performed. Refer to **Figure 13.1.7.**

④ A program is executed beginning with the address set in the reset vector addresses (addresses FFFE_{16} and FFFF_{16}).

EOL announced

13.1.1 Pin state

Table 13.1.1 lists the pin state while pin $\overline{\text{RESET}}$ is at "L" level.

Table 13.1.1 Pin state while pin $\overline{\text{RESET}}$ is at "L" level

	Pin CNVSS's level	Pin (Port) name	Pin state
Mask ROM version	VSS or VCC	P0 to P8	Floating
		$\overline{E}$	"H" level is output.
Built-in PROM version	VSS	P0 to P8	Floating
		$\overline{E}$	"H" level is output.
	VCC	P0, P1, P3 to P8	Floating
		P2	•Floating when "H" level is applied to both or one of pins $P5_1$ and $P5_2$ •"H" or "L" level is output when "L" level is applied to both of pins $P5_1$ and $P5_2$.
		$\overline{E}$	"H" level is output.
External ROM version	VCC	A_0 to A_7, A_8/D_8 to A_{23}/D_7, $\overline{BHE}$	Undefined value is output.
		R/$\overline{W}$, $\overline{HLDA}$, $\overline{E}$,	"H" level is output.
		ALE	"L" level is output.
		P4 to P8	Floating

EOL announced

RESET

13.1 Hardware reset

13.1.2 State of CPU, SFR area, and internal RAM area

Figure 13.1.2 shows the state of the CPU registers immediately after reset. Figures 13.1.3 to 13.1.6 show the state of the SFR area and internal RAM area immediately after reset.

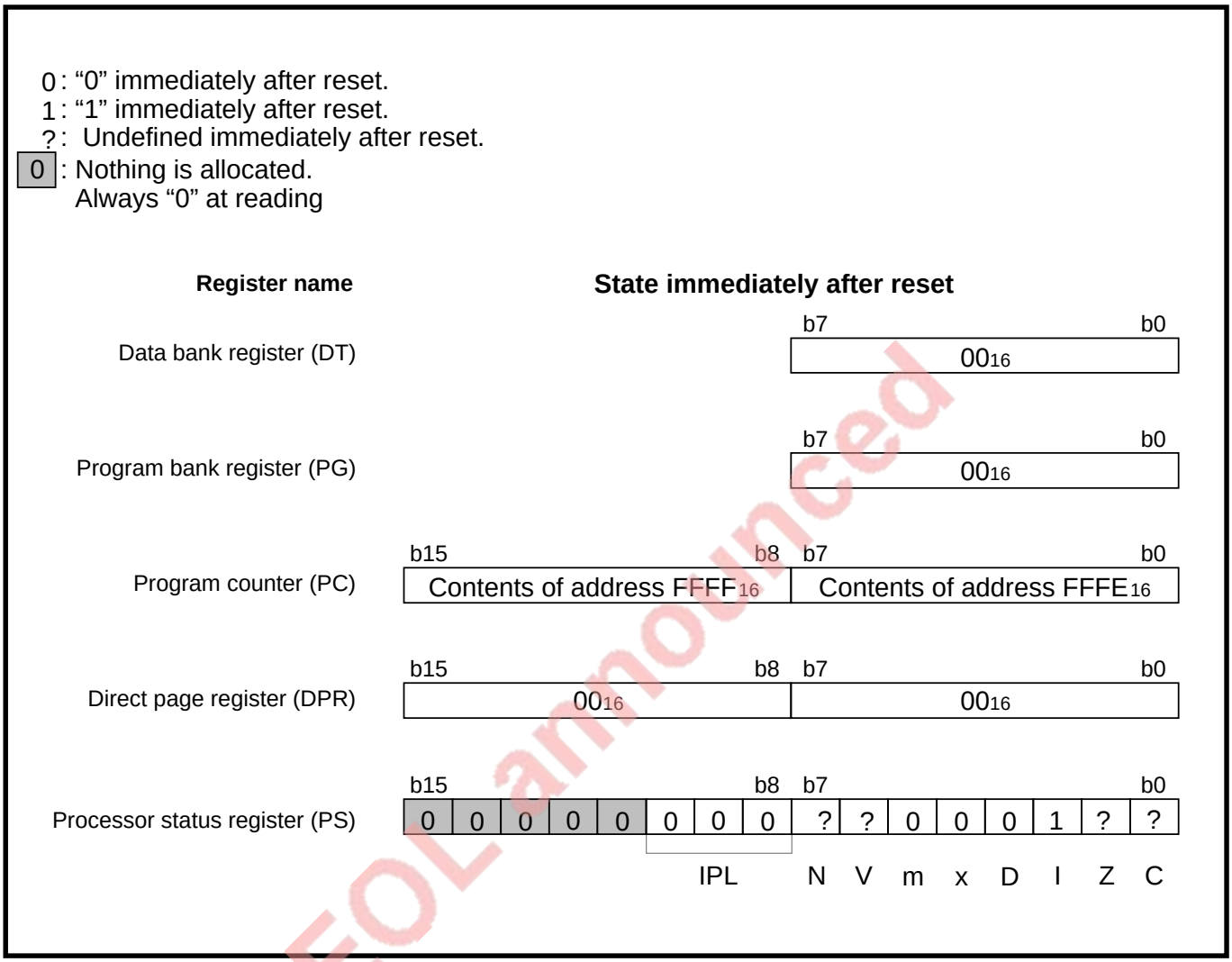


Fig. 13.1.2 State of CPU registers immediately after reset

EOL announced

■SFR area (addresses 0_{16} to $7F_{16}$)

Abbreviations and symbols which represent access characteristics

RW : It is possible to read the bit state at reading. The written value becomes valid.
RO : It is possible to read the bit state at reading. The written value becomes invalid.
WO : The written value becomes valid. It is impossible to read the bit state.
▭ : Not implemented. It is impossible to read the bit state. The written value becomes invalid.

0 : "0" immediately after reset.
1 : "1" immediately after reset.
? : Undefined immediately after reset.

0 : Always "0" at reading
? : Always undefined at reading
0 : "0" immediately after reset. Must be fixed to "0."

Address	Register name	Access characteristics (b7 … b0)	State immediately after reset (b7 … b0)
0_{16}			?
1_{16}			?
2_{16}	Port P0 register	RW	?
3_{16}	Port P1 register	RW	?
4_{16}	Port P0 direction register	RW	00_{16}
5_{16}	Port P1 direction register	RW	00_{16}
6_{16}	Port P2 register	RW	?
7_{16}	Port P3 register	▭ ▭ ▭ ▭ RW	0 0 0 0 ?
8_{16}	Port P2 direction register	RW	00_{16}
9_{16}	Port P3 direction register	▭ ▭ ▭ ▭ RW	0 0 0 0 0 0 0 0
A_{16}	Port P4 register	RW	?
B_{16}	Port P5 register	RW	?
C_{16}	Port P4 direction register	RW	00_{16}
D_{16}	Port P5 direction register	RW	00_{16}
E_{16}	Port P6 register	RW	?
F_{16}	Port P7 register	RW	?
10_{16}	Port P6 direction register	RW	00_{16}
11_{16}	Port P7 direction register	RW	00_{16}
12_{16}	Port P8 register	RW	?
13_{16}			?
14_{16}	Port P8 direction register	RW	00_{16}
15_{16}			?
16_{16}			?
17_{16}			?
18_{16}			?
19_{16}			?
$1A_{16}$			?
$1B_{16}$			?
$1C_{16}$	(Reserved area)✻		?
$1D_{16}$	(Reserved area)✻		?
$1E_{16}$	A-D control register 0	RW	0 0 0 0 0 ? ? ?
$1F_{16}$	A-D control register 1	▭ ▭ RW ▭ RW	? ? 0 0 0 ? 1 1

✻ Do not write data to addresses $1C_{16}$ and $1D_{16}$.

FOL announced

Fig. 13.1.3 State of SFR area and internal RAM area immediately after reset (1)

RESET

13.1 Hardware reset

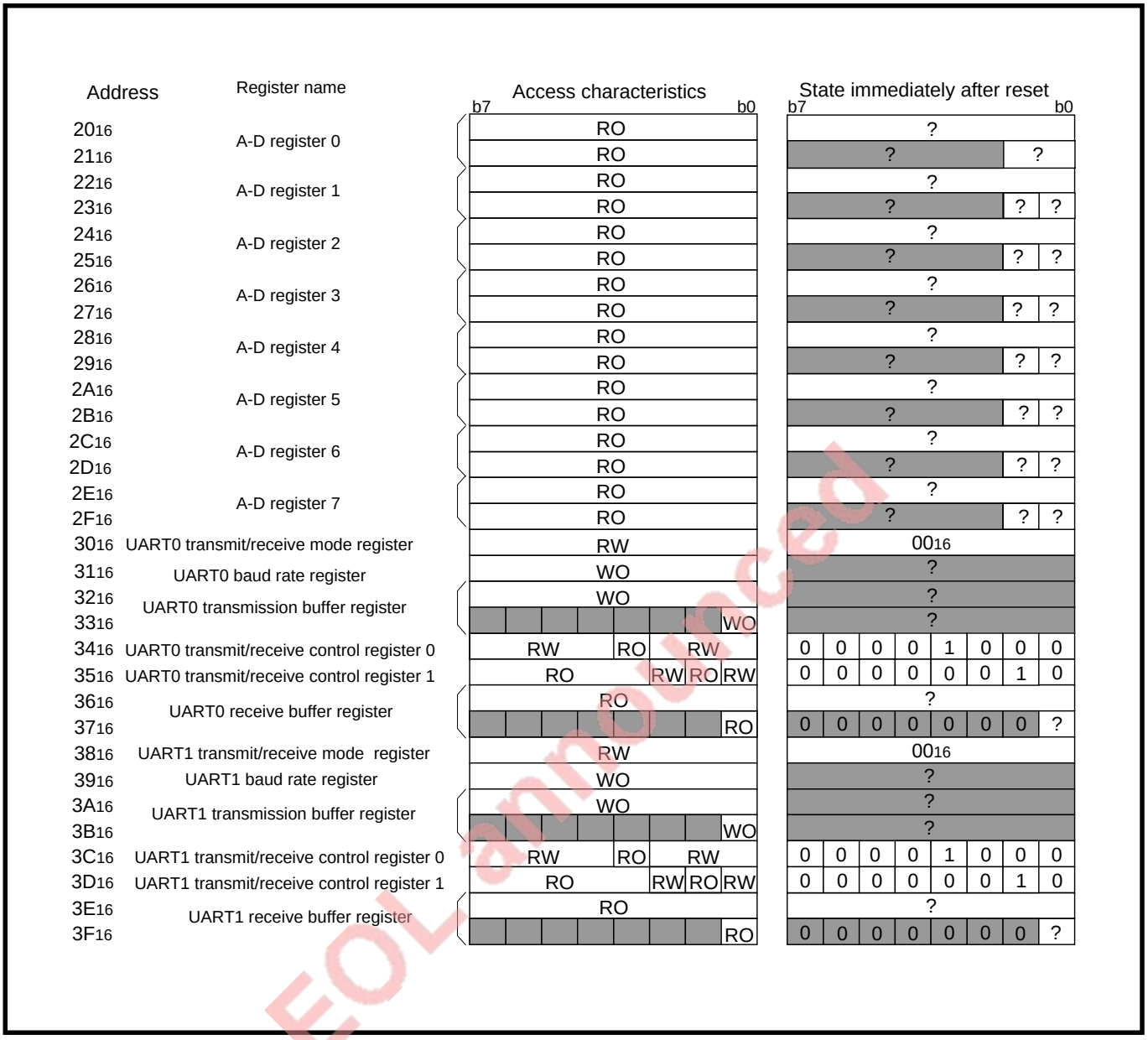


Fig. 13.1.4 State of SFR area and internal RAM area immediately after reset (2)

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
4016	Count start flag	RW	0016
4116			?
4216	One-shot start flag	WO	? 0 0 0 0 0
4316			?
4416	Up-down flag	WO RW	0 0 0 0 0 0 0 0
4516			?
4616	Timer A0 register	✻1	?
4716		✻1	?
4816	Timer A1 register	✻1	?
4916		✻1	?
4A16	Timer A2 register	✻1	?
4B16		✻1	?
4C16	Timer A3 register	✻1	?
4D16		✻1	?
4E16	Timer A4 register	✻1	?
4F16		✻1	?
5016	Timer B0 register	✻1	?
5116		✻1	?
5216	Timer B1 register	✻1	?
5316		✻1	?
5416	Timer B2 register	✻1	?
5516		✻1	?
5616	Timer A0 mode register	RW	0016
5716	Timer A1 mode register	RW	0016
5816	Timer A2 mode register	RW	0016
5916	Timer A3 mode register	RW	0016
5A16	Timer A4 mode register	RW	0016
5B16	Timer B0 mode register	RW ✻2 RW	0 0 ? ? 0 0 0 0
5C16	Timer B1 mode register	RW ✻2 RW	0 0 ? ? 0 0 0 0
5D16	Timer B2 mode register	RW ✻2 RW	0 0 ? ? 0 0 0 0
5E16	Processor mode register 0	RW WO RW ✻3 RW	0 0 0 0 0 0 ✻3 0
5F16	Processor mode register 10	RW	0

EOL announced

✻1 Access characteristics at addresses 4616 to 5516 vary according to the timer's operating mode. (Refer to chapters **"6. TIMER A" and "7. TIMER B."**)

✻2 Access characteristics for bit 5 at addresses 5B16 to 5D16 vary according to the timer B's operating mode. (Refer to chapter **"7. TIMER B."**)

✻3 Access characteristics for bit 1 at address 5E16 and its state immediately after reset vary according to the voltage level applied to pin CNVSS. (Refer to section **"2.5 Processor modes."**)

Fig. 13.1.5 State of SFR area and internal RAM area immediately after reset (3)

RESET

13.1 Hardware reset

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
6016	Watchdog timer register	WO	? (∗1)
6116	Watchdog timer frequency selection flag	RW	? 0
6216	(Reserved area) ∗4		?
6316	Memory allocation control register	RW	? 0 0 0 0 0 0
6416	UART2 transmit/receive mode register	RW	? 0 0 0 0 0 0 0
6516	UART2 baud rate register (BRG2)	WO	?
6616	UART2 transmission buffer register	WO	?
6716		WO	?
6816	UART2 transmit/receive control register 0	RO RW	? 1 0 0 0
6916	UART2 transmit/receive control register 1	RO RW RO RW	0 0 0 0 0 0 1 0
6A16	UART2 receive buffer register	RO	?
6B16		RO	0 0 0 0 0 0 0 ?
6C16	Oscillation circuit control register 0	RW(∗2) RW	? 0 0 0 0 0 ? 1
6D16	Port function control register	RW	0 0 0 0 0 0 0 0
6E16	Serial transmit control register	RW	? 0 0 ?
6F16	Oscillation circuit control register 1	WO RW	0 ? 0 ∗3 0 0 0
7016	A-D / UART2 trans./rece. interrupt control register	RW	? 0 0 0 0
7116	UART0 transmission interrupt control register	RW	? 0 0 0 0
7216	UART0 receive interrupt control register	RW	? 0 0 0 0
7316	UART1 transmission interrupt control register	RW	? 0 0 0 0
7416	UART1 receive interrupt control register	RW	? 0 0 0 0
7516	Timer A0 interrupt control register	RW	? 0 0 0 0
7616	Timer A1 interrupt control register	RW	? 0 0 0 0
7716	Timer A2 interrupt control register	RW	? 0 0 0 0
7816	Timer A3 interrupt control register	RW	? 0 0 0 0
7916	Timer A4 interrupt control register	RW	? 0 0 0 0
7A16	Timer B0 interrupt control register	RW	? 0 0 0 0
7B16	Timer B1 interrupt control register	RW	? 0 0 0 0
7C16	Timer B2 interrupt control register	RW	? 0 0 0 0
7D16	$\overline{INT_0}$ interrupt control register	RW	? 0 0 0 0 0 0
7E16	$\overline{INT_1}$ interrupt control register	RW	? 0 0 0 0 0 0
7F16	$\overline{INT_2}$/Key input interrupt control register	RW	? 0 0 0 0 0 0

∗1 Value "FFF16" is set to the watchdog timer. (Refer to chapter **"10. WATCHDOG TIMER."**)
∗2 For access characteristics at address 6C16, also refer to **Figure 14.3.2.**
∗3 State immediately after reset for bit 3 at address 6F16 vary according to the microcomputer. (Refer to **Figure 14.3.3.**)
∗4 Do not write data to address 6216.

■Internal RAM area (M37733MHBXXXFP: addresses 8016 to FFF16)

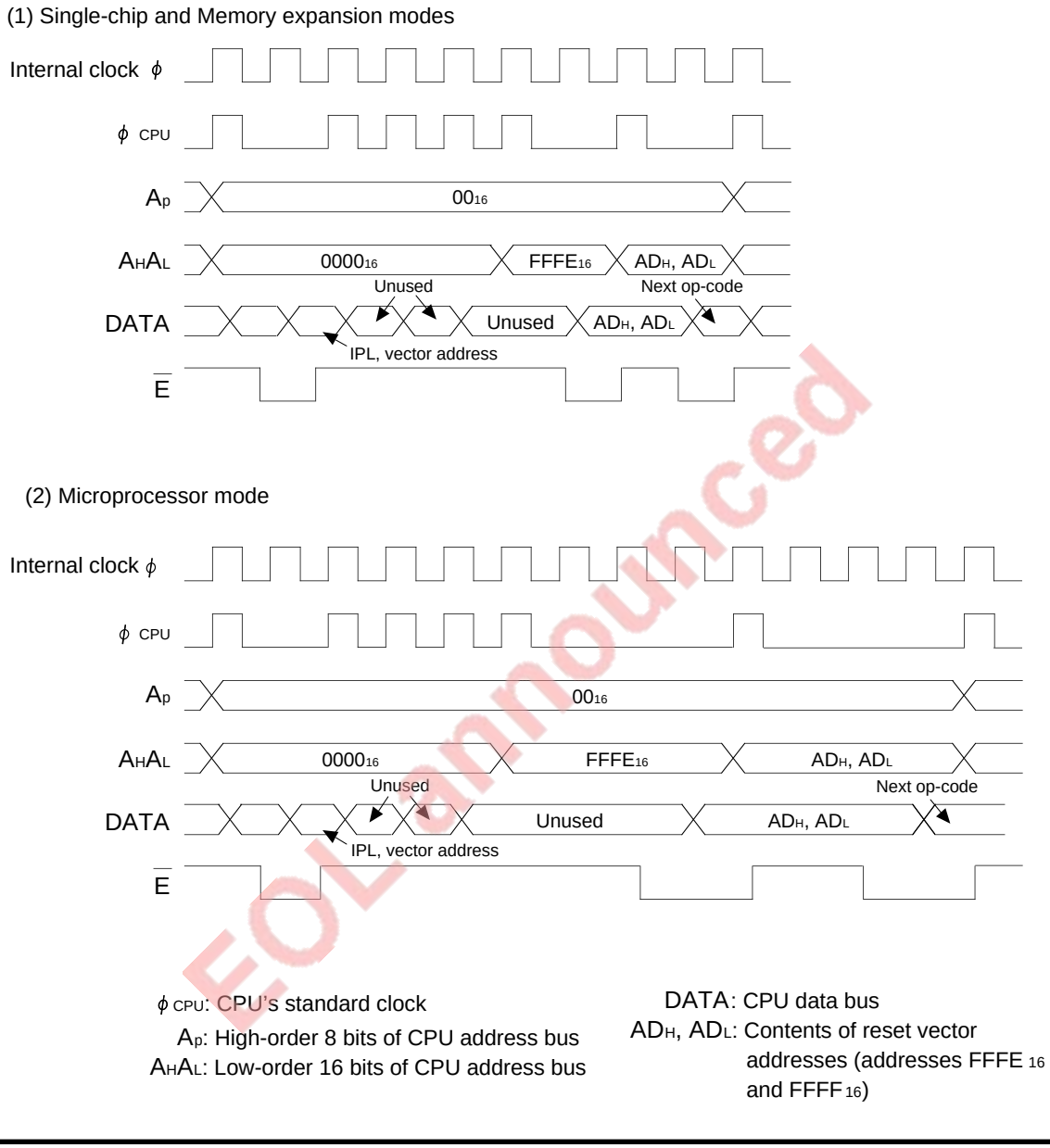
- At hardware reset
  (not including the case where the stop or wait mode is terminated)...Undefined.
- At software reset...Retains the state immediately before reset.
- When the stop or wait mode is terminated
  (when hardware reset is applied)...Retains the state immediately before the **STP** or **WIT** instruction was executed.

EOL announced

Fig. 13.1.6 State of SFR area and internal RAM area immediately after reset (4)

13.1.3 Internal processing sequence after a reset

Figure 13.1.7 shows the internal processing sequence after reset.



EOL announced

Fig. 13.1.7 Internal processing sequence after reset

RESET

13.1 Hardware reset

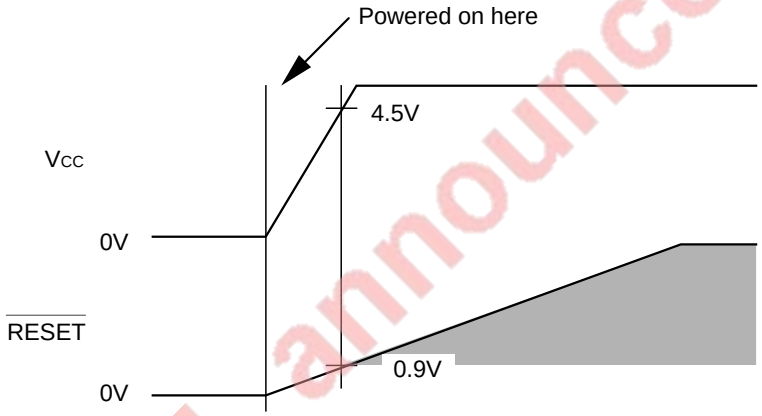
13.1.4 Time required for applying "L" level to pin $\overline{\text{RESET}}$

Time required for applying "L" level to pin $\overline{\text{RESET}}$ varies according to the main clock oscillation circuit's state.

■The case where an oscillator is stably oscillating or an external clock is stably input from pin X_{IN}
Apply "L" level for 2 μs or more.

■The case where an oscillator is not stably oscillating (including the cases where power-on reset is applied and where the microcomputer operates in the stop mode)
Apply "L" level until oscillation is stabilized.
The time required for stabilizing oscillation varies according to the oscillator. For details, contact with the oscillator manufacturer.
Figure 13.1.8 shows power-on reset conditions. Figure 13.1.9 shows an example of a power-on reset circuit.

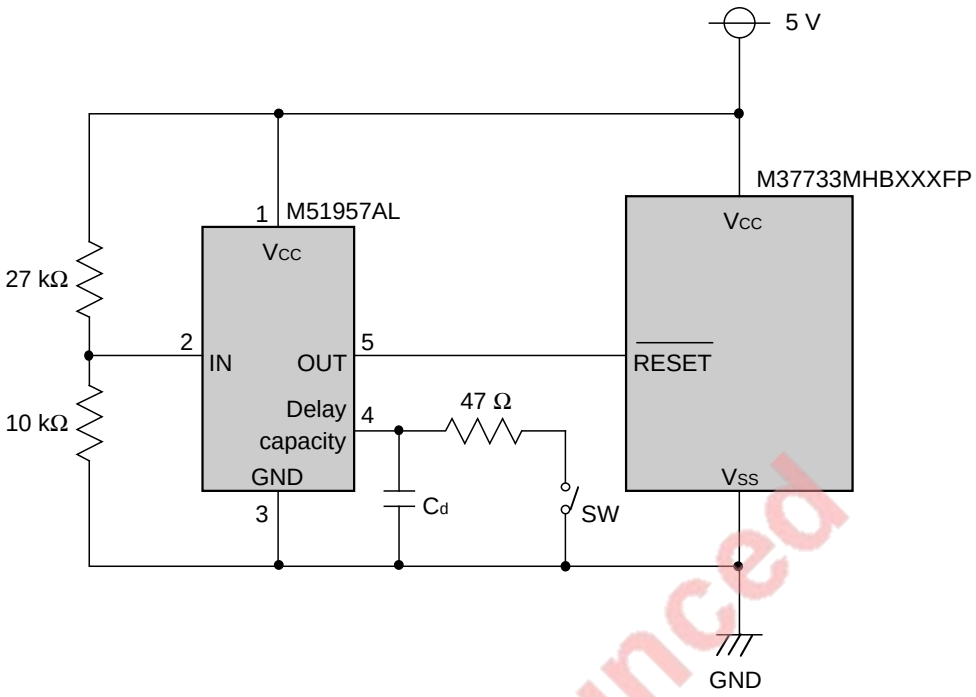
✵ For the stop mode, refer to chapter **"11. STOP MODE AND WAIT MODES."** For clocks, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**



Note: For the low voltage version, refer to **Figure 18.3.1**.

Fig. 13.1.8 Power-on reset conditions

EOL announced



✵ Delay time td is about 11 ms when C_d = 0.033 μF.

$t_d \approx 0.34 \times C_d$ [μs], C_d: [pF]

Note: For the low voltage version, refer to **Figure 18.3.2**.

Fig. 13.1.9 Example of power-on reset circuit

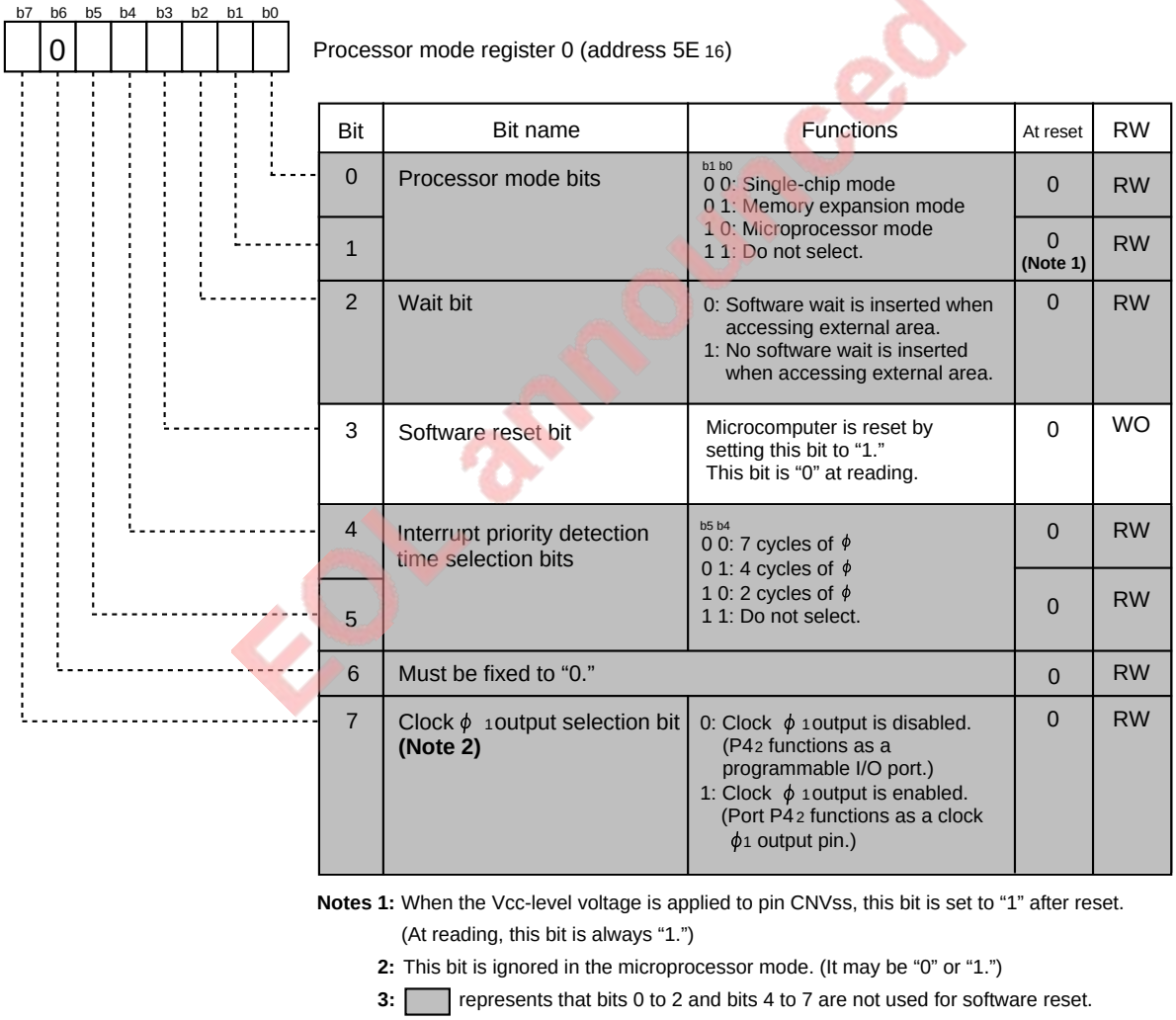
EOL announced

13.2 Software reset

When the power source voltage satisfies the recommended operating conditions and the main clock is stably supplied (**Note**), the microcomputer is reset by writing "1" to the software reset bit (bit 3 at address 5E16). (This is called "Software reset.") In this case, the microcomputer initializes pins, CPU, and SFR area as in the case of a hardware reset. However, the microcomputer retains the contents of the internal RAM area. (Refer to **Table 13.1.1** and **Figures 13.1.2. to 13.1.6.**)

After completing initialization, the microcomputer performs "internal processing sequence after reset." (Refer to **Figure 13.1.7.**) Then, a program is executed beginning with the address set in the reset vector addresses (addresses FFFE16 and FFFF16).

Note: This means "when a oscillator is stably oscillating or when an external clock is stably input from pin XIN." For clocks, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**



Bit	Bit name	Functions	At reset	RW
0	Processor mode bits	b1 b0 0 0: Single-chip mode 0 1: Memory expansion mode 1 0: Microprocessor mode 1 1: Do not select.	0	RW
1			0 **(Note 1)**	RW
2	Wait bit	0: Software wait is inserted when accessing external area. 1: No software wait is inserted when accessing external area.	0	RW
3	Software reset bit	Microcomputer is reset by setting this bit to "1." This bit is "0" at reading.	0	WO
4	Interrupt priority detection time selection bits	b5 b4 0 0: 7 cycles of ϕ 0 1: 4 cycles of ϕ 1 0: 2 cycles of ϕ 1 1: Do not select.	0	RW
5			0	RW
6	Must be fixed to "0."		0	RW
7	Clock ϕ_1 output selection bit **(Note 2)**	0: Clock ϕ_1 output is disabled. (P42 functions as a programmable I/O port.) 1: Clock ϕ_1 output is enabled. (Port P42 functions as a clock ϕ_1 output pin.)	0	RW

Notes 1: When the Vcc-level voltage is applied to pin CNVss, this bit is set to "1" after reset. (At reading, this bit is always "1.")

2: This bit is ignored in the microprocessor mode. (It may be "0" or "1.")

3: ▭ represents that bits 0 to 2 and bits 4 to 7 are not used for software reset.

EOL announced

Fig. 13.2.1 Structure of processor mode register 0

CHAPTER 14

CLOCK GENERATING CIRCUIT

14.1 Overview
14.2 Oscillation circuit example
14.3 Clock control

EOL announced

CLOCK GENERATING CIRCUIT

14.1 Overview

The clock generating circuit is described below.

14.1 Overview

This clock generating circuit includes two oscillation circuits, which are main-clock and sub-clock oscillation circuits. Each of the main and sub clocks can be used as an operating clock for the CPU, internal peripheral devices, and clock timer.

Table 14.1.1 Main-clock and sub-clock oscillation circuits

	Main-clock oscillation circuit	Sub-clock oscillation circuit
Usage of clock	• Operating clock source of CPU • Operating clock source of internal peripheral devices • Operating clock source of clock timer	
Resonator/Oscillator which can be connected	• Ceramic resonator • Quartz-crystal oscillator	Quartz-crystal oscillator
Pins which are connected to resonator/oscillator	Pins XIN and XOUT	Pins XCIN and XCOUT
Oscillation stop/restart **(Note 2)**	Available	Not available
Oscillator's state just after reset	Operating	Stopped **(Note 1)**
Remarks	A clock which is externally generated can be input.	• A clock which is externally generated can be input. • Sub clock can be input to external devices. (Refer to **14.3.1.**)

Notes 1: Immediately after reset, pins XCIN and XCOUT function as ports P7$_7$ and P7$_6$, respectively. The oscillator starts operating when pins' function is switched by the port-XC selection bit (bit 4 at address 6C$_{16}$).

2: Whether oscillation is stopped or restarted is set by the main clock stop bit (bit 2 at address 6C$_{16}$). In the main-clock/sub-clock oscillation circuit, oscillation can be stopped by the **STP** instruction; oscillation can be restarted by an interrupt request generated. (Refer to **Figure 14.3.9.**)

EOL announced

14.2 Oscillation circuit example

Main-clock and sub-clock oscillation circuits' examples are described below.

14.2.1 Main-clock oscillation circuit example

To the main-clock oscillation circuit, a resonator/ oscillator can be connected, or a clock which is externally generated can be input.

(1) Connection example of resonator/oscillator

Figure 14.2.1 shows an example where pins XIN and XOUT connect across a ceramic resonator/quartz-crystal oscillator.

Circuit constants such as Rf, Rd, CIN, and COUT (shown in Figure 14.2.1) depend on the resonator/oscillator. These values shall be set to the resonator/oscillator manufacturer's recommended values.

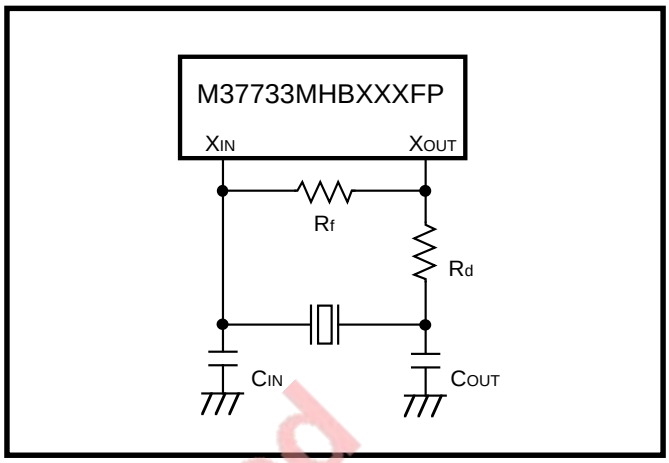


Fig. 14.2.1 Connection example of resonator/oscillator

(2) Input example of clock which is externally generated

Figure 14.2.2 shows an input example of a clock which is externally generated.

When inputting a main clock from an external circuit, set "1" to bit 1 of the main-clock oscillation circuit control register 1. (Refer to **Figure 14.3.3.**) By this setting, the main-clock oscillation circuit stops operating and power consumption can be held down. Note that this bit has a function to select return conditions from the stop mode. (Refer to chapter **"11. STOP AND WAIT MODES."**) Furthermore, when writing to the oscillation circuit control register 1, follow the procedure shown in Figure 14.3.4.

When inputting a main clock from an external circuit, that the external clock must be input from pin XIN, and pin XOUT must be left open.

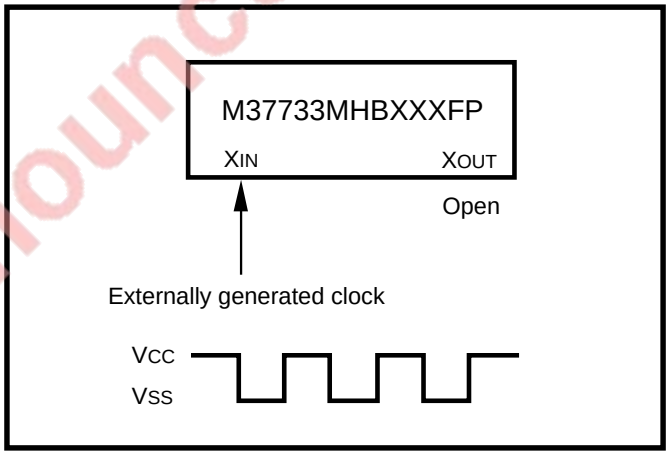


Fig. 14.2.2 Externally generated clock input example

Not announced

CLOCK GENERATING CIRCUIT

14.2 Oscillation circuit example

14.2.2 Sub-clock oscillation circuit example

To the Sub-clock oscillation circuit, an oscillator can be connected, or a clock which is externally generated can be input.

(1) Connection example of oscillator

When using an oscillator, connect a quartz-crystal oscillator between pins XCIN and XCOUT. (A ceramic resonator cannot be connected.) Figure 14.2.3 shows a quartz-crystal oscillator connection example.

Circuit constants such as Rcf, Rcd, CCIN, and CCOUT (shown in Figure 14.2.3) depend on the oscillator. These values shall be set to the oscillator manufacturer's recommended values.

When connecting an oscillator to the sub-clock oscillation circuit, set the port-Xc selection bit (bit 4 at address $6C_{16}$) to "1" and the sub clock external input selection bit (bit 2 at address $6F_{16}$) to "0." Note that the sub clock external input selection bit has a function to select return conditions from the stop mode. (Refer to chapter **"11. STOP AND WAIT MODES."**)

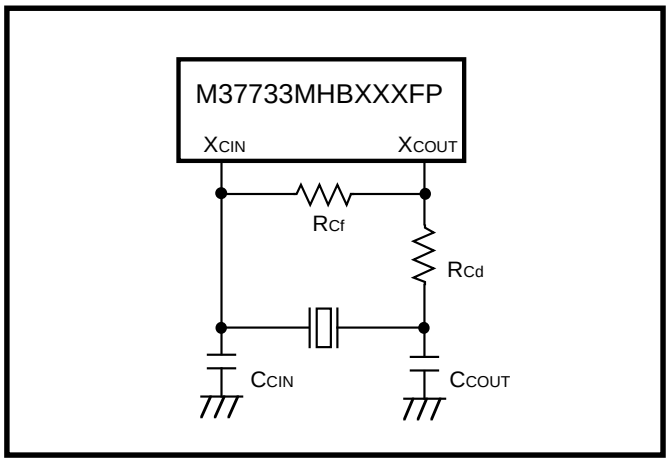


Fig. 14.2.3 Connection example of quartz-crystal oscillator

(2) Input example of clock which is externally generated

Figure 14.2.4 shows an input example of a clock which is generated in an external circuit.

When inputting a sub clock from an external circuit, be sure to set the sub clock external input selection bit to "1," and then, select pins XCIN and XCOUT by the port-Xc selection bit.

In this case, an externally generated clock is input to pin XIN, and pin XOUT functions as pin $P7_6$/AN_6. Note that the sub clock external input selection bit has a function to select return conditions from the stop mode. (Refer to chapter **"11. STOP AND WAIT MODES."**)

If the sub-clock output selection bit (bit 1 at address $6D_{16}$) is set to "1" when the port-Xc selection bit = "1" **(Note)**, sub clock ϕ_{SUB} is output from port $P6_7$. Accordingly, a 32-kHz sub clock can be supplied to external gates.

Note: At this time, a sub clock is used.

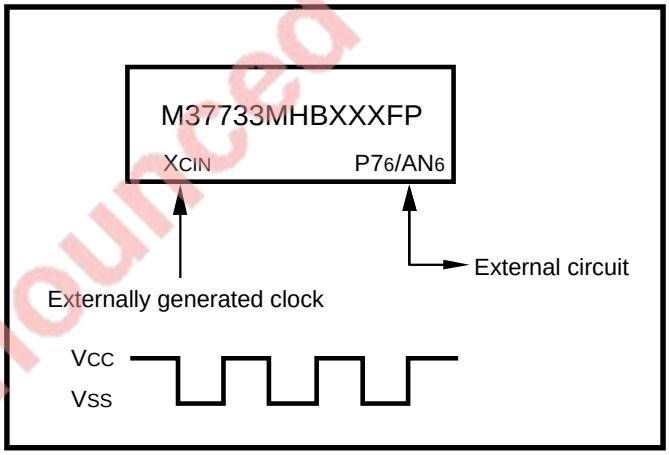


Fig. 14.2.4 Externally generated clock input example

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14.3 Clock control

Figure 14.3.1 shows the clock generating circuit block diagram.

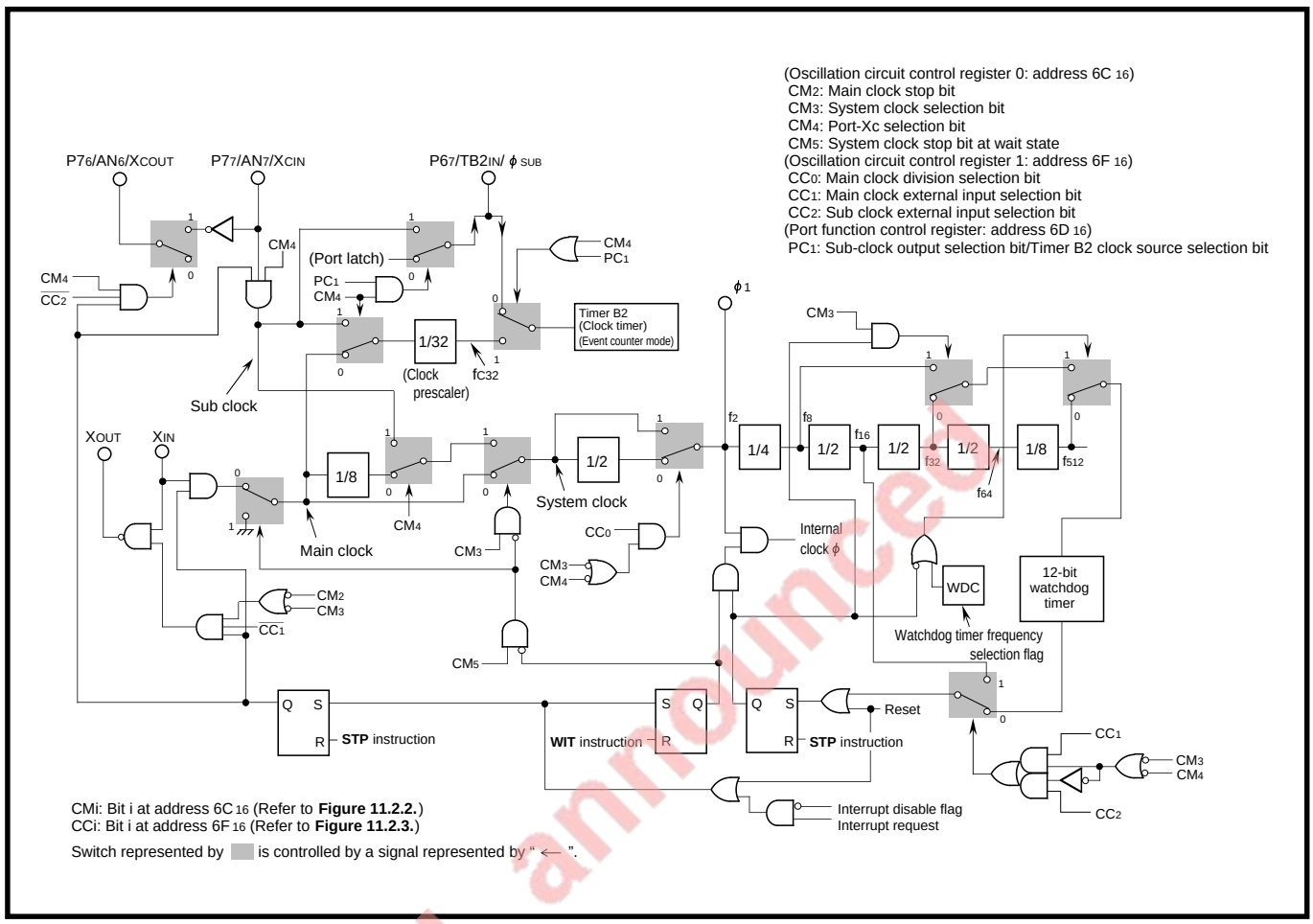

Fig. 14.3.1 Clock generating circuit block diagram

EOL announced

CLOCK GENERATING CIRCUIT

14.3 Clock control

14.3.1 Clock generated in clock generating circuit

(1) System clock

It is the clock source of the system clock divided by 2, internal clock ϕ, clock ϕ_1, and clocks f_2 to f_{512}. (Refer to **Figure 14.3.1.**) Each of the main clock, main clock divided by 8, and the sub clock can be selected as the system clock by the system clock selection bit (bit 3 at address $6C_{16}$). Table 14.3.1 lists clock combinations of the system clock, internal clock ϕ, ϕ_1, and f_2.

Table 14.3.1 Clock combinations of system clock, internal clock ϕ, ϕ_1, and f_2

Port-Xc selection bit (bit 4 at 6C16)	System clock selection bit (bit 3 at $6C_{16}$)	Main clock division selection bit (bit 0 at $6C_{16}$)	System clock	Internal clock ϕ, ϕ_1, f_2
0 (Sub clock is not used.)	0	0	Main clock	Main clock divided by 2
		1	Main clock	Main clock
	1	0	Main clock divided by 8	Main clock divided by 16
		1	Main clock divided by 8	Main clock divided by 8
1 (Sub clock is used.)	0	0	Main clock	Main clock divided by 2
		1	Main clock	Main clock
	1	0	Sub clock	Sub clock divided by 2
		1		

(2) Main clock

It is the clock supplied by the main-clock oscillation circuit. This clock is selected as the system clock immediately after reset.

After the sub clock is selected as the system clock, the main-clock supply is stopped/restarted by the main clock stop bit (bits 2 at address $6C_{16}$). (Refer to **Figures 14.3.6 and 14.3.7.**)

By stopping the main-clock supply, power consumption can be held down.

Figure 14.3.5 shows the clock f_2 state transition when a sub clock is not used because the port-Xc selection bit (bit 4 at address $6C_{16}$) = "0." During reset and till after reset state is terminated, the main clock divided by 2 is selected as clock f_2. If the system clock selection bit (bit 3 at address $6C_{16}$) is set to "1," at this time, the main clock divided by 16 is selected as clock f_2, and the clock frequency which is supplied to the CPU and peripheral devices becomes 1/8. Though this slow down the processing speed, current consumption is held down. Furthermore, by setting "1" to both of the main clock division selection bit (bit 0 at address $6F_{16}$) and system clock selection bit, the main clock divided by 8 is selected as clock f_2.

When the port-Xc selection bit = "0," clock f_{C32}, which is the main clock divided by 32, is connected as the timer B2's count source if the timer B2 clock source selection bit (bit 1 at address $6D_{16}$) = "1" and timer B2 is used as a clock timer. By this, even when the main clock's ratio is changed, the clock timer can use the same clock source. (Refer to **Figure 14.3.1.**)

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(3) Sub clock

It is the clock supplied by the sub-clock oscillation circuit. The sub-clock supply is stopped immediately after reset (**Note**). When the port-Xc selection bit (bit 4 at address $6C_{16}$) is set to "1," the sub-clock oscillation circuit starts operating, in other words, oscillation starts or an external clock is input. Furthermore, in this case, f_{C32} (sub clock divided by 32) is connected. (Refer to section **"7.6 Clock timer."**)

Furthermore, a sub clock can be the system clock by specifying the system clock selection bit after the oscillation is stabilized. (Refer to **Figure 14.3.6.**)

The X_{COUT} pin's drivability can be lowered by the X_{COUT} drivability selection bit (bit 0 at address $6C_{16}$) after oscillation of the sub-clock oscillation circuit is stabilized.

By lowering the X_{COUT} pin's drivability, power consumption is held down.

When a sub clock is used, in other words, bit 4 at address $6C_{16}$ = "1," sub clock ϕ_{SUB} is output from pin $P6_7$/$TB2_{IN}$/ϕ_{SUB} if the sub-clock output selection bit (bit 1 at address $6D_{16}$) is set to "1."

Note: At this time, the oscillator which is connected to the sub-clock oscillation circuit stops operating, and pins X_{CIN} and X_{COUT} function as ports $P7_6$ and $P7_7$.

(4) Internal clock ϕ

It is the CPU's operating clock source, and its clock source is the system clock.

(5) Clocks f_2 to f_{512}

Each of them is the internal peripheral devices' operating clock, and its clock source is the system clock.

(6) Clock ϕ_1

It is output to external circuits and has the same period as internal clock ϕ, and its clock source is the system clock.

(7) f_{C32}

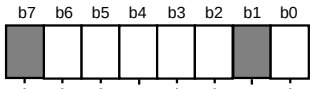
It is the main clock/sub clock divided by 32 (Refer to **Figure 14.3.1.**) and the count source of the clock timer. (Refer to **"7.6 Clock timer."**)

(8) Sub clock ϕ_{SUB}

Sub clock ϕ_{SUB} is output from port $P6_7$ if the sub clock output selection bit (bit 1 at address $6D_{16}$) is set to "1" when the port Xc selection bit = "1," in other words, when the sub clock is used. Therefore, the 32-kHz sub clock can be supplied to the external gate.

EOL announced

14.3 Clock control



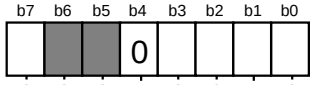
Oscillation circuit control register 0 (address 6C 16)

Bit	Bit name	Functions	At reset	RW
0	X_{COUT} drivability selection bit	0: Drivability "LOW" 1: Drivability "HIGH"	1	RW (**Note 1**)
1	Not implemented.		Un-defined	–
2	Main clock stop bit	0: Main clock oscillation or external clock input is available. 1: Main clock oscillation or external clock input is stopped.	0	RW (**Note 1**)
3	System clock selection bit	When the port-Xc selection bit = "0," 0: Main clock 1: Main clock divided by 8 When the port-Xc selection bit = "1," 0: Main clock 1: Sub clock	0	RW (**Note 2**)
4	Port-Xc selection bit	0: Operate as I/O ports ($P7_7$, $P7_6$). 1: Operate as pins X_{CIN} and X_{COUT}.	0	RW (**Notes 2 and 3**)
5	System clock stop bit at wait state **(Note 4)**	0: Operates in the wait mode. 1: Stopped in the wait mode.	0	RW
6	Signal output disable selection bit	0: Output is enabled. (Refer to **Tables 12.1.2 and 12.1.5**) 1: Output is disabled.	0	RW
7	Not implemented.		Un-defined	–

Notes 1: Nothing can be written to this bit after reset. Writing to this bit is enabled when the port-Xc selection bit = "1."
2: When selecting the sub clock as the system clock, set bit 3 to "1" after setting bit 4 to "1." If the above settings are performed simultaneously, in other words, performed by executing only one instruction, only bit 3 is set to "1."
3: Although this bit can be set to "1," it cannot be cleared to "0" after this bit is once set to "1."
4: When setting the system clock stop bit at wait state to "1," perform it immediately before the **WIT** instruction is executed. Furthermore, clear this bit to "0" immediately after the wait mode is terminated.

Announced

Fig. 14.3.2 Structure of oscillation circuit control register 0



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 3)**	Ignored in the mask ROM and external ROM versions.		0	RW
	Must be fixed to "1" in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to "0" **(Note 2)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing "1" to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 14.3.4.
2: The case where data "01010101_2" is written with the procedure shown in Figure 14.3.4 is not included.
3: In the 7735 Group, fix this bit to "0."
4: ☐ represents that bits 3 to 7 are not used for the clock generating circuit

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Fig. 14.3.3 Structure of oscillation circuit control register 1

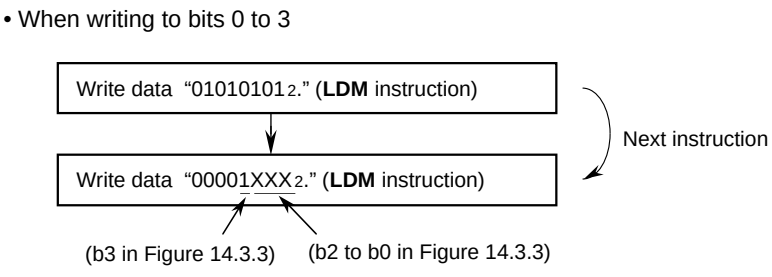

Fig. 14.3.4 Procedure for writing data to oscillation circuit control register 1

CLOCK GENERATING CIRCUIT

14.3 Clock control

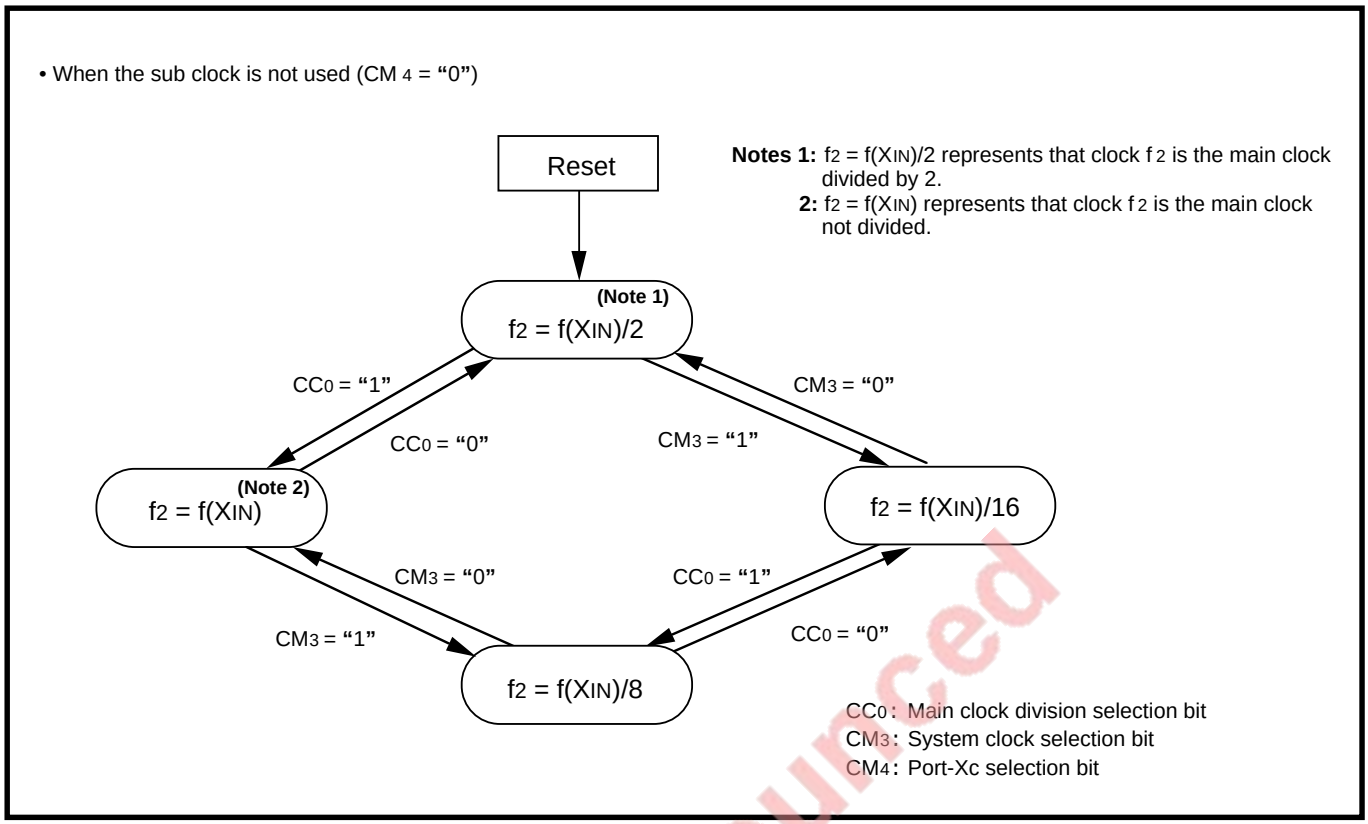

Fig. 14.3.5 Clock f2 state transition (when sub clock is not used)

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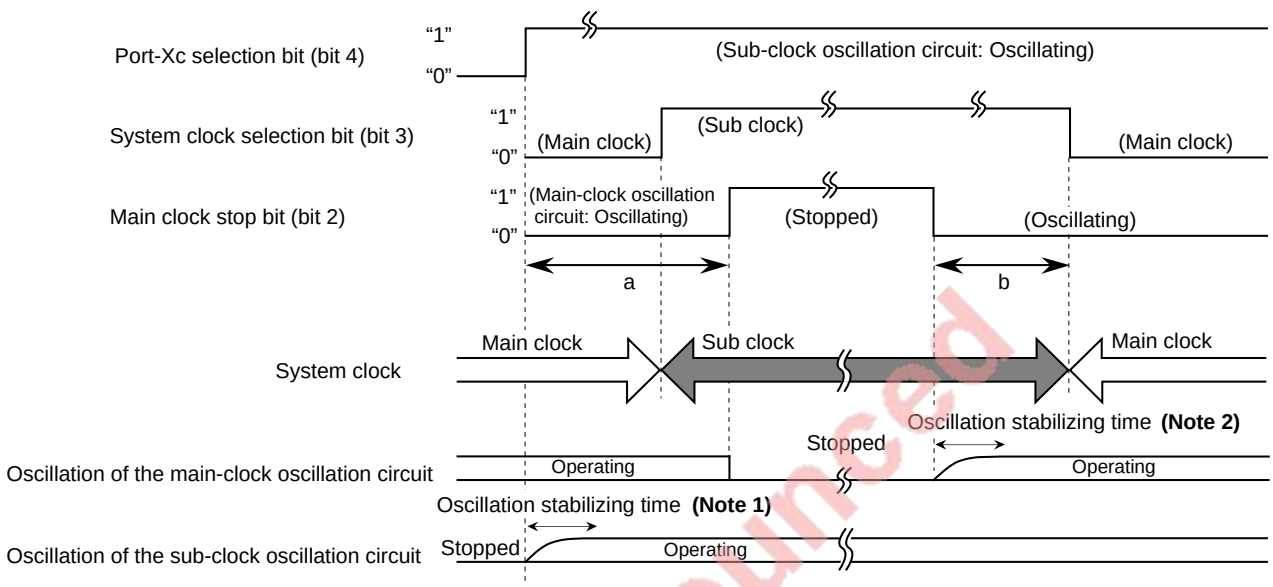
14.3.2 System clock switching procedure

Figures 14.3.6 to 14.3.8 show the system clock switching procedure.

■ State of bits 4 to 1 of the oscillation circuit control register 0 when switching the system clock



Notes 1: Before selecting the sub clock, make sure that oscillation of the sub clock is fully stabilized after oscillation starts.
2: Before selecting the main clock, make sure that oscillation of the main clock is fully stabilized after oscillation restarts.

Fig. 14.3.6 System clock switching procedure (1)

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CLOCK GENERATING CIRCUIT

14.3 Clock control

■ System clock switching procedure in order to stop the main clock supply when oscillator connected to the sub-clock oscillation circuit stops operating. (Refer to **"a" in Figure 14.3.6.**)

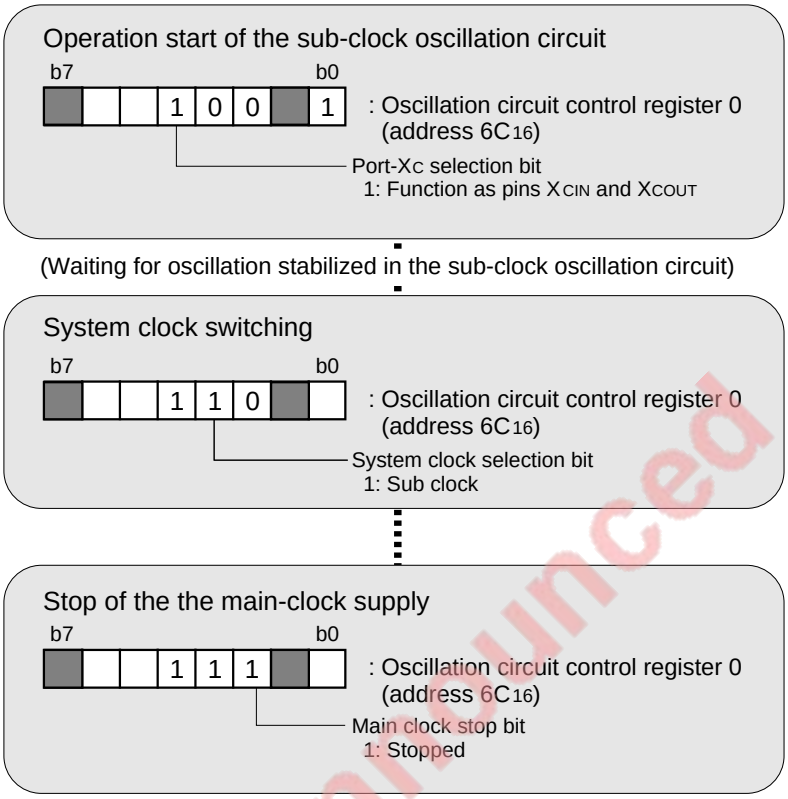

Fig. 14.3.7 System clock switching procedure (2)

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■System clock switching procedure in order to select the main clock as the system clock when the main clock supply stops. (Refer to **"b" in Figure 14.3.6.**)

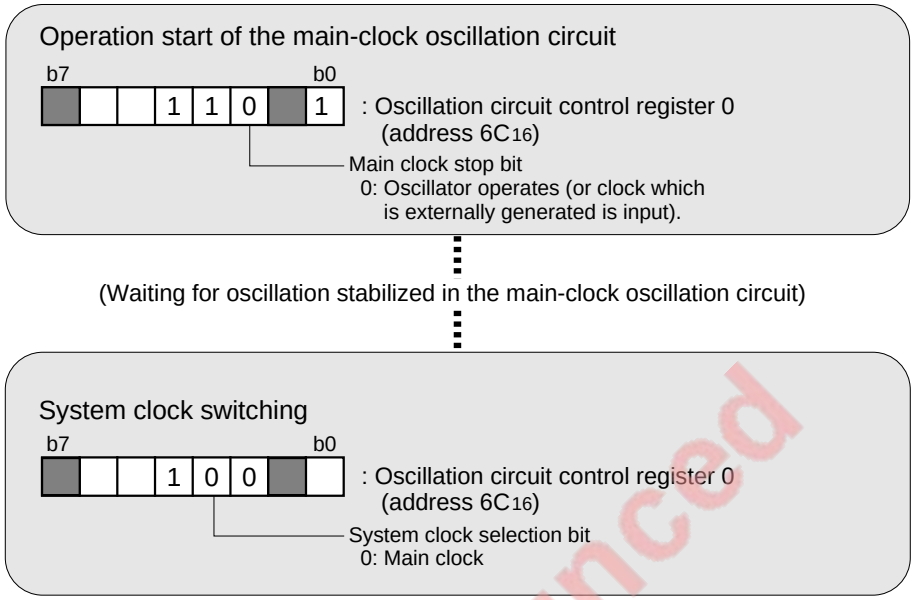

Fig. 14.3.8 System clock switching procedure (3)

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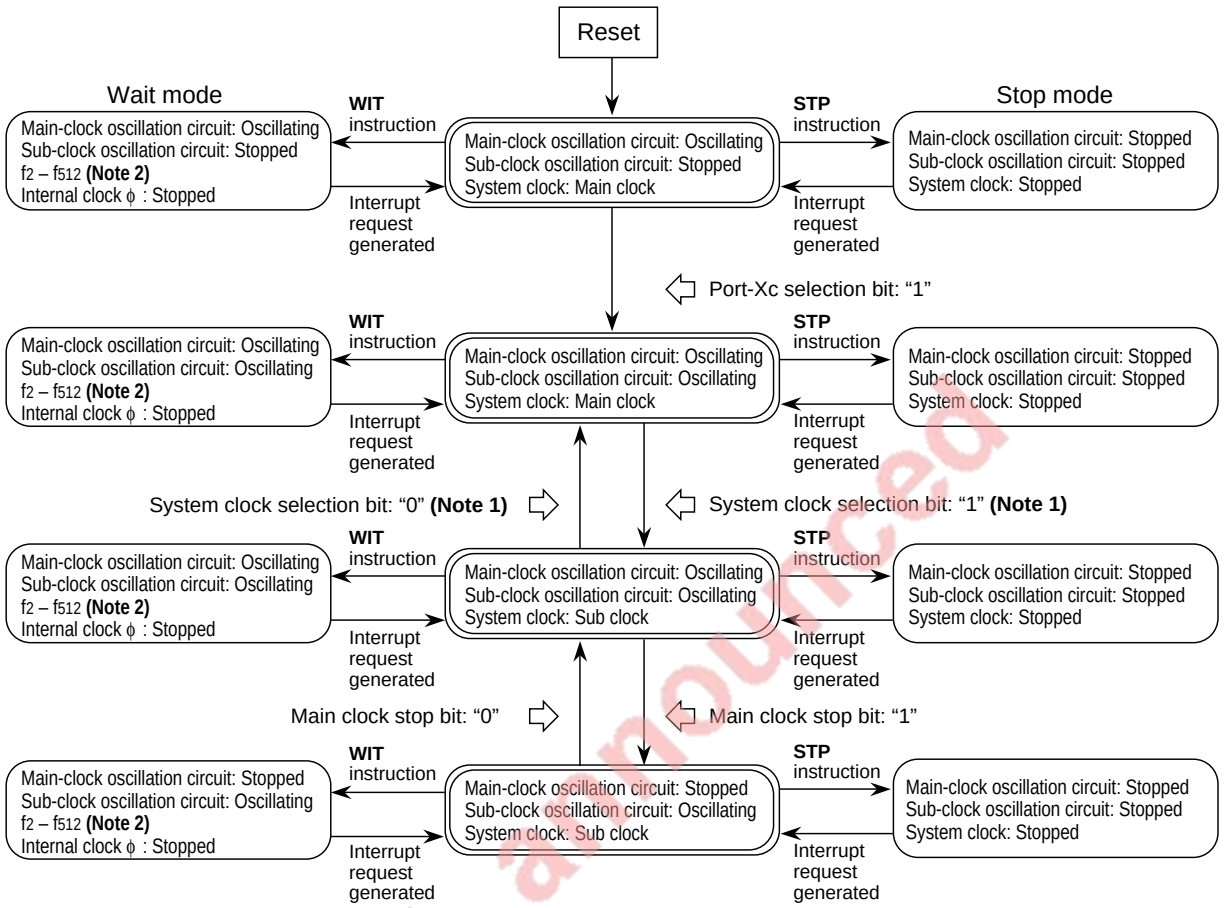
CLOCK GENERATING CIRCUIT

14.3 Clock control

14.3.3 Clock transition

Figure 14.3.9 shows the clock transition.



✺ For the stop and wait modes, refer to chapter **"11. STOP AND WAIT MODES."**

Notes 1: Before selecting the system clock, make sure that operation of the oscillator is fully stabilized. Additionally, generate oscillation stabilizing time by software.

2: In the wait mode, whether clocks f2 to f512 are supplied or stopped can be specified by the system clock stop bit at wait state.

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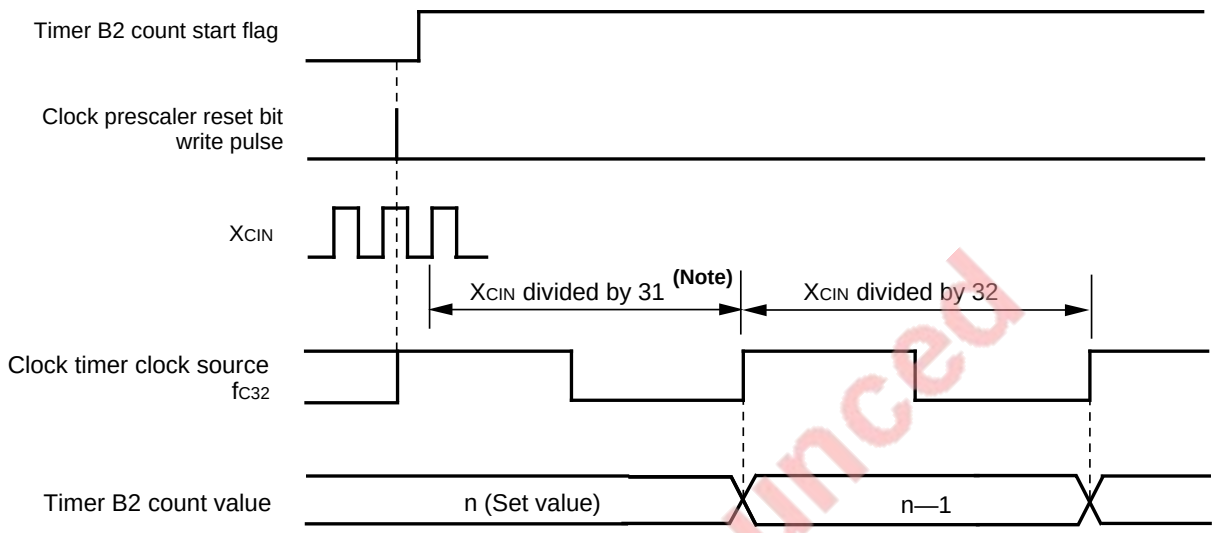
Fig. 14.3.9 Clock transition

14.3.4 Clock prescaler reset

The clock prescaler, which divides a sub clock by 32, is reset by writing “1” to the clock prescaler reset bit (bit 7 at address $6F_{16}$). By this function, the count source (f_{C32}) error immediately after the clock timer starts counting can be held down. Figure 14.3.10 shows the operation timing of the clock prescaler and timer B2.



The above is applied when the main clock is selected as the system clock, in other words, when the system clock selection bit
(CM_3) = “0.”

Note: Only in this period, X_{CIN} divided by 31 is selected.
After this period, X_{CIN} divided by 32 is selected.

Figure 14.3.10 Operation timing of clock prescaler and timer B2

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Memo

EOL announced

CHAPTER 15

ELECTRICAL CHARACTERISTICS

EOL announced

15.1 Absolute maximum ratings
15.2 Recommended operating conditions
15.3 Electrical characteristics
15.4 A-D converter characteristics
15.5 Internal peripheral devices
15.6 Ready and Hold
15.7 Single-chip mode
15.8 Memory expansion mode and Microprocessor mode : with no wait
15.9 Memory expansion mode and Microprocessor mode : with wait 1
15.10 Memory expansion mode and Microprocessor mode : with wait 0
15.11 Measuring circuit for ports P0 to P8 and pins ϕ_1 and $\overline{E}$

ELECTRICAL CHARACTERISTICS

15.1 Absolute maximum ratings

M37733MHBXXXFP's electrical characteristics are described below.
For low voltage version, refer to section **"18.4 Electrical characteristics."**
For the latest data, inquire of addresses described last (☞**"CONTACT ADDRESSES FOR FURTHER INFORMATION")** .

15.1 Absolute maximum ratings

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to 7	V
AVcc	Analog power source voltage		–0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to 12	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, V_{REF}, X_{IN}		–0.3 to Vcc+0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}, $\overline{E}$		–0.3 to Vcc+0.3	V
P_d	Power dissipation	Ta = 25 °C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 150	°C

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15.2 Recommended operating conditions

Recommended operating conditions (Vcc = 5 V ± 10 %, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Power source voltage	$f(X_{IN})$:Operating	4.5	5.0	5.5	V
		$f(X_{IN})$:Stopped, $f(X_{CIN})$ = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} **(Note 3)**	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} **(Note 3)**	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0		0.16 Vcc	V
$I_{OH\ (peak)}$	High-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–10	mA
$I_{OH\ (avg)}$	High-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–5	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			10	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P4_4$–$P4_7$, $P5_0$–$P5_3$			20	mA
$I_{OL\ (avg)}$	Low-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			5	mA
$I_{OL\ (avg)}$	Low-level average output current	$P4_4$–$P4_7$, $P5_0$–$P5_3$			15	mA
$f(X_{IN})$	Main-clock oscillation frequency **(Note 4)**				25	MHz
$f(X_{CIN})$	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1: Average output current is the average value of a 100 ms interval.

2: The sum of I_{OL}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL}(peak) for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I_{OH}(peak) for ports P4, P5, P6, and P7 must be 80 mA or less.

3: Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1."

4: The maximum value of $f(X_{IN})$ = 12.5 MHz when the main clock division selection bit = "1."

EOL announced

ELECTRICAL CHARACTERISTICS

15.3 Electrical characteristics

Electrical characteristics (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz, unless otherwise noted)

Symbol	Parameter		Measuring conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OH} = –10 mA	3			V
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	I_{OH} = –400 μA	4.7			V
V_{OH}	High-level output voltage	$P3_0$–$P3_2$	I_{OH} = –10 mA	3.1			V
			I_{OH} = –400 μA	4.8			
V_{OH}	High-level output voltage	$\overline{E}$	I_{OH} = –10 mA	3.4			V
			I_{OH} = –400 μA	4.8			
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_5$, $P8_0$–$P8_7$	I_{OL} = 10 mA			2	V
V_{OL}	Low-level output voltage	$P4_4$–$P4_7$, $P5_0$–$P5_3$	I_{OL} = 20 mA			2	V
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	I_{OL} = 2 mA			0.45	V
V_{OL}	Low-level output voltage	$P3_0$–$P3_2$	I_{OL} = 10 mA			1.9	V
			I_{OL} = 2 mA			0.43	
V_{OL}	Low-level output voltage	$\overline{E}$	I_{OL} = 10 mA			1.6	V
			I_{OL} = 2 mA			0.4	
V_{T+}–V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$–$TA4_{IN}$, $TB0_{IN}$–$TB2_{IN}$, $\overline{INT_0}$–$\overline{INT_2}$, $\overline{ADTRG}$, $\overline{CTS_0}$, $\overline{CTS_1}$, $\overline{CTS_2}$, CLK_0, CLK_1, CLK_2, $\overline{KI_0}$–$\overline{KI_3}$		0.4		1	V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$		0.2		0.5	V
V_{T+}–V_{T-}	Hysteresis	X_{IN}		0.1		0.4	V
V_{T+}–V_{T-}	Hysteresis	X_{CIN} (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I = 5 V			5	μA
I_{IL}	Low-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, $P6_5$– $P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I = 0 V			–5	μA
I_{IL}	Low-level input current	$P5_4$–$P5_7$, $P6_2$–$P6_4$	V_I = 0 V, without a pull-up transistor			–5	μA
			V_I = 0 V, with a pull-up transistor	–0.25	–0.5	–1.0	mA
V_{RAM}	RAM hold voltage		When clock is stopped	2			V

Announced

ELECTRICAL CHARACTERISTICS (Vcc= 5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	In single-chip mode, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, f(X_{IN}) = 25 MHz (Square waveform), (f(f_2) = 12.5 MHz), f(X_{CIN}) = 32.768 kHz, in operating **(Note 1)**		9.5	19	mA
			Vcc = 5V, f(X_{IN}) = 25 MHz (Square waveform), (f(f_2) = 1.5625 MHz), f(X_{CIN}) : Stopped, in operating **(Note 1)**		1.3	2.6	mA
			Vcc = 5V, f(X_{IN}) = 25 MHz (Square waveform), f(X_{CIN}) = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		10	20	μA
			Vcc = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, in operating **(Note 3)**		50	100	μA
			Vcc = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		5	10	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop selection bit at wait state = "1."

3: This is applied when the CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

EOL announced

15.4 A-D converter characteristics

A-D CONVERTER CHARACTERISTICS (Vcc = AVcc = 5 V, Vss = AVss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note)**, unless otherwise noted)

Symbol	Parameter	Measuring conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF} = Vcc			10	Bits
—	Absolute accuracy	V_{REF} = Vcc			± 3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = Vcc	10		25	kΩ
t_{CONV}	Conversion time		9.44			μs
V_{REF}	Reference voltage		2		Vcc	V
V_{IA}	Analog input voltage		0		V_{REF}	V

Note: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.

15.5 Internal peripheral devices

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	80		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	40		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time **(Note 3)**	$\frac{8 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	320		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width **(Note 3)**	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	160		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width **(Note 3)**	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	160		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	320		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width		80		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	80		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} input high-level pulse width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} input low-level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	400		ns

Notes 1: This is applied when the main clock division selection bit = “0” and f(f_2) = 12.5 MHz.

2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

3: The TAi_{IN} input cycle time must be 4 cycles of a count source or more.
The TAi_{IN} input high-level pulse width and low-level pulse width must be 2 cycles of a count source or more, respectively.

EOL announced

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Measuring conditions	Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAj_{IN} input cycle time	$f(X_{IN})$ = 8 MHz	800		ns
		$f(X_{IN})$ = 16 MHz	800		ns
		$f(X_{IN})$ = 25 MHz	800		ns
$t_{su(TAj_{IN}-TAj_{OUT})}$	TAj_{IN} input setup time	$f(X_{IN})$ = 8 MHz	500		ns
		$f(X_{IN})$ = 16 MHz	250		ns
		$f(X_{IN})$ = 25 MHz	200		ns
$t_{su(TAj_{OUT}-TAj_{IN})}$	TAj_{OUT} input setup time	$f(X_{IN})$ = 8 MHz	500		ns
		$f(X_{IN})$ = 16 MHz	250		ns
		$f(X_{IN})$ = 25 MHz	200		ns

Note: This is applied when the main clock division selection bit = “0.”

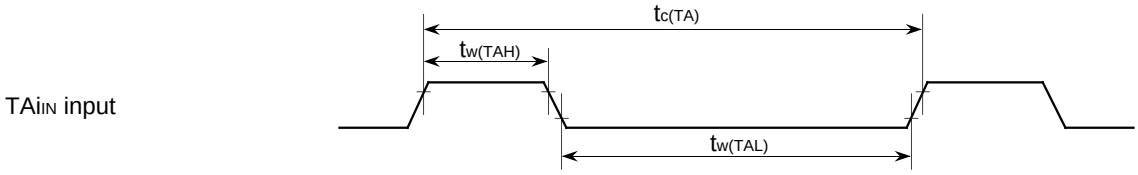
EOL announced

ELECTRICAL CHARACTERISTICS

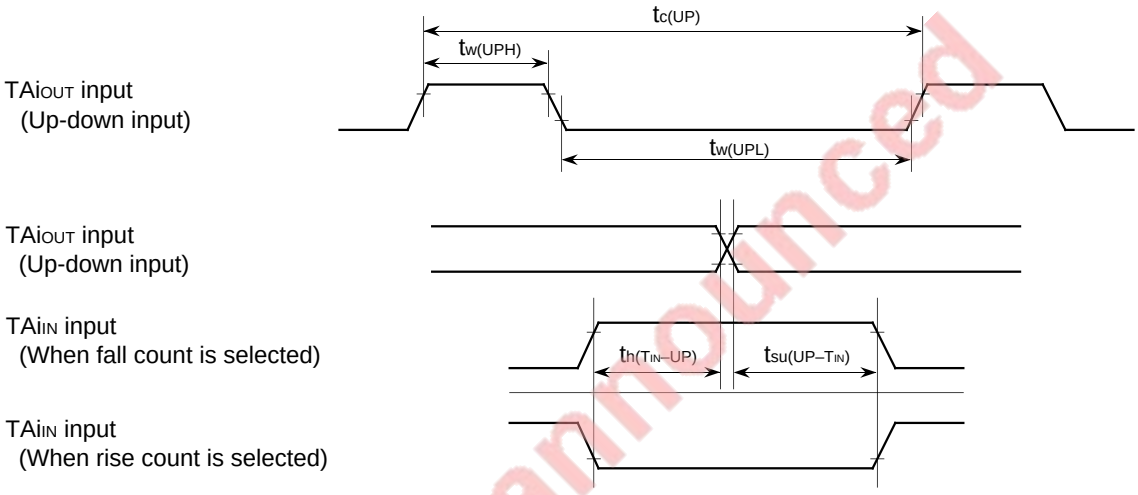
15.5 Internal peripheral devices

Internal peripheral devices

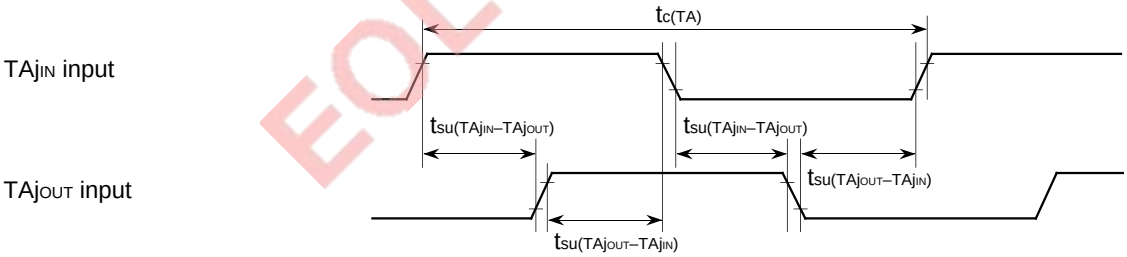
●Count input in event counter mode
●Gating input in timer mode
●External trigger input in one-shot pulse mode
●External trigger input in pulse width modulation mode



●Up-down input and count input in event counter mode



●Two-phase pulse input in event counter mode



EOL announced

Measuring conditions

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (One edge count)	80		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (One edge count)	40		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (One edge count)	40		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (Both edges count)	160		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Both edges count)	80		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time **(Note 1)**	$\frac{8 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	320		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width **(Note 1)**	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	160		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width **(Note 1)**	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	160		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	320		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	160		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	160		ns

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ input cycle time (Minimum allowable trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK_i input cycle time	200		ns
$t_{w(CKH)}$	CLK_i input high-level pulse width	100		ns
$t_{w(CKL)}$	CLK_i input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxD_i output delay time		80	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	30		ns
$t_{h(C-D)}$	RxD_i input hold time	90		ns

Notes 1: The TBi_{IN} input cycle time must be 4 cycles of a count source or more.
The TBi_{IN} input high-level pulse width and low-level pulse width must be 2 cycles of a count source or more, respectively.

2: $f(f_2)$ represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

EOL announced

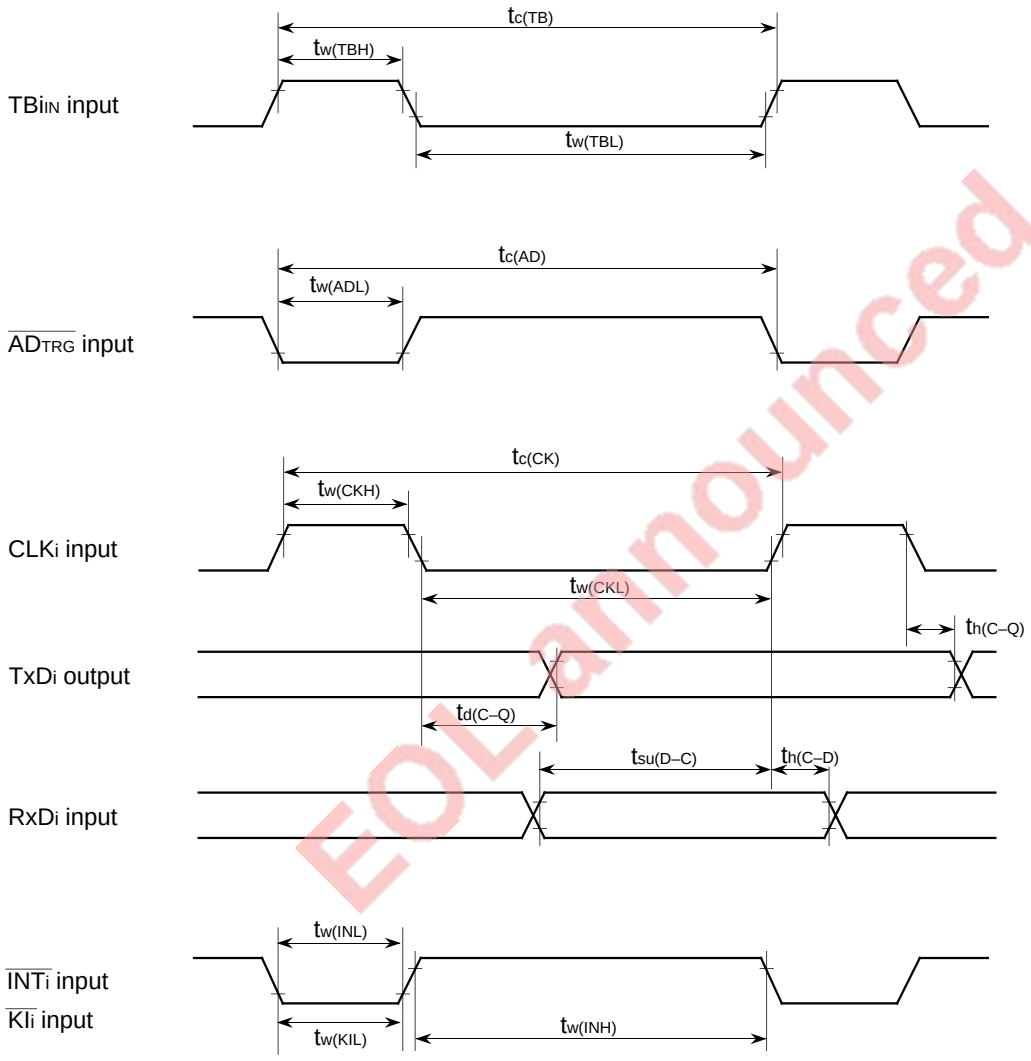
ELECTRICAL CHARACTERISTICS

15.5 Internal peripheral devices

External interrupt $\overline{INT_i}$ input, Key input interrupt $\overline{KI_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI_i}$ input low-level pulse width	250		ns

Internal peripheral devices



EOL announced

Measuring conditions

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.6 Ready and Hold

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(RDY-\phi1)}$	$\overline{RDY}$ input setup time	55		ns
$t_{su(HOLD-\phi1)}$	$\overline{HOLD}$ input setup time	55		ns
$t_{h(\phi1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Note: This is applied when the main clock division selection bit = “0” and f(f_2) = 12.5 MHz.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
$t_{d(\phi1-HLDA)}$	$\overline{HLDA}$ output delay time	Fig. 15.11.1		50	ns

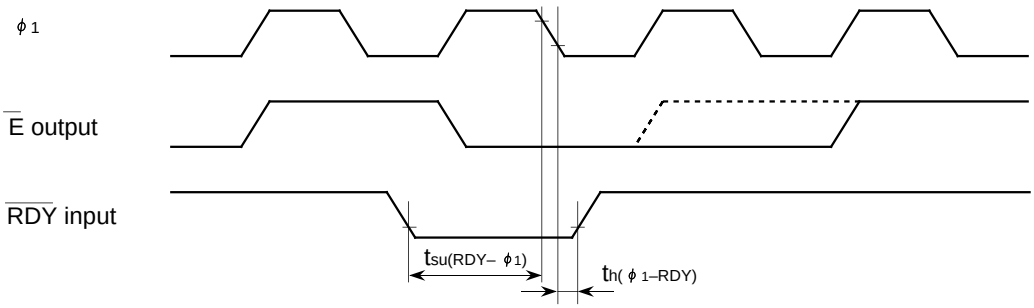
EOL announced

ELECTRICAL CHARACTERISTICS

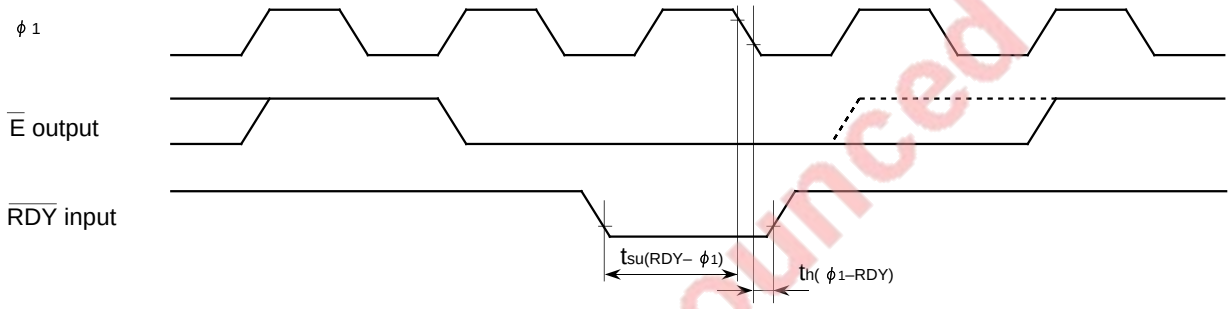
15.6 Ready and Hold

● Ready

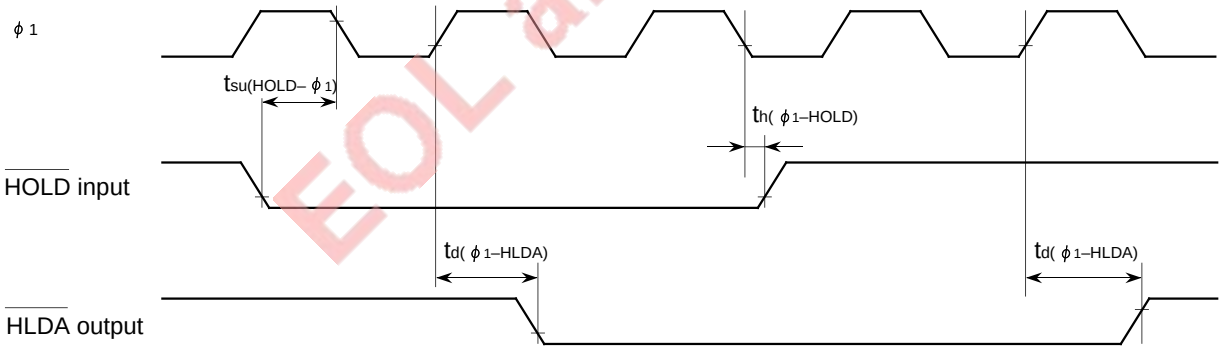
With no wait



With wait



● Hold



EOL announced

Measuring conditions

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.7 Single-chip mode

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(P0D–E)}$	Port P0 input setup time	60		ns
$t_{su(P1D–E)}$	Port P1 input setup time	60		ns
$t_{su(P2D–E)}$	Port P2 input setup time	60		ns
$t_{su(P3D–E)}$	Port P3 input setup time	60		ns
$t_{su(P4D–E)}$	Port P4 input setup time	60		ns
$t_{su(P5D–E)}$	Port P5 input setup time	60		ns
$t_{su(P6D–E)}$	Port P6 input setup time	60		ns
$t_{su(P7D–E)}$	Port P7 input setup time	60		ns
$t_{su(P8D–E)}$	Port P8 input setup time	60		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = “0” and f(f_2) = 12.5 MHz.
2: When the main clock division selection bit = “1,” the minimum value of tc = 80 ns.
3: When the main clock division selection bit = “1,” values of $tw_{(H)}$/tc and $tw_{(L)}$/tc must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
$t_{d(E–P0Q)}$	Port P0 data output delay time	Fig. 15.11.1		80	ns
$t_{d(E–P1Q)}$	Port P1 data output delay time			80	ns
$t_{d(E–P2Q)}$	Port P2 data output delay time			80	ns
$t_{d(E–P3Q)}$	Port P3 data output delay time			80	ns
$t_{d(E–P4Q)}$	Port P4 data output delay time			80	ns
$t_{d(E–P5Q)}$	Port P5 data output delay time			80	ns
$t_{d(E–P6Q)}$	Port P6 data output delay time			80	ns
$t_{d(E–P7Q)}$	Port P7 data output delay time			80	ns
$t_{d(E–P8Q)}$	Port P8 data output delay time			80	ns

Note: This is applied when the main clock division selection bit = “0” and f(f_2) = 12.5 MHz.

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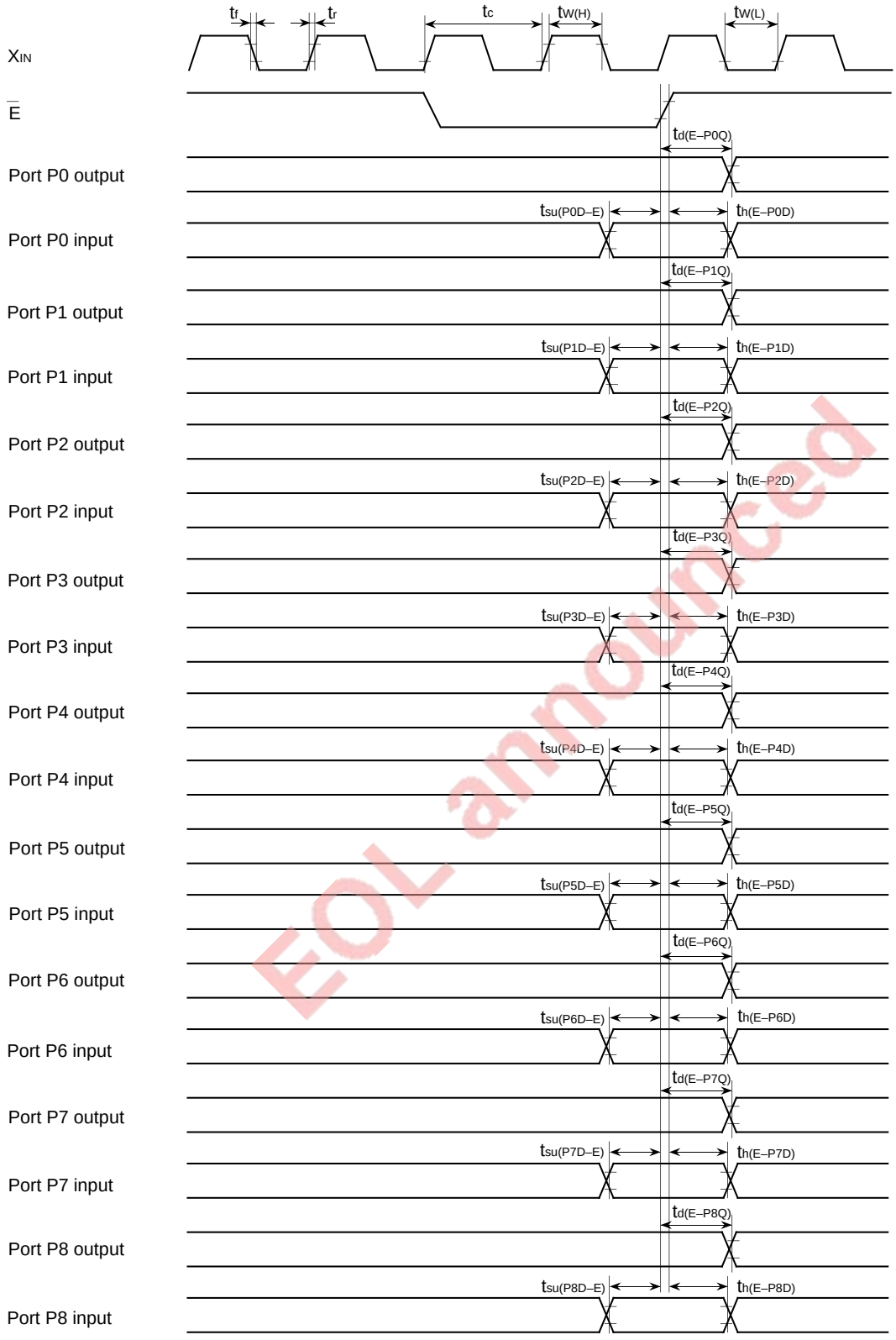
ELECTRICAL CHARACTERISTICS

15.7 Single-chip mode

Single-chip mode



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Measuring conditions

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.8 Memory expansion mode and Microprocessor mode : with no wait

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(D–E)}$	Data input setup time	32		ns
$t_{h(E–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: When the main clock division selection bit = "1," the minimum value of tc = 80 ns.
3: When the main clock division selection bit = "1," values of $tw_{(H)}$/tc and $tw_{(L)}$/tc must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(An–E)}$	Address output delay time	Fig. 15.11.1	$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{d(A–E)}$	Address output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{h(E–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \times f(f_2)} - 18$	22		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 35$	5		ns
$t_{h(ALE–A)}$	Address hold time			9		ns
$t_{d(ALE–E)}$	ALE output delay time			4		ns
$t_{d(E–DQ)}$	Data output delay time				45	ns
$t_{h(E–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{w(EL)}$	$\overline{E}$ pulse width		$\frac{2 \times 10^9}{2 \times f(f_2)} - 30$	50		ns
$t_{pxz(E–DZ)}$	Floating start delay time				5	ns
$t_{pzx(E–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 20$	20		ns
$t_{d(BHE–E)}$	$\overline{BHE}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{d(R/W–E)}$	R/$\overline{W}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{h(E–BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{h(E–R/W)}$	R/$\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{d(E–\phi 1)}$	$\phi 1$ output delay time			0	18	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

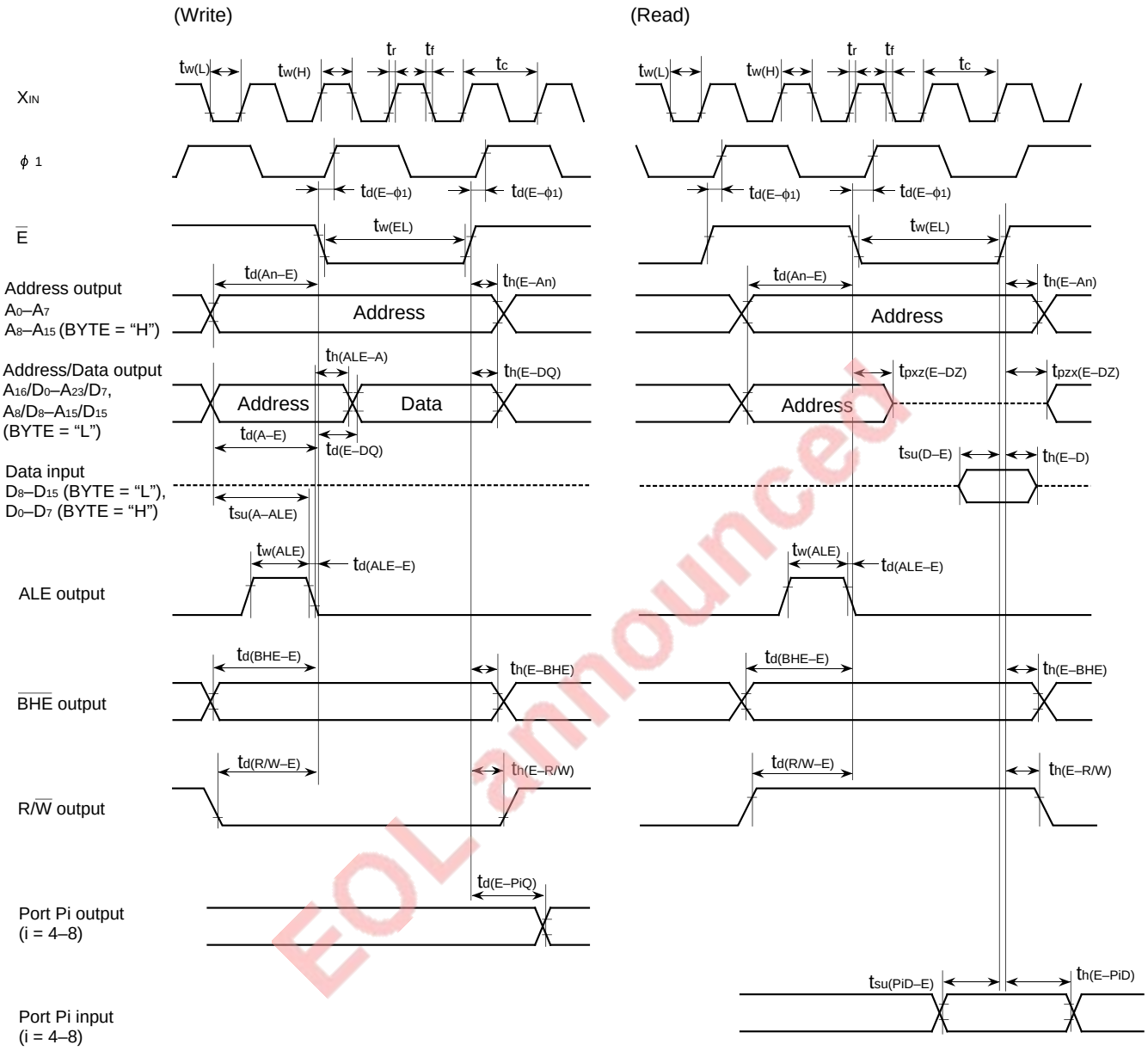
EOL announced

ELECTRICAL CHARACTERISTICS

15.8 Memory expansion mode and Microprocessor mode : with no wait

Memory expansion mode and Microprocessor mode :

With no wait (Wait bit = “1”)



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Measuring conditions (ϕ 1, $\overline{E}$, Ports P0–P3)

- V_{CC} = 5 V ± 10 %
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Port P1, P2 input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Measuring conditions (Ports P4–P8)

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.9 Memory expansion mode and Microprocessor mode : with wait 1

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(D-E)}$	Data input setup time	32		ns
$t_{h(E-D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: When the main clock division selection bit = "1," the minimum value of tc = 80 ns.
3: When the main clock division selection bit = "1," values of $tw_{(H)}$/tc and $tw_{(L)}$/tc must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(An-E)}$	Address output delay time	Fig. 15.11.1	$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{d(A-E)}$	Address output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{h(E-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \times f(f_2)} - 18$	22		ns
$t_{su(A-ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 35$	5		ns
$t_{h(ALE-A)}$	Address hold time			9		ns
$t_{d(ALE-E)}$	ALE output delay time			4		ns
$t_{d(E-DQ)}$	Data output delay time				45	ns
$t_{h(E-DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{w(EL)}$	$\overline{E}$ pulse width		$\frac{4 \times 10^9}{2 \times f(f_2)} - 30$	130		ns
$t_{pxz(E-DZ)}$	Floating start delay time				5	ns
$t_{pzx(E-DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 20$	20		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 28$	12		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{d(E-\phi 1)}$	$\phi 1$ output delay time			0	18	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

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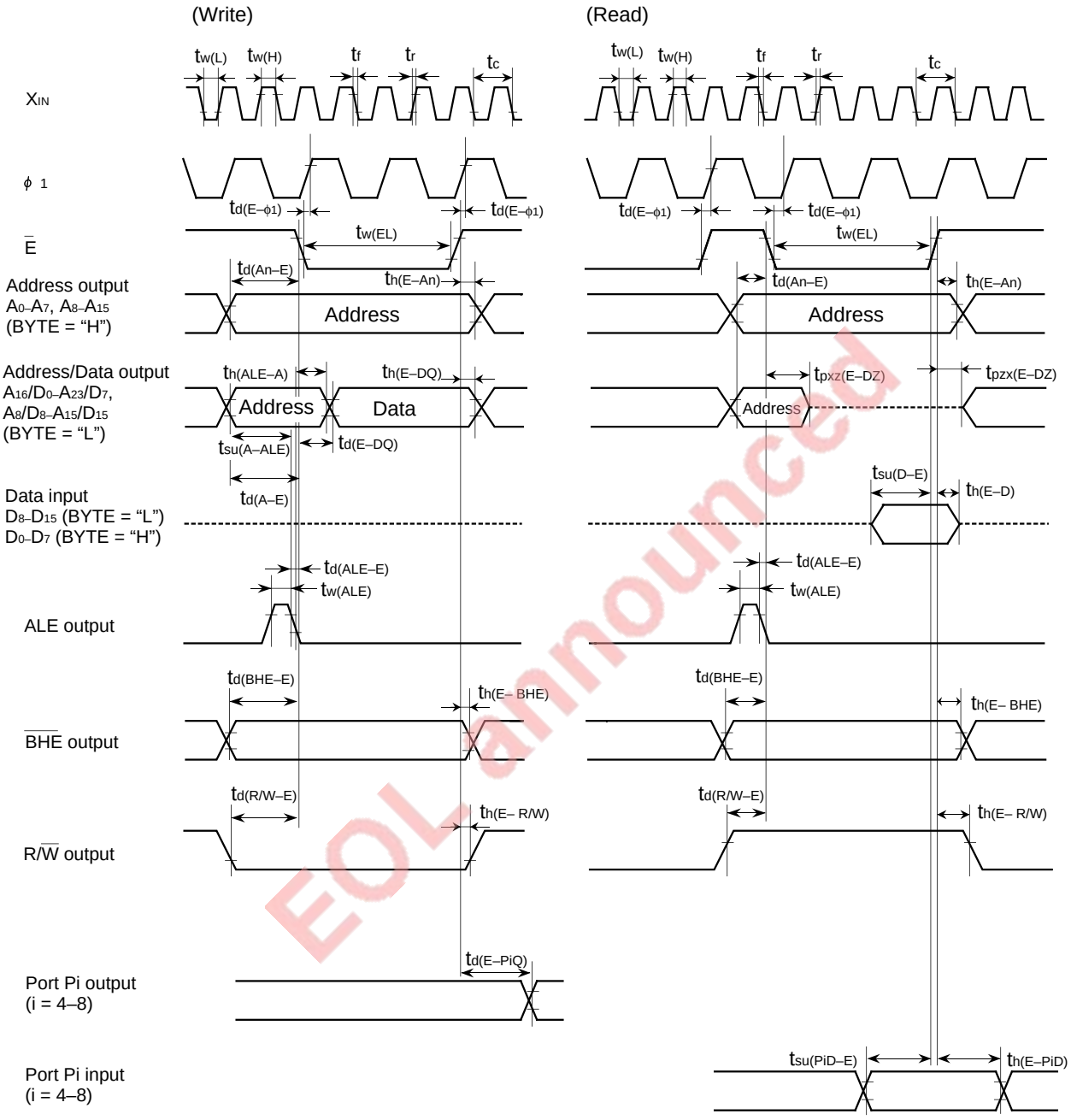
ELECTRICAL CHARACTERISTICS

15.9 Memory expansion mode and Microprocessor mode : with wait 1

Memory expansion mode and Microprocessor mode :

When external memory area is accessed with wait 1 (Wait bit = “0” and Wait selection bit = “1”)



Measuring conditions (ϕ 1, E, Ports P0–P3)

- V_{CC} = 5 V ± 10 %
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Ports P1, P2 input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Measuring conditions (Ports P4–P8)

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

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15.10 Memory expansion mode and Microprocessor mode : with wait 0

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(D–E)}$	Data input setup time	32		ns
$t_{h(E–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: When the main clock division selection bit = "1," the minimum value of tc = 80 ns.
3: When the main clock division selection bit = "1," values of $tw_{(H)}$/tc and $tw_{(L)}$/tc must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(An–E)}$	Address output delay time	Fig. 15.11.1	$\frac{3 \times 10^9}{2 \times f(f_2)} - 33$	87		ns
$t_{d(A–E)}$	Address output delay time		$\frac{3 \times 10^9}{2 \times f(f_2)} - 45$	75		ns
$t_{h(E–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{2 \times 10^9}{2 \times f(f_2)} - 23$	57		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{2 \times 10^9}{2 \times f(f_2)} - 35$	45		ns
$t_{h(ALE–A)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 25$	15		ns
$t_{d(ALE–E)}$	ALE output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 30$	10		ns
$t_{d(E–DQ)}$	Data output delay time				45	ns
$t_{h(E–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{w(EL)}$	$\overline{E}$ pulse width		$\frac{4 \times 10^9}{2 \times f(f_2)} - 30$	130		ns
$t_{pxz(E–DZ)}$	Floating start delay time				5	ns
$t_{pzx(E–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 20$	20		ns
$t_{d(BHE–E)}$	$\overline{BHE}$ output delay time		$\frac{3 \times 10^9}{2 \times f(f_2)} - 33$	87		ns
$t_{d(R/W–E)}$	R/$\overline{W}$ output delay time		$\frac{3 \times 10^9}{2 \times f(f_2)} - 33$	87		ns
$t_{h(E–BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{h(E–R/W)}$	R/$\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 22$	18		ns
$t_{d(E–\phi 1)}$	$\phi 1$ output delay time			0	18	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

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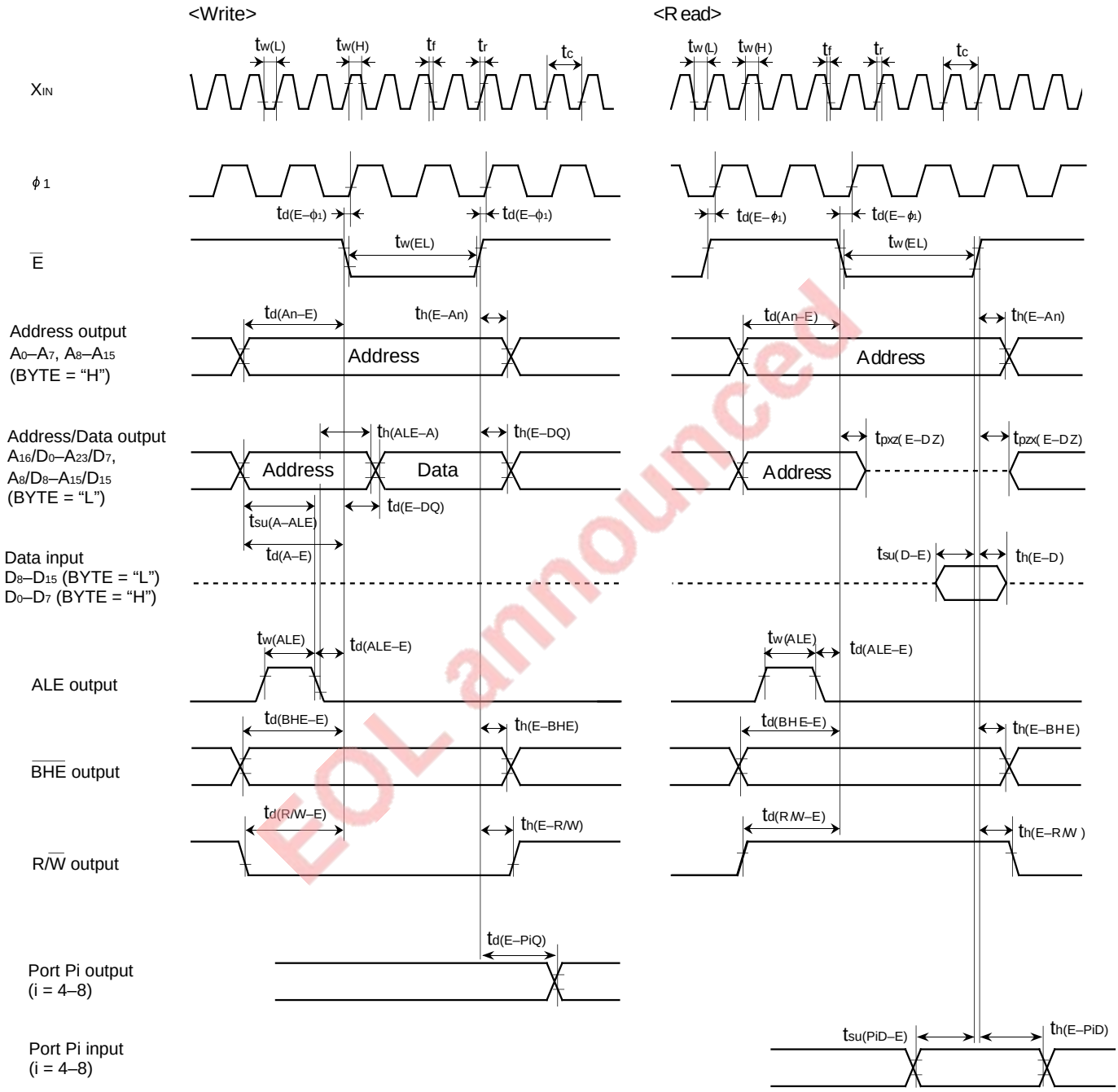
ELECTRICAL CHARACTERISTICS

15.10 Memory expansion mode and Microprocessor mode : with wait 0

Memory expansion mode and Microprocessor mode :

When external memory area is accessed with wait 0 (Wait bit = “0” and Wait selection bit = “0”)



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Measuring conditions ($\phi 1$, $\overline{E}$, Ports P0–P3)

- V_{CC} = 5 V ± 10 %
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Ports P1, P2 input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Measuring conditions (Ports P4–P8)

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.11 Measuring circuit for ports P0 to P8 and pins ϕ1 and $\overline{E}$

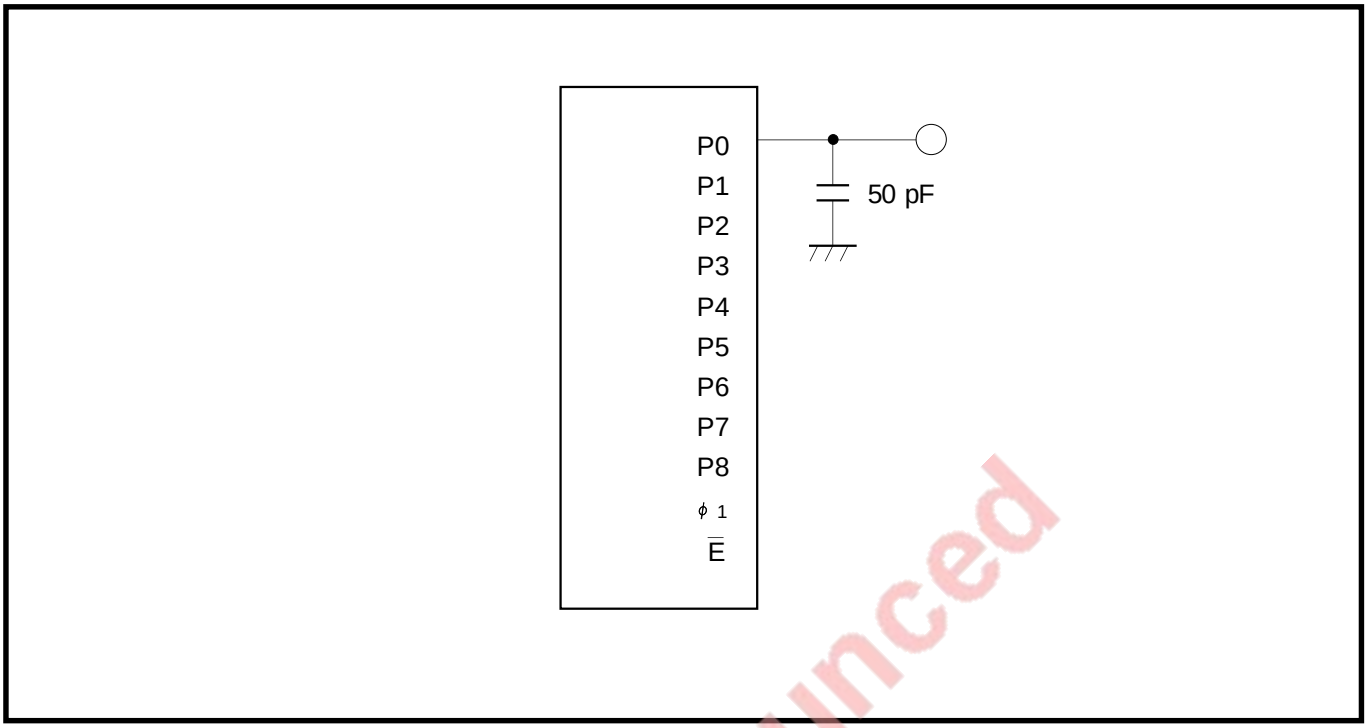

Fig. 15.11.1 Measuring circuit for ports P0 to P8 and pins ϕ1 and $\overline{E}$

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ELECTRICAL CHARACTERISTICS

15.11 Measuring circuit for ports P0 to P8 and pins $\phi 1$ and $\overline{E}$

MEMO

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CHAPTER 16

STANDARD CHARACTERISTICS

16.1 Standard characteristics

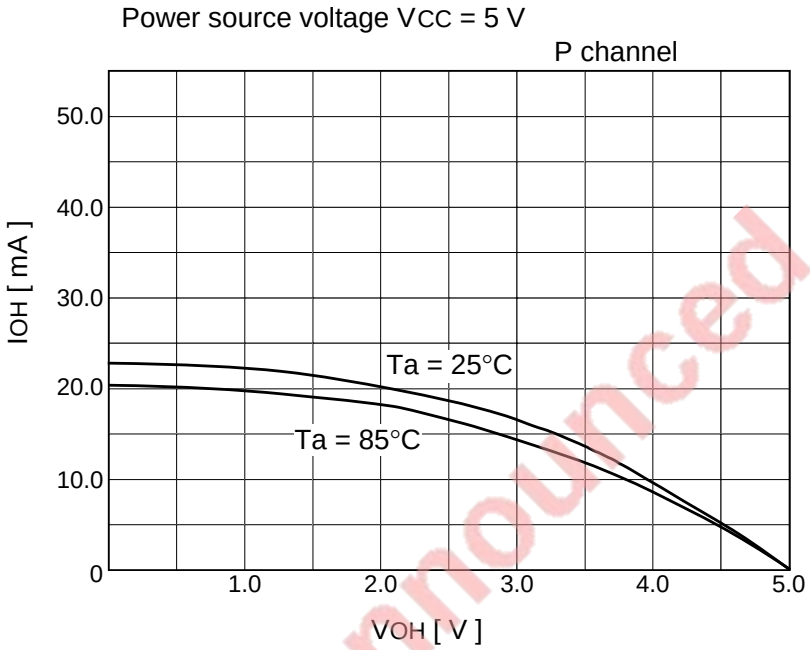
EOL announced

16.1 Standard characteristics

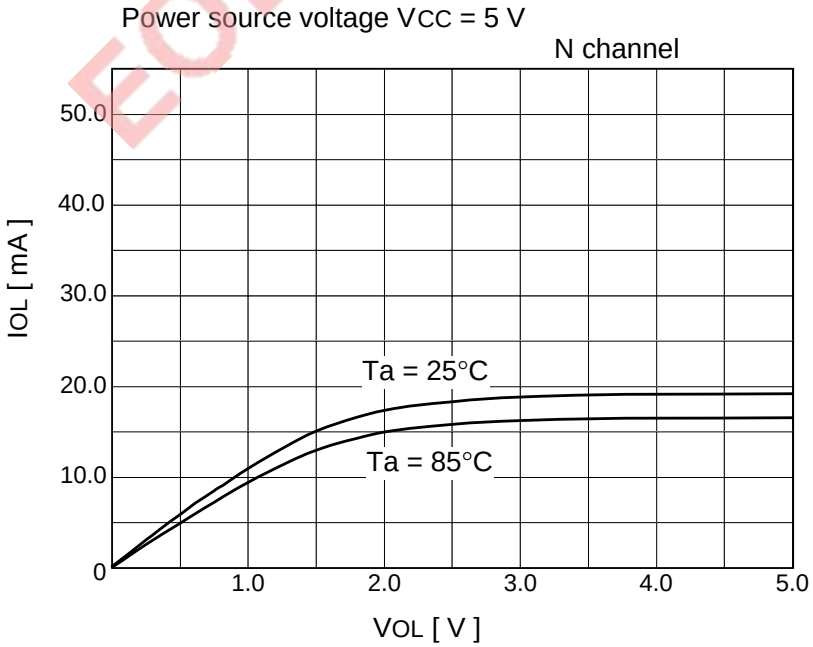
Standard characteristics described below are characteristic examples of the M37733MHBXXXFP and are not guaranteed. For each parameter's limits, refer to chapter **"15. ELECTRICAL CHARACTERISTICS."**

16.1.1 Programmable I/O port (CMOS output) standard characteristics: P0 to P3, $P4_0$ to $P4_3$, $P5_4$ to $P5_7$, P6, P7, and P8

(1) P-channel I_{OH}–V_{OH} characteristics



(2) N-channel I_{OL}–V_{OL} characteristics



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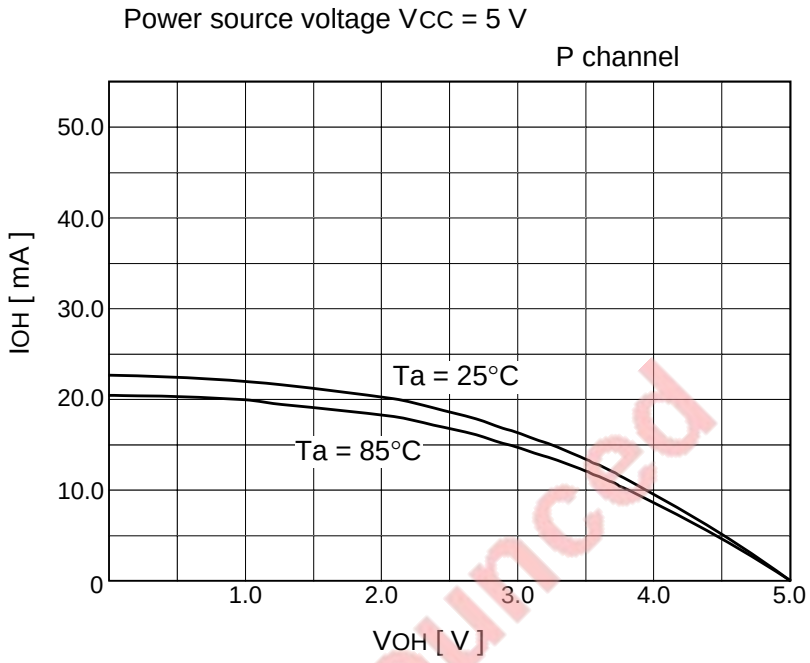
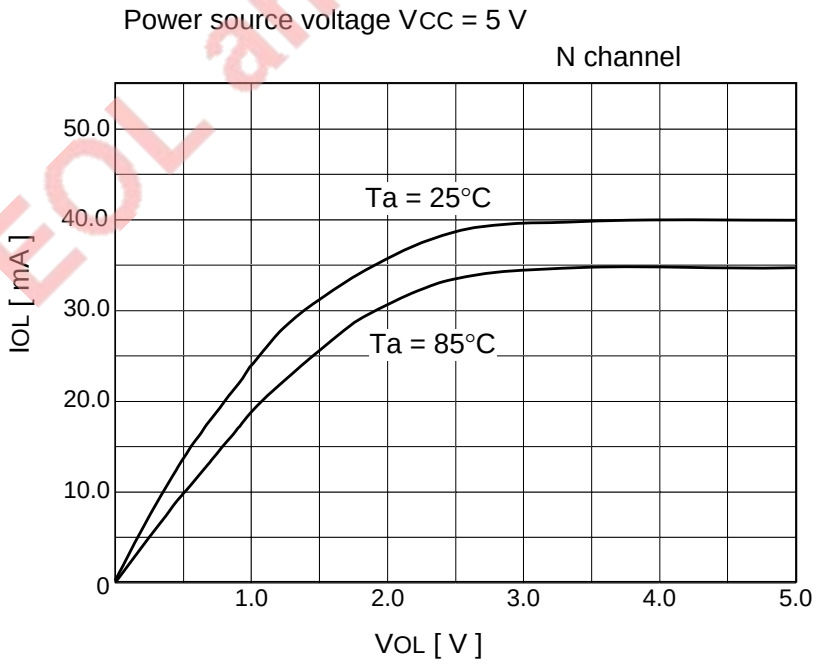
16.1.2 Programmable I/O port (CMOS output) standard characteristics: P44 to P47 and P50 to P53

(1) P-channel IOH–VOH characteristics



(2) N-channel IOL–VOL characteristics



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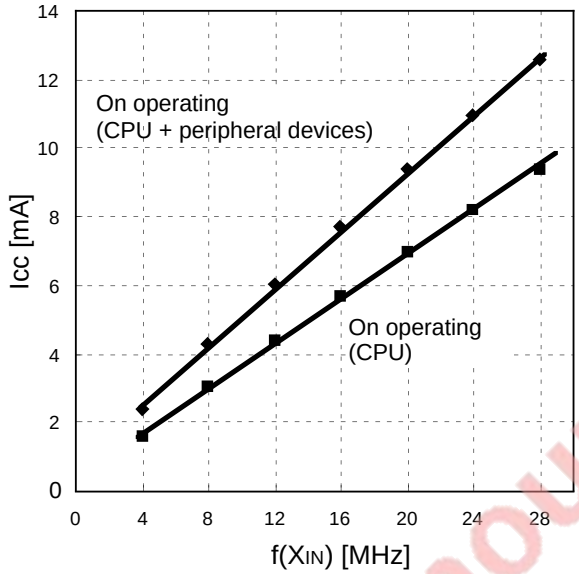
STANDARD CHARACTERISTICS

16.1 Standard characteristics

16.1.3 Icc–f(XIN) standard characteristics

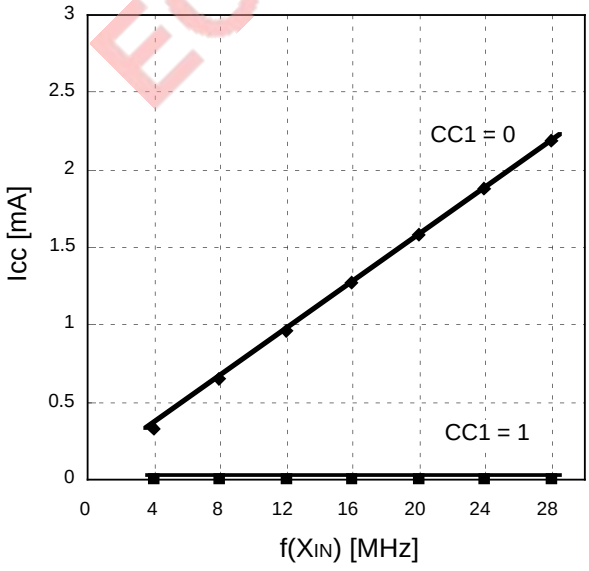
(1) Icc–f(XIN) characteristics on operating and at reset

- Measurement condition
  Vcc = 5V,Ta = 25°C, f(XIN): square waveform input, single-chip mode
- Register setting condition
  Oscillation circuit control register 1 = "02$_{16}$" (Main clock is input from the external.)



(2) Icc–f(XIN) characteristics in wait mode

- Measurement condition
  Vcc = 5V,Ta = 25°C, f(XIN): square waveform input, single-chip mode
- Register setting condition
  Oscillation circuit control register 0 = "20$_{16}$" (In the wait mode, clocks f_2 to f_{512} are stopped.)
  Oscillation circuit control register 1 = "02$_{16}$" (Main clock is input from the external.) or
  "00$_{16}$" (Main-clock oscillation circuit is operating by itself)



CC1: Main clock external input selection bit (b1 of the oscillation circuit control register 1)

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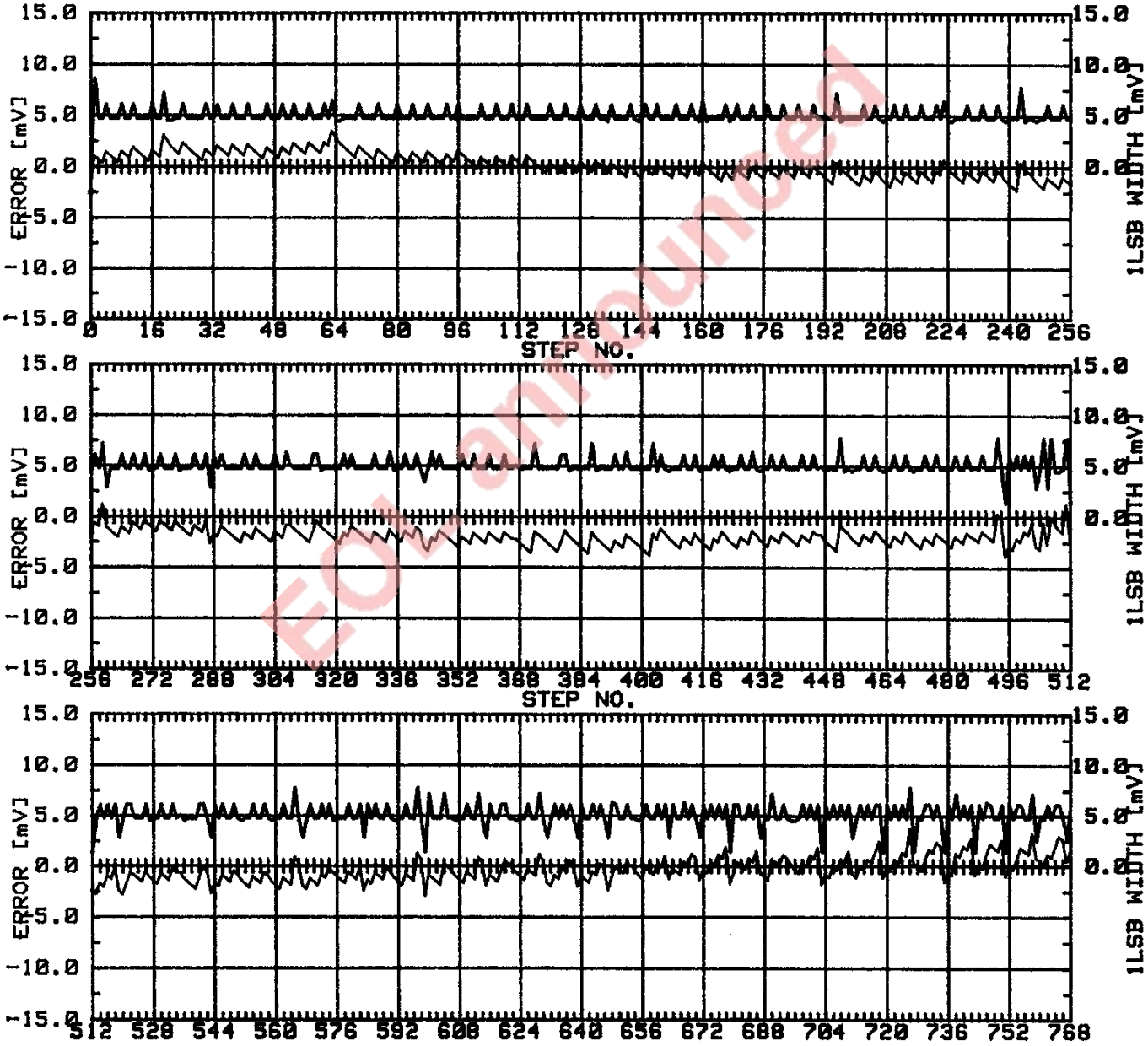
16.1.4 A-D converter standard characteristics

The lower lines of the graph indicate the absolute precision errors. These are expressed as the deviation from the ideal value when the output code changes. For example, the change in output code from "0E16" to "0F16" should occur at 72.5 mV, but the measured value is 0.6 mV. Accordingly, the measured point of change is 72.5 + 0.6 = 73.1 mV.

The upper lines of the graph indicate the input voltage width for which the output code is constant. For example, the measured input voltage width for which the output code is "0F16" is 4.7 mV. Accordingly, the differential non-linear error is 4.7 – 5.0 = –0.3 mV (–0.06LSB).

[Measurement condition]

• VCC = AVCC = 5 V, • VREF = 5.12 V, • f(XIN) = 25 MHz, • Ta = 25 °C



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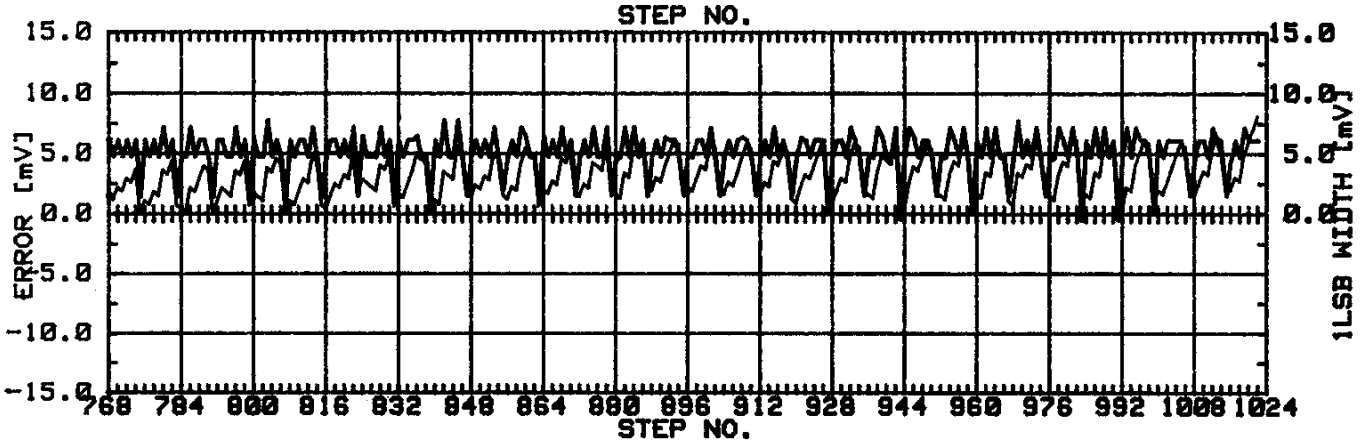
STANDARD CHARACTERISTICS

16.1 Standard characteristics



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CHAPTER 17
APPLICATIONS

17.1 Memory expansion
17.2 Serial I/O
17.3 Watchdog timer
17.4 Power saving
17.5 Timer B

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APPLICATIONS

17.1 Memory expansion

Some application examples are described below.
Applications shown here are just examples. Modify the desired application to suit the user's need and make sufficient evaluation before actually using it.

17.1 Memory expansion

Memory • I/O expansion examples are described below.

- For functions and operations of pins used in memory • I/O expansion, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**
- For timing characteristics, refer to chapter **"15. ELECTRICAL CHARACTERISTICS."**
- For timing characteristics and applications of the low voltage version, refer to chapter **"18. LOW VOLTAGE VERSION."**

17.1.1 Memory expansion model

Memory expansion to the external is enabled in the memory expansion or microprocessor mode. In the 7733 Group, the desired memory expansion model can be selected from four models listed in Table 17.1.1. This selection depends on the level of the external data bus width selection signal (BYTE).

(1) Minimum model

The external data bus is 8 bits wide and the accessible area can be expanded up to 64 Kbytes. No external address latch is necessary, so this model gives priority to cost and is most suitable when connecting a memory of which data bus is 8 bits wide.

(2) Medium model A

The external data bus is 8 bits wide and the accessible area can be expanded up to 16 Mbytes. The high-order 8 bits of the external address bus (A_{23} to A_{16}) are multiplexed with the external data bus. Therefore, one n-bit ($n \leq 8$) address latch is necessary in order to latch n bits of address in A_{23} to A_{16}.

(3) Medium model B

The external data bus is 16 bits wide and the accessible area can be expanded up to 64 Kbytes. This model gives priority to speed. The middle-order 8 bits of the external address bus (A_{15} to A_8) are multiplexed with the external data bus. Therefore, one 8-bit address latch is necessary in order to latch A_{15} to A_8.

(4) Maximum model

The external data bus is 16 bits wide and the accessible area can be expanded up to 16 Mbytes. The high- and middle- order 16 bits of the external address bus (A_{23} to A_8) are multiplexed with the external data bus. Therefore, both of the following latches are necessary:

- One 8-bit address latch used for latching A_{15} to A_8
- One n-bit ($n \leq 8$) address latch used for latching n bits of address in A_{23} to A_{16}

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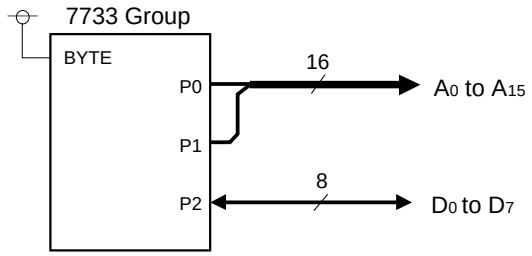
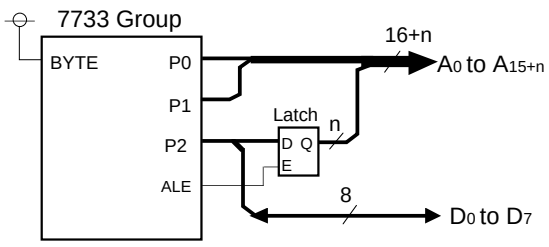
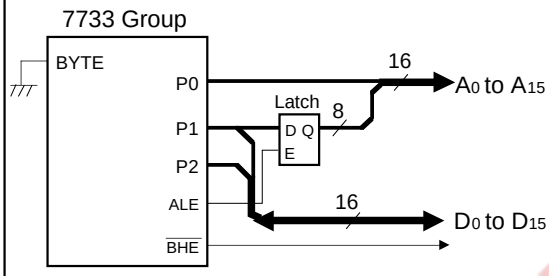
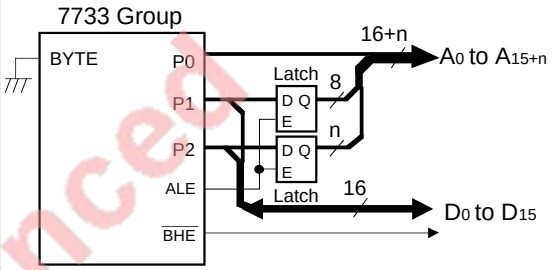
Table 17.1.1 Memory expansion models

Accessible area / External data bus	64 Kbytes (Max.)	16 Mbytes (Max.)
8 bits wide BYTE = "H"	 Memory expansion model: Minimum model	 Memory expansion model: Medium model A
16 bits wide BYTE = "L"	 Memory expansion model: Medium model B	 Memory expansion model: Maximum model

❋ For functions and operations of pins used in memory expansion, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."** For timing characteristics, refer to chapter **"15. ELECTRICAL CHARACTERISTICS."**

❋ In memory expansion, the address bus can be expanded up to 24 bits wide. Accordingly, be sure to strengthen the 7733 Group's Vss line on the system. (Refer to section **"Appendix 8.Countermeasure examples against noise."**)

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APPLICATIONS

17.1 Memory expansion

17.1.2 Calculation ways for timing

When expanding memory, use a memory of which specifications satisfy the following timing requirements: address access time ($t_{a(AD)}$) and data setup time for writing data ($t_{su(D)}$). Calculation ways for $t_{a(AD)}$ and $t_{su(D)}$ are described below.

① **Address access time of external memory [$t_{a(AD)}$]**

$t_{a(AD)} = t_{d(An/A-E)} + t_{w(EL)} - t_{su(D-E)}$
$- (\text{address decode time}^{*1} + \text{address latch delay time}^{*2})$
$t_{d(An/A-E)}$: $t_{d(An-E)}$ or $t_{d(A-E)}$

address decode time*1: time necessary for validating a chip select signal after an address is decoded
address latch delay time*2: delay time necesarry for latching an address
(This is not necessary on the minimum model.)

② **Data setup time of external memory for writing data [$t_{su(D)}$]**

$t_{su(D)} = t_{w(EL)} - t_{d(E-D)}$

Table 17.1.2 lists the calculation formulas and constants for each parameter in the above formulas. Figure 17.1.1 shows bus timing diagrams. Figure 17.1.2 shows the relationship between $t_{a(AD)}$ and $2 \bullet f(f_2)$. Figure 17.1.3 shows the relationship between $t_{su(D)}$ and $2 \bullet f(f_2)$.

Table 17.1.2 Calculation formulas and constants for each parameter (Unit: ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{d(A-E)}$ $t_{d(An-E)}$	$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 28$		$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 45$
$t_{w(EL)}$	$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 30$	$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 30$	
$t_{su(D-E)}$	32		
$t_{d(E-DQ)}$	45		

Wait bit: Bit 2 at address $5E_{16}$
Wait selection bit: Bit 0 at address $5F_{16}$
Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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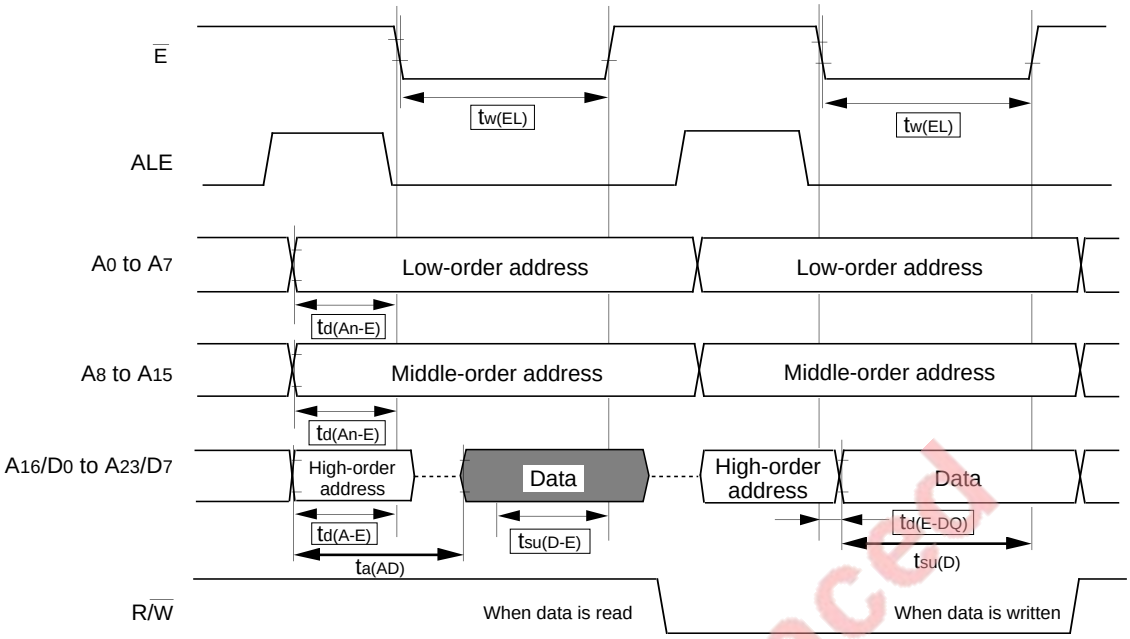
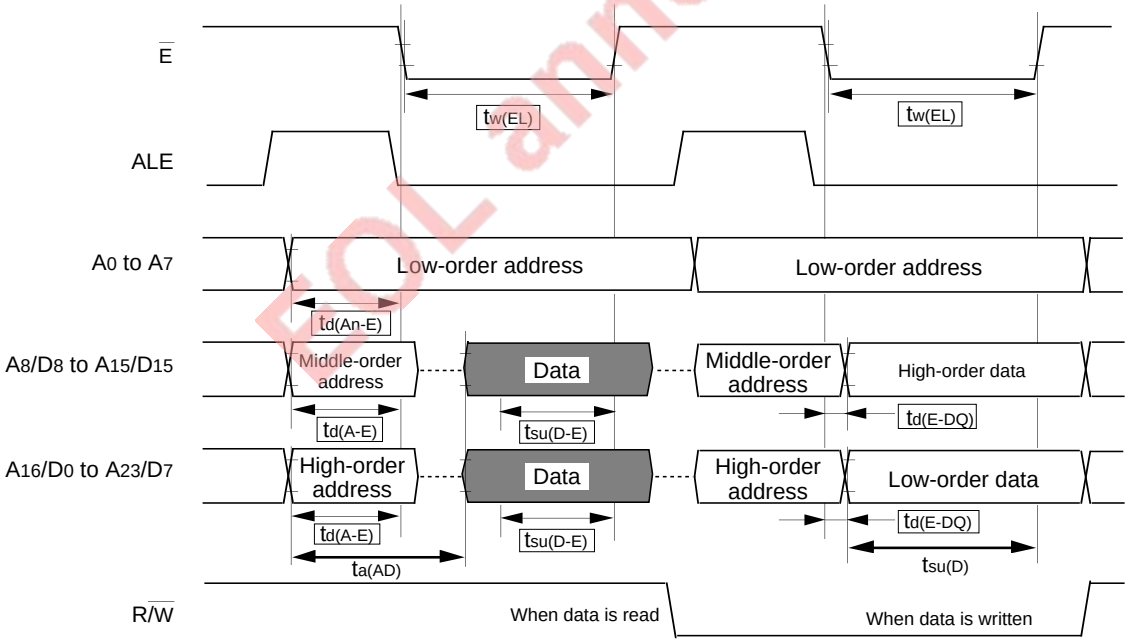
When BYTE = “H” (External data bus = 8 bits wide)



When BYTE = “L” (External data bus = 16 bits wide)



EOL announced

: Specifications of the 7733 Group
(The others are specifications of external memory.)

Fig. 17.1.1 Bus timing diagrams

APPLICATIONS

17.1 Memory expansion

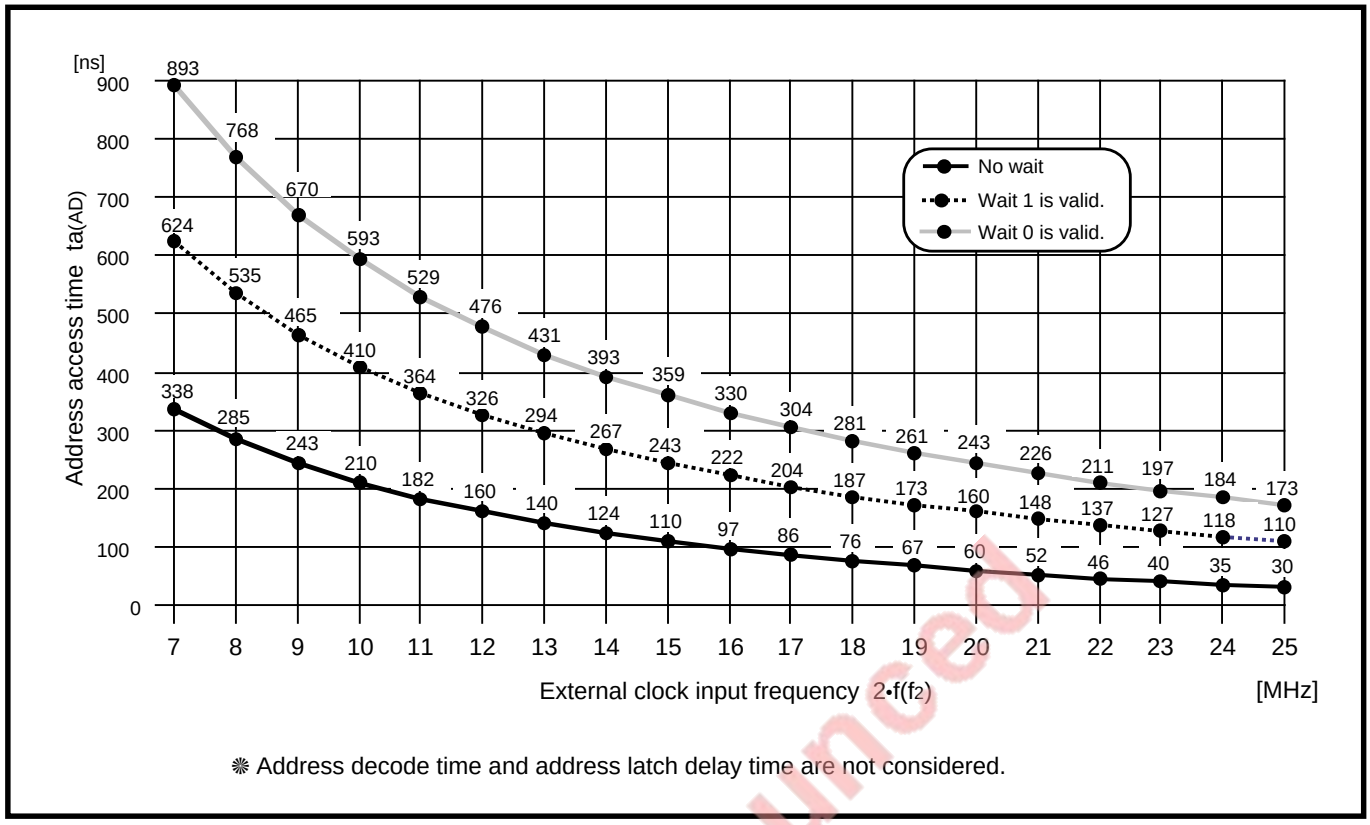


Fig. 17.1.2 Relationship between ta(AD) and 2•f(f2)

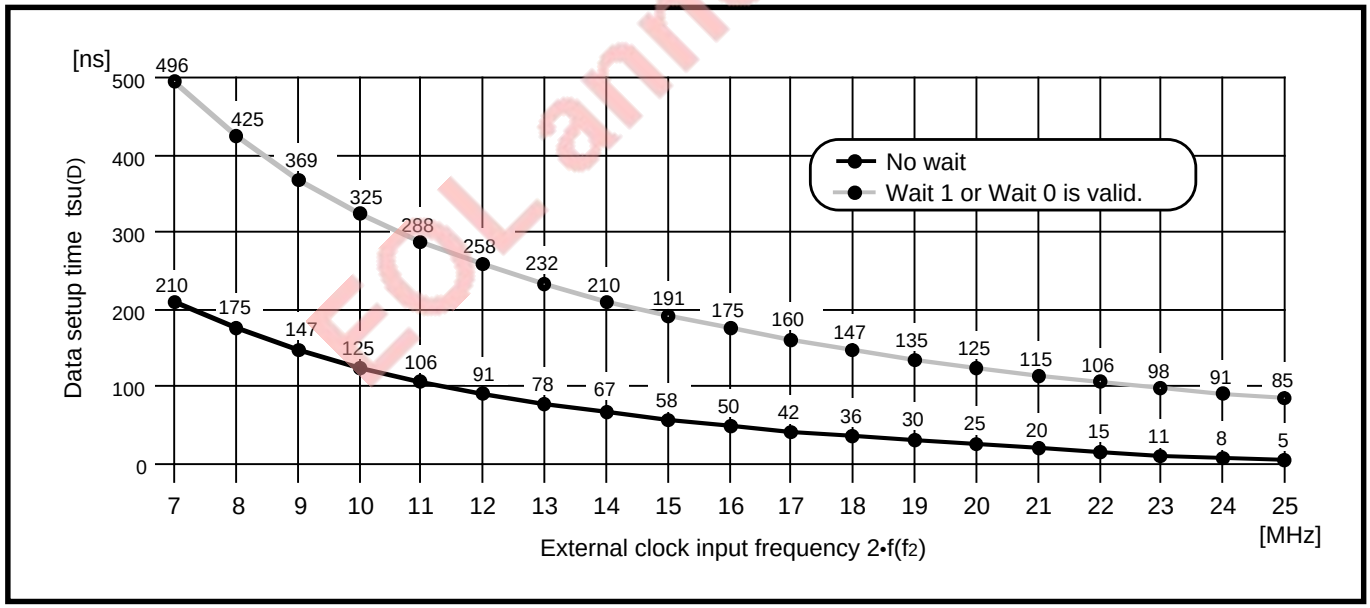


Fig. 17.1.3 Relationship between tsu(D) and 2•f(f2)

EOL announced

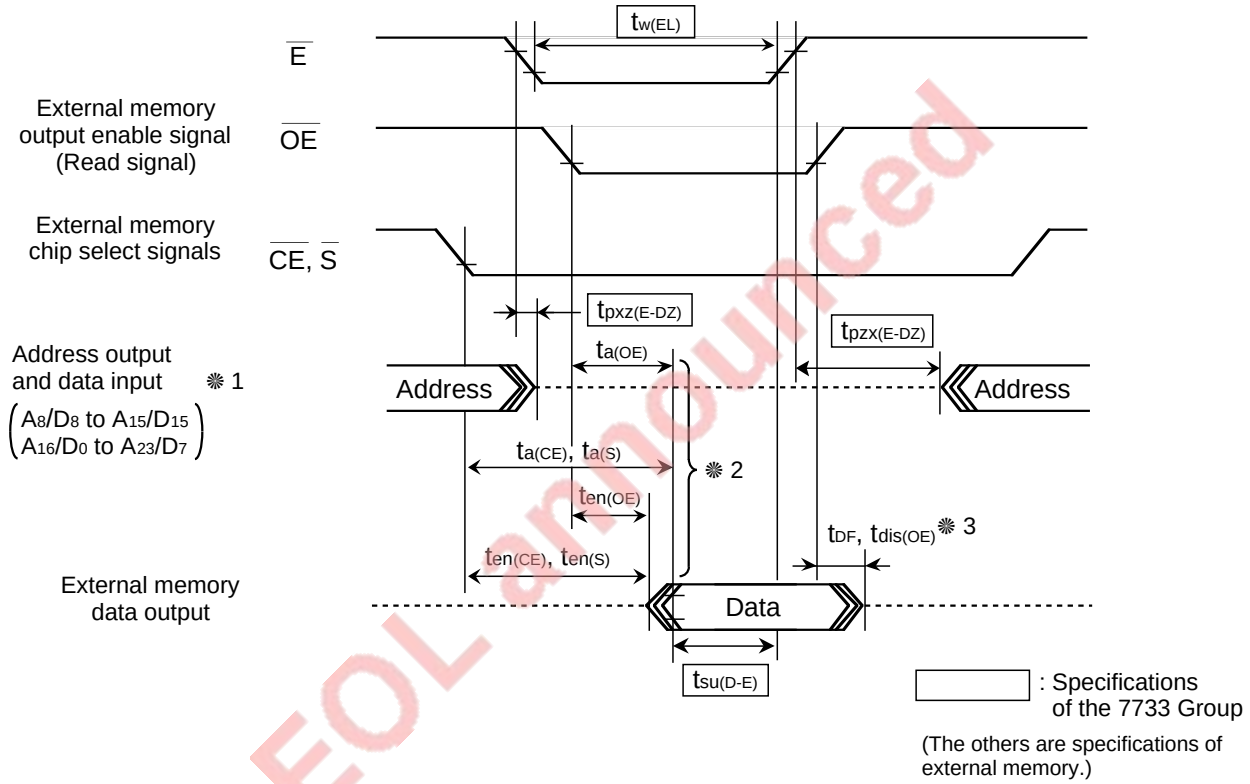
17.1.3 Points in memory expansion

(1) Timing for reading data

Figure 17.1.4 shows the timing at which data is read from an external memory.

When data is read, the external data bus enters a floating state and reads data from the external memory. The floating state of the external data bus is retained from when an interval of $t_{pxz(E\text{-}DZ)}$ has passed after signal $\overline{E}$'s falling edge until an interval of $t_{pzx(E\text{-}DZ)}$ has passed after signal $\overline{E}$'s rising edge. Table 17.1.3 lists the value of $t_{pxz(E\text{-}DZ)}$ and the calculation formula for $t_{pzx(E\text{-}DZ)}$.

Note that the external data bus is multiplexed with the external address bus. Therefore, when reading data, it is necessary to consider timing to avoid collision between data being read-in and an address which is output preceding or following the data. (Refer to **"(3) Precautions on memory expansion."**)



EOL announced

❋ 1 This is applied when the external data bus = 16 bits wide (BYTE = "L").

❋ 2 When the external memory's specifications are smaller than $t_{pxz(E\text{-}DZ)}$, there is a possibility that the tail of address collides with the head of data.→ Refer to **"(3) Precautions on memory expansion."**

❋ 3 When the external memory's specifications are greater than $t_{pzx(E\text{-}DZ)}$, there is a possibility that the tail of data collides with the head of address. → Refer to **"(3) Precautions on memory expansion."**

Fig. 17.1.4 Timing at which data is read from external memory

APPLICATIONS

17.1 Memory expansion

Table 17.1.3 Value of $t_{pxz(E\text{-}DZ)}$ and calculation formula for $t_{pzx(E\text{-}DZ)}$ (Unit: ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{pxz(E\text{-}DZ)}$	5		
$t_{pzx(E\text{-}DZ)}$	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		

Wait bit: Bit 2 at address $5E_{16}$
Wait selection bit: Bit 0 at address $5F_{16}$
Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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(2) Timing for writing data

Figure 17.1.5 shows the timing for writing data to an external memory.

When data is written, the data is output from when an interval of $t_{d(E\text{-}DQ)}$ has passed after signal $\overline{E}$'s falling edge until an interval of $t_{h(E\text{-}DQ)}$ has passed after signal $\overline{E}$'s rising edge. Table 17.1.4 lists the value of $t_{d(E\text{-}DQ)}$ and the calculation formula for $t_{h(E\text{-}DQ)}$.

Make sure that the data output timing for writing data satisfies the following specifications of the external memory: data setup time ($t_{su(D)}$) and data hold time ($t_{h(D)}$) for writing data.

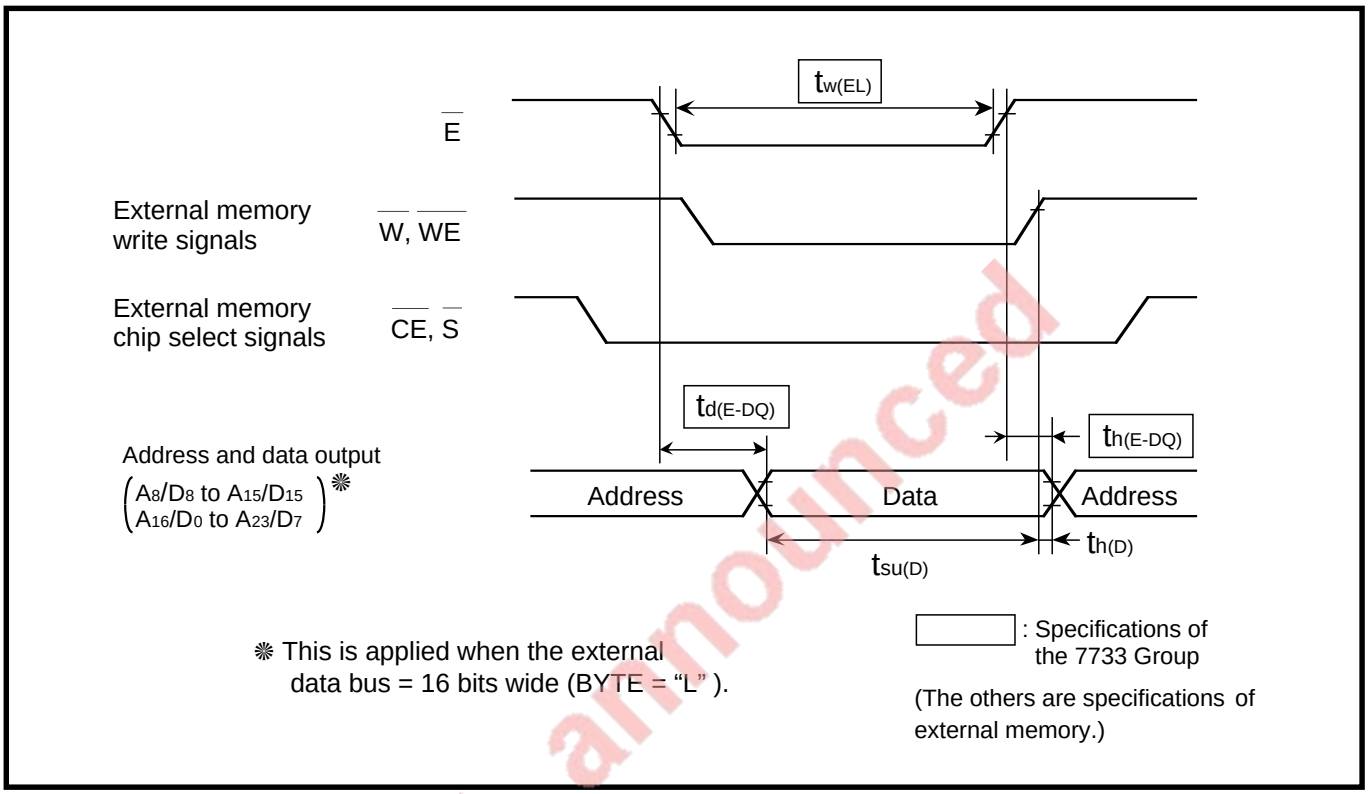

Fig. 17.1.5 Timing at which data is written to external memory

Table 17.1.4 Value of $t_{d(E\text{-}DQ)}$ and calculation formula for $t_{h(E\text{-}DQ)}$ (Unit: ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{d(E\text{-}DQ)}$	45		
$t_{h(E\text{-}DQ)}$	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		

Wait bit: Bit 2 at address $5E_{16}$

Wait selection bit: Bit 0 at address $5F_{16}$

Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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APPLICATIONS

17.1 Memory expansion

(3) Precautions on memory expansion

When specifications of the 7733 Group do not match those of an external memory as described in the following ① to ③, some considerations about the circuit are necessary:

① When using an external memory which requires a long address access time ($t_{a(AD)}$)
② When using an external memory which outputs data within an interval of $t_{pxz(E\text{-}DZ)}$ after signal $\overline{E}$'s falling edge.
③ When using an external memory which outputs data for more than an interval of $t_{pzx(E\text{-}DZ)}$ after signal $\overline{E}$'s rising edge

① **When using an external memory which requires a long address access time ($t_{a(AD)}$)**

When an external memory requires a long address access time ($t_{a(AD)}$) which does not satisfy the 7733 Group's $t_{su(D\text{-}E)}$, try to carry out the following:

- Lower 2•f(f_2)
- Select "Software wait is inserted." (Refer to section **"12.2 Software wait."**)
- Use the ready function. (Refer to section **"12.3 Ready function."**)

Figure 17.1.6 shows a ready generating circuit example (with no wait). Figure 17.1.7 shows a ready generating circuit example (with wait 1).
Note that the ready function is also valid for the internal area. Therefore, in Figures 17.1.6 and 17.1.7, areas where the ready function is valid are specified by using the chip select signal ($\overline{CS_2}$) which is externally generated.

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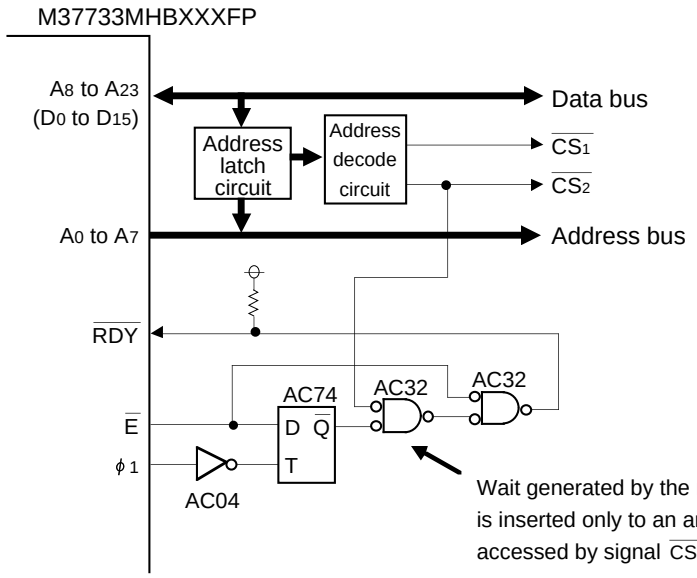
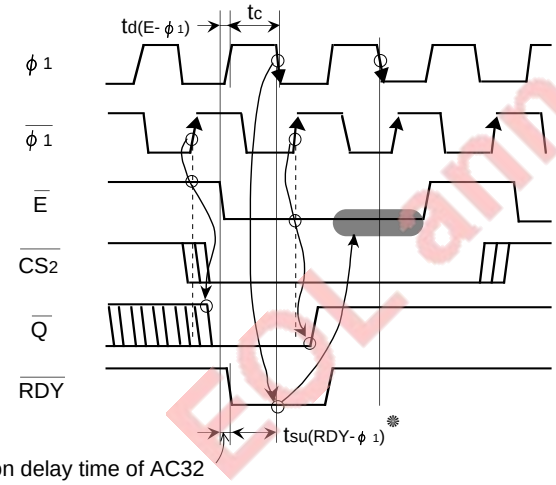


Circuit conditions: f(XIN) ≤ 15.7 MHz, no wait

$$\phi 1 = \frac{f(X_{IN})}{2}, \frac{f(X_{IN})}{8}, \frac{f(X_{IN})}{16}, \text{ or } \frac{f(X_{CIN})}{2}$$



Propagation delay time of AC32 (Max.: 8.5 ns)

❋ Condition to satisfy the relationship of $t_{su(RDY-\phi 1)} \geq 55$ ns in the left timing chart is tc ≥ 63.5 ns.
Accordingly, when f(XIN) ≤ 15.7 MHz, this example satisfies the relationship of $t_{su(RDY-\phi 1)} \geq 55$ ns.

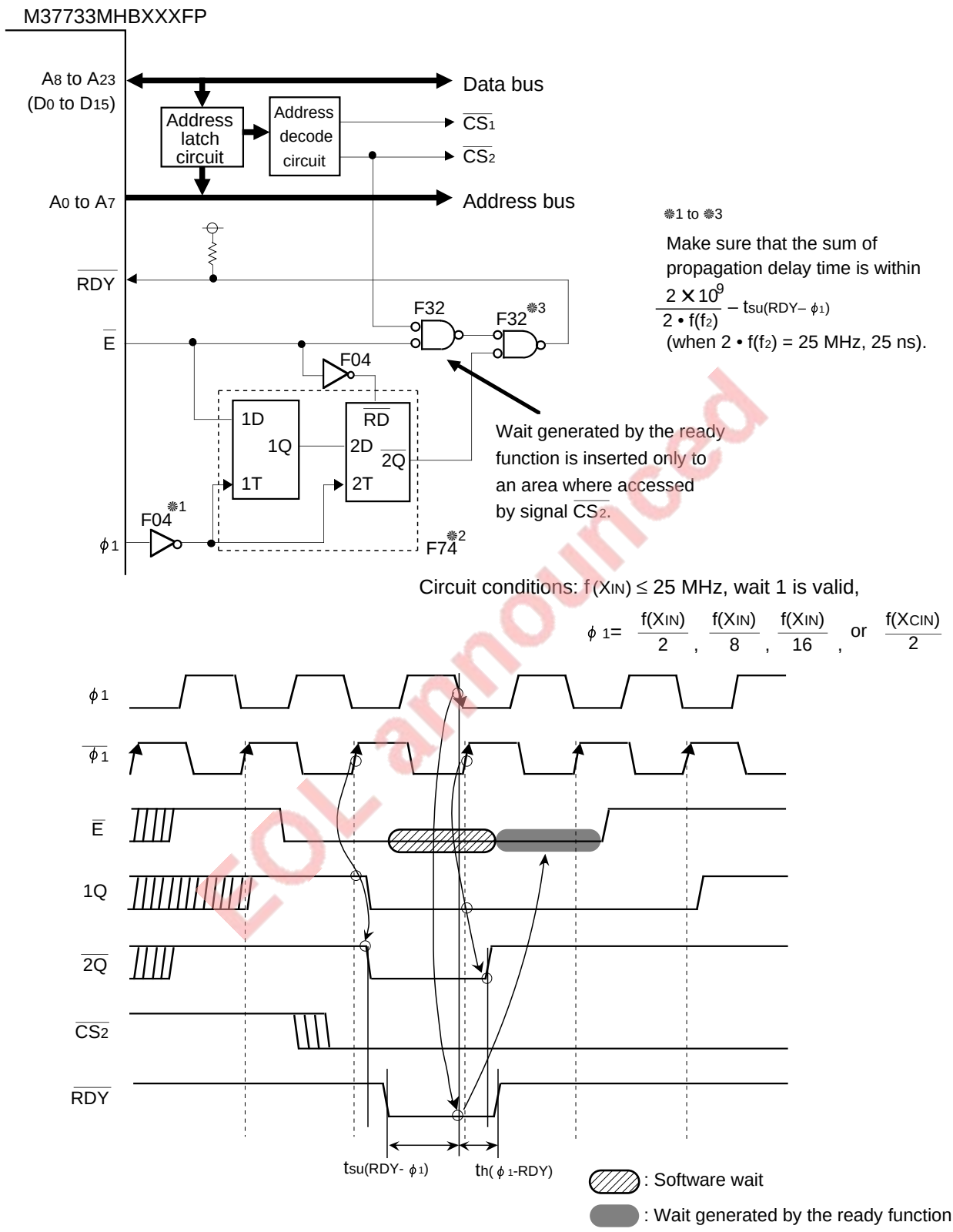
: Wait generated by the ready function

EOL announced

Fig. 17.1.6 Ready generating circuit example (with no wait)

APPLICATIONS

17.1 Memory expansion

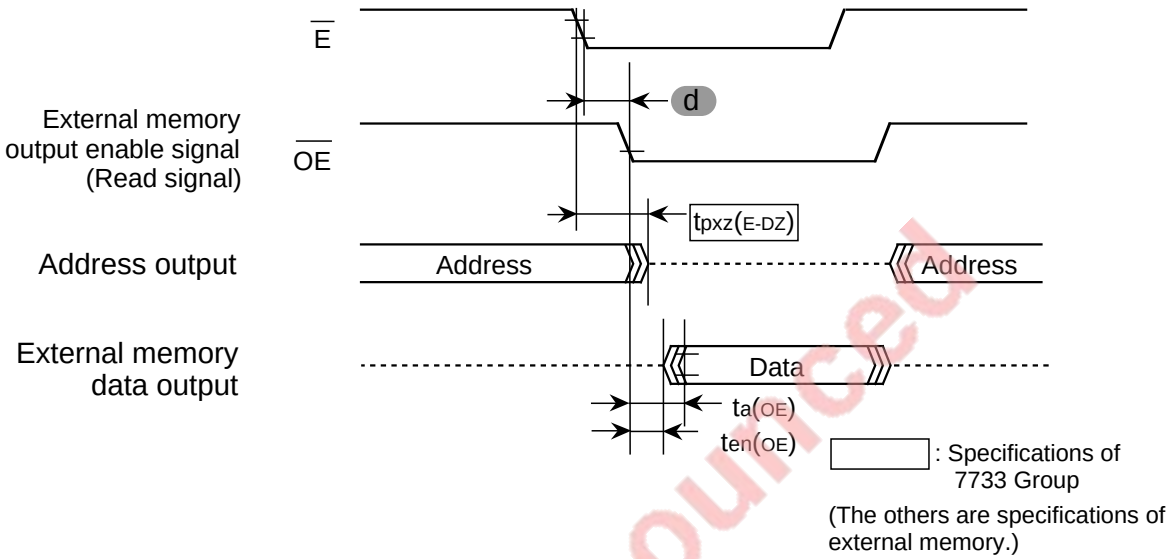


EOL announced

Fig. 17.1.7 Ready generating circuit example (with wait 1)

② **When using an external memory which outputs data within an interval of $t_{pxz(E\text{-}DZ)}$ after signal $\overline{E}$'s falling edge**

When there is a possibility that the tail of an address collides with the head of data because the external memory outputs data within an interval of $t_{pxz(E\text{-}DZ)}$ after signal $\overline{E}$'s falling edge, delay only the $\overline{E}$'s front falling edge. In this case, the falling edge of the read signal ($\overline{OE}$) for the memory, which is generated from signal $\overline{E}$, is delayed. (Refer to **Figure 17.1.8.**)



Note: Satisfy the following conditions:

- $t_{pxz(E\text{-}DZ)} \leq t_{en(OE)} + d$
- When $t_{en(OE)} \leq t_{pxz(E\text{-}DZ)}$ (= 5 ns), make sure that signal $\overline{E}$'s falling edge precedes signal $\overline{OE}$'s falling edge and an interval of "d" is secured.

Fig. 17.1.8 Timing example when data output is delayed

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17.1 Memory expansion

③ **When using an external memory which outputs data for more than an interval of $t_{pzx(E\text{-}DZ)}$ after signal $\overline{E}$'s rising edge**

When there is a possibility that the tail of data collides with the head of an address because the external memory outputs the data for more than an interval of $t_{pzx(E\text{-}DZ)}$ after signal $\overline{E}$'s rising edge, try to carry out the following:

- By using bus buffers and others, delete the tail of data which is output from the memory.
- Use a memory which is made by MITSUBISHI ELECTRIC CORPORATION and can be connected without bus buffers.

Figures 17.1.9 to 17.1.12 show bus buffer usage examples and the corresponding timing diagrams. Table 17.1.5 lists memories which can be connected without bus buffers (made by MITSUBISHI ELECTRIC CORPORATION). The reason why these memories do not need buffers is that timing parameters t_{DF} or $t_{dis(OE)}$ is guaranteed. (Make sure that the read signal rises within 10 ns after signal $\overline{E}$'s rising edge.)

Table 17.1.5 Memories which can be connected without bus buffers (made by MITSUBISHI ELECTRIC CORPORATION)

Memory	Type	$t_{DF}/t_{dis(OE)}$ (Max.)	Usage condition
EPROM	M5M27C256AK-85, -10, -12, -15 M5M27C512AK-10, -12, -15 M5M27C100K-12, -15 M5M27C101K-12, -15 M5M27C102K-12, -15 M5M27C201K, JK-10, -12, -15 M5M27C202K, JK-10, -12, -15	15 ns (When guaranteed as kit) (**Note**)	$2 \cdot f(f_2) \leq 20$ MHz
One time PROM	M5M27C256AP, FP, VP, RV-12, -15 M5M27C512AP, FP-15 M5M27C100P-15 M5M27C101P, FP, J, VP, RV-15 M5M27C102P, FP, J, VP, RV-15 M5M27C201P, FP, J, VP, RV-12, -15 M5M27C202P, FP, J, VP, RV-12, -15		
Frash memory	M5M28F101P, FP, J, VP, RV-10, -12, -15 M5M28F102FP, J, VP, RV-10, -12, -15		
SRAM	M5M5256CP, FP, KP, VP, RV-55LL, -55XL, -70LL, -70XL, -85LL, -85XL, -10LL, -10XL		
	M5M5278CP, FP, J-20, -20L	8 ns	$2 \cdot f(f_2) \leq 25$ MHz
	M5M5278CP, FP, J-25, -25L	10 ns	
	M5M5278DP, J-12	6 ns	
	M5M5278DP, FP, J-15, -15L	7 ns	
	M5M5278DP, FP, J-20, -20L	8 ns	

Note: Specifications of the above memories are available if a comment of "$t_{DF}/t_{dis(OE)}$ = 15 ns, microcomputer and kit" is added.

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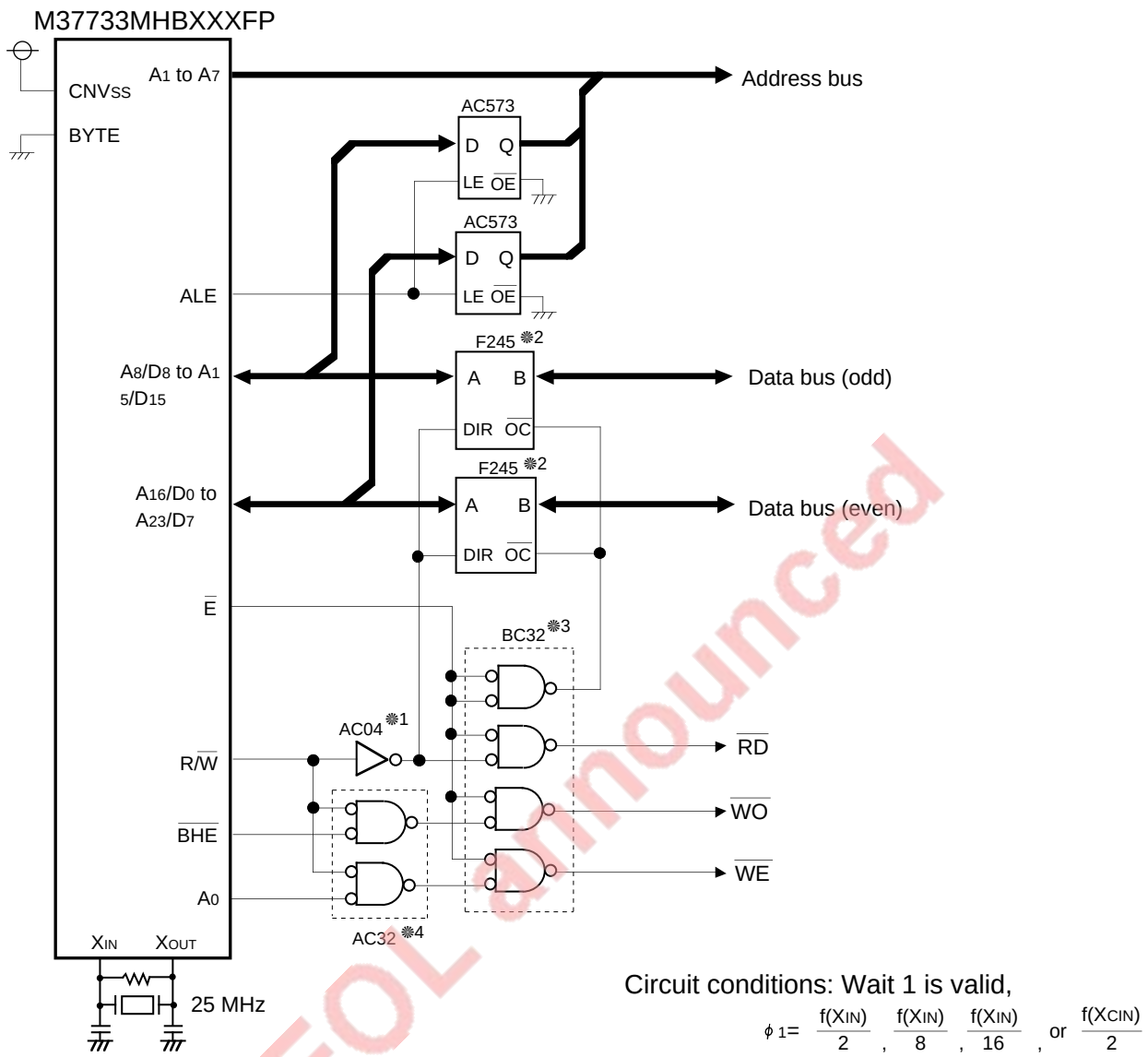

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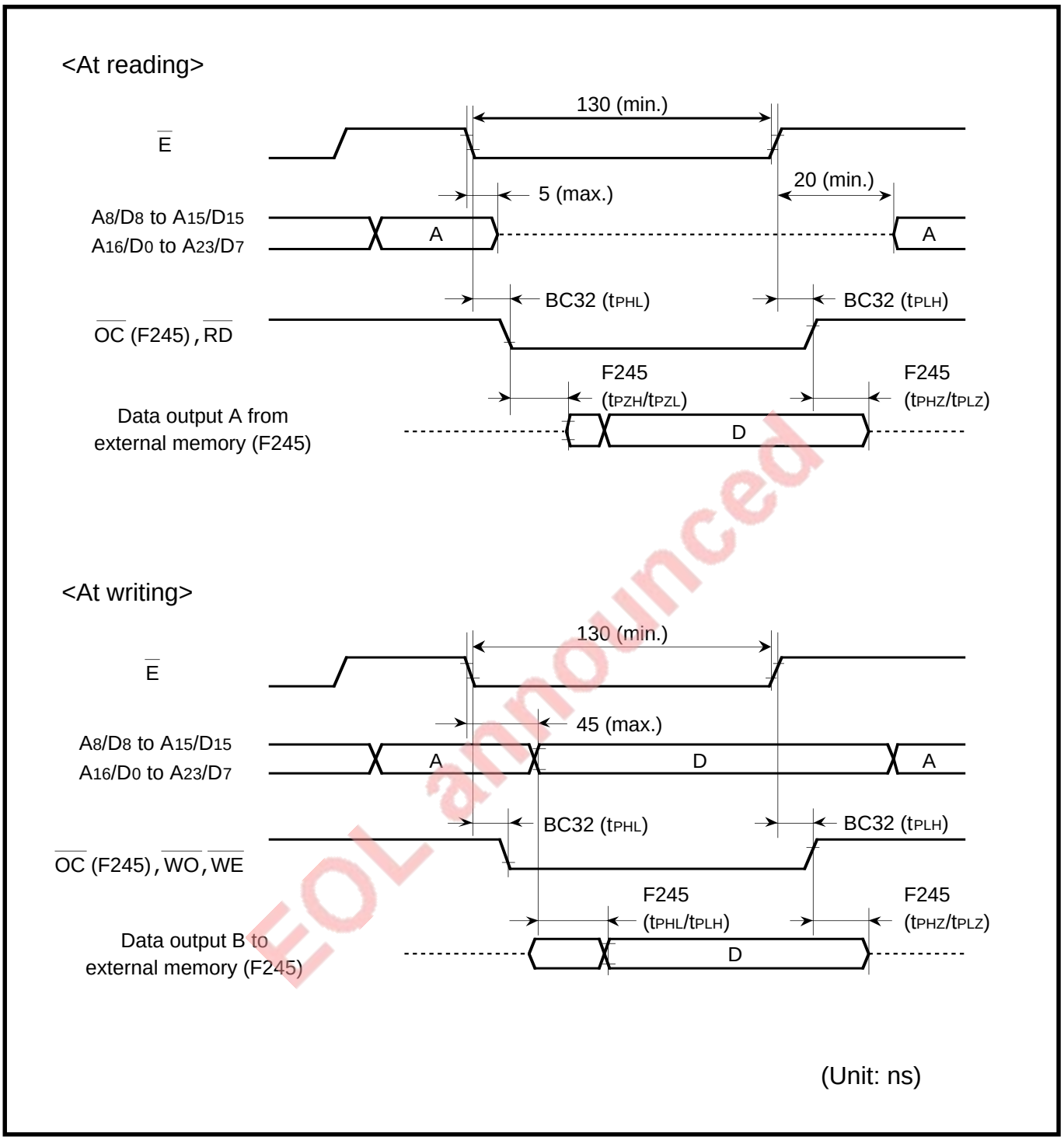
❋1 Make sure that the propagation delay time is 12 ns or less.
❋2, ❋3 Make sure that the following relationships are satisfied:
- The sum of output disable time of ❋2 and propagation delay time of ❋3 is 20 ns or less.
- The sum of output enable time of ❋2 and propagation delay time of ❋3 is 5 ns or more.

❋4 Make sure that the propagation delay time is 12 ns or less.

Fig. 17.1.9 Bus buffer usage example (1)

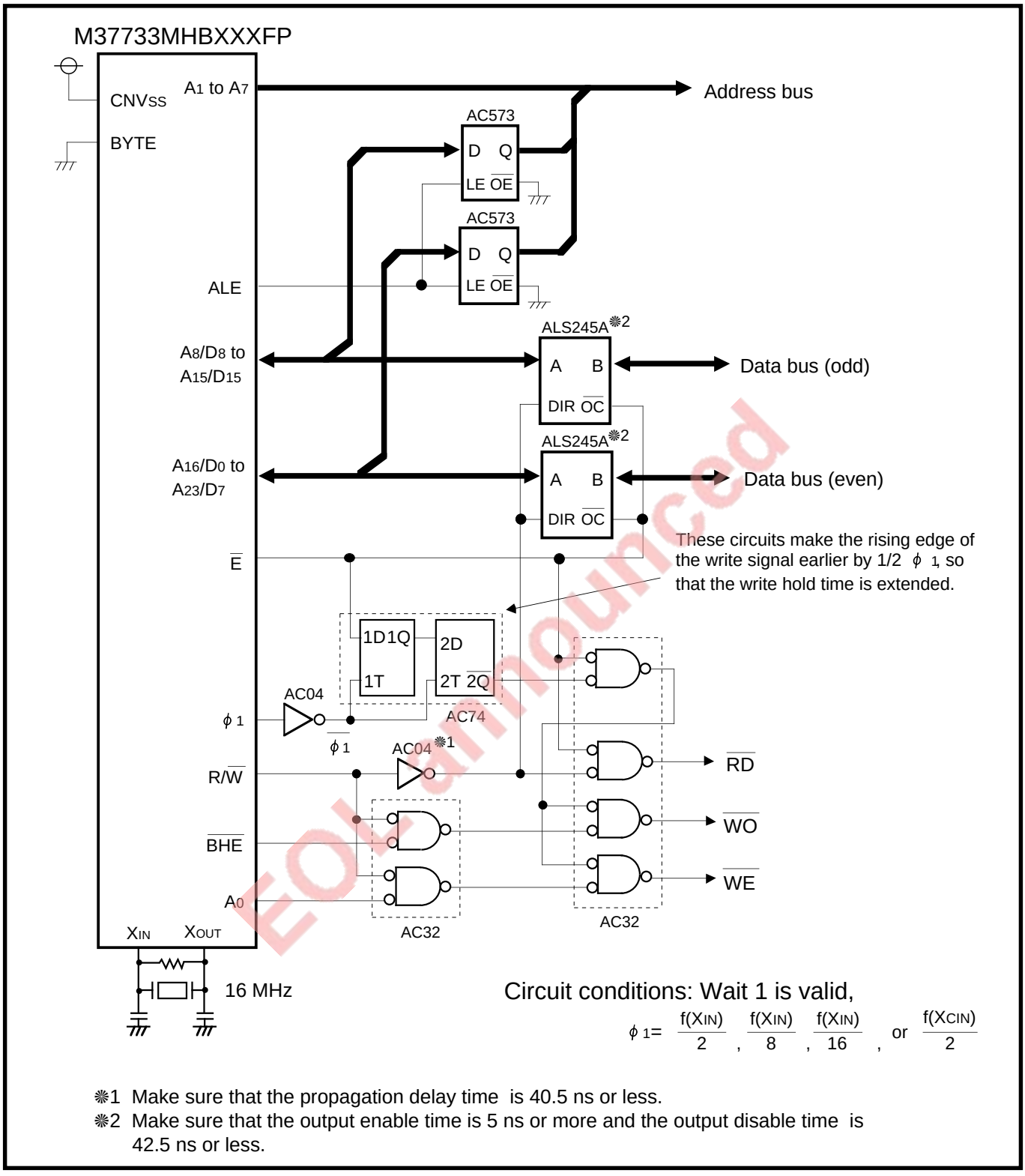
APPLICATIONS

17.1 Memory expansion



EOL announced

Fig. 17.1.10 Timing diagram for bus buffer usage example (1)



※1 Make sure that the propagation delay time is 40.5 ns or less.
※2 Make sure that the output enable time is 5 ns or more and the output disable time is 42.5 ns or less.

Fig. 17.1.11 Bus buffer usage example (2) (when a memory which requires a long data hold time for writing is connected)

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APPLICATIONS

17.1 Memory expansion

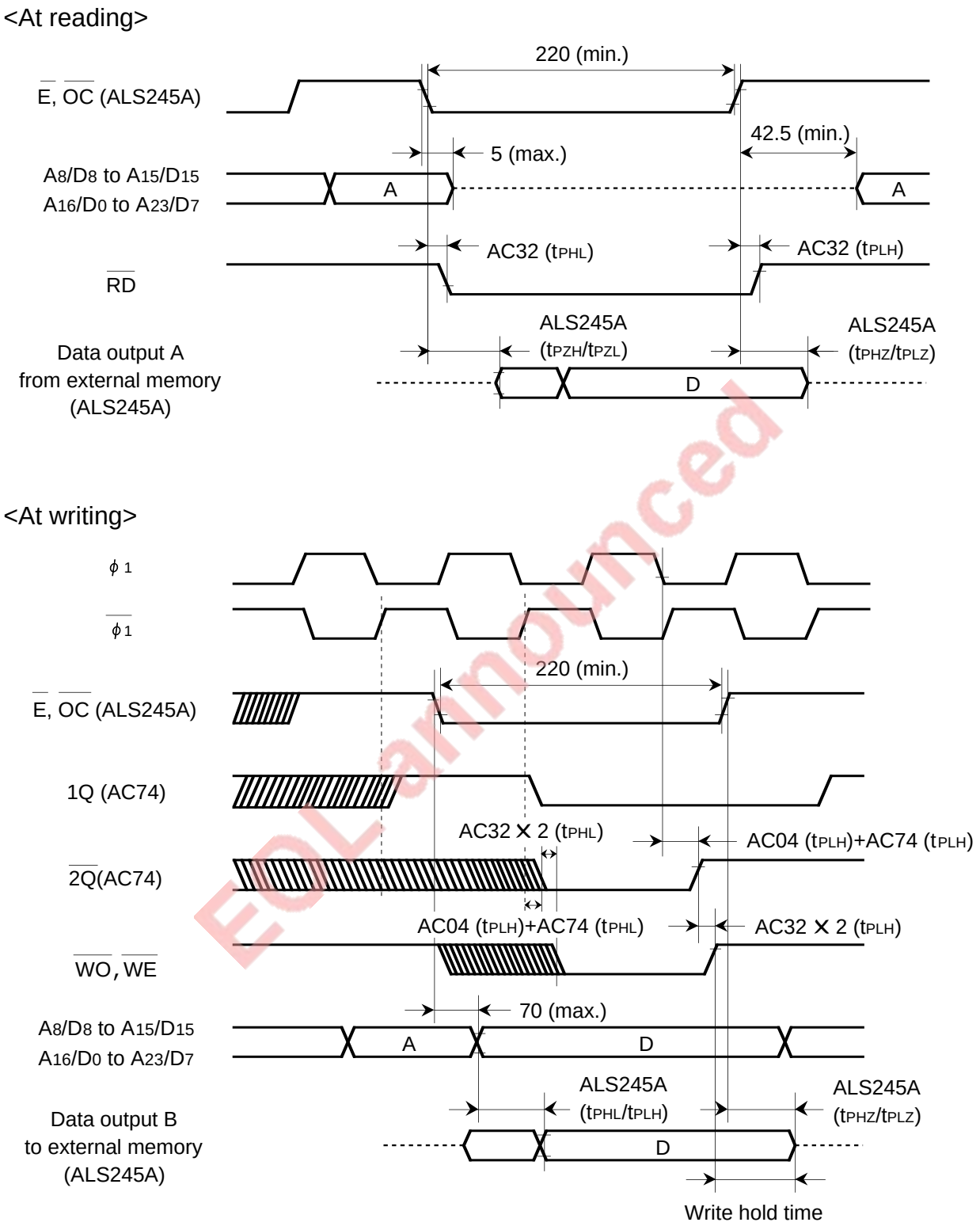

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Fig. 17.1.12 Timing diagram for bus buffer usage example (2)

17.1.4 Memory expansion example

(1) ROM expansion example on minimum model

Figure 17.1.3 shows a ROM expansion example on the minimum model (with a 32-Kbyte ROM, memory expansion mode). Figure 17.1.4 shows the corresponding timing diagram.

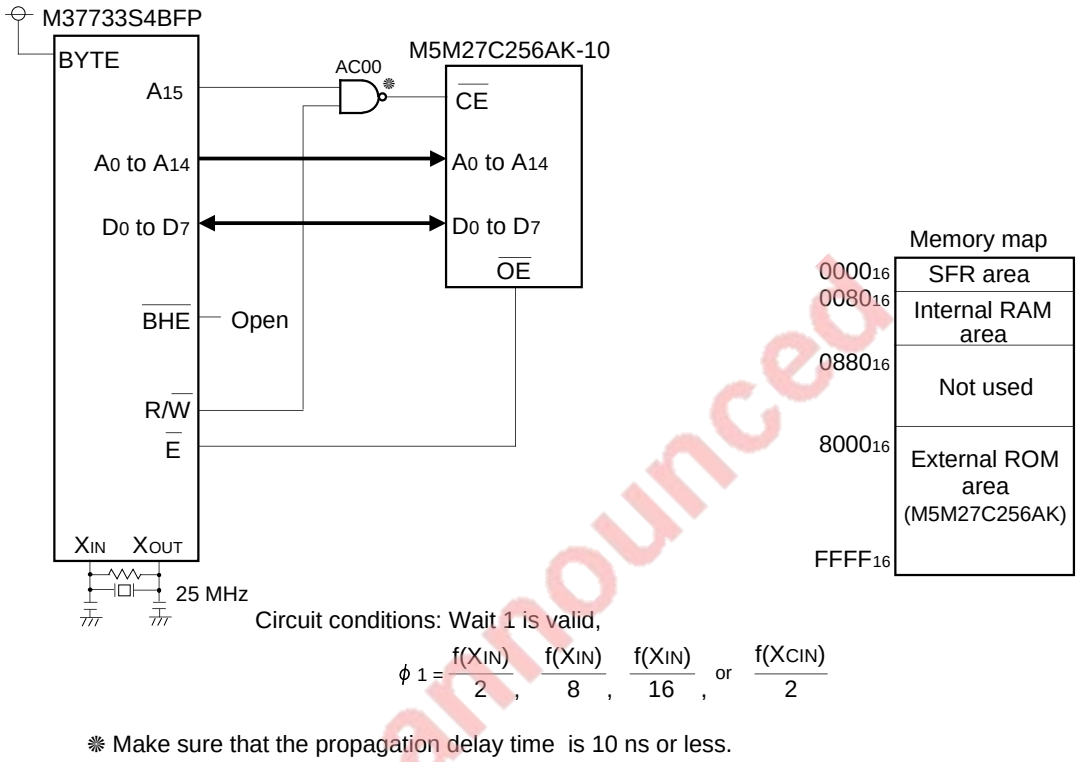

Fig. 17.1.13 ROM expansion example on minimum model

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APPLICATIONS

17.1 Memory expansion

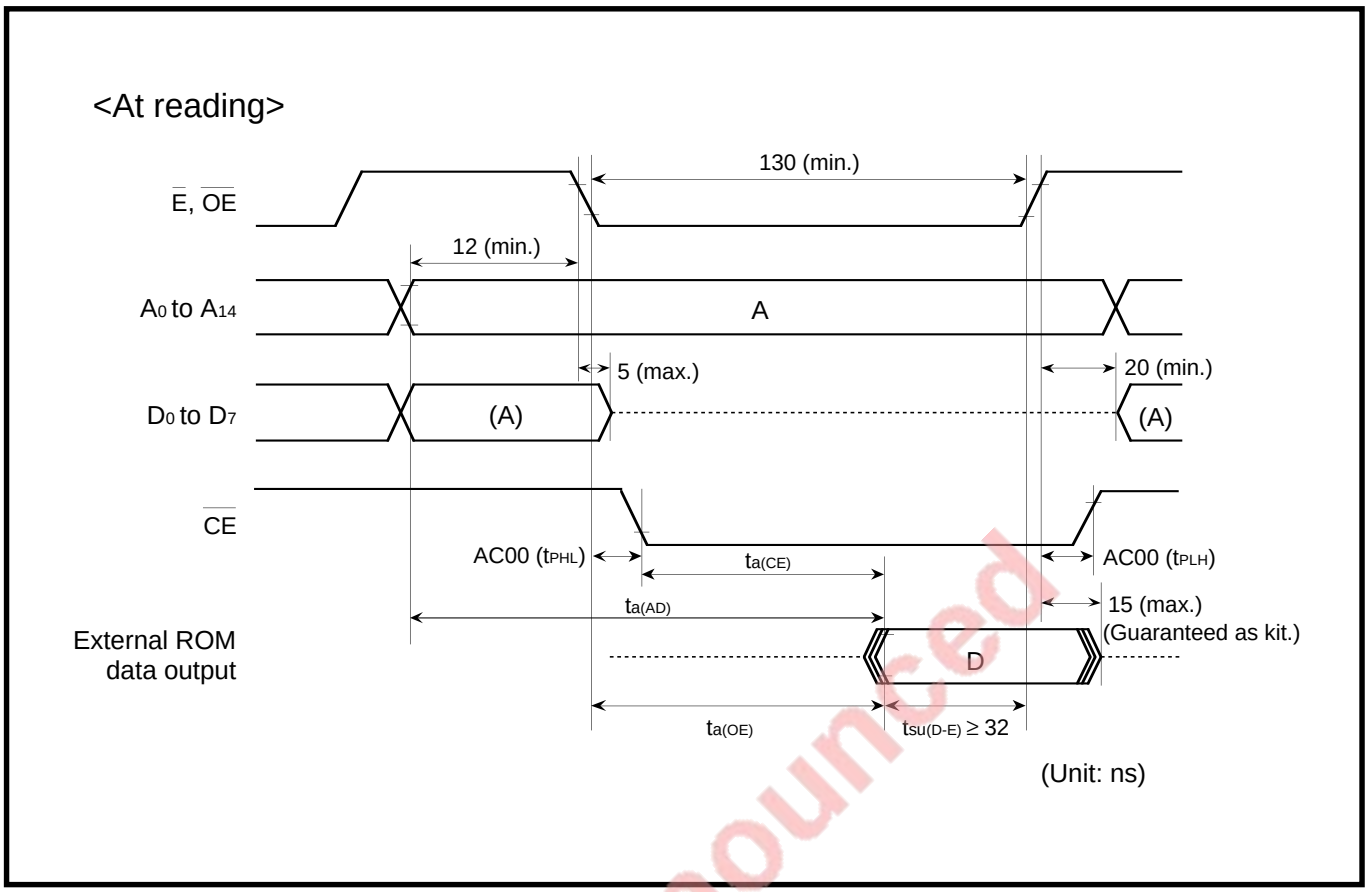

Fig. 17.1.14 Timing diagram for ROM expansion example on minimum model

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(2) ROM expansion example on maximum model

Figure 17.1.5 shows a ROM expansion example on the maximum model (with a 2-Mbit ROM, microprocessor mode). Figure 17.1.6 shows the corresponding timing diagram.

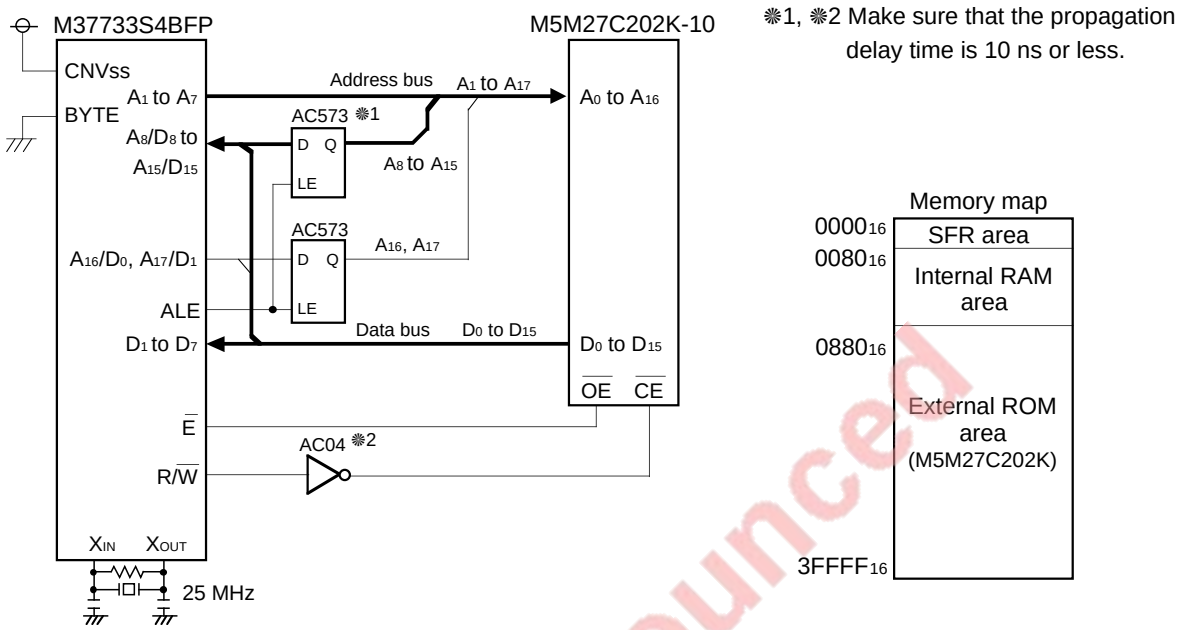

Fig. 17.1.15 ROM expansion example on maximum model

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APPLICATIONS

17.1 Memory expansion

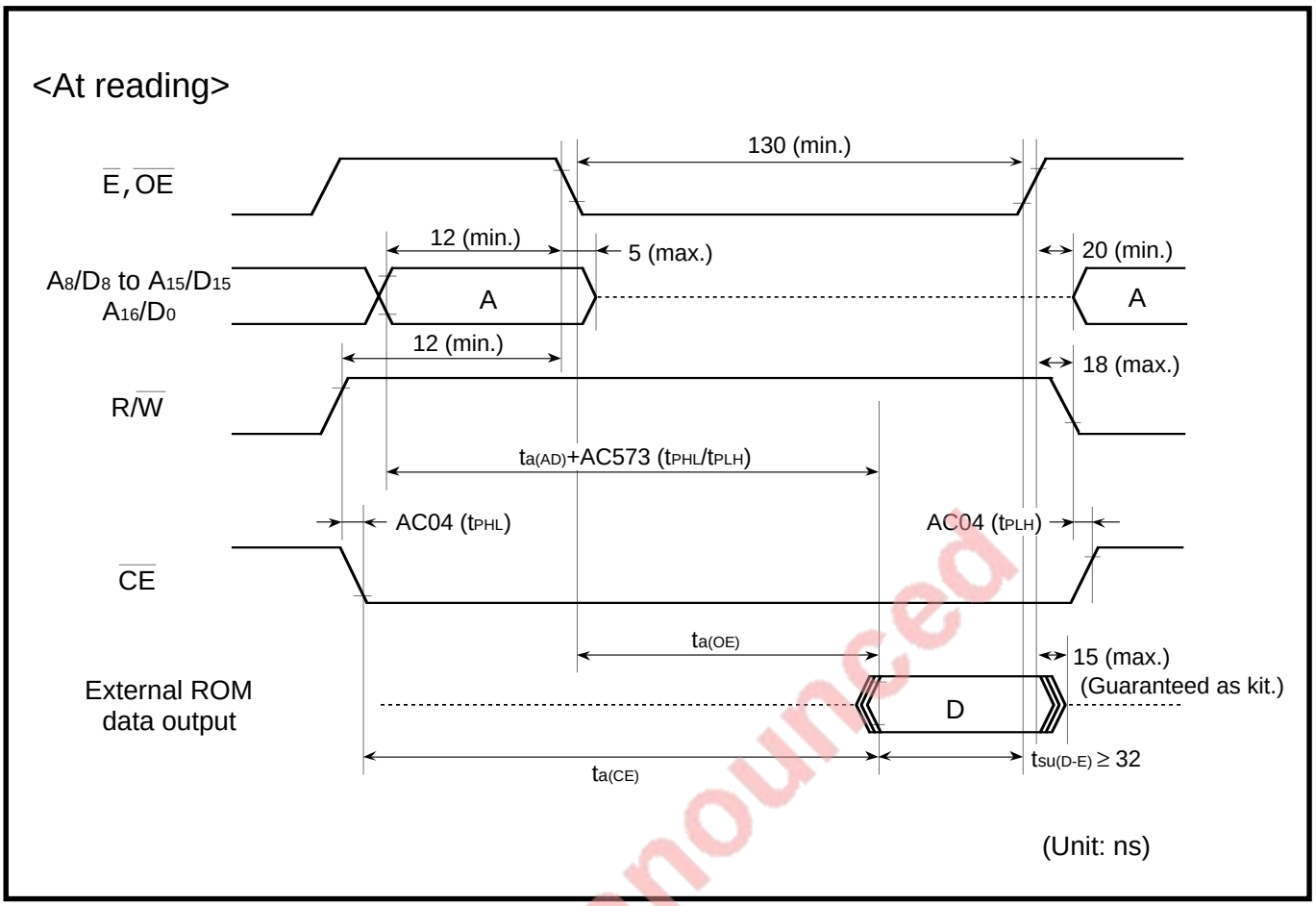
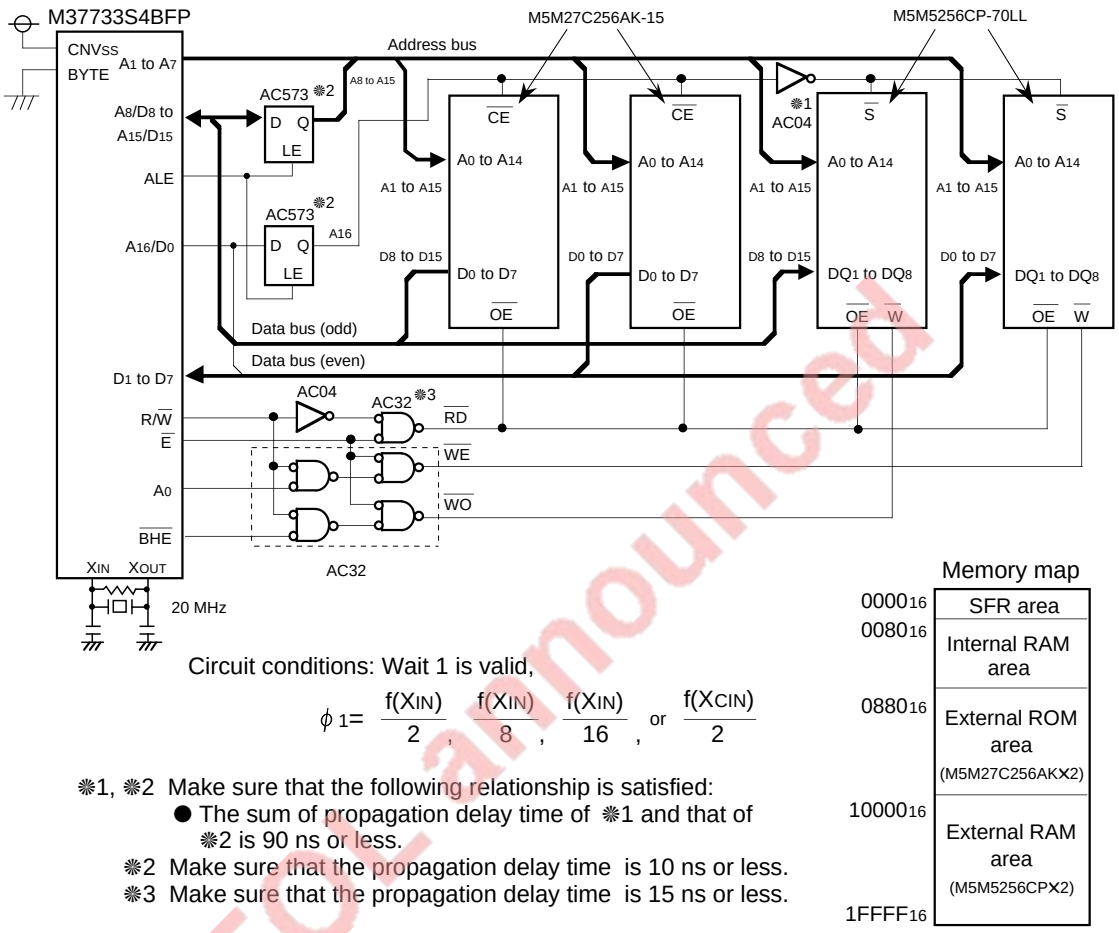


Fig. 17.1.16 Timing diagram for ROM expansion example on maximum model

EOL announced

(3) ROM and SRAM expansion example on maximum model

Figure 17.1.17 shows an expansion example for ROM and SRAM on the maximum model (with two 32-Kbyte ROMs and two 32-Kbyte SRAMs, microprocessor mode). Figure 17.1.18 shows the corresponding timing diagram.



EC announced

Fig. 17.1.17 Expansion example for ROM and SRAM on maximum model

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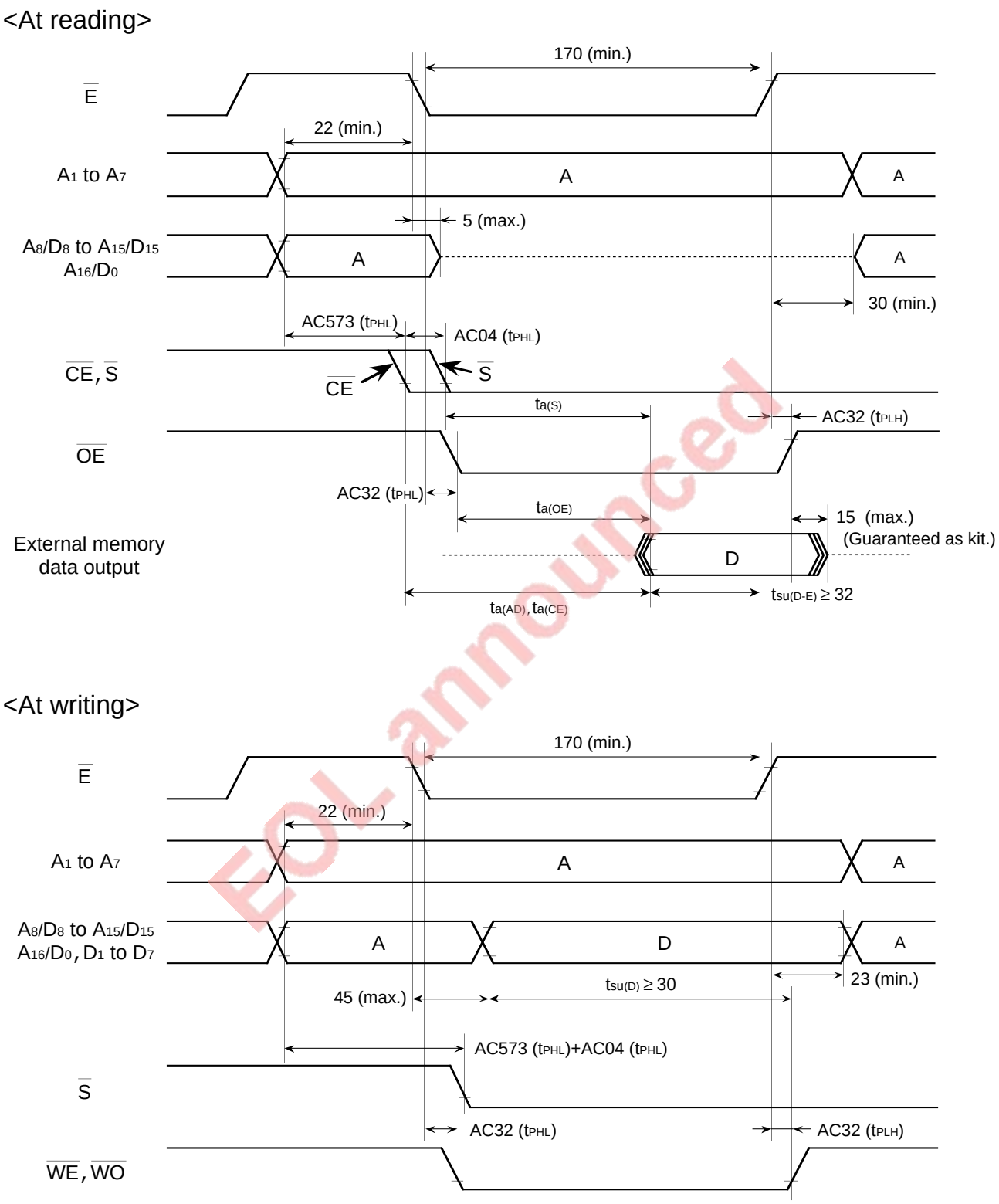
17.1 Memory expansion



EOL announced

Fig. 17.1.18 Timing diagram for ROM and SRAM expansion example on maximum model

17.1.5 I/O expansion example

(1) Port expansion example where the M66010FP is used

Fig. 17.1.19 shows a port expansion example where the M66010FP is used. The frequency of a transmit clock for serial I/O must be 1.923 MHz or less.
Serial I/O control in this expansion example is described below.
In this expansion example, 8-bit data transmission/reception is performed three times by using UART0, and so ports expand by 24 bits. UART0 is set as follows:

- Clock synchronous serial I/O mode is selected. Transmission/Reception is enabled.
- An internal clock is selected. Transfer rate = 1.5625 MHz
- LSB first is selected.

The control procedure is as follows:

① "L" level is output from port $P4_5$.
(By this signal, the expanded I/O ports of the M66010FP enter a floating state.)
② "H" level is output from port $P4_5$.
③ "L" level is output from port $P4_4$.
④ 24-bit data is transmitted/received using UART0.
⑤ "H" level is output from port $P4_4$.

Fig. 17.1.20 shows the timing of serial transfer between the M37733MHBXXXFP and M66010FP.

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APPLICATIONS

17.1 Memory expansion

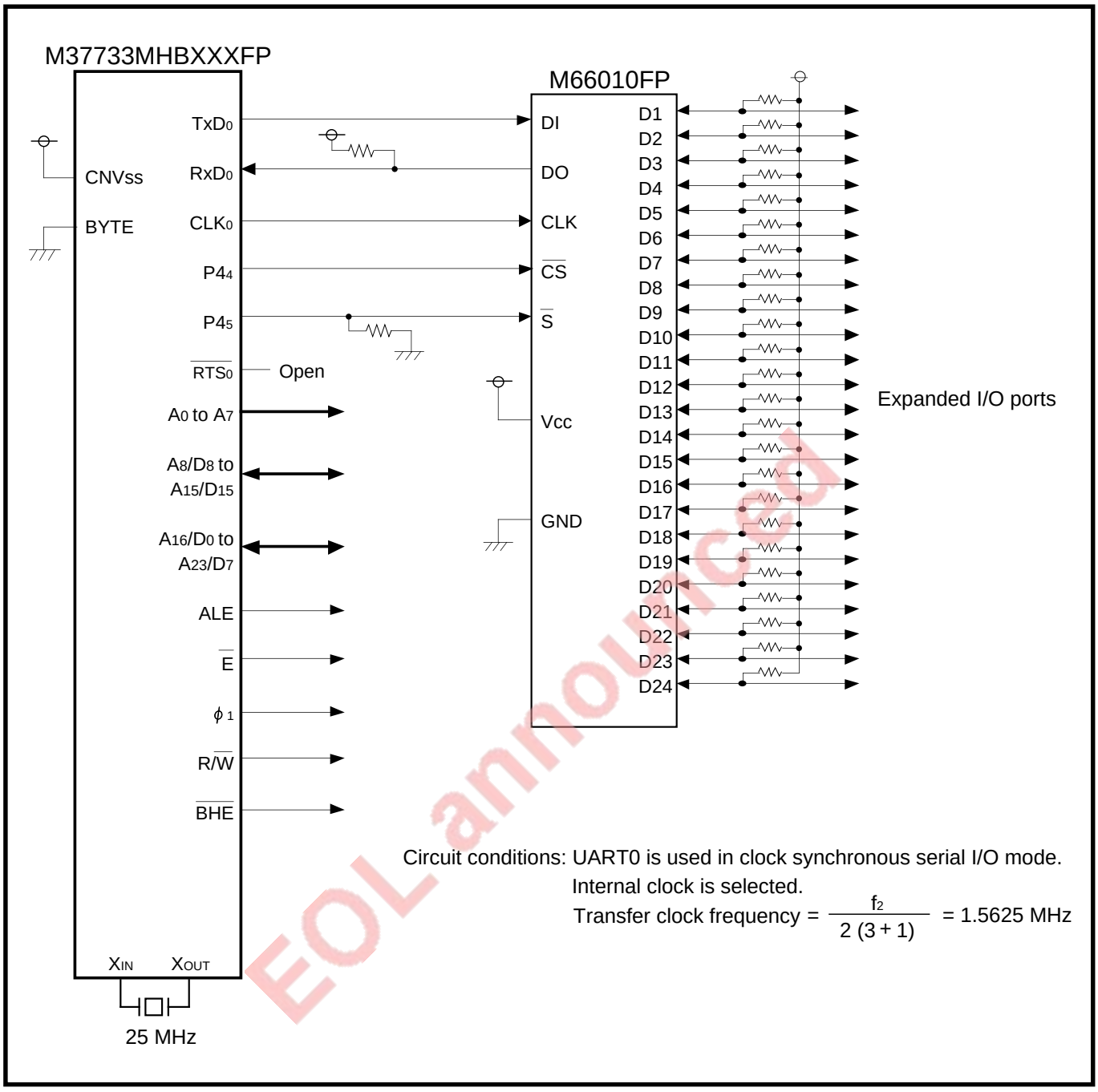

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Fig. 17.1.19 Port expansion example where M66010FP is used

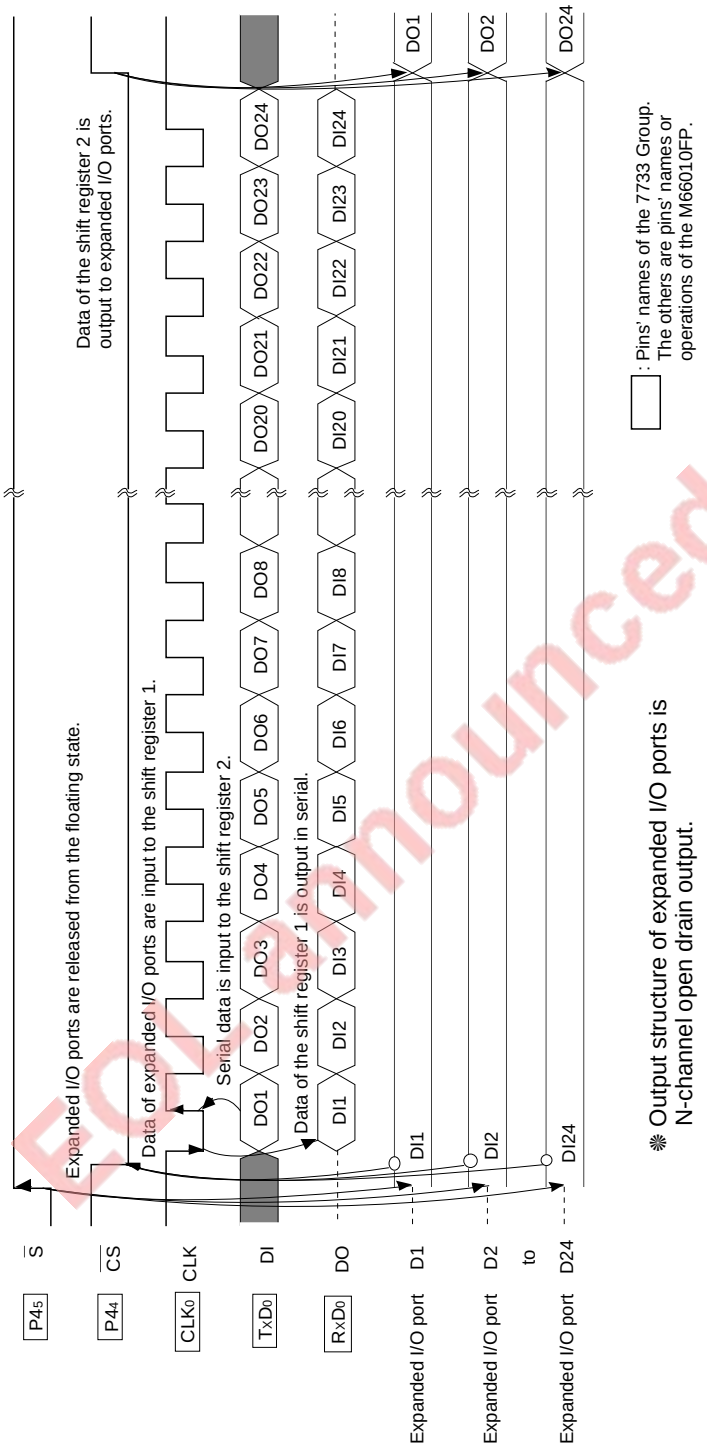

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Fig. 17.1.20 Timing of serial transfer between M37733MHBXXXFP and M66010FP

17.2 Serial I/O

Examples for serial I/O are described below:

•Examples where the microcomputer is connected with an external device by using serial I/O

•Examples where serial data is transmitted and received

17.2.1 Connection examples with external device (Clock synchronous serial I/O mode)

(1) Connection with peripheral ICs

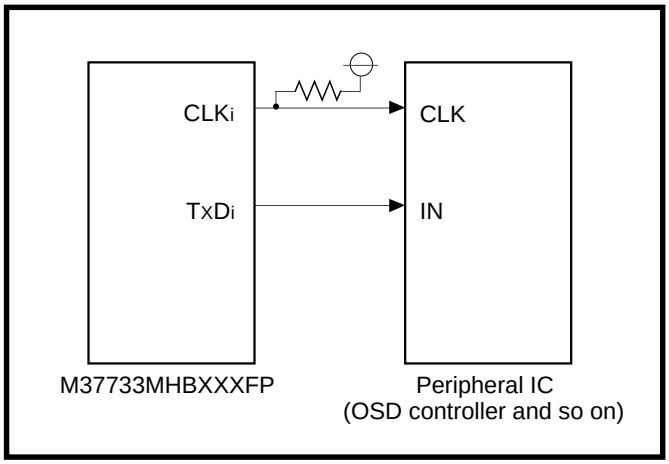

Fig. 17.2.1 Example where only transmission is performed

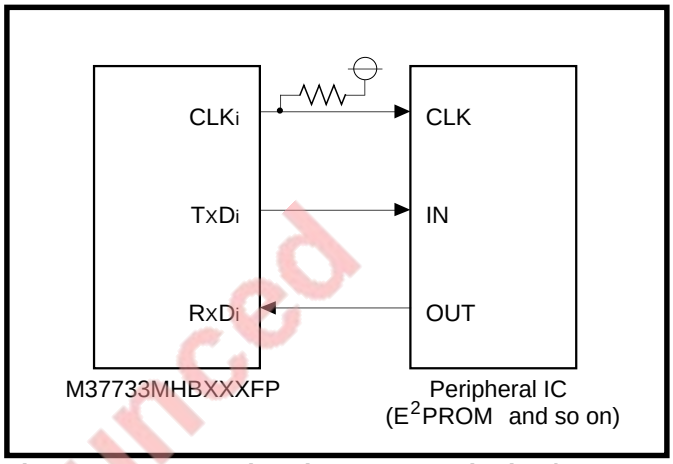

Fig. 17.2.2 Example where transmission/reception is performed

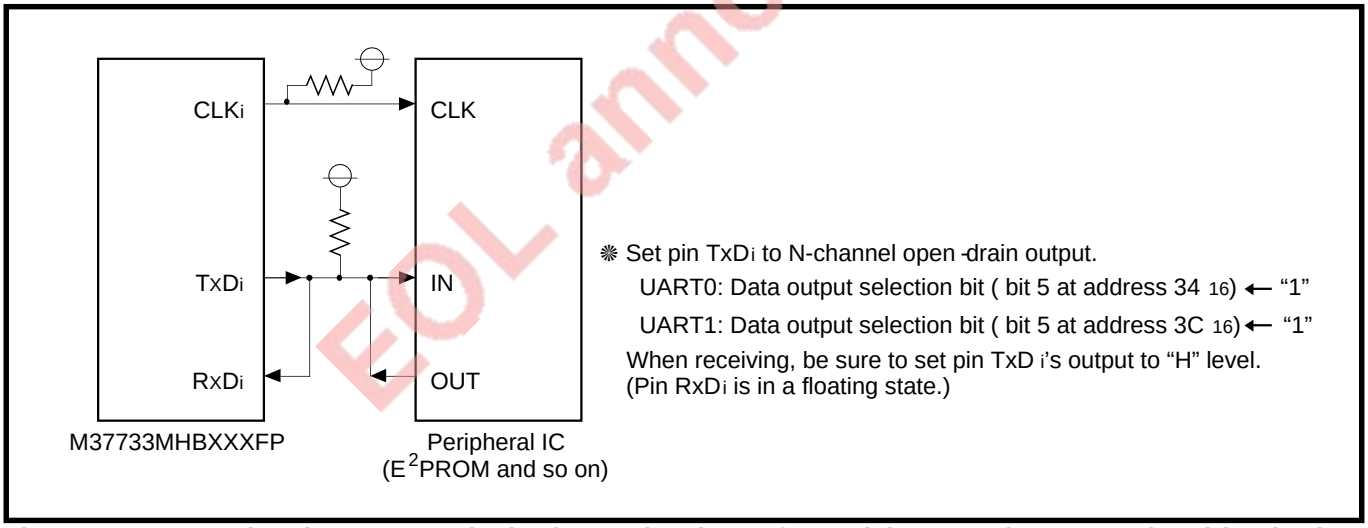

Fig. 17.2.3 Example where transmission/reception is performed (Connection example with wired-OR)

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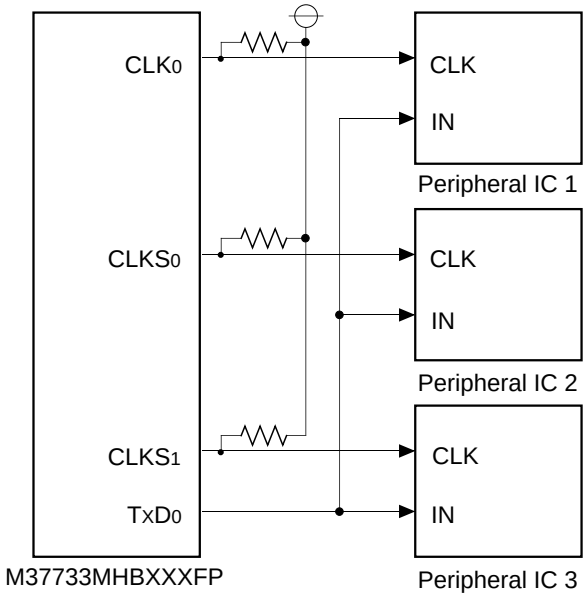


❋ One of three transmit clock output pins, which is selected by software, outputs a transmit clock.
Multiple transmit clock output pins can be used only when the following conditions are satisfied:
- Clock synchronous serial I/O mode is selected.
- Internal clock is selected.
- Only transmission is performed with UART0 used.

Fig. 17.2.4 Case where transmission for several peripheral devices is performed with 1-channel serial I/O used

(2) Connection with microcomputer

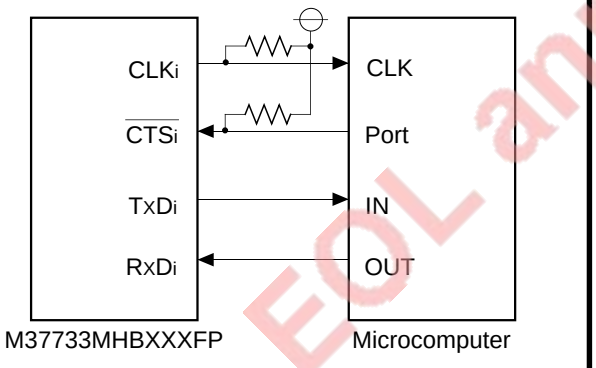
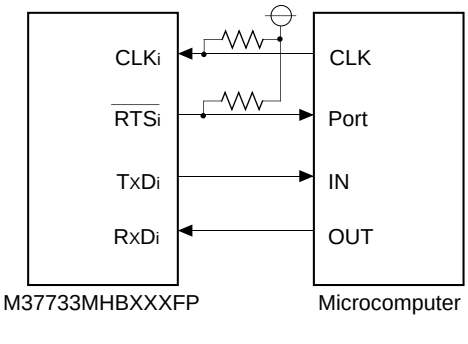


Fig. 17.2.5 Case where internal clock is selected



Note: The $\overline{\text{RTS}}$ output function is not assigned for UART2.

Fig. 17.2.6 Case where external clock is selected

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APPLICATIONS

17.2 Serial I/O

17.2.2 Examples of transmission for several peripheral ICs (Clock synchronous serial I/O mode)

In this example, transmission for three peripheral ICs is performed with UART0 used. (Note that simultaneous transmission for several peripheral ICs is disabled.)

(1) Specifications

① Clock synchronous serial I/O mode is selected.
② An internal clock is selected. Transfer rate = 2 MHz
③ MSB first is selected.
④ Transmit data is output at the falling edge of the transfer clock.
⑤ Pin TxD_0's output structure: CMOS output
⑥ Completion of transmission is determined by checking the transmission register empty flag.

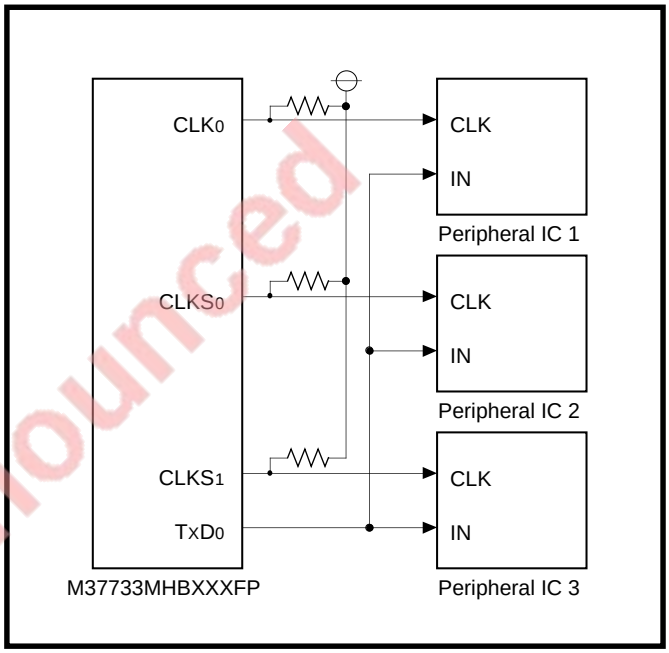

Fig. 17.2.7 Connection example

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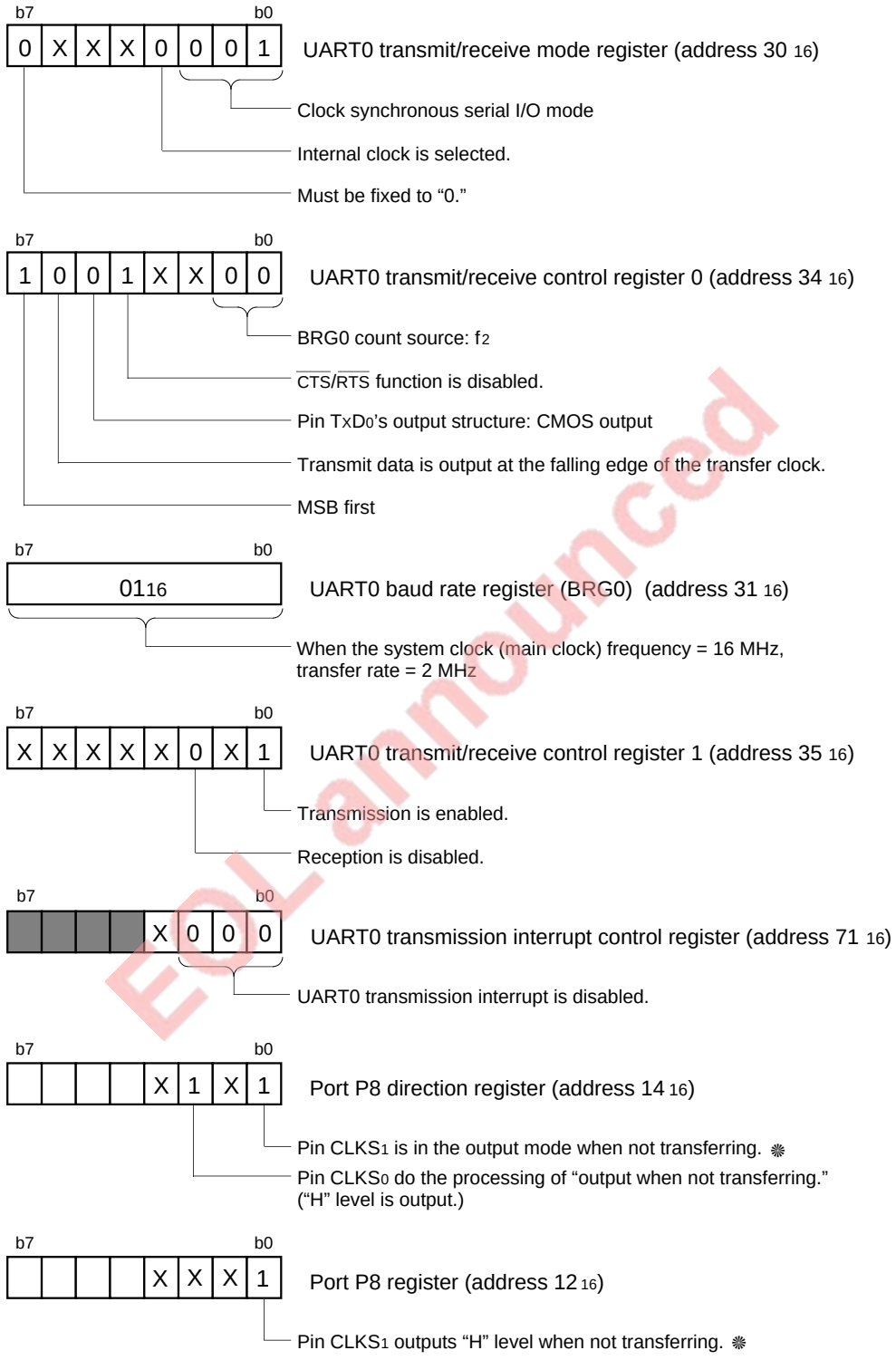
(2) Initial settings for related registers



✵ By this setting, pin CLKS1 functions as port P80 and outputs "H" level when not transferring, in other words, when no clock is output.

X: It may be "0" or "1."

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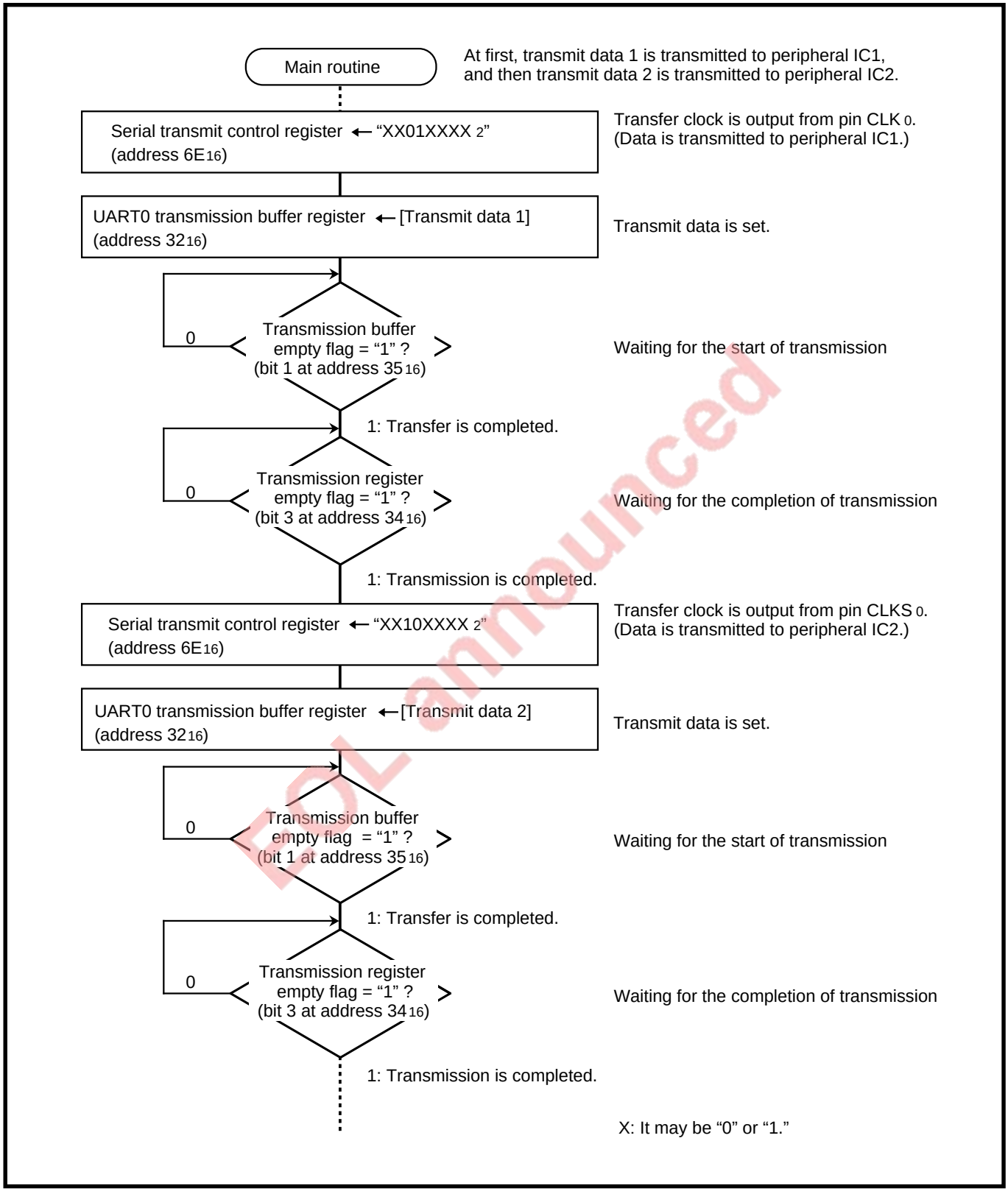
Fig. 17.2.8 Initial settings for related registers

17.2 Serial I/O

(3) Approximate flowchart



EOL announced

Fig. 17.2.9 Approximate flowchart

17.2.3 Transmission/Reception example (UART mode, transfer data length = 8 bits)

In this example, transmission/reception is performed with UART1 used (transfer data length = 8 bits).

(1) Specifications

① UART mode is selected (transfer data length = 8 bits)
② An internal clock is selected. Baud rate = 9,600 bps
③ Parity is disabled.
④ 1 stop bit is selected.
⑤ Pin TxD_1's output structure: CMOS output
⑥ The sleep mode is invalid.
⑦ Transmission start is determined by using a UART1 transmission interrupt.
⑧ Receive data is read out by using a UART1 reception interrupt.

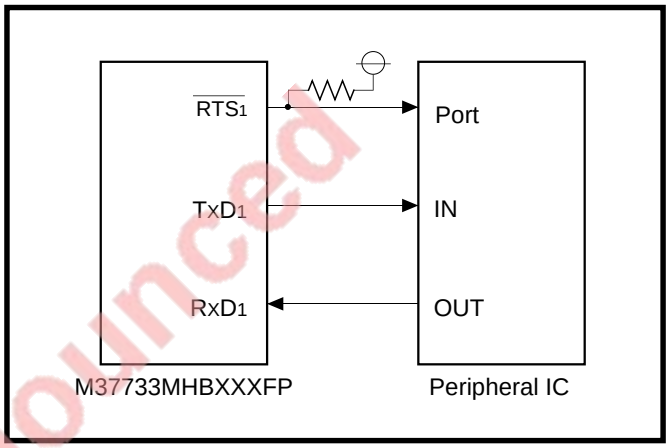


Fig. 17.2.10 Connection example

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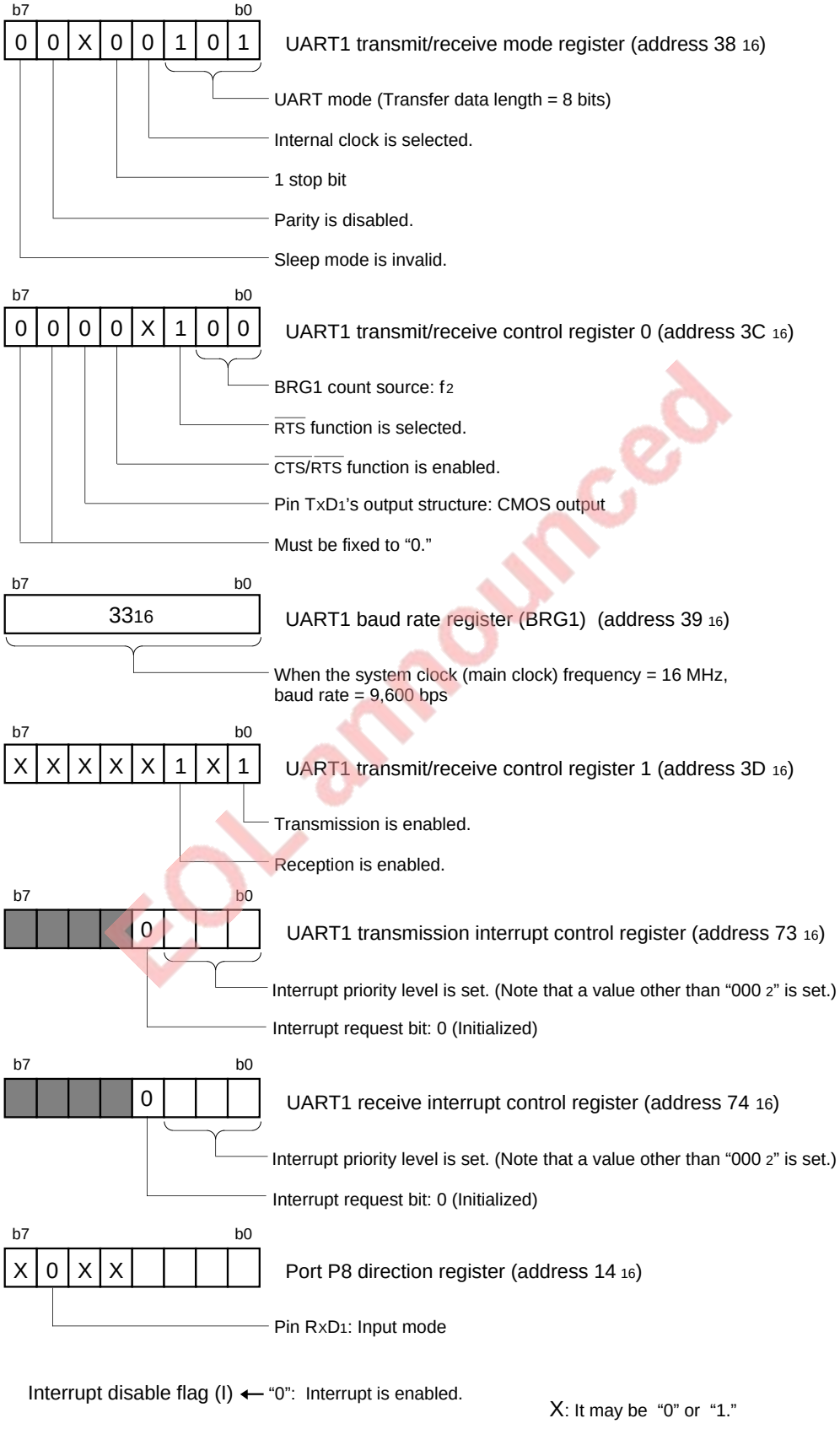
17.2 Serial I/O

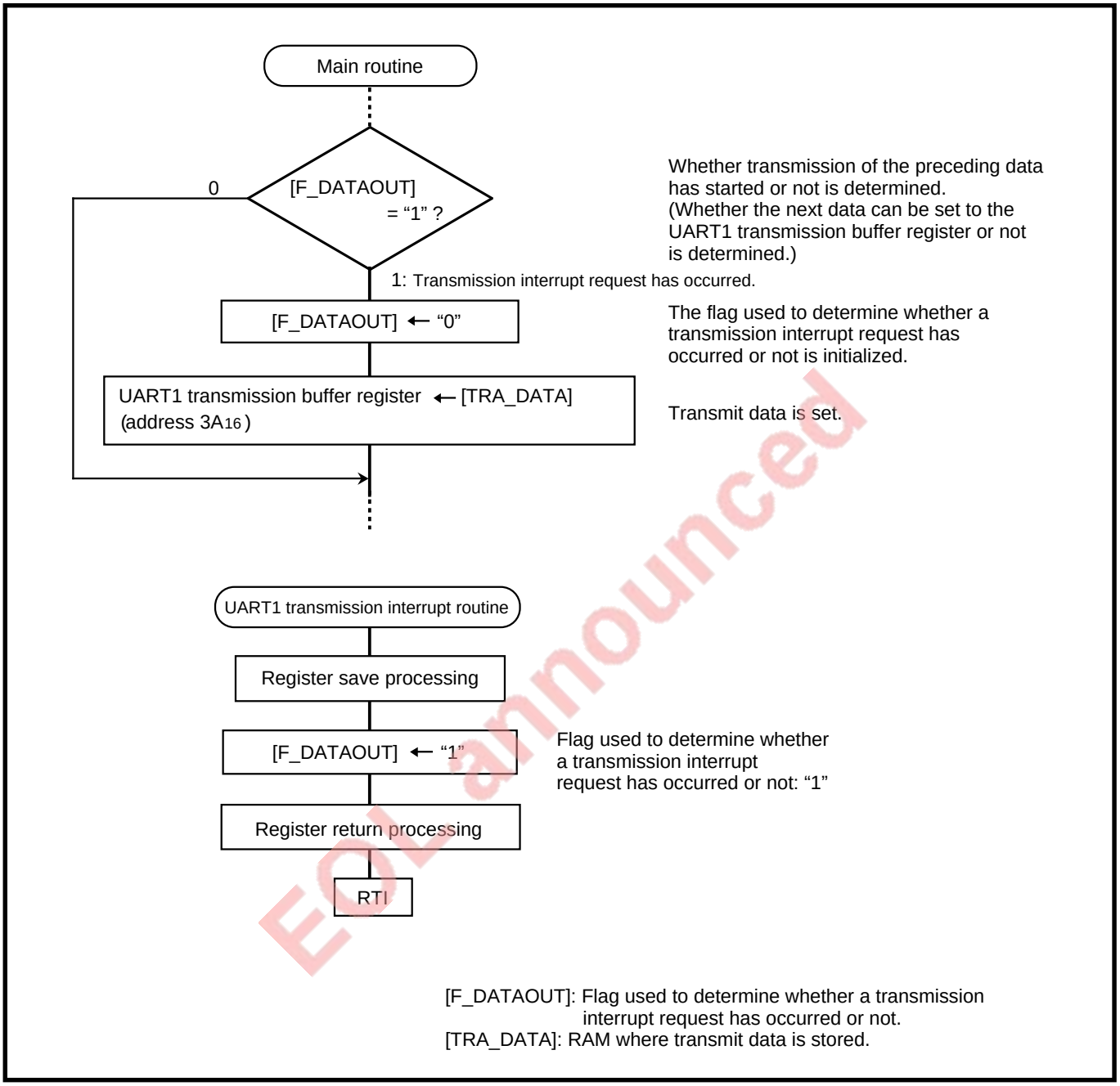
(2) Initial settings for related registers



EOL announced

Fig. 17.2.11 Initial settings for related registers

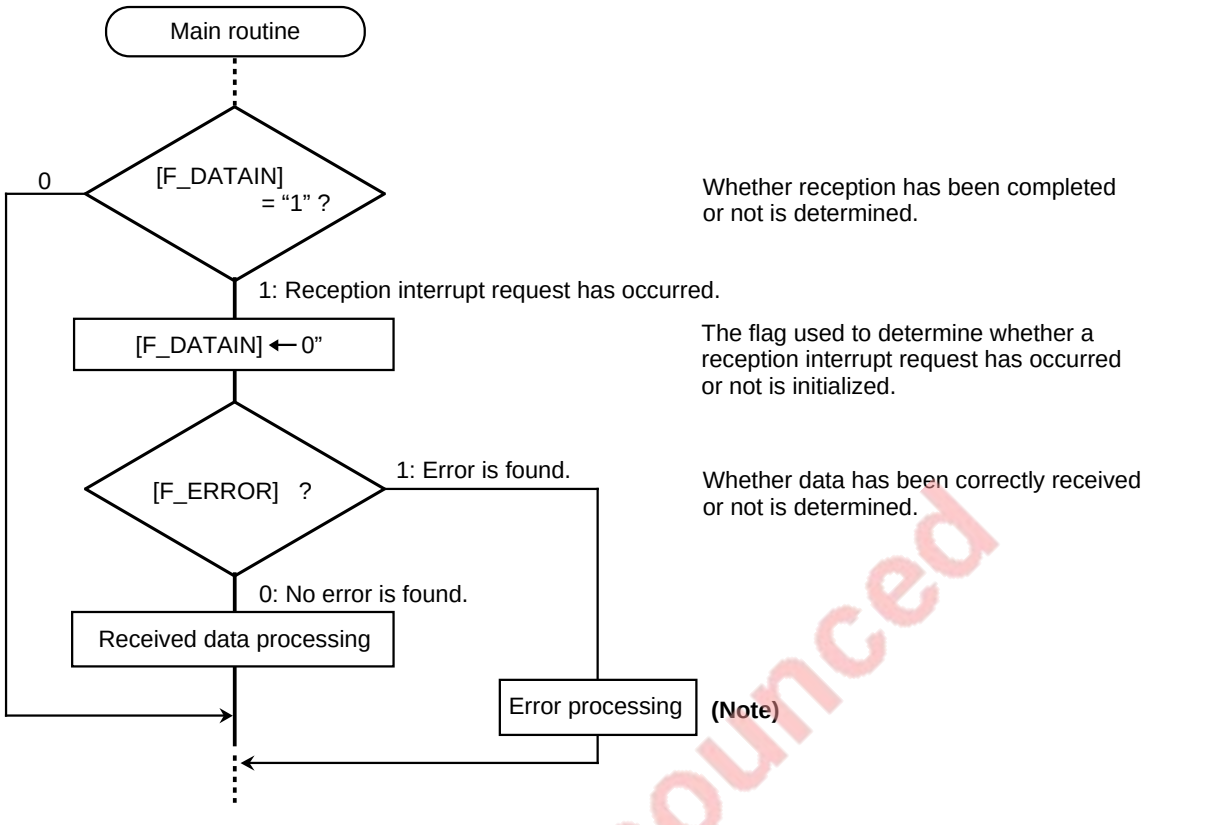
(3) Approximate flowchart



EOL announced

Fig. 17.2.12 Approximate flowchart (1)

17.2 Serial I/O



Note: When an error occurs, reception is disabled in a reception interrupt routine. Therefore, when restarting reception after error processing is completed in the main routine, make reception enabled again.

Fig. 17.2.13 Approximate flowchart (2)

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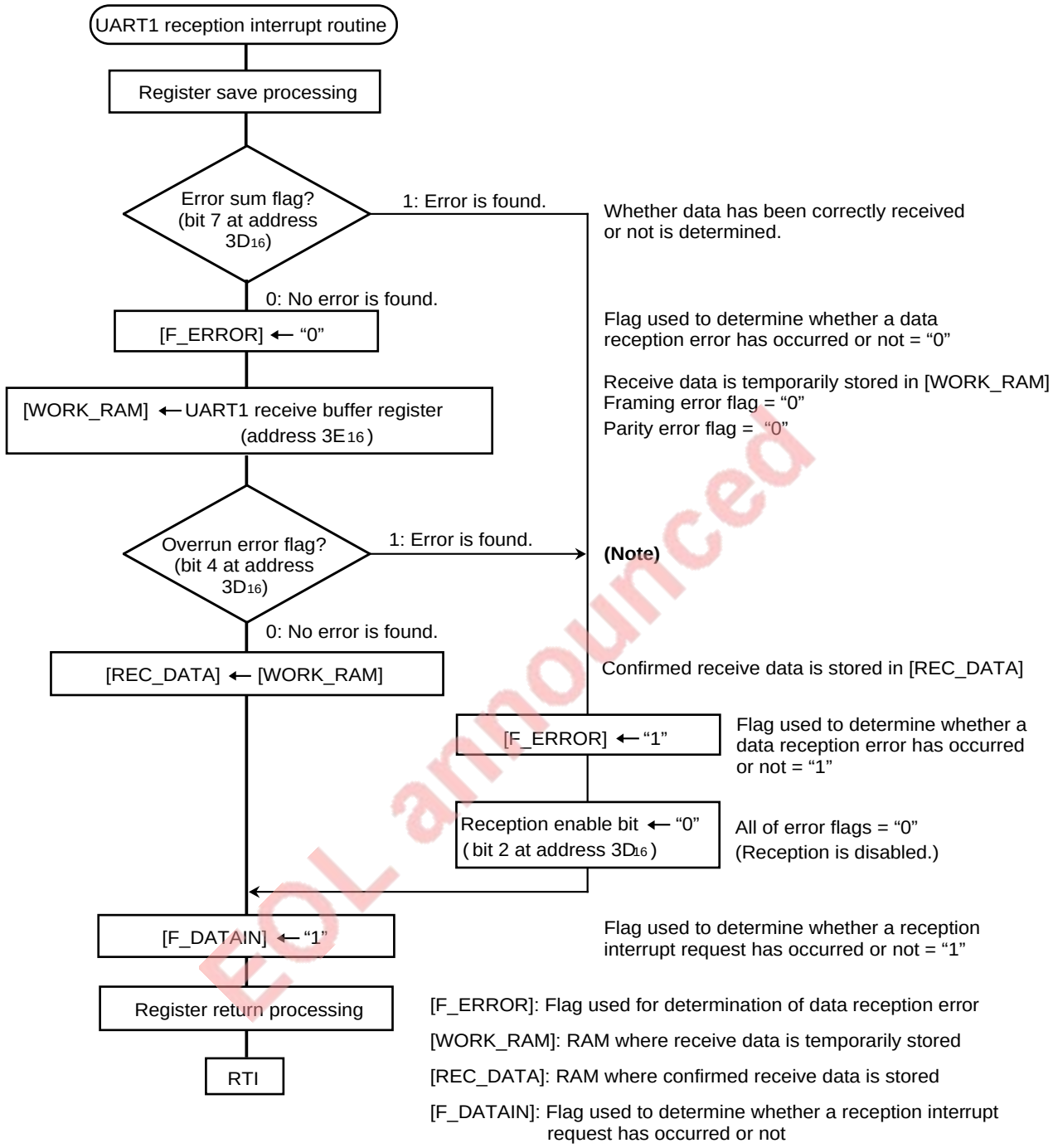

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Note: If the next data is received from when the error sum flag is checked until the contents of the UART1 receive buffer register is transferred to [WORK_RAM], an overrun error occurs.
Therefore, at this timing, the content of the overrun error flag is checked again.

Fig. 17.2.14 Approximate flowchart (3)

APPLICATIONS

17.2 Serial I/O

17.2.4 8-bit transmission example (Clock synchronous serial I/O mode)

In this example, after 8-bit data is transmitted with UART1 used, a strobe signal is output.

(1) Specifications

① Clock synchronous serial I/O mode is selected.
② An internal clock is selected. Transfer rate = 2 MHz
③ LSB first is selected.
④ Transmit data is output at the falling edge of the transfer clock.
⑤ Pin T_XD_1's output structure: CMOS output
⑥ A strobe signal is output from port $P4_3$ each time 8-bit data is transmitted. (Refer to **Figure 17.2.16.**)
⑦ Completion of the transmission is determined by checking the transmission register empty flag.

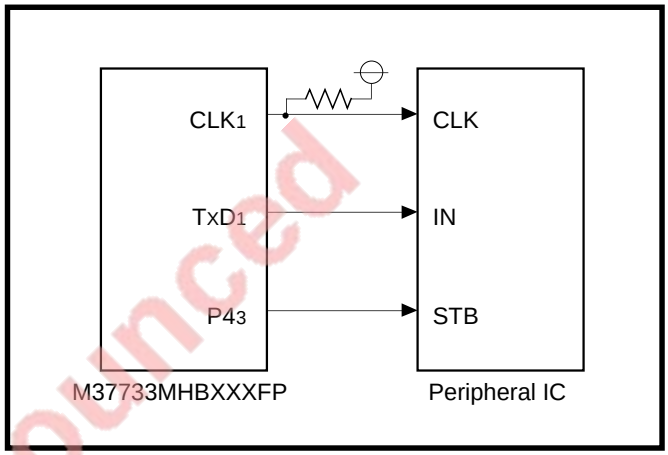

Fig. 17.2.15 Connection example

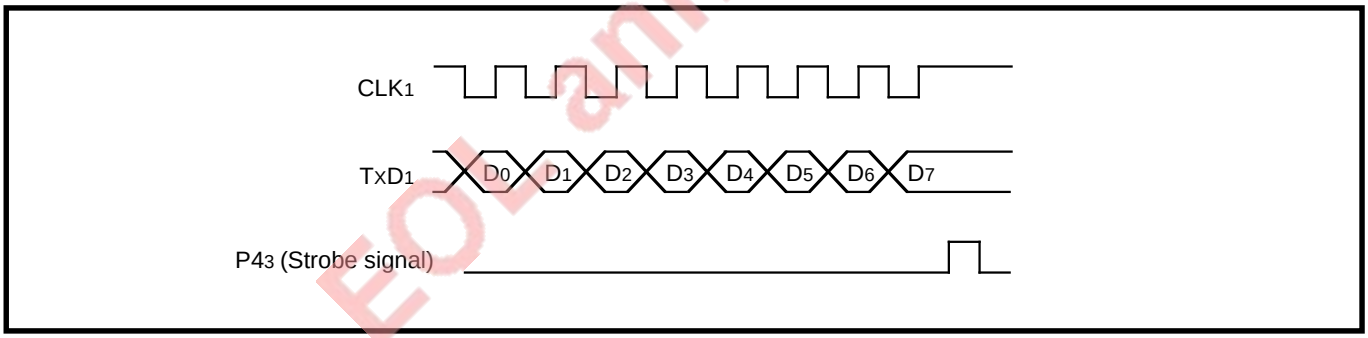

Fig. 17.2.16 Strobe signal output timing

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(2) Initial settings for related registers

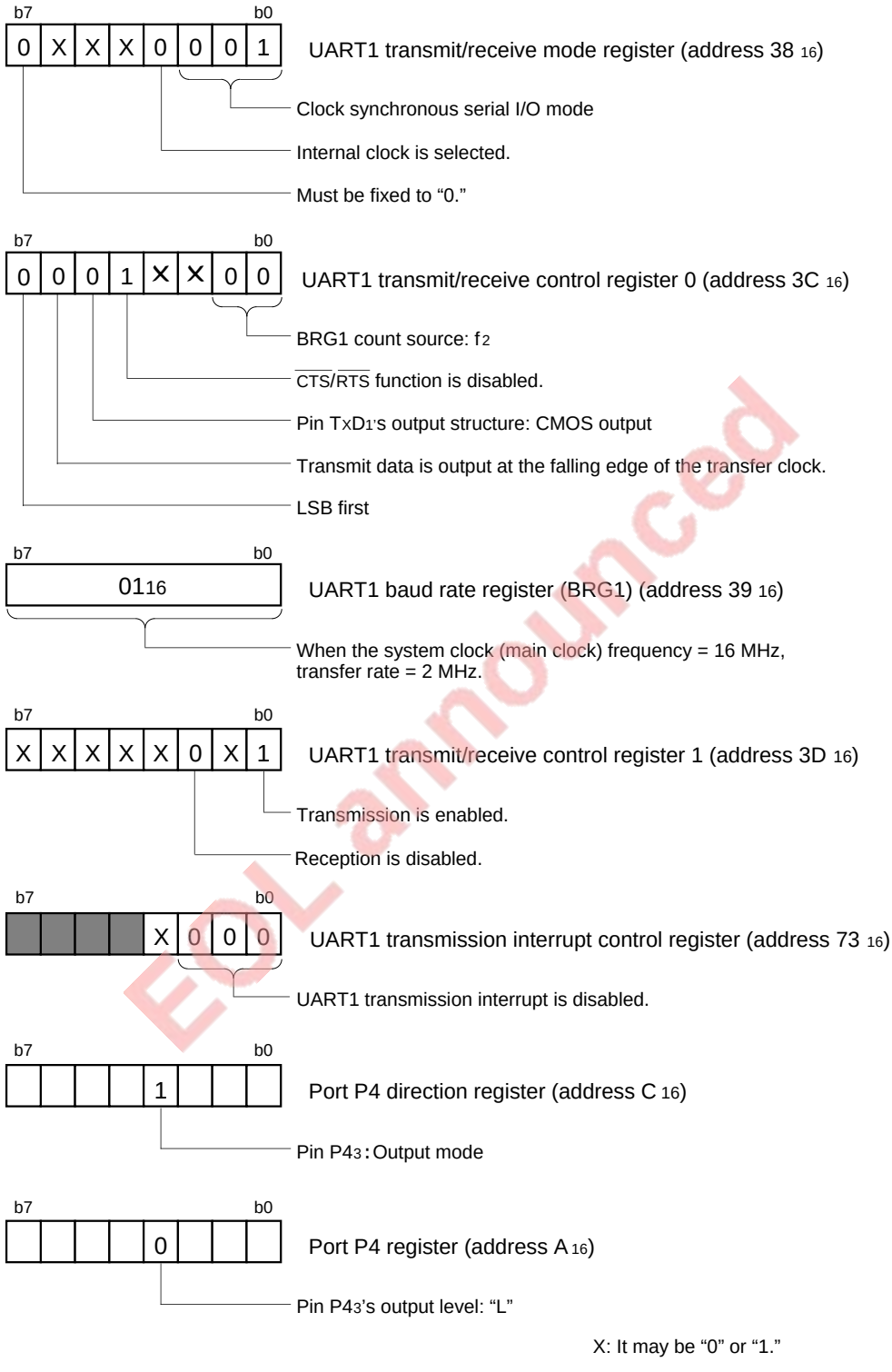

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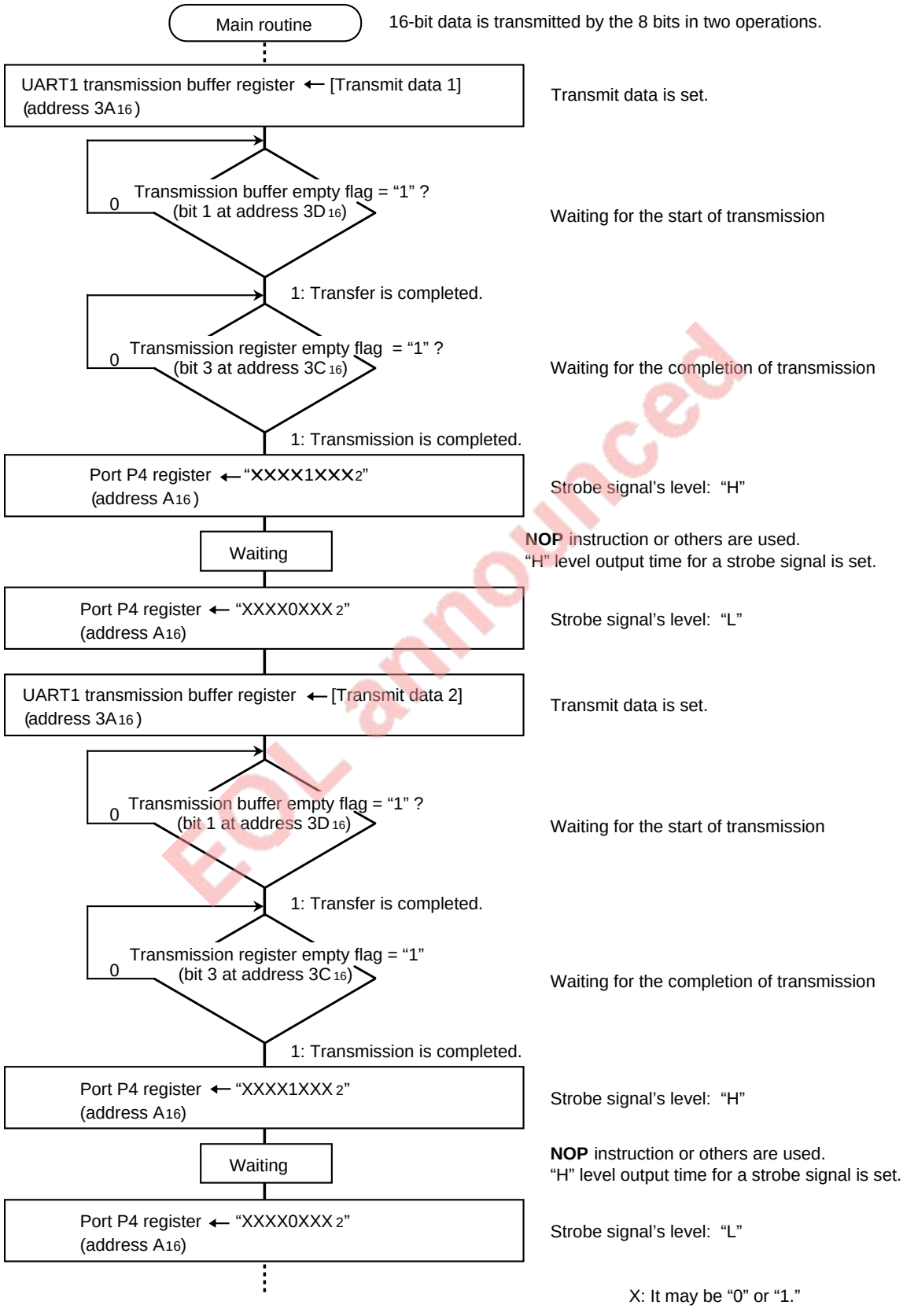
Fig. 17.2.17 Initial settings for related registers

APPLICATIONS

17.2 Serial I/O

(3) Approximate flowchart



EOL announced

Fig. 17.2.18 Approximate flowchart

17.3 Watchdog timer

A program runaway detection example with using the watchdog timer is described below.

17.3.1 Program runaway detection example

In this example, when the watchdog timer detect a program runaway, the microcomputer is reset.

(1) Specifications

① The main clock is the system clock and f(XIN) = 16 MHz.
② When an interval of 4.09 ms has passed after value "FFF16" is set, the watchdog timer issues an interrupt request. (When writing to address 6016 is not performed because of a program runaway.)
③ When a watchdog timer interrupt request occurs, the microcomputer is reset. ("Software reset" is applied.)

(2) Initial setting for related register

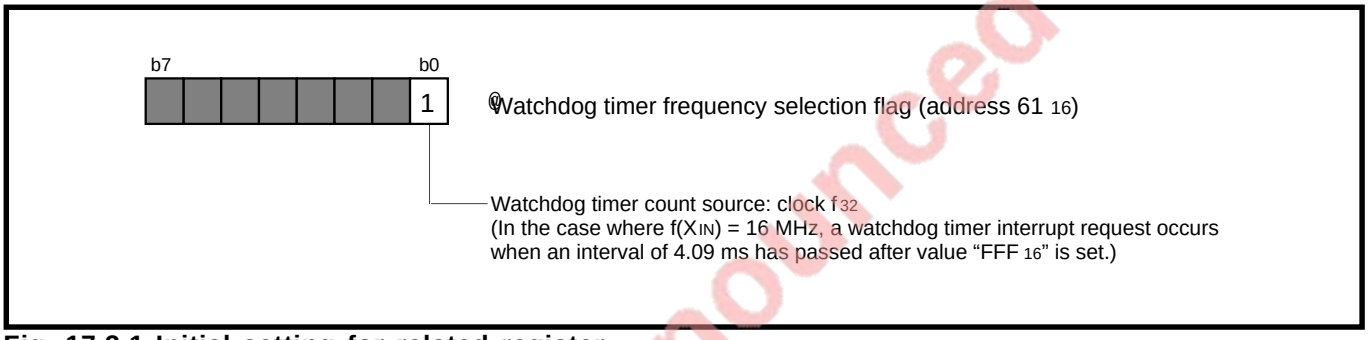


Fig. 17.3.1 Initial setting for related register

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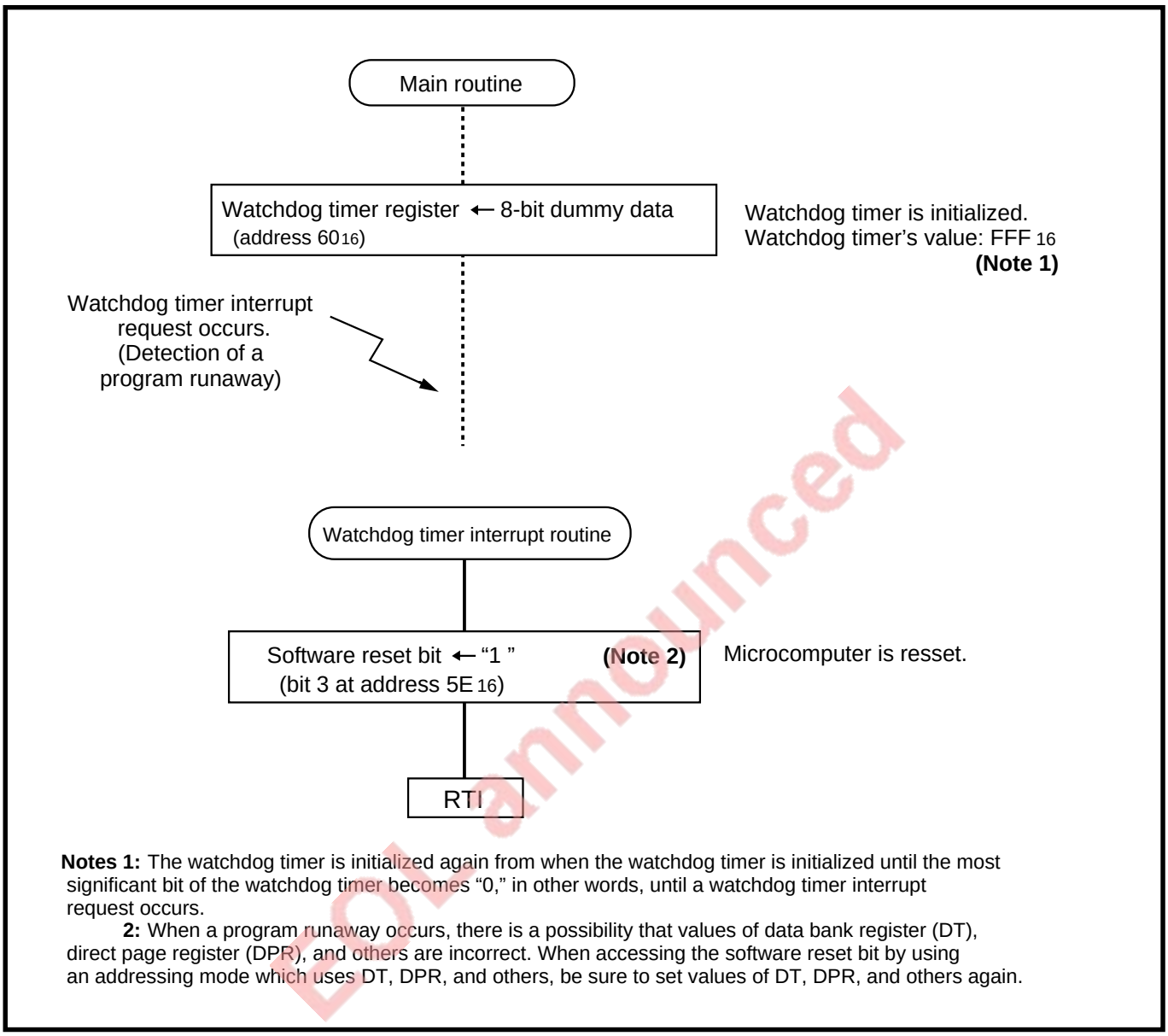
17.3 Watchdog timer

(3) Approximate flowchart



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Notes 1: The watchdog timer is initialized again from when the watchdog timer is initialized until the most significant bit of the watchdog timer becomes "0," in other words, until a watchdog timer interrupt request occurs.

2: When a program runaway occurs, there is a possibility that values of data bank register (DT), direct page register (DPR), and others are incorrect. When accessing the software reset bit by using an addressing mode which uses DT, DPR, and others, be sure to set values of DT, DPR, and others again.

Fig. 17.3.2 Approximate flowchart

(4) Precautions

1. The watchdog timer stops counting when the **STP** instruction is executed. For systems which use the watchdog timer, select "**STP** instruction disabled" with "**STP** instruction option" on "MASK ROM ORDER CONFIRMATION FORM."

2. The watchdog timer stops counting when the **WIT** instruction is executed after the system clock stop bit at wait state (bit 5 at address $6C_{16}$) is set to "1."

3. The contents of the processor interrupt priority level (IPL) is not initialized in the following cases:
   - When a value which is the same as the reset vector address's contents is set to the watchdog timer's vector address
   - When a program branches to the destination address at reset in a watchdog timer interrupt routine.

   Reset of the microcomputer is realized by applying the software reset.

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17.4 Power saving

Power saving examples (in other words, examples to save power consumption) with the stop or wait mode used are described below.

17.4.1 Power saving example with stop mode used

In this example, power saving is realized by using the stop mode. The stop mode is terminated by using the key input interrupt function.

(1) Specifications

① The microcomputer operates in the single-chip mode.
② Pins P5$_0$ to P5$_3$ are used as output pins for the key matrix scanning.
Input pins (KI$_0$ to KI$_3$) for the key input interrupt function are used as key input pins.
Pins KI$_0$ to KI$_3$ are pulled high by using the pull-up function.
③ The initial output levels of pins P5$_0$ to P5$_3$ are “L.”
④ When a key input interrupt request occurs owing to a key push, the key data is read-in. (This reading is surely performed independent of power saving.)
⑤ In the stop mode, interrupts other than a key input interrupt are disabled.
⑥ An external clock is used as the main clock.

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(2) Initial settings for related registers

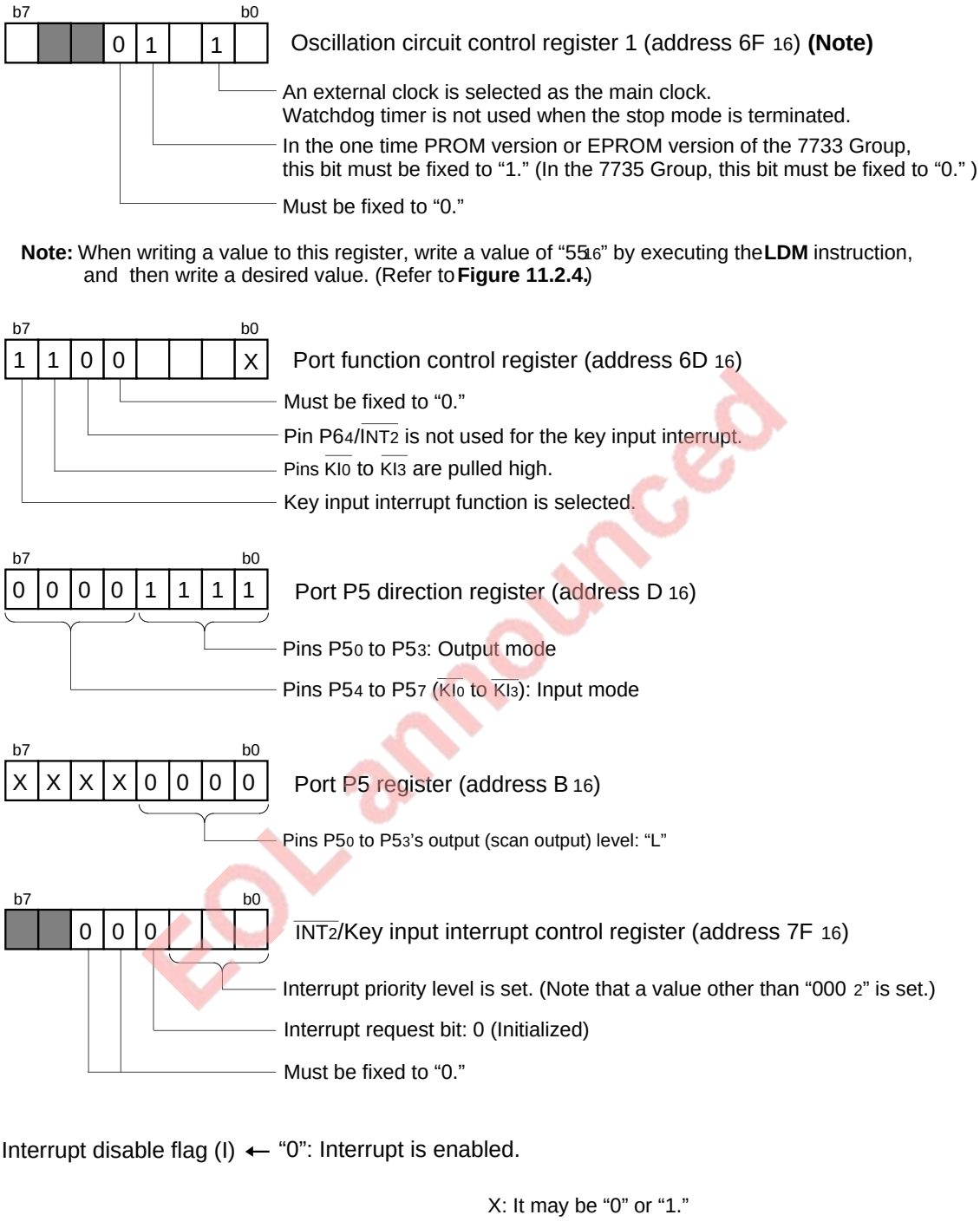

Fig. 17.4.1 Initial settings for related registers

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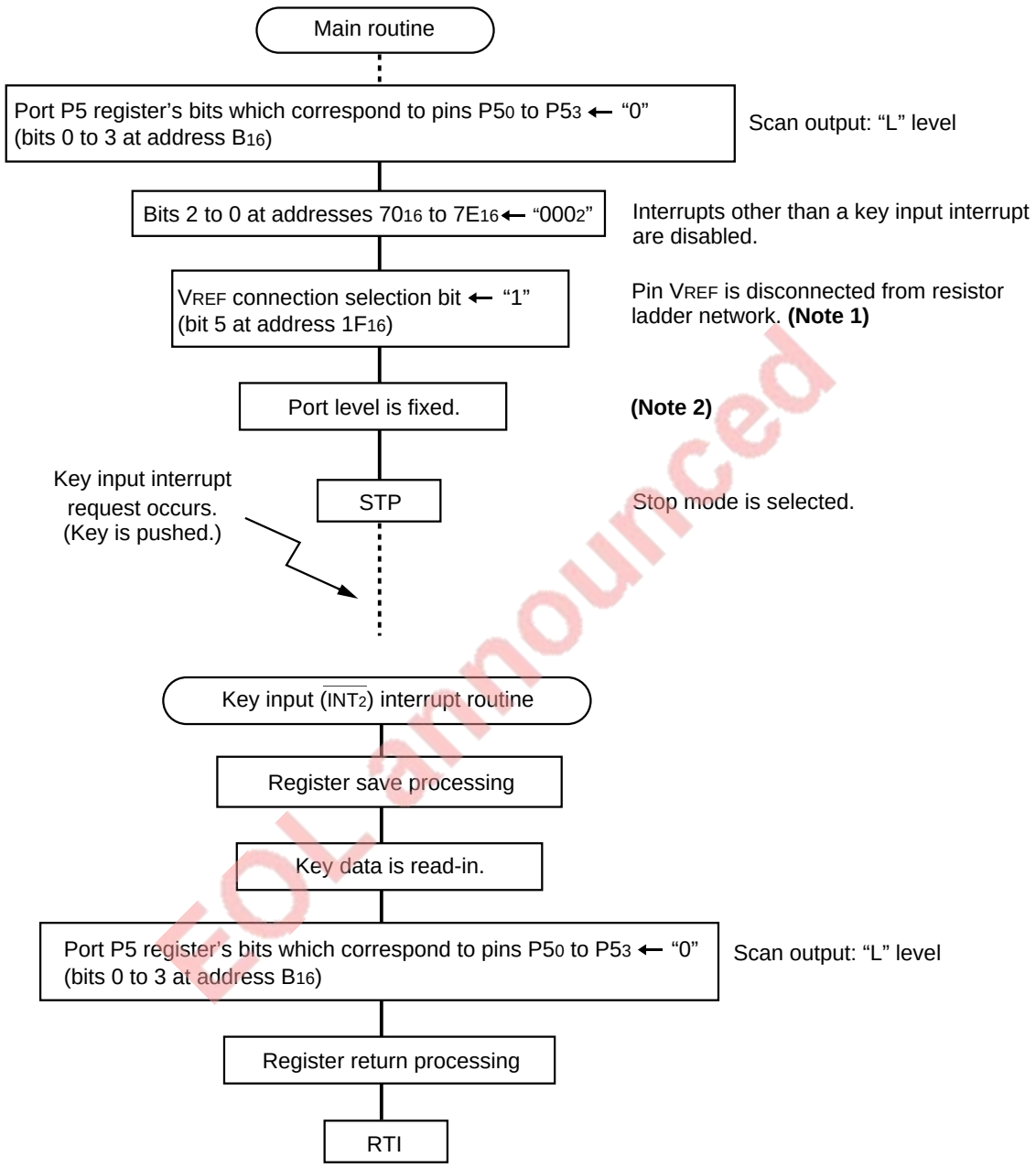
APPLICATIONS

17.4 Power saving

(3) Approximate flowchart



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Notes 1: When pin VREF and resistor ladder network are connected, current flows into the resistor ladder network. When using the A-D converter after the stop mode is terminated, do as follows:

q Reconnect pin VREF and resistor ladder network.

w And then, start A-D conversion after a period of 1 µs or more passed.

2: When a port is connected to an external device and so on, there is a possibility that current consumption increases according to the port's level. In order to avoid this problem, do as follows:

•When output mode is selected: Fix the port's level to a level where no current flows into the external.

•When input mode is selected : Pull the port high or low via a resistor. (Floating state is disabled.)

Fig. 17.4.2 Approximate flowchart

(4) Settings for performing power saving in memory expansion or microprocessor mode

In the memory expansion or microprocessor mode, when saving power consumption, it is necessary to fix the I/O pins' levels of the external bus and bus control signals in the stop mode. For this purpose, set the standby state selection bit to "1."

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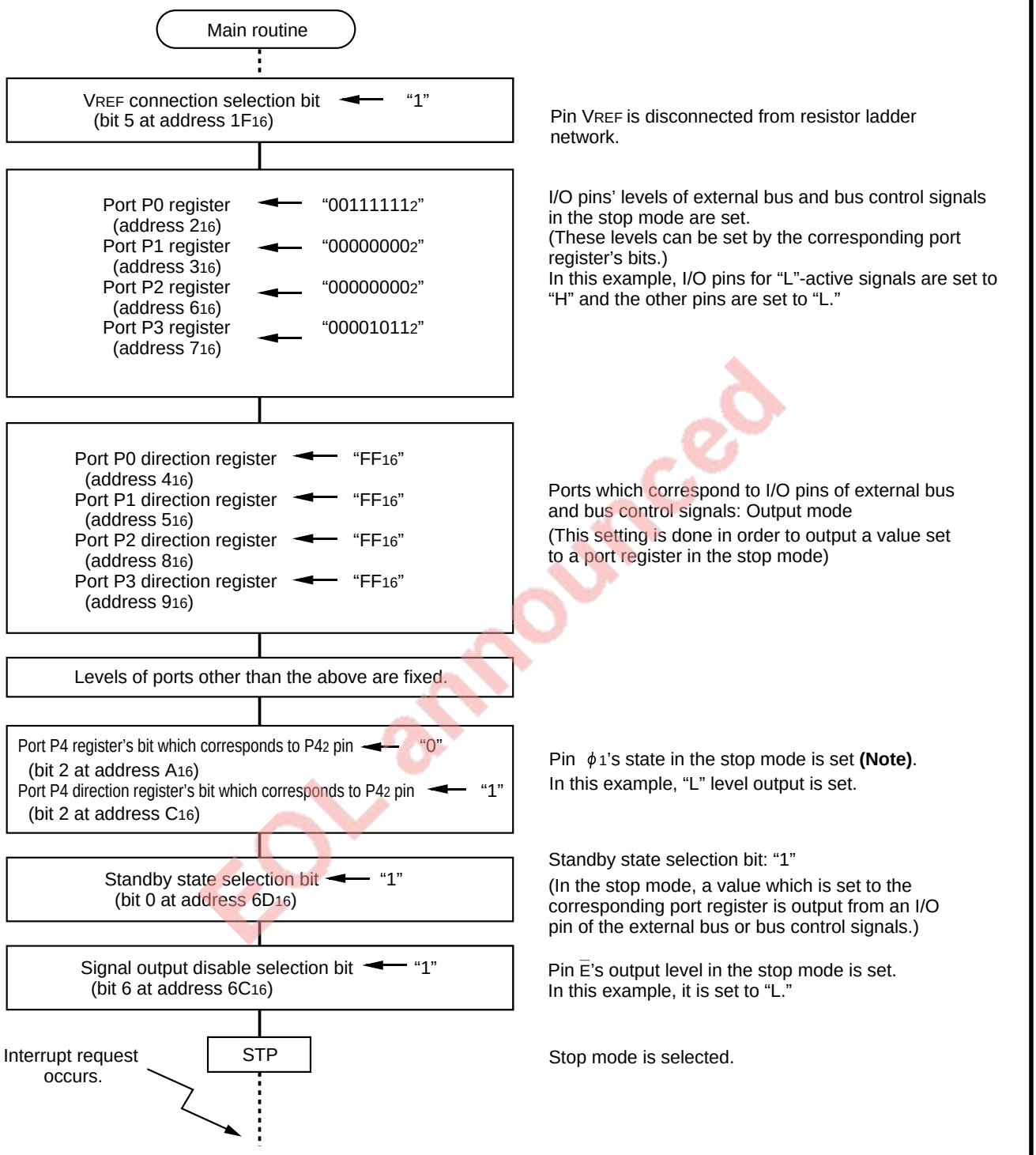

Note: Regardless of this setting, in the following cases, pin ϕ_1 outputs "L" level in the stop mode:

- When the signal output disable selection bit is set to "0" in the microprocessor mode
- When the clock ϕ_1 output selection bit is set to "1" in the memory expansion mode

Fig. 17.4.3 Fixing I/O pins' levels of external bus and bus control signals (Microprocessor mode)

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17.4.2 Power saving example with wait mode used

In this example, power saving is realized by using the wait mode. While power is saved, the clock function is realized by using the clock timer (Timer B2).

(1) Specifications

① The microcomputer operates in the single-chip mode.
② The frequency of the sub clock (f(XCIN)) = 32.768 kHz. An external clock is used as the sub clock.
③ Clock counting is performed by using the clock timer. (An interrupt request occurs every second.)
④ When an $\overline{INT_0}$ interrupt request occurs **(Note)**, the wait mode is terminated.
Note: An interrupt request occurs at every falling edge of the signal input from pin $\overline{INT_0}$.
⑤ In the wait mode, interrupts other than the following interrupts are disabled.
•Timer B2 interrupt
•$\overline{INT_0}$ interrupt
⑥ An external input is used as the main clock.

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APPLICATIONS

17.4 Power saving

(2) Initial settings for related registers

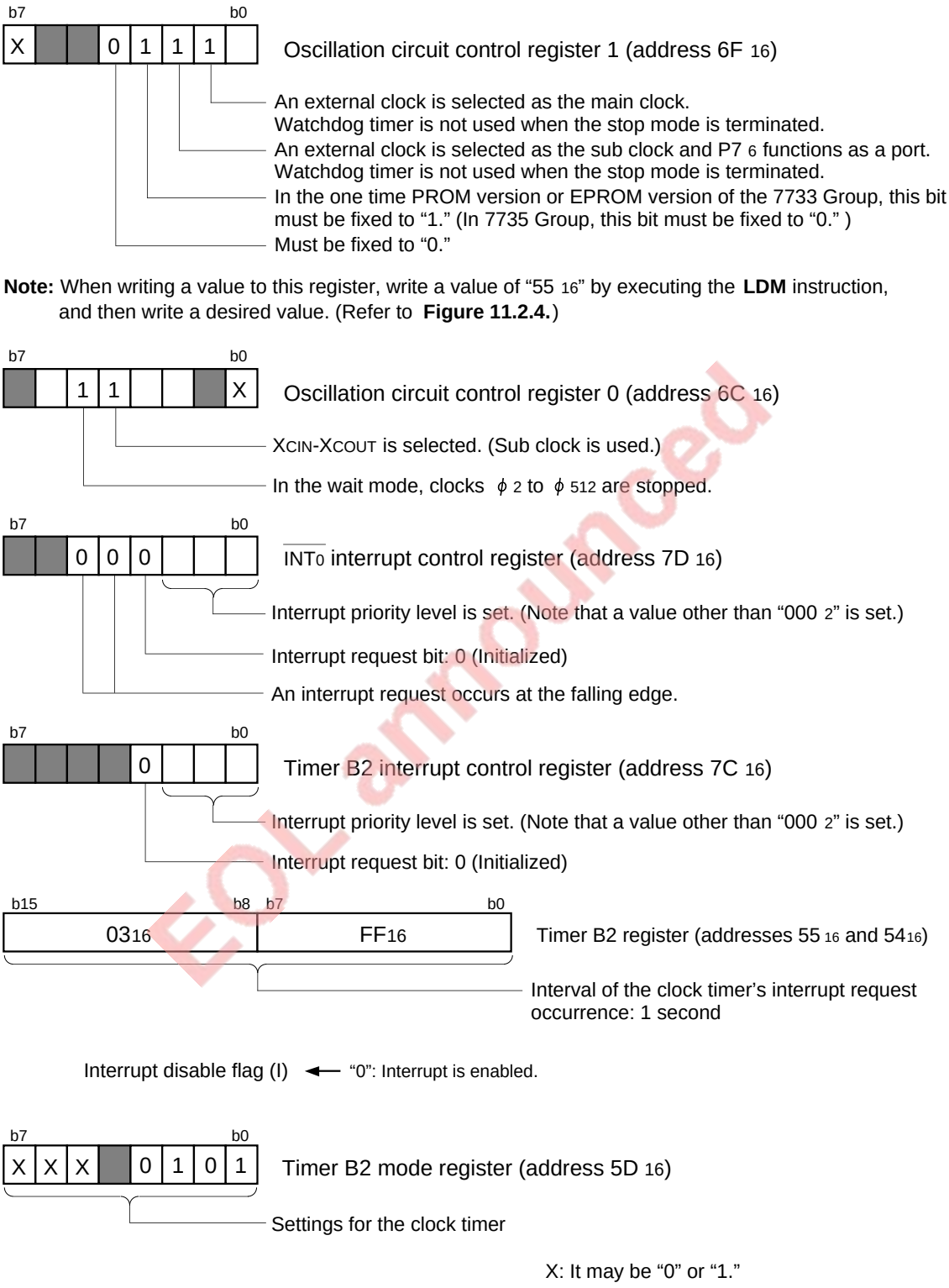

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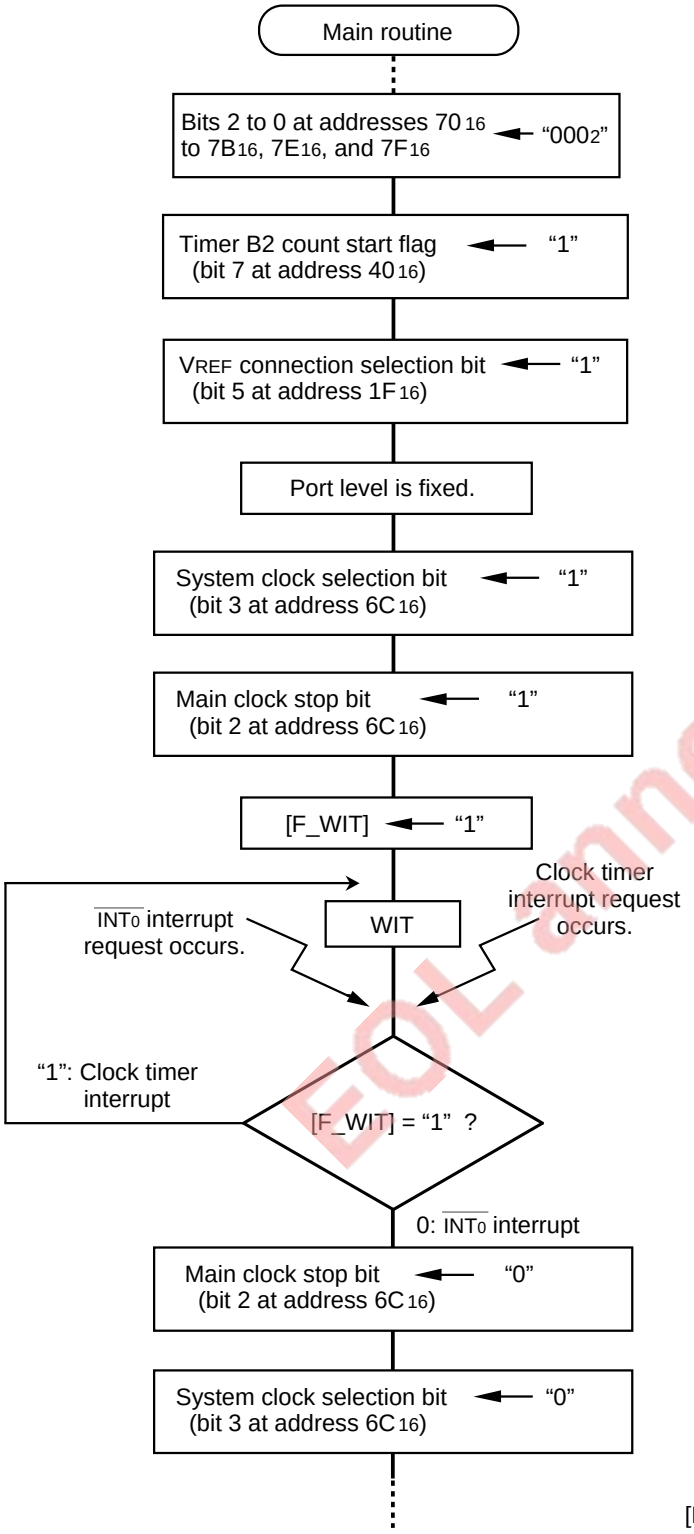
Fig. 17.4.4 Initial settings for related registers

(3) Approximate flowchart



Interrupts other than timer B2 and $\overline{INT_0}$ interrupts are disabled.

Clock timer starts counting .

Pin V_{REF} is disconnected from resistor ladder network. **(Note 1)**

(Note 2)

System clock:
Main clock → Sub clock
<<A>>

Main clock oscillation circuit: Stopped
<<B>>

(By this setting, the wait mode is terminated only when an $\overline{INT_0}$ interrupt request occurs.)

Wait mode is selected.

Main clock oscillation circuit: Oscillating
<<C>>

System clock:
Sub clock → Main clock **(Note 3)**
<<D>>

[F_WIT]: Flag used to determine whether an $\overline{INT_0}$ interrupt request has occurred or not

<<A>> <<B>> <<C>> <<D>>: Refer to **Figure 17.4.8.**

For **Notes 1 to 3**, refer to the next page.

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Fig. 17.4.5 Approximate flowchart (1)

17.4 Power saving

Notes 1: When pin V_{REF} and resistor ladder network are connected, current flows into the resistor ladder network.
When using the A-D converter after the wait mode is terminated, do as follows:
①Reconnect pin V_{REF} and resistor ladder network.
②And then, start A-D conversion after a period of 1µs or more passed.

2: When a port is connected to an external device and so on, there is a possibility that current consumption increases according to the port's level.
In order to avoid this problem, do as follows:
•When output mode is selected: Fix the port's level to a level where no current flows into the external.
•When input mode is selected: Pull the port high or low via a resistor. (Floating state is disabled.)

3: Do not switch the system clock until oscillation of a clock which is input from the external is stabilized.

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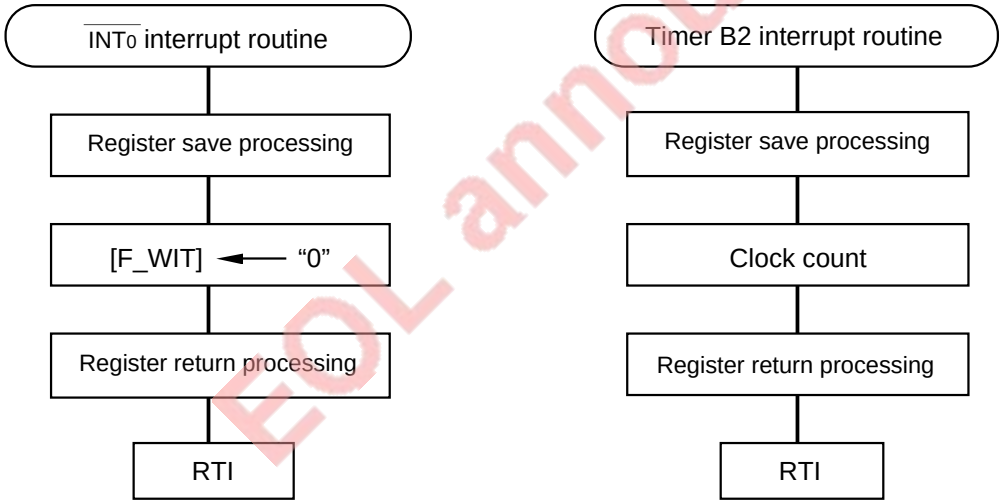

[F_WIT]: Flag used to determine whether an $\overline{INT_0}$ interrupt request has occurred or not

Fig. 17.4.6 Approximate flowchart (2)

Notes 1: When pin V_{REF} and resistor ladder network are connected, current flows into the resistor ladder network.
When using the A-D converter after the wait mode is terminated, do as follows:
q Reconnect pin V_{REF} and resistor ladder network.
w And then, start A-D conversion after a period of 1µs or more passed.

2: When a port is connected to an external device and so on, there is a possibility that current consumption increases according to the port's level.
In order to avoid this problem, do as follows:
•When output mode is selected: Fix the port's level to a level where no current flows into the external.
•When input mode is selected: Pull the port high or low via a resistor. (Floating state is disabled.)

3: Do not switch the system clock until oscillation of a clock which is input from the external is stabilized.

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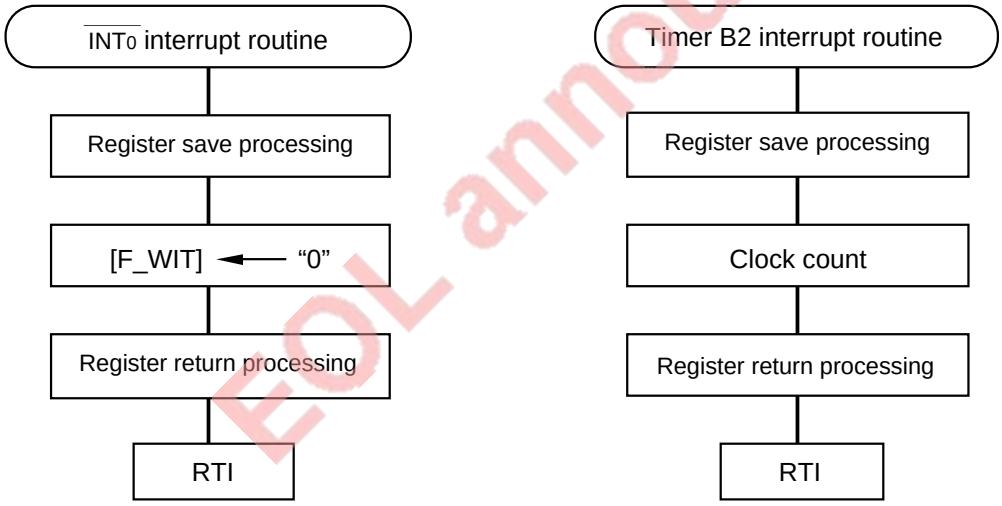
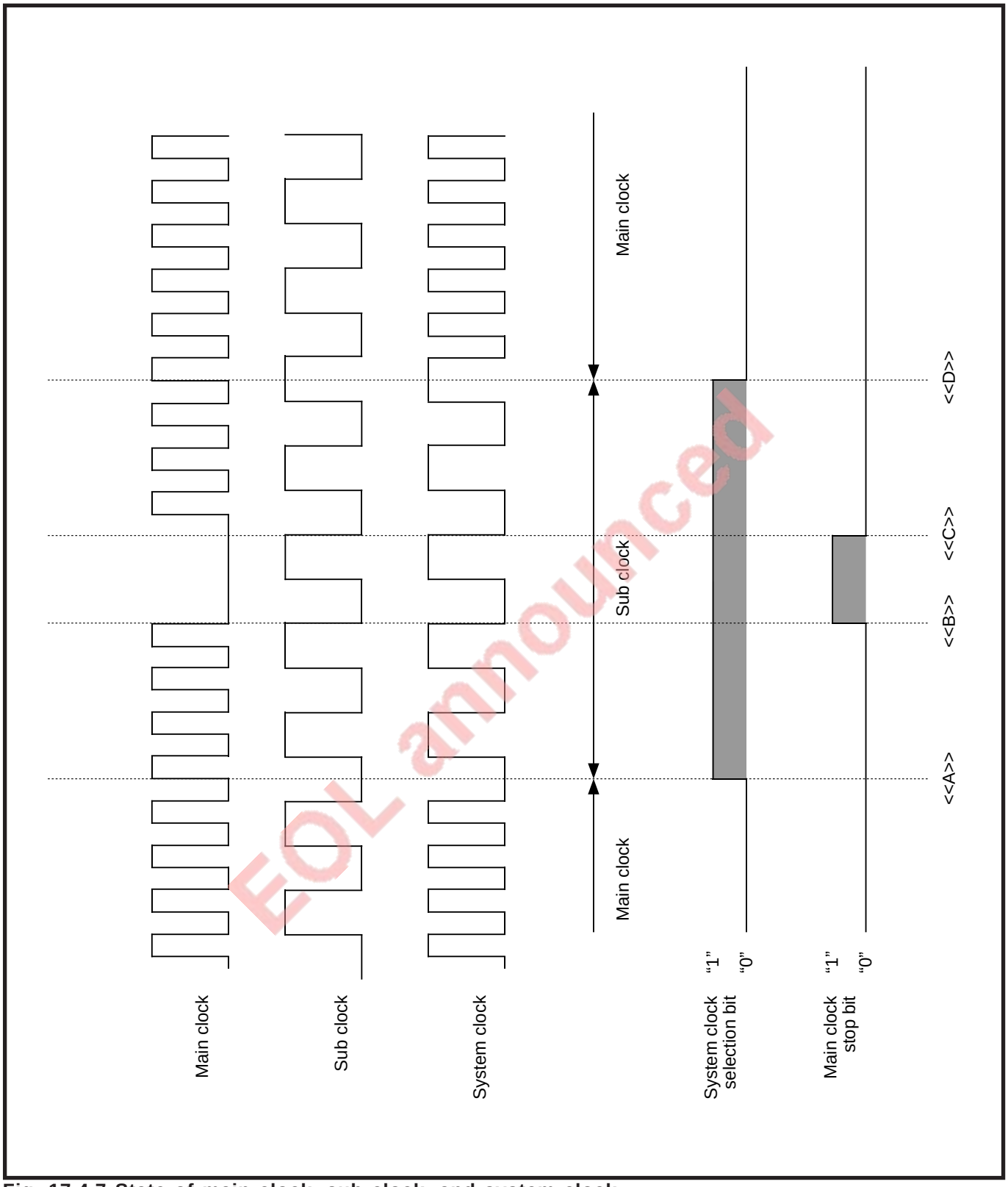


[F_WIT]: Flag used to determine whether an $\overline{INT_0}$ interrupt request has occurred or not

Fig. 17.4.6 Approximate flowchart (2)



EOL announced

Fig. 17.4.7 State of main clock, sub clock, and system clock

17.5 Timer B

An application example of the clock timer (Timer B) is described below.

17.5.1 Application example of clock timer

In this example, the clock timer is controlled by a clock of 32.768 kHz. When the main power source is off, the clock timer can continue counting for the maximum of approximate 45 days by using the backup power source and the internal connect function between timers B1 and B2.

(1) Specifications

① Main power source = 5 V to 2.75 V. Backup power source = 2.75 V to 2.2 V
② Timer B2 uses the sub clock (32.768 kHz) divided by 32 as the count source and counts the time up to 1 minute.
③ Timer B2 counts the power-source-off time up to the maximum of approximate 45 days, checking the timer B2's overflow signal.
④ The clock counter is counted up each time timer B2 interrupt occurs, in other words, every 1 minute.
⑤ When Vcc is less than 2.75 V, in other words, when the main power source is off, the $\overline{INT_0}$ input's level changes from "H" to "L" and the microcomputer enters the wait mode at this falling edge. (Refer to **"a" in Figure 17.5.2.**)
⑥ In the wait mode (Vcc = 2.2 V or more), only timers B2 and B1 do counting. (In this case, note that clock display is disabled and the timer B2 and B1 interrupts are disabled.)
⑦ When Vcc = 2.75 V or more in the wait mode, in other words, when the main power source is on, the $\overline{INT_0}$ input's level changes from "L" to "H" and the wait mode is terminated at the $\overline{INT_0}$ input's rise. (Refer to **"b" in Figure 17.5.2.**) At this time, the following is done according to the timer B1's state.
•When no overflow has occurred in timer B1 (Timer B1 interrupt request bit = "0"), timer B1's value is added to the clock counter's value which was obtained immediately before the wait mode.
•When an overflow has occurred in timer B1, in other words, when a period of approximate 45 days or more has passed, a message for resetting time is displayed.
⑧ When Vcc = 2.2 V or less, the microcomputer enters the reset state owing to the power source detection circuit. (Refer to **"c" in Figure 17.5.2.**) And then, when Vcc = 2.75 V or more, the microcomputer is released from reset state. (Refer to **"d" in Figure 17.5.2.**)

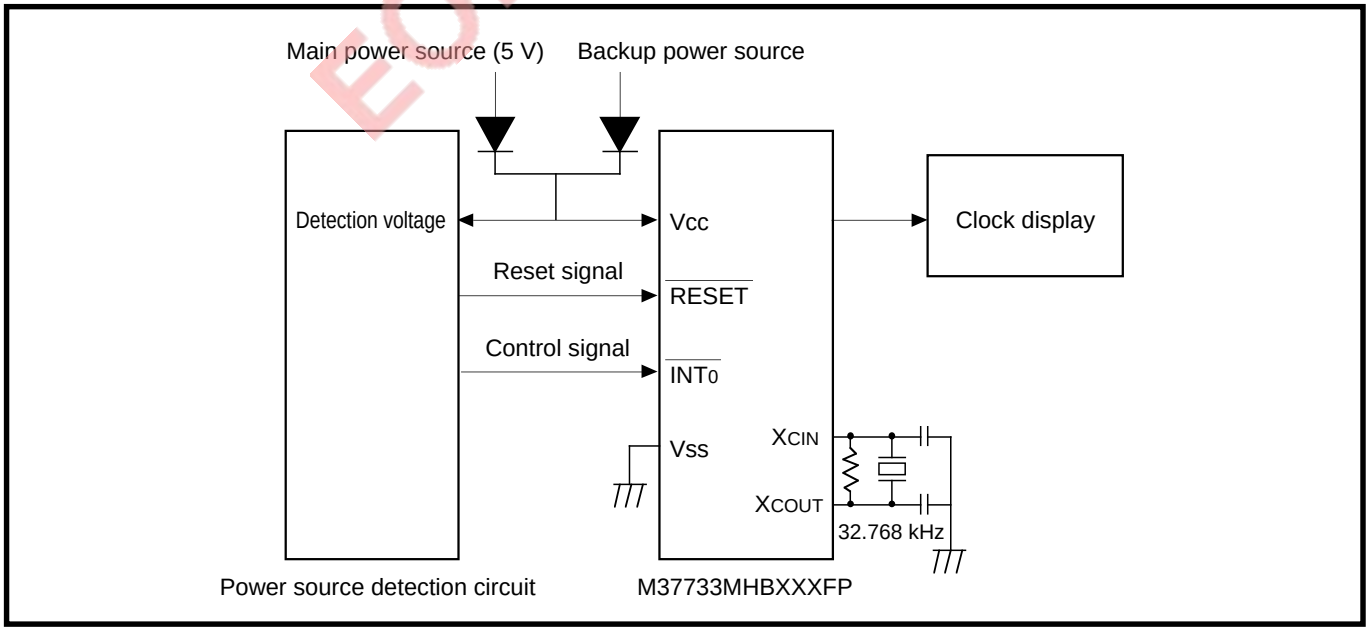


Fig. 17.5.1 Connection example

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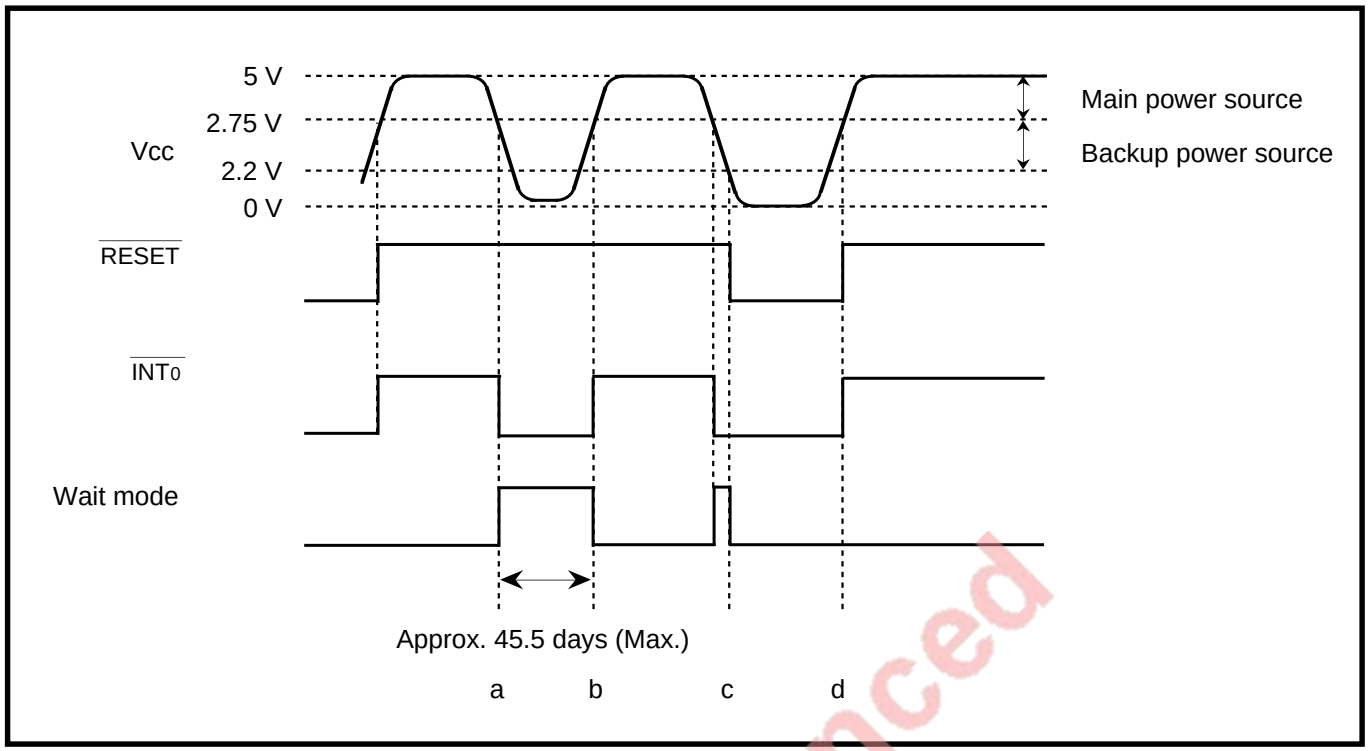

Fig. 17.5.2 Timing chart

(2) Structure of timer B block where timers B1 and B2 are internally connected

Figure 17.5.3 shows the structure of the timer B block.

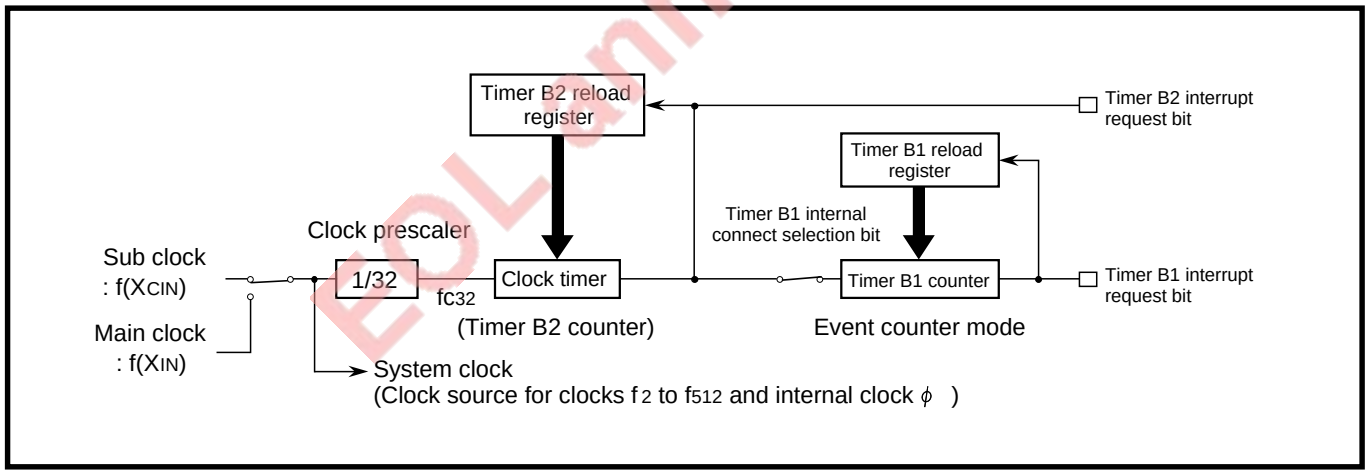

Fig. 17.5.3 Structure of timer B block

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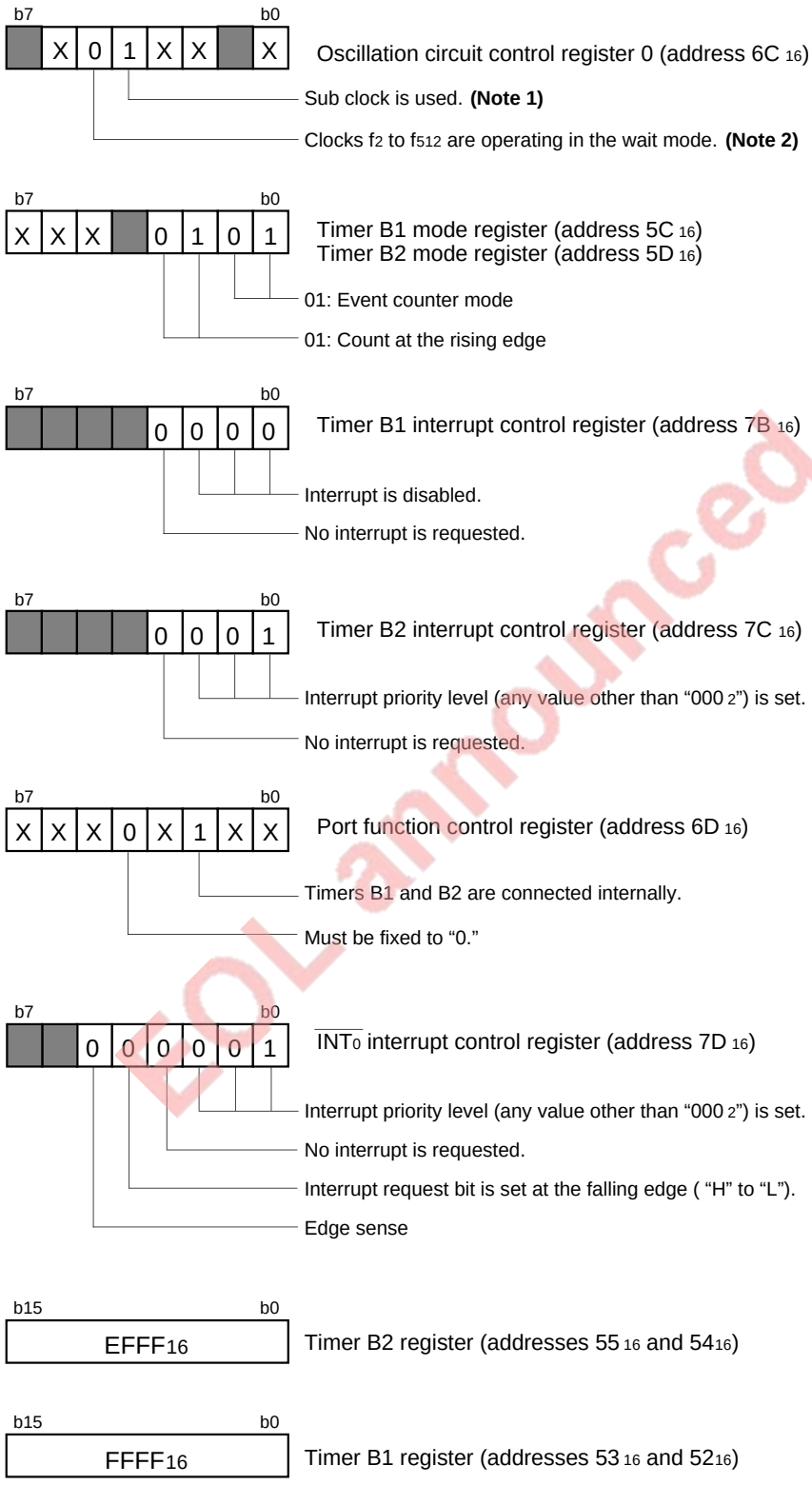
APPLICATIONS

17.5 Timer B

(3) Initial settings for related registers



X: It may be "0" or "1."

Notes 1: Once this bit is set to "1," it cannot be cleared to "0."

2: When setting this bit to "1," set "1" to this bit immediately before the **WIT** instruction is executed. Furthermore, clear this bit to "0" immediately after the wait mode is terminated.

Fig. 17.5.4 Initial settings for related registers

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(4) Approximate flowchart

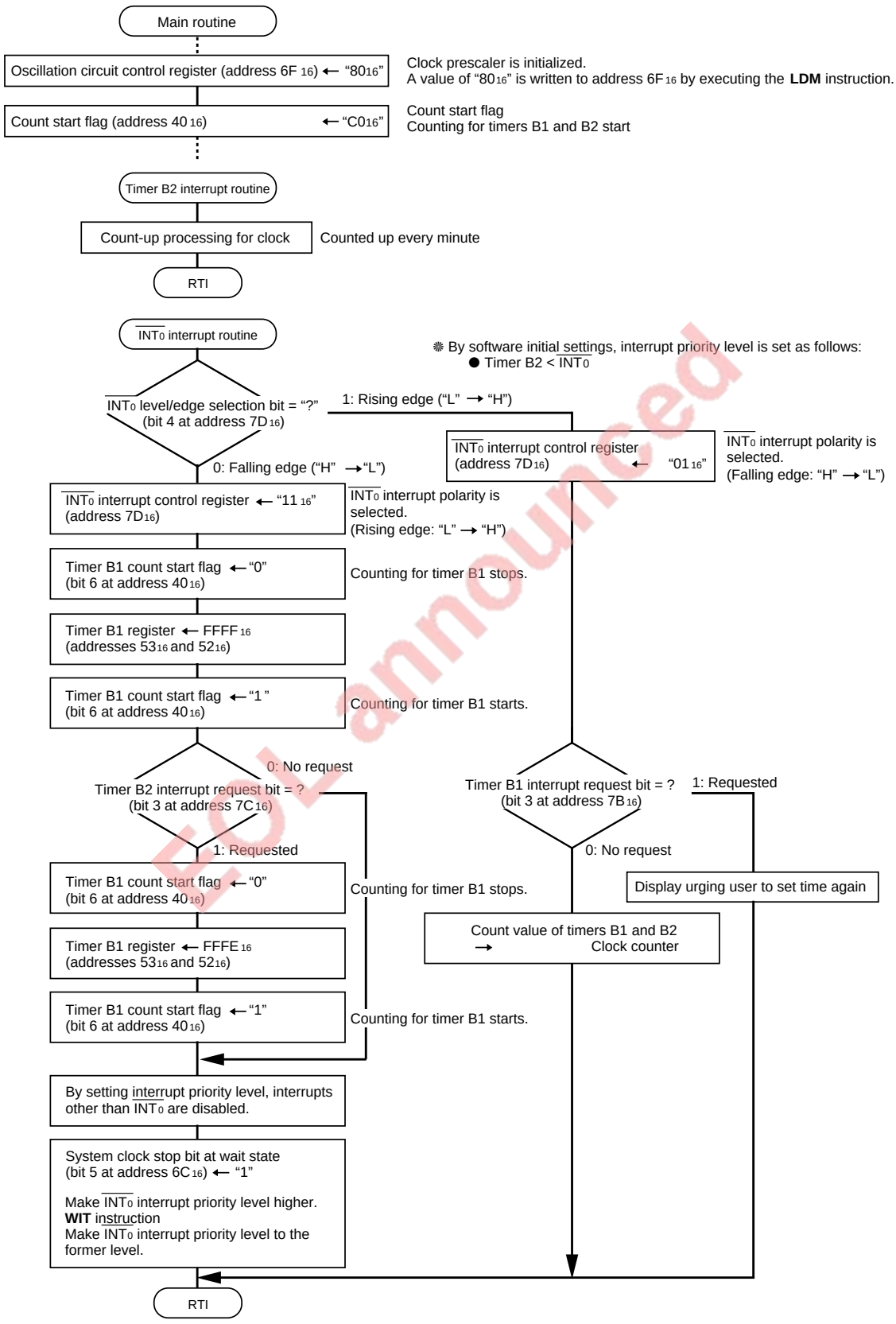

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Fig. 17.5.5 Approximate flowchart

MEMO

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CHAPTER 18
LOW VOLTAGE VERSION

18.1 Performance overview
18.2 Pin configuration
18.3 Functional description
18.4 Electrical characteristics
18.5 Standard characteristics
18.6 Applications

EOL announced

LOW VOLTAGE VERSION

The low voltage version has the following characteristics:
• Low power source voltage (2.7 to 5.5 V)
• Wide operating temperature range (–40 to 85 °C)
The low voltage version is suitable to control equipment which is required to process a large amount of data with a little power dissipation, for example portable equipment which is driven by a battery and OA equipment.

Differences between the M37733MHLXXXHP, which is the low voltage version of the 7733 Group, and the M37733MHBXXXFP are mainly described below.
For the EPROM mode of the built-in PROM version, refer to chapter **"19. BUILT-IN PROM VERSION."**

EOL announced

18.1 Performance overview

Table 18.1.1 shows the performance overview of the M37733MHLXXXHP.

Table 18.1.1 M37733MHLXXXHP performance overview

Items		Performance
Number of basic instructions		103
The minimum instruction execution time		333 ns (When f(XIN) = 12 MHz and main clock is system clock)
Main-clock frequency f(XIN)		12 MHz (Max.) **(Note)**
Sub-clock frequency f(XCIN)		32.768 kHz (Typ.)
Memory size	ROM	124 kbytes
	RAM	3968 bytes
Programmable input/output ports	Ports P0–P2, P4–P8	8 bits × 8
	Port P3	4 bits × 1
Multi-function timers	Timers A0–A4	16 bits × 5
	Timers B0–B2	16 bits × 3
Serial I/O	UART0–UART2	(UART or clock synchronous serial I/O) × 3
A-D converter		(10-bit successive approximation method) × 1(8 channels)
Watchdog timer		12 bits × 1
Interrupts		3 external, 16 internal (By software, one of interrupt priority levels 0 to 7 can be set for each interrupt.)
Clock generating circuits	Main-clock oscillation circuit	Built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
	Sub-clock oscillation circuit	Built-in (externally connected to a quartz-crystal oscillator)
Power source voltage		2.7 V – 5.5 V
Power consumption (in single-chip mode)		9 mW (When f(XIN) = 12 MHz, Vcc = 3 V, and the main clock is the system clock, Typ.)
		22.5 mW (When f(XIN) = 12 MHz, Vcc = 5 V, the main clock is the system clock, Typ.)
		90 μW (When f(XCIN) = 32 kHz, Vcc = 3 V, the sub clock is the system clock, and the main clock is stopped, Typ.)
Port input/output characteristics	Input/Output withstand voltage	5 V
	Output current	5 mA
Memory expansion		Possible (Maximum of 16 Mbytes)
Operating temperature range		–40 °C to +85 °C
Device structure		High-performance CMOS silicon gate process
Package		80-pin plastic molded fine-pitch QFP

Note: When the main clock division selection bit = “1,” the maximum value of f(XIN) = 6 MHz.

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18.2 Pin configuration

Figure 18.2.1 shows the M37733MHLXXXHP pin configuration.

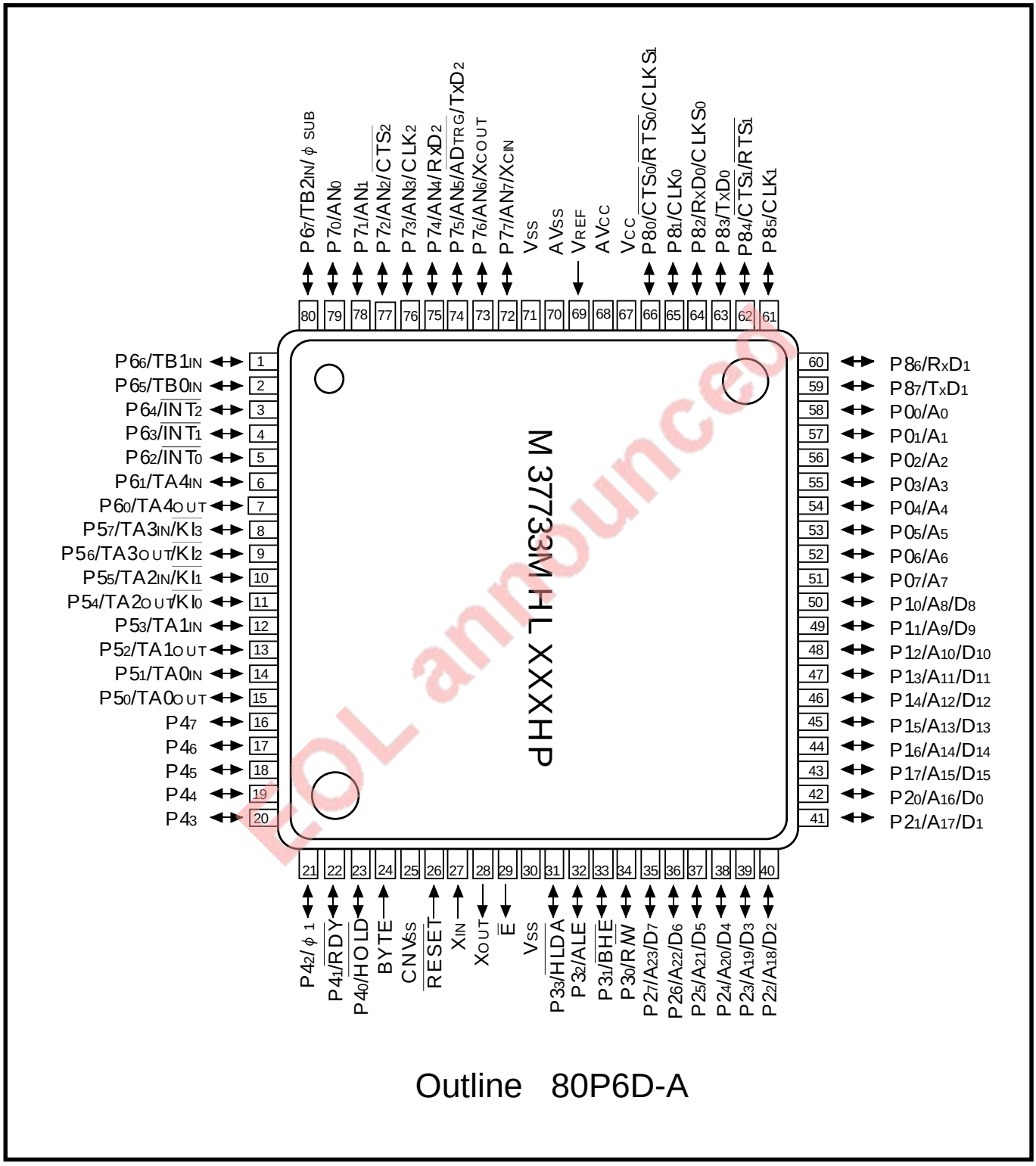

Fig. 18.2.1 M37733MHLXXXHP pin configuration (Top view)

18.3 Functional description

The M37733MHLXXXHP has the same functions as the M37733MHBXXXFP except for the power-on reset conditions. Power-on reset conditions are described below.

For the other functions, refer to chapters **"2. CENTRAL PROCESSING UNIT"** to **"14. CLOCK GENERATING CIRCUIT."**

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LOW VOLTAGE VERSION

18.3 Functional description

18.3.1 Power-on reset conditions

Figure 18.3.1 shows the power-on reset conditions and Figure 18.3.2 shows an example of power-on reset circuit. For details of reset, refer to chapter **"13. RESET."**

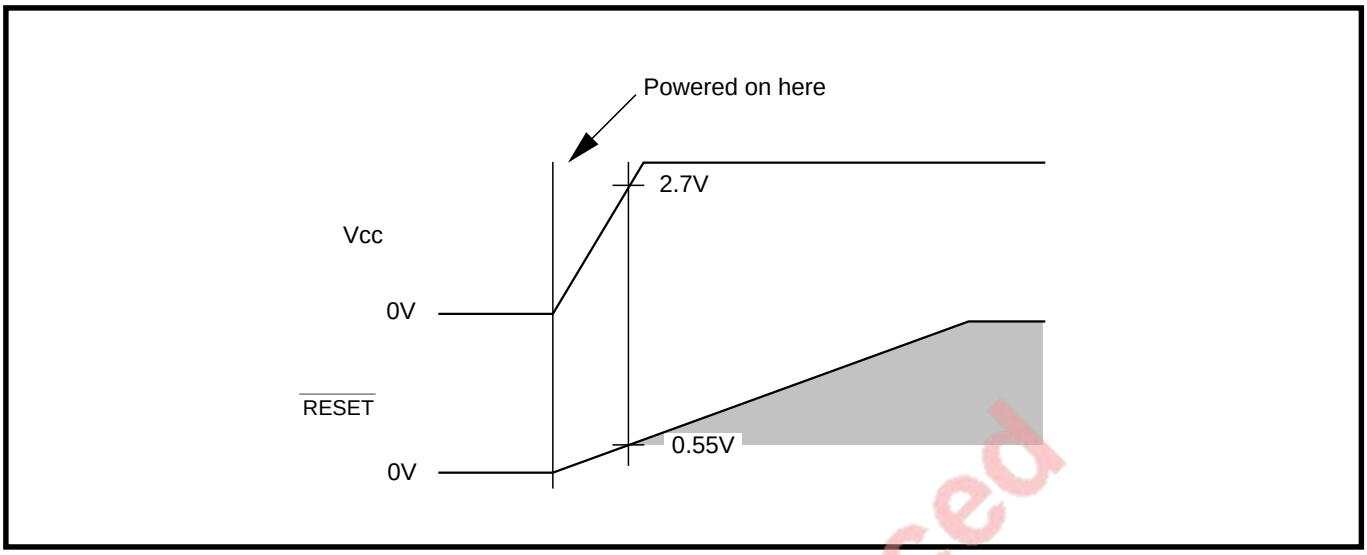

Fig. 18.3.1 Power-on reset conditions

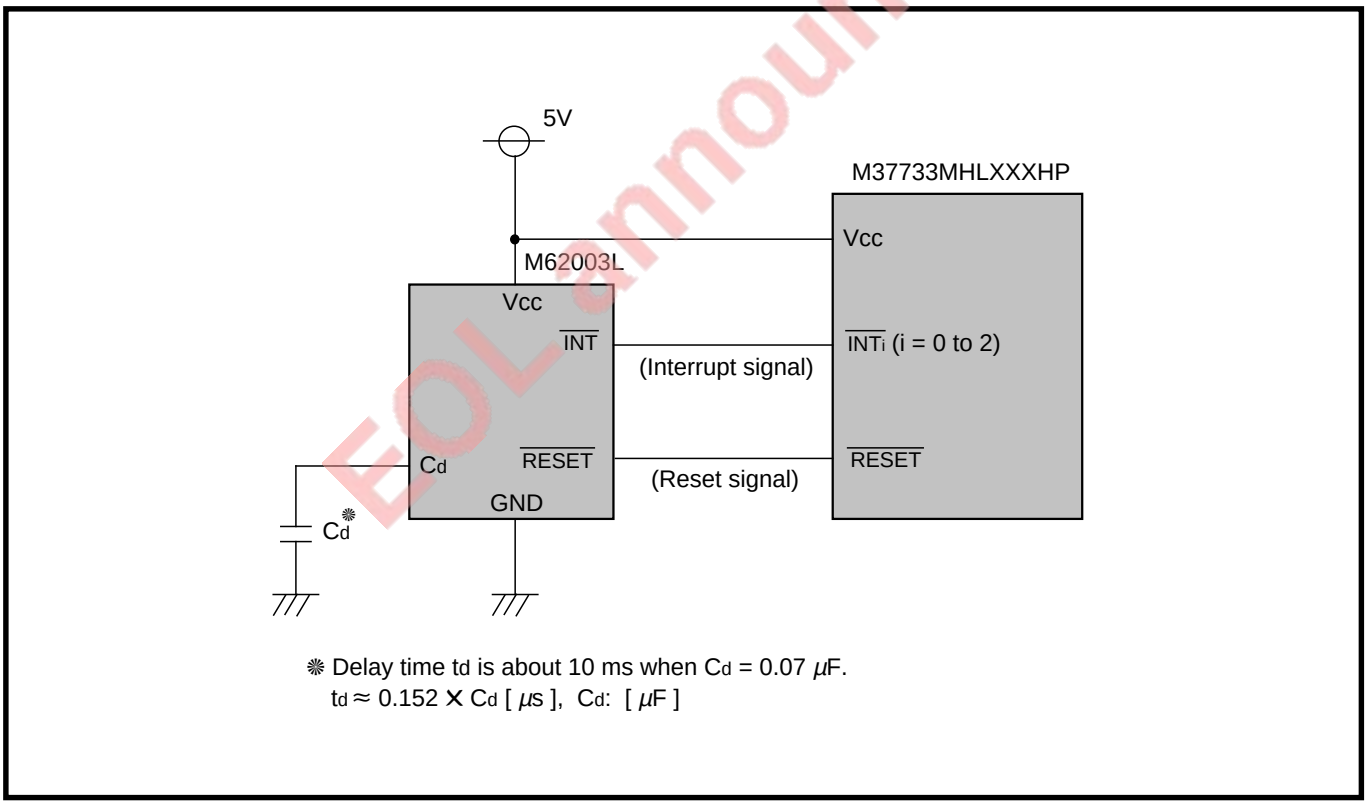

Fig. 18.3.2 Example of power-on reset circuit

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18.4 Electrical characteristics

The M37733MHLXXXHP's electrical characteristics are described below. For the latest data, inquire of addresses described last (**"CONTACT ADDRESSES FOR FURTHER INFORMATION")** .

18.4.1 Absolute maximum ratings

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to 7	V
AVcc	Analog power source voltage		–0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to 12	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, V_{REF}, X_{IN}		–0.3 to Vcc+0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}, $\overline{E}$		–0.3 to Vcc+0.3	V
P_d	Power dissipation	Ta = 25 °C	200	mW
T_{opr}	Operating temperature		–40 to 85	°C
T_{stg}	Storage temperature		–65 to 150	°C

EOL announced

LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.2 Recommended operating conditions

Recommended operating conditions (Vcc = 2.7 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Power source voltage	$f(X_{IN})$:Operating	2.7		5.5	V
		$f(X_{IN})$:Stopped, $f(X_{CIN})$ = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} **(Note 3)**	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} **(Note 3)**	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0		0.16 Vcc	V
$I_{OH\ (peak)}$	High-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–10	mA
$I_{OH\ (avg)}$	High-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–5	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			10	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P4_4$–$P4_7$, $P5_0$–$P5_3$			16	mA
$I_{OL\ (avg)}$	Low-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			5	mA
$I_{OL\ (avg)}$	Low-level average output current	$P4_4$–$P4_7$, $P5_0$–$P5_3$			12	mA
$f(X_{IN})$	Main-clock oscillation frequency **(Note 4)**				12	MHz
$f(X_{CIN})$	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1: Average output current is the average value of an interval of 100 ms.

2: The sum of I_{OL}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL}(peak) for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I_{OH}(peak) for ports P4, P5, P6, and P7 must be 80 mA or less.

3: Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1."

4: The maximum value of $f(X_{IN})$ = 6 MHz when the main clock division selection bit = "1."

EOL announced

18.4.3 Electrical characteristics

Electrical characteristics (Vcc = 5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	Vcc = 5 V, I_{OH} = –10 mA		3			V
			Vcc = 3 V, I_{OH} = –1 mA		2.5			
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	Vcc = 5 V, I_{OH} = –400 μA		4.7			V
V_{OH}	High-level output voltage	$P3_0$–$P3_2$	Vcc = 5 V, I_{OH} = –10 mA		3.1			V
			Vcc = 5 V, I_{OH} = –400 μA		4.8			
			Vcc = 3 V, I_{OH} = –1 mA		2.6			
V_{OH}	High-level output voltage	$\overline{E}$	Vcc = 5 V, I_{OH} = –10 mA		3.4			V
			Vcc = 5 V, I_{OH} = –400 μA		4.8			
			Vcc = 3 V, I_{OH} = –1 mA		2.6			
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_5$, $P8_0$–$P8_7$	Vcc = 5 V, I_{OL} = 10 mA				2	V
			Vcc = 3 V, I_{OL} = 1 mA				0.5	
V_{OL}	Low-level output voltage	$P4_4$–$P4_7$, $P5_0$–$P5_3$	Vcc = 5 V, I_{OL} = 16 mA				1.8	V
			Vcc = 3 V, I_{OL} = 10 mA				1.5	
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	Vcc = 5 V, I_{OL} = 2 mA				0.45	V
V_{OL}	Low-level output voltage	$P3_0$–$P3_2$	Vcc = 5 V, I_{OL} = 10 mA				1.9	V
			Vcc = 5 V, I_{OL} = 2 mA				0.43	
			Vcc = 3 V, I_{OL} = 1 mA				0.4	
V_{OL}	Low-level output voltage	$\overline{E}$	Vcc = 5 V, I_{OL} = 10 mA				1.6	V
			Vcc = 5 V, I_{OL} = 2 mA				0.4	
			Vcc = 3 V, I_{OL} = 1 mA				0.4	
V_{T+}–V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$–$TA4_{IN}$, $TB0_{IN}$–$TB2_{IN}$, $\overline{INT0}$–$\overline{INT2}$, AD_{TRG}, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS2}$, $CLK0$, $CLK1$, $CLK2$, $\overline{KI0}$–$\overline{KI3}$	Vcc = 5 V		0.4		1	V
			Vcc = 3 V		0.1		0.7	
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$		Vcc = 5 V		0.2		0.5	V
			Vcc = 3 V		0.1		0.4	
V_{T+}–V_{T-}	Hysteresis X_{IN}		Vcc = 5 V		0.1		0.4	V
			Vcc = 3 V		0.06		0.26	
V_{T+}–V_{T-}	Hysteresis X_{CIN} (When external clock is input)		Vcc = 5 V		0.1		0.4	V
			Vcc = 3 V		0.06		0.26	
I_{IH}	High-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	Vcc = 5 V, V_I = 5 V				5	μA
			Vcc = 3 V, V_I = 3 V				4	
I_{IL}	Low-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, $P6_5$– $P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	Vcc = 5 V, V_I = 0 V				–5	μA
			Vcc = 3 V, V_I = 0 V				–4	
I_{IL}	Low-level input current	$P5_4$–$P5_7$, $P6_2$–$P6_4$	V_I = 0 V, without a pull-up transistor	Vcc = 5 V			–5	μA
				Vcc = 3 V			–4	
			V_I = 0 V, with a pull-up transistor	Vcc = 5 V	–0.25	–0.5	–1.0	mA
				Vcc = 3 V	–0.08	–0.18	–0.35	
V_{RAM}	RAM hold voltage		When clock is stopped		2			V

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LOW VOLTAGE VERSION

18.4 Electrical characteristics

ELECTRICAL CHARACTERISTICS (Vcc= 5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	In single-chip mode, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, f(X_{IN}) = 12 MHz (Square waveform), (f(f_2) = 6 MHz), f(X_{CIN}) = 32.768 kHz, in operating **(Note 1)**		4.5	9	mA
			Vcc = 3 V, f(X_{IN}) = 12 MHz (Square waveform), (f(f_2) = 6 MHz), f(X_{CIN}) = 32.768 kHz, in operating **(Note 1)**		3	6	mA
			Vcc = 3 V, f(X_{IN}) = 12 MHz (Square waveform), (f(f_2) = 0.75 MHz), f(X_{CIN}) : Stopped, in operating **(Note 1)**		0.4	0.8	mA
			Vcc = 3V, f(X_{IN}) = 12 MHz (Square waveform), f(X_{CIN}) = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		6	12	μA
			Vcc = 3 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, in operating **(Note 3)**		30	60	μA
			Vcc = 3 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		3	6	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

Pre-announced

Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1."

3: This is applied when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

18.4.4 A-D converter characteristics

A-D CONVERTER CHARACTERISTICS (Vcc = AVcc = 5 V, Vss = AVss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note)** , unless otherwise noted)

Symbol	Parameter	Measuring conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF} = Vcc			10	Bits
—	Absolute accuracy	V_{REF} = Vcc			± 3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = Vcc	10		25	kΩ
t_{CONV}	Conversion time		19.6			μs
V_{REF}	Reference voltage		2.7		Vcc	V
V_{IA}	Analog input voltage		0		V_{REF}	V

Note: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

18.4.5 Internal peripheral devices

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	250		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	125		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time **(Note 3)**	$\frac{8 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	666		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width **(Note 3)**	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	333		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width **(Note 3)**	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	333		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	666		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width		166		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width		166		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	166		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	3333		ns
$t_{w(UPH)}$	TAi_{OUT} input high-level pulse width	1666		ns
$t_{w(UPL)}$	TAi_{OUT} input low-level pulse width	1666		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	666		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	666		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

3: The TAi_{IN} input cycle time must be 4 cycles of a count source or more.
The TAi_{IN} input high-level pulse width and low-level pulse width must be 2 cycles of a count source or more, respectively.

EOL announced

LOW VOLTAGE VERSION

18.4 Electrical characteristics

Timer A input (Two-phase pulse input in event counter mode)

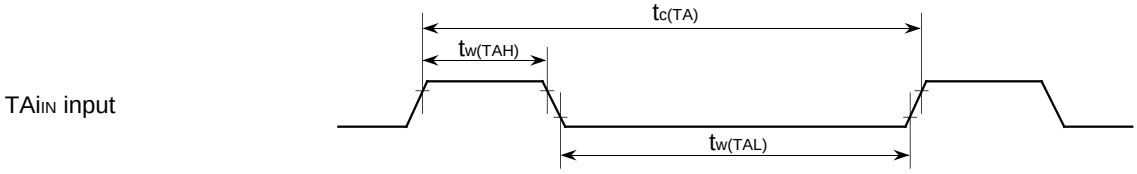
Symbol	Parameter	Measuring conditions	Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAj_{IN} input cycle time		2		μs
$t_{su(TAj_{IN}\text{-}TAj_{OUT})}$	TAj_{IN} input setup time		500		ns
$t_{su(TAj_{OUT}\text{-}TAj_{IN})}$	TAj_{OUT} input setup time		500		ns

Note: This is applied when the main clock division selection bit = “0” and $f(f_2)$ = 6 MHz.

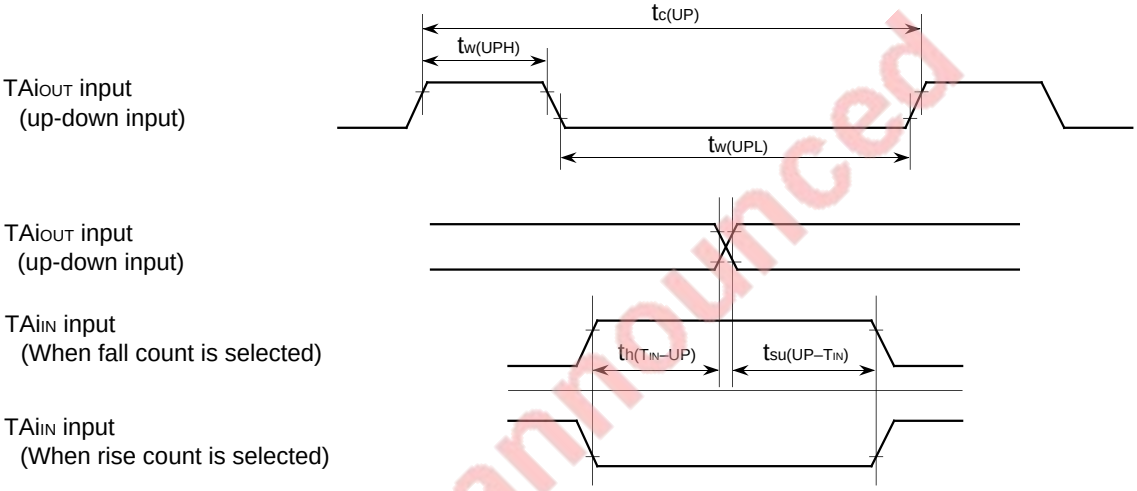
EOL announced

Internal peripheral devices

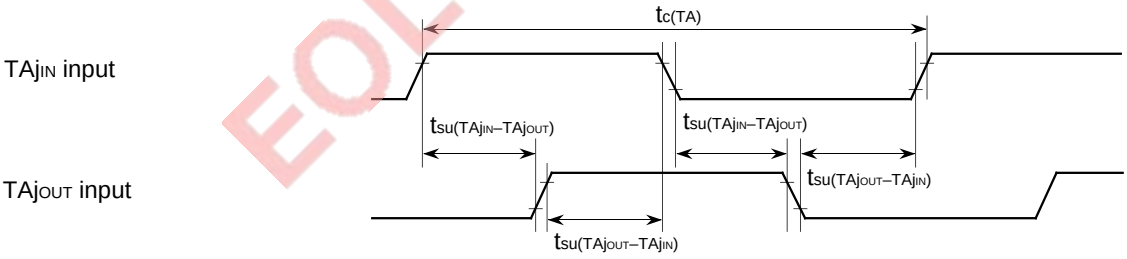
●Count input in event counter mode
●Gating input in timer mode
●External trigger input in one-shot pulse mode
●External trigger input in pulse width modulation mode



●Up-down input and count input in event counter mode



●Two-phase pulse input in event counter mode



Measuring conditions

•V_{CC} = 2.7 to 5.5 V

•Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}

EOL announced

LOW VOLTAGE VERSION

18.4 Electrical characteristics

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (One edge count)	250		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (One edge count)	125		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (One edge count)	125		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (Both edges count)	500		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Both edges count)	250		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \times f(f_2)}$ **(Note 2)**	333		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Data formula (Min.)	Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \times f(f_2)}$	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \times f(f_2)}$	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \times f(f_2)}$	333		ns

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (Minimum allowable trigger)	1333		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK_i input cycle time	333		ns
$t_{w(CKH)}$	CLK_i input high-level pulse width	166		ns
$t_{w(CKL)}$	CLK_i input low-level pulse width	166		ns
$t_{d(C-Q)}$	TxD_i output delay time		100	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	65		ns
$t_{h(C-D)}$	RxD_i input hold time	75		ns

Notes 1: The TBi_{IN} input cycle time must be 4 cycles of a count source or more.
The TBi_{IN} input high-level pulse width and low-level pulse width must be 2 cycles of a count source or more, respectively.

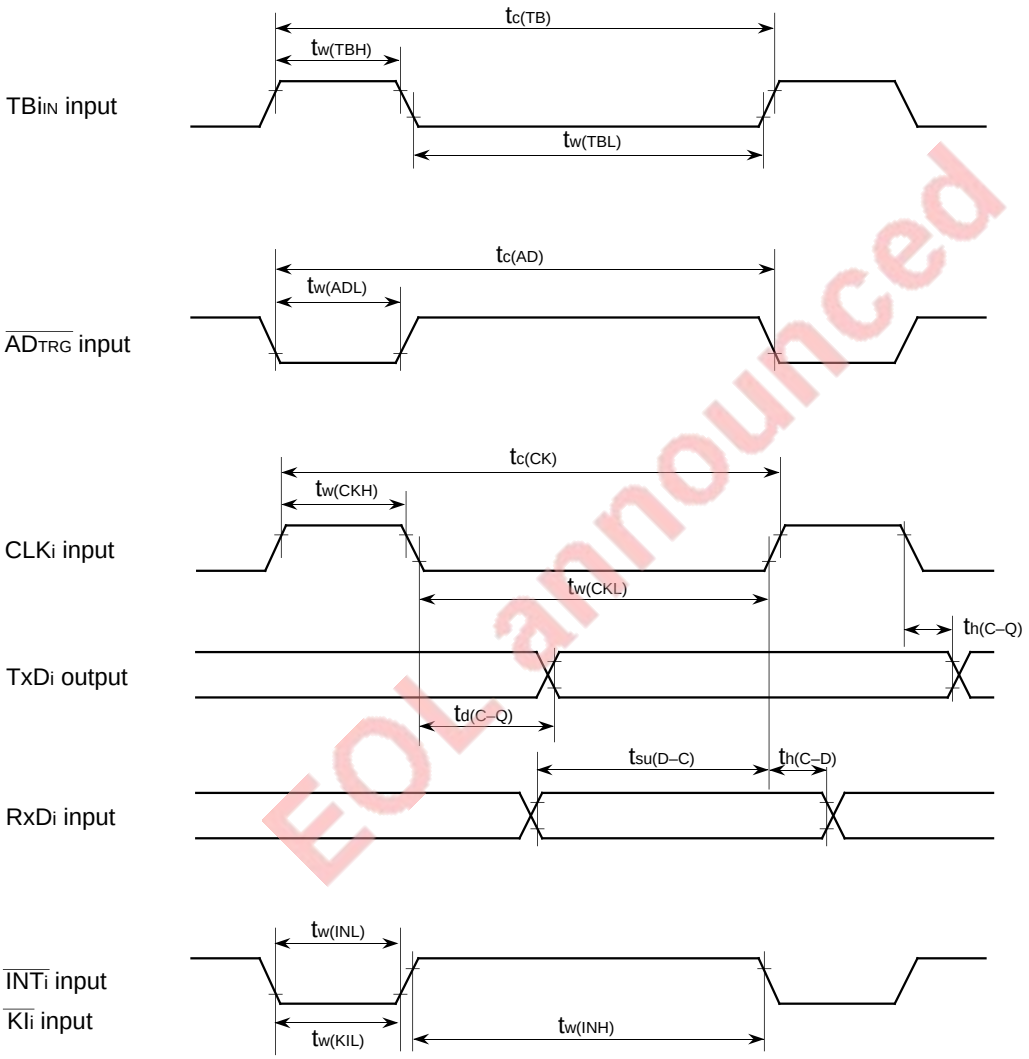
2: $f(f_2)$ represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

EOL announced

External interrupt $\overline{INT_i}$ input, Key input interrupt $\overline{KI_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI_i}$ input low-level pulse width	250		ns

Internal peripheral devices



EOL announced

Measuring conditions

- V_{CC} = 2.7 to 5.5 V
- Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.6 Ready and Hold

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(RDY-\phi_1)}$	$\overline{RDY}$ input setup time	80		ns
$t_{su(HOLD-\phi_1)}$	$\overline{HOLD}$ input setup time	80		ns
$t_{h(\phi_1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi_1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Note: This is applied to the case where the main clock division selection bit = “0” and f(f_2) = 6 MHz.

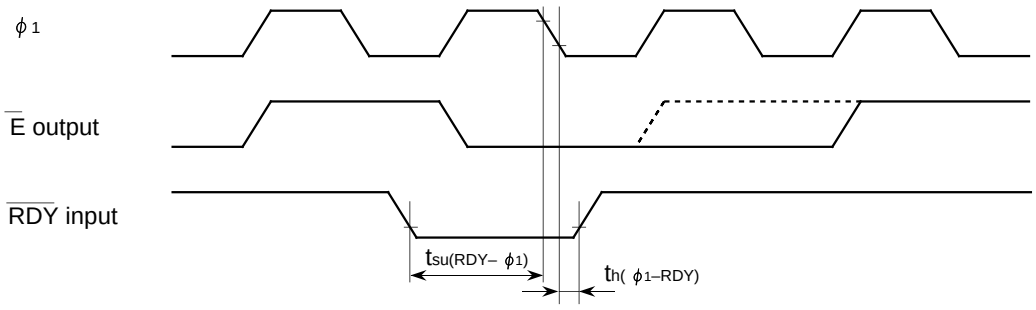
Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time	Fig. 18.4.1		120	ns

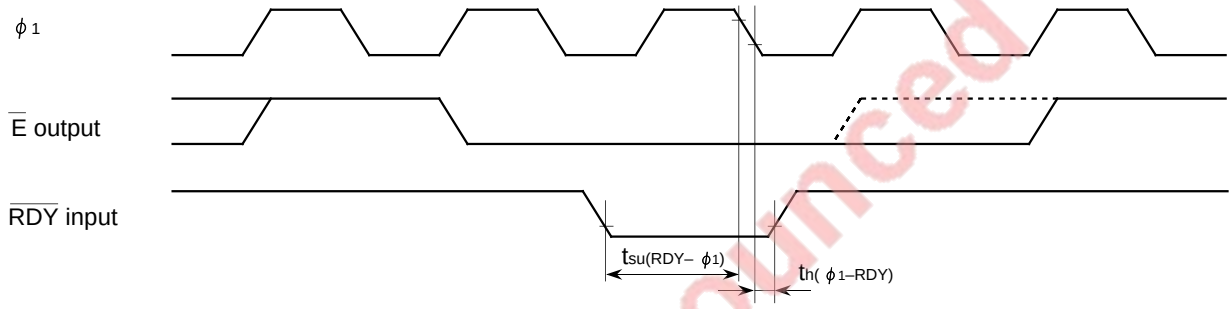
EOL announced

● Ready

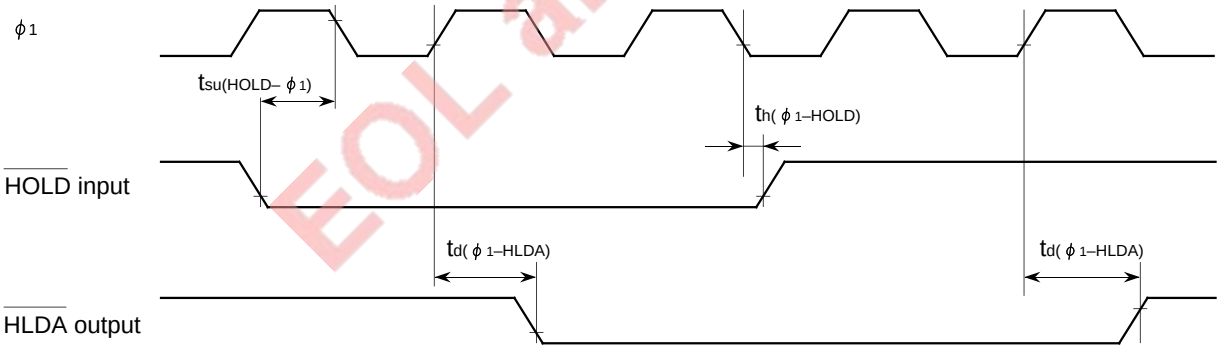
With no wait



With wait



● Hold



EOL announced

Measuring conditions

•V_{CC} = 2.7 to 5.5 V

•Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}

•Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.7 Single-chip mode

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(P0D–E)}$	Port P0 input setup time	200		ns
$t_{su(P1D–E)}$	Port P1 input setup time	200		ns
$t_{su(P2D–E)}$	Port P2 input setup time	200		ns
$t_{su(P3D–E)}$	Port P3 input setup time	200		ns
$t_{su(P4D–E)}$	Port P4 input setup time	200		ns
$t_{su(P5D–E)}$	Port P5 input setup time	200		ns
$t_{su(P6D–E)}$	Port P6 input setup time	200		ns
$t_{su(P7D–E)}$	Port P7 input setup time	200		ns
$t_{su(P8D–E)}$	Port P8 input setup time	200		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = “0” and f(f_2) = 6 MHz.

2: When the main clock division selection bit = “1,” the minimum value of t_c = 166 ns.

3: When the main clock division selection bit = “1,” values of $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 2)**, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
$t_{d(E–P0Q)}$	Port P0 data output delay time	Fig. 18.4.1		300	ns
$t_{d(E–P1Q)}$	Port P1 data output delay time			300	ns
$t_{d(E–P2Q)}$	Port P2 data output delay time			300	ns
$t_{d(E–P3Q)}$	Port P3 data output delay time			300	ns
$t_{d(E–P4Q)}$	Port P4 data output delay time			300	ns
$t_{d(E–P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(E–P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(E–P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(E–P8Q)}$	Port P8 data output delay time			300	ns

Note: This is applied when the main clock division selection bit = “0” and f(f_2) = 6 MHz.

EOL announced

Single-chip mode

EOL announced

Measuring conditions

- V_{CC} = 2.7 to 5.5 V
- Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.8 Memory expansion mode and Microprocessor mode : with no wait

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(D–E)}$	Data input setup time	80		ns
$t_{h(E–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: When the main clock division selection bit = "1," the minimum value of t_c = 166 ns.
3: When the main clock division selection bit = "1," values of $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

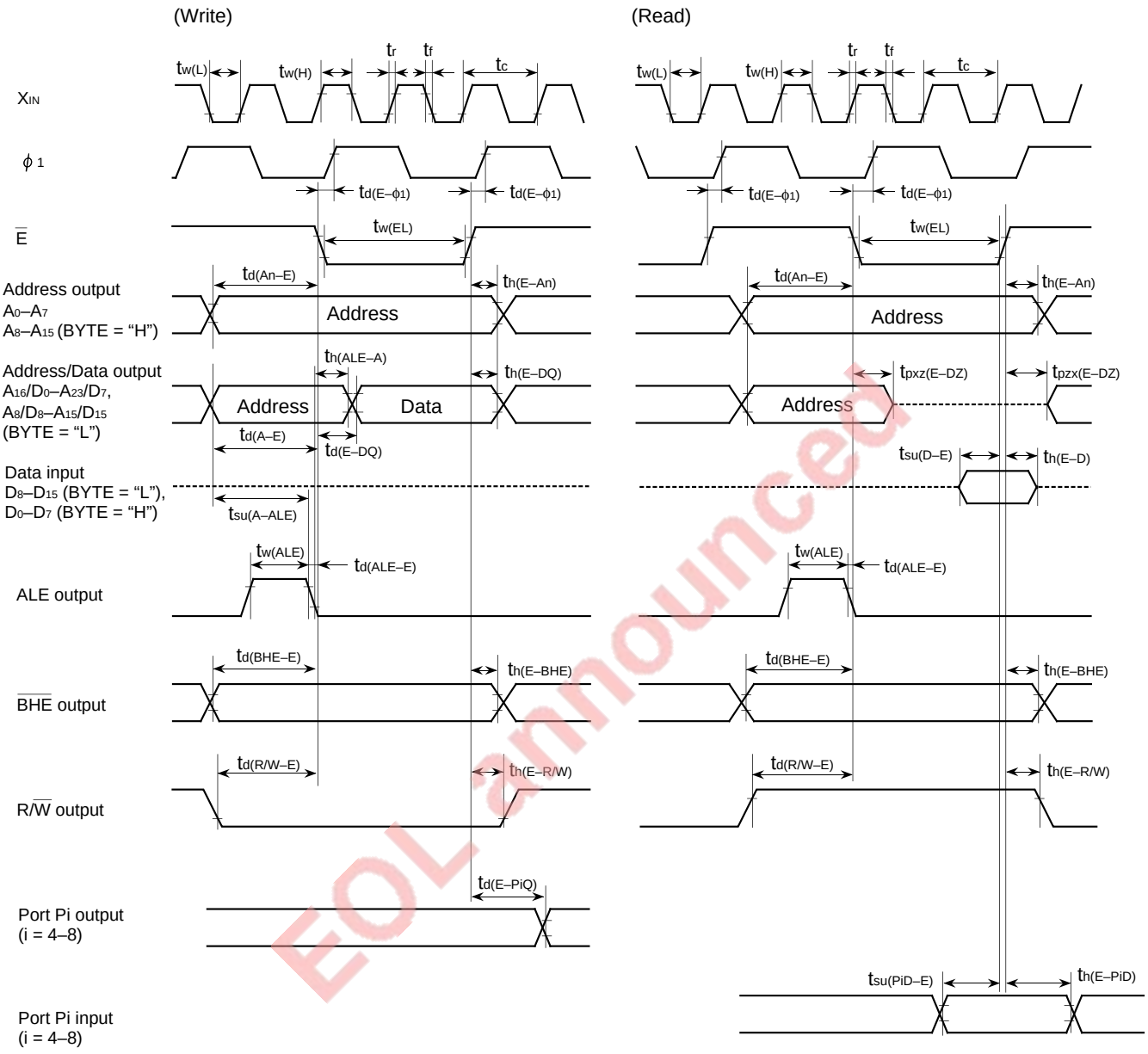
Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Typ.	
$t_{d(An–E)}$	Address output delay time	Fig. 18.4.1	$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{d(A–E)}$	Address output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{h(E–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 73$	10		ns
$t_{h(ALE–A)}$	Address hold time			9		ns
$t_{d(ALE–E)}$	ALE output delay time			4		ns
$t_{d(E–DQ)}$	Data output delay time				90	ns
$t_{h(E–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{w(EL)}$	$\overline{E}$ pulse width		$\frac{2 \times 10^9}{2 \times f(f_2)} - 35$	131		ns
$t_{pxz(E–DZ)}$	Floating start delay time				10	ns
$t_{pzx(E–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 30$	53		ns
$t_{d(BHE–E)}$	$\overline{BHE}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{d(R/W–E)}$	R/$\overline{W}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{h(E–BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 50$	33		ns
$t_{h(E–R/W)}$	R/$\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 50$	33		ns
$t_{d(E–\phi 1)}$	$\phi 1$ output delay time			0	30	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

EOL announced

Memory expansion mode and Microprocessor mode :

With no wait (Wait bit = “1”)



EOL announced

Measuring conditions

- V_{CC} = 2.7 to 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.9 Memory expansion mode and Microprocessor mode : with wait 1

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(D-E)}$	Data input setup time	80		ns
$t_{h(E-D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: When the main clock division selection bit = "1," the minimum value of t_c = 166 ns.
3: When the main clock division selection bit = "1," values of $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

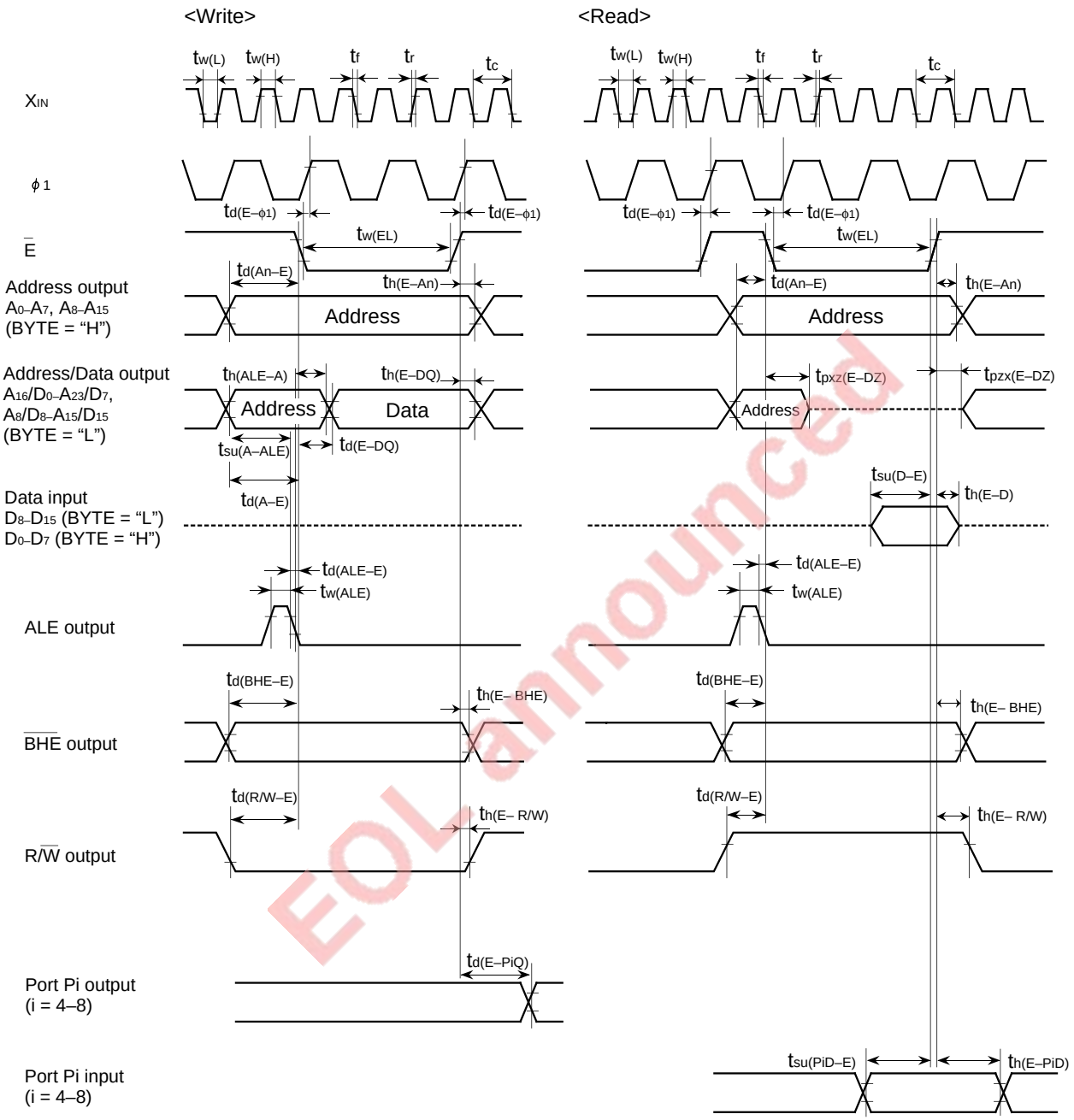
Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Typ.	
$t_{d(An-E)}$	Address output delay time	Fig. 18.4.1	$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{d(A-E)}$	Address output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{h(E-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{su(A-ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 73$	10		ns
$t_{h(ALE-A)}$	Address hold time			9		ns
$t_{d(ALE-E)}$	ALE output delay time			4		ns
$t_{d(E-DQ)}$	Data output delay time				90	ns
$t_{h(E-DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{w(EL)}$	$\overline{E}$ pulse width		$\frac{4 \times 10^9}{2 \times f(f_2)} - 35$	298		ns
$t_{pxz(E-DZ)}$	Floating start delay time				10	ns
$t_{pzx(E-DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 30$	53		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$	20		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 50$	33		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 50$	33		ns
$t_{d(E-\phi 1)}$	$\phi 1$ output delay time			0	30	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

EOL announced

Memory expansion mode and Microprocessor mode :

When external memory area is accessed with wait 1 (Wait bit = “0” and Wait selection bit = “1”)



EOL announced

Measuring conditions

- V_{CC} = 2.7 to 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.10 Memory expansion mode and microprocessor mode : with wait 0

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(D–E)}$	Data input setup time	80		ns
$t_{h(E–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: When the main clock division selection bit = "1," the minimum value of t_c = 166 ns.
3: When the main clock division selection bit = "1," values of $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Typ.	
$t_{d(An–E)}$	Address output delay time	Fig. 18.4.1	$\frac{3 \times 10^9}{2 \times f(f_2)} - 68$	182		ns
$t_{d(A–E)}$	Address output delay time		$\frac{3 \times 10^9}{2 \times f(f_2)} - 88$	162		ns
$t_{h(E–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{2 \times 10^9}{2 \times f(f_2)} - 43$	123		ns
$t_{su(A–ALE)}$	Address output set up time		$\frac{2 \times 10^9}{2 \times f(f_2)} - 73$	93		ns
$t_{h(ALE–A)}$	Address hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{d(ALE–E)}$	ALE output delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{d(E–DQ)}$	Data output delay time				90	ns
$t_{h(E–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 43$	40		ns
$t_{w(EL)}$	$\overline{E}$ pulse width		$\frac{4 \times 10^9}{2 \times f(f_2)} - 35$	298		ns
$t_{pxz(E–DZ)}$	Floating start delay time				10	ns
$t_{pzx(E–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 30$	53		ns
$t_{d(BHE–E)}$	$\overline{BHE}$ output delay time		$\frac{3 \times 10^9}{2 \times f(f_2)} - 68$	182		ns
$t_{d(R/W–E)}$	R/$\overline{W}$ output delay time		$\frac{3 \times 10^9}{2 \times f(f_2)} - 68$	182		ns
$t_{h(E–BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 50$	33		ns
$t_{h(E–R/W)}$	R/$\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \times f(f_2)} - 50$	33		ns
$t_{d(E–\phi 1)}$	$\phi 1$ output delay time			0	30	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

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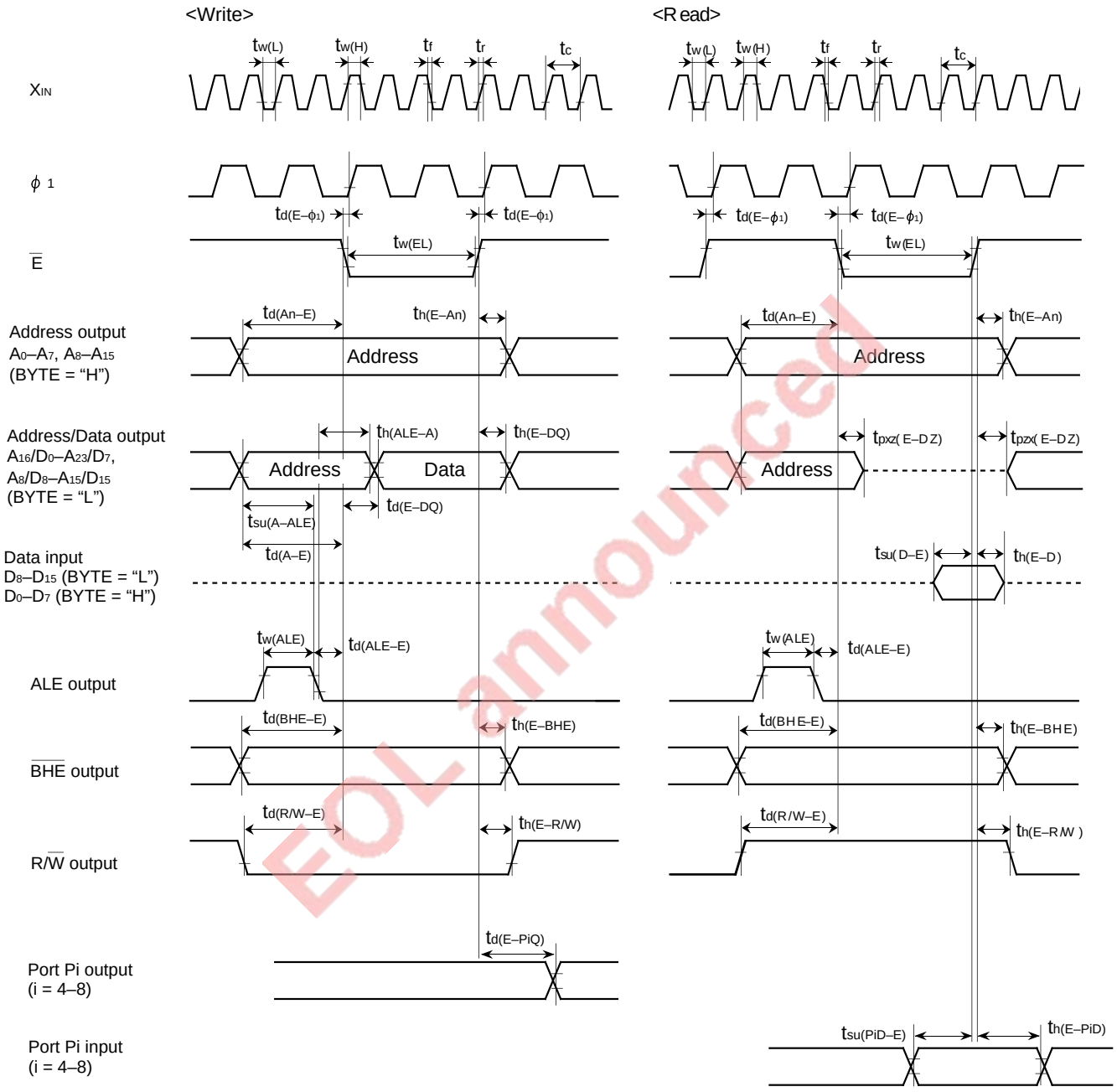
Memory expansion mode and Microprocessor mode :

When external memory area is accessed with wait 0 (Wait bit = “0” and Wait selection bit = “0”)



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Measuring conditions

- V_{CC} = 2.7 to 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.11 Measuring circuit for ports P0 to P8 and pins $\phi 1$ and $\overline{E}$

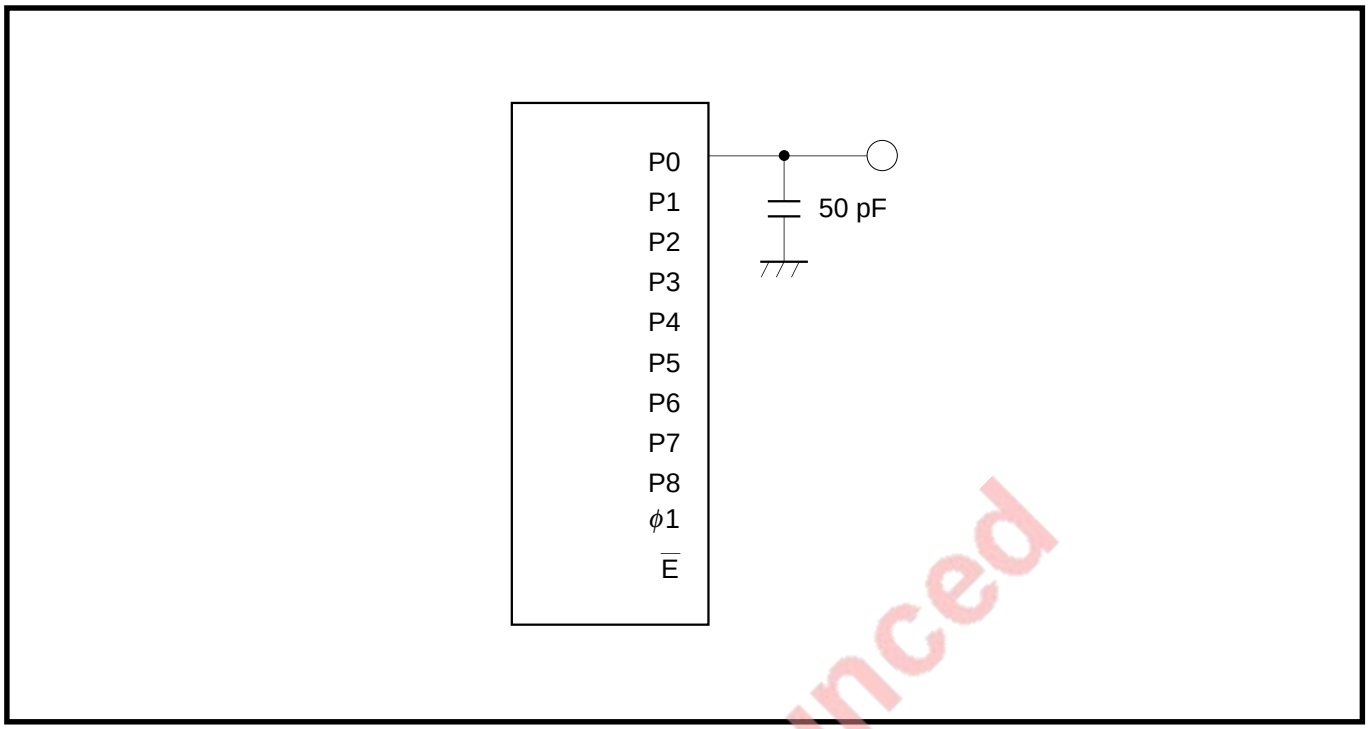


Fig. 18.4.1 Measuring circuit for ports P0 to P8 and pins $\phi 1$ and $\overline{E}$

EOL announced

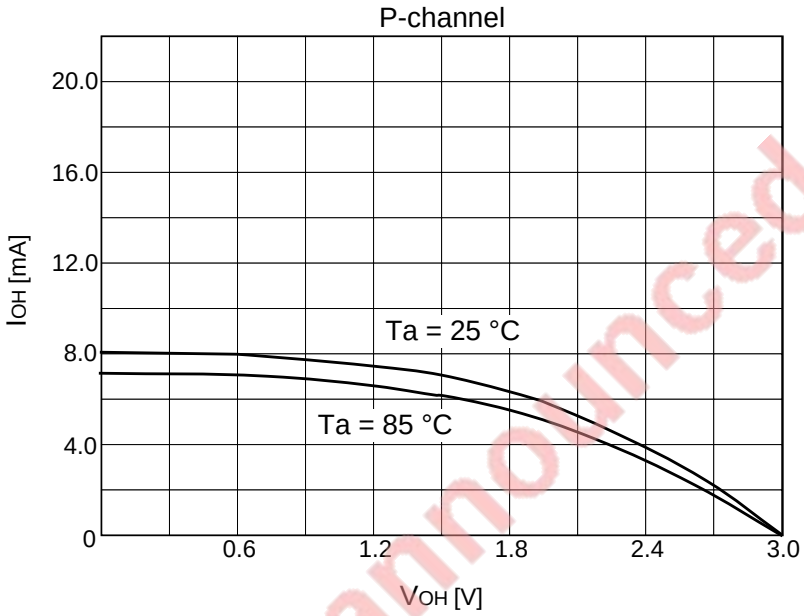
18.5 Standard characteristics

Standard characteristics described below are just examples of the M37733MHLXXXHP's characteristics and are not guaranteed. For rated values, refer to section **"18.4 Electrical characteristics."**

18.5.1 Programmable I/O port (CMOS output) standard characteristics: Ports P0 to P3, $P4_0$–$P4_3$, $P5_4$–$P5_7$, P6, P7, and P8

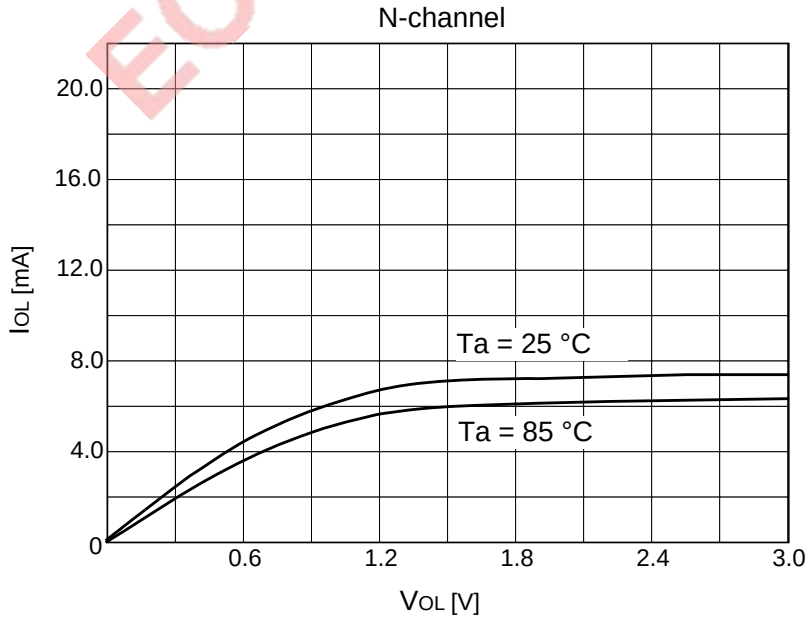
(1) P-channel I_{OH}–V_{OH} characteristics

Power source voltage V_{CC} = 3 V



(2) N-channel I_{OL}–V_{OL} characteristics

Power source voltage V_{CC} = 3 V



EOL announced

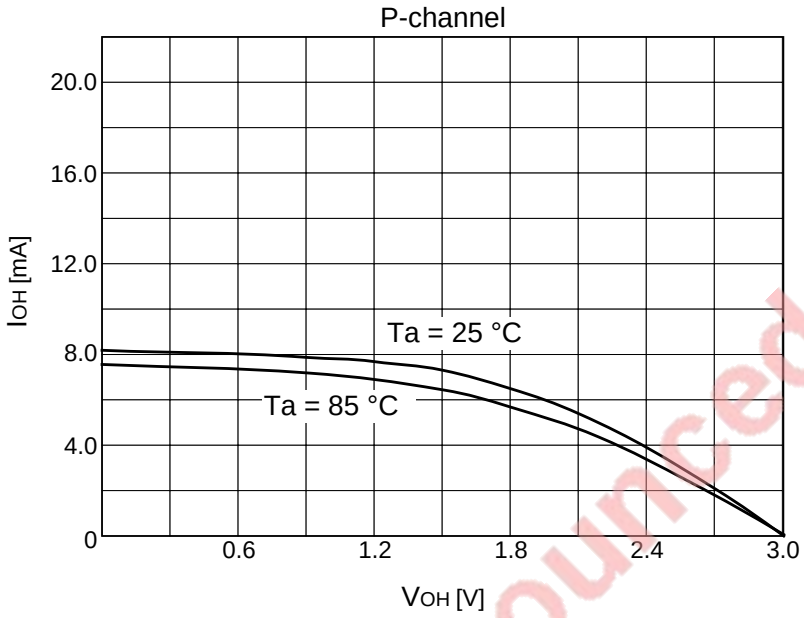
LOW VOLTAGE VERSION

18.5 Standard characteristics

18.5.2 Programmable I/O port (CMOS output) standard characteristics: Ports $P4_4$ to $P4_7$ and $P5_0$ to $P5_3$

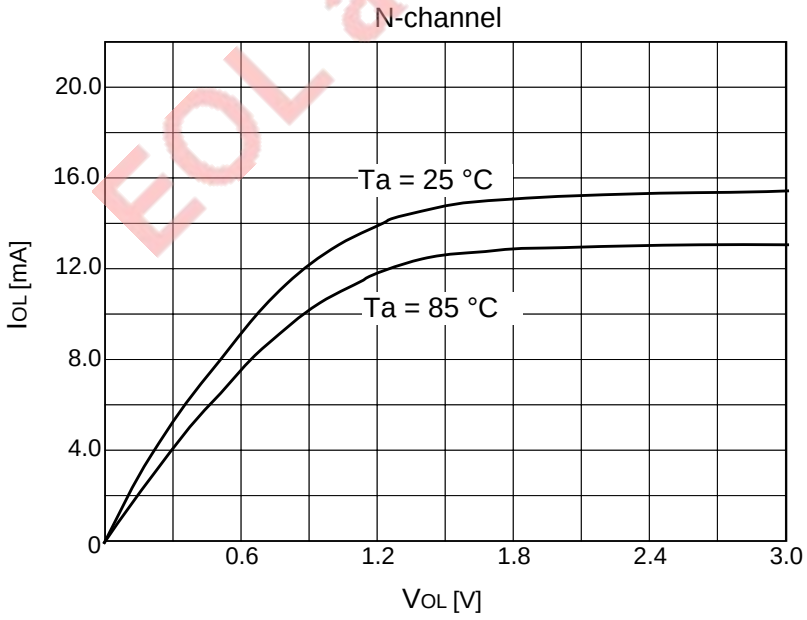
(1) P-channel I_{OH}–V_{OH} characteristics

Power source voltage V_{CC} = 3 V



(2) N-channel I_{OL}–V_{OL} characteristics

Power source voltage V_{CC} = 3 V

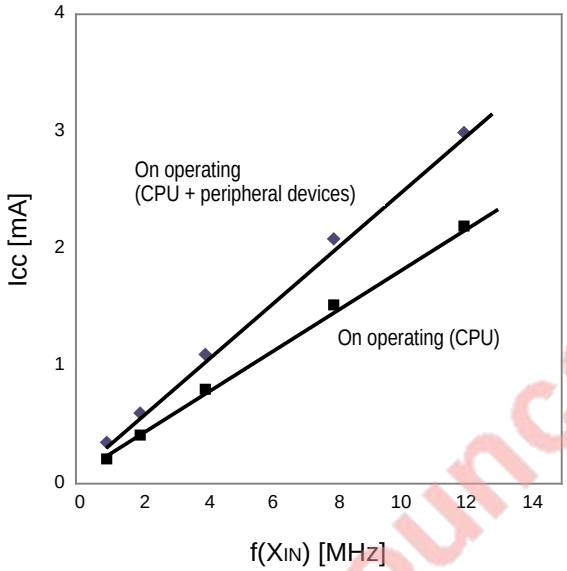


EOL announced

18.5.3 Icc–f(XIN) standard characteristics

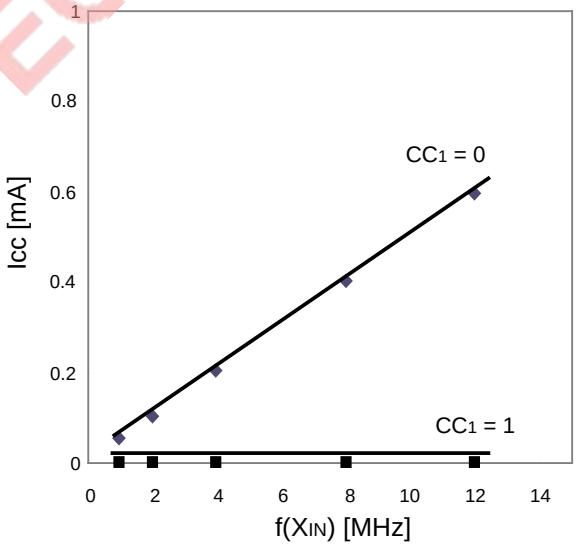
(1) Icc–f(XIN) characteristics on operating and at reset

•Measuring conditions
(Vcc = 3 V, Ta = 25 °C, f(XIN):square waveform input, single-chip mode)
•Register setting conditions
Oscillation circuit control register 1 = “02_{16}” (Main clock is input from the external.)



(2) Icc–f(XIN) characteristics during wait mode

•Measuring conditions
(Vcc = 3 V, Ta = 25 °C, f(XIN):square waveform input, single-chip mode)
•Register setting conditions
Oscillation circuit control register 0 = “20_{16}” (In wait mode, clocks f_2 to f_{512} are stopped.)
Oscillation circuit control register 1 = “02_{16}” (Main clock is input from the external.) or
“00_{16}” (Main-clock oscillation circuit is operating by itself.)



CC_1 : Main clock external input selection bit (bit 1 of oscillation circuit control register 1)

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LOW VOLTAGE VERSION

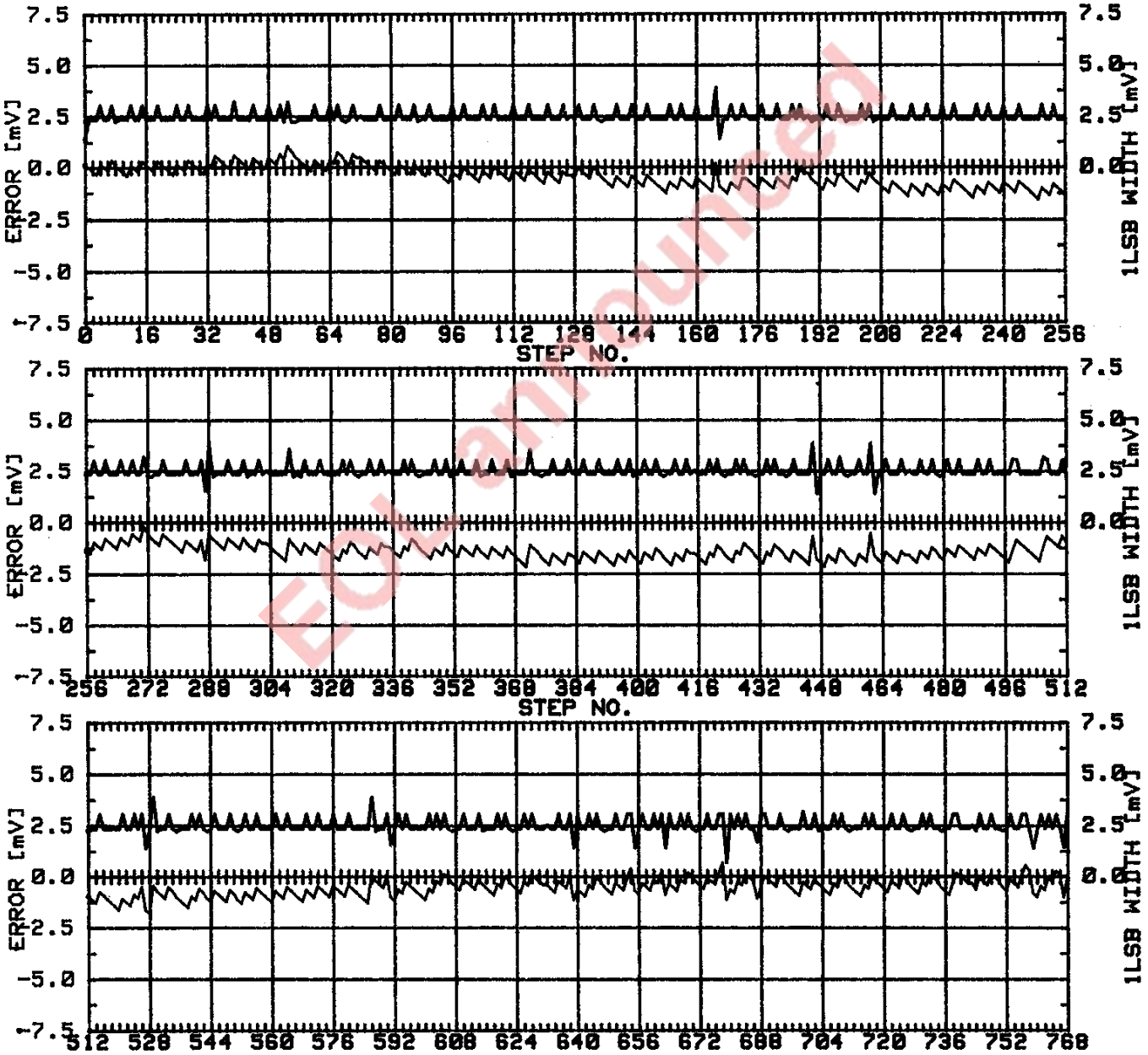
18.5 Standard characteristics

18.5.4 A-D converter standard characteristics

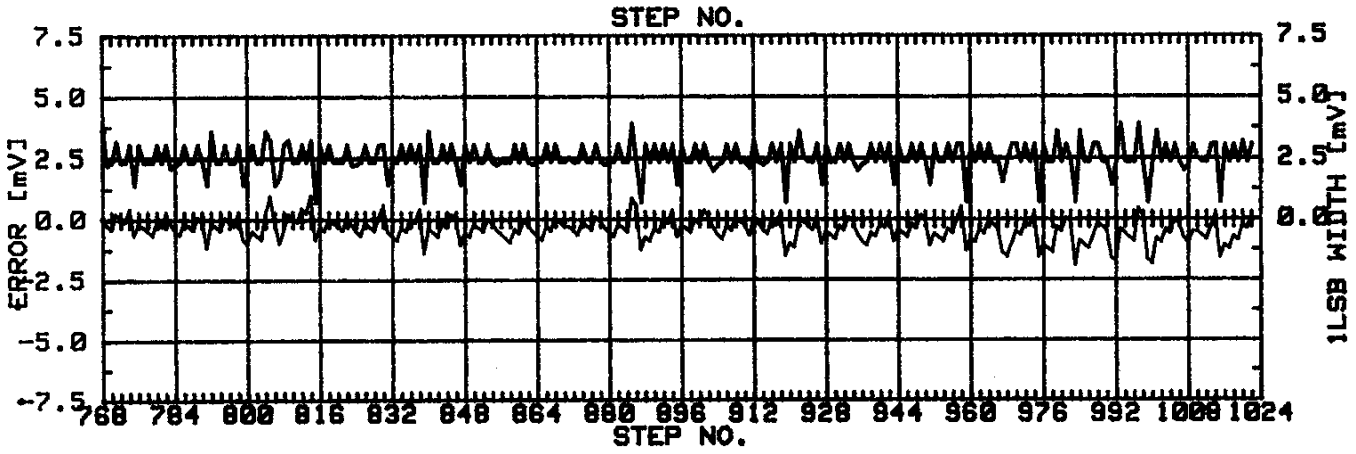
The lower line of the graph indicate the absolute precision errors. These are expressed as the deviation from the ideal value when the output code changes. For example, the change in output code from "0E16" to "0F16" should occur at 36.25 mV, but the measured value is 0.3 mV. Accordingly, the measured point of change is 36.25 + 0.3 = 36.55 mV.

The upper line of the graph indicate the input voltage width for which the output code is constant. For example, the measured input voltage width for which the output code is "0F16" is 2.2 mV. Accordingly, the differential non-linear error is 2.2 – 2.5 = –0.3 mV (–0.12 LSB).

[Measuring conditions]
•Vcc = AVcc = 3 V, •VREF = 2.56 V, •f(XIN) = 12 MHz, •Temp. = 25 °C



Evaluation purpose



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18.6 Applications

Some application examples of connecting external memorys for the low voltage version are described bellow.
Applications shown here are just examples. Modify the desired application to suit the user's need and make sufficient evaluation before actually using it.

18.6.1 Memory expansion

The following items of the low voltage version are the same as section **"17.1 Memory expansion,"** but a part of the calculation way and constants for parameters is different:

- Memory expansion model
- Calculation way for address access time of external memory
- Bus timing
- Memory expansion way

① **Address access time of external memory $t_{a(AD)}$**

$t_{a(AD)} = t_{d(A-E)} + t_{w(EL)} - t_{su(D-E)} -$ (address decode time*1 + address latch delay time*2)

address decode time*1 : time necessary for validating a chip select signal after an address is decoded
address latch delay time*2 : delay time necessary for latching an address
(This is not necessary on the minimum model.)

② **Data setup time of external memory for writing data $t_{su(D)}$**

$t_{su(D)} = t_{w(EL)} - t_{d(E-DQ)}$

Table 18.6.1 lists the calculation formulas and constants for each parameter of the low voltage version. Figure 18.6.1 shows the relationship between $t_{a(AD)}$ and $2 \times f(f_2)$. Figure 18.6.2 shows the relationship between $t_{su(D)}$ and $2 \times f(f_2)$.

Table 18.6.1 Calculation formulas and constants for each parameter (Unit : ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{d(A-E)}$	$\frac{1 \times 10^9}{2 \times f(f_2)} - 63$		$\frac{3 \times 10^9}{2 \times f(f_2)} - 88$
$t_{w(EL)}$	$\frac{2 \times 10^9}{2 \times f(f_2)} - 35$	$\frac{4 \times 10^9}{2 \times f(f_2)} - 35$	
$t_{su(D-E)}$	80		
$t_{su(E-DQ)}$	90		
$t_{pxz(E-DZ)}$	10		
$t_{pzx(E-DZ)}$	$\frac{1 \times 10^9}{2 \times f(f_2)} - 30$		

Wait bit : Bit 2 at address $5E_{16}$
Wait selection bit : Bit 0 at address $5F_{16}$
Note: This is applied to the case where the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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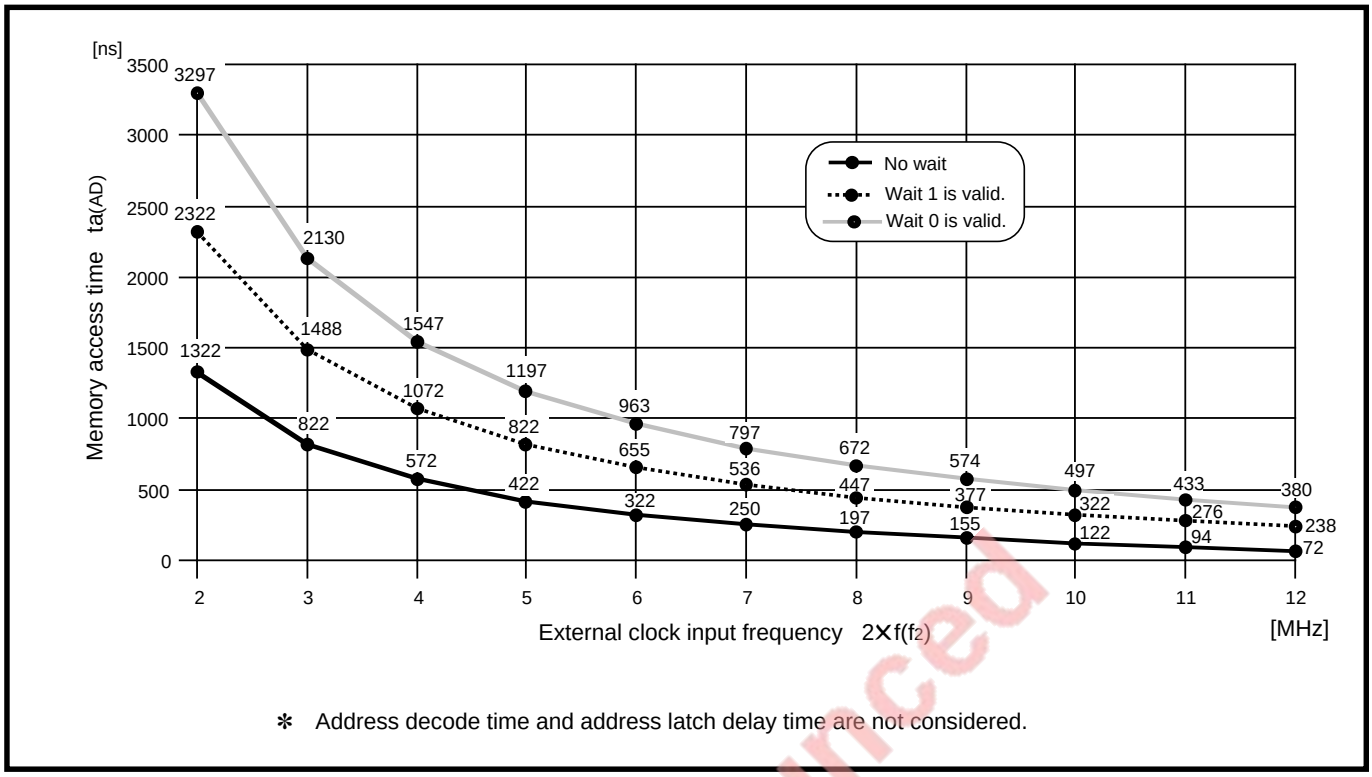


Fig. 18.6.1 Relationship between $t_{a(AD)}$ and $2 \times f(f_2)$

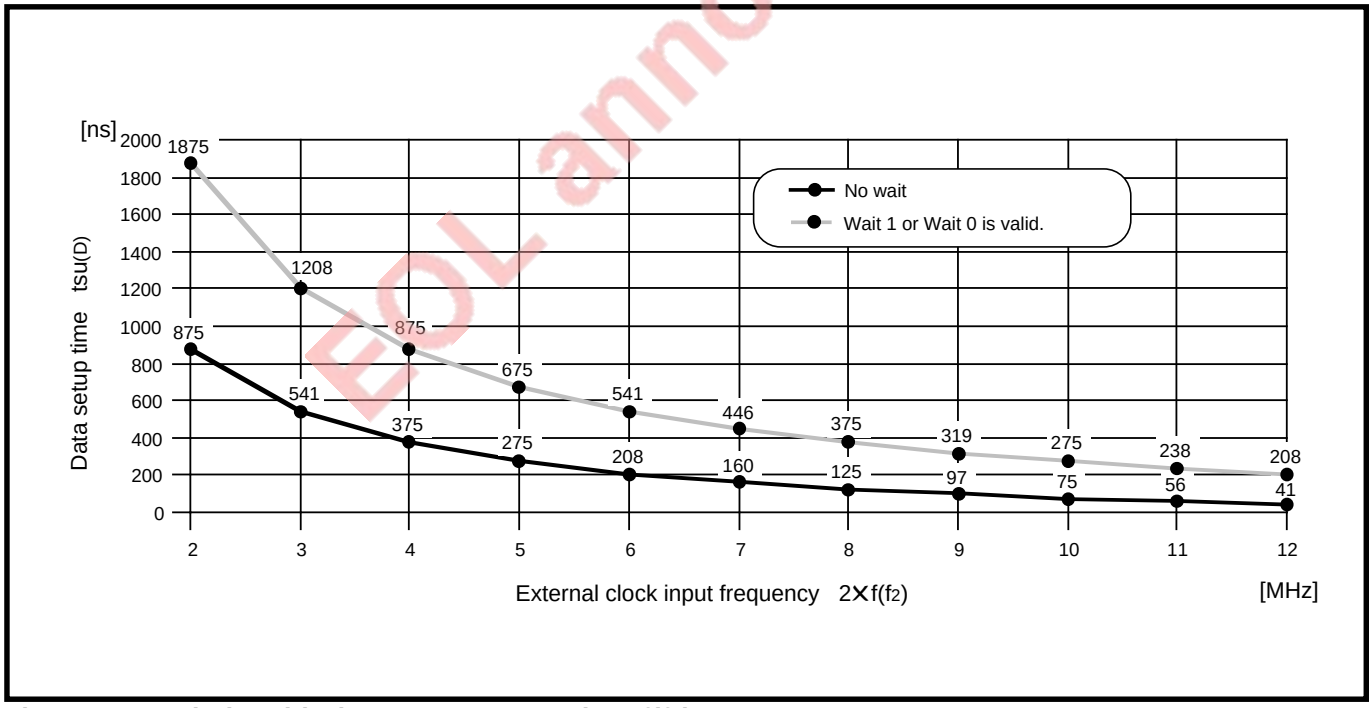


Fig. 18.6.2 Relationship between $t_{su(D)}$ and $2 \times f(f_2)$

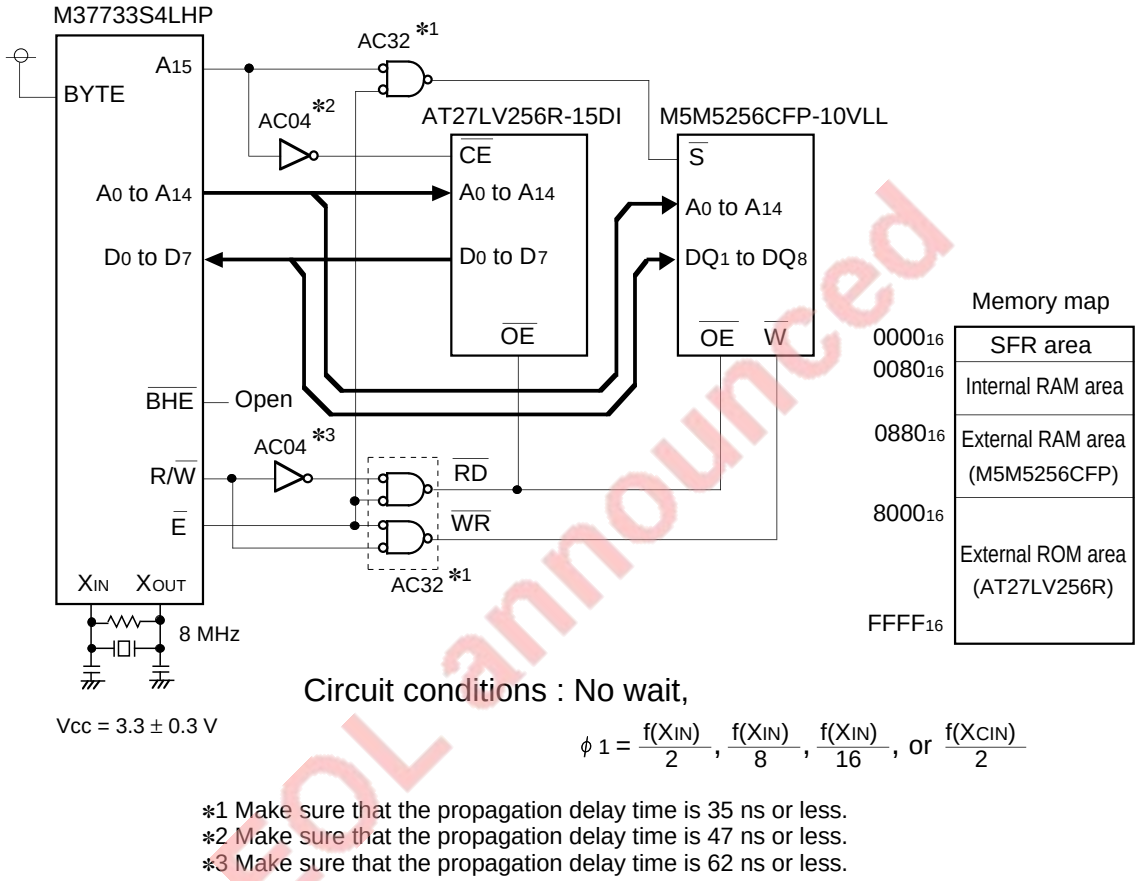
EOL announced

18.6 Applications

18.6.2 Memory expansion example on minimum model

Figure 18.6.3 shows a memory expansion example on the minimum model (with external RAM) and Figure 18.6.4 shows the corresponding timing diagram. In example, an Atmel company's EPROM (AT27LV256R) is used as the external ROM.

In Figure 18.6.3, the circuit condition is "No wait."



*1 Make sure that the propagation delay time is 35 ns or less.
*2 Make sure that the propagation delay time is 47 ns or less.
*3 Make sure that the propagation delay time is 62 ns or less.

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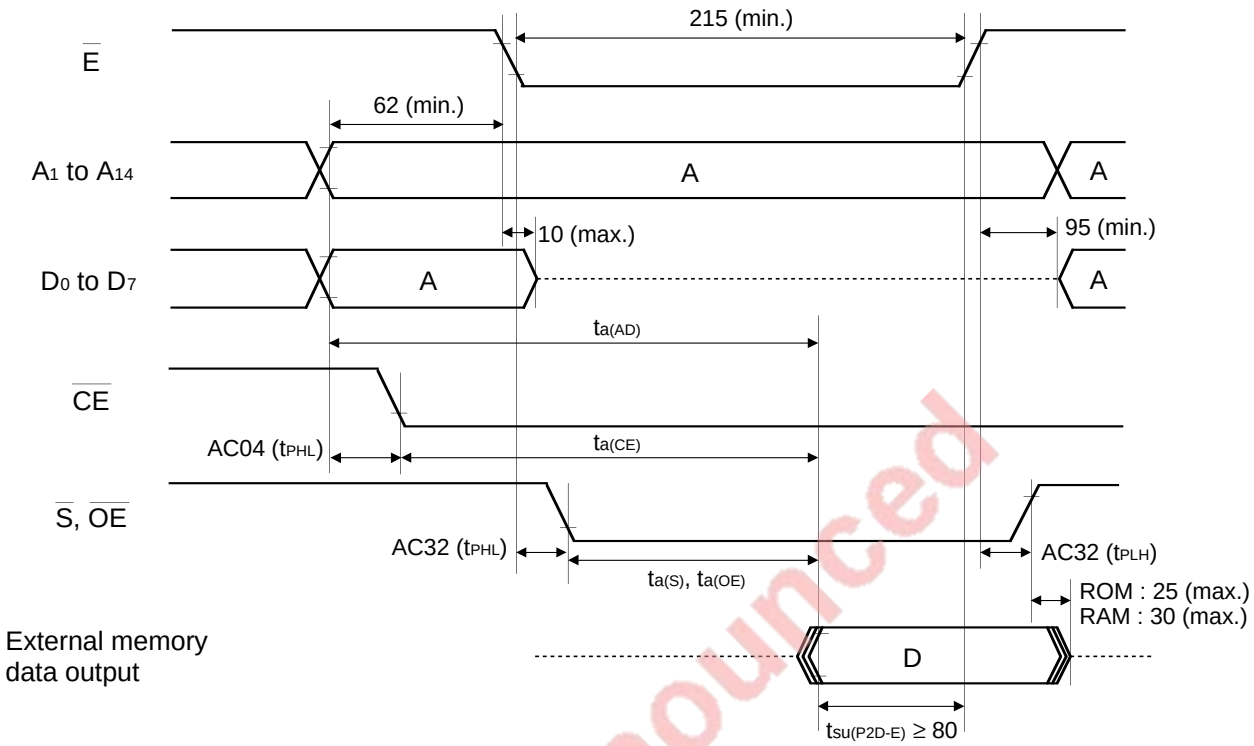
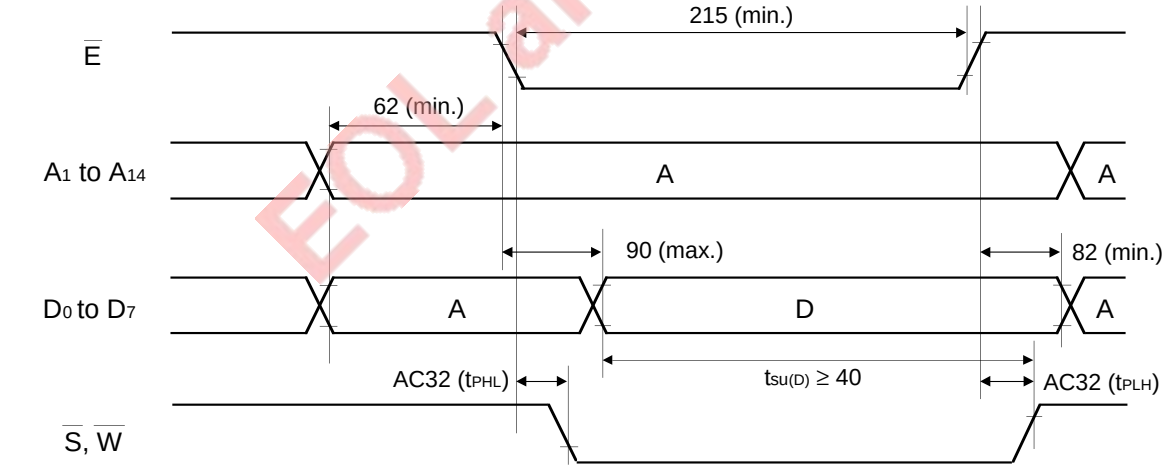
Fig. 18.6.3 Memory expansion example on minimum model

●At reading



●At writing



(Unit : ns)

EOL announced

Fig. 18.6.4 Timing diagram on minimum model

18.6 Applications

18.6.3 Memory expansion example on medium model A

Figure 18.6.5 shows a memory expansion example on the medium model A. Figure 18.6.6 shows the corresponding timing diagram.

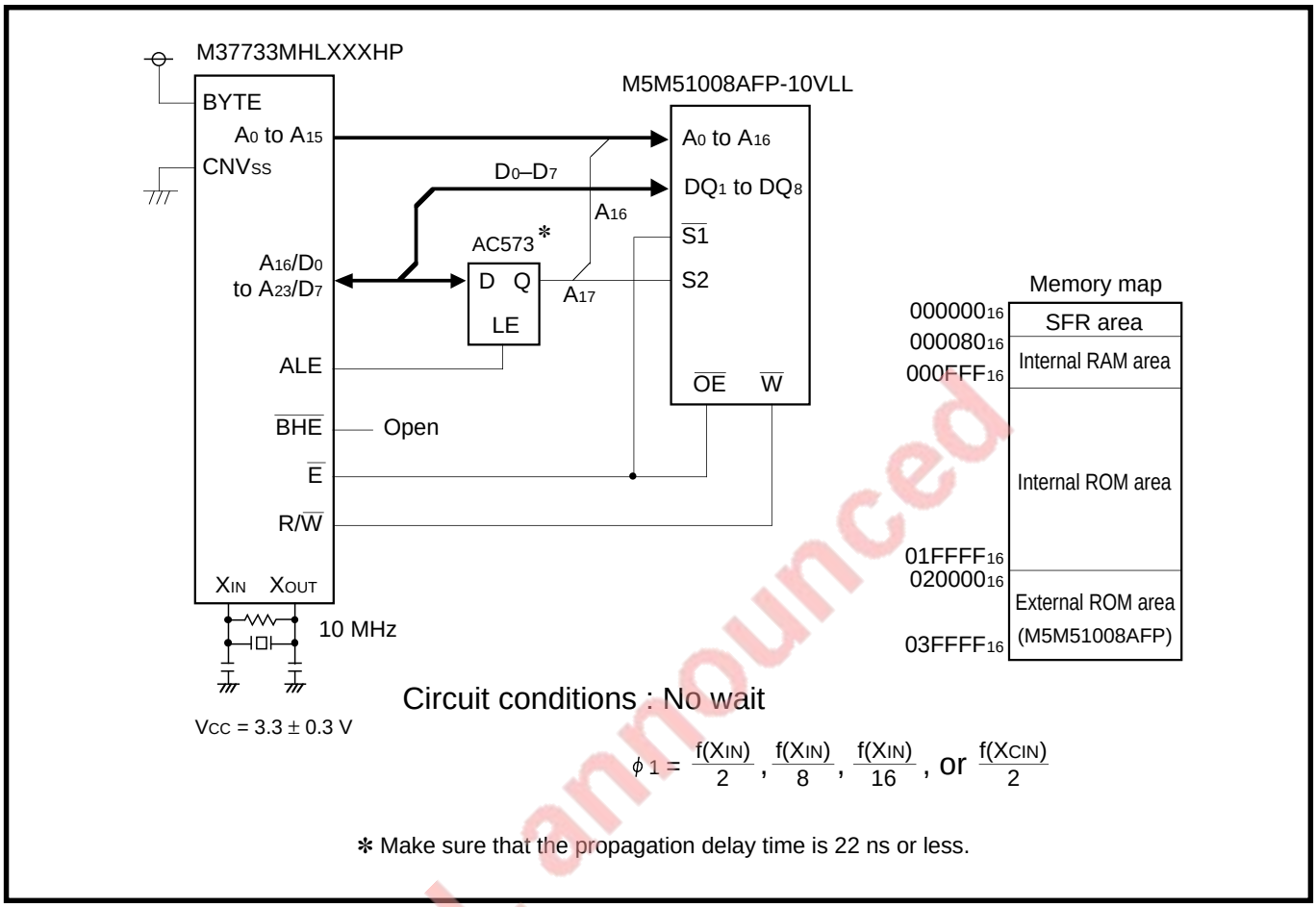


Fig. 18.6.5 Memory expansion example on medium model A

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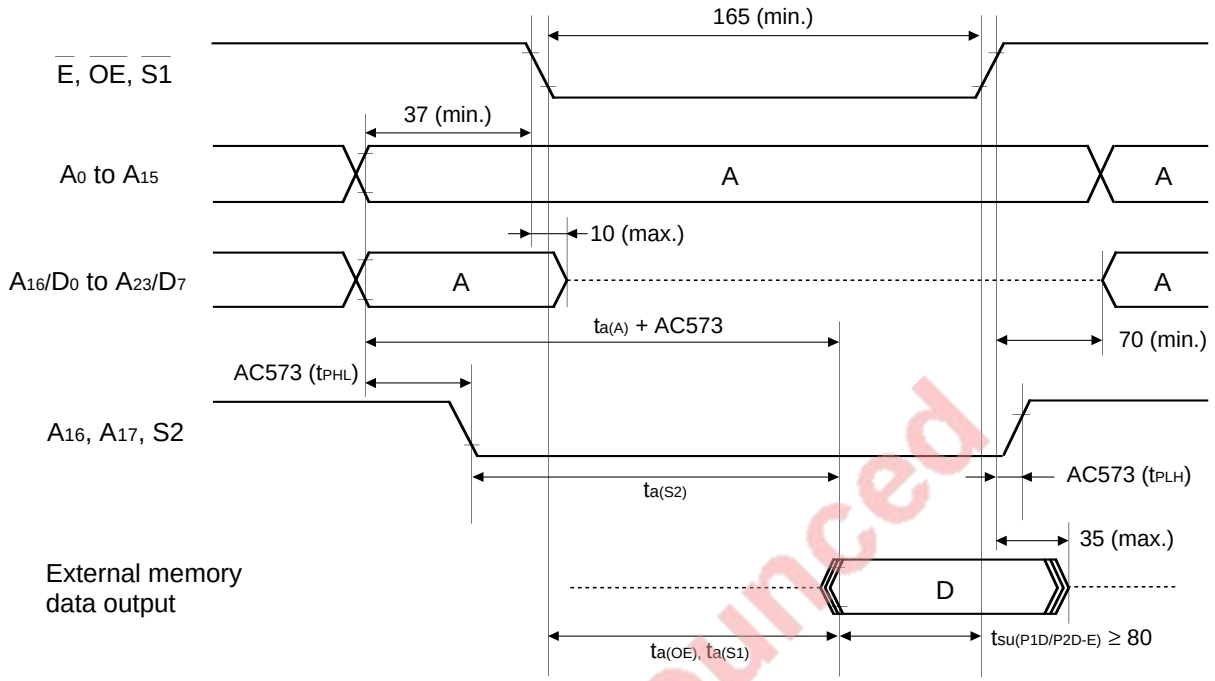
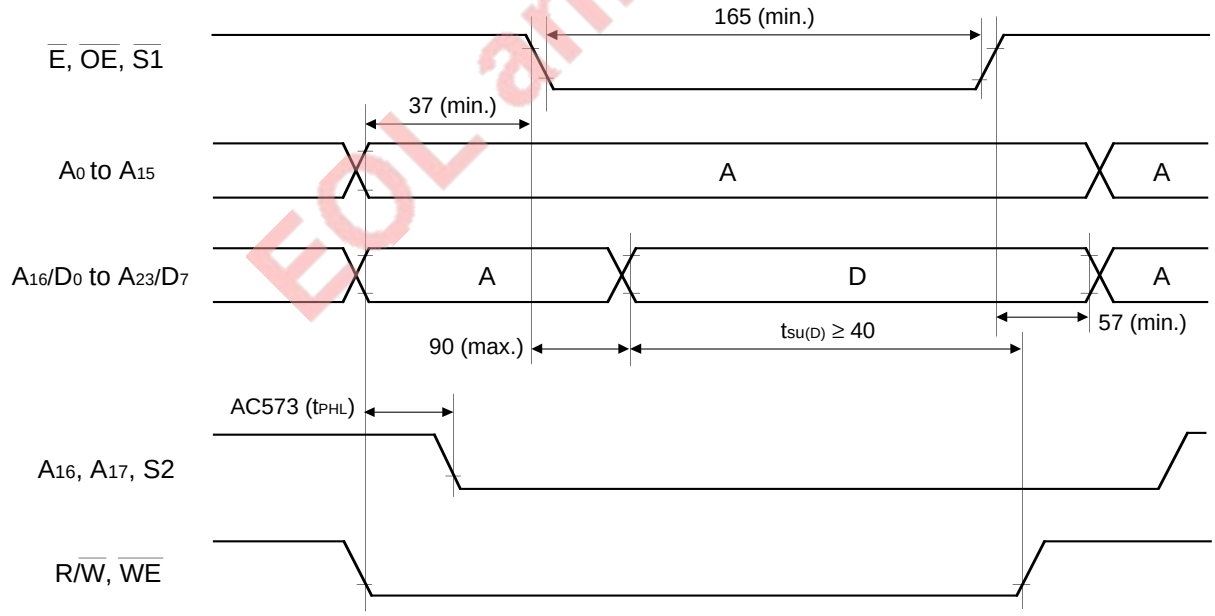
●At reading



●At writing



(Unit : ns)

EOL announced

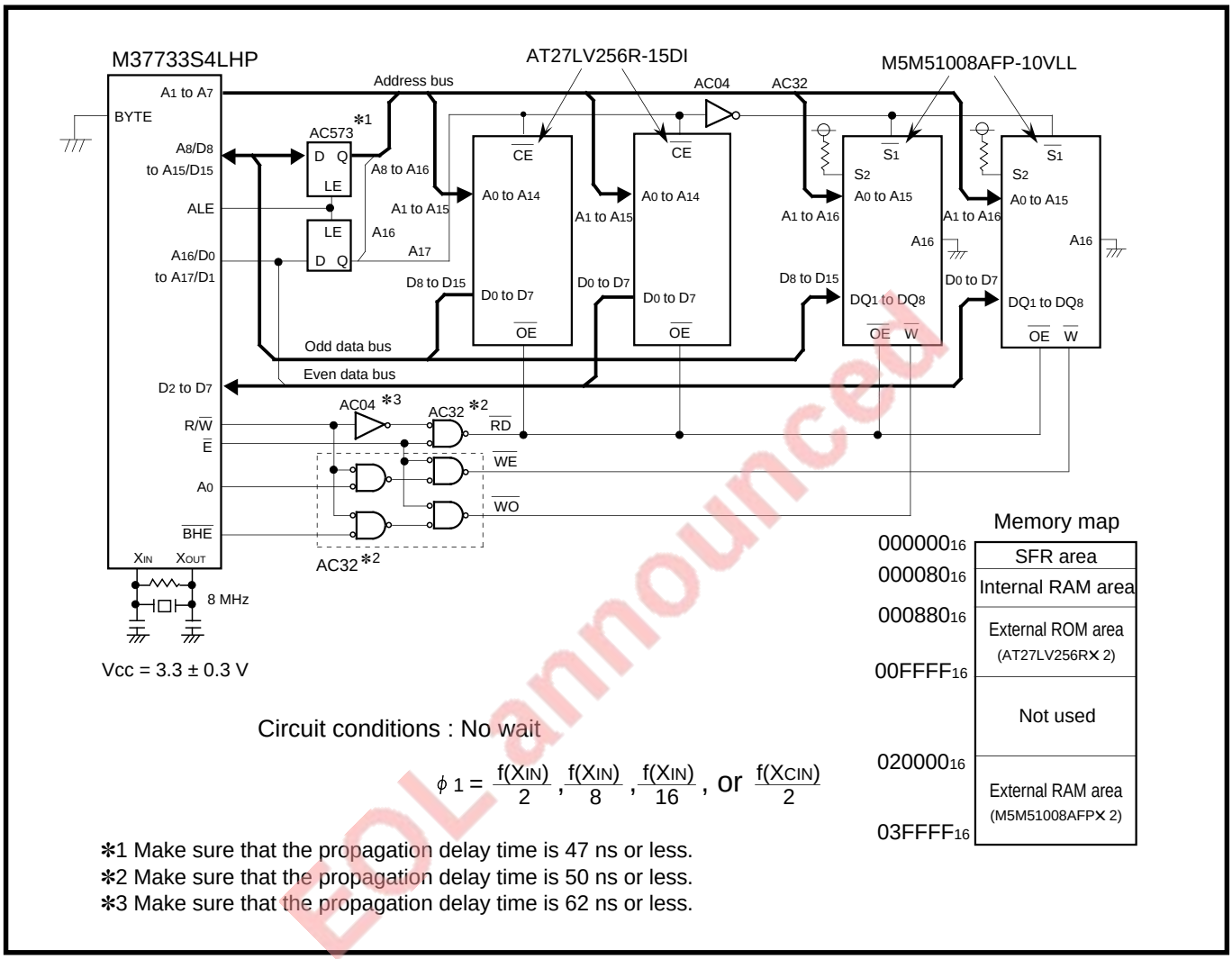
Fig. 18.6.6 Timing diagram on medium model A

18.6 Applications

18.6.4 Memory expansion example on maximum model

Figure 18.6.7 shows a memory expansion example on the maximum model. Figure 18.6.8 shows the corresponding timing diagram. In this example, Atmel company's EPROMs (AT27LV256R) are used as the external ROMs.

In Figure 18.6.7, the circuit condition is "No wait."



$$\phi 1 = \frac{f(X_{IN})}{2}, \frac{f(X_{IN})}{8}, \frac{f(X_{IN})}{16}, \text{ or } \frac{f(X_{CIN})}{2}$$

∗1 Make sure that the propagation delay time is 47 ns or less.
∗2 Make sure that the propagation delay time is 50 ns or less.
∗3 Make sure that the propagation delay time is 62 ns or less.

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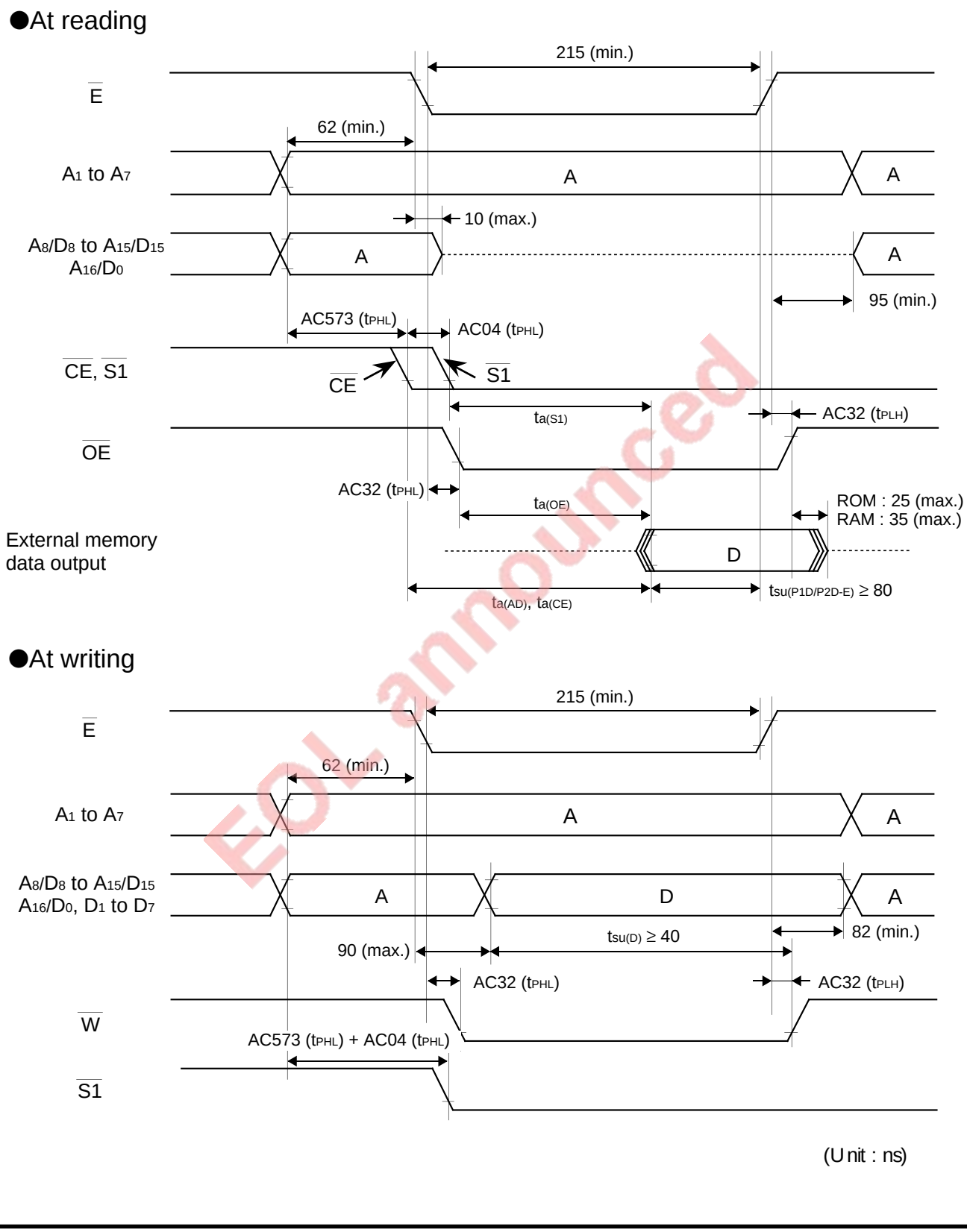
Fig. 18.6.7 Memory expansion example on maximum model



EOL announced

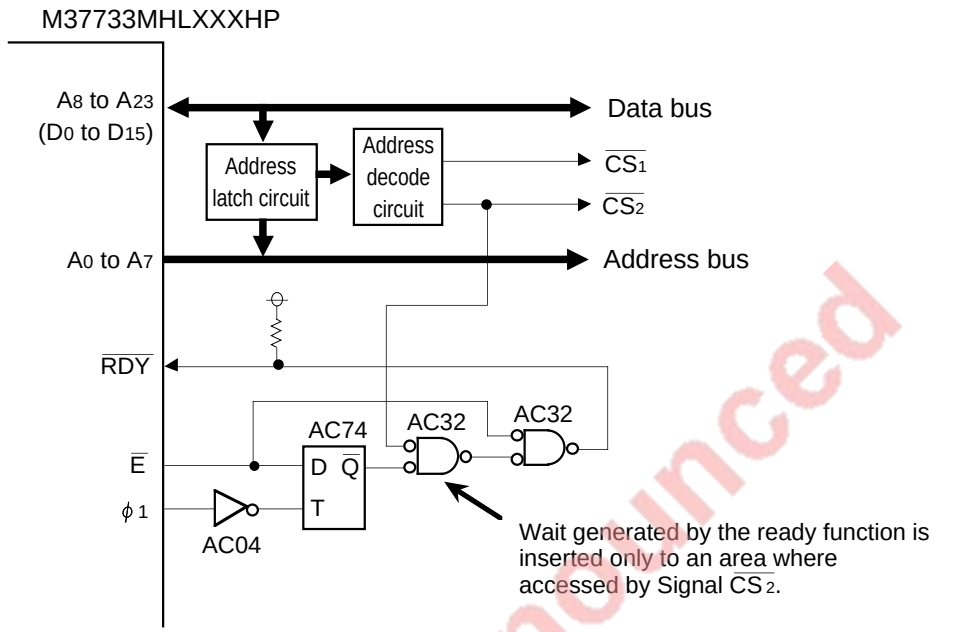
Fig. 18.6.8 Timing diagram on maximum model

18.6 Applications

18.6.5 Ready generating circuit example

When validating “wait” only for a certain area (for example, ROM area) in Figures 18.6.3 to 18.6.8, use the ready function.

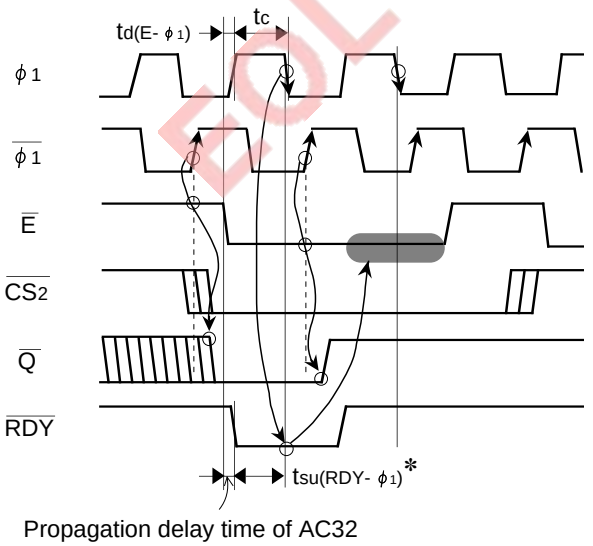
Figure 18.6.9 shows a ready generating circuit example.



Circuit conditions : $f(X_{IN}) \leq 10.8$ MHz, no wait,

V_{CC} = 3.0 to 5.5 V

$\phi 1 = \frac{f(X_{IN})}{2}, \frac{f(X_{IN})}{8}, \frac{f(X_{IN})}{16}$, or $\frac{f(X_{CIN})}{2}$



Propagation delay time of AC32
(Max. : 11.9 ns)

* Condition to satisfy the relationship of $t_{su(RDY-\phi 1)} \geq 80$ ns in the left timing chart is $t_c \geq 91.9$ ns. Accordingly, when $f(X_{IN}) \leq 10.8$ MHz, this example satisfies the relationship of $t_{su(RDY-\phi 1)} \geq 80$ ns.

: Wait generated by the ready function

EOL announced

Fig. 18.6.9 Ready generating circuit example

CHAPTER 19

BUILT-IN PROM VERSION

19.1 EPROM mode
19.2 Usage precaution

EOL announced

BUILT-IN PROM VERSION

In the PROM version, programming to the built-in PROM is possible by using a general-purpose PROM programmer and a programming adapter which is suitable for the microcomputer.
The built-in PROM version has the following two types :

●**One Time PROM version**
Programming to the PROM is possible once.
This version is suitable for a small quantity of and various production.

●**EPROM version**
Programming to the PROM is possible repeatedly because a program can be erased by exposing the erase window on the top of the package to an ultraviolet light source.
This version can be used only for program development (Evaluation only).

The built-in PROM version differs from the mask ROM version in the following:
- The built-in PROM version has a built-in PROM.
- Bit 3 of the oscillation circuit control register 1 (address $6F_{16}$) of the built-in PROM version is “1” at reset.
- Bit 3 of the oscillation circuit control register 1 (address $6F_{16}$) of the built-in PROM version must be fixed to “1.”

EOL announced

19.1 EPROM mode

The built-in PROM version has the following two modes :

●**Normal operating mode**
The microcomputer has the same function as the mask ROM version.

●**EPROM mode**
Programming to the built-in PROM can be performed. The built-in PROM version enters this mode when "L" level is input to pin $\overline{\text{RESET}}$.

19.1.1 Pin description

Table 19.1.1 lists the pin description in the EPROM mode.
In the normal operating mode, each pin has the same function as the mask ROM version.

Table 19.1.1 Pin description in EPROM mode

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source input	—	Apply 5 V ± 10% to pin Vcc, and 0 V to pin Vss.
CNVss	V_{PP} input	Input	Apply V_{PP} level when programming or verifying.
BYTE			
$\overline{\text{RESET}}$	Reset input	Input	Connect to pin Vss.
X_{IN}	Clock input	Input	Connect pins X_{IN} and X_{OUT} via a ceramic resonator or a quartz-crystal oscillator. When an external clock is used, the clock should be input to pin X_{IN}, and pin X_{OUT} should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Open.
AVcc, AVss	Analog power source input	—	Connect pin AVcc to pin Vcc and pin AVss to pin Vss.
V_{REF}	Reference voltage input	Input	Connect to pin Vss.
$P0_0$–$P0_7$	Address input (A_0–A_7)	Input	Input pins for low-order 8 bits (A_0–A_7) of address
$P1_0$–$P1_7$	Address input (A_8–A_{15})	Input	Input pins for middle-order 8 bits (A_8–A_{15}) of address
$P2_0$–$P2_7$	Data input/output (D_0–D_7)	I/O	I/O pins for 8-bit data (D_0–D_7)
$P3_0$	Address input (A_{16})	Input	Input pin for the most significant bit (A_{16}) address
$P3_1$–$P3_3$	Input port P3	Input	Connect to pin Vss.
$P4_0$–$P4_7$	Input port P4	Input	Connect to pin Vss.
$P5_0$–$P5_7$	Control input	Input	$P5_0$, $P5_1$ and $P5_2$ respectively function as $\overline{\text{PGM}}$, $\overline{\text{OE}}$ and $\overline{\text{CE}}$ input pins. Connect $P5_3$–$P5_6$ to pin Vcc, and $P5_7$ to pin Vss.
$P6_0$–$P6_7$	Input port P6	Input	Connect to pin Vss.
$P7_0$–$P7_7$	Input port P7	Input	Connect to pin Vss.
$P8_0$–$P8_7$	Input port P8	Input	Connect to pin Vss.

EOL announced

BUILT-IN PROM VERSION

19.1 EPROM mode

19.1.2 Reading/Programming from and to built-in PROM

In the EPROM mode, ports P0, P1, P2, $P3_0$, $P5_0$, $P5_1$, $P5_2$ and pins CNVss and BYTE are EPROM pins (M5M27C101K equivalent), and reading/programming from and to the built-in PROM can be performed in the same manner as for M5M27C101K. However, there is no device identification code. Accordingly, programming conditions must be set carefully. Furthermore, specify addresses from 01000_{16} to $1FFFF_{16}$ as the programmable area.

Table 19.1.2 lists the pin correspondence in the EPROM mode and Table 19.1.3 lists the programmable area. Figures 19.1.1 and 19.1.2 show the pin connections in the EPROM mode.

Table 19.1.2 Pin correspondence in EPROM mode

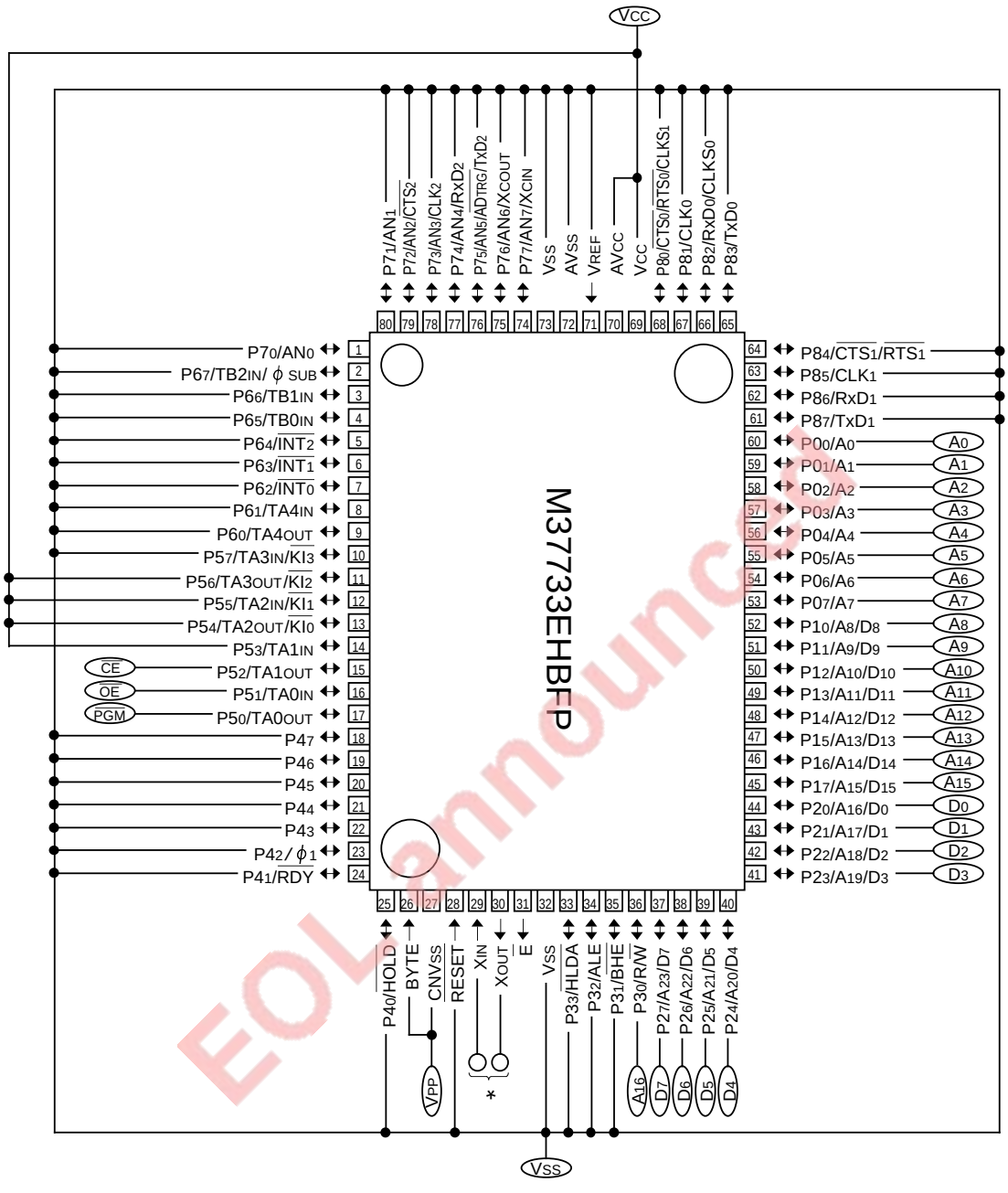
	M37733EHBFP(M37733EHBXXXFP) M37733EHBFS M37733EHLHP(M37733EHLXXXHP)	M5M27C101K
Vcc	Vcc	Vcc
V_{PP}	CNVss, BYTE	V_{PP}
Vss	Vss	Vss
Address input	P0, P1, $P3_0$	A_0–A_{16}
Data I/O	P2	D_0–D_7
$\overline{CE}$	$P5_2$	$\overline{CE}$
$\overline{OE}$	$P5_1$	$\overline{OE}$
$\overline{PGM}$	$P5_0$	$\overline{PGM}$

Table 19.1.3 Programmable area

Memory allocation selection bits			Programmable area
b2	b1	b0	
0	0	0	01000_{16}–$1FFFF_{16}$
0	0	1	02000_{16}–$1FFFF_{16}$
0	1	0	01000_{16}–$0FFFF_{16}$
1	0	0	08000_{16}–$0FFFF_{16}$
1	0	1	$0C000_{16}$–$0FFFF_{16}$
1	1	0	08000_{16}–$1FFFF_{16}$

Note: When changing the allocation of the internal memory by the memory allocation selection bits (Refer to **Figure 2.4.1.**), specify addresses listed in **Table 19.1.3** as the programmable area.

EOL announced



* : Connect these pins to a resonator or an oscillator.

: EPROM pin.

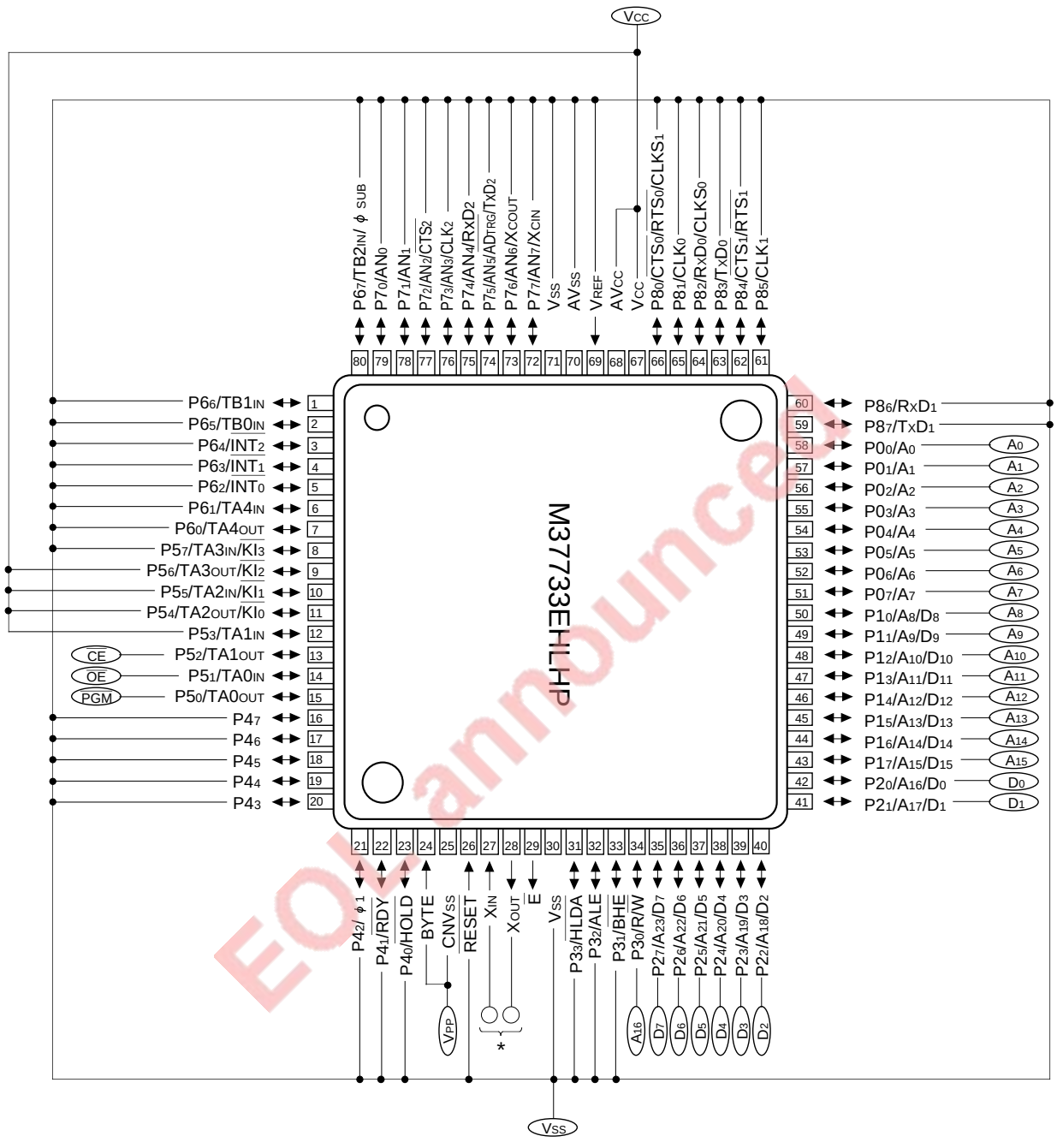
Outline 80P6N-A

Fig. 19.1.1 Pin connections in EPROM mode (M37733EHBFP)

EOL announced

BUILT-IN PROM VERSION

19.1 EPROM mode



* : Connect these pins to a resonator or an oscillator.

: EPROM pin.

Outline 80P6D-A

Fig. 19.1.2 Pin connections in EPROM mode (M37733EHLHP)

(1) Read

When pins $\overline{CE}$ and $\overline{OE}$ are set to "L" level and an address is input to address input pins, the contents of the built-in PROM can be read from data I/O pins; When pins $\overline{CE}$ and $\overline{OE}$ are set to "H" level, data I/O pins enter the floating state.

(2) Program

When pin $\overline{CE}$ is set to "L" level, pin $\overline{OE}$ is set to "H" level, and V_{PP} level is applied to pin V_{PP}, programming to the PROM can be performed.

Input an address to address input pins and supply data to be programmed to data I/O pins in 8-bit parallel. On this condition, when pin $\overline{PGM}$ is set to "L" level, the data is programmed into the built-in PROM.

(3) Erase (Available only in EPROM version)

The contents of the built-in PROM is erased by exposing the glass window on top of the package to an ultraviolet light which has a wave length of 2537 Angstrom. The light must be 15 W•s/cm^2 or more.

Table 19.1.4 I/O signals in EPROM mode

Mode \ Pin name	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	X	5 V	5 V	Output
Output disable	V_{IL}	V_{IH}	X	5 V	5 V	Floating
	V_{IH}	X	X	5 V	5 V	Floating
Program	V_{IL}	V_{IH}	V_{IL}	12.5 V	6 V	Input
Program verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6 V	Output
Program disable	V_{IH}	V_{IH}	V_{IH}	12.5 V	6 V	Floating

X : It may be V_{IL} or V_{IH}.

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BUILT-IN PROM VERSION

19.1 EPROM mode

19.1.3 Programming algorithm to built-in PROM

① Set Vcc = 6 V, VPP = 12.5 V, and address to 0100016. (Refer to **Table 19.1.3.**)
② After applying a programming pulse of 0.2 ms, check whether data can be read or not.
③ If the data cannot be read, apply a programming pulse of 0.2 ms again.
④ Repeat the procedure, which consists of applying a programming pulse of 0.2 ms and read check, until the data can be read. Additionally, record the number of pulses applied (X) before the data was read.
⑤ Apply X pulses (0.2 × X ms) (described in ④) as additional programming pulses.
⑥ When this procedure (① to ⑤) is complete, increment the address and repeat the above procedure until the last address is reached.
⑦ After programming to the last address, read data when Vcc = VPP = 5 V (or Vcc = VPP = 5.5 V).

Figure 19.1.3 shows the programming algorithm flow chart.

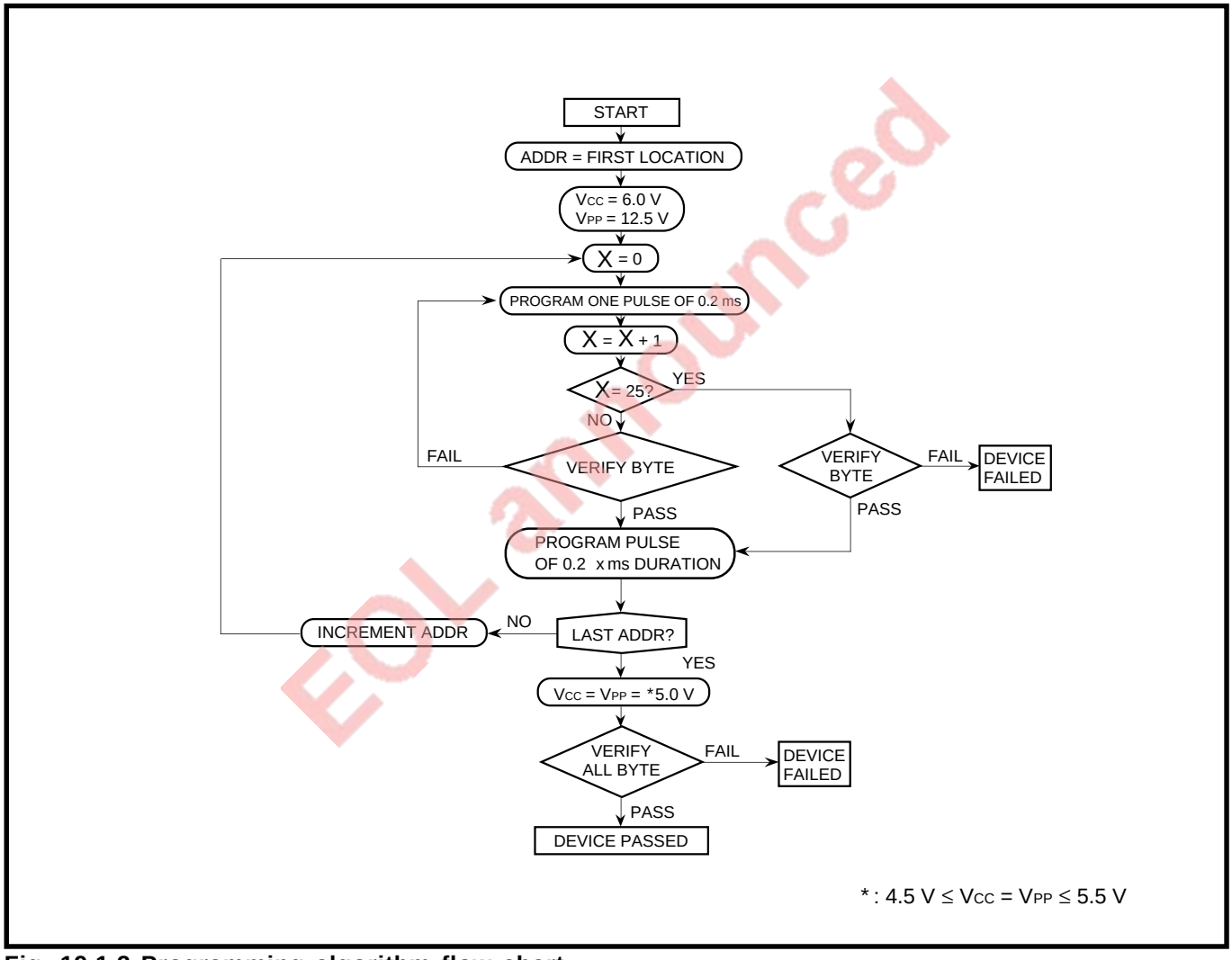

Fig. 19.1.3 Programming algorithm flow chart

EOL announced

19.1.4 Electrical characteristics of programming algorithm

AC electrical characteristics (Ta = 25 ± 5 °C, Vcc = 6 V ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address setup time	2			μs
t_{OES}	$\overline{OE}$ setup time	2			μs
t_{DS}	Data setup time	2			μs
t_{AH}	Address hold time	0			μs
t_{DH}	Data hold time	2			μs
t_{DFP}	Output floating delay time after $\overline{OE}$	0		130	ns
t_{VCS}	Vcc setup time	2			μs
t_{VPS}	V_{PP} setup time	2			μs
t_{PW}	$\overline{PGM}$ pulse width	0.19	0.2	0.21	ms
t_{OPW}	Additional $\overline{PGM}$ pulse width	0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time	2			μs
t_{OE}	Data delay time after $\overline{OE}$			150	ns

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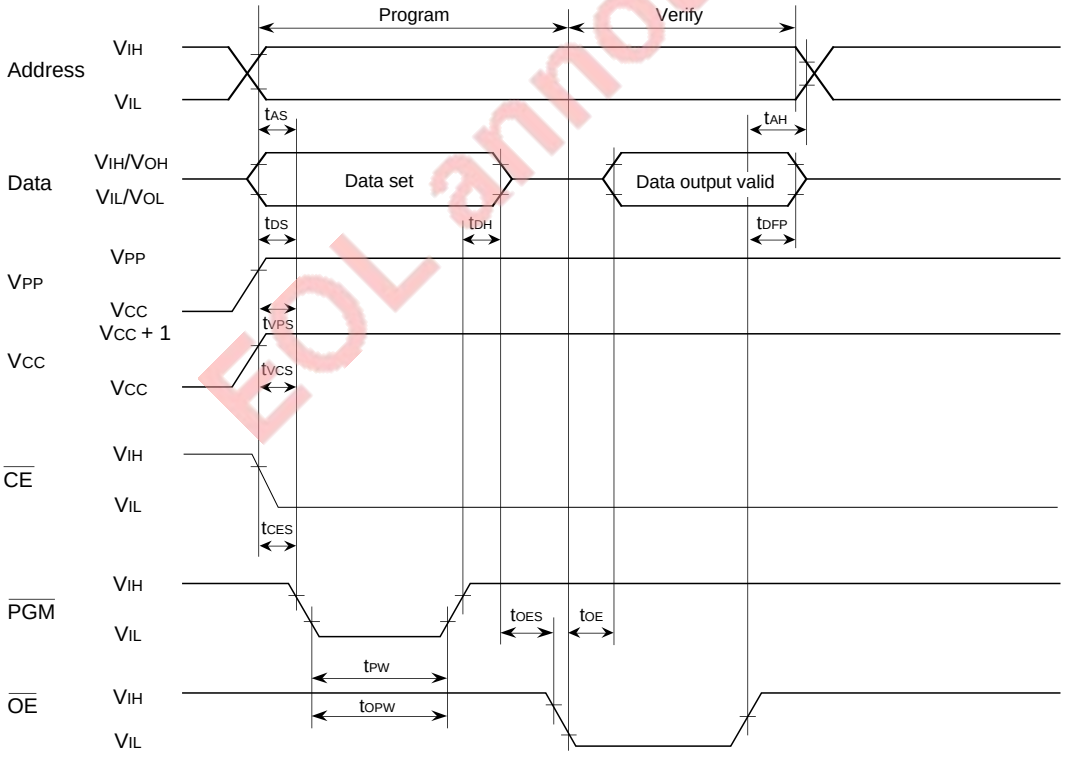
Programming timing diagram



Switching characteristics measuring conditions
- Input voltage : V_{IL} = 0.45 V, V_{IH} = 2.4 V
- Input signal rise/fall time (10%–90%) : ≤ 20 ns
- Reference voltage in timing measurement : Input/output “L” = 0.8 V, “H” = 2 V

19.2 Usage precaution

[Precautions on all built-in PROM versions]
When programming to the built-in PROM, high voltage is required. Accordingly, be careful not to apply excessive voltage to the microcomputer. Furthermore, be especially careful during power-on.

[Precautions on One Time PROM version]
One Time PROM versions shipped in blank (M37733EHBFP, M37733EHLHP), of which built-in PROMs are programmed by users, are also provided.
For these microcomputers, a programming test and screening are not performed in the assembly process and the following processes. To improve their reliability after programming, we recommend to program and test as the flow shown in Figure 19.2.1 before use.

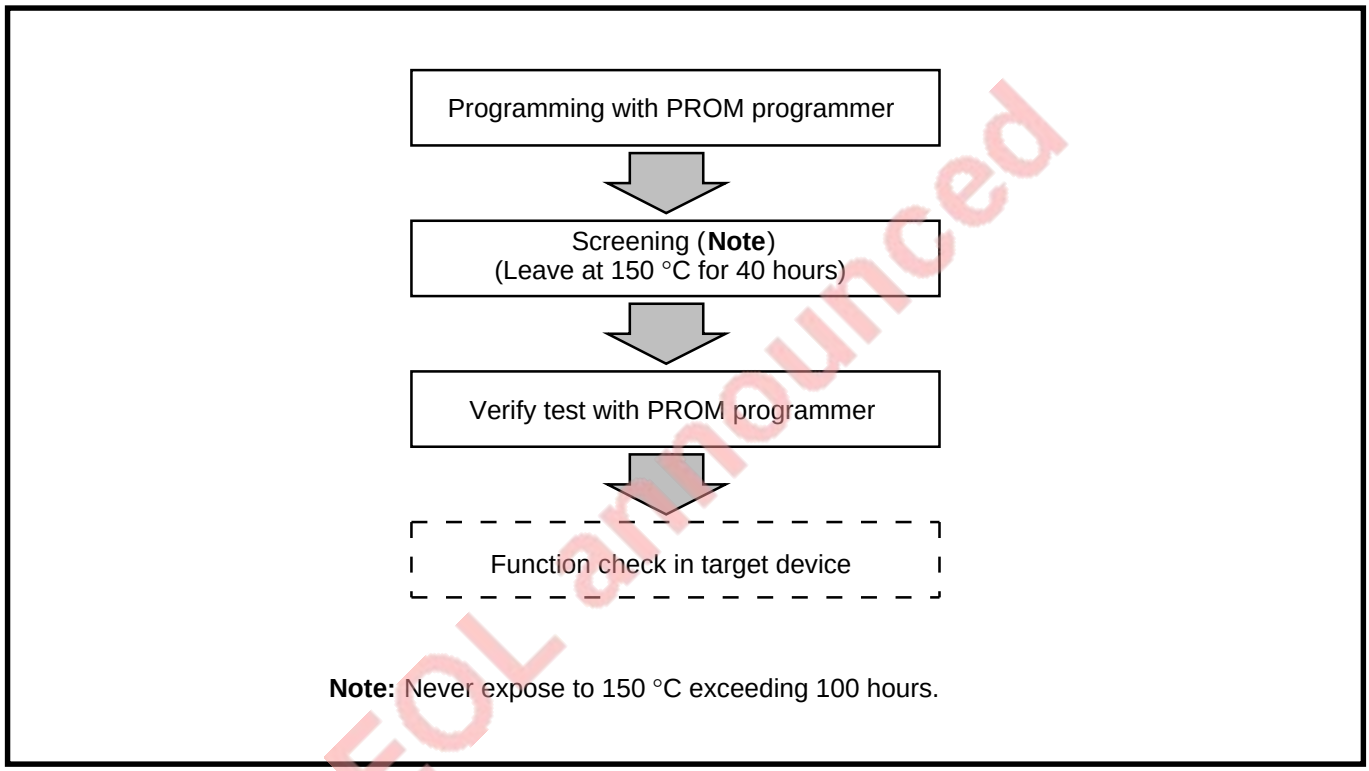


Fig. 19.2.1 Programming and test flow for One Time PROM version

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[Precautions on EPROM version]
- Cover the transparent glass window with a shield or others during the read mode because exposing to sun light or fluorescent lamp can cause erasing the programmed data.
  A shield to cover the transparent window is available from Mitsubishi Electric Corporation. Be careful that the shield does not touch the EPROM lead pins.
- Clean the transparent glass before erasing. There is a possibility that fingers' flat and paste disturb the passage of ultraviolet rays and affect badly the erasure capability.
- The EPROM version is a tool only for program development (Evaluation only), and do not use it for the mass product run.

CHAPTER 20
EXTERNAL ROM VERSION

EOL announced

20.1 Performance overview
20.2 Pin configuration
20.3 Pin description
20.4 Block description
20.5 Memory allocation
20.6 Processor modes
20.7 Timer A
20.8 Reset
20.9 Electrical characteristics
20.10 Low voltage version

EXTERNAL ROM VERSION

The external ROM version can operate only in the microprocessor mode.
Functions of the external ROM version differ from those of the mask ROM version in the following. Therefore, only the differences are described in this chapter:

- Memory allocation
- Operation is available only in the microprocessor mode
- The ROM area change function is not available.
- Timer A has the pulse output port mode.
- Power source current and Current consumption

For the other functions, refer to chapters **"2. CENTRAL PROCESSING UNIT (CPU)"** to **"18. LOW VOLTAGE VERSION."**

✵ For product expansion information of the 7733 Group, contact the appropriate office, as listed in "CONTACT ADDRESSES FOR FURTHER INFORMATION."

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20.1 Performance overview

Performance overview of the external ROM version differs from that of the mask ROM version in the following: memory size and current consumption. For the other items, refer to section **"1.1 Overview."**

Table 20.1.1 lists the M37733S4BFP's performance overview.

Table 20.1.1 M37733S4BFP's performance overview

Items		Performance
Memory size	RAM	2048 bytes
Current consumption		57 mW (When f(XIN) = 25-MHz external square wave input, Vcc = 5 V, and the main clock is the system clock, Typ.)
		300 μW (When f(XCIN) = 32 kHz, Vcc = 5 V, the sub clock is the system clock, and the main clock is stopped, Typ.)

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20.2 Pin configuration

Figure 20.2.1 shows the M37733S4BFP pin configuration.

Note: For the low voltage version, refer to section **"20.10 Low voltage version."**

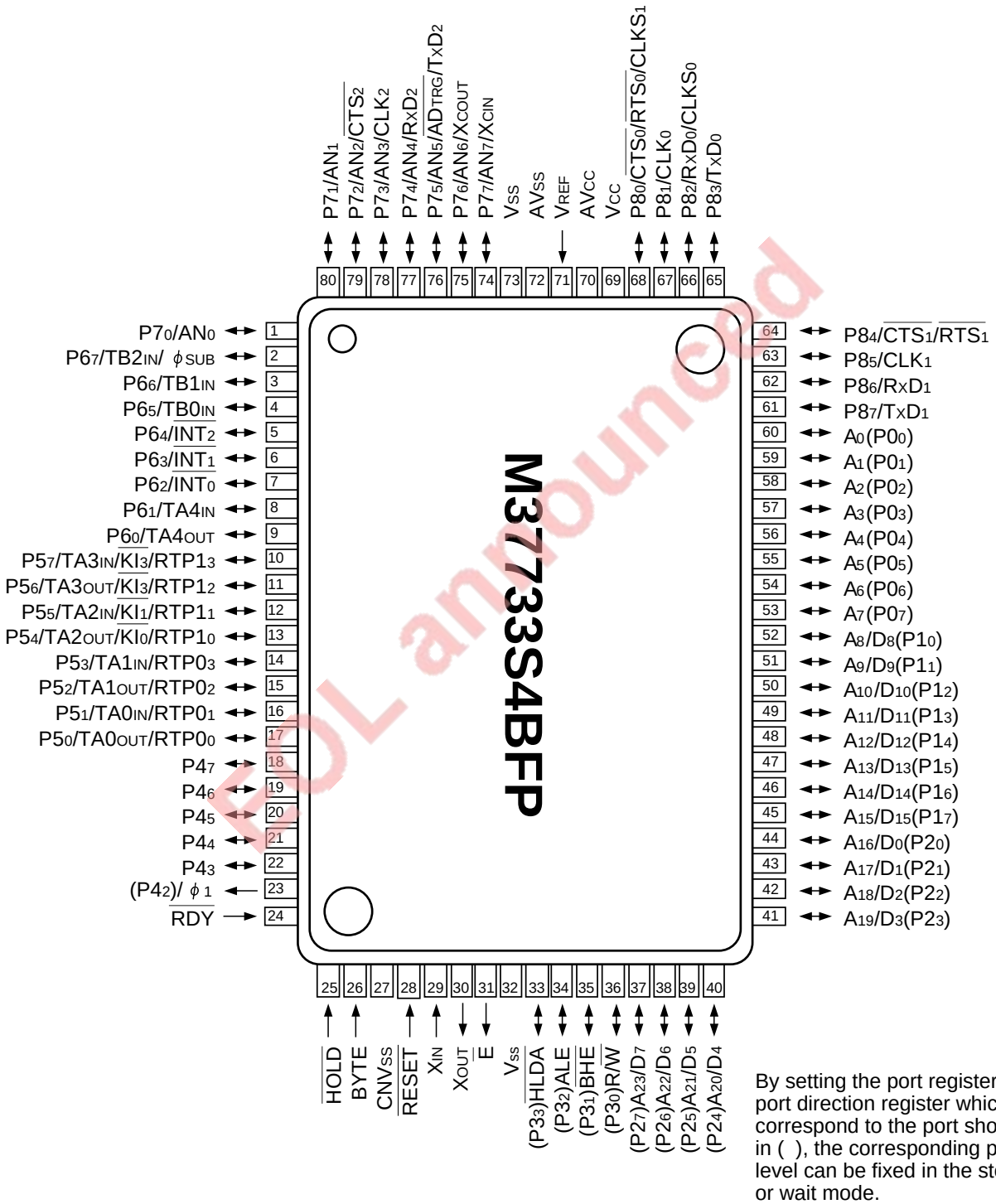

Fig. 20.2.1 M37733S4BFP pin configuration (Top view)

20.3 Pin description

Tables 20.3.1 and 20.3.2 list the pin description.

Table 20.3.1 Pin description (1)

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source input		To pin Vcc, apply 5 V±10% (When the main clock is the system clock) or 2.7 V to 5.5 V (When the sub-clock is the system clock). To pin Vss, apply 0 V.
CNVss	CNVss	Input	Connect to pin Vcc.
$\overline{\text{RESET}}$	Reset input	Input	The microcomputer is reset when "L" level is input to this pin.
XIN	Clock input	Input	Pins XIN and XOUT are the I/O pins of the clock generating circuit, respectively. Connect these pins via a ceramic resonator or a quartz-crystal oscillator. When an external clock is used, the clock should be input to pin XIN, and pin XOUT should be left open.
XOUT	Clock output	Output	
$\overline{E}$	Enable output	Output	This pin outputs signal $\overline{E}$. When $\overline{E}$'s level is "L," the microcomputer reads data and instruction codes or writes data. Also, output of signal $\overline{E}$ can be stopped by software.
BYTE	External data bus width selection input	Input	Input level to this pin determines whether the external data bus has a 16-bit width or an 8-bit width. A 16-bit width is selected when the level is "L," and an 8-bit width is selected when the level is "H."
AVcc	Analog power source input		Power source input for the A-D converter. Connect to pin Vcc.
AVss			Power source input for the A-D converter. Connect to pin Vss.
VREF	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
A0 (P00)–A7 (P07)	Address (low order) output	Output	Address's low-order 8 bits (A0–A7) are output.
A8/D8 (P10)–A15/D15 (P17)	Address (middle order) output/Data (high order) I/O	I/O	● When the external data bus width = 8 bits (Pin BYTE is at "H" level) Address's middle-order 8 bits (A8–A15) are output. ● When the external bus width = 16 bits (Pin BYTE is at "L" level) Input/Output of data (D8–D15) and output of address's middle-order 8 bits (A8–A15) are performed with the time sharing method.
A16/D0 (P20)–A23/D7 (P27)	Address (high order) output/Data (low-order) I/O	I/O	Input/Output of data (D0–D7) and output of address's high-order 8 bits (A16–A23) are performed with the time sharing method.

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EXTERNAL ROM VERSION

20.3 Pin description

Table 20.3.2 Pin description (2)

Pin	Name	Input/Output	Functions
R/$\overline{W}$ ($P3_0$), $\overline{BHE}$ ($P3_1$), ALE ($P3_2$), $\overline{HLDA}$ ($P3_3$)	Read write output, Byte high enable output, Address latch enable output, Hold acknowledge output	Output	These pins respectively output signals R/$\overline{W}$, $\overline{BHE}$, ALE, and $\overline{HLDA}$. ● Signal R/$\overline{W}$ This signal indicates the data bus state. When this signal level is "H," a data bus is in the read state. When this signal level is "L," a data bus is in the write state. ● Signal $\overline{BHE}$ This signal's level is "L" when the microcomputer accesses an odd address. ● Signal ALE This signal is used to separate the multiplexed signal which consists of an address and data to the address and the data. ● Signal $\overline{HLDA}$ This signal informs the external whether the microcomputer enters the Hold state or not. In Hold state, pin $\overline{HLDA}$ outputs "L" level.
$\overline{HOLD}$, $\overline{RDY}$, ϕ_1($P4_2$), $P4_3$–$P4_7$	Hold request, Ready, Clock output, I/O port P4	Input Input Output I/O	The microcomputer is in Hold state while pin $\overline{HOLD}$'s input level is "L" and is in Ready state while pin $\overline{RDY}$'s input level is "L." Clock ϕ_1 is output from pin ϕ_1. $P4_3$–$P4_7$ function as I/O ports with the same functions as port P5.
$P5_0$–$P5_7$	I/O port P5	I/O	P5 is a CMOS 8-bit I/O port and has an I/O direction register. Each pin can be programmed as an input port or an output port. And it can be programmed as I/O pins for timers A0–A3 and input pins (KI_0–KI_3) for the key input interrupt.
$P6_0$–$P6_7$	I/O port P6	I/O	P6 is an 8-bit I/O port with the same function as port P5 and can be programmed as I/O pins for timer A4, external interrupt input pins, and input pins for timers B0–B2. $P6_7$ also functions as an output pin for the sub clock (ϕSUB).
$P7_0$–$P7_7$	I/O port P7	I/O	P7 is an 8-bit I/O port with the same function as port P5 and can be programmed as analog input pins for the A-D converter. $P7_6$ and $P7_7$ can be programmed as I/O pins (XCOUT, XCIN) for the sub-clock (32 kHz) oscillation circuit. When using $P7_6$ and $P7_7$ as pins XCOUT and XCIN, connect a quartz-crystal oscillator between them. $P7_2$–$P7_5$ also function as UART2's I/O pins.
$P8_0$–$P8_7$	I/O port P8	I/O	P8 is an 8-bit I/O port with the same function as port P5 and can be programmed as serial I/O's I/O pins.

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20.4 Block description

Figure 20.4.1 shows the M37733S4BFP block diagram.

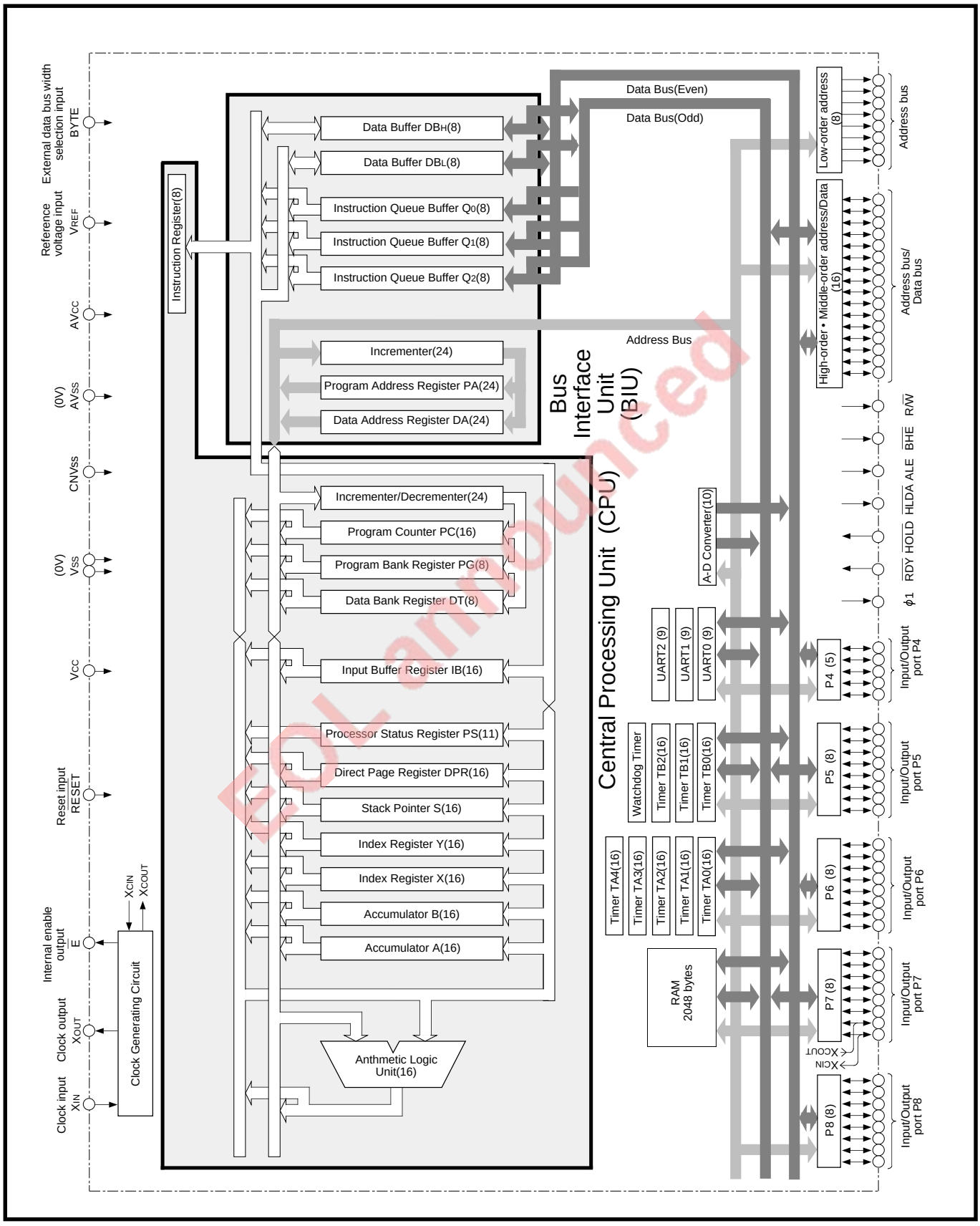

Fig.20.4.1 M37733S4BFP block diagram

20.5 Memory allocation

The internal area's memory allocation is described below. For details, refer to section **"2.4 Memory allocation."** For the external area, refer to section **"20.6 Processor modes."** Figure 20.5.1 shows the M37733S4BFP's memory map and Figure 20.5.2 shows the SFR area's memory map.

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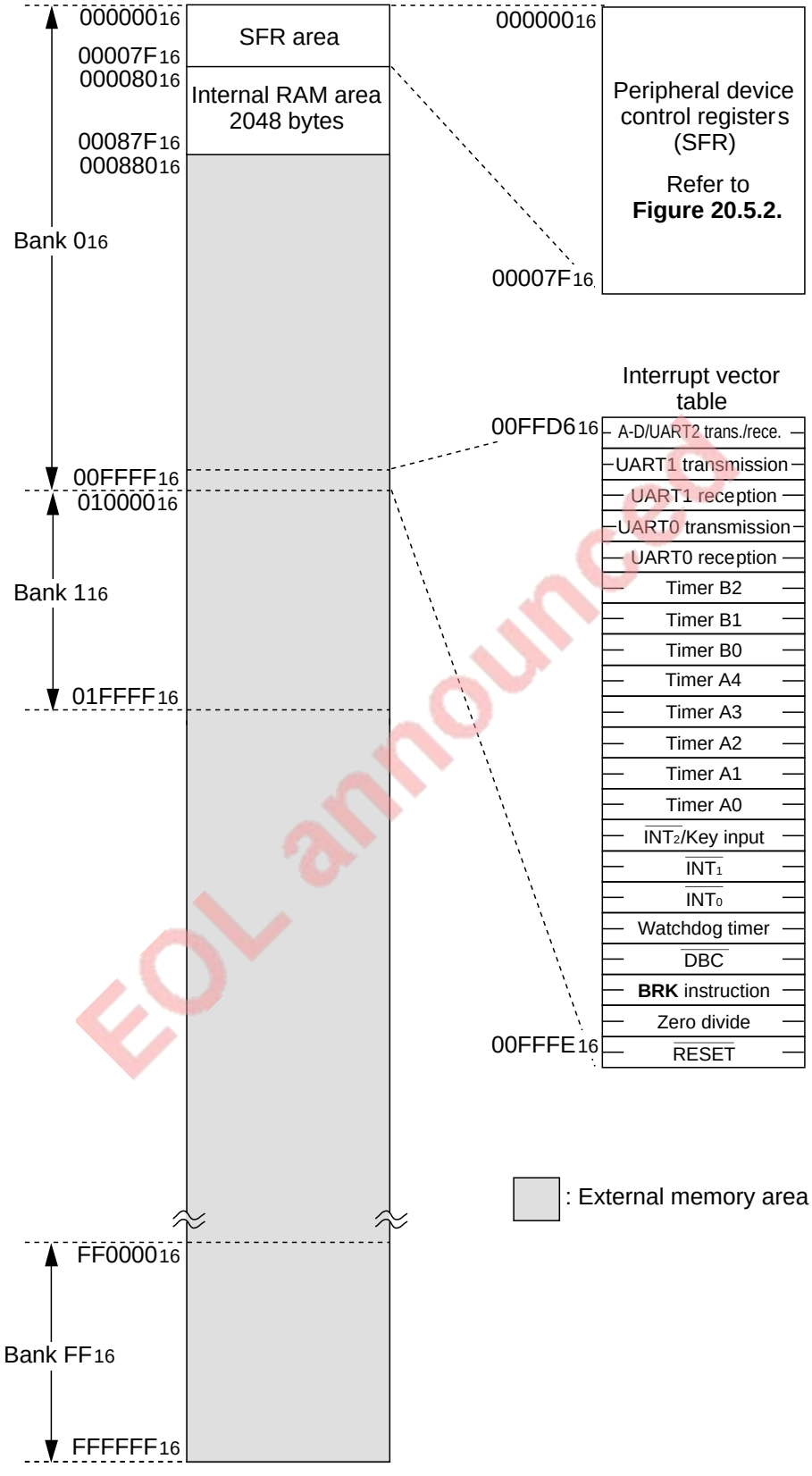

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❋ For the 7733 Group's microcomputers other than the M37733S4BFP, refer to section **"Appendix 1. 7733 Group memory allocation ."**

Fig. 20.5.1 M37733S4BFP's memory map

EXTERNAL ROM VERSION

20.5 Memory allocation

Address (Hexadecimal notation)	
000000	
000001	
000002	Port P0 register (**Note 3**)
000003	Port P1 register (**Note 3**)
000004	Port P0 direction register (**Note 3**)
000005	Port P1 direction register (**Note 3**)
000006	Port P2 register (**Note 3**)
000007	Port P3 register (**Note 3**)
000008	Port P2 direction register (**Note 3**)
000009	Port P3 direction register (**Note 3**)
00000A	Port P4 register (**Note 3**)
00000B	Port P5 register
00000C	Port P4 direction register (**Note 3**)
00000D	Port P5 direction register
00000E	Port P6 register
00000F	Port P7 register
000010	Port P6 direction register
000011	Port P7 direction register
000012	Port P8 register
000013	
000014	Port P8 direction register
000015	
000016	
000017	
000018	
000019	
00001A	
00001B	
00001C	Pulse output data register 1 (**Note 1**)
00001D	Pulse output data register 0 (**Note 1**)
00001E	A-D control register 0
00001F	A-D control register 1
000020	A-D register 0
000021	
000022	A-D register 1
000023	
000024	A-D register 2
000025	
000026	A-D register 3
000027	
000028	A-D register 4
000029	
00002A	A-D register 5
00002B	
00002C	A-D register 6
00002D	
00002E	A-D register 7
00002F	
000030	UART 0 transmit/receive mode register
000031	UART 0 baud rate register (BRG0)
000032	UART 0 transmission buffer register
000033	
000034	UART 0 transmit/receive control register 0
000035	UART 0 transmit/receive control register 1
000036	UART 0 receive buffer register
000037	
000038	UART 1 transmit/receive mode register
000039	UART 1 baud rate register (BRG1)
00003A	UART 1 transmission buffer register
00003B	
00003C	UART 1 transmit/receive control register 0
00003D	UART 1 transmit/receive control register 1
00003E	UART 1 receive buffer register
00003F	

Address (Hexadecimal notation)	
000040	Count start flag
000041	
000042	One-shot start flag
000043	
000044	Up-down flag
000045	
000046	Timer A0 register
000047	
000048	Timer A1 register
000049	
00004A	Timer A2 register
00004B	
00004C	Timer A3 register
00004D	
00004E	Timer A4 register
00004F	
000050	Timer B0 register
000051	
000052	Timer B1 register
000053	
000054	Timer B2 register
000055	
000056	Timer A0 mode register
000057	Timer A1 mode register
000058	Timer A2 mode register
000059	Timer A3 mode register
00005A	Timer A4 mode register
00005B	Timer B0 mode register
00005C	Timer B1 mode register
00005D	Timer B2 mode register
00005E	Processor mode register 0
00005F	Processor mode register 1
000060	Watchdog timer register
000061	Watchdog timer frequency selection flag
000062	Waveform output mode register (**Note 1**)
000063	Reserved area **(Notes 1, 2)**
000064	UART2 transmit/receive mode register
000065	UART2 baud rate register (BRG2)
000066	UART2 transmission buffer register
000067	
000068	UART2 transmit/receive control register 0
000069	UART2 transmit/receive control register 1
00006A	UART2 receive buffer register
00006B	
00006C	Oscillation circuit control register 0
00006D	Port function control register
00006E	Serial transmit control register
00006F	Oscillation circuit control register 1
000070	A-D/UART2 trans./rece. interrupt control register
000071	UART 0 transmission interrupt control register
000072	UART 0 receive interrupt control register
000073	UART 1 transmission interrupt control register
000074	UART 1 receive interrupt control register
000075	Timer A0 interrupt control register
000076	Timer A1 interrupt control register
000077	Timer A2 interrupt control register
000078	Timer A3 interrupt control register
000079	Timer A4 interrupt control register
00007A	Timer B0 interrupt control register
00007B	Timer B1 interrupt control register
00007C	Timer B2 interrupt control register
00007D	$\overline{INT_0}$ interrupt control register
00007E	$\overline{INT_1}$ interrupt control register
00007F	$\overline{INT_2}$/Key input interrupt control register

Notes 1: Memory map of the M37733S4BFP differs from that of the M37733MHBXXXFP in addresses $1C_{16}$, $1D_{16}$, 62_{16}, and 63_{16}.
2: Writing to the reserved area is disabled.
3: These registers are used when outputting an arbitrary data in the stop or wait mode.

EOL announced

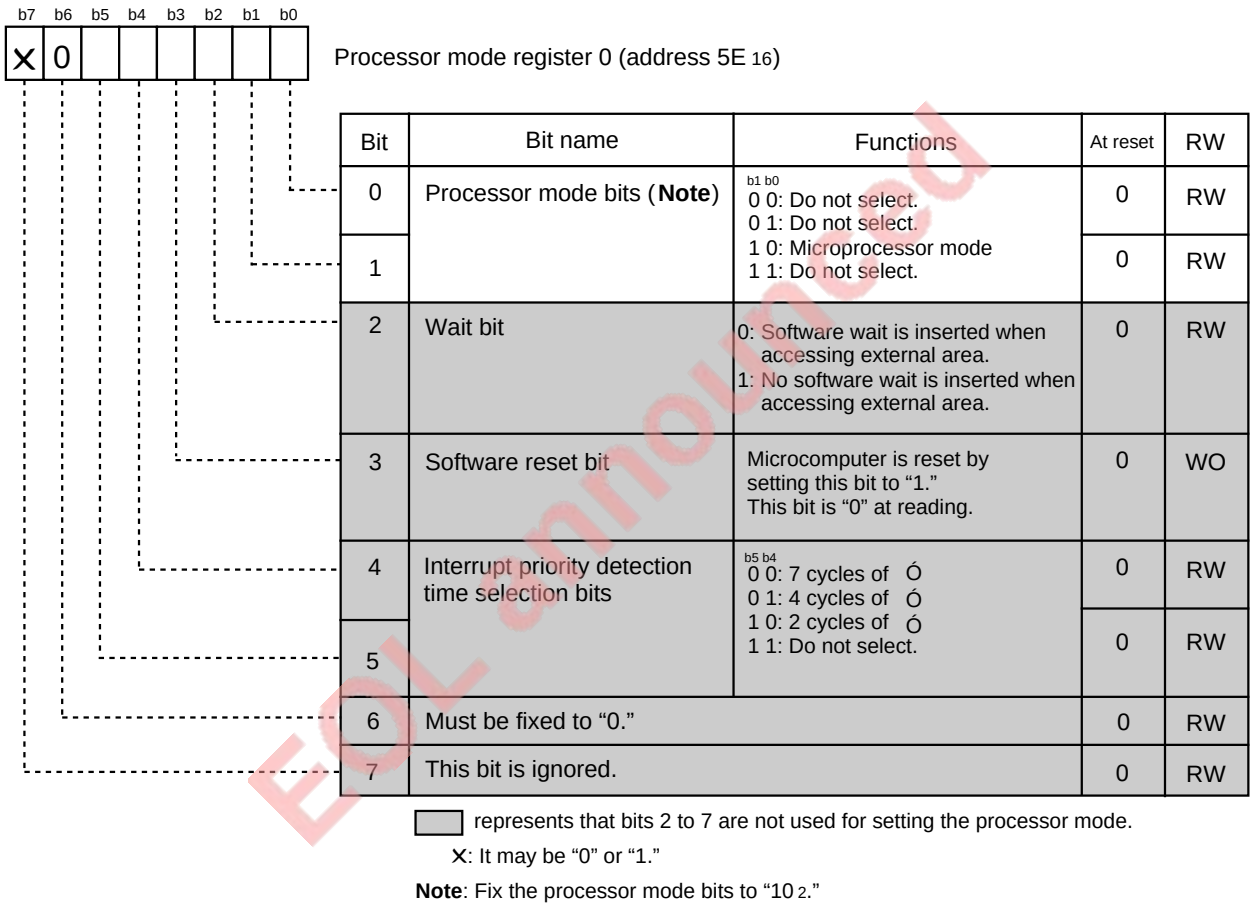
Fig. 20.5.2 SFR area's memory map

20.6 Processor modes

The M37733S4BFP can operate only in the microprocessor mode. For the processor mode, refer to the description of the microprocessor mode in section **"2.5 Processor modes."**
Also, be sure to set as follows:

- Connect pin CNVss to Vcc.
- Fix the processor mode bits to "10$_2$."

Figure 20.6.1 shows the structure of the processor mode register 0.



Bit	Bit name	Functions	At reset	RW
0	Processor mode bits (**Note**)	b1 b0 0 0: Do not select. 0 1: Do not select. 1 0: Microprocessor mode 1 1: Do not select.	0	RW
1			0	RW
2	Wait bit	0: Software wait is inserted when accessing external area. 1: No software wait is inserted when accessing external area.	0	RW
3	Software reset bit	Microcomputer is reset by setting this bit to "1." This bit is "0" at reading.	0	WO
4	Interrupt priority detection time selection bits	b5 b4 0 0: 7 cycles of Ó 0 1: 4 cycles of Ó 1 0: 2 cycles of Ó 1 1: Do not select.	0	RW
5			0	RW
6	Must be fixed to "0."		0	RW
7	This bit is ignored.		0	RW

represents that bits 2 to 7 are not used for setting the processor mode.
X: It may be "0" or "1."
Note: Fix the processor mode bits to "10 2."

EOL announced

Fig. 20.6.1 Structure of processor mode register 0

20.7 Timer A

Timer A is used mainly for output to the external. It consists of five counters (Timers A0 to A4) each equipped with a 16-bit reload function. Timers A0 to A4 operate independently of each other.

20.7.1 Overview

In the external ROM version, timer A has five operating modes listed below. In operating modes ① to ④, the external ROM version operates the same as the mask ROM and PROM versions.
Operating mode ⑤ is described in this chapter.

① Timer mode
② Event counter mode
③ One shot pulse mode
④ Pulse width modulation (PWM) mode
⑤ Pulse output mode

] Refer to chapter **"6. TIMER A."**

EOL announced

20.7.2 Pulse output port mode

(1) Overview

In the pulse output mode, there are two types of pulse output port: RTP0 controlled by timer A0 and RTP1 controlled by timer A2.

When an underflow occurs in timer A0 or A2, the contents of the pulse output data register 0 or 1 is output from the corresponding pulse output pins.

Also, the pulse width can be modulated by timer A as follows: use timer A1 for RTP0 and use timer A3 for RTP1. In addition, RTP0 can reverse the polarity of the contents of the pulse output data register 0 by software and outputs it.

Table 20.7.1 lists the specifications of the pulse output mode.

Table 20.7.1 Specifications of pulse output port mode

Pulse output port	RTP0	RTP1
Control timer	Timer A0	Timer A2
Pulse output pins	$RTP0_0$–$RTP0_3$ (Ports $P5_0$–$P5_3$)	$RTP1_0$–$RTP1_3$ (Ports $P5_4$–$P5_7$)
Register where pulse data is set	Pulse output data register 0	Pulse output data register 1
Pulse width modulation	Possible (Timer A1 is used)	Possible (Timer A3 is used)
Output level reverse function	Available	Not available

EOL announced

20.7 Timer A

(2) Block description

Figure 20.7.1 shows the block diagram for the pulse output mode. Figures 20.7.3 to 20.7.6 show the structures of registers related to the pulse output port mode.

Also, Figure 20.7.2 shows the structure of the port P5 output control circuit.

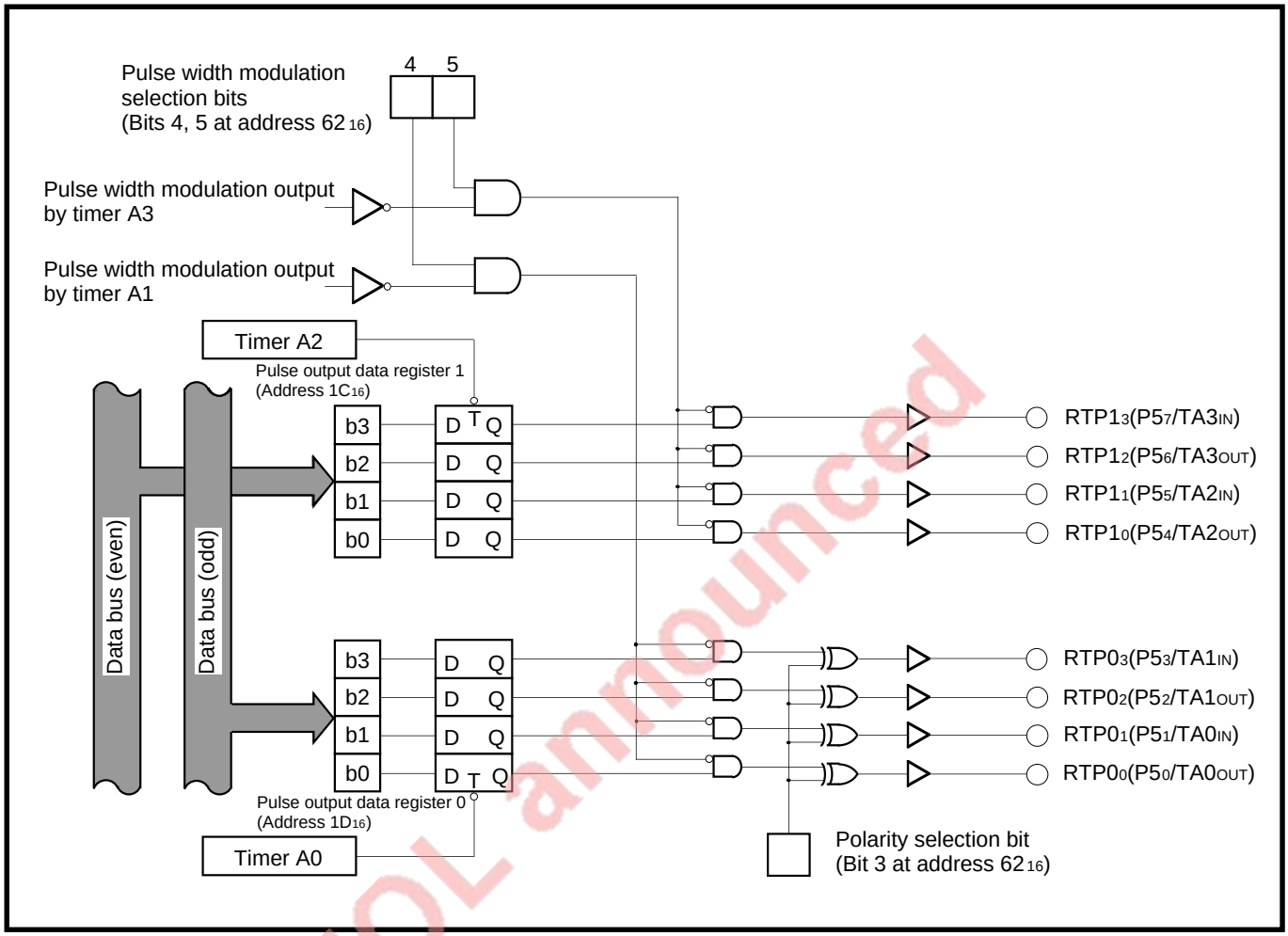
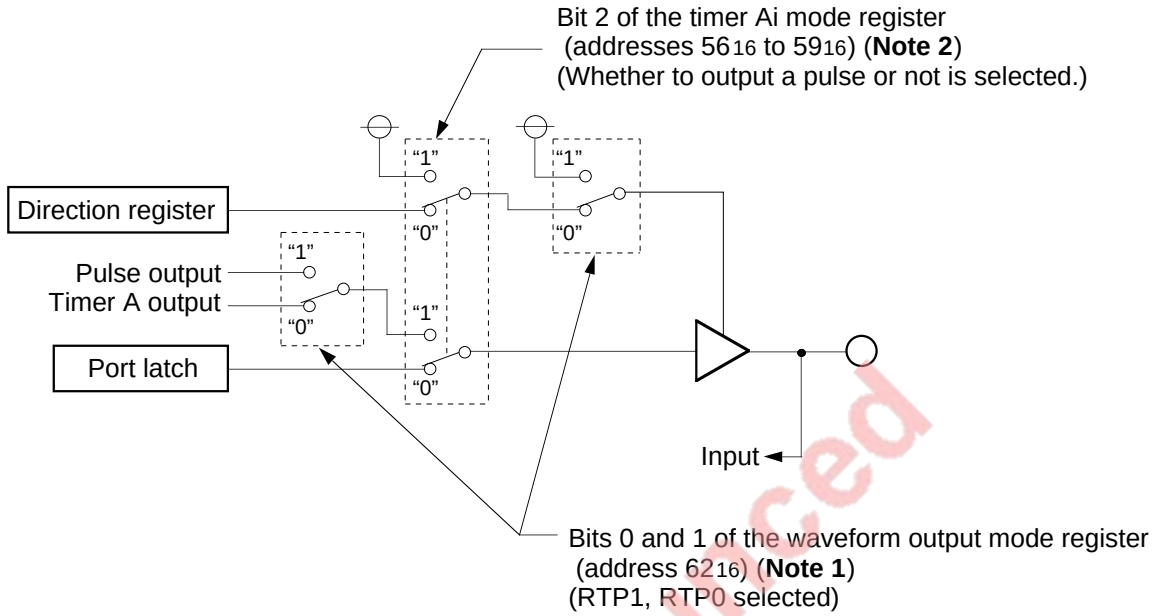


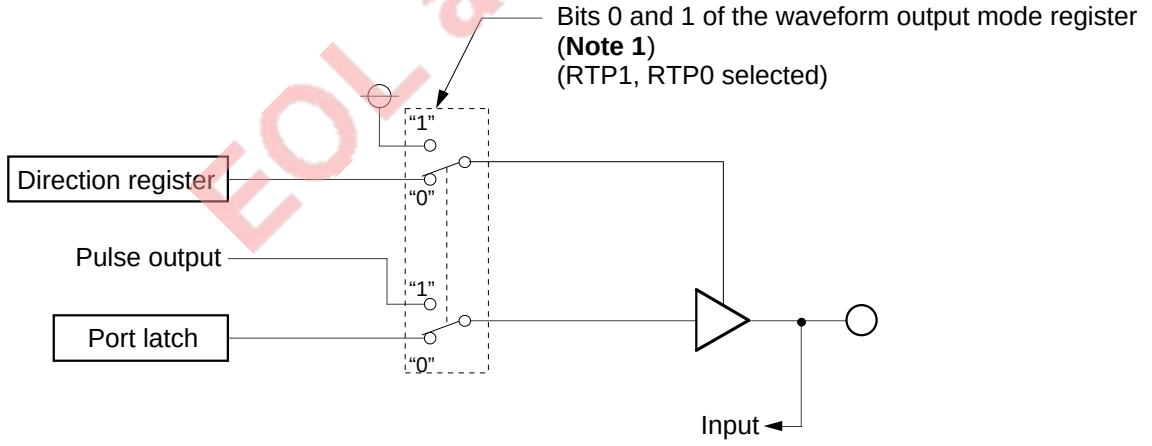
Fig. 20.7.1 Block diagram for pulse output port mode

EOL announced

● P5$_0$/TA0$_{OUT}$/RTP0$_0$, P5$_2$/TA1$_{OUT}$/RTP0$_2$, P5$_4$/TA2$_{OUT}$/RTP1$_0$, P5$_6$/TA3$_{OUT}$/RTP1$_2$



● P5$_1$/TA0$_{IN}$/RTP0$_1$, P5$_3$/TA1$_{IN}$/RTP0$_3$, P5$_5$/TA2$_{IN}$/RTP1$_1$, P5$_7$/TA3$_{IN}$/RTP1$_3$

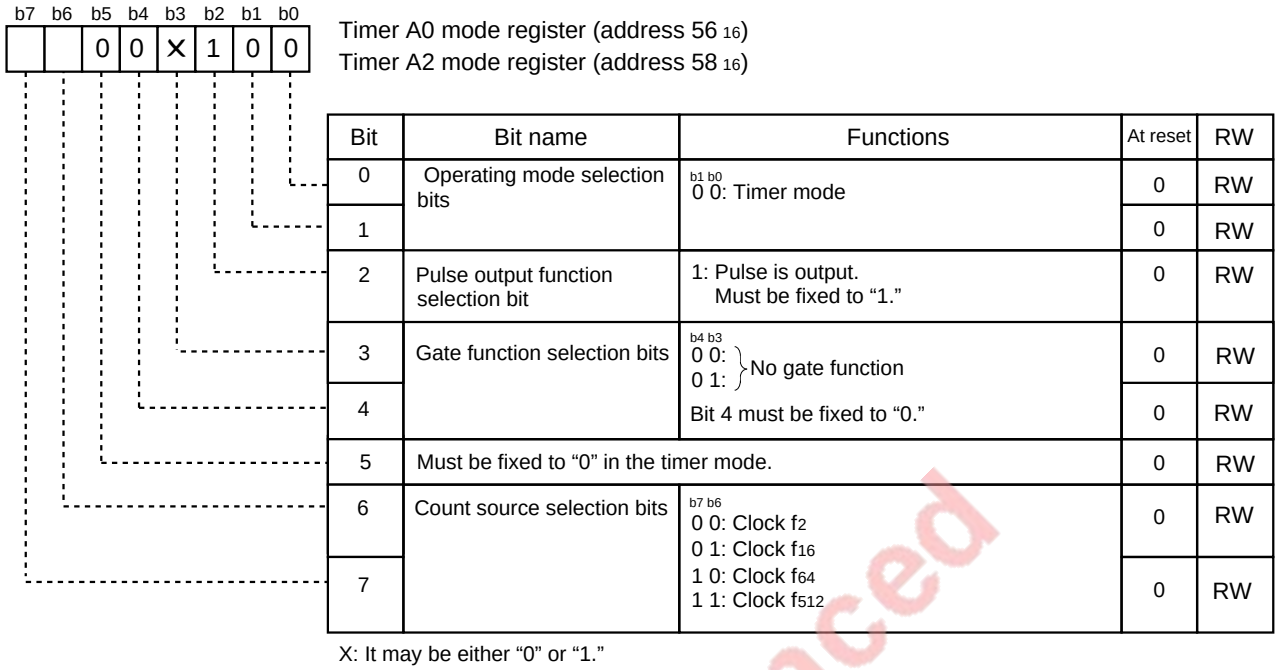


EOL announced

Notes 1: Ports P5$_0$ to P5$_3$ correspond to bit 1.
Ports P5$_4$ to P5$_7$ correspond to bit 0.
2: Bit 2 of the timer Ai mode register which corresponds to each port

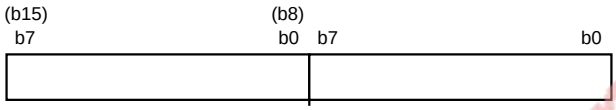
Fig. 20.7.2 Port P5 output control circuit

20.7 Timer A



Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode	0	RW
1			0	RW
2	Pulse output function selection bit	1: Pulse is output. Must be fixed to "1."	0	RW
3	Gate function selection bits	b4 b3 0 0: } No gate function 0 1: }	0	RW
4		Bit 4 must be fixed to "0."	0	RW
5	Must be fixed to "0" in the timer mode.		0	RW
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

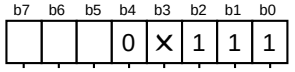
X: It may be either "0" or "1."



Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Undefined	RW

EOL announced

Fig. 20.7.3 Structures of timer A0, A2 mode registers and timer A0, A2 registers in pulse output port mode

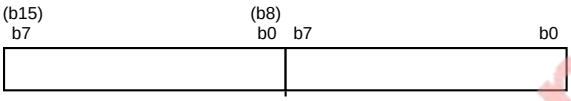


Timer A1 mode register (address 57 16)
Timer A3 mode register (address 59 16)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 1 1: PWM mode	0	RW
1			0	RW
2	Must be fixed to “1” in the PWM mode. (**Note**)		0	RW
3	Trigger selection bits (**Note**)	b4 b3 0 0: } Writing “1” to the count start flag 0 1: } (Pin TAiIN functions as a programmable I/O port.)	0	RW
4			0	RW
5	16/8-bit PWM mode selection bit	0: The counter operates as a 16-bit pulse width modulator. 1: The counter operates as an 8-bit pulse width modulator.	0	RW
6	Count source selection bits	b7 b6 0 0: Clock f2 0 1: Clock f16 1 0: Clock f64 1 1: Clock f512	0	RW
7			0	RW

Note: Fix bit 2 to “1” and bit 4 to “0” even when not using the pulse width modulation function.
X: It may be “0” or “1.”

■ When operating as a 16-bit pulse width modulator

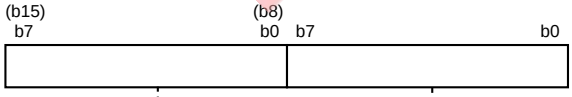


Timer A1 register (addresses 49 16, 4816)
Timer A3 register (addresses 4D 16, 4C16)

Bit	Functions	At reset	RW
15 to 0	Values 0000₁₆ to FFFE₁₆ can be set. Assuming that the set value = n, “H” level width of the PWM pulse which is output from pin TA1OUT or TA3OUT is n/fi.	Undefined	WO

fi: Frequency of the count source (f2, f16, f64, or f512)

■ When operating as an 8-bit pulse width modulator



Timer A1 register (addresses 49 16, 4816)
Timer A3 register (addresses 4D 16, 4C16)

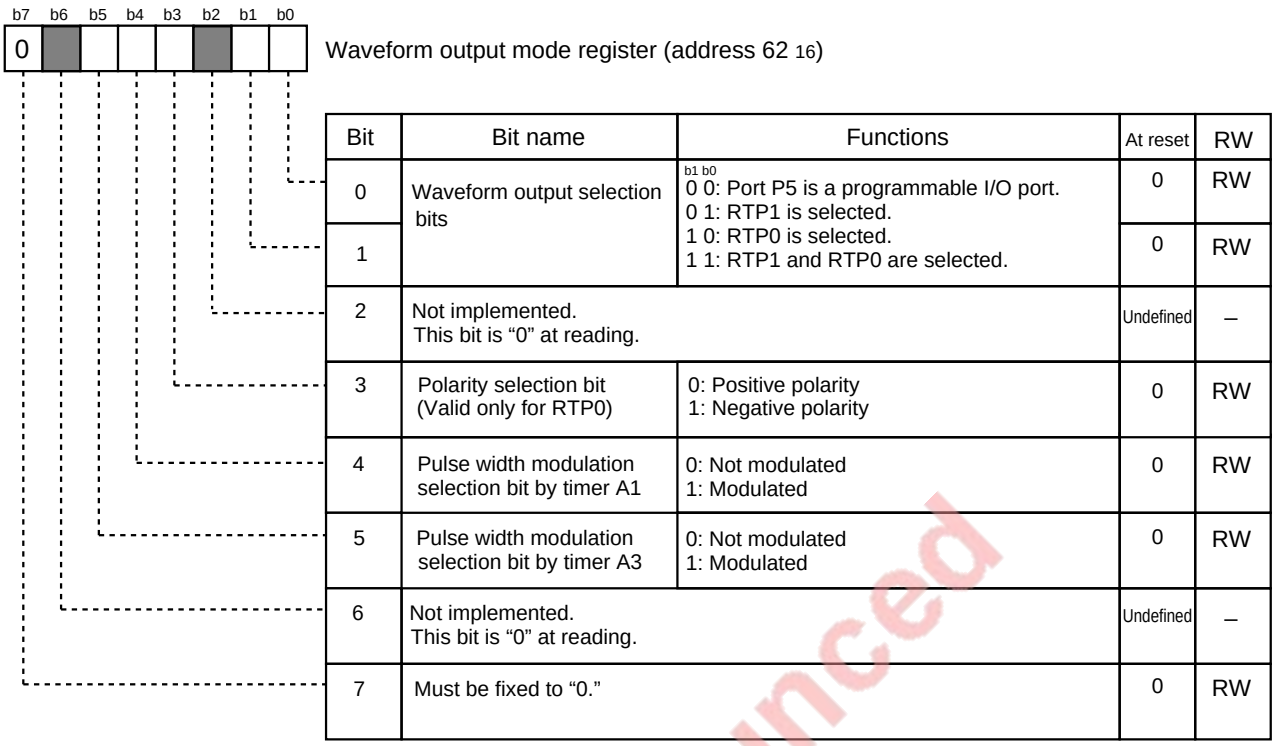
Bit	Functions	At reset	RW
7 to 0	Values 00₁₆ to FF₁₆ can be set. Assuming that the set value = m, period of the PWM pulse which is output from pin TA1OUT or TA3OUT is (m + 1)(2^8 – 1)/fi.	Undefined	WO
15 to 8	Values 00₁₆ to FE₁₆ can be set. Assuming that the set value = n, “H” level width of the PWM pulse which is output from pin TA1 OUT or TA3OUT is n(m +1)/fi.	Undefined	WO

fi: Frequency of the count source (f2, f16, f64, or f512)

EOL announced

Fig. 20.7.4 Structures of timer A1, A3 mode registers and timer A1, A3 registers in pulse output port mode (when pulse width modulation function is used)

20.7 Timer A



Bit	Bit name	Functions	At reset	RW
0	Waveform output selection bits	b1 b0 0 0: Port P5 is a programmable I/O port. 0 1: RTP1 is selected. 1 0: RTP0 is selected. 1 1: RTP1 and RTP0 are selected.	0	RW
1			0	RW
2	Not implemented. This bit is “0” at reading.		Undefined	–
3	Polarity selection bit (Valid only for RTP0)	0: Positive polarity 1: Negative polarity	0	RW
4	Pulse width modulation selection bit by timer A1	0: Not modulated 1: Modulated	0	RW
5	Pulse width modulation selection bit by timer A3	0: Not modulated 1: Modulated	0	RW
6	Not implemented. This bit is “0” at reading.		Undefined	–
7	Must be fixed to “0.”		0	RW

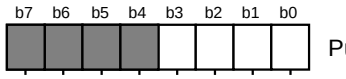
Fig. 20.7.5 Structures of waveform output mode register

EOL announced

Pulse output data register 1 (address 1C 16)

Bit	Bit name	Functions	At reset	RW
0	RTP10 output data bit	0: "L" level is output. 1: "H" level is output.	Undefined	WO
1	RTP11 output data bit		Undefined	WO
2	RTP12 output data bit		Undefined	WO
3	RTP13 output data bit		Undefined	WO
4 to 7	Not implemented.		Undefined	–

Note: Use the **LDM** and **STA** instructions to set bits 0 to 3.



Pulse output data register 1 (address 1D 16)

Bit	Bit name	Functions	At reset	RW
0	RTP00 output data bit	When the positive polarity is selected, 0: "L" level is output. 1: "H" level is output. When the negative polarity is selected, 0: "H" level is output. 1: "L" level is output.	Undefined	WO
1	RTP01 output data bit		Undefined	WO
2	RTP02 output data bit		Undefined	WO
3	RTP03 output data bit		Undefined	WO
4 to 7	Not implemented.		Undefined	–

Note: Use the **LDM** and **STA** instructions to set bits 0 to 3.

Fig. 20.7.6 Structures of pulse output data registers 0, 1

EOL announced

20.7 Timer A

(3) Initial setting example for registers related to pulse output port mode

Figures 20.7.7 to 20.7.9 show an initial setting example for registers related to the pulse output port mode.

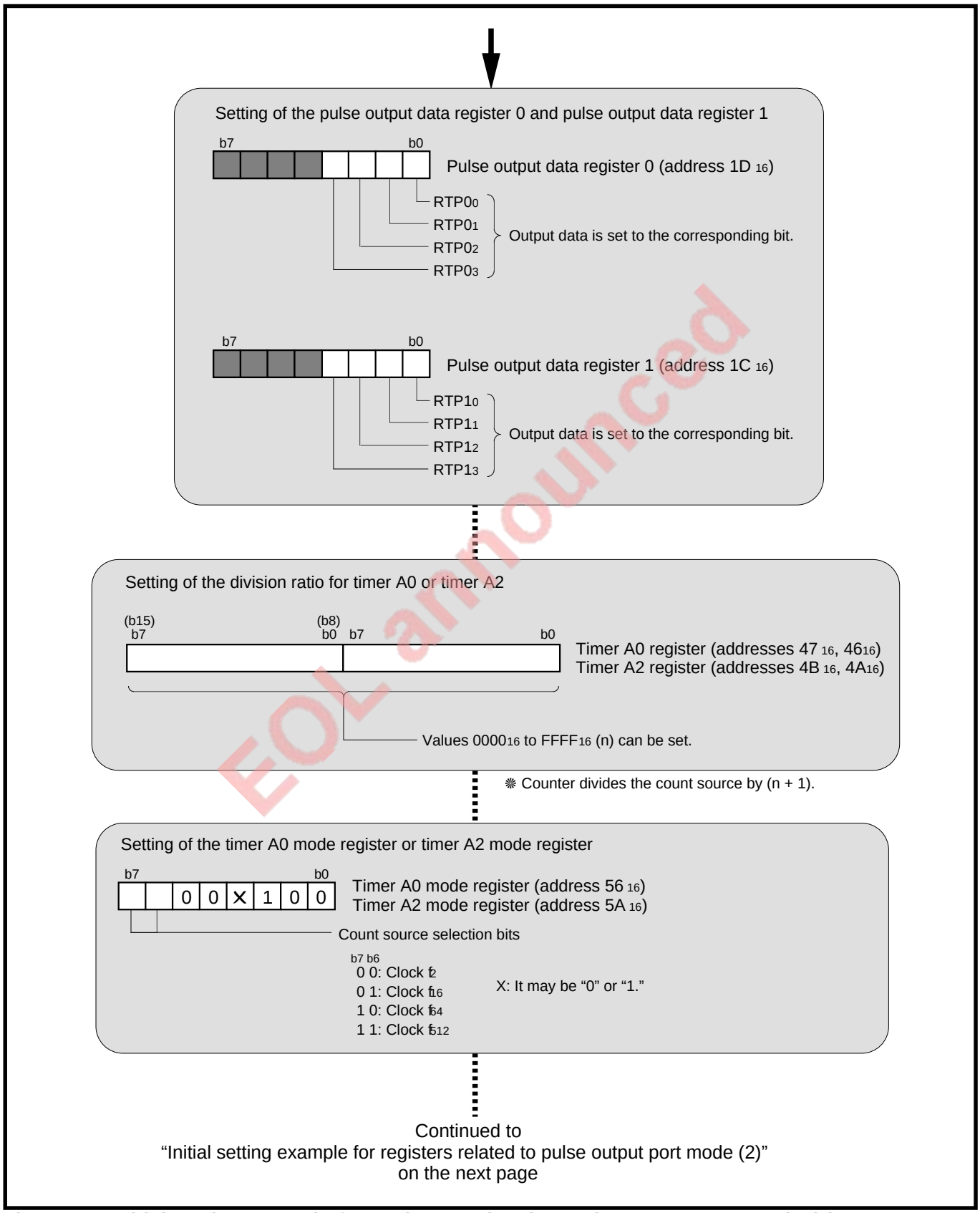
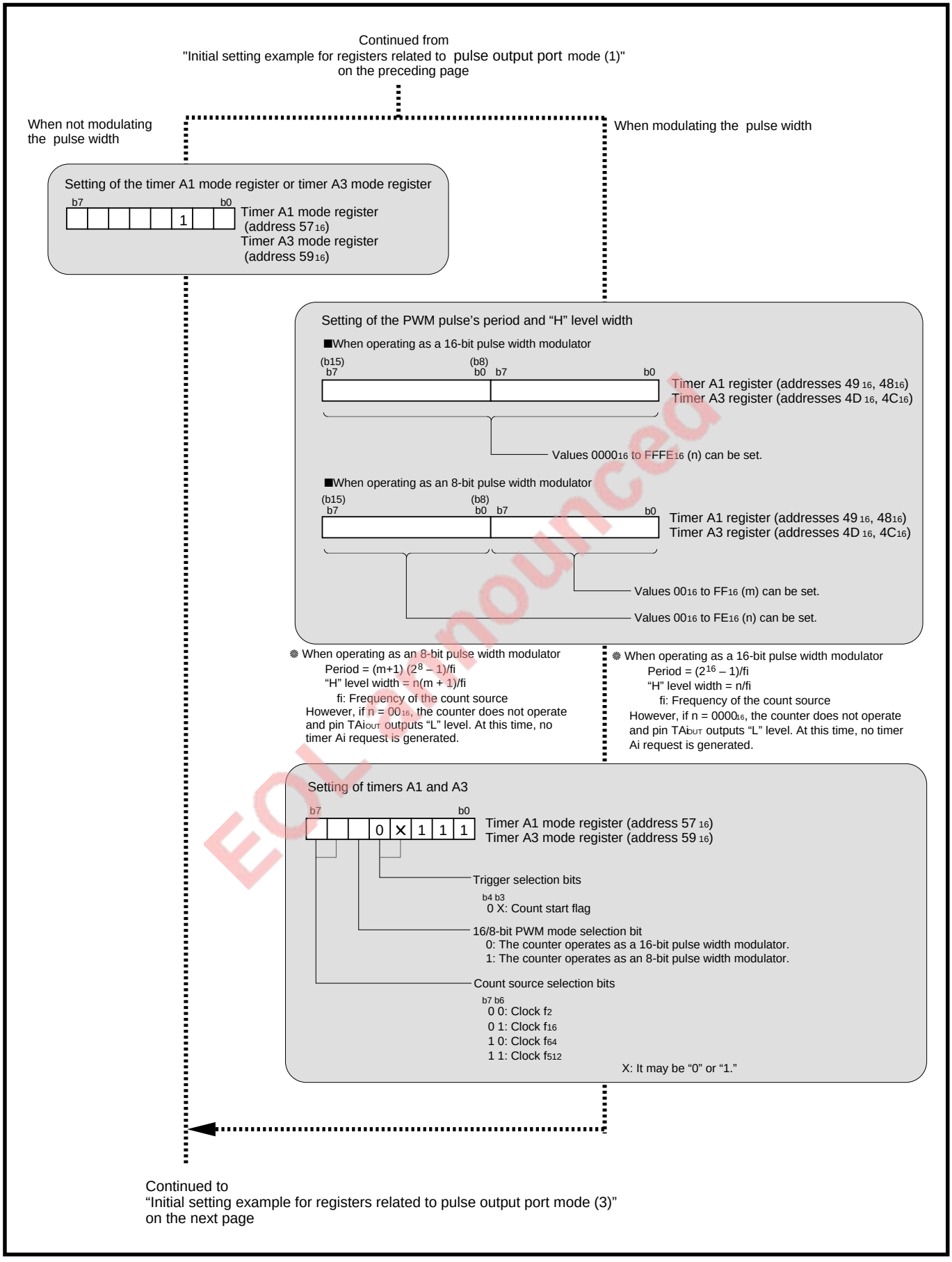


Fig. 20.7.7 Initial setting example for registers related to pulse output port mode (1)

EOL announced



EOL announced

Fig. 20.7.8 Initial setting example for registers related to pulse output port mode (2)

20.7 Timer A

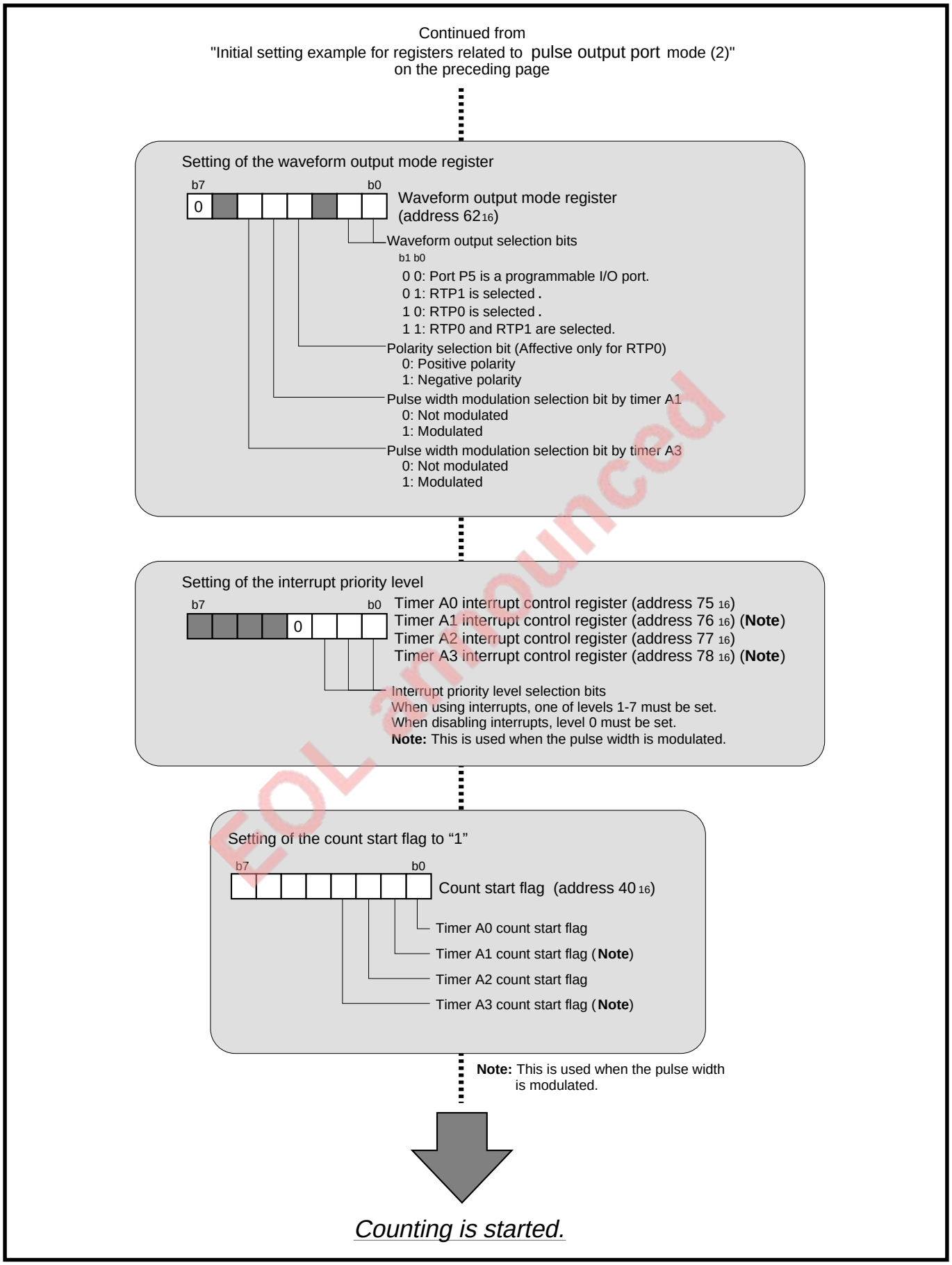


Fig. 20.7.9 Initial setting example for registers related to pulse output port mode (3)

EOL announced

(4) Operation in pulse output port mode

The RTP0 operation when the pulse width is not modulated and the output level reverse function is not used is described below.

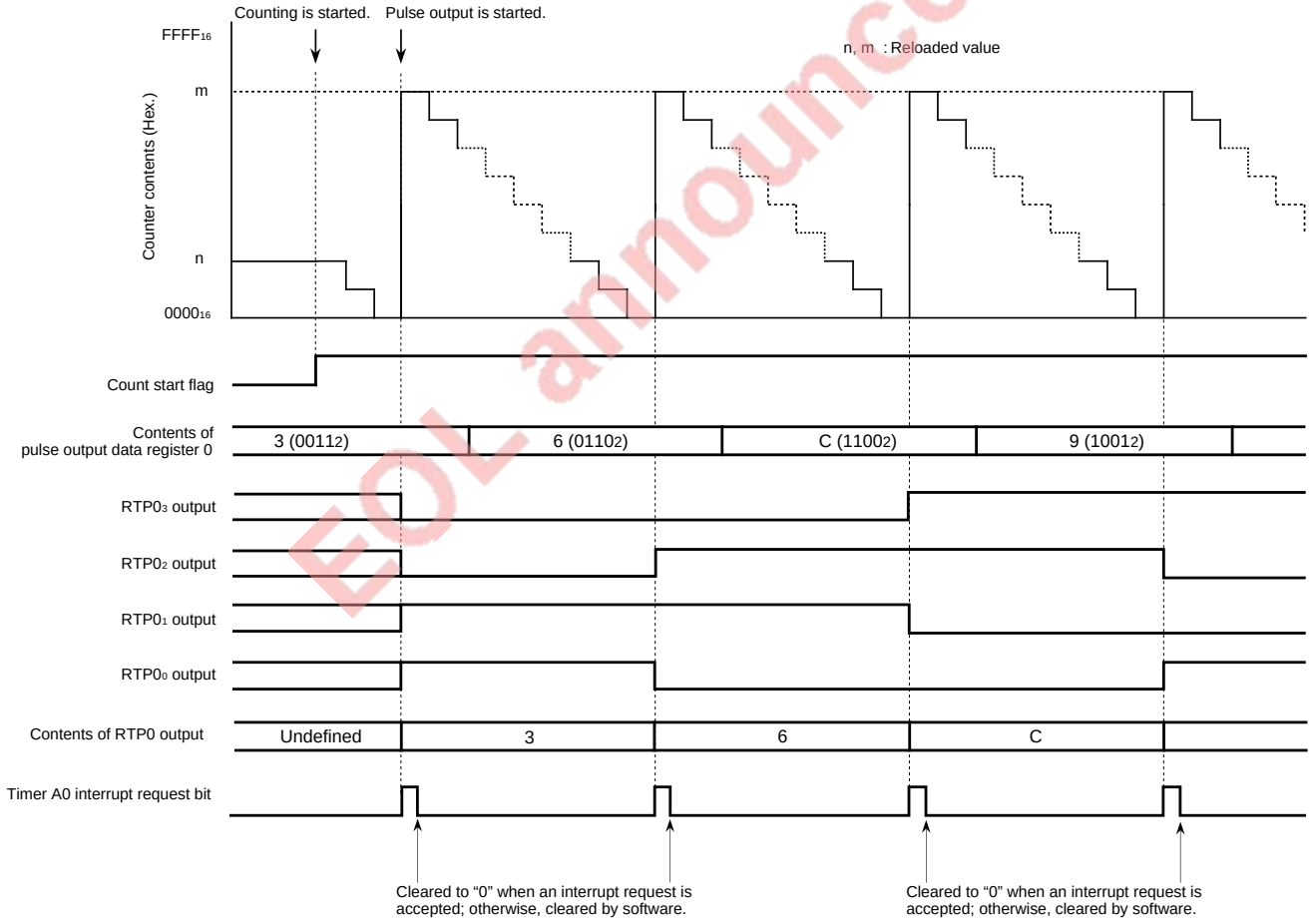
Note: Description in ( ) is applied to the RTP1 operation.

① When the count start flag of timer A0 (A2) is set to “1,” the counter starts counting of the count source.

② When an underflow occurs, data is output from each bit of RTP0 (RTP1) according to the setting of each bit of the pulse output data register 0 (1). This data is retained until the next underflow occurs. Timer A0 (A2) reloads the contents of the reload register and continues counting.

③ When the underflow occurs in ②, the timer A0 (A2) interrupt request bit is set to “1.” Then, the interrupt request bit remains set to “1” until the interrupt request is accepted or the interrupt request bit is cleared to “0” by software.

Figure 20.7.10 shows an operation example of the pulse output port mode.



EOL announced

Note: The output level of the pulse output port is undefined from when the pulse output port mode is set until the first timer underflow occurs. Also, this output level is at a floating state after reset because the pulse output port becomes the input port at that time.
In the above example, in order to shorten this undefined period, the following procedure is performed:
- A small value (n) is set to the timer counter as the initial value.
- After the first underflow occurs, the normal value (m) is set to the timer counter.

Fig. 20.7.10 Operation example of pulse output port mode

20.7 Timer A

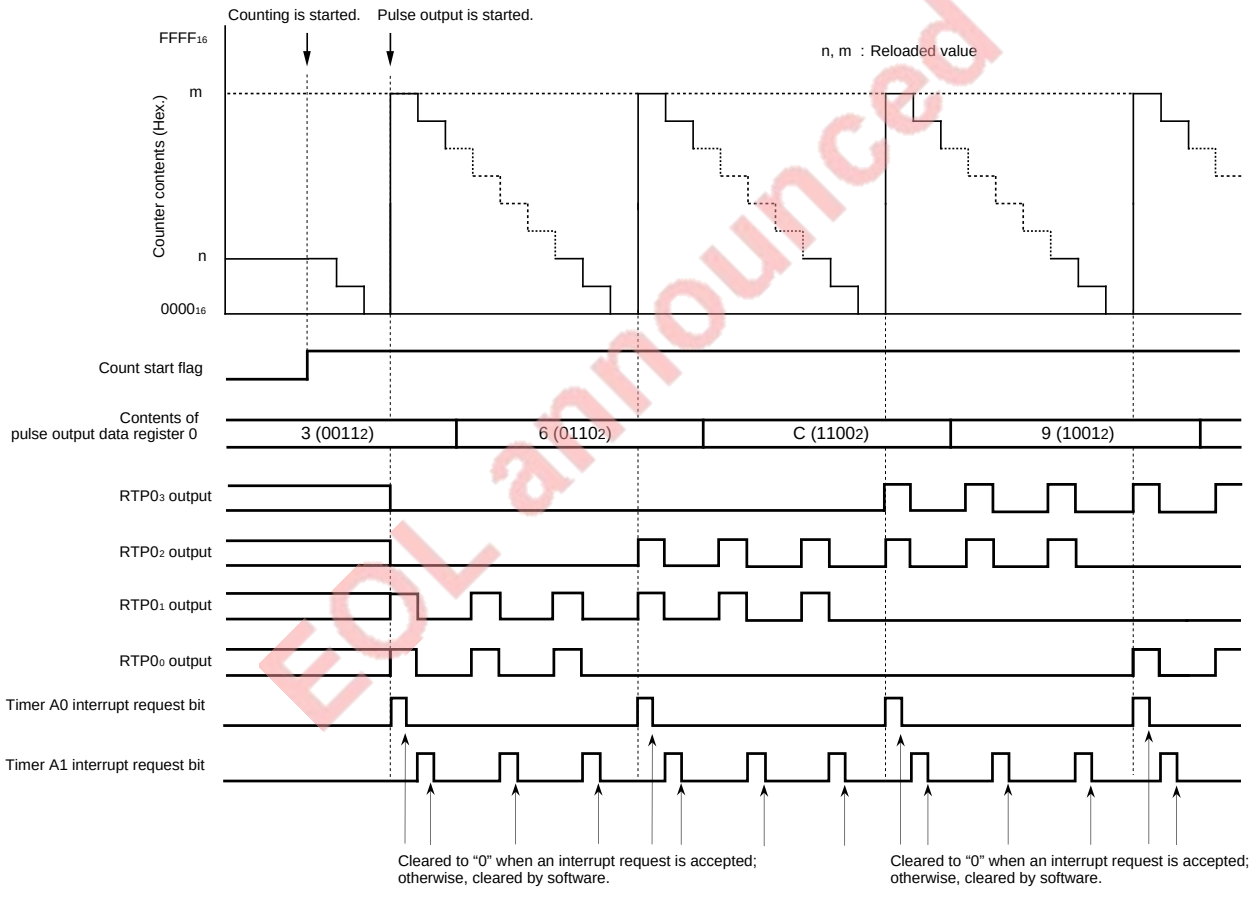
(5) Selectable functions

The pulse width modulation function and the RTP0 output level reverse function are described below.

● Pulse width modulation function

The RTP0 operation when the positive polarity is selected is described below.
Note: Description in ( ) is applied to the RTP1 operation.

When "the pulse width modulation selection bit by timer A1(A3)" [bit 4(5)) at address 62_{16}] is set to "1," "modulated" (Refer to **Figure 20.7.5.**) is selected. The pulse width modulation is performed while pins $RTP0_0$ to $RTP0_3$ ($RTP1_0$ to $RTP1_3$) output "H" level. (Refer to section **"6.6 Pulse width modulation (PWM) mode"** and **Figure 20.7.4**.) Figure 20.7.11 shows an operation example when "modulated" is selected.



Note: The output level of the pulse output port is undefined from when the pulse output port mode is set until the first timer underflow occurs. Also, this output level is at a floating state after reset because the pulse output port becomes the input port at that time.
In the above example, in order to shorten this undefined period, the following procedure is performed:
• A small value (n) is set to the timer counter as the initial value.
• After the first underflow occurs, the normal value (m) is set to the timer counter.

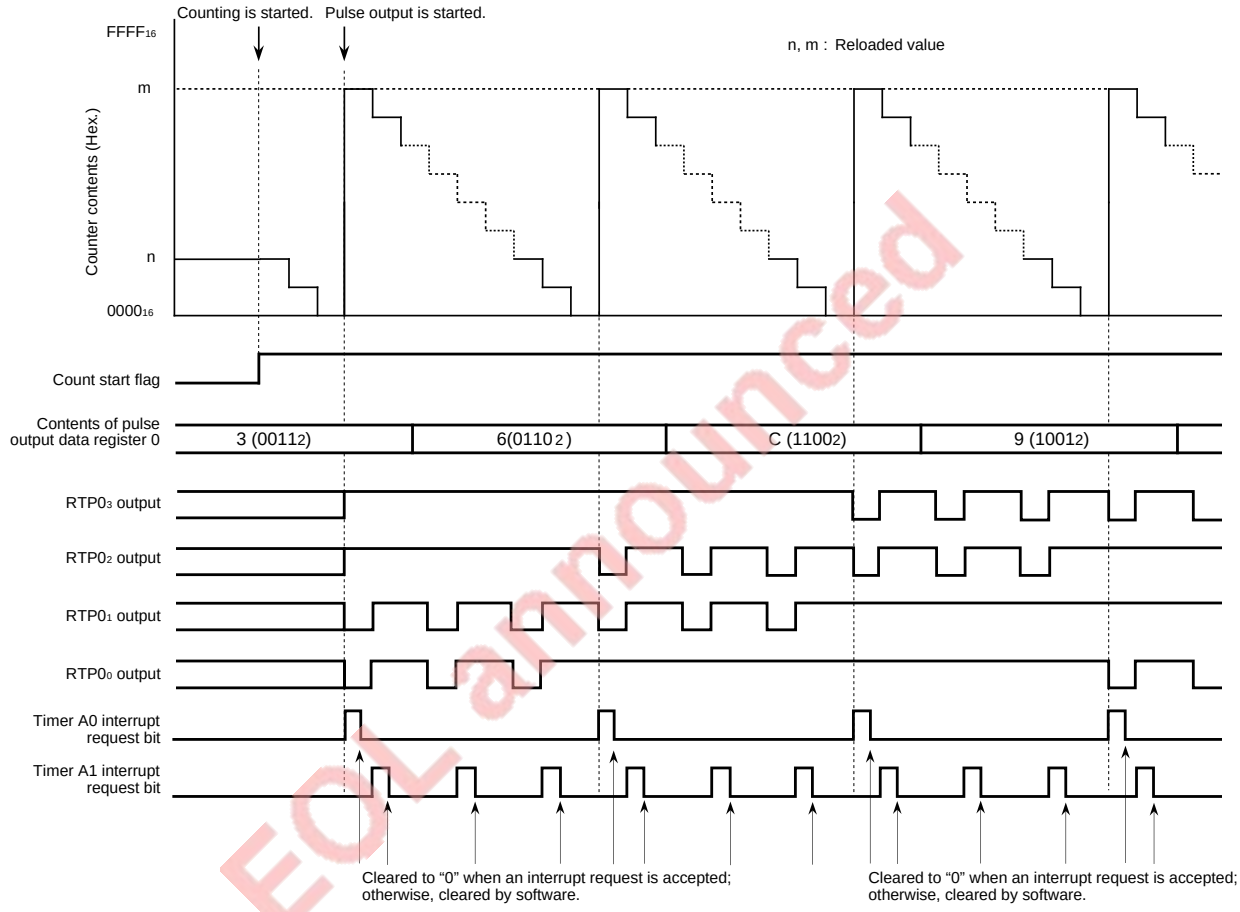
Fig. 20.7.11 Operation example when "modulated" is selected

EOL announced

● Output level reverse function (only for RTP0)

When the polarity selection bit (bit 3 at address 62_{16}) is set to "1," the output level can be reversed. In this case, when the $RTP0_0$ to $RTP0_3$ output data bits (bits 0 to 3 at address $1D_{16}$) are set to "0," pins $RTP0_0$ to $RTP0_3$ output "H" level; when these bits are set to "1," these pins output "L" level.

When the output level reverse function and "modulated" are selected, the pulse width modulation is performed while pins $RTP0_0$ to $RTP0_3$ output "L" level. Figure 20.7.12 shows an operation example when the output level is reversed with "modulated" selected.



Note: The output level of the pulse output port is undefined from when the pulse output port mode is set until the first timer underflow occurs. Also, this output level is at a floating state after reset because the pulse output port becomes the input port at that time.
In the above example, in order to shorten this undefined period, the following procedure is performed:
• A small value (n) is set to the timer counter as the initial value.
• After the first underflow occurs, the normal value (m) is set to the timer counter.

Fig. 20.7.12 Operation example when RTP0 output level reverse function and "modulated" are selected

EOL announced

[Precautions for pulse output port mode (pulse output function)]

1. In order to make ports $P5_0$ ($RTP0_0$), $P5_2$ ($RTP0_2$), $P5_4$ ($RTP1_0$), and $P5_6$ ($RTP1_2$) function as the pulse output pins, fix bit 2 of the timer A0 to A3 mode registers to "1."
   ● When using RTP0: Fix bit 2 of the timer A0 and A1 mode registers to "1."
   ● When using RTP1: Fix bit 2 of the timer A2 and A3 mode registers to "1."

2. When the pulse width modulation function is not used, timers A1 and A3 can be used as timers which do not have I/O pins. In this case, fix bit 2 of the timer A1 and A3 mode registers to "1." In addition, fix bits 0, 1, 4, and 5 of these registers to "0."

20.8 Reset

The reset description of the external ROM version differs from that of the mask ROM version in the state immediately after reset.

The state immediately after reset of the external ROM version differs from that of the mask ROM version in the following addresses: addresses $1C_{16}$, $1D_{16}$, 62_{16} and 63_{16}. Only the differences are described below. Figures 20.8.1 and 20.8.2 show the state of SFR area and internal RAM area immediately after reset (1) and (4). Figure 20.8.1 corresponds to Figure 13.1.3. Figure 20.8.2 corresponds to Figure 13.1.6. For the other descriptions, refer to chapter **"13. RESET."**

EOL announced

■SFR area (addresses 0_{16} to $7F_{16}$)

Abbreviations which represent access characteristics

RW : It is possible to read the bit state at reading. The written value becomes valid.
RO : It is possible to read the bit state at reading. The written value becomes invalid.
WO : The written value becomes valid. It is impossible to read the bit state.
▭ : Not implemented. It is impossible to read the bit state. The written value becomes invalid.

0 : "0" immediately after reset.
1 : "1" immediately after reset.
? : Undefined immediately after reset.

[0] : Always "0" at reading
[?] : Always undefined at reading
[0] : "0" immediately after reset. Must be fixed to "0."

Address	Register name	Access characteristics (b7 … b0)	State immediately after reset (b7 … b0)
0_{16}			?
1_{16}			?
2_{16}	Port P0 register	RW	?
3_{16}	Port P1 register	RW	?
4_{16}	Port P0 direction register	RW	00_{16}
5_{16}	Port P1 direction register	RW	00_{16}
6_{16}	Port P2 register	RW	?
7_{16}	Port P3 register	▭ ▭ ▭ ▭ RW	0 0 0 0 ?
8_{16}	Port P2 direction register	RW	00_{16}
9_{16}	Port P3 direction register	▭ ▭ ▭ ▭ RW	0 0 0 0 0 0 0 0
A_{16}	Port P4 register	RW	?
B_{16}	Port P5 register	RW	?
C_{16}	Port P4 direction register	RW	00_{16}
D_{16}	Port P5 direction register	RW	00_{16}
E_{16}	Port P6 register	RW	?
F_{16}	Port P7 register	RW	?
10_{16}	Port P6 direction register	RW	00_{16}
11_{16}	Port P7 direction register	RW	00_{16}
12_{16}	Port P8 register	RW	?
13_{16}			?
14_{16}	Port P8 direction register	RW	00_{16}
15_{16}			?
16_{16}			?
17_{16}			?
18_{16}			?
19_{16}			?
$1A_{16}$			?
$1B_{16}$			?
$1C_{16}$	Pulse output data register 1 ❋	▭ ▭ ▭ ▭ ▭ ▭ WO	?
$1D_{16}$	Pulse output data register 0 ❋	▭ ▭ ▭ ▭ ▭ ▭ WO	?
$1E_{16}$	A-D control register 0	RW	0 0 0 0 0 ? ? ?
$1F_{16}$	A-D control register 1	▭ ▭ RW ▭ RW	? ? 0 0 0 ? 1 1

❋ The contents of addresses $1C_{16}$ and $1D_{16}$ of the M37733S4BFP differ from those of the M37733MHBXXXFP.

EOL announced

Fig. 20.8.1 State of SFR area and internal RAM area immediately after reset (1)

20.8 Reset

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
6016	Watchdog timer register	WO	? (✵1)
6116	Watchdog timer frequency selection flag	RW	? 0
6216	Waveform output mode register ✵3	RW RW RW	0 ? 0 0 0 ? 0 0
6316	(Reserved area) ✵4		?
6416	UART 2 transmit/receive mode register	RW	? 0 0 0 0 0 0 0
6516	UART 2 baud rate register (BRG2)	WO	?
6616	UART 2 transmission buffer register	WO	?
6716		WO	?
6816	UART 2 transmit/receive control register 0	RO RW	? 1 0 0 0
6916	UART 2 transmit/receive control register 1	RO RW RO RW	0 0 0 0 0 0 1 0
6A16	UART 2 receive buffer register	RO	?
6B16		RO	0 0 0 0 0 0 0 ?
6C16	Oscillation circuit control register 0	RW(✵2) RW	? 0 0 0 0 0 ? 1
6D16	Port function control register	RW	0 0 0 0 0 0 0 0
6E16	Serial transmit control register	RW	? 0 0 ?
6F16	Oscillation circuit control register 1	WO RW	0 ? 0 ✵3 0 0 0
7016	A-D / UART 2 trans./rece. interrupt control register	RW	? 0 0 0 0
7116	UART0 transmission interrupt control register	RW	? 0 0 0 0
7216	UART0 receive interrupt control register	RW	? 0 0 0 0
7316	UART1 transmission interrupt control register	RW	? 0 0 0 0
7416	UART1 receive interrupt control register	RW	? 0 0 0 0
7516	Timer A0 interrupt control register	RW	? 0 0 0 0
7616	Timer A1 interrupt control register	RW	? 0 0 0 0
7716	Timer A2 interrupt control register	RW	? 0 0 0 0
7816	Timer A3 interrupt control register	RW	? 0 0 0 0
7916	Timer A4 interrupt control register	RW	? 0 0 0 0
7A16	Timer B0 interrupt control register	RW	? 0 0 0 0
7B16	Timer B1 interrupt control register	RW	? 0 0 0 0
7C16	Timer B2 interrupt control register	RW	? 0 0 0 0
7D16	$\overline{INT_0}$ interrupt control register	RW	? 0 0 0 0 0 0
7E16	$\overline{INT_1}$ interrupt control register	RW	? 0 0 0 0 0 0
7F16	$\overline{INT_2}$/Key input interrupt control register	RW	? 0 0 0 0 0 0

Preliminary announced

✵**1** A value of "FFF16" is set to the watchdog timer. (Refer to Chapter **"10. WATCHDOG TIMER."**)
✵**2** For access characteristics at address 6C16, also refer to **Figure 14.3.2.**
✵**3** The contents of addresses 6216 and 6316 of the M37733S4BFP differ from those of the M37733MHBXXFP.
✵**4** Do not wirte to address 6316.

■Internal RAM area (M37733S4BFP: addresses 8016 to FFF16)

●At hardware reset
(not including the case where the stop or wait mode is terminated)...Undefined.
●At software reset...Retains the state immediately before reset.
●When the stop or wait mode is terminated
(when hardware reset is used)...Retains the state immediately before the **STP** or **WIT** instruction is executed.

Fig. 20.8.2 State of SFR area and internal RAM area immediately after reset (4)

20.9 Electrical characteristics

Except for "Icc," the electrical characteristics of the M37733S4BFP are the same as those of the M37733MHBXXXFP in the microprocessor mode. For the others, refer to chapter **"15. ELECTRICAL CHARACTERISTICS.")**

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	External bus is operating, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, f(X_{IN}) = 25 MHz (Square waveform), (f(f_2) = 12.5 MHz), f(X_{CIN}) = 32.768 kHz, in operating **(Note 1)**		11.4	22.8	mA
			Vcc = 5V, f(X_{IN}) = 25 MHz (Square waveform), (f(f_2) = 1.5625 MHz), f(X_{CIN}) : Stopped, in operating **(Note 1)**		1.6	3.2	mA
			Vcc = 5V, f(X_{IN}) = 25 MHz (Square waveform), f(X_{CIN}) = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		10	20	μA
			Vcc = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, in operating **(Note 3)**		60	120	μA
			Vcc = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		5	10	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop selection bit at wait state = "1."

3: This is applied when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

EOL announced

20.10 Low voltage version

Differences from the M37733S4BFP are mainly described below.

20.10.1 Performance overview

The performance overview of the low voltage version differs from that of the mask ROM version in the following: memory size and current consumption. For the other items, refer to section **"18.1 Performance overview."**

Table 20.10.1 shows the performance overview of the M37733S4LHP.

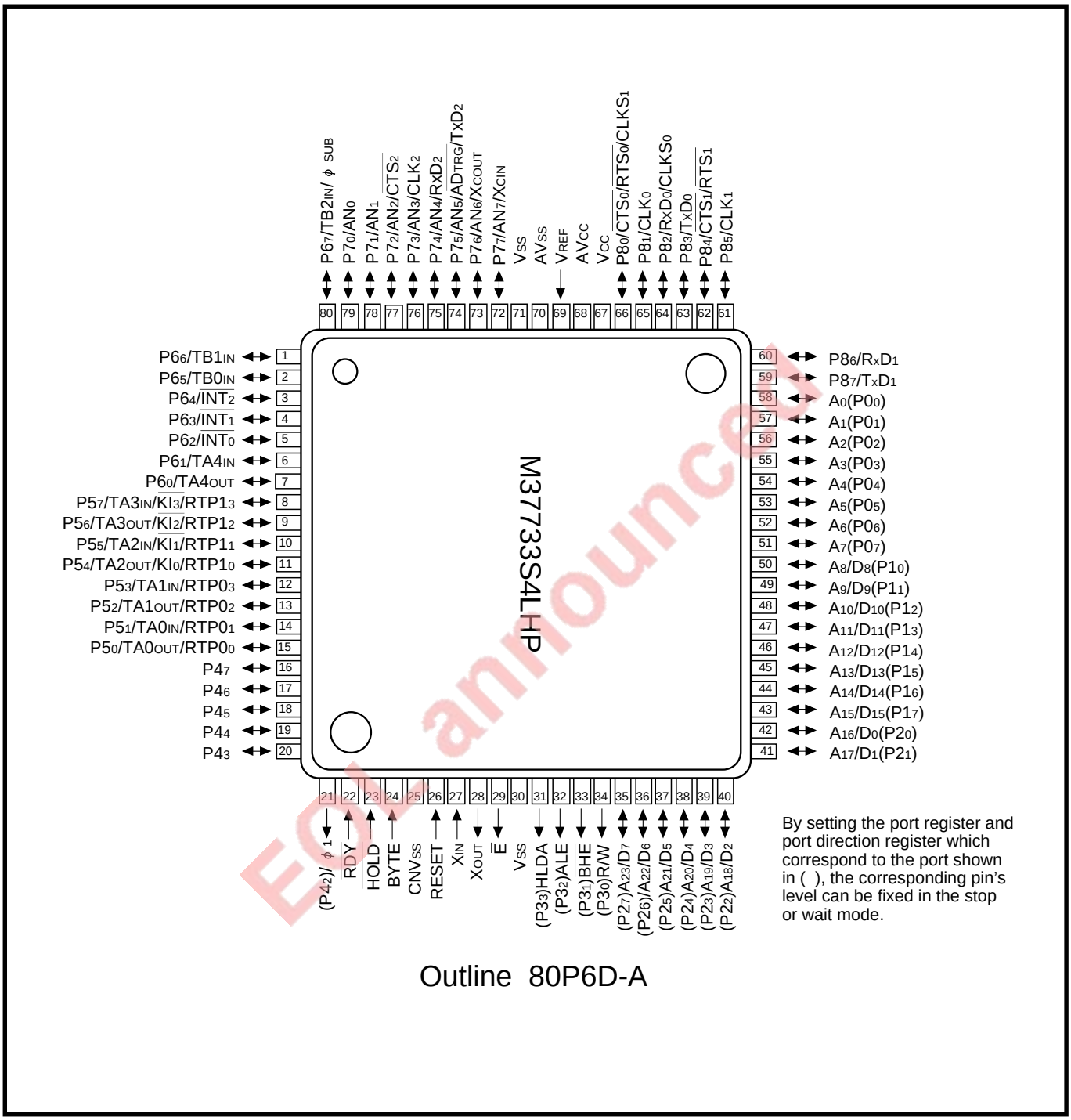
Table 20.10.1 M37733S4LHP's performance overview

Items		Performance
Memory size	RAM	2048 bytes
Current consumption		10.8 mW (When f(XIN) = 12-MHz external square wave input, Vcc = 3 V, and the main clock is the system clock, Typ.)
		120 μW (When f(XCIN) = 32 kHz, Vcc = 3 V, the sub clock is the system clock, and the main clock is stopped, Typ.)

EOL announced

20.10.2 Pin configuration

Figure 20.10.1 shows the M37733S4LHP pin configuration.



By setting the port register and port direction register which correspond to the port shown in ( ), the corresponding pin's level can be fixed in the stop or wait mode.

Outline 80P6D-A

Eol announced

Fig. 20.10.1 M37733S4LHP pin configuration (Top view)

EXTERNAL ROM VERSION

20.10 Low voltage version

20.10.3 Functional description

Except for the power-on reset conditions, the M37733S4LHP has the same functions as the M37733S4BFP. For the other functions, refer to chapters **"2. CENTRAL PROCESSING UNIT (CPU)"** to **"14. CLOCK GENERATING CIRCUIT."**

The power-on reset conditions of the M37733S4LHP are the same as those of the M37733MHLXXXHP. For details, refer to section **"18.3 Functional description"**.

20.10.4 Electrical characteristics

Except for "Icc," the electrical characteristics of the M37733S4LHP are the same as those of the M37733MHLXXXHP in the microprocessor mode. For the others, refer to section **"18.4 Electrical characteristics."**

ELECTRICAL CHARACTERISTICS (Vcc= 5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
Icc	Power source current	External bus is operating, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating **(Note 1)**		5.4	10.8	mA
			Vcc = 3 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating **(Note 1)**		3.6	7.2	mA
			Vcc = 3 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 0.75 MHz), $f(X_{CIN})$: Stopped, in operating **(Note 1)**		0.5	1.0	mA
			Vcc = 3 V, $f(X_{IN})$ = 12 MHz (Square waveform), $f(X_{CIN})$ = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		6	12	μA
			Vcc = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, in operating **(Note 3)**		40	80	μA
			Vcc = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		3	6	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

EOL announced

Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1."

3: This is applied when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

APPENDIX

Appendix 1. Memory allocation of 7733 Group
Appendix 2. Memory allocation in SFR area
Appendix 3. Control registers
Appendix 4. Package outlines
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Appendix 6. Machine instructions
Appendix 7. Examples of handling unused pins
Appendix 8. Countermeasure examples against noise
Appendix 9. Q & A

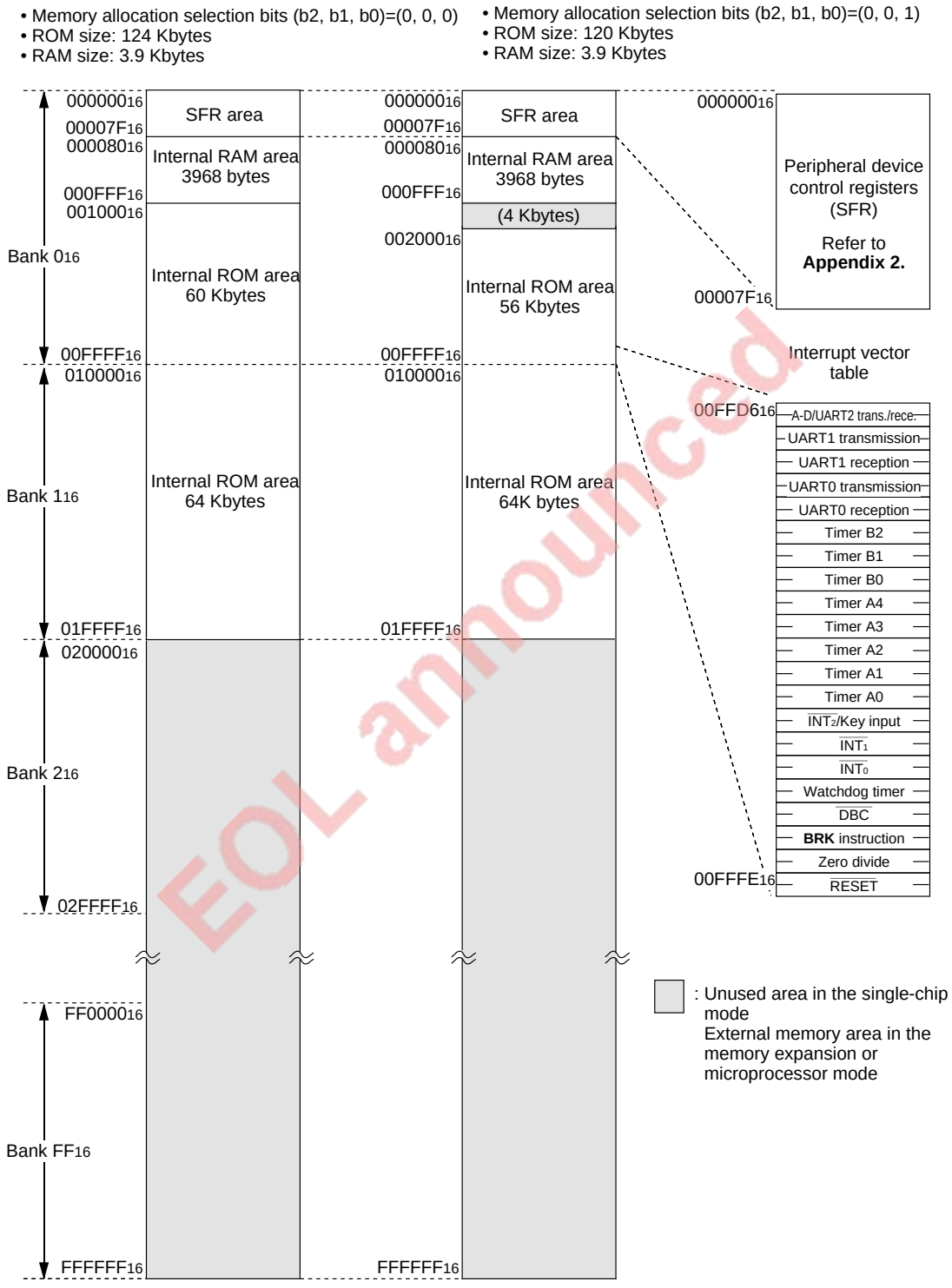
EOL announced

APPENDIX

Appendix 1. Memory allocation of 7733 Group

Appendix 1. Memory allocation of 7733 Group

1. M37733MHBXXXFP, M37733EHBXXXFP, M37733EHBFS, M37733MHLXXXHP, M37733EHLXXXHP



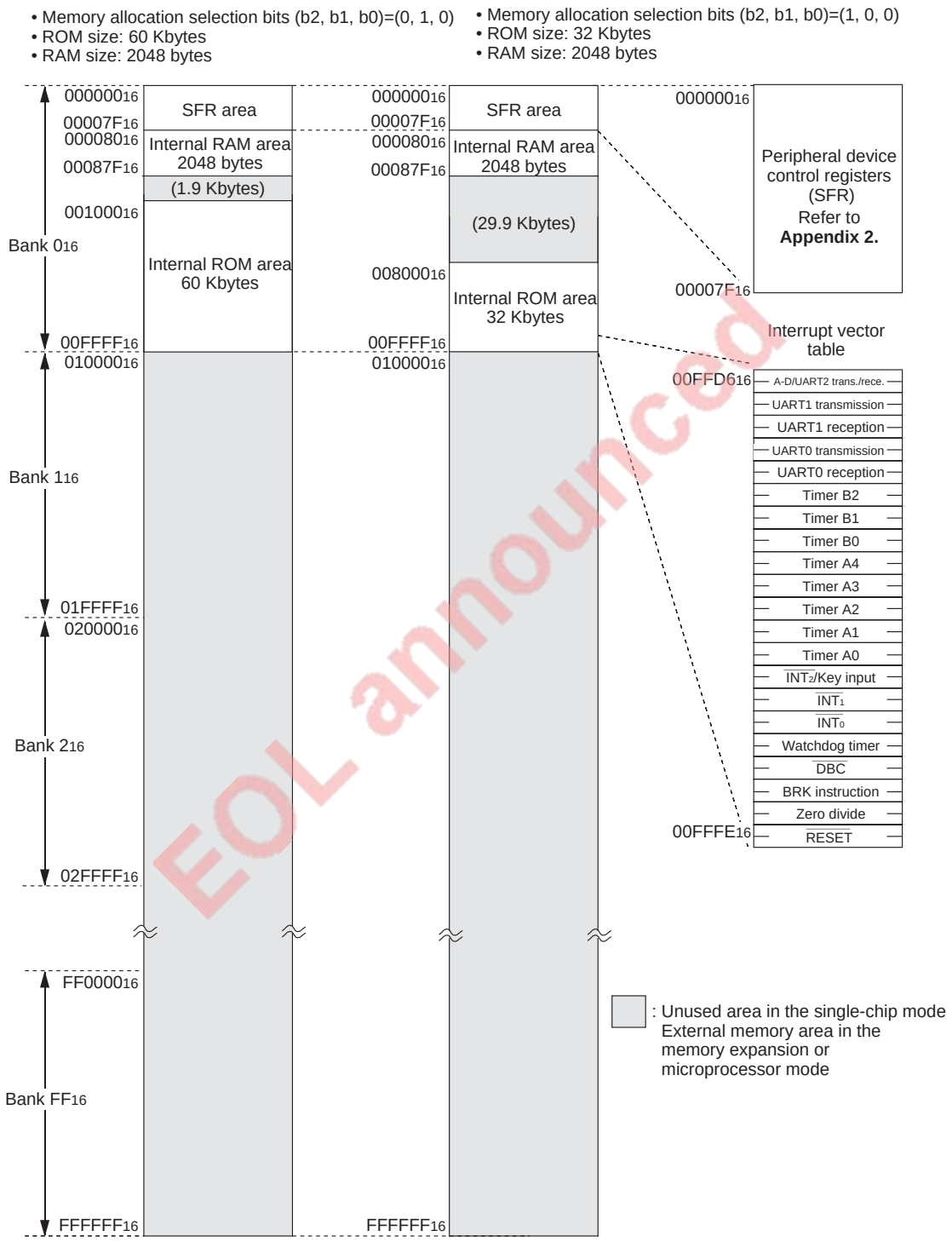
EOL announced

Notes 1: Access to internal ROM area is disabled in the microprocessor mode.
(Refer to section **"2.5 Processor modes."**)
2: Memory allocation of the 7735 Group differs from that of the 7733 Group.
(For the memory allocation of the 7735 Group, refer to section **"Appendix 1 in part 2."**)

Fig. 1 Memory allocation of M37733MHBXXXFP, M37733EHBXXXFP, M37733EHBFS, M37733MHLXXXHP, M37733EHLXXXHP (1)

APPENDIX

Appendix 1. Memory allocation of 7733 Group



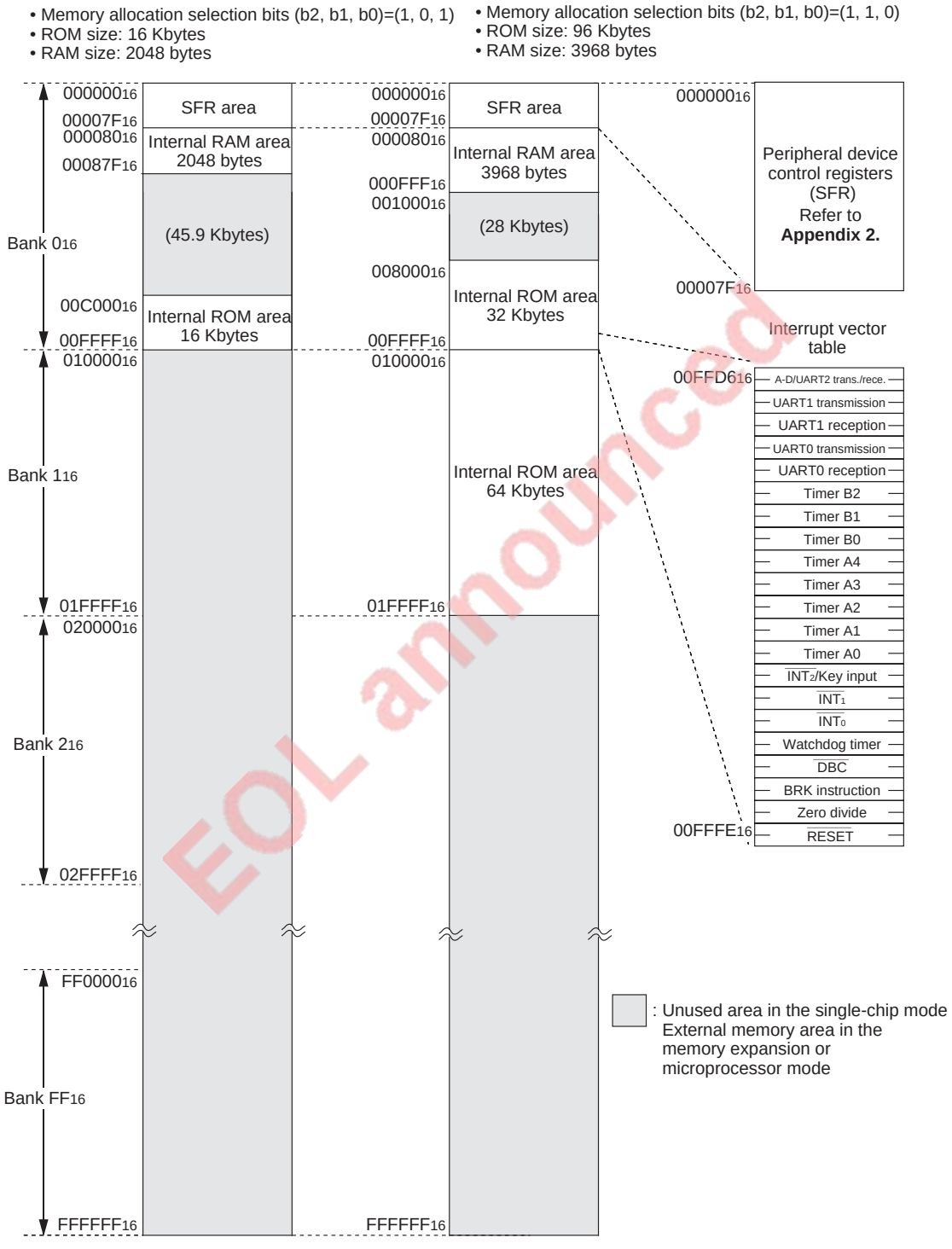
EOL announced

Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)
2: Banks 10₁₆ to FF₁₆ cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 2 Memory allocation of M37733MHBXXXFP, M37733EHBXXXFP, M37733EHBFS, M37733MHLXXXHP, M37733EHLXXXHP (2)

APPENDIX

Appendix 1. Memory allocation of 7733 Group

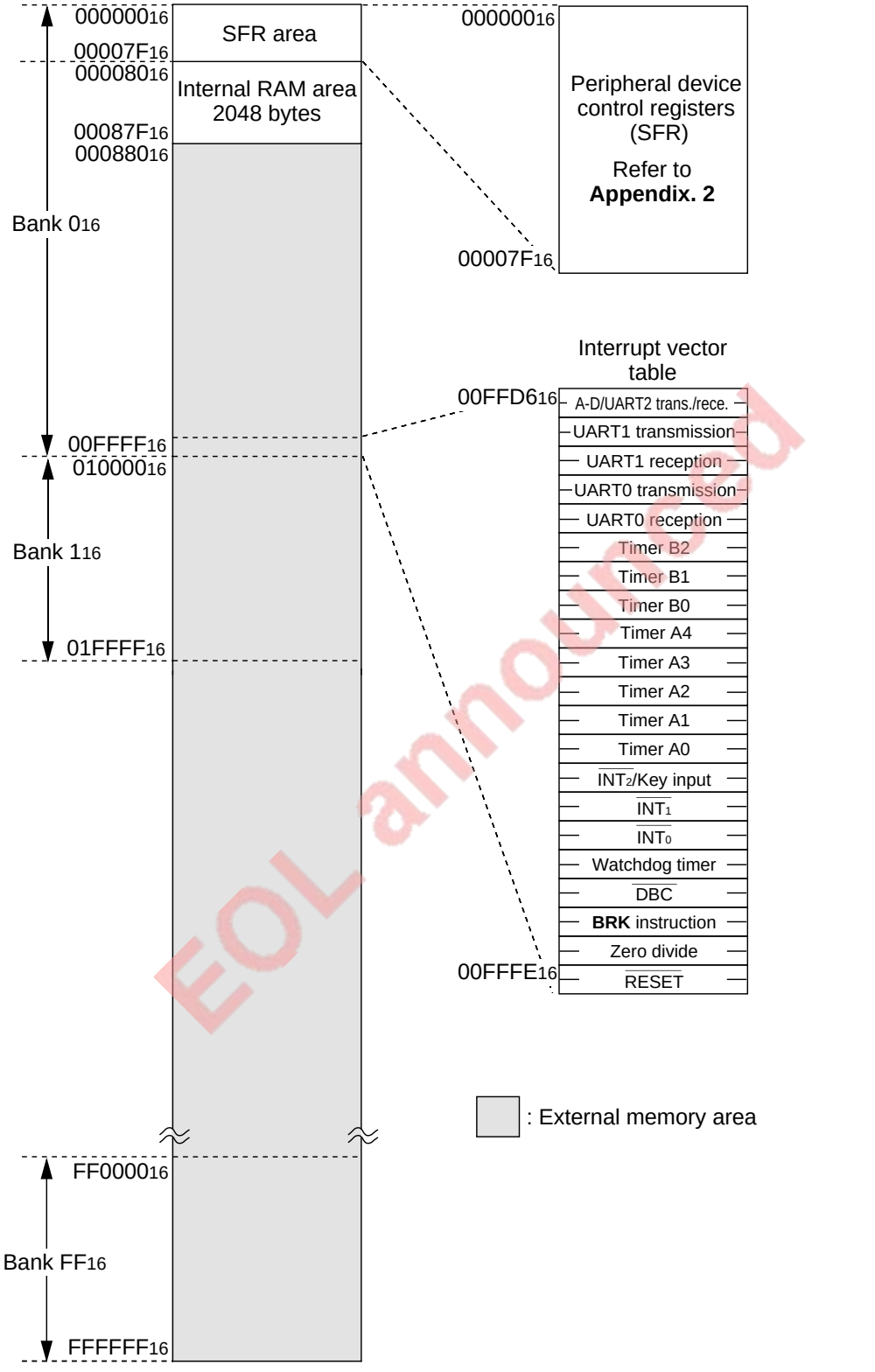


EOL announced

Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)
2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 3 Memory allocation of M37733MHBXXXFP, M37733EHBXXXFP, M37733EHBFS, M37733MHLXXXHP, M37733EHLXXXHP (3)

2. M37733S4BFP, M37733S4LHP



EOL announced

❋ The area at addresses 00FFD6₁₆ to 00FFFF₁₆ is the interrupt vector table area. Be sure to set ROM to this area.

❋ Memory allocation of the 7735 Group differs from that of the 7733 Group. (For the memory allocation of the 7735 Group, refer to section **"Appendix 1 in part 2."**)

Fig. 4 Memory allocation of M37733S4BFP, M37733S4LHP

APPENDIX

Appendix 2. Memory allocation in SFR area

Figures 5 to 8 show the memory allocation in SFR area.
The signals used in Figures 5 to 8 are shown below.

Abbreviations which represent access characteristics

RW : It is possible to read the bit state at reading. The written value becomes valid.
RO : It is possible to read the bit state at reading. The written value becomes invalid.
WO : The written value becomes valid. It is impossible to read the bit state.
▭ : Not implemented. It is impossible to read the bit state. The written value becomes invalid.

0 : "0" immediately after reset.
1 : "1" immediately after reset.
? : Undefined immediately after reset.

0 : Always "0" at reading
? : Always undefined at reading
0 : "0" immediately after reset. Must be fixed to "0."

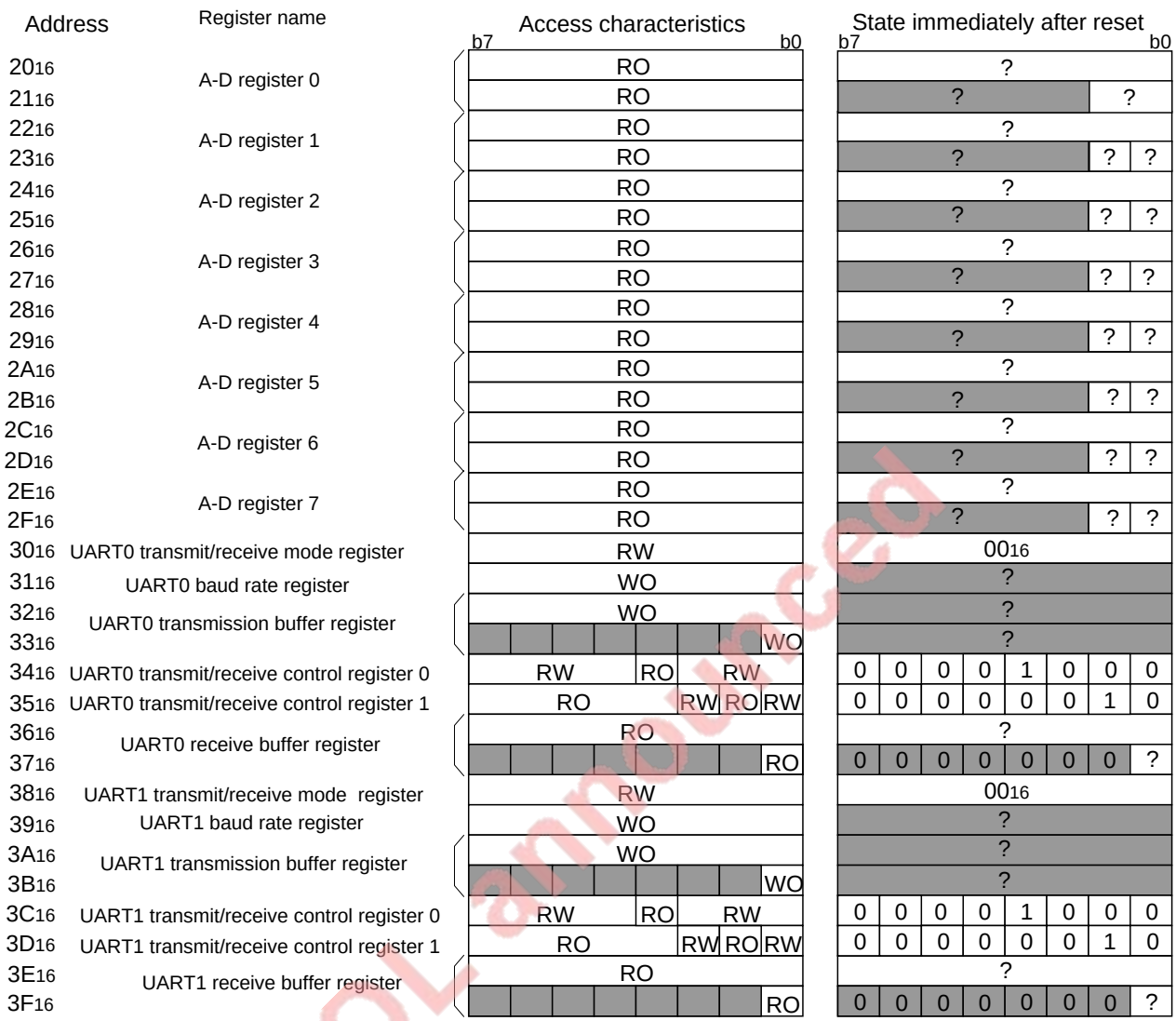
■SFR area (addresses 0_{16} to $7F_{16}$)

Address	Register name	Access characteristics (b7 … b0)	State immediately after reset (b7 … b0)
0_{16}			?
1_{16}			?
2_{16}	Port P0 register	RW	?
3_{16}	Port P1 register	RW	?
4_{16}	Port P0 direction register	RW	00_{16}
5_{16}	Port P1 direction register	RW	00_{16}
6_{16}	Port P2 register	RW	?
7_{16}	Port P3 register	RW	0 0 0 0 ?
8_{16}	Port P2 direction register	RW	00_{16}
9_{16}	Port P3 direction register	RW	0 0 0 0 0 0 0 0
A_{16}	Port P4 register	RW	?
B_{16}	Port P5 register	RW	?
C_{16}	Port P4 direction register	RW	00_{16}
D_{16}	Port P5 direction register	RW	00_{16}
E_{16}	Port P6 register	RW	?
F_{16}	Port P7 register	RW	?
10_{16}	Port P6 direction register	RW	00_{16}
11_{16}	Port P7 direction register	RW	00_{16}
12_{16}	Port P8 register	RW	?
13_{16}			?
14_{16}	Port P8 direction register	RW	00_{16}
15_{16}			?
16_{16}			?
17_{16}			?
18_{16}			?
19_{16}			?
$1A_{16}$			?
$1B_{16}$			?
$1C_{16}$	(Reserved area)❋		?
$1D_{16}$	(Reserved area)❋		?
$1E_{16}$	A-D control register 0	RW	0 0 0 0 0 ? ? ?
$1F_{16}$	A-D control register 1	RW RW	? ? 0 0 0 ? 1 1

❋ Do not write to the reserved area. (For the M37733S4BFP, M37733S4LHP, M37735S4BFP, M37735S4LHP, refer to Figure 20.8.1.)

EOL announced

Fig. 5 Memory allocation in SFR area (1)



EOL announced

Fig. 6 Memory allocation in SFR area (2)

APPENDIX

Appendix 2. Memory allocation in SFR area

Address	Register name	Access characteristics (b7 … b0)	State immediately after reset (b7 … b0)
4016	Count start flag	RW	0016
4116			?
4216	One-shot start flag	WO	? 0 0 0 0 0
4316			?
4416	Up-down flag	WO RW	0 0 0 0 0 0 0 0
4516			?
4616	Timer A0 register	❋1	?
4716		❋1	?
4816	Timer A1 register	❋1	?
4916		❋1	?
4A16	Timer A2 register	❋1	?
4B16		❋1	?
4C16	Timer A3 register	❋1	?
4D16		❋1	?
4E16	Timer A4 register	❋1	?
4F16		❋1	?
5016	Timer B0 register	❋1	?
5116		❋1	?
5216	Timer B1 register	❋1	?
5316		❋1	?
5416	Timer B2 register	❋1	?
5516		❋1	?
5616	Timer A0 mode register	RW	0016
5716	Timer A1 mode register	RW	0016
5816	Timer A2 mode register	RW	0016
5916	Timer A3 mode register	RW	0016
5A16	Timer A4 mode register	RW	0016
5B16	Timer B0 mode register	RW ❋2 RW	0 0 ? ? 0 0 0 0
5C16	Timer B1 mode register	RW ❋2 RW	0 0 ? ? 0 0 0 0
5D16	Timer B2 mode register	RW ❋2 RW	0 0 ? ? 0 0 0 0
5E16	Processor mode register 0	RW WO RW ❋3 RW	0 0 0 0 0 0 ❋3 0
5F16	Processor mode register 1	RW	0

EOL announced

❋1 Access characteristics at addresses 4616 to 5516 vary according to the timer's operating mode. (Refer to chapter **"6. TIMER A,"** and chapter **"7. TIMER B."**)

❋2 Access characteristics for bit 5 at addresses 5B16 to 5D16 vary according to the timer B's operating mode. (Refer to chapter **"7. TIMER B."**)

❋3 Access characteristics for bit 1 at address 5E16 and its state immediately after reset vary according to the voltage level applied to pin CNVSS. (Refer to section **"2.5 Processor modes."**)

Fig. 7 Memory allocation in SFR area (3)

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
60₁₆	Watchdog timer register	WO	? (✵1)
61₁₆	Watchdog timer frequency selection flag	RW	? 0
62₁₆	(Reserved area) ✵4		?
63₁₆	Memory allocation control register	RW	? 0 0 0 0 0
64₁₆	UART 2 transmit/receive mode register	RW	? 0 0 0 0 0 0 0
65₁₆	UART 2 baud rate register (BRG2)	WO	?
66₁₆	UART 2 transmission buffer register	WO	?
67₁₆		WO	?
68₁₆	UART 2 transmit/receive control register 0	RO RW	? 1 0 0 0
69₁₆	UART 2 transmit/receive control register 1	RO RW RO RW	0 0 0 0 0 0 1 0
6A₁₆	UART 2 receive buffer register	RO	?
6B₁₆		RO	0 0 0 0 0 0 0 ?
6C₁₆	Oscillation circuit control register 0	RW(✵2) RW	? 0 0 0 0 0 ? 1
6D₁₆	Port function control register	RW	0 0 0 0 0 0 0 0
6E₁₆	Serial transmit control register	RW	? 0 0 ?
6F₁₆	Oscillation circuit control register 1	WO RW	0 ? 0 ✵3 0 0 0
70₁₆	A-D / UART 2 trans./rece. interrupt control register	RW	? 0 0 0 0
71₁₆	UART0 transmission interrupt control register	RW	? 0 0 0 0
72₁₆	UART0 receive interrupt control register	RW	? 0 0 0 0
73₁₆	UART1 transmission interrupt control register	RW	? 0 0 0 0
74₁₆	UART1 receive interrupt control register	RW	? 0 0 0 0
75₁₆	Timer A0 interrupt control register	RW	? 0 0 0 0
76₁₆	Timer A1 interrupt control register	RW	? 0 0 0 0
77₁₆	Timer A2 interrupt control register	RW	? 0 0 0 0
78₁₆	Timer A3 interrupt control register	RW	? 0 0 0 0
79₁₆	Timer A4 interrupt control register	RW	? 0 0 0 0
7A₁₆	Timer B0 interrupt control register	RW	? 0 0 0 0
7B₁₆	Timer B1 interrupt control register	RW	? 0 0 0 0
7C₁₆	Timer B2 interrupt control register	RW	? 0 0 0 0
7D₁₆	$\overline{INT_0}$ interrupt control register	RW	? 0 0 0 0 0 0
7E₁₆	$\overline{INT_1}$ interrupt control register	RW	? 0 0 0 0 0 0
7F₁₆	$\overline{INT_2}$/Key input interrupt control register	RW	? 0 0 0 0 0 0

FOL announced

✵1 A value of "FFF₁₆" is set to the watchdog timer. (Refer to chapter **"10. WATCHDOG TIMER."**)
✵2 For access characteristics at address 6C₁₆, also refer to **Figure 14.3.2.**
✵3 Fix this bit to "1" in the One Time PROM version and EPROM version.
(However, fix this bit to "0" in the 7735 Group.)
✵4 Do not write to the reserved area.
(Refer to Figure 20.8.1 for the M37733S4BFP, M37733S4LHP, M37735S4BFP, 37735S4LHP.)

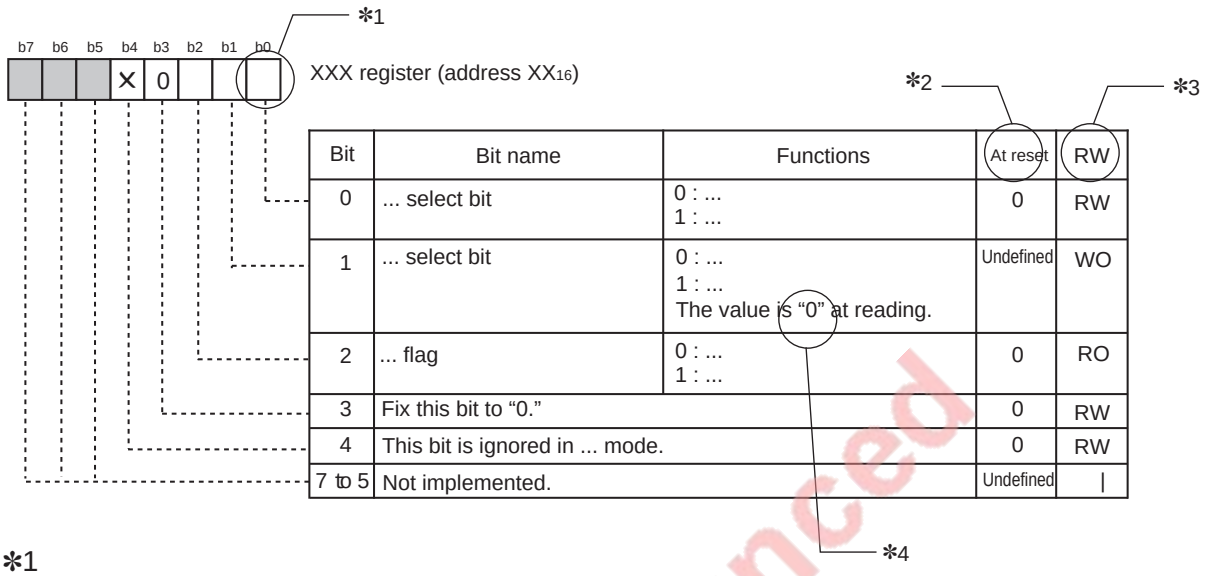
■Internal RAM area (M37733MHBXXXFP: addresses 80₁₆ to FFF₁₆)

- At hardware reset
(not including the case where the stop or wait mode is terminated)...Undefined.
- At software reset...Retains the state immediately before reset.
- When the stop or wait mode is terminated
(when the hardware reset is used)...Retains the state immediately before the **STP** or **WIT** instruction is executed.

Fig. 8 Memory allocation in SFR area (4)

Appendix 3. Control registers

The control registers allocated in the SFR area are shown on the following pages.
Below is the structure diagram for all registers.



Bit	Bit name	Functions	At reset	RW
0	... select bit	0 : ... 1 : ...	0	RW
1	... select bit	0 : ... 1 : ... The value is "0" at reading.	Undefined	WO
2	... flag	0 : ... 1 : ...	0	RO
3	Fix this bit to "0."		0	RW
4	This bit is ignored in ... mode.		0	RW
7 to 5	Not implemented.		Undefined	—

PDL announced

*1

Blank : Set to "0" or "1" according to the usage.
0 : Set to "0" at writing.
1 : Set to "1" at writing.
X : Ignored depending on the mode or state. It may be "0" or "1."
▭ : Not implemented.

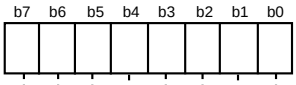
*2

0 : "0" immediately after reset.
1 : "1" immediately after reset.
Undefined : Undefined immediately after reset.

*3

RW : It is possible to read the bit state at reading. The written value becomes valid.
RO : It is possible to read the bit state at reading. The written value becomes invalid. Accordingly, the written value may be "0" or "1."
WO : The written value becomes valid. It is impossible to read the bit state. The value is undefined at reading. However, when ["0" at reading] is indicated in the "Function" or "Note" column, the bit is always "0" at reading.(See to *4 above.)
— : It is impossible to read the bit state. The value is undefined at reading. However, when ["0" at reading] is indicated in the "Function" or "Note" column, the bit is always "0" at reading.(See to *4 above.)
The written value becomes invalid. Accordingly, the written value may be "0" or "1."

Port Pi register

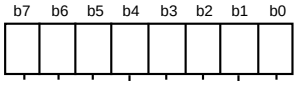


Port Pi register (i = 0 to 8)
(addresses 2_{16},3_{16},6_{16},7_{16},A_{16},B_{16},E_{16},F_{16},12_{16})

Bit	Bit name	Functions	At reset	RW
0	Port Pi_0's pin	Data is input from or output to a pin by reading from or writing to the corresponding bit. 0: "L" level 1: "H" level	Undefined	RW
1	Port Pi_1's pin		Undefined	RW
2	Port Pi_2's pin		Undefined	RW
3	Port Pi_3's pin		Undefined	RW
4	Port Pi_4's pin		Undefined	RW
5	Port Pi_5's pin		Undefined	RW
6	Port Pi_6's pin		Undefined	RW
7	Port Pi_7's pin		Undefined	RW

Note: Writing to bits 4 to 7 of the port P3 register is invalid and these bits are fixed to "0" when they are read.

Port Pi direction register



Port Pi direction register (i = 0 to 8)
(addresses 4_{16},5_{16},8_{16},9_{16},C_{16},D_{16},10_{16},11_{16},14_{16})

Bit	Bit name	Functions	At reset	RW
0	Port Pi_0 direction selection bit	0: Input mode (The port functions as an input port.) 1: Output mode (The port functions as an output port.)	0	RW
1	Port Pi_1 direction selection bit		0	RW
2	Port Pi_2 direction selection bit		0	RW
3	Port Pi_3 direction selection bit		0	RW
4	Port Pi_4 direction selection bit		0	RW
5	Port Pi_5 direction selection bit		0	RW
6	Port Pi_6 direction selection bit		0	RW
7	Port Pi_7 direction selection bit		0	RW

Note: Writing to bits 4 to 7 of the port P3 direction register is invalid and these bits are fixed to "0" when they are read.

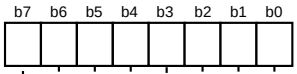
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Corresponding pin	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0

EOL announced

APPENDIX

Appendix 3. Control registers

A-D control register 0



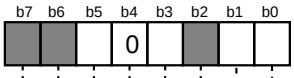
A-D control register 0 (address $1E_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Analog input selection bits (Valid in the one-shot and repeat modes.) **(Note 1)**	b2 b1 b0 0 0 0: AN_0 is selected. 0 0 1: AN_1 is selected. 0 1 0: AN_2 is selected. 0 1 1: AN_3 is selected. 1 0 0: AN_4 is selected. 1 0 1: AN_5 is selected. **(Note 2)** 1 1 0: AN_6 is selected. 1 1 1: AN_7 is selected.	Undefined	RW
1			Undefined	RW
2			Undefined	RW
3	A-D operation mode selection bits	b4b3 00: One-shot mode 01: Repeat mode 10: Single sweep mode 11: Repeat sweep mode	0	RW
4			0	RW
5	Trigger selection bit	0: Internal trigger 1: External trigger	0	RW
6	A-D conversion start flag	0: A-D conversion is stopped. 1: A-D conversion is started.	0	RW
7	A-D conversion frequency (ϕ_{AD}) selection flag	0: $f_2/4$* 1: $f_2/2$	0	RW

f_2*: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Notes 1: These bits are ignored in the single sweep and repeat sweep modes. (They may be "0" or "1.")
2: When an external trigger is selected, pin AN_5 cannot be used as an analog input pin.
3: Writing to each bit (except bit 6) of the A-D control register 0 must be performed while the A-D converter stops operating.

A-D control register 1



A-D control register 1 (address $1F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	A-D sweep pin selection bits (Valid in the single sweep and repeat sweep modes.) **(Note 1)**	b1 b0 0 0: Pins AN_0 and AN_1 (2 pins) 0 1: Pins AN_0 to AN_3 (4 pins) 1 0: Pins AN_0 to AN_5 (6 pins) **(Note 2)** 1 1: Pins AN_0 to AN_7 (8 pins)	1	RW
1			1	RW
2	Not implemented.		Undefined	_
3	8/10-bit mode selection bit	0: 8-bit resolution 1: 10-bit resolution	0	RW
4	Must be fixed to "0."		0	RW
5	V_{REF} connection selection bit **(Note 4)**	0: Pin V_{REF} is connected. 1: Pin V_{REF} is disconnected. (High impedance)	0	RW
6	Not implemented.		Undefined	_
7				

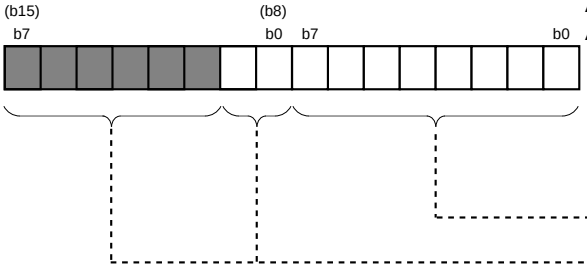
Notes 1: These bits are ignored in the one-shot and repeat modes. (They may be "0" or "1.")
2: When an external trigger is selected, pin AN_5 cannot be used as an analog input pin.
3: Writing to each bit of the A-D control register 1 must be performed while the A-D converter stops operating.
4: When the V_{REF} connection selection bit is cleared from "1" to "0," wait for an interval of 1 µs or more passed, and then start A-D conversion.

EOL announced

A-D register i

●When resolution = 8 bits

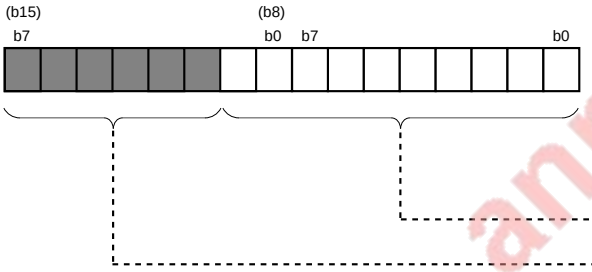
A-D register 0 (addresses 21_{16} and 20_{16})
A-D register 1 (addresses 23_{16} and 22_{16})
A-D register 2 (addresses 25_{16} and 24_{16})
A-D register 3 (addresses 27_{16} and 26_{16})
A-D register 4 (addresses 29_{16} and 28_{16})
A-D register 5 (addresses $2B_{16}$ and $2A_{16}$)
A-D register 6 (addresses $2D_{16}$ and $2C_{16}$)
A-D register 7 (addresses $2F_{16}$ and $2E_{16}$)



Bit	Functions	At reset	RW
7 to 0	The A-D conversion result is read out.	Undefined	RO
15 to 8	"0" at reading.	0	RO

●When resolution = 10 bits

A-D register 0 (addresses 21_{16} and 20_{16})
A-D register 1 (addresses 23_{16} and 22_{16})
A-D register 2 (addresses 25_{16} and 24_{16})
A-D register 3 (addresses 27_{16} and 26_{16})
A-D register 4 (addresses 29_{16} and 28_{16})
A-D register 5 (addresses $2B_{16}$ and $2A_{16}$)
A-D register 6 (addresses $2D_{16}$ and $2C_{16}$)
A-D register 7 (addresses $2F_{16}$ and $2E_{16}$)



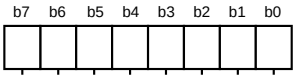
Bit	Functions	At reset	RW
9 to 0	The A-D conversion result is read out.	Undefined	RO
15 to 10	"0" at reading.	0	RO

EOL announced

APPENDIX

Appendix 3. Control registers

UART0, UART1 transmit/receive mode register



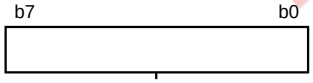
UART0 transmit/receive mode register (address 30_{16})
UART1 transmit/receive mode register (address 38_{16})

Bit	Bit name	Functions	At reset	RW
0	Serial I/O mode selection bits	b2 b1 b0 0 0 0: Serial I/O is disabled. (P8 functions as a programmable I/O port.) 0 0 1: Clock synchronous serial I/O mode 0 1 0: Do not select. 0 1 1: Do not select. 1 0 0: UART mode (Transfer data length = 7 bits) 1 0 1: UART mode (Transfer data length = 8 bits) 1 1 0: UART mode (Transfer data length = 9 bits) 1 1 1: Do not select.	0	RW
1			0	RW
2			0	RW
3	Internal/External clock selection bit	0: Internal clock 1: External clock	0	RW
4	Stop bit length selection bit (Valid in the UART mode.) **(Note)**	0: One stop bit 1: Two stop bits	0	RW
5	Odd/Even parity selection bit (Valid in the UART mode when the parity enable bit = "1.") **(Note)**	0: Odd parity 1: Even parity	0	RW
6	Parity enable bit (Valid in the UART mode.) **(Note)**	0: Parity is disabled. 1: Parity is enabled.	0	RW
7	Sleep selection bit (Valid in the UART mode.) **(Note)**	0: The sleep mode is terminated. (Ignored.) 1: The sleep mode is selected.	0	RW

Note: Bits 4 to 6 are ignored in the clock synchronous serial I/O mode. (They may be "0" or "1.")
Fix bit 7 to "0."

EOL announced

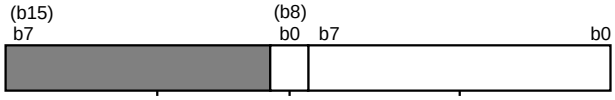
UARTi baud rate register (BRGi)



UART0 baud rate register (address 31_{16})
UART1 baud rate register (address 39_{16})
UART2 baud rate register (address 65_{16})

Bit	Functions	At reset	RW
7 to 0	Values 00_{16} to FF_{16} can be set. Assuming that the set value = n, BRGi divides the count source frequency by (n + 1).	Un-defined	WO

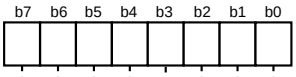
UARTi transmission buffer register



UART0 transmission buffer register (addresses 33_{16}, 32_{16})
UART1 transmission buffer register (addresses $3B_{16}$, $3A_{16}$)
UART2 transmission buffer register (addresses 67_{16}, 66_{16})

Bit	Functions	At reset	RW
8 to 0	The transmit data is set.	Un-defined	WO
15 to 9	Not implemented.	Un-defined	—

UARTi transmit/receive control register 0



UART0 transmit/receive control register 0 (address 34_{16})
UART1 transmit/receive control register 0 (address $3C_{16}$)

Bit	Bit name	Functions	At reset	RW
0	BRG count source selection bits	b1 b0 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
1			0	RW
2	$\overline{CTS}/\overline{RTS}$ function selection bit (Valid when the $\overline{CTS}/\overline{RTS}$ enable bit is "0.")	0: The $\overline{CTS}$ function is selected. 1: The $\overline{RTS}$ function is selected.	0	RW
3	Transmission register empty flag	0: Data is present in the transmission register. (Transmission is in progress.) 1: No data is present in the transmission register. (Transmission is completed.)	1	RO
4	$\overline{CTS}/\overline{RTS}$ enable bit	0: The $\overline{CTS}/\overline{RTS}$ function is enabled. 1: The $\overline{CTS}/\overline{RTS}$ function is disabled. ($P8_0$ and $P8_4$ function as programmable I/O ports.)	0	RW
5	Data output selection bit	0: Pin TxD_i is set for CMOS output. 1: Pin TxD_i is set for N-channel open-drain output.	0	RW
6	CLK polarity selection bit (This bit is used in the clock synchronous serial I/O mode.) **(Note)**	0: At the falling edge of the transfer clock, transmit data is output; at the rising edge of the transfer clock, receive data is input. When not in transferring, pin CLK_i's level is "H." 1: At the rising edge of the transfer clock, transmit data is output; at the falling edge of the transfer clock, receive data is input. When not in transferring, pin CLK_i's level is "L."	0	RW
7	Transfer format selection bit (This bit is used in the clock synchronous serial I/O mode.) **(Note)**	0: LSB (Least Significant Bit) first 1: MSB (Most Significant Bit) first	0	RW

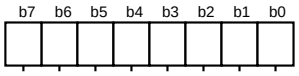
Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**
Note: Fix bits 6 and 7 to "0" in the UART mode.

EOL announced

APPENDIX

Appendix 3. Control registers

UARTi transmit/receive control register 1



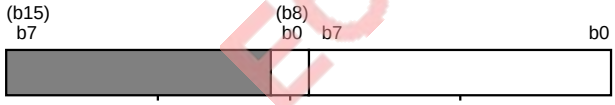
UART0 transmit/receive control register 1 (address 35_{16})
UART1 transmit/receive control register 1 (address $3D_{16}$)
UART2 transmit/receive control register 1 (address 69_{16})

Bit	Bit name	Functions	At reset	RW
0	Transmit enable bit	0: Transmission is disabled. 1: Transmission is enabled.	0	RW
1	Transmission buffer empty flag	0: Data is present in the transmission buffer register. 1: No data is present in the transmission buffer register.	1	RO
2	Receive enable bit	0: Reception is disabled. 1: Reception is enabled.	0	RW
3	Receive completion flag	0: No data is present in the receive buffer register. 1: Data is present in the receive buffer register.	0	RO
4	Overrun error flag **(Note 1)**	0: No overrun error is detected. 1: Overrun error is detected.	0	RO
5	Framing error flag **(Notes 1 and 2)** (Valid in the UART mode.)	0: No framing error is detected. 1: Framing error is detected.	0	RO
6	Parity error flag **(Notes 1 and 2)** (Valid in the UART mode.)	0: No parity error is detected. 1: Parity error is detected.	0	RO
7	Error sum flag **(Notes 1 and 2)** (Valid in the UART mode.)	0: No error is detected. 1: Error is detected.	0	RO

Notes 1: Bits 4 to 7 are cleared to "0" when the serial I/O mode selection bits (bits 2 to 0 at addresses 30_{16}, 38_{16}) are cleared to "000_2" or when the receive enable bit is cleared to "0." (Bit 7 is cleared to "0" when all of bits 4 to 6 are "0.")
Note also that bits 5 and 6 are cleared to "0" when the low-order byte of the UARTi receive buffer register (addresses 36_{16}, $3E_{16}$, $6A_{16}$) is read out.
2: Bits 5 to 7 are ignored in the clock synchronous serial I/O mode.

EOL announced

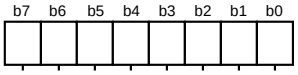
UARTi receive buffer register



UART0 receive buffer register (addresses 37_{16}, 36_{16})
UART1 receive buffer register (addresses $3F_{16}$, $3E_{16}$)
UART2 receive buffer register (addresses $6B_{16}$, $6A_{16}$)

Bit	Functions	At reset	RW
8 to 0	The receive data is read out from here.	Un-defined	RO
15 to 9	Not implemented. A value of "0" is read out from here.	0	—

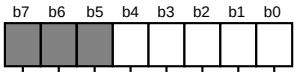
Count start flag



Count start flag (address 40_{16})

Bit	Bit name	Functions	At reset	RW
0	Timer A0 count start flag	0: Counting is stopped. 1: Counting is started.	0	RW
1	Timer A1 count start flag		0	RW
2	Timer A2 count start flag		0	RW
3	Timer A3 count start flag		0	RW
4	Timer A4 count start flag		0	RW
5	Timer B0 count start flag		0	RW
6	Timer B1 count start flag		0	RW
7	Timer B2 count start flag		0	RW

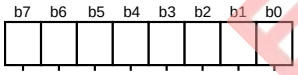
One-shot start flag



One-shot start flag (address 42_{16})

Bit	Bit name	Functions	At reset	RW
0	Timer A0 one-shot start flag	1: One-shot pulse output is started. (Valid when the internal trigger is selected.) "0" at reading.	0	WO
1	Timer A1 one-shot start flag		0	WO
2	Timer A2 one-shot start flag		0	WO
3	Timer A3 one-shot start flag		0	WO
4	Timer A4 one-shot start flag		0	WO
7 to 5	Not implemented.		Undefined	—

Up-down flag



Up-down flag (address 44_{16})

Bit	Bit name	Functions	At reset	RW
0	Timer A0 up-down flag	0: Countdown 1: Countup This bits is valid when the contents of the up-down flag is selected as the up-down switching factor.	0	RW
1	Timer A1 up-down flag		0	RW
2	Timer A2 up-down flag		0	RW
3	Timer A3 up-down flag		0	RW
4	Timer A4 up-down flag		0	RW
5	Timer A2 two-phase pulse signal processing selection bit	0: Two-phase pulse signal processing function is disabled. 1: Two-phase pulse signal processing function is enabled. When not using the two-phase pulse signal processing function, be sure to set this bit to "0." This bit is "0" at reading.	0	WO
6	Timer A3 two-phase pulse signal processing selection bit		0	WO
7	Timer A4 two-phase pulse signal processing selection bit		0	WO

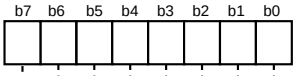
Note: When writing to bits 5 to 7, use the **LDM** or **STA** instruction.

EOL announced

APPENDIX

Appendix 3. Control registers

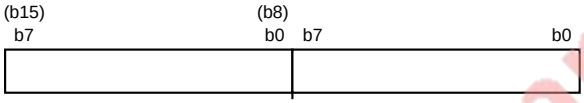
Timer Ai mode register



Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode 0 1: Event counter mode 1 0: One-shot pulse mode 1 1: Pulse width modulation (PWM) mode	0	RW
1			0	RW
2	These bits have different functions according to the operating mode.		0	RW
3			0	RW
4			0	RW
5			0	RW
6			0	RW
7			0	RW

Timer Ai register

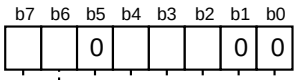


Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Undefined	RW

EOL announced

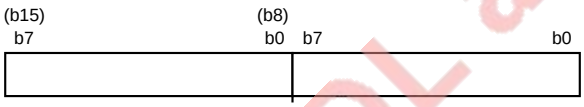
■Timer mode



Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode	0	RW
1			0	RW
2	Pulse output function selection bit	0: No pulse is output. (Pin TAi_{OUT} functions as a programmable I/O port.) 1: Pulse is output. (Pin TAi_{OUT} functions as a pulse output pin.)	0	RW
3	Gate function selection bits	b4 b3 0 X: No gate function (Pin TAi_{IN} functions as a programmable I/O port.) 1 0: Counter counts only while pin TAi_{IN}'s input signal level is "L." 1 1: Counter counts only while pin TAi_{IN}'s input signal level is "H."	0	RW
4			0	RW
5	Must be fixed to "0" in the timer mode.		0	RW
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**



Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Undefined	RW

EOL announced

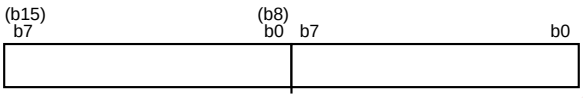
APPENDIX

Appendix 3. Control registers

■Event counter mode

Timer A0 mode register (address 56_{16})
Timer A1 mode register (address 57_{16})

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 1: Event counter mode	0	RW
1			0	RW
2	Pulse output function selection bit	0: No pulse is output. (Pin TA0OUT or TA1OUT functions as a programmable I/O port.) 1: Pulse is output. (Pin TA0OUT or TA1OUT functions as a pulse output pin.)	0	RW
3	Count polarity selection bit	0: Counts at falling edge of external signal 1: Counts at rising edge of external signal	0	RW
4	Up-down switching factor selection bit	0: Contents of the up-down flag 1: A signal which is input to pin TA0OUT or TA1OUT	0	RW
5	Must be fixed to "0" in the event counter mode.		0	RW
6	These bits are ignored in the event counter mode.		0	RW
7			0	RW



Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})

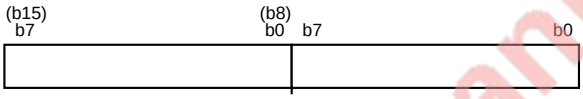
Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1) in down-counting, or by ($FFFF_{16}$ – n + 1) in up-counting. At reading this register, the counter value is read out.	Undefined	RW

EOL announced

Timer A2 mode register (address 58_{16})
Timer A3 mode register (address 59_{16})
Timer A4 mode register (address $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 1: Event counter mode	0	RW
1			0	RW
2	Pulse output function selection bit	0: No pulse is output. (Pin $TA2_{OUT}$, $TA3_{OUT}$, or $TA4_{OUT}$ functions as a programmable I/O port.) 1: Pulse is output. (Pin $TA2_{OUT}$, $TA3_{OUT}$, or $TA4_{OUT}$ functions as a pulse output pin.)	0	RW
3	Count polarity selection bit	0: Counting is performed at the falling edge of the external signal. 1: Counting is performed at the rising edge of the external signal.	0	RW
4	Up-down switching factor selection bit	0: Contents of the up-down flag 1: A signal which is input to pin $TA2_{OUT}$, $TA3_{OUT}$, or $TA4_{OUT}$	0	RW
5	Must be fixed to “0” in the event counter mode.		0	RW
6	Count type selection bit	0: Reload count type 1: Free-run count type	0	RW
7	Two-phase pulse signal processing type selection bit **(Note)**	0: Normal processing 1: Quadruple processing	0	RW

Note: This bit is valid only for the timer A3 mode register.
For the timer A2 and A4 mode registers, this bit is ignored. (It may be “0” or “1.”)

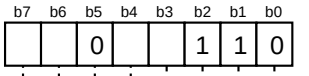


Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1) in down-counting, or by ($FFFF_{16}$ – n + 1) in up-counting. At reading this register, the counter value is read out.	Undefined	RW

EOL announced

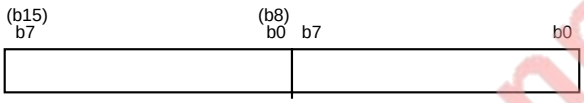
■One-shot pulse mode



Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 1 0: One-shot pulse mode	0	RW
1			0	RW
2	Must be fixed to “1” in the one-shot pulse mode.		0	RW
3	Trigger selection bits	b4 b3 0 X: Writing “1” to the one-shot start flag (Pin TAi_{IN} functions as a programmable I/O port.) 1 0: Falling edge of the pin TAi_{IN}’s input signal 1 1: Rising edge of the pin TAi_{IN}’s input signal	0	RW
4			0	RW
5	Must be fixed to “0” in the one-shot pulse mode.		0	RW
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **“14. CLOCK GENERATING CIRCUIT.”**



Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, “H” level width of the one-shot pulse output from pin TAi_{OUT} is n/fi.	Undefined	WO

fi: Frequency of the count source (f_2, f_{16}, f_{64}, or f_{512})

EOL announced

■Pulse width modulation (PMW) mode

b7	b6	b5	b4	b3	b2	b1	b0
					1	1	1

Timer Ai mode register (i = 0 to 4) (addresses 56_{16} to $5A_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 1 1: PWM mode	0	RW
1			0	RW
2	Must be fixed to "1" in the PWM mode.		0	RW
3	Trigger selection bits	b4 b3 0 X: Writing "1" to the count start flag (Pin TAi_{IN} functions as a programmable I/O port.) 1 0: Falling edge of the pin TAi_{IN}'s input signal 1 1: Rising edge of the pin TAi_{IN}'s input signal	0	RW
4			0	RW
5	16/8-bit PWM mode selection bit	0: The counter operates as a 16-bit pulse width modulator. 1: The counter operates as an 8-bit pulse width modulator.	0	RW
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

■ When operating as a 16-bit pulse width modulator

(b15) b7 (b8) b0 b7 b0

Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFE_{16}$ can be set. Assuming that the set value = n, "H" level width of the PWM pulse which is output from pin TAi_{OUT} is n/fi.	Un-defined	WO

fi: Frequency of the count source (f_2, f_{16}, f_{64}, or f_{512})

■ When operating as an 8-bit pulse width modulator

(b15) b7 (b8) b0 b7 b0

Timer A0 register (addresses 47_{16}, 46_{16})
Timer A1 register (addresses 49_{16}, 48_{16})
Timer A2 register (addresses $4B_{16}$, $4A_{16}$)
Timer A3 register (addresses $4D_{16}$, $4C_{16}$)
Timer A4 register (addresses $4F_{16}$, $4E_{16}$)

Bit	Functions	At reset	RW
7 to 0	Values 00_{16} to FF_{16} can be set. Assuming that the set value = m, period of the PWM pulse which is output from pin TAi_{OUT} is $(m + 1)(2^8 - 1)$/fi.	Un-defined	WO
15 to 8	Values 00_{16} to FE_{16} can be set. Assuming that the set value = n, "H" level width of the PWM pulse which is output from pin TAi_{OUT} is n(m +1)/fi.	Un-defined	WO

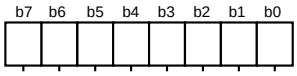
fi: Frequency of the count source (f_2, f_{16}, f_{64}, or f_{512})

EOL announced

APPENDIX

Appendix 3. Control registers

Timer Bi mode register

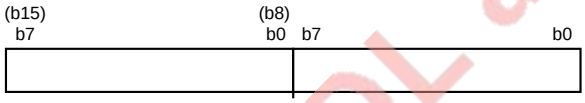


Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode 0 1: Event counter mode 1 0: Pulse period/Pulse width measurement mode 1 1: Do not select.	0	RW
1			0	RW
2	These bits have different functions according to the operating mode.		0	RW
3			0	RW
4	Must be fixed to “0” (i = 0).		0	RW
	Not implemented (i = 1, 2).		Un-defined	—
5	These bits have different functions according to the operating mode.		Un-defined	RO **(Note)**
6			0	RW
7			0	RW

Note: In the timer and event counter modes, bit 5 is ignored and undefined at reading.

Timer Bi register



Timer B0 register (addresses 51_{16}, 50_{16})
Timer B1 register (addresses 53_{16}, 52_{16})
Timer B2 register (addresses 55_{16}, 54_{16})

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Un-defined	RW

EOL announced

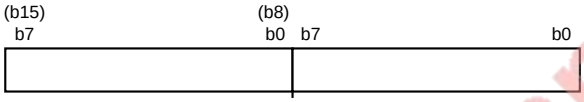
■Timer mode

b7	b6	b5	b4	b3	b2	b1	b0
		X		X	X	0	0

Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 0: Timer mode	0	RW
1			0	RW
2	These bits are ignored in the timer mode.		0	RW
3			0	RW
4	•Timer B0 mode register Must be fixed to "0."		0	RW
	•Timer B1 and B2 mode registers Not implemented.		Un-defined	—
5	This bit is ignored in the timer mode and is undefined at reading.		Un-defined	RO
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**



Timer B0 register (addresses 51_{16}, 50_{16})
Timer B1 register (addresses 53_{16}, 52_{16})
Timer B2 register (addresses 55_{16}, 54_{16})

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Un-defined	RW

EOL announced

Appendix 3. Control registers

■Event counter mode

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X				0	1

Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 0 1: Event counter mode	0	RW
1			0	RW
2	Count polarity selection bits	b3 b2 0 0: Counting is performed at the falling edge of the external signal. 0 1: Counting is performed at the rising edge of the external signal. 1 0: Counting is performed at both falling and rising edges of the external signal. 1 1: Do not select.	0	RW
3			0	RW
4	•Timer B0 mode register Must be fixed to "0."		0	RW
	•Timer B1 and B2 mode registers Not implemented.		Un-defined	—
5	This bit is ignored in the event counter mode and is undefined at reading.		Un-defined	RO
6	These bits are ignored in the event counter mode.		0	RW
7			0	RW

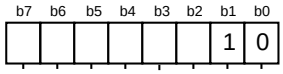
(b15) (b8) b7 b0 b7 b0

Timer B0 register (addresses 51_{16}, 50_{16})
Timer B1 register (addresses 53_{16}, 52_{16})
Timer B2 register (addresses 55_{16}, 54_{16})

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Un-defined	RW

EOL announced

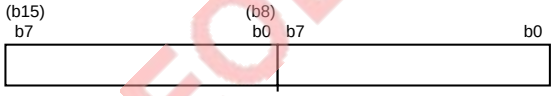
■Pulse period/Pulse width measurement mode



Timer Bi mode register (i = 0 to 2) (addresses $5B_{16}$ to $5D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Operating mode selection bits	b1 b0 1 0: Pulse period/pulse width measurement mode	0	RW
1			0	RW
2	Measurement mode selection bits	b3 b2 0 0: Pulse period measurement Interval between falling edges of the measurement pulse) 0 1: Pulse period measurement Interval between rising edges of the measurement pulse) 1 0: Pulse width measurement Interval from a falling edge to a rising edge, and from a rising edge to a falling edge of the measurement pulse) 1 1: Do not select.	0	RW
3			0	RW
4	•Timer B0 mode register Must be fixed to "0."		0	RW
	•Timer B1 and B2 mode registers Not implemented.		Undefined	—
5	Timer Bi overflow flag **(Note)**	0: No overflow 1: Overflow	1	RO
6	Count source selection bits	b7 b6 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
7			0	RW

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**
Note: Timer Bi overflow flag is cleared to "0" when writing to the timer Bi mode register is performed with the count start flag = "1." This flag cannot be set to "1" by software.



Timer B0 register (addresses 51_{16}, 50_{16})
Timer B1 register (addresses 53_{16}, 52_{16})
Timer B2 register (addresses 55_{16}, 54_{16})

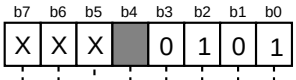
Bit	Functions	At reset	RW
15 to 0	The result of the pulse period or pulse width measurement is read out.	Undefined	RO

EOL announced

APPENDIX

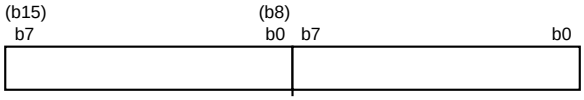
Appendix 3. Control registers

■Clock timer



Timer B2 mode register (address $5D_{16}$)

Bit	Functions	At reset	RW
0	Must be fixed to “1” for the clock timer.	0	RW
1	Must be fixed to “0” for the clock timer.	0	RW
2	Must be fixed to “1” for the clock timer.	0	RW
3	Must be fixed to “0” for the clock timer.	0	RW
4	Not implemented.	Un-defined	—
5	This bit is ignored for the clock timer.	Un-defined	RO
6	These bits are ignored for the clock timer.	0	RW
7		0	RW



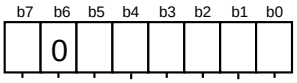
Timer B2 register (addresses 55_{16} and 54_{16})

Bit	Functions	At reset	RW
15 to 0	Values 0000_{16} to $FFFF_{16}$ can be set. Assuming that the set value = n, counter divides the count source frequency by (n + 1). At reading this register, the counter value is read out.	Un-defined	RW

EOL announced

Processor mode register 0

b7	b6	b5	b4	b3	b2	b1	b0
	0						



Processor mode register 0 (address 5E16)

Bit	Bit name	Functions	At reset	RW
0	Processor mode bits	b1 b0 0 0: Single-chip mode 0 1: Memory expansion mode 1 0: Microprocessor mode 1 1: Do not select.	0	RW
1			0 **(Note 1)**	RW
2	Wait bit	0: Software wait is inserted when accessing external area. 1: No software wait is inserted when accessing external area.	0	RW
3	Software reset bit	Microcomputer is reset by setting this bit to "1." This bit is "0" at reading.	0	WO
4	Interrupt priority detection time selection bits	b5 b4 0 0: 7 cycles of ϕ 0 1: 4 cycles of ϕ 1 0: 2 cycles of ϕ 1 1: Do not select.	0	RW
5			0	RW
6	Must be fixed to "0."		0	RW
7	Clock ϕ_1 output selection bit **(Note 2)**	0: Clock ϕ_1 output is disabled. (P42 functions as a programmable I/O port.) 1: Clock ϕ_1 output is enabled. (Port P42functions as a clock ϕ_1 output pin.)	0	RW

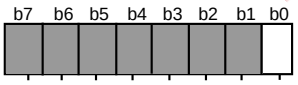
Notes 1: When the Vcc-level voltage is applied to pin CNVss, this bit is set to "1" after reset. (At reading, this bit is always "1.")

2: This bit is ignored in the microprocessor mode. (It may be "0" or "1.")

EOL announced

Processor mode register 1

b7	b6	b5	b4	b3	b2	b1	b0



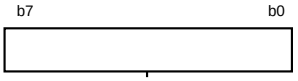
Processor mode register 1 (address 5F16)

Bit	Bit name	Function	At reset	RW
0	Wait selection bit	0 : Wait 0 1 : Wait 1	0	RW
7 to1	Not implemented.		Un-defined	–

APPENDIX

Appendix 3. Control registers

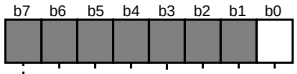
Watchdog timer register



Watchdog timer register (address 60_{16})

Bit	Functions	At reset	RW
7 to 0	Watchdog timer is initialized. By writing dummy data to this register, watchdog timer's value is initialized to "FFF_{16}" (Dummy data: 00_{16} to FF_{16}).	Un-defined	WO

Watchdog timer frequency selection flag



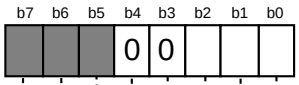
Watchdog timer frequency selection flag (address 61_{16})

Bit	Bit name	Functions	At reset	RW
0	Watchdog timer frequency selection flag	0 : Clock f_{512} 1 : Clock f_{32}	0	RW
7 to 1	Not implemented.		Un-defined	—

Clocks f_{32}, f_{512} : Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

EOL announced

Memory allocation control register

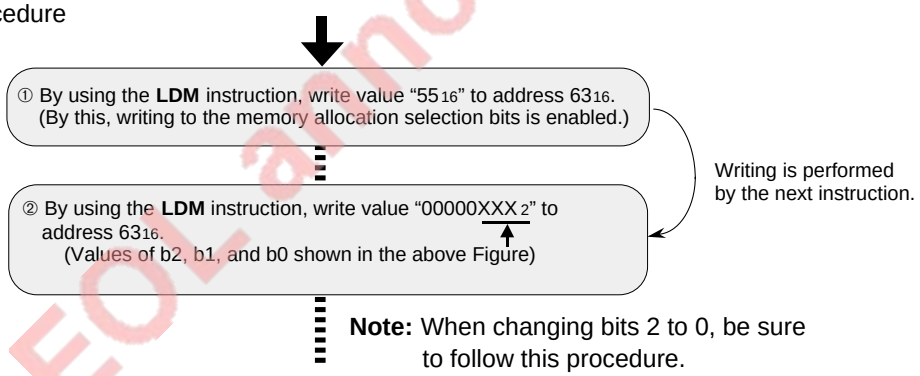


Memory allocation control register (address 63 16) **(Note 3)**

Bit	Bit name	Functions	At reset	RW
0	Memory allocation selection bits **(Notes 1 and 2)**	b2b1b0 ROM size ROM size 0 0 0: 124 Kbytes, 3968 bytes 0 0 1: 120 Kbytes, 3968 bytes 0 1 0: 60 Kbytes, 2048 bytes 0 1 1: Do not select. 1 0 0: 32 Kbytes, 2048 bytes 1 0 1: 16 Kbytes, 2048 bytes 1 1 0: 96 Kbytes, 3968 bytes 1 1 1: Do not select.	0	RW
1			0	RW
2			0	RW
3	Must be fixed to "0." **(Note 1)**		0	RW
4			0	RW
7 to 5	Not implemented.		Un-defined		

Notes 1: The case where value "55 16" is written in ① of the procedure listed below is not included.
2: When changing these bits, this change must be performed in an area which is internal ROM area before and after this change, for example addresses 00C000 16 to 00FFFF16. Also, when changing these bits, be sure to follow the procedure listed below.
3: This figure is applied only to the M37733MHBXXXFP. For the other microcoputers, please refer to the latest datasheets on the English document CD-ROM or our Web site.

Procedure

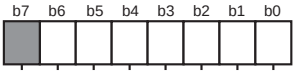


EOL announced

APPENDIX

Appendix 3. Control registers

UART2 transmit/receive mode register



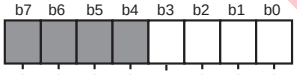
UART2 transmit/receive mode register (address 64_{16})

Bit	Bit name	Functions	At reset	RW
0	Serial I/O mode selection bits **(Note 1)**	b2 b1 b0 0 0 0: Serial I/O is ignored. (P7 functions as a programmable I/O port) 0 0 1: Clock synchronous serial I/O mode 0 1 0: } Do not select. 0 1 1: } 1 0 0: UART mode (Transfer data length = 7 bits) 1 0 1: UART mode (Transfer data length = 8 bits) 1 1 0: UART mode (Transfer data length = 9 bits) 1 1 1: Do not select.	0	RW
1 @			0	RW
2 @			0	RW
3	Internal/External clock selection bit	0: Internal clock 1: External clock	0	RW
4	Stop bit length selection bit (Valid in the UART mode.) **(Note 2)**	0: One stop bit 1: Two stop bits	0	RW
5	Odd/Even Parity selection bit (Valid in the UART mode when the parity enable bit = "1".) **(Note 2)**	0: Odd parity 1: Even parity	0	RW
6	Parity enable bit (Valid in the UART mode.) **(Note 2)**	0: Parity is disabled. 1: Parity is enabled.	0	RW
7	Not implemented.		Un-defined	—

Notes 1: By specifying these bits, an A-D conversion interrupt or a UART2 transmit/receive interrupt is selected.
When bits 2 to 0 = "000_2," an A-D conversion interrupt is selected. When bits 2 to 0 = "001_2" or "100_2 to 111_2," a UART2 transmit/receive interrupt is selected.
2: In the clock synchronous serial I/O mode, bits 4 to 6 are ignored. (They may be "0" or "1.")

EOL announced

UART2 transmit/receive control register 0

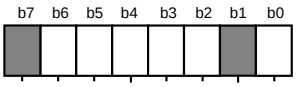


UART2 transmit/receive control register 0 (address 68_{16})

Bit	Bit name	Functions	At reset	RW
0	BRG count source selection bits	b1 b0 0 0: Clock f_2 0 1: Clock f_{16} 1 0: Clock f_{64} 1 1: Clock f_{512}	0	RW
1 @			0	RW
2	$\overline{CTS}$ enable bit	0: The $\overline{CTS}$ function is enabled. 1: The $\overline{CTS}$ function is disabled. ($P8_0$ and $P8_4$ function as programmable I/O ports.)	0	RW
3	Transmission register empty flag	0: Data is present in the transmission register. (Transmission is in progress.) 1: No data is present in the transmission @ @ register. (Transmission is completed.)	1	RO
7 to 4	Not implemented.		Un-defined	[

Clocks f_2, f_{16}, f_{64}, and f_{512}: Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Oscillation circuit control register 0



Oscillation circuit control register 0 (address $6C_{16}$)

Bit	Bit name	Functions	At reset	RW
0	X_{COUT} drivability selection bit	0: Drivability "LOW" 1: Drivability "HIGH"	1	RW (**Note 1**)
1	Not implemented.		Un-defined	–
2	Main clock stop bit	0: Main clock oscillation or external clock input is available. 1: Main clock oscillation or external clock input is stopped.	0	RW (**Note 1**)
3	System clock selection bit	When the port-Xc selection bit = "0," 0: Main clock 1: Main clock divided by 8 When the port-Xc selection bit = "1," 0: Main clock 1: Sub clock	0	RW (**Note 2**)
4	Port-Xc selection bit	0: Operate as I/O ports ($P7_7$, $P7_6$). 1: Operate as pins X_{CIN} and X_{COUT}.	0	RW (**Notes 2 and 3**)
5	System clock stop bit at wait state **(Note 4)**	0: Operates in the wait mode. 1: Stopped in the wait mode.	0	RW
6	Signal output disable selection bit	0: Output is enabled. (Refer to **Tables 12.1.2 and 12.1.5**) 1: Output is disabled.	0	RW
7	Not implemented.		Un-defined	–

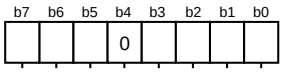
Notes 1: Nothing can be written to this bit after reset. Writing to this bit is enabled when the port-Xc selection bit = "1."
2: When selecting the sub clock as the system clock, set bit 3 to "1" after setting bit 4 to "1." If the above settings are performed simultaneously, in other words, performed by executing only one instruction, only bit 3 is set to "1."
3: Although this bit can be set to "1," it cannot be cleared to "0" after this bit is once set to "1."
4: When setting the system clock stop bit at wait state to "1," perform it immediately before the **WIT** instruction is executed. Furthermore, clear this bit to "0" immediately after the wait mode is terminated.

EOL announced

APPENDIX

Appendix 3. Control registers

Port function control register



Port function control register (address $6D_{16}$)

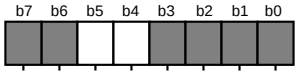
Bit	Bit name	Functions	At reset	RW
0	Standby state selection bit	0: Pins P0 to P3 are used for the external bus output. 1: Pins P0 to P3 are used for the port output.	0	RW
1	Sub-clock output selection bit/ Timer B2 clock source selection bit	•Port-X_C selection bit* = "0" (when the sub clock is not used) Timer B2 (event counter mode) clock source selection **(Note 1)** 0: $TB2_{IN}$ input (event counter mode) 1: Main clock divided by 32 (clock timer) •Port-X_C selection bit = "1" (when the sub clock is used) Sub-clock output selection 0: Pin $P6_7/TB2_{IN}/\phi_{SUB}$ functions as a programmable I/O port. 1: Sub clock ϕ_{SUB} is output from pin $P6_7/TB2_{IN}/\phi_{SUB}$.	0	RW
2	Timer B1 internal connect selection bit **(Note 2)**	0: No internal connection 1: Internal connection with timer B2	0	RW
3	Port P6 pull-up selection bit 0	0: No pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$ 1: With pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$	0	RW
4	Must be fixed to "0."		0	RW
5	Port P6 pull-up selection bit 1	•Key input interrupt selection bit = "0" 0: No pull-up for pin $P6_4/\overline{INT_2}$ 1: With pull-up for pin $P6_4/\overline{INT_2}$ •Key input interrupt selection bit = "1" 0: Pin $P6_4/\overline{INT_2}$ is a port with no pull-up. 1: Pin $P6_4/\overline{INT_2}$ is an input pin with pull-up and is used for the key input interrupt.	0	RW
6	Port P5 pull-up selection bit	0: No pull-up for pins $P5_4/TA2_{OUT}/\overline{KI_0}$ to $P5_7/TA3_{IN}/\overline{KI_3}$ 1: With pull-up for pins $P5_4/TA2_{OUT}/\overline{KI_0}$ to $P5_7/TA3_{IN}/\overline{KI_3}$	0	RW
7	Key input interrupt selection bit	0: $\overline{INT_2}$ interrupt 1: Key input interrupt	0	RW

Port-Xc selection bit* : Bit 4 of the oscillation circuit control register 0 (address $6C_{16}$)

Notes 1: When the port-Xc selection bit = "0" and timer B2 operates in the timer mode or the pulse period /pulse width measurement mode, bit 1 is invalid.
2: When timer B1 operates in the event counter mode, bit 2 is valid.

EOL announced

Serial transmit control register



Serial transmit control register (address $6E_{16}$)

Bit	Bit name	Functions	At reset	RW
3 to 0	Not implemented.		Un-defined	—
4	Transmission clock output pin selection bits (Valid only in the clock synchronous serial I/O mode.) **(Note)**	b5 b4 0 0: One transfer clock output pin (CLK_0) 0 1: } Multiple transfer clock output pins 1 0: } 1 1: }	0	RW
5			0	RW
7, 6	Not implemented. Value "0" is read out from here.		0	—

✺ When using multiple transfer clock output pins, satisfy the following conditions:

- Serial I/O mode selection bits (bits 2 to 0 at address 30_{16}) = "001_2"
- Internal/external clock selection bit (bit 3 at address 30_{16}) = "0"
- $\overline{CTS}/\overline{RTS}$ enable bit (bit 4 at address 34_{16}) = "1"
- Receive enable bit (bit 2 at address 35_{16}) = "0" (for cases ① and ② in Table 8.3.4)
- Transmission clock output pin selection bits = "01_2", "10_2", or "11_2" (Refer to **Table 8.3.3**.)

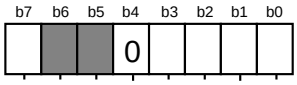
Note: Bits 4 and 5 are ignored in the UART mode. (They may be "0" or "1.")

EOL announced

APPENDIX

Appendix 3. Control registers

Oscillation circuit control register 1



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 3)**	Ignored in the mask ROM and external ROM versions.		0	RW
	Must be fixed to "1" in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to "0" **(Note 2)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing "1" to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 10.2.3.
2: The case where data "01010101_2" is written with the procedure shown in Figure 10.2.3 is not included.
3: In the 7735 Group, fix this bit to "0."

• When performing clock prescaler reset

Write data "80_{16}." (**LDM** instruction)

• When writing to bits 0 to 3

Write data "01010101_2." (**LDM** instruction)

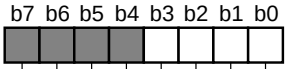
Write data "$00001XXX_2$." (**LDM** instruction)

Next instruction

(b3 in Figure 10.2.2) (b2 to b0 in Figure 10.2.2)

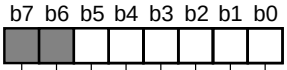
EOL announced

Interrupt control register



A-D/UART2 trans./rece., UART0 and 1 transmission, UART0 and 1 receive, Timers A0 to A4, Timers B0 to B2 interrupt control registers (addresses 7016 to 7C16)

Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2b1b0 0 0 0 : Level 0 (Interrupt is disabled.) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
4	Not implemented.		Un-defined	—
5				
6				
7				



$\overline{INT0}$, $\overline{INT1}$, and $\overline{INT2}$/Key input interrupt control registers (addresses 7D16 to 7F16)

Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2b1b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit **(Note)**	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
4	Polarity selection bit	0: Interrupt request bit is set to "1" at "H" level when level sense is selected; this bit is set to "1" at falling edge when edge sense is selected. 1: Interrupt request bit is set to "1" at "L" level when level sense is selected; this bit is set to "1" at rising edge when level sense is selected.	0	RW
5	Level sense/Edge sense selection bit	0: Edge sense 1: Level sense	0	RW
6	Not implemented.		Un-defined	—
7				

Note: The interrupt request bits of $\overline{INT0}$ to $\overline{INT2}$/Key input interrupts are ignored when the level sense is selected.

EOL announced

APPENDIX

Appendix 4. Package outlines

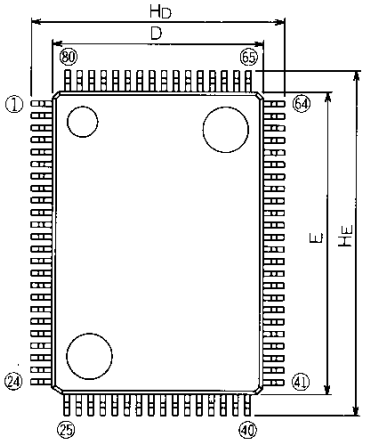
Appendix 4. Package outlines

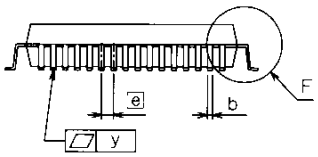
80P6N−A

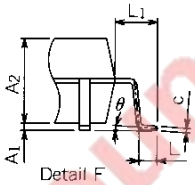
Plastic 80pin 14×20mm body QFP

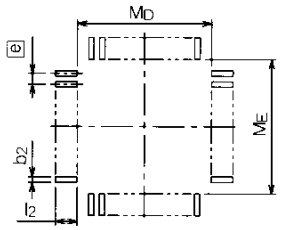
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	—	1.58	Alloy 42

Scale : 2/1









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.8	—
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	—	1.4	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.5	—
l_2	1.3	—	—
M_D	—	14.6	—
M_E	—	20.6	—

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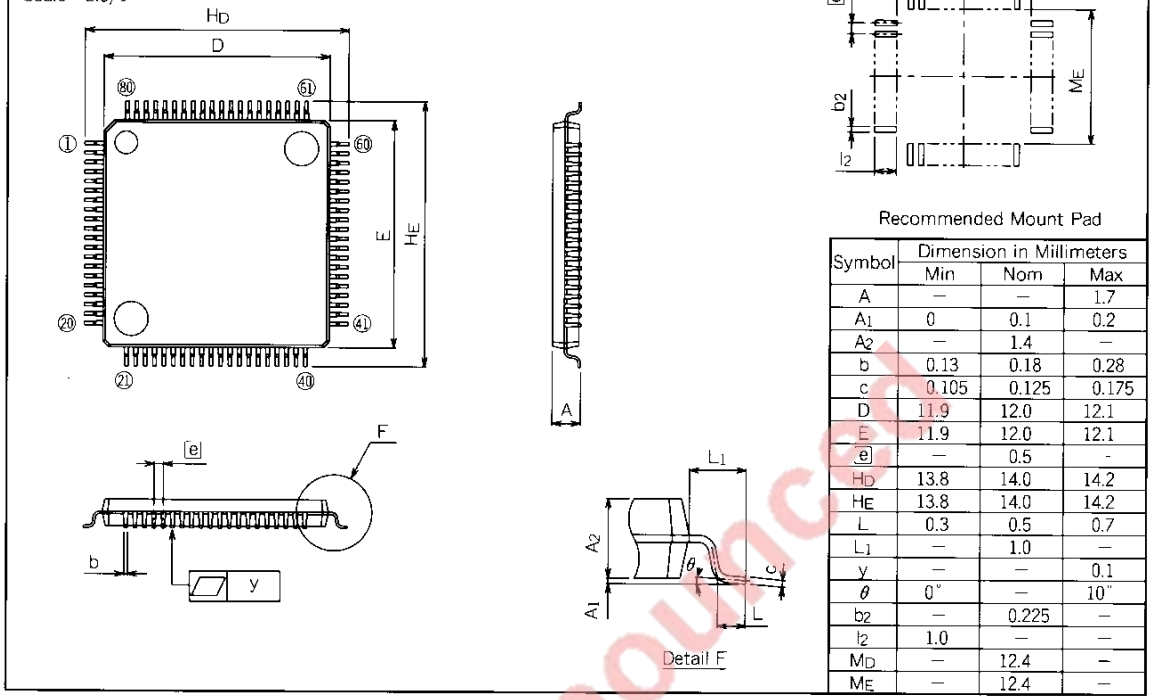
80P6D−A — Plastic 80pin 12×12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.50		0.44	Alloy 42

Scale : 2.5/1



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	—	0.5	-
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	—	1.0	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	1.0	—	—
M_D	—	12.4	—
M_E	—	12.4	—

EOL announced

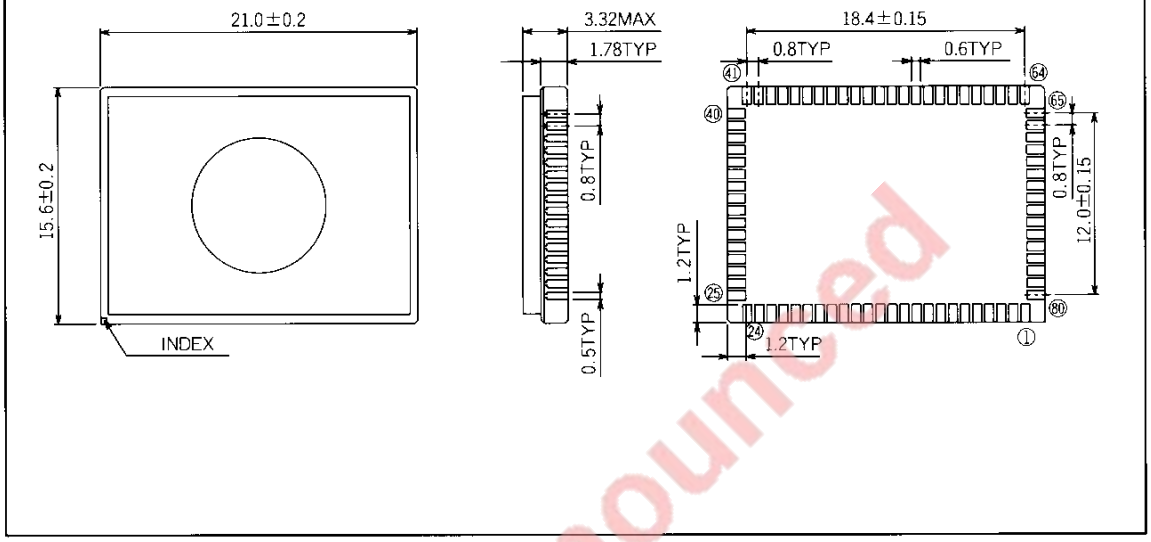
APPENDIX

Appendix 4. Package outlines

80D0 Glass seal 80pin QFN

EIAJ Package Code	JEDEC Code	Weight(g)
—	—	

Scale : 2/1



EOL announced

Appendix 5. Hexadecimal instruction code table

INSTRUCTION CODE TABLE-1

D7–D4 \ D3–D0	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA A,(DIR,X)		ORA A,SR	SEB DIR,b	ORA A,DIR	ASL DIR	ORA A,L(DIR)	PHP	ORA A,IMM	ASL A	PHD	SEB ABS,b	ORA A,ABS	ASL ABS	ORA A,ABL
0001	1	BPL	ORA A,(DIR),Y	ORA A,(DIR)	ORA A,(SR),Y	CLB DIR,b	ORA A,DIR,X	ASL DIR,X	ORA A,L(DIR),Y	CLC	ORA A,ABS,Y	DEC A	TAS	CLB ABS,b	ORA A,ABS,X	ASL ABS,X	ORA A,ABL,X
0010	2	JSR ABS	AND A,(DIR,X)	JSR ABL	AND A,SR	BBS DIR,b,R	AND A,DIR	ROL DIR	AND A,L(DIR)	PLP	AND A,IMM	ROL A	PLD	BBS ABS,b,R	AND A,ABS	ROL ABS	AND A,ABL
0011	3	BMI	AND A,(DIR),Y	AND A,(DIR)	AND A,(SR),Y	BBC DIR,b,R	AND A,DIR,X	ROL DIR,X	AND A,L(DIR),Y	SEC	AND A,ABS,Y	INC A	TSA	BBC ABS,b,R	AND A,ABS,X	ROL ABS,X	AND A,ABL,X
0100	4	RTI	EOR A,(DIR,X)	**Note 1**	EOR A,SR	MVP	EOR A,DIR	LSR DIR	EOR A,L(DIR)	PHA	EOR A,IMM	LSR A	PHG	JMP ABS	EOR A,ABS	LSR ABS	EOR A,ABL
0101	5	BVC	EOR A,(DIR),Y	EOR A,(DIR)	EOR A,(SR),Y	MVN	EOR A,DIR,X	LSR DIR,X	EOR A,L(DIR),Y	CLI	EOR A,ABS,Y	PHY	TAD	JMP ABL	EOR A,ABS,X	LSR ABS,X	EOR A,ABL,X
0110	6	RTS	ADC A,(DIR,X)	PER	ADC A,SR	LDM DIR	ADC A,DIR	ROR DIR	ADC A,L(DIR)	PLA	ADC A,IMM	ROR A	RTL	JMP (ABS)	ADC A,ABS	ROR ABS	ADC A,ABL
0111	7	BVS	ADC A,(DIR),Y	ADC A,(DIR)	ADC A,(SR),Y	LDM DIR,X	ADC A,DIR,X	ROR DIR,X	ADC A,L(DIR),Y	SEI	ADC A,ABS,Y	PLY	TDA	JMP (ABS,X)	ADC A,ABS,X	ROR ABS,X	ADC A,ABL,X
1000	8	BRA REL	STA A,(DIR,X)	BRA REL	STA A,SR	STY DIR	STA A,DIR	STX DIR	STA A,L(DIR)	DEY	**Note 2**	TXA	PHT	STY ABS	STA A,ABS	STX ABS	STA A,ABL
1001	9	BCC	STA A,(DIR),Y	STA A,(DIR)	STA A,(SR),Y	STY DIR,X	STA A,DIR,X	STX DIR,Y	STA A,L(DIR),Y	TYA	STA A,ABS,Y	TXS	TXY	LDM ABS	STA A,ABS,X	LDM ABS,X	STA A,ABL,X
1010	A	LDY IMM	LDA A,(DIR,X)	LDX IMM	LDA A,SR	LDY DIR	LDA A,DIR	LDX DIR	LDA A,L(DIR)	TAY	LDA A,IMM	TAX	PLT	LDY ABS	LDA A,ABS	LDX ABS	LDA A,ABL
1011	B	BCS	LDA A,(DIR),Y	LDA A,(DIR)	LDA A,(SR),Y	LDY DIR,X	LDA A,DIR,X	LDX DIR,Y	LDA A,L(DIR),Y	CLV	LDA A,ABS,Y	TSX	TYX	LDY ABS,X	LDA A,ABS,X	LDX ABS,Y	LDA A,ABL,X
1100	C	CPY IMM	CMP A,(DIR,X)	CLP IMM	CMP A,SR	CPY DIR	CMP A,DIR	DEC DIR	CMP A,L(DIR)	INY	CMP A,IMM	DEX	WIT	CPY ABS	CMP A,ABS	DEC ABS	CMP A,ABL
1101	D	BNE	CMP A,(DIR),Y	CMP A,(DIR)	CMP A,(SR),Y	PEI	CMP A,DIR,X	DEC DIR,X	CMP A,L(DIR),Y	CLM	CMP A,ABS,Y	PHX	STP	JMP L(ABS)	CMP A,ABS,X	DEC ABS,X	CMP A,ABL,X
1110	E	CPX IMM	SBC A,(DIR,X)	SEP IMM	SBC A,SR	CPX DIR	SBC A,DIR	INC DIR	SBC A,L(DIR)	INX	SBC A,IMM	NOP	PSH	CPX ABS	SBC A,ABS	INC ABS	SBC A,ABL
1111	F	BEQ	SBC A,(DIR),Y	SBC A,(DIR)	SBC A,(SR),Y	PEA	SBC A,DIR,X	INC DIR,X	SBC A,L(DIR),Y	SEM	SBC A,ABS,Y	PLX	PUL	JSR (ABS,X)	SBC A,ABS,X	INC ABS,X	SBC A,ABL,X

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Notes 1: 42_{16} specifies the contents of the INSTRUCTION CODE TABLE-2.
About the second word's codes, refer to the INSTRUCTION CODE TABLE-2.
2: 89_{16} specifies the contents of the INSTRUCTION CODE TABLE-3.
About the second word's codes, refer to the INSTRUCTION CODE TABLE-2.

APPENDIX

Appendix 5. Hexadecimal instruction code table

INSTRUCTION CODE TABLE-2 (The first word's code of each instruction is 42_{16})

D7–D4 \ D3–D0	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		ORA B,(DIR,X)		ORA B,SR		ORA B,DIR		ORA B,L(DIR)		ORA B,IMM	ASL B			ORA B,ABS		ORA B,ABL
0001	1		ORA B,(DIR),Y	ORA B,(DIR)	ORA B,(SR),Y		ORA B,DIR,X		ORA B,L(DIR),Y		ORA B,ABS,Y	DEC B	TBS		ORA B,ABS,X		ORA B,ABL,X
0010	2		AND B,(DIR,X)		AND B,SR		AND B,DIR		AND B,L(DIR)		AND B,IMM	ROL B			AND B,ABS		AND B,ABL
0011	3		AND B,(DIR),Y	AND B,(DIR)	AND B,(SR),Y		AND B,DIR,X		AND B,L(DIR),Y		AND B,ABS,Y	INC B	TSB		AND B,ABS,X		AND B,ABL,X
0100	4		EOR B,(DIR,X)		EOR B,SR		EOR B,DIR		EOR B,L(DIR)	PHB	EOR B,IMM	LSR B			EOR B,ABS		EOR B,ABL
0101	5		EOR B,(DIR),Y	EOR B,(DIR)	EOR B,(SR),Y		EOR B,DIR,X		EOR B,L(DIR),Y		EOR B,ABS,Y		TBD		EOR B,ABS,X		EOR B,ABL,X
0110	6		ADC B,(DIR,X)		ADC B,SR		ADC B,DIR		ADC B,L(DIR)	PLB	ADC B,IMM	ROR B			ADC B,ABS		ADC B,ABL
0111	7		ADC B,(DIR),Y	ADC B,(DIR)	ADC B,(SR),Y		ADC B,DIR,X		ADC B,L(DIR),Y		ADC B,ABS,Y		TDB		ADC B,ABS,X		ADC B,ABL,X
1000	8		STA B,(DIR,X)		STA B,SR		STA B,DIR		STA B,L(DIR)			TXB			STA B,ABS		STA B,ABL
1001	9		STA B,(DIR),Y	STA B,(DIR)	STA B,(SR),Y		STA B,DIR,X		STA B,L(DIR),Y	TYB	STA B,ABS,Y				STA B,ABS,X		STA B,ABL,X
1010	A		LDA B,(DIR,X)		LDA B,SR		LDA B,DIR		LDA B,L(DIR)	TBY	LDA B,IMM	TBX			LDA B,ABS		LDA B,ABL
1011	B		LDA B,(DIR),Y	LDA B,(DIR)	LDA B,(SR),Y		LDA B,DIR,X		LDA B,L(DIR),Y		LDA B,ABS,Y				LDA B,ABS,X		LDA B,ABL,X
1100	C		CMP B,(DIR,X)		CMP B,SR		CMP B,DIR		CMP B,L(DIR)		CMP B,IMM				CMP B,ABS		CMP B,ABL
1101	D		CMP B,(DIR),Y	CMP B,(DIR)	CMP B,(SR),Y		CMP B,DIR,X		CMP B,L(DIR),Y		CMP B,ABS,Y				CMP B,ABS,X		CMP B,ABL,X
1110	E		SBC B,(DIR,X)		SBC B,SR		SBC B,DIR		SBC B,L(DIR)		SBC B,IMM				SBC B,ABS		SBC B,ABL
1111	F		SBC B,(DIR),Y	SBC B,(DIR)	SBC B,(SR),Y		SBC B,DIR,X		SBC B,L(DIR),Y		SBC B,ABS,Y				SBC B,ABS,X		SBC B,ABL,X

EOL announced

Appendix 5. Hexadecimal instruction code table

INSTRUCTION CODE TABLE-3 (The first word's code of each instruction is 89_{16})

D_7–D_4 \ D_3–D_0	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		MPY (DIR,X)		MPY SR		MPY DIR		MPY L(DIR)		MPY IMM				MPY ABS		MPY ABL
0001	1		MPY (DIR),Y	MPY (DIR)	MPY (SR),Y		MPY DIR,X		MPY L(DIR),Y		MPY ABS,Y				MPY ABS,X		MPY ABL,X
0010	2		DIV (DIR,X)		DIV SR		DIV DIR		DIV L(DIR)	XAB	DIV IMM				DIV ABS		DIV ABL
0011	3		DIV (DIR),Y	DIV (DIR)	DIV (SR),Y		DIV DIR,X		DIV L(DIR),Y		DIV ABS,Y				DIV ABS,X		DIV ABL,X
0100	4										RLA IMM						
0101	5																
0110	6																
0111	7																
1000	8																
1001	9																
1010	A																
1011	B																
1100	C			LDT IMM													
1101	D																
1110	E																
1111	F																

EOL announced

APPENDIX

Appendix 6. Machine instructions

Appendix 6. Machine instructions

Symbol	Functions	Details	Addressing modes																																	
			IMP			IMM			A			DIR			DIR,b			DIR,X			DIR,Y			(DIR)			(DIR,X)			(DIR),Y					
			op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#			
ADC **(Notes 1,2)**	Acc,C←Acc+M+C	Adds the carry, the accumulator and the memory contents.The result is entered into the accumulator. When the D flag is “0,” binary additions is done, and when the D flag is “1,” decimal addition is done.				69	2	2				65	4	2				75	5	2				72	6	2	61	7	2	71	8	2			
						42 69	4	3				42 65	6	3				42 75	7	3				42 72	8	3	42 61	9	3	42 71	10	3			
AND **(Notes 1,2)**	Acc←Acc∧M	Obtains the logical product of the contents of the accumulator and the contents of the memory . The result is entered into the accumulator.				29	2	2				25	4	2				35	5	2				32	6	2	21	7	2	31	8	2			
						42 29	4	3				42 25	6	3				42 35	7	3				42 32	8	3	42 21	9	3	42 31	10	3			
ASL **(Note 1)**	m=0 C ← b15 ··· b0 ←0 m=1 C ← b7 ··· b0 ←0	Shifts the accumulator or the memory contents one bit to the left. “0” is entered into bit 0 of the accumulator or the memory. The contents of bit 15 (bit 7 when the m flag is “1”) of the accumulator or memory before shift is entered into the C flag.							0A	2	1	06	7	2				16	7	2															
									42 0A	4	2																									
BBC **(Notes 3,5)**	Mb=0?	Tests the specified bit of the memory. Branches when all the contents of the specified bit is “0.”																																		
BBS **(Notes 3,5)**	Mb=1?	Tests the specified bit of the memory. Branches when all the contents of the specified bit is “1.”																																		
BCC **(Note 3)**	C=0?	Branches when the contents of the C flag is “0.”																																		
BCS **(Note 3)**	C=1?	Branches when the contents of the C flag is “1.”																																		
BEQ **(Note 3)**	Z=1?	Branches when the contents of the Z flag is “1.”																																		
BMI **(Note 3)**	N=1?	Branches when the contents of the N flag is “1.”																																		
BNE **(Note 3)**	Z=0?	Branches when the contents of the Z flag is “0.”																																		
BPL **(Note 3)**	N=0?	Branches when the contents of the N flag is “0.”																																		
BRA **(Note 4)**	PC←PC±offset PG←PG+1 (when carry occurs) PG←PG–1 (when borrow occurs)	Jumps to the address indicated by the program counter plus the offset value.																																		
BRK	PC←PC+2 M(S)←PG S←S–1 M(S)←PCH S←S–1 M(S)←PCL S←S–1 M(S)←PSH S←S–1 M(S)←PSL S←S–1 I←1 PCL←ADL PCH←ADH PG←00$_{16}$	Executes software interruption.	00	15	2																															
BVC (Note 3)	V=0?	Branches when the contents of the V flag is “0.”																																		
BVS **(Note 3)**	V=1?	Branches when the contents of the V flag is “1.”																																		
CLB (Note 5)	Mb←0	Makes the contents of the specified bit in the memory “0.”													14	8	3																			
CLC	C←0	Makes the contents of the C flag “0.”	18	2	1																															
CLI	I←0	Makes the contents of the I flag “0.”	58	2	1																															
CLM	m←0	Makes the contents of the m flag “0.”	D8	2	1																															
CLP	PSb←0	Specifies the bit position in the processor status register by the bit pattern of the second byte in the instruction, and sets “0” in that bit.				C2	4	2																												
CLV	V←0	Makes the contents of the V flag “0.”	B8	2	1																															
CMP **(Notes 1,2)**	Acc–M	Compares the contents of the accumulator with the contents of the memory.				C9	2	2				C5	4	2				D5	5	2				D2	6	2	C1	7	2	D1	8	2			
						42 C9	4	3				42 C5	6	3				42 D5	7	3				42 D2	8	3	42 C1	9	3	42 D1	10	3			

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Symbol	Functions	Details	Addressing modes																																		
			IMP			IMM			A			DIR			DIR,b			DIR,X			DIR,Y			(DIR)			(DIR,X)			(DIR),Y								
			op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#						
CPX **(Note 2)**	X–M	Compares the contents of the index register X with the contents of the memory.				E0	2	2				E4	4	2																							
CPY **(Note 2)**	Y–M	Compares the contents of the index register Y with the contents of the memory.				C0	2	2				C4	4	2																							
DEC **(Note 1)**	Acc←Acc–1 or M←M–1	Decrements the contents of the accumulator or memory by 1.							1A	2	1	C6	7	2				D6	7	2																	
									42 1A	4	2																											
DEX	X←X–1	Decrements the contents of the index register X by 1.	CA	2	1																																
DEY	Y←Y–1	Decrements the contents of the index register Y by 1.	88	2	1																																
DIV **(Notes 2,10)**	A(quotient)←B,A/M B(remainder)	The numeral that places the contents of accumulator B to the higher order and the contents of accumulator A to the lower order is divided by the contents of the memory. The quotient is entered into accumulator A and the remainder into accumulator B.				89 29	27	3				89 25	29	3				89 35	30	3				89 32	31	3	89 21	32	3	89 31	33	3						
EOR **(Notes 1,2)**	Acc←Acc▽M	Logical exclusive sum is obtained of the contents of the accumulator and the contents of the memory. The result is placed into the accumulator.				49	2	2				45	4	2				55	5	2				52	6	2	41	7	2	51	8	2						
						42 49	4	3				42 45	6	3				42 55	7	3				42 52	8	3	42 41	9	3	42 51	10	3						
INC **(Note 1)**	Acc←Acc+1 or M←M+1	Increments the contents of the accumulator or memory by 1.							3A	2	1	E6	7	2				F6	7	2																	
									42 3A	4	2																											
INX	X←X+1	Increments the contents of the index register X by 1.	E8	2	1																																
INY	Y←Y+1	Increments the contents of the index register Y by 1.	C8	2	1																																
JMP	ABS PCL←ADL PCH←ADH ABL PCL←ADL PCH←ADH PG←ADG (ABS) PCL←(ADH, ADL) PCH←(ADH,ADL+1) L(ABS) PCL←(ADH, ADL) PCH←(ADH, ADL+1) PG←(ADH, ADL+2) (ABS, X) PCL←(ADH, ADL+X) PCH←(ADH, ADL+X +1)	Places a new address into the program counter and jumps to that new address.																																			
JSR	ABS M(S)←PCH S←S–1 M(S)←PCL S←S–1 PCL←ADL PCH←ADH ABL M(S)←PG S←S–1 M(S)←PCH S←S–1 M(S)←PCL S←S–1 PCL←ADL PCH←ADH PG←ADG (ABS, X) M(S)←PCH S←S–1 M(S)←PCL S←S–1 PCL←(ADH, ADL+X) PCH←(ADH, ADL+X +1)	Saves the contents of the program counter (also the contents of the program bank register for ABL) into the stack, and jumps to the new address.																																			

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Symbol	Functions	Details	Addressing modes																															
			IMP			IMM			A			DIR			DIR,b			DIR,X			DIR,Y			(DIR)			(DIR,X)			(DIR),Y		
			op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#
LDA **(Notes 1,2)**	Acc←M	Enters the contents of the memory into the accummulator.				A9	2	2				A5	4	2				B5	5	2				B2	6	2	A1	7	2	B1	8	2
						42 A9	4	3				42 A5	6	3				42 B5	7	3				42 B2	8	3	42 A1	9	3	42 B1	10	3
LDM **(Note 5)**	M←IMM	Enters the immediate vaiue into the memory.										64	4	3				74	5	3												
LDT	DT←IMM	Enters the immediate value into the data bank regiater.				89 C2	5	3																								
LDX **(Note 2)**	X←M	Enters the contents of the memory into index register X.				A2	2	2				A6	4	2							B6	5	2									
LDY **(Note 2)**	Y←M	Enters the contents of the memory into index register Y.				A0	2	2				A4	4	2				B4	5	2												
LSR **(Note 1)**	m=0 0 → b15 ··· b0 →C m=1 0 → b7 ··· b0 →C	Shifts the contents of the accumulator or the contents of the memory one bit to the right. The bit 0 of the accumulator or the memory is entered into the C flag. “0” is entered into bit 15 (bit 7 when the m flag is “1.”)							4A	2	1	46	7	2				56	7	2												
									42 4A	4	2																					
MPY **(Notes 2,11)**	B, A←A✻M	Multiplies the contents of accumulator A and the contents of the memory. The higher order of the result of operation are entered into accumulator B, and the lower order into accumulator A.				89 09	16	3				89 05	18	3				89 15	19	3				89 12	20	3	89 01	21	3	89 11	22	3
MVN **(Note 8)**	Mn+i←Mm+i	Transmits the data block. The transmission is done from the lower order address of the block.																														
MVP **(Note 9)**	Mn–i←Mm–i	Transmits the data block. Transmission is done form the higher order address of the data block.																														
NOP	PC←PC+1	Advances the program counter, but pertorms nothing else.	EA	2	1																											
ORA **(Notes 1,2)**	Acc←AccVM	Logical sum per bit of the contents of the accumulator and the contents of the memory is obtained. The result is entered into the accumulator.				09	2	2				05	4	2				15	5	2				12	6	2	01	7	2	11	8	2
						42 09	4	3				42 05	6	3				42 15	7	3				42 12	8	3	42 01	9	3	42 11	10	3
PEA	M(S)←IMM2 S←S–1 M(S)←IMM1 S←S–1	The 3rd and the 2nd bytes of the instruction are saved into the stack, in this order.																														
PEI	M(S)←M((DPR)+IMM +1) S←S–1 M(S)←M((DPR)+IMM) S←S–1	Specifies 2 sequential bytes in the direct page in the 2nd byte of the instruction, and saves the contents into the stack.																														
PER	EAR←PC+IMM2,IMM1 M(S)←EARH S←S–1 M(S)←EARL S←S–1	Regards the 2nd and 3rd bytes of the instruction as 16-bit numerals, adds them to the program counter, and saves the result into the stack.																														
PHA	m=0 M(S)←AH S←S–1 M(S)←AL S←S–1 m=1 M(S)←AL S←S–1	Saves the contents of accumulator A into the stack.																														
PHB	m=0 M(S)←BH S←S–1 M(S)←BL S←S–1 m=1 M(S)←BL S←S–1	Saves the contents of accumuator B into the stack.																														

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Symbol	Functions	Details	Addressing modes																																		
			IMP			IMM			A			DIR			DIR,b			DIR,X			DIR,Y			(DIR)			(DIR,X)			(DIR),Y								
			op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#						
PHD	M(S)←DPRH S←S–1 M(S)←DPRL S←S–1	Saves the contents of the direct page register into the stack.																																			
PHG	M(S)←PG S←S–1	Saves the contents of the program bank register into the stack.																																			
PHP	M(S)←PSH S←S–1 M(S)←PSL S←S–1	Saves the contents of the program status register into the stack.																																			
PHT	M(S)←DT S←S–1	Saves the contents of the data bank register into the stack.																																			
PHX	x=0 M(S)←XH S←S–1 M(S)←XL S←S–1 x=1 M(S)←XL S←S–1	Saves the contents of the index register X into the stack.																																			
PHY	x=0 M(S)←YH S←S–1 M(S)←YL S←S–1 x=1 M(S)←YL S←S–1	Saves the contents of the index register Y into the stack.																																			
PLA	m=0 S←S+1 AL←M(S) S←S+1 AH←M(S) m=1 S←S+1 AL←M(S)	Restores the contents of the stack on the accumulator A.																																			
PLB	m=0 S←S+1 BL←M(S) S←S+1 BH←M(S) m=1 S←S+1 BL←M(S)	Restores the contents of the stack on the accumulator B.																																			
PLD	S←S+1 DPRL←M(S) S←S+1 DPRH←M(S)	Restores the contents of the stack on the direct page register.																																			
PLP	S←S+1 PSL←M(S) S←S+1 PSH←M(S)	Restores the contents of the stack on the processor status register.																																			
PLT	S←S+1 DT←M(S)	Restores the contents of the stack on the data bank register.																																			
PLX	x=0 S←S+1 XL←M(S) S←S+1 XH←M(S) x=1 S←S+1 XL←M(S)	Restores the contents of the stack on the index register X.																																			

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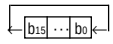
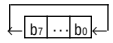
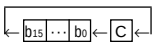
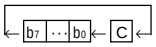
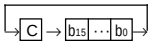
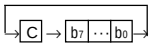
Symbol	Functions	Details	Addressing modes																																		
			IMP			IMM			A			DIR			DIR,b			DIR,X			DIR,Y			(DIR)			(DIR,X)			(DIR),Y								
			op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#						
PLY	x=0 S←S+1 YL←M(S) S←S+1 YH←M(S) x=1 S←S+1 YL←M(S)	Restores the contents of the stack on the index register Y.																																			
PSH **(Note 6)**	M(S)←A, B, X···	Saves the registers among accumulator, index register, direct page register, data bank register, program bank register, or processor status register, specified by the bit pattern of the second byte of the instruction into the stack.																																			
PUL **(Note 7)**	A, B, X··←M(S)	Restores the contents of the stack to the registers among accumulator, index register, direct page register, data bank register, or processor status register, specified by the bit pattern of the second byte of the instruction.																																			
RLA **(Note 13)**	m=0 n bit rotate left  m=1 n bit rotate left 	Rotates the contents of the accumulator A, n bits to the left.				89 49	6 + i	3																															
ROL **(Note 1)**	m=0  m=1 	Links the accumulator or the memory to C flag, and rotates result to the left by 1 bit.							2A 42 2A	2 4	1 2	26	7	2				36	7	2																			
ROR **(Note 1)**	m=0  m=1 	Links the accumulator or the memory to C flag, and rotates result to the right by 1 bit.							6A 42 6A	2 4	1 2	66	7	2				76	7	2																			
RTI	S←S+1 PSL←M(S) S←S+1 PSH←M(S) S←S+1 PCL←M(S) S←S+1 PCH←M(S) S←S+1 PG←M(S)	Returns from the interruption routine.	40	11	1																																
RTL	S←S+1 PCL←M(S) S←S+1 PCH←M(S) S←S+1 PG←M(S)	Returns from the subroutine. The contents of the program bank register are also restored.	6B	8	1																																
RTS	S←S+1 PCL←M(S) S←S+1 PCH←M(S)	Returns from the subroutine. The contents of the program bank register are not restored.	60	5	1																																
SBC **(Notes 1,2)**	ACC, C←ACC–M–$\overline{C}$	Subtracts the contents of the memory and the borrow from the contents of the accumulator.				E9 42 E9	2 4	2 3				E5 42 E5	4 6	2 3				F5 42 F5	5 7	2 3				F2 42 F2	6 8	2 3	E1 42 E1	7 9	2 3	F1 42 F1	8 10	2 3						

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Symbol	Functions	Details	Addressing modes																																
			IMP			IMM			A			DIR			DIR,b			DIR,X			DIR,Y			(DIR)			(DIR,X)			(DIR),Y					
			op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#	op	n	#			
SEB **(Note 5)**	Mb←1	Makes the contents of the specified bit in the memory "1."													04	8	3																		
SEC	C←1	Makes the contents of the C flag "1."	38	2	1																														
SEI	I←1	Makes the contents of the I flag "1."	78	2	1																														
SEM	m←1	Makes the contents of the m flag "1."	F8	2	1																														
SEP	PSb←1	Set the specified bit of the processor status register's lower byte (PS_L) to "1."				E2	3	2																											
STA **(Note 1)**	M←Acc	Stores the contents of the accumulator into the memory.										85	4	2				95	5	2				92	7	2	81	7	2	91	7	2			
												42 85	6	3				42 95	7	3				42 92	9	3	42 81	9	3	42 91	9	3			
STP		Stops the oscillation of the oscillator.	DB	3	1																														
STX	M←X	Stores the contents of the index register X into the memory.										86	4	2							96	5	2												
STY	M←Y	Stores the contents of the index register Y into the memory.										84	4	2				94	5	2														
TAD	DPR←A	Transmits the contents of the accumulator A to the direct page register.	5B	2	1																														
TAS	S←A	Transmits the contents of the accumulator A to the stack pointer.	1B	2	1																														
TAX	X←A	Transmits the contents of the accumulator A to the index register X.	AA	2	1																														
TAY	Y←A	Transmits the contents of the accumulator A to the index register Y.	A8	2	1																														
TBD	DPR←B	Transmits the contents of the accumulator B to the direct page register.	42 5B	4	2																														
TBS	S←B	Transmits the contents of the accumulator B to the stack pointer.	42 1B	4	2																														
TBX	X←B	Transmits the contents of the accumulator B to the index register X.	42 AA	4	2																														
TBY	Y←B	Transmits the contents of the accumulator B to the index register Y.	42 A8	4	2																														
TDA	A←DPR	Transmits the contents of the direct page register to the accumulator A.	7B	2	1																														
TDB	B←DPR	Transmits the contents of the direct page register to the accumulator B.	42 7B	4	2																														
TSA	A←S	Transmits the contents of the stack pointer to the accumulator A.	3B	2	1																														
TSB	B←S	Transmits the contents of the stack pointer to the accumulator B.	42 3B	4	2																														
TSX	X←S	Transmits the contents of the stack pointer to the index register X.	BA	2	1																														
TXA	A←X	Transmits the contents of the index register X to the accumulator A.	8A	2	1																														
TXB	B←X	Transmits the contents of the index register X to the accumulator B.	42 8A	4	2																														
TXS	S←X	Transmits the contents of the index register X to the stack pointer.	9A	2	1																														
TXY	Y←X	Transmits the contents of the index register X to the index register Y.	9B	2	1																														
TYA	A←Y	Transmits the contents of the index register Y to the accumulator A.	98	2	1																														
TYB	B←Y	Transmits the contents of the index register Y to the accumulator B.	42 98	4	2																														
TYX	X←Y	Transmits the contents of the index register Y to the index register X.	BB	2	1																														
WIT		Stops the internal clock.	CB	3	1																														
XAB	A⇆B	Exchanges the contents of the accumulator A and the contents of the accumulator B.	89 28	6	2																														

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The number of cycles shown in the table is described in the case of the fastest mode for each instruction. The number of cycles shown in the table is calculated for DPR_L=0. The number of cycles in the addressing mode concerning the DPR when $DPR_L \neq 0$ must be incremented by 1.
The number of cycles shown in the table differs according to the bytes fetched into the instruction queue buffer, or according to whether the memory read/write address is odd or even. It also differs when the external region memory is accessed by BYTE="H."

Notes 1. The operation code at the upper row is used for accumulator A, and the operation at the lower row is used for accumulator B.

2. When setting flag m=0 to handle the data as 16-bit data in the immediate addressing mode, the number of bytes increments by 1.

3. The number of cycles increments by 2 when branching.

4. The operation code on the upper row is used for branching in the range of –128 to +127, and the operation code on the lower row is used for branching in the range of –32768 to +32767.

5. When handling 16-bit data with flag m=0, the byte in the table is incremented by 1.

6.

Type of register	A	B	X	Y	DPR	DT	PG	PS
Number of cycles	2	2	2	2	2	1	1	2

The number of cycles corresponding to the register to be pushed are added. The number of cycles when no pushing is done is 12. i_1 indicates the number of registers among A, B, X, Y, DPR, and PS to be saved, while i_2 indicates the number of registers among DT and PG to be saved.

7.

Type of register	A	B	X	Y	DPR	DT	PS
Number of cycles	3	3	3	3	4	3	3

The number of cycles corresponding to the register to be pulled are added. The number of cycles when no pulling is done is 14. i_1 indicates the number of registers among A, B, X, Y, DT, and PS to be restored, while i_2=1 when DPR is to be restored.

8. The number of cycles is the case when the number of bytes to be transferred is even.
When the number of bytes to be transferred is odd, the number is calculated as;

$$7 + (i/2) \times 7 + 4$$

Note that, (i/2) shows the integer part when i is divided by 2.

9. The number of cycles is the case when the number of bytes to be transferred is even.
When the number of bytes to be transferred is odd, the number is calculated as;

$$9 + (i/2) \times 7 + 5$$

Note that, (i/2) shows the integer part when i is divided by 2.

10. The number of cycles is the case in the 16-bit ÷ 8-bit operation. The number of cycles is incremented by 16 for 32-bit ÷ 16-bit operation.

11. The number of cycles is the case in the 8-bit × 8-bit operation. The number of cycles is incremented by 8 for 16-bit × 16-bit operation.

12. When setting flag x=0 to handle the data as 16-bit data in the immediate addressing mode, the number of bytes increments by 1.

13. When flag m is 0, the byte in the table is incremented by 1.

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Symbols in machine instructions table

Symbol	Description	Symbol	Description
IMP	Implied addressing mode	∀	Exclusive OR
IMM	Immediate addressing mode	–	Negation
A	Accumulator addressing mode	←	Movement to the arrow direction
DIR	Direct addressing mode	Acc	Accumulator
DIR, b	Direct bit addressing mode	AccH	Accumulator's upper 8 bits
DIR, X	Direct indexed X addressing mode	AccL	Accumulator's lower 8 bits
DIR, Y	Direct indexed Y addressing mode	A	Accumulator A
(DIR)	Direct indirect addressing mode	AH	Accumulator A's upper 8 bits
(DIR,X)	Direct indexed X indirect addressing mode	AL	Accumulator A's lower 8 bits
(DIR), Y	Direct indirect indexed Y addressing mode	B	Accumulator B
L (DIR)	Direct indirect long addressing mode	BH	Accumulator B's upper 8 bits
L (DIR),Y	Direct indirect long indexed Y addressing mode	BL	Accumulator B's lower 8 bits
ABS	Absolute addressing mode	X	Index register X
ABS, b	Absolute bit addressing mode	XH	Index register X's upper 8 bits
ABS, X	Absolute indexed X addressing mode	XL	Index register X's lower 8 bits
ABS, Y	Absolute indexed Y addressing mode	Y	Index register Y
ABL	Absolute long addressing mode	YH	Index register Y's upper 8 bits
ABL, X	Absolute long indexed X addressing mode	YL	Index register Y's lower 8 bits
(ABS)	Absolute indirect addressing mode	S	Stack pointer
L (ABS)	Absolute indirect long addressing mode	PC	Program counter
(ABS, X)	Absolute indexed X indirect addressing mode	PCH	Program counter's upper 8 bits
STK	Stack addressing mode	PCL	Program counter's lower 8 bits
REL	Relative addressing mode	PG	Program bank register
DIR, b, REL	Direct bit relative addressing mode	DT	Data bank register
ABS, b, REL	Absolute bit relative addressing mode	DPR	Direct page register
SR	Stack pointer relative addressing mode	DPRH	Direct page register's upper 8 bits
(SR), Y	Stack pointer relative indirect indexed Y addressing mode	DPRL	Direct page register's lower 8 bits
		PS	Processor status register
BLK	Block transfer addressing mode	PSH	Processor status register's upper 8 bits
C	Carry flag	PSL	Processor status register's lower 8 bits
Z	Zero flag	PSb	Processor status register's b-th bit
I	Interrupt disable flag	M(S)	Contents of memory at address indicated by stack pointer
D	Decimal operation mode flag		
x	Index register length selection flag	Mb	b-th memory location
m	Data length selection flag	ADG	Value of 24-bit address's upper 8-bit (A_{23}–A_{16})
V	Overflow flag	ADH	Value of 24-bit address's middle 8-bit (A_{15}–A_8)
N	Negative flag	ADL	Value of 24-bit address's lower 8-bit (A_7–A_0)
IPL	Processor interrupt priority level	op	Operation code
+	Addition	n	Number of cycle
−	Subtraction	#	Number of byte
*	Multiplication	i	Number of transfer byte or rotation
/	Division	i_1, i_2	Number of registers pushed or pulled
∧	Logical AND		
∨	Logical OR		

EOL announced

APPENDIX

Appendix 7. Examples of handling unused pins

Appendix 7. Examples of handling unused pins

The following are examples of handling unused pins.
These are, however, just examples. In actual use, make the necessary adaptations and properly evaluate performance according to the user's application.

1. In single-chip mode

Table 1 Examples of handling unused pins in single-chip mode

Pins	Handling example
P0–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Note 1**).
$\overline{E}$	Leave this pin open.
XOUT (**Note 2**)	
AVcc	Connect this pin to pin Vcc.
AVss, VREF, BYTE	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.
For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).
2: This is applied when an external clock is input to pin XIN.

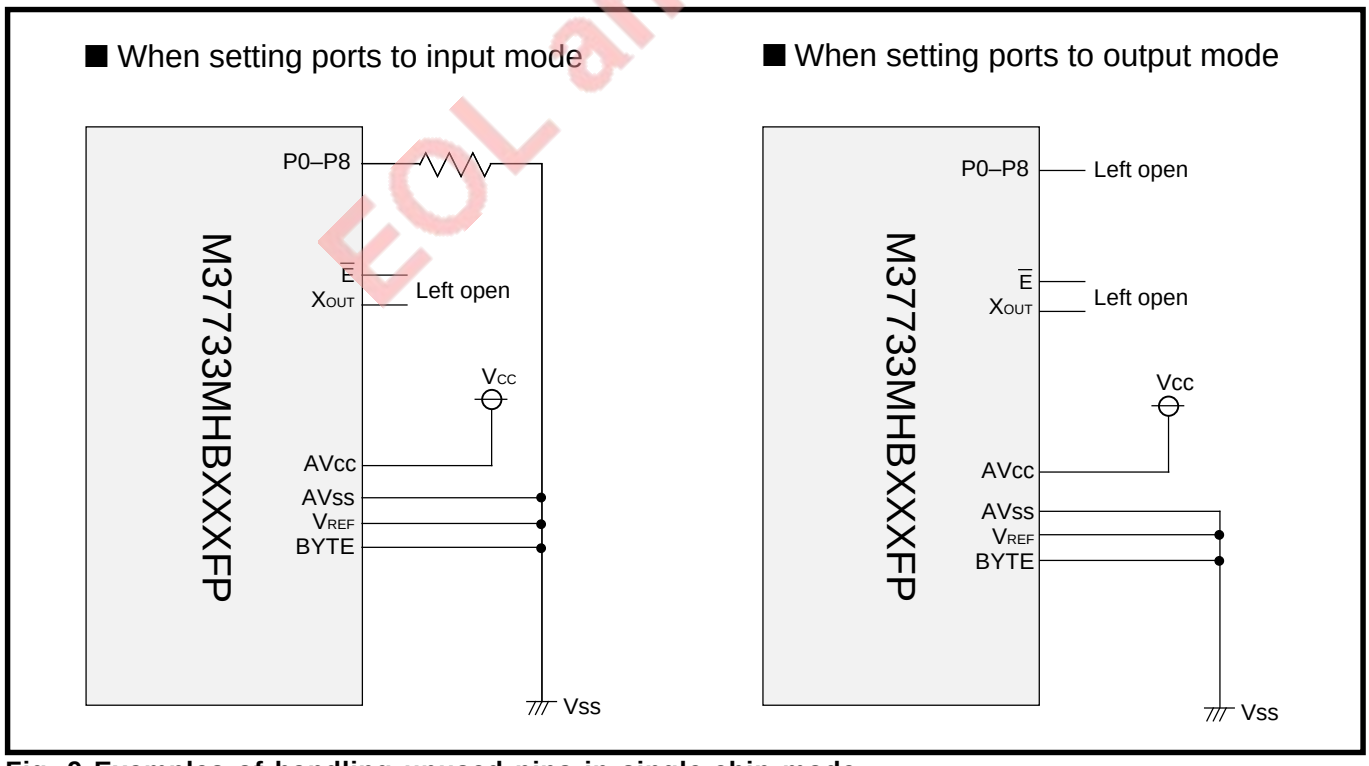

Fig. 9 Examples of handling unused pins in single-chip mode

EOL announced

2. In memory expansion mode

Table 2 Examples of handling unused pins in memory expansion

Pins	Handling example
P42–P47, P5–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Notes 1, 2, and 7**).
$\overline{\text{BHE}}$ (**Note 3**)	Leave this pin open. (**Note 5**)
ALE (**Note 4**)	
$\overline{\text{HLDA}}$	
XOUT (**Note 6**)	Leave this pin open.
$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$	Connect these pins to pin Vcc via resistors after these pins set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched t
voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: this pin functions as an input port from reset until the processor mode is switched to the memory exp
a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

6: This is applied when an external clock is input to pin XIN.

7: Set pin P42/ϕ1 as pin P42. (Clock ϕ1 output is disabled.) And then, for this pin, do the same handling as that for pins P43 to P47 and P5 to P8.

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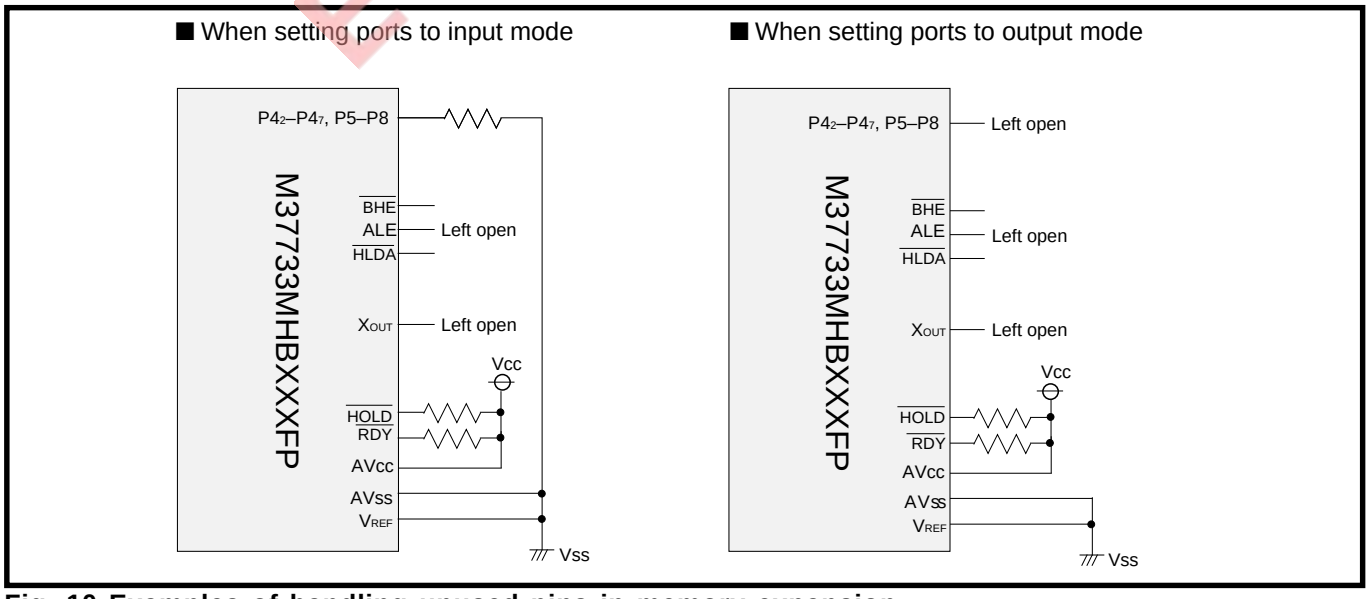


Fig. 10 Examples of handling unused pins in memory expansion

APPENDIX

Appendix 7. Examples of handling unused pins

3. In microprocessor mode

Table 3 Examples of handling unused pins in microprocessor mode

Pins	Handling example
P43–P47, P5–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Notes 1 and 2**).
$\overline{BHE}$ (**Note 3**)	Leave this pin open. (**Note 5**)
ALE (**Note 4**)	
$\overline{HLDA}$, ϕ1	
XOUT (**Note 6**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: this pin functions as an input port from reset until the processor mode is switched to the microprocessor mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

6: This is applied when an external clock is input to pin XIN.

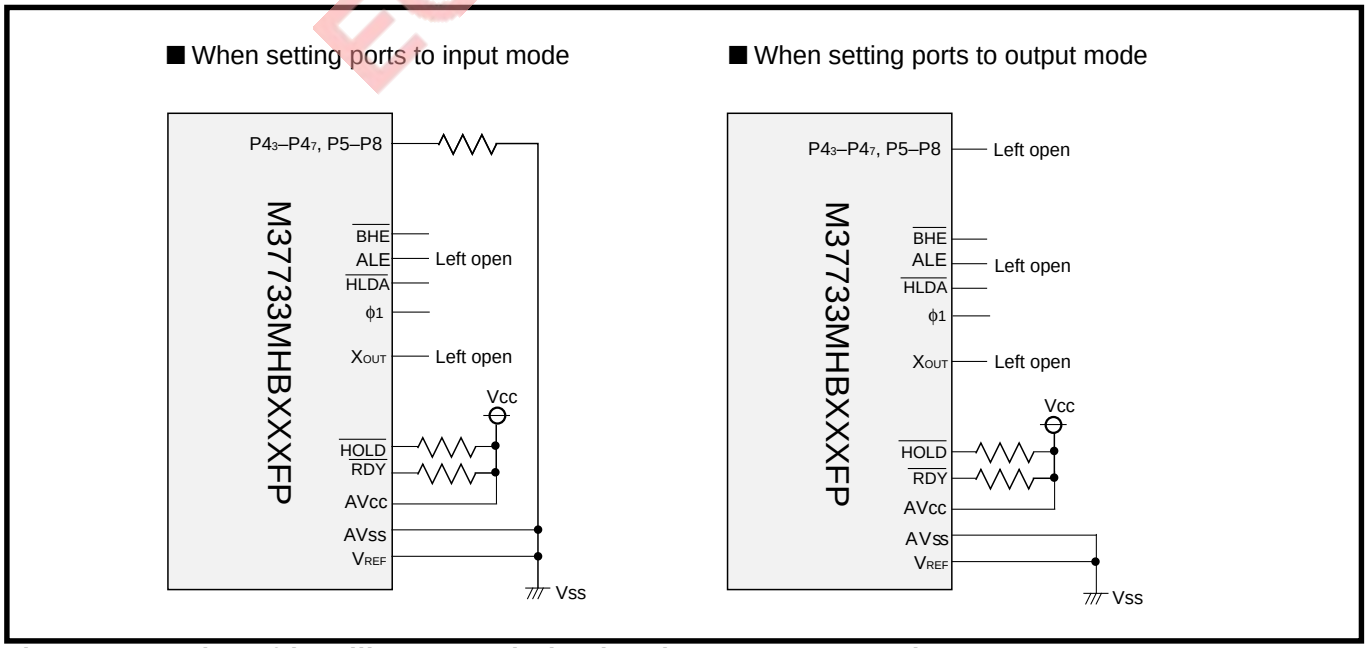


Fig. 11 Examples of handling unused pins in microprocessor mode

EOL announced

Appendix 8. Countermeasure examples against noise

General countermeasure examples against noise are described below. Although the effect of these countermeasures depends on each system, refer to the following when a noise-related problem occurs.

1. Shortest wiring length

The wiring on a printed circuit board may function as an antenna which feeds noise into the microcomputer. The shorter the total wiring length (by mm unit), the less possibility of noise insertion into the microcomputer.

(1) Wiring for pin $\overline{\text{RESET}}$

Make the length of wiring connected to pin $\overline{\text{RESET}}$ as short as possible. In particular, connect a capacitor between pin $\overline{\text{RESET}}$ and pin Vss with the shortest possible wiring (within 20 mm).

Reason

If noise is input to pin $\overline{\text{RESET}}$, the microcomputer restarts operation before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

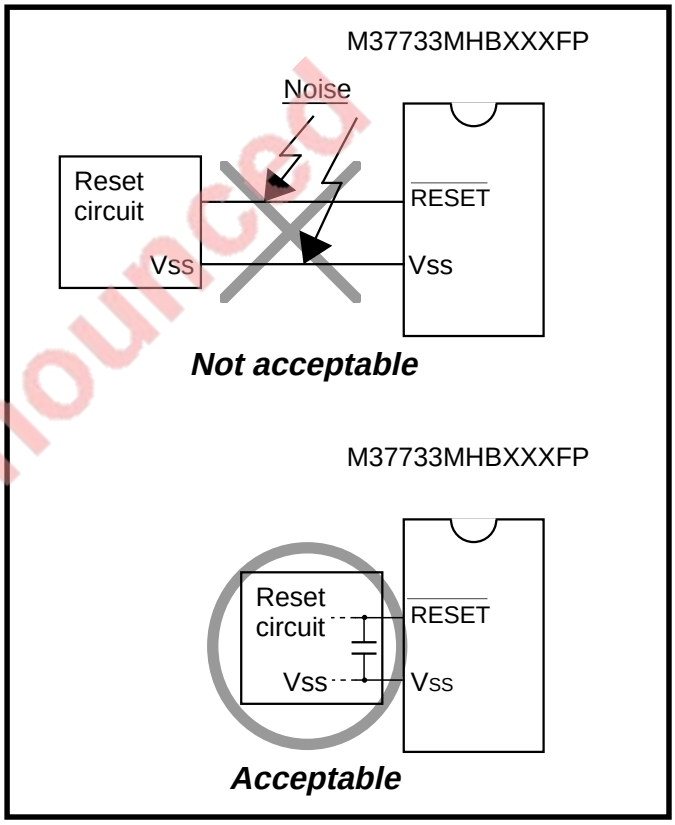


Fig. 12 Wiring for pin $\overline{\text{RESET}}$

EOL announced

APPENDIX

Appendix 8. Countermeasure examples against noise

(2) Wiring for clock I/O pins

- Make the length of wiring connected to clock I/O pins as short as possible.
- Make the length of wiring between the grounding lead of the capacitor, which is connected to the oscillator and pin Vss of the microcomputer, as short as possible (within 20 mm).
- Separate the Vss pattern only for oscillation from all other Vss patterns. (Refer to **Figure 21.**)

Reason

The microcomputer's operation synchronizes with a clock generated by the oscillation circuit. If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a malfunction or a program runaway.

Also, if the noise causes a potential difference between the Vss level of the microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

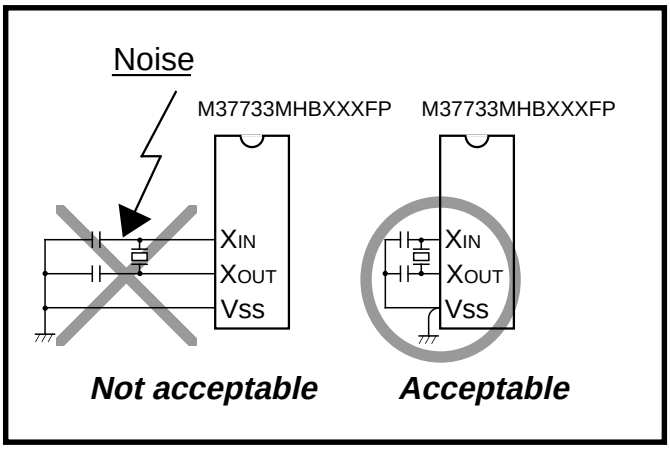


Fig. 13 Wiring for clock I/O pins

(3) Wiring for pin CNVss

Connect pin CNVss to pin Vss with the shortest possible wiring.

Reason

The processor mode of the microcomputer is influenced by a potential at pin CNVss when pin CNVss and pin Vss are connected. If the noise causes a potential difference between the two pins, the processor mode may become unstable. This may cause a malfunction or a program runaway.

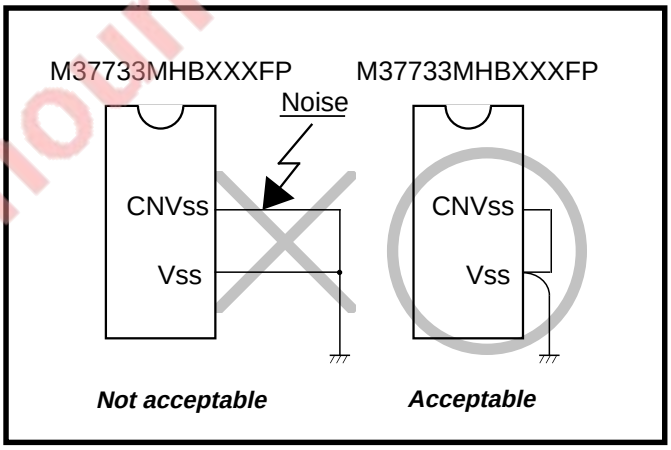


Fig. 14 Wiring for pin CNVss

EOL announced

(4) Wiring to pin CNVss

[In single-chip and memory expansion modes]

- Connect pin CNVss to pin Vss of the microcomputer with the shortest possible wiring.
- If the above countermeasure cannot be taken, insert an approximate 5 kΩ resistor between pins CNVss and Vss and, again, make the distance between the resistor and pin CNVss as short as possible.

[In microprocessor mode]

- Connect pin CNVss to pin Vcc with the shortest possible wiring.

Reason

Pin CNVss is connected to the internal ROM in the low-impedance state. (Noise is easily to be fed to the pin in this condition.)

If noise enters pin CNVss, incorrect instruction codes or data are fetched from the built-in PROM. This may cause a program runaway.

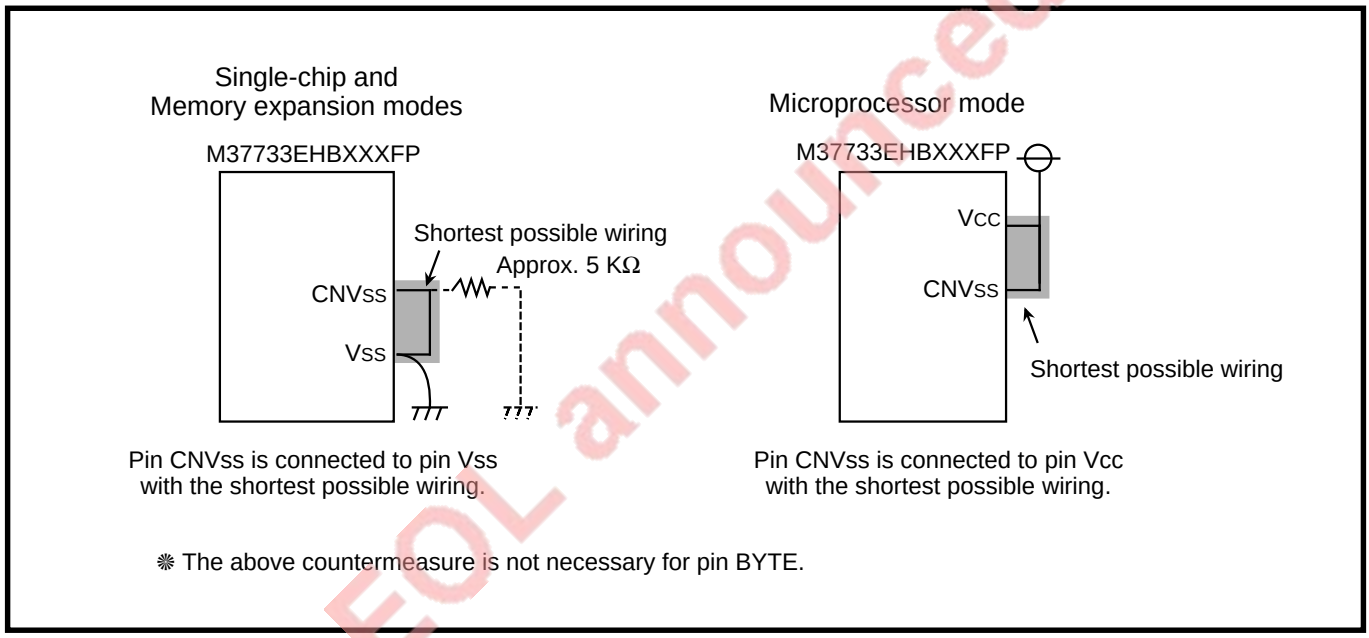


Fig. 15 Built-in PROM version: Wiring for pin CNVss

EOL announced

APPENDIX

Appendix 8. Countermeasure examples against noise

2. Connection of bypass capacitor between Vss line and Vcc line

Connect an approximate 0.1 μF bypass capacitor as follows:

- Connect a bypass capacitor between pin Vss and pin Vcc, at equal lengths.
- The wiring connecting the bypass capacitor between pin Vss and pin Vcc should be as short as possible.
- Use thicker wiring for the Vss and Vcc lines than for the other signal lines.

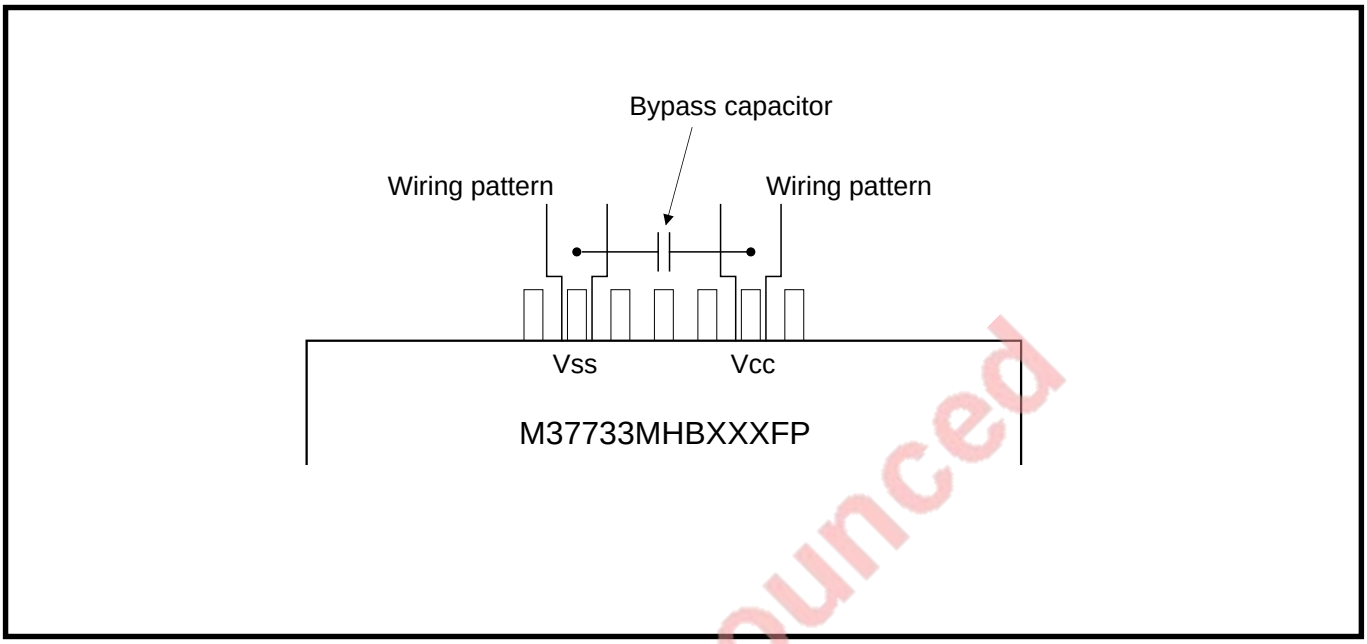


Fig. 16 Bypass capacitor connection

EOL announced

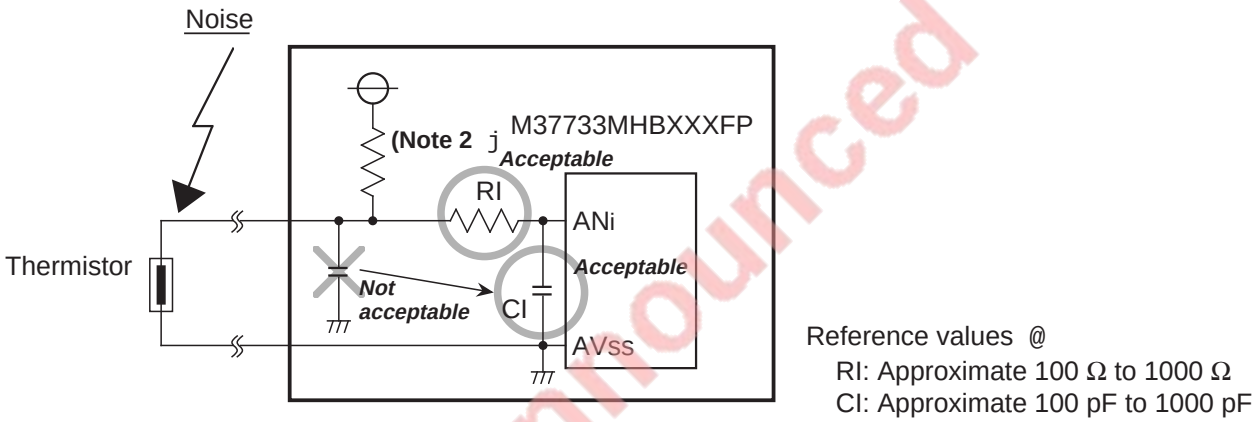
3. Wiring for analog input pins, analog power source pins, etc.

(1) Processing analog input pins

- Connect a resistor to the analog signal line, which is connected to an analog input pin, in series. Additionally, connect the resistor to the microcomputer as close as possible.
- Connect a capacitor between pin AVss and the analog input pin, as close to pin AVss as possible.

Reason

A signal which is input to the analog input pin is usually an output signal from a sensor.
The sensor, which detects changes in status, is installed far from the printed circuit board. Therefore, this long wiring between them becomes an antenna which picks up noise and feeds it into the microcomputer.
If a capacitor between an analog input pin and pin AVss is grounded far away from pin AVss, noise on the GND line may enter the microcomputer through the capacitor.



Notes 1: Design an external circuit for pin ANi so that charge/discharge is available within 1 cycle of AD.
2: This resistor and the thermistor are used to divide resistance.

Fig. 17 Countermeasure example against noise for analog input pin using thermistor

EOL announced

APPENDIX

Appendix 8. Countermeasure examples against noise

(2) Processing for analog power source pins, etc.

- Use independent power sources for pins Vcc, AVcc and VREF.
- Insert capacitors between pins AVcc and AVss, and between pins VREF and AVss, respectively.

Reasons: Prevents noise from affecting the A-D converter on the Vcc

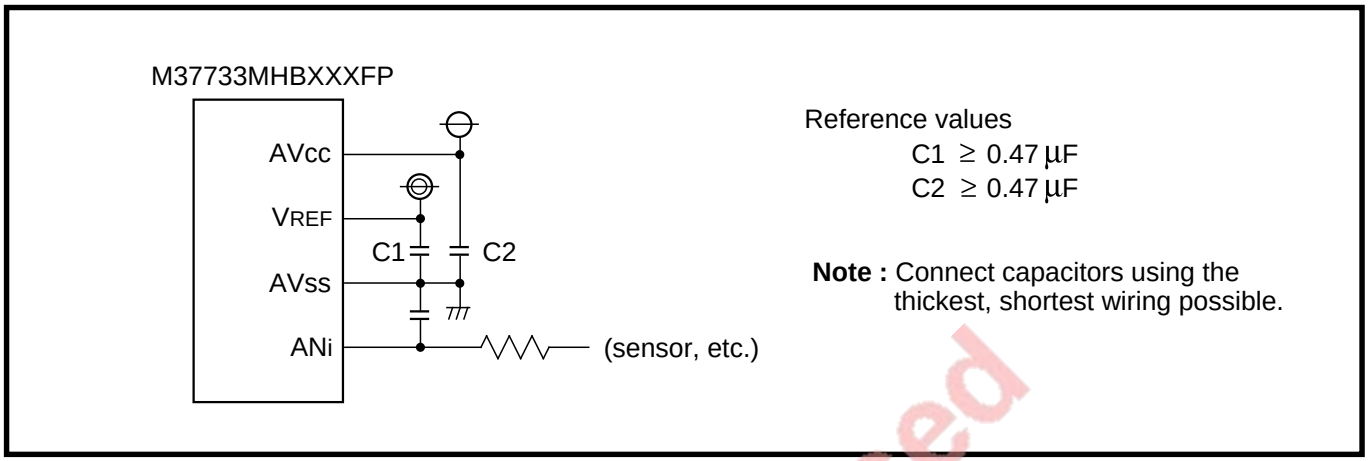


Fig. 18 Processing for analog power source pins, etc.

EOL announced

4. Oscillator protection

The oscillator, which generates the basic clock for the microcomputer operations, must be protected from the affect of other signals.

(1) Distance oscillator from signal lines with large current flows

- Install the microcomputer, especially the oscillator, as far as possible from signal lines which handle currents larger than the microcomputer current value tolerance.

Reason

The microcomputer is used in systems which contain signal lines for controlling motors, LEDs, thermal heads, etc. Noise occurs due to mutual inductance when a large current flows through the signal lines.

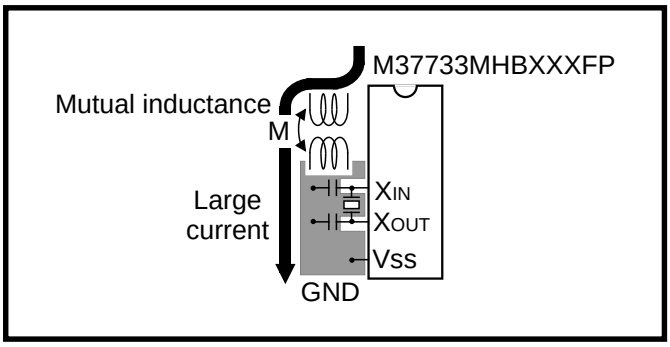


Fig. 19 Wiring for signal lines with large current flows

(2) Distance oscillator from signal lines with frequent potential level changes

- Install an oscillator and a connecting pattern away from signal lines in which potential levels change frequently.
- Do not cross these signal lines over clock-related or noise-sensitive signal lines.

Reason

Signal lines with frequently changing potential levels may affect other signal lines at the rising or falling edge. In particular, if the lines cross over a clock-related signal line, clock waveforms may be deformed, which causes a microcomputer malfunction or a program runaway.

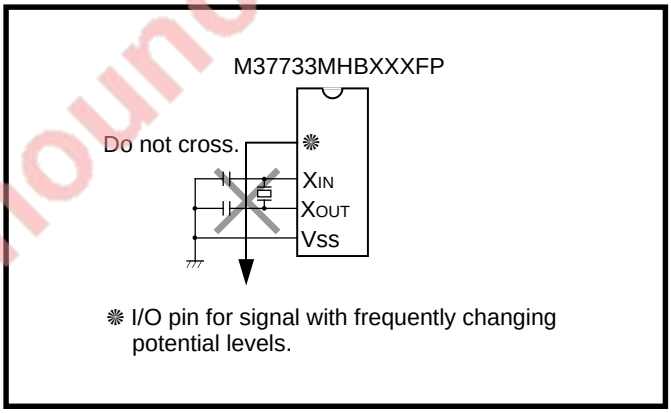


Fig. 20 Wiring for signal lines with frequent potential level changes

EOL announced

APPENDIX

Appendix 8. Countermeasure examples against noise

(3) Oscillator protection using Vss pattern

Print a Vss pattern on the bottom (soldering side) of a double-sided printed circuit board, under the oscillator mount position.

Connect the Vss pattern to pin Vss of the microcomputer with the shortest possible wiring, separating it from other Vss patterns.

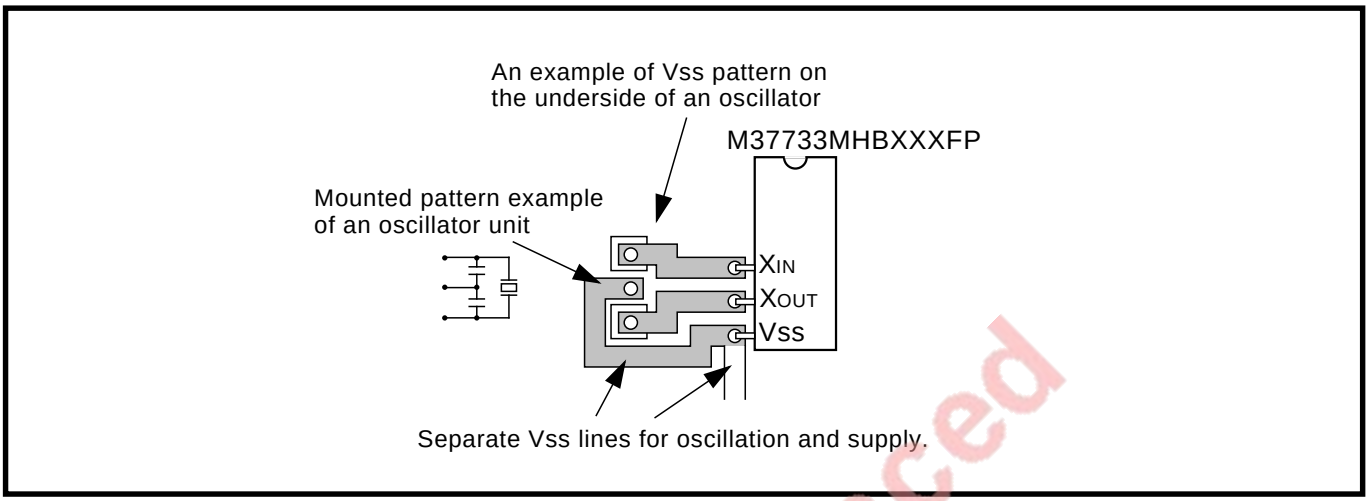


Fig. 21 Vss pattern underneath mounted oscillator

EOL announced

5. Setup for I/O ports

Setup for I/O ports is follows:

<Hardware>

●Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>

- Read the data of an input port several times to confirm that input levels are equal.
- Periodically rewrite data to the output port's Pi register, as the data may reverse due to noise.
- Rewrite data to port Pi direction registers periodically.

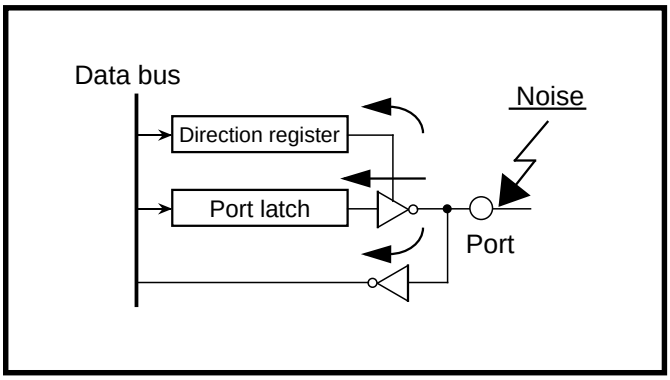


Fig. 22 Setup for I/O ports

EOL announced

APPENDIX

Appendix 8. Countermeasure examples against noise

6. Reinforcement of the power source line

- For the Vss and Vcc lines, use thicker wiring than that of other signal lines.
- When using a multilayer printed circuit board, the Vss pattern and the Vcc pattern must each be one of the middle layers.
- The following is necessary for double-sided printed circuit boards:
  - On one side, the microcomputer is installed at the center, and the Vss line is looped or meshed around it. The vacant area is filled with the Vss line.
  - On the opposite side, the Vcc line is wired the same as the Vss line.
  - The power source lines of external devices which are connected by bus to the microcomputer must be connected to the microcomputer's power source lines with the shortest possible wiring.

Reasons

With external devices connected to the microcomputer, the levels of many of the signal lines (total external address buses: 24 bits) may change simultaneously, causing noise on the power source line.

EOL announced

Appendix 9. Q & A

Information which may be helpful in fully utilizing the 7733 Group is provided in Q & A format.
In Q & A, as a rule, one question and its answer are summarized within one page. The upper box on each page is a question, and a box below the question is its answer. (If a question or an answer extends to two or more pages, there is a page number at the lower right corner.)
At the upper right corner of each page, the main function related to the contents of description in that page is listed.

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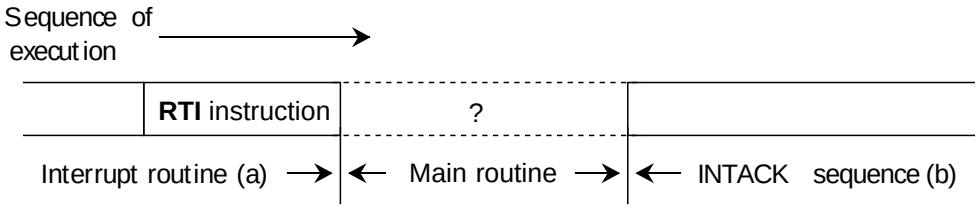
APPENDIX

Appendix 9. Q & A

Q

If an interrupt request (b) occurs while an interrupt routin
routine is not executed at all from when the execution of th
execution of the INTACK sequence for the next interrupt (b)

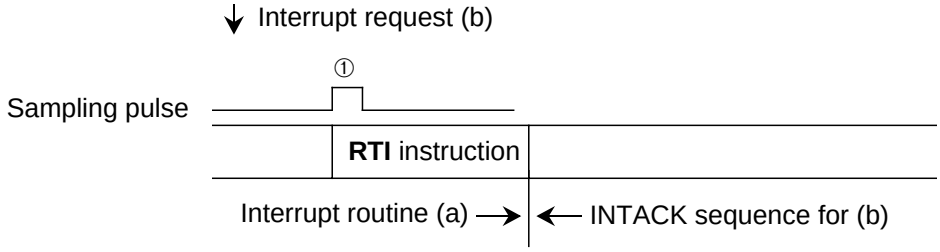


Conditions:
- I = 0 by executing the **RTI** instruction
- Interrupt priority level of interrupt (b) is higher than IPL of main routine.
- Interrupt priority level detection time = 2 cycles of ϕ

A

An interrupt request is sampled by detecting a sampling puls
the CPU's op-code fetch cycle.

(1) If the next interrupt request (b) occurs before sampling pul ① of the **RTI** instruction is generated, sampling for this interrupt request is completed while the **RTI** instruction is executed. Therefore, the INTACK sequence for (b) is executed without executing the main routine. (Even one instruction is not executed.)

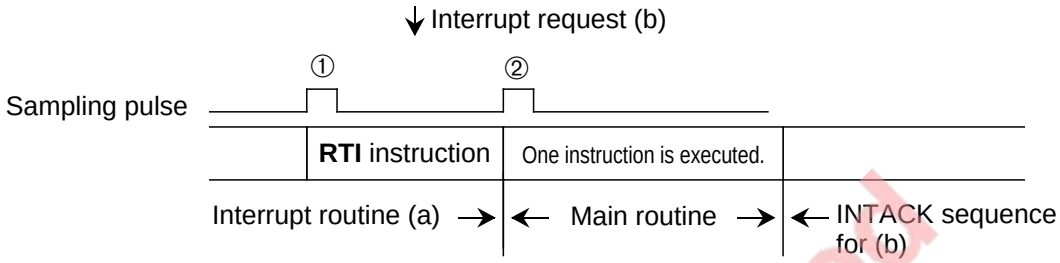


EOL announced

Interrupt

A

(2) If the next interrupt request (b) occurs immediately after sampling pulse ① is generated, this interrupt request is sampled when sampling pulse ② for the next instruction is generated. Therefore, one instruction in the main routine is executed, and then the INTACK sequence for (b) is executed.



(2/2)

EOL announced

APPENDIX

Appendix 9. Q & A

Interrupt

Q

Suppose that there is a routine where a certain interrupt request should not be accepted. (The other interrupt requests are acceptable.)
Although when the interrupt priority level selection bits for the above interrupt are set to "000_2," in other words, when this interrupt is set to be disabled, this interrupt request is actually accepted immediately after the change of the priority level. Why did this occur and what should I do about it?

```
                    :
Interrupt request is   CLB #07H, XXXIC  ; The interrupt priority level selection bits are set to "000₂"
accepted                                ; or the interrupt request bit is set to "0."
in this interval →     LDA A,DATA       ; The first instruction of a routine where a certain
                                          interrupt request should not be accepted
                    :                   ;
```

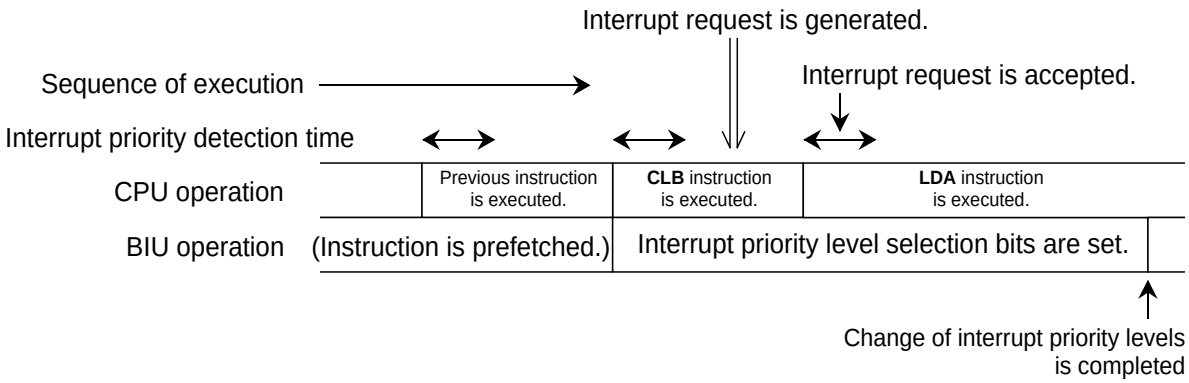
A

As for the change of the interrupt priority level, when the following are met, the microcomputer may pretend to accept an interrupt request immediately after this interrupt is set to be disabled:

- The next instruction (in the above example, it is the **LDA** instruction) is already stored into a instruction queue buffer for the BIU.
- Conditions for accepting the instruction which should not be accepted are satisfied immediately before the next instruction in the instruction queue buffer is executed.

When writing to the memory • I/O, the CPU transfers an address and data to the BIU. And then, the CPU executes the next instruction in the instruction queue buffer while the BIU is writing the data into the actual address. Interrupt priority level is determined at the start of each instruction.

In the above case, the CPU <u>executes the next instruction before the BIU completes the change</u> of the interrupt priority level. Therefore, when the interrupt priority level is detected synchronously with the execution of the next instruction, <u>the interrupt priority level before the change is detected and its interrupt request is accepted.</u>



(1/2)

EOL announced

Interrupt

A

To solve this problem, make sure that, by software, the execution of a routine where a certain interrupt request should not be accepted starts after the change of the interrupt level is completed. The following lists a sample program.

[Sample program]

After an instruction which writes value "000_2" to the interrupt priority level selection bits, fill the instruction queue buffer with several **NOP** instructions and make the next instruction not to be executed until the writing is completed.

```
    :
CLB #07H, XXXIC  ; The interrupt priority level selection bits are set to "0002."
NOP              ;
NOP              ;
NOP              ;
LDA  A,DATA      ; The first instruction of a routine where a certain interrupt
                   request should not be accepted
```


EOL announced

APPENDIX

Appendix 9. Q & A

Q

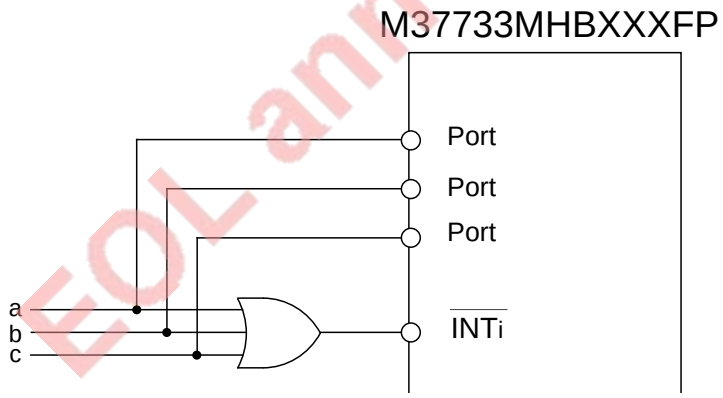
(1) At what timing of clock ϕ_1 is an external interrupt (an input signal on the $\overline{INT_i}$ pin) detected?
(2) Suppose that more than three external interrupt input pins ($\overline{INT_i}$) are necessary, what should I do?

A

(1) If the edge sense or level sense is selected, an external interrupt request occurs when the level of an input signal on the $\overline{INT_i}$ pin changes. This is independent of clock ϕ_1.
At this time, if the edge sense is selected, the interrupt request bit is set to "1," also.

(2) There are two methods: one is the method to use the external interrupt's level sense; the other one is the method to use the timer's event counter mode.

① Method to use the external interrupt's level sense
As for hardware, input a logical sum of several interrupt signals (for example, 'a', 'b', and 'c') to the $\overline{INT_i}$ pin and input each signal to the corresponding port.
As for software, check the ports' input levels in an $\overline{INT_i}$ interrupt routine in order to detect a signal (one of signals 'a,' 'b,' and 'c') which is input.



Note : The same process can be realized by using the key input interrupt function, also.

② Method to use the timer's event counter mode
As for hardware, input an interrupt signal to the TA_{iIN} or TB_{iIN} pin.
As for software, set the timer's operating mode to the event counter mode and set value "0000_{16}" to the timer. Furthermore, select a valid edge.
The timer's interrupt request occurs when an interrupt signal (selected valid edge) is input.

EOL announced

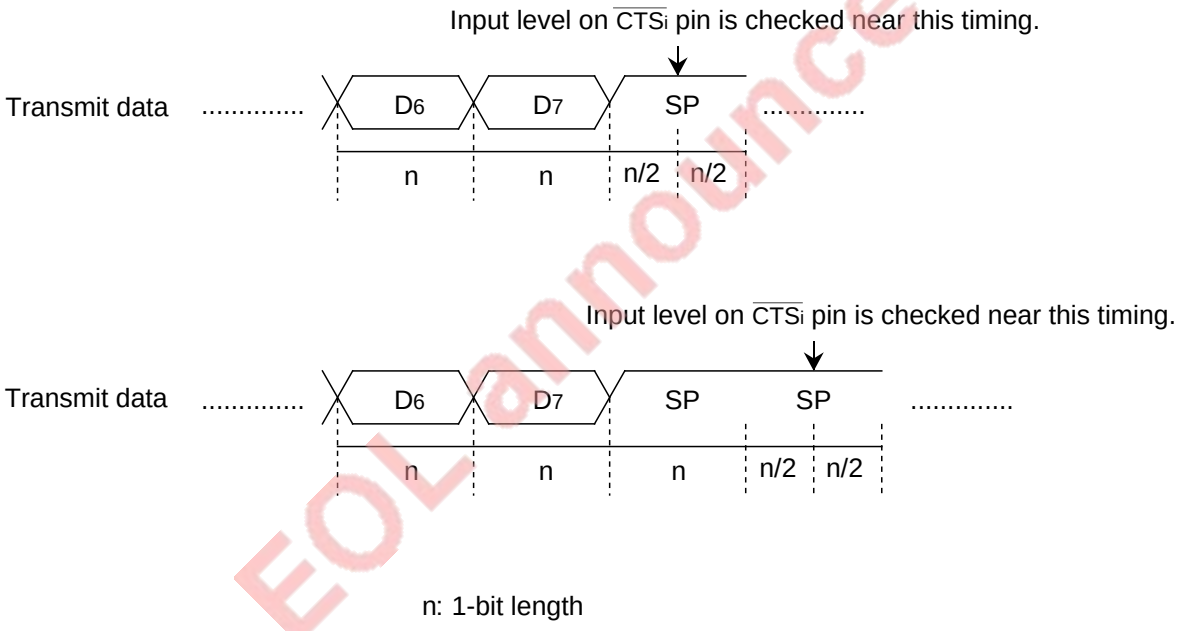
Serial I/O (UART mode)

Q

If the $\overline{CTS}$ function is selected in UART (clock asynchronous serial I/O) mode, at what timing should the $\overline{CTS}$ input's level be checked by the transmitter?

A

Checked near the middle of the stop bit (if two stop bits are selected, the second stop bit).



n: 1-bit length

EOL announced

APPENDIX

Appendix 9. Q & A

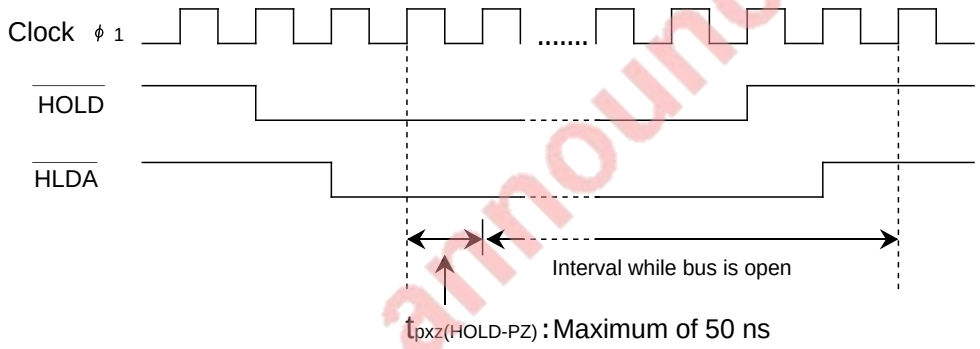
Hold function

Q

If “L” level is input to the $\overline{\text{HOLD}}$ pin, when is a bus actually opened?

A

When interval 50 ns (max.) has passed since clock ϕ_1 is risen immediately after the $\overline{\text{HLDA}}$ pin’s output becomes “L,” a bus is opened.



EOL announced

Processor mode

Q

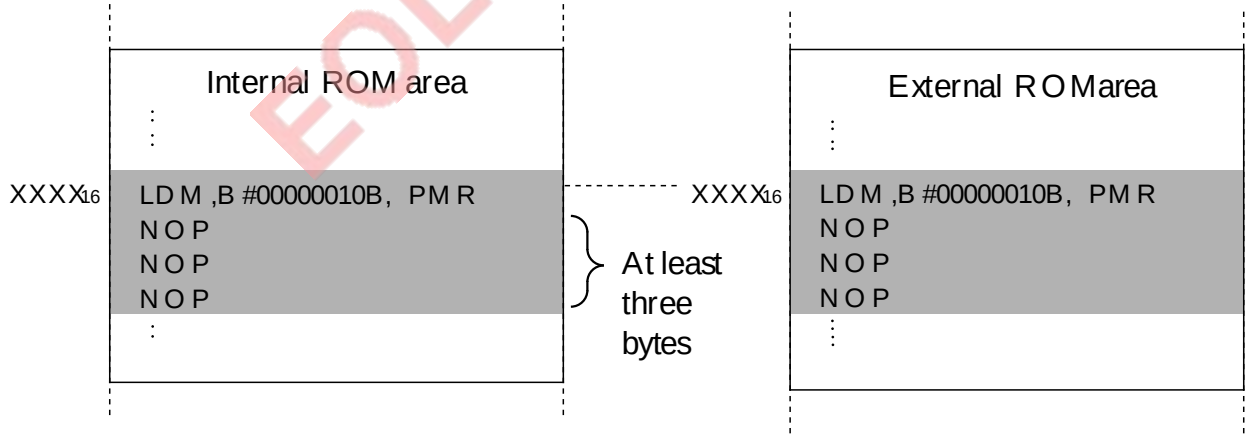
When the processor mode is switched, as described below, by setting the processor mode bits (bits 1 and 0 at address $5E_{16}$) while a program is executed, is there any precaution on software?

- Single-chip mode →Microprocessor mode
- Memory expansion mode →Microprocessor mode

A

Although when the processor mode bits are set in order to switch the processor mode, as described above, the mode is not switched until the write cycle for the processor mode bits is completed. (The processor mode is actually switched simultaneously with the write cycle's completion.)
At this time, the program counter indicates the address which is next to the address (address XXXX_{16}) where the write instruction for the processor mode bits is stored. Also, access to the internal ROM area is disabled. Note that there is a possibility that less than four bytes of instructions are prefetched into instruction queue buffers. Therefore, the address which resides in the external ROM area and is accessed first after the mode is switched is one of addresses "XXXX_{16} + 1" to "XXXX_{16} + 4." Note also that instructions at addresses "XXXX_{16} + 1" to "XXXX_{16} + 3" in the internal ROM area may be executed. To solve this problem, do the following processes by software.

[Process ①]
Program a write instruction for the processor mode bits and the following instructions (at least three bytes) to the same addresses of the internal ROM and external ROM areas. (See below.)



[Process ②]
Transfer a write instruction for the processor mode bits to an internal RAM area and make the program branch to the address in order to execute the write instruction. And then, make the program branch to the program address in the external ROM area. (Contents of instruction queue buffers are initialized by a branch instruction.)

EOL announced

APPENDIX

Appendix 9. Q & A

SFR

Q

Is there any SFR where a certain write instruction can not be used?

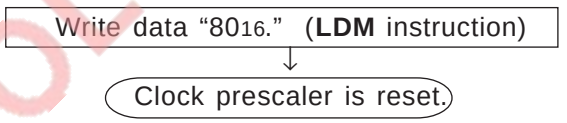
A

① Use the **STA** and **LDM** instructions for setting the registers or the bits listed below.
Do not use read-modify-write instructions (for example, **CLB, SEB, INC, DEC, ASL, LSR, ROL,** and **ROR**).

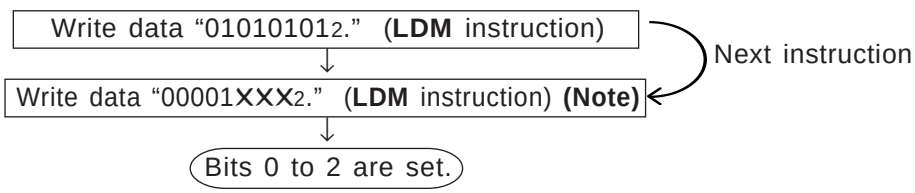
UART0 baud rate register (address 31_{16})
UART1 baud rate register (address 39_{16})
UART2 baud rate register (address 65_{16})
UART0 transmission buffer register (addresses 33_{16}, 32_{16})
UART1 transmission buffer register (addresses $3B_{16}$, $3A_{16}$)
UART2 transmission buffer register (addresses 67_{16}, 66_{16})
Timer A4 two-phase pulse signal processing selection bit (bit 7 at address 44_{16})
Timer A3 two-phase pulse signal processing selection bit (bit 6 at address 44_{16})
Timer A2 two-phase pulse signal processing selection bit (bit 5 at address 44_{16})

② When writing data to the oscillation circuit control register 1 (address $6F_{16}$), be sure to follow the procedure shown below.

• When initializing the clock prescaler

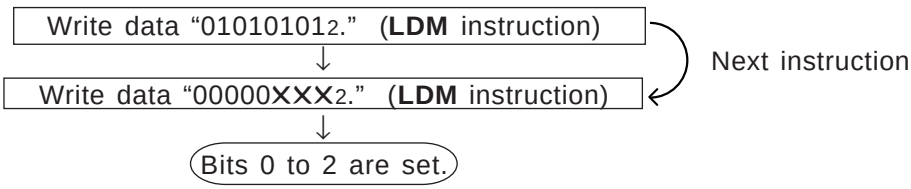


• When writing to bits 0 to 2



Note: In the case of the 7735 Group, write data "0000**0**XXX$_2$."

③ When writing data to the memory allocation control register (address 63_{16}), be sure to follow the procedure shown below.



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Debug

Q

Is there any precaution when debugging?

A

Some functions of the 7733 Group cannot be evaluated by a debugger. For the operations listed below, use the built-in PROM version to make full evaluation.
When debugging, be sure to read the user's manual supplied with the debugger.

<<Operation examples that cannot be evaluated by a debugger>>

① Operation when the signal output disable selection bit (bit 6 at address $6C_{16}$) = "1"
② Operation when the stand-by state selection bit (bit 0 at address $6D_{16}$) = "1"
③ Operations for reading from and writing to addresses 02_{16} to 09_{16} in the memory expansion or microprocessor mode

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APPENDIX

Appendix 9. Q & A

Memory

Q

Questions about the memory allocation selection function are described below:
① For what purpose is this function used?
② Is there any precaution on use of this function?

A

① This function is used in order to secure an external memory area to bank 0_{16} in the memory expansion mode.
If there is an external device which is frequently accessed, this device's memory allocation in bank 0_{16} is effective for accessing this device, as well as internal RAM and SFR, with using DPR and DT efficiently. In the M37733MHBXXXFP, all of bank 0_{16} is specified as an area for internal resources. Therefore, this function is used to secure an external memory area in bank 0_{16}.
Note that the memory allocation selection bits are valid in the single-chip mode, also. In the single-chip mode, the memory allocation selection function is valid only for reduction of usable ROM area. Therefore, in the single-chip mode, we recommend to set these bits to "000_2" (the state immediately after reset) and not to change them.

② Note the following:
- When changing the memory allocation selection bits, follow the procedure in Figure 2.4.1.
- When changing the memory allocation selection bits, make sure that the change is done within an area which is in the internal ROM area both of after and before the change, for example addresses $00C000_{16}$ to $00FFFF_{16}$.
- We recommend to set the memory allocation selection bits only when a processor mode is set after reset and not to change them after this setting.
- When programming to the EPROM and one time PROM versions, program to addresses listed in Table 19.1.3.
- As for debugging for an area in bank 0_{16} or 1_{16} which is specified as an external area, some considerations may be necessary. For details concerning the development support tools, refer to the respective operation manuals.

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PART 2

7735 Group

CHAPTER 1 OVERVIEW
CHAPTER 2 CENTRAL PROCESSING UNIT (CPU)
CHAPTER 3 PROGRAMMABLE I/O PORTS
CHAPTER 4 INTERRUPTS
CHAPTER 5 KEY INPUT INTERRUPT FUNCTION
CHAPTER 6 TIMER A
CHAPTER 7 TIMER B
CHAPTER 8 SERIAL I/O
CHAPTER 9 A-D CONVERTER
CHAPTER 10 WATCHDOG TIMER
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CHAPTER 12 CONNECTING EXTERNAL DEVICES
CHAPTER 13 RESET
CHAPTER 14 CLOCK GENERATING CIRCUIT
CHAPTER 15 ELECTRICAL CHARACTERISTICS
CHAPTER 16 STANDARD CHARACTERISTICS
CHAPTER 17 APPLICATIONS
CHAPTER 18 LOW VOLTAGE VERSION
CHAPTER 19 BUILT-IN PROM VERSION
CHAPTER 20 EXTERNAL ROM VERSION
APPENDIX

EOL announced

PART 2 7735 Group

The differences between the 7735 Group and the 7733 Group are mainly described below.
For the 7733 Group, refer to part **"1. 7733 Group."**

The 7735 Group differs from the 7733 Group in the following:

- **External bus mode in the memory expansion mode and the microprocessor mode**
- **External memory area**
  (The 7735 Group has the maximum of 1-Mbyte external memory area.)
- **Setting conditions for bit 3 of the oscillation circuit control register 1**
  (In the 7735 Group, this bit must be "0." Note that, in the one time PROM version and the EPROM version, this bit is automatically set to "1" after reset. Therefore, be sure to clear this bit to "0.")
- **Functions of pin $\overline{\text{E}}$/$\overline{\text{RDE}}$**

EOL announced

CHAPTER 1
OVERVIEW

1.1 Performance overview
1.2 Pin configuration
1.3 Pin description
1.4 Block diagram

EOL announced

OVERVIEW

1.1 Performance overview

Concerning chapter “1. OVERVIEW,” the 7735 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“1.1 Performance overview”**
- **“1.2 Pin configuration”**
- **“1.3 Pin description”**

The following section of the 7735 Group is the same as that of the 7733 Group. Therefore, for this section, refer to part 1:

- **“1.4 Block diagram” (page 1-11 in part 1)**

1.1 Performance overview

Concerning section “1.1 Performance overview,” the 7735 Group differs from the 7733 Group in the following:

- **Description of the memory expansion in Table 1.1.1**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“1.1 Performance overview” (page 1-3 in part 1)**

Table 1.1.1 M37735MHBXXXFP’s performance overview

Items	Performance
Memory expansion	Possible (Maximum of 1 Mbytes)

EOL announced

1.2 Pin configuration

Figure 1.2.1 shows the M37735MHBXXXFP pin configuration.

Note: For the low voltage version, refer to chapter **"18. LOW VOLTAGE VERSION."**

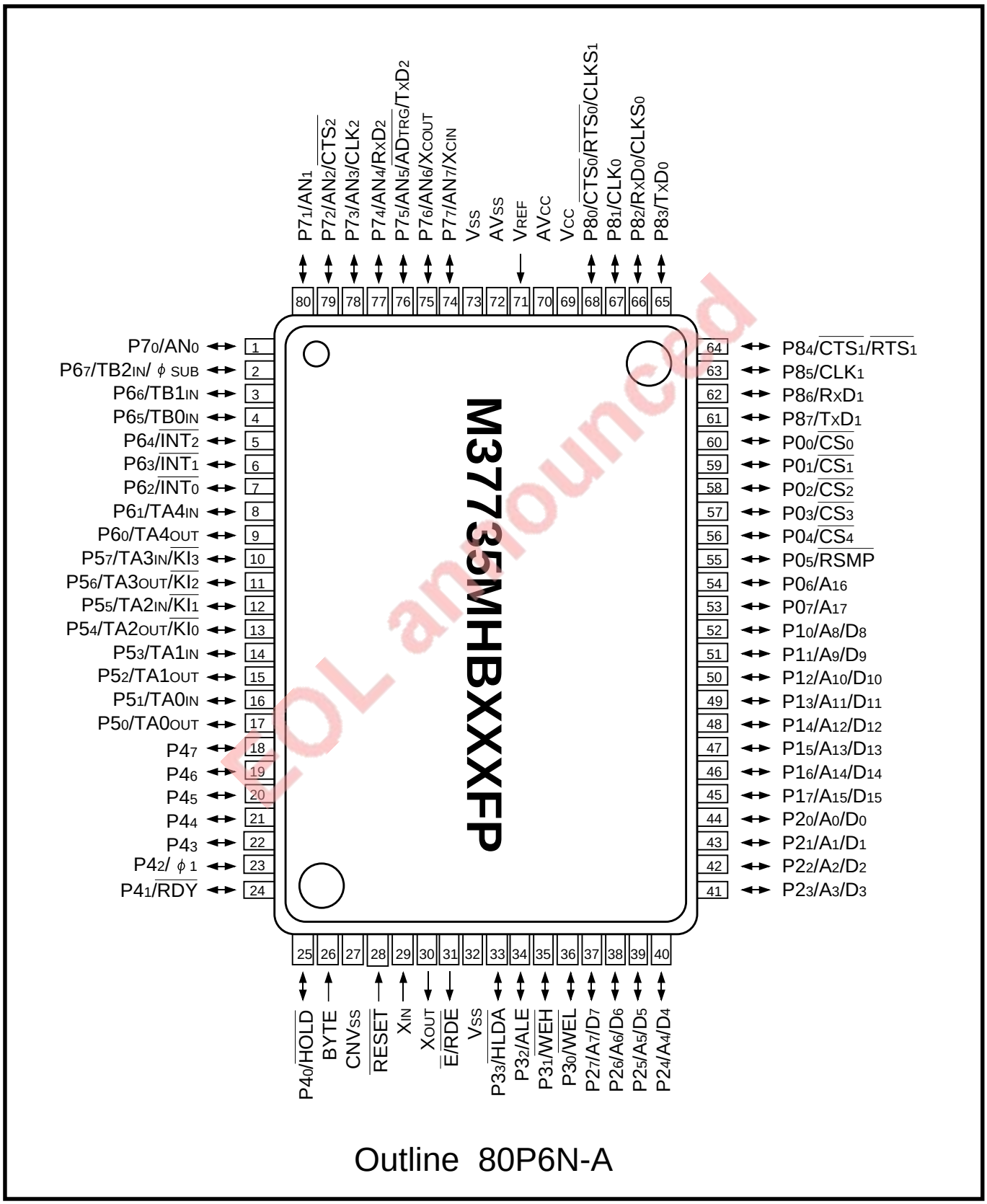

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Fig. 1.2.1 M37735MHBXXXFP pin configuration (Top view)

1.3 Pin description

Concerning section “1.3 Pin description,” the 7735 Group differs from the 7733 Group in the following:

- **“Description of pin $\overline{E}$ in Table 1.3.1”**
- **“Description of pins $P0_0$–$P0_7$, $P2_0$–$P2_7$ and $P3_0$–$P3_3$ in Table 1.3.2”**
- **“1.3.1 Examples of handling unused pins”**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“1.3 Pin description” (page 1-5 in part 1)**

Table 1.3.1 Pin description (1)

Pin	Name	Input/Output	Functions
$\overline{E}$	Internal enable output	Output	**[Single-chip Mode]** This pin outputs internal enable signal $\overline{E}$. When $\overline{E}$'s level is “L,” the microcomputer reads data and instruction codes or writes data. Also, output of internal enable signal $\overline{E}$ can be stopped by software. **[Memory Expansion Mode] [Microprocessor Mode]** This pin outputs read enable signal $\overline{RDE}$. This signal's level is “L” in the data read period of the read cycle.

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Table 1.3.2 Pin description (2)

Pin	Name	Input/Output	Functions
P0$_0$–P0$_7$	I/O port P0	I/O	**[Single-chip Mode]** Same as the 7733 Group.
$\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$, A$_{16}$, A$_{17}$		Output	**[Memory Expansion Mode] [Microprocessor Mode]** These pins respectively output signals $\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$, and address's high-order 2 bits (A$_{16}$ and A$_{17}$). ● Signal $\overline{CS_0}$–$\overline{CS_4}$ These signals are the chip select signals. When the microcomputer accesses a certain area, the corresponding pin outputs "L" level. (Refer to **Table 2.5.3.**) ● Signal $\overline{RSMP}$ This signal is the ready sampling signal and is used to generate signal $\overline{RDY}$ for accessing external memory area.
P2$_0$–P2$_7$	I/O port P2	I/O	**[Single-chip Mode]** Same as the 7733 Group.
A$_0$/D$_0$–A$_7$/D$_7$			**[Memory Expansion Mode] [Microprocessor Mode]** Input/Output of data (D$_0$–D$_7$) and output of address's low-order 8 bits (A$_0$–A$_7$) are performed with the time sharing method.
P3$_0$–P3$_3$	I/O port P3	I/O	**[Single-chip Mode]** Same as the 7733 Group.
$\overline{WEL}$, $\overline{WEH}$, ALE, $\overline{HLDA}$		Output	**[Memory Expansion Mode] [Microprocessor Mode]** These pins respectively output signals $\overline{WEL}$, $\overline{WEH}$, ALE, and $\overline{HLDA}$. ● Signal $\overline{WEL}$, $\overline{WEH}$ Signal $\overline{WEL}$ is the write enable low signal. Signal $\overline{WEH}$ is the write enable high signal. These signals' levels are "L" in the data write period of the write cycle. The operations of these signals depend on the level of pin BYTE. (Refer to **Table 12.1.1.**) ● Signal ALE This signal is used to separate the multiplexed signal which consists of an address and data to the address and the data. ● Signal $\overline{HLDA}$ This signal informs the external whether the microcomputer enters the Hold state or not. In Hold state, pin $\overline{HLDA}$ outputs "L" level.

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OVERVIEW

1.3 Pin description

1.3.1 Examples of handling unused pins

The following are examples of handling unused pins.
These are, however, just examples. In actual use, make the necessary adaptations and properly evaluate performance according to the user's system.

(1) In single-chip mode

Table 1.3.4 Examples of handling unused pins in single-chip mode

Pins	Handling example
P0–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Note 1**).
$\overline{E}$	Leave this pin open.
XOUT (**Note 2**)	
AVcc	Connect this pin to pin Vcc.
AVss, VREF, BYTE	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until the they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these ports function as input ports.
Software reliability can be enhanced when the contents of the above ports ' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.
For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).
2: This is applied when an external clock is input to pin XIN.

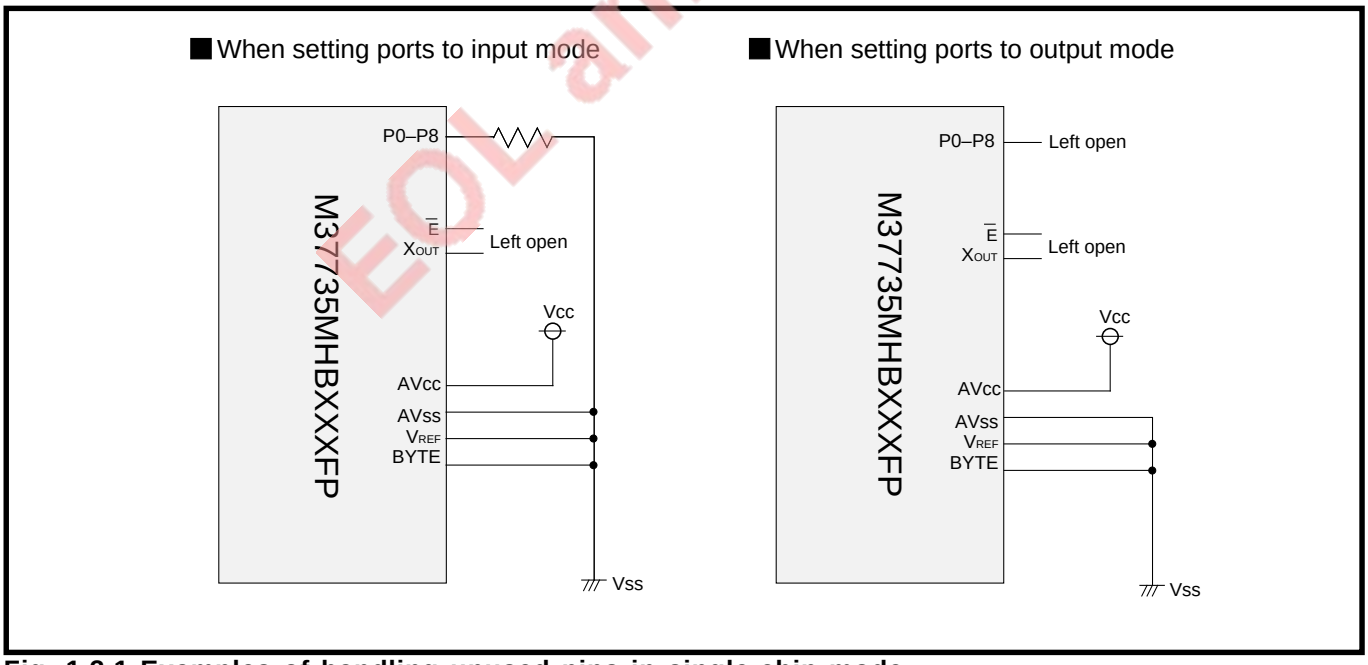


Fig. 1.3.1 Examples of handling unused pins in single-chip mode

EOL announced

(2) In memory expansion mode

Table 1.3.5 Examples of handling unused pins in memory expansion mode

Pins	Handling example
P42–P47, P5–P8 (**Note 5**)	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
$\overline{WEH}$, $\overline{WEL}$, $\overline{RDE}$, $\overline{HLDA}$, $\overline{CS0}$–$\overline{CS4}$, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
XOUT (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the memory expansion mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

4: This is applied when an external clock is input to pin XIN.

5: Set pin P42/ϕ1 as pin P42. (Clock ϕ1 output is disabled.) And then, for this pin, do the same handling as that for pins P43 to P47 and P5 to P8.

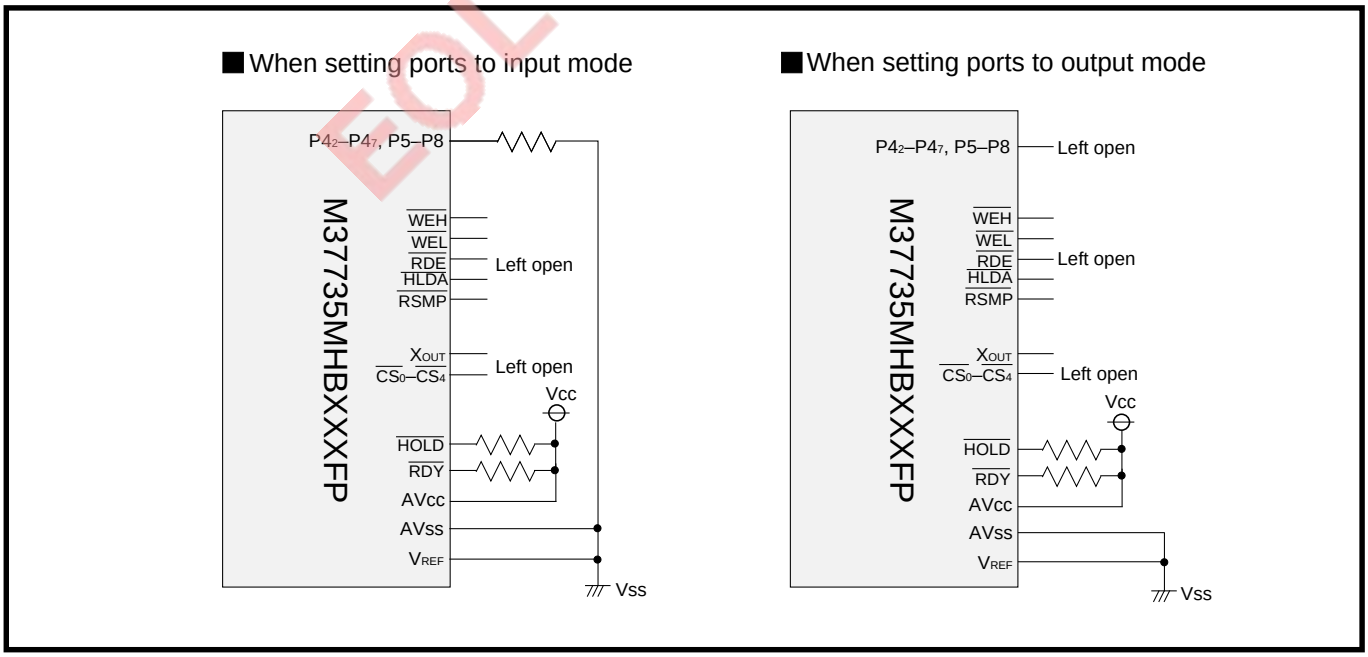


Fig. 1.3.2 Examples of handling unused pins in memory expansion mode

EOL announced

OVERVIEW

1.3 Pin description

(3) In microprocessor mode

Table 1.3.6 Examples of handling unused pins in microprocessor mode

Pins	Handling example
P43–P47, P5–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
$\overline{WEH}$, $\overline{WEL}$, $\overline{RDE}$ $\overline{HLDA}$, ϕ1, $\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
XOUT (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVCC	Connect this pin to pin Vcc.
AVSS, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the microprocessor mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.

4: This is applied when an external clock is input to pin XIN.

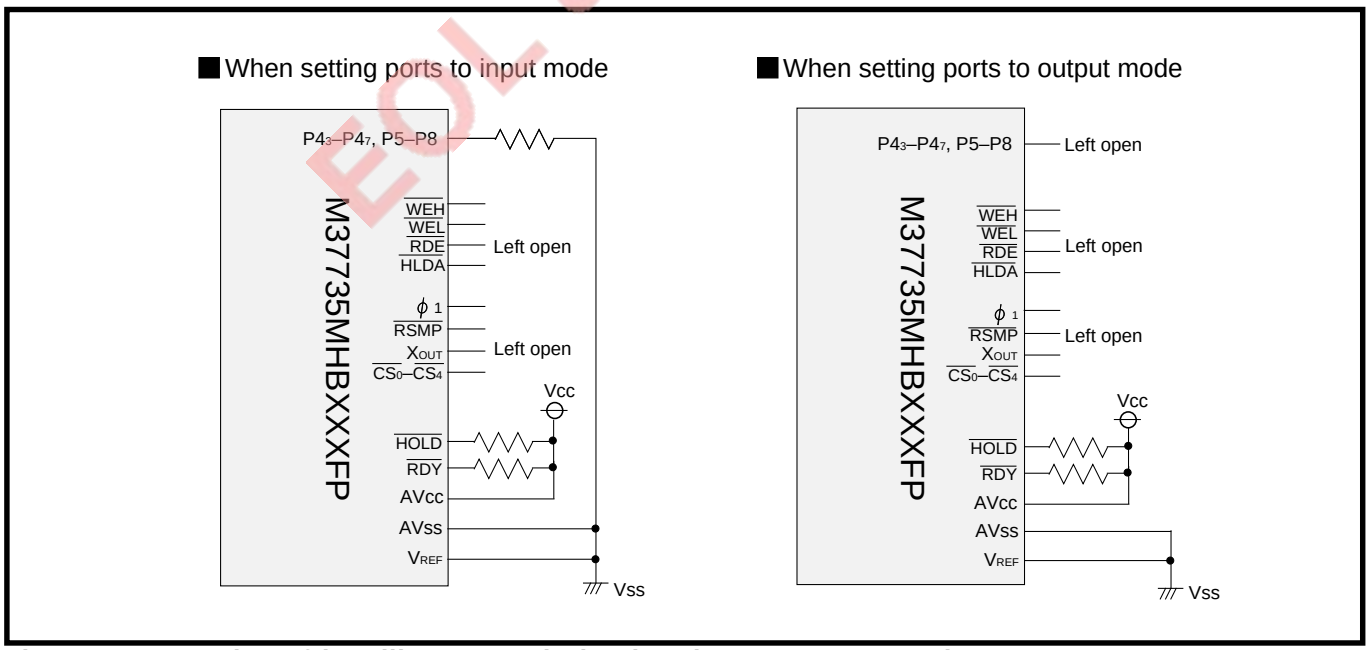


Fig. 1.3.3 Examples of handling unused pins in microprocessor mode

EOL announced

CHAPTER 2

CENTRAL PROCESSING UNIT (CPU)

EOL announced

2.1 Central processing unit
2.2 Bus interface unit
2.3 Accessible area
2.4 Memory allocation
2.5 Processor modes

CENTRAL PROCESSING UNIT (CPU)

2.2 Bus interface unit

Concerning chapter “2. CENTRAL PROCESSING UNIT (CPU),” the 7735 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“2.2 Bus interface unit”**
- **“2.3 Accessible area”**
- **“2.5 Processor modes”**

The following sections of the 7735 Group are the same as those of the 7733 Group. Therefore, for these section, refer to part 1:

- **“2.1 Central processing unit” (page 2–2 in part 1)**
- **“2.4 Memory allocation” (page 2–18 in part 1)**

2.2 Bus interface unit

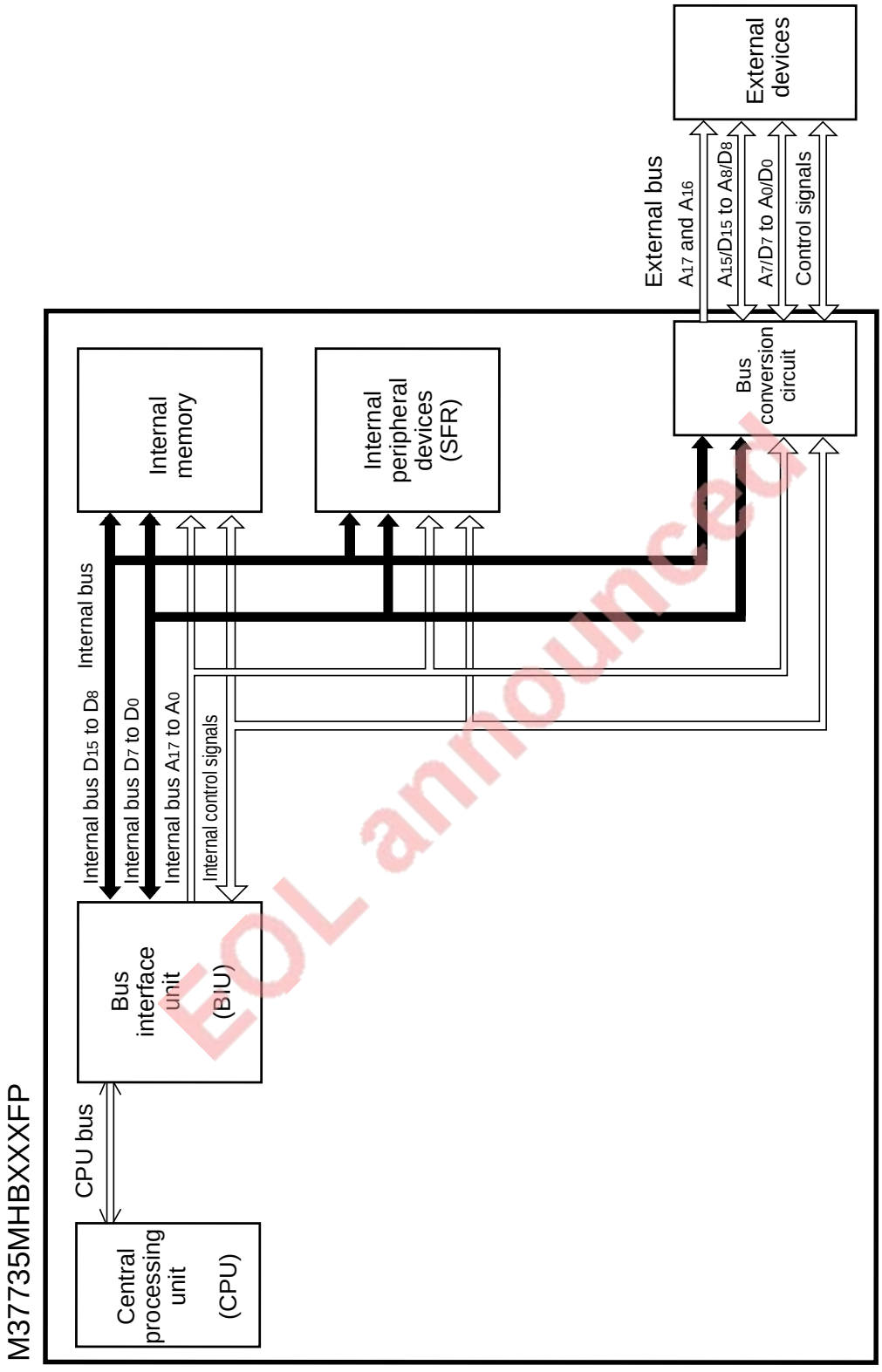
Concerning section “2.2 Bus interface unit,” the 7735 Group differs from the 7733 Group in the following.

- **External buses in Figure 2.2.1**
- **Signal names in Figure 2.2.3**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“2.2 Bus interface unit” (page 2–10 in part 1)**

EOL announced



SFR : Special Function Register

Notes 1: CPU bus, internal bus, and external bus are independent of each other.
2: For details about signals on the external buses, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**

EOL announced

Fig. 2.2.1 Buses and bus interface unit (BIU)

2.2 Bus interface unit

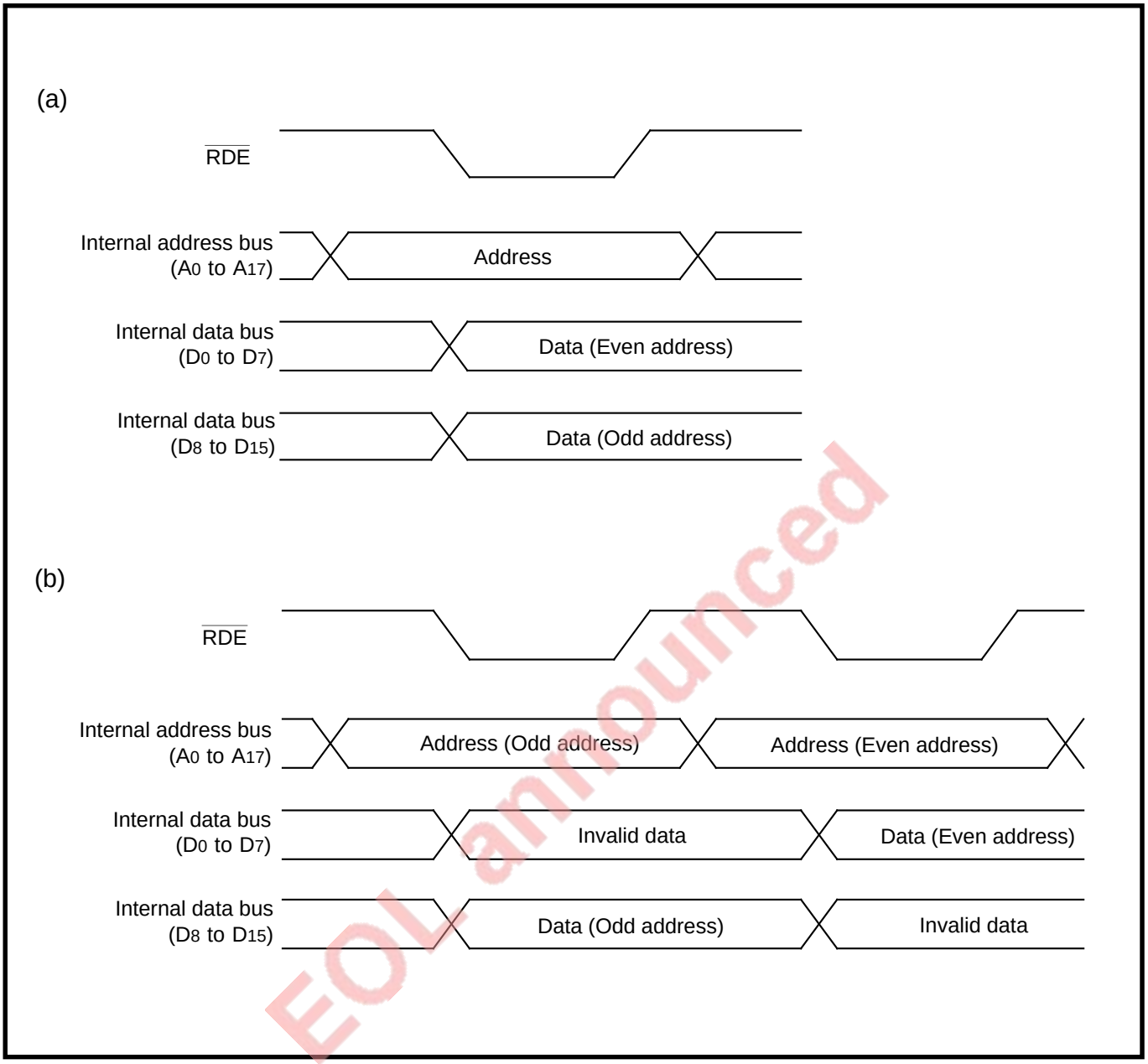


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Fig. 2.2.3 Basic operating waveforms of bus interface unit (BIU)

2.3 Accessible area

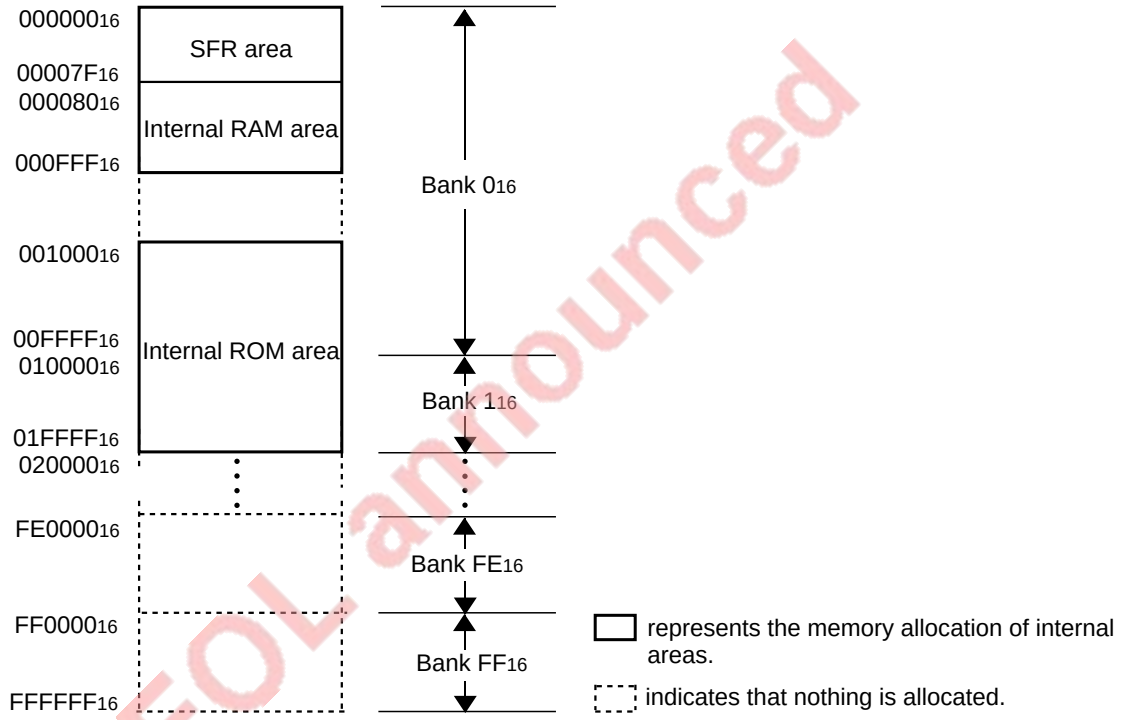
Concerning section "2.3 Accessible area," the 7735 Group differs from the 7733 Group in the following:

- **Accessible area which is allocated to addresses 0_{16} to $0FFFFF_{16}$ (Maximum of 1 Mbytes)**
- **Figure 2.3.1**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"2.3 Accessible area" (page 2–16 in part 1)**

•SFR : Special Function Register



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Notes 1: Banks 10_{16} to FF_{16} cannot be accessed.

2: Memory allocation of internal area in bank 0_{16} depends on the microcomputer's type and settings of the memory allocation selection bits.
The above diagram shows the M37735MHBXXXFP's accessible area immediately after reset.
For the other microcomputers of the 7735 Group, refer to **"Appendix 1. Memory allocation of 7735 Group."** For settings of the memory allocation selection bits, refer to section **"2.4 Memory allocation."**

Fig. 2.3.1 M37735MHBXXXFP's accessible area

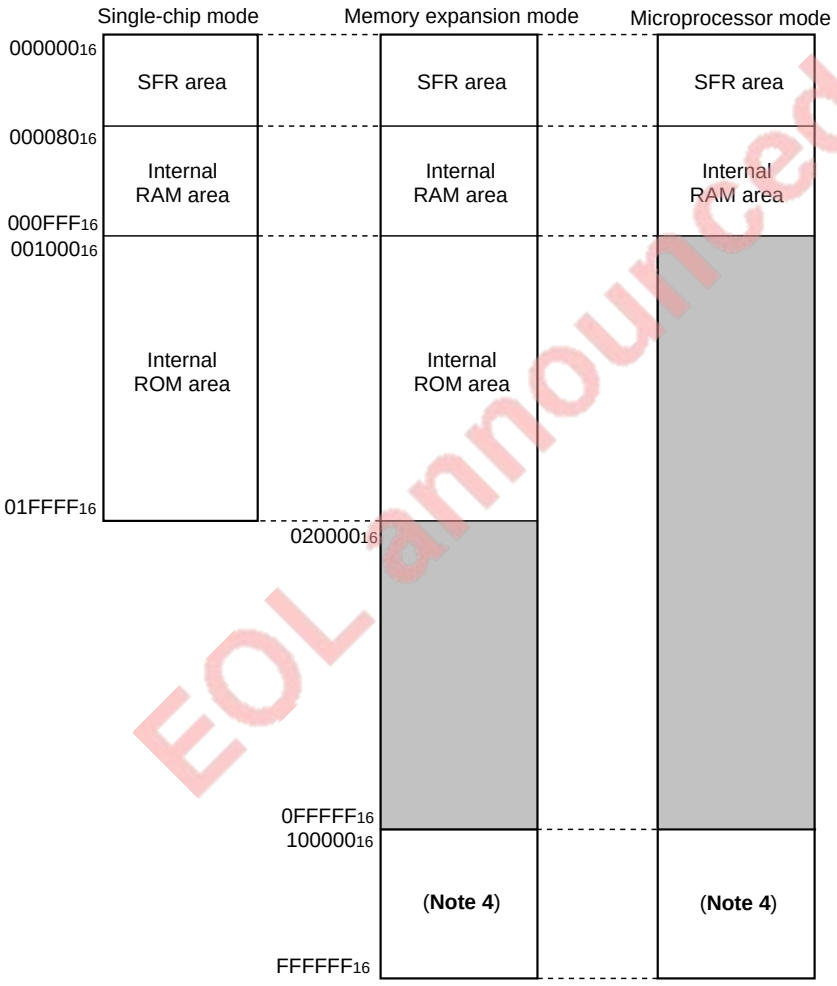
2.5 Processor modes

Concerning section “2.5 Processor modes,” the 7735 Group differs from that of the 7733 Group in the following:

- **“Fig. 2.5.1 Memory map in each processor mode”**
- **“Fig. 2.5.2 Pin configuration in each processor mode (Top view)”**
- **“Table 2.5.1 Relationship between processor modes and functions of P0 to P4”**
- **“2.5.4 Relationship between access addresses and chip select signals ($\overline{CS_0}$–$\overline{CS_4}$) (This section is added in part 2.)**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“2.5 Processor modes” (page 2–24 in part 1)**

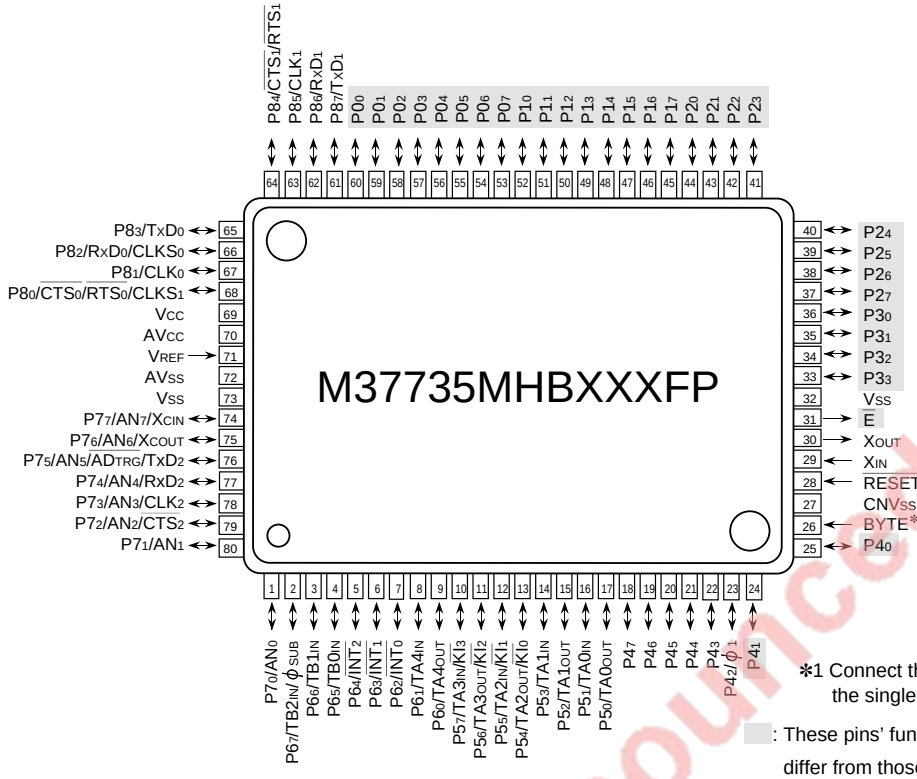


EOL announced

Notes 1: ▭ represents external area.
By accessing this area, an external device connected to the M37735MHBXXXFP can be accessed .
2: This applies when the contents of memory allocation selection bits (bits 2 to 0 at address 63_{16}) = “000_2.”
3: For the other microcomputers of the 7735 Group, refer to section **“Appendix 1. Memory allocation of 7735 Group.”**
4: Banks 10_{16} to FF_{16} cannot be accessed.

Fig. 2.5.1 Memory map in each processor mode (M37735MHBXXXFP)

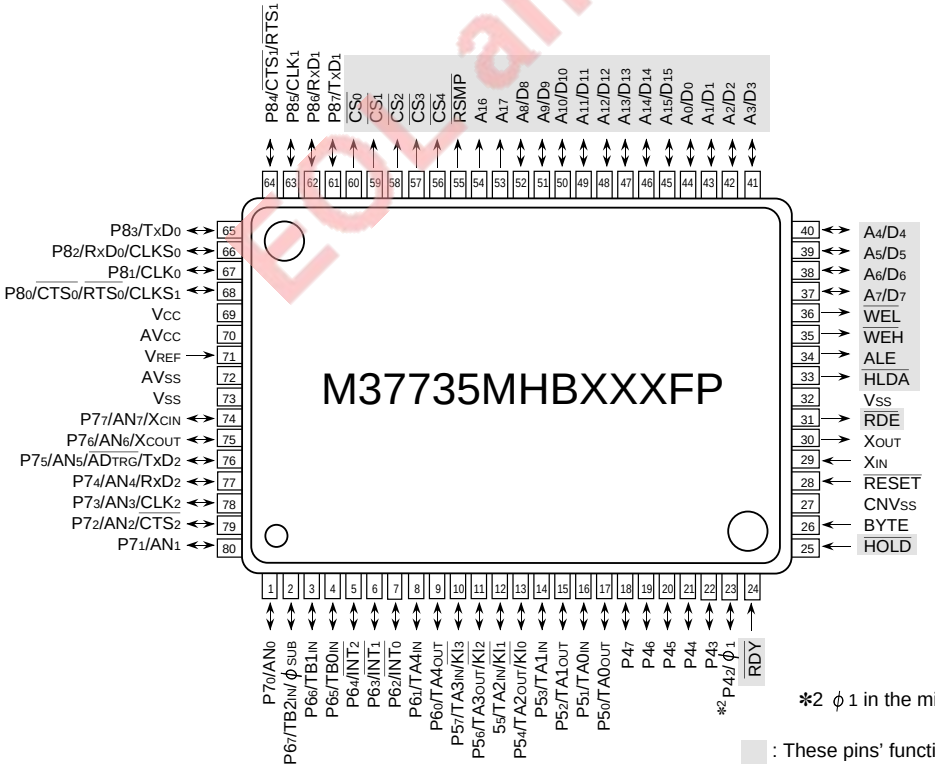
<Single-chip mode>



*1 Connect this pin to Vss in the single-chip mode.

: These pins' functions in the single-chip mode differ from those in the memory expansion or microprocessor mode.

<Memory expansion and Microprocessor modes>



*2 φ1 in the microprocessor mode

: These pins' functions in the single-chip mode differ from those in the memory expansion or microprocessor mode.

Pre-announced

Fig. 2.5.2 Pin configuration in each processor mode (Top view)

CENTRAL PROCESSING UNIT (CPU)

2.5 Processor modes

Table 2.5.1 Relationship between processor modes and functions of P0 to P4

Pin name \ Processor mode	Single-chip mode	Memory expansion and Microprocessor modes
P0	P P: Functions as a programmable I/O port.	$P0_0$ to $P0_4$ $\overline{CS_0}$ to $\overline{CS_4}$ (**Note 1**) $P0_5$ $\overline{RSMP}$ $P0_6$ and $P0_7$ A_{16}, A_{17}
P1	P P: Functions as a programmable I/O port.	■ When external data bus is 16 bits wide (BYTE = "L") A_8 to A_{15} D(odd) D(odd): Data at odd address ■ When external data bus is 8 bits wide (BYTE = "H") A_8 to A_{15}
P2	P P: Functions as a programmable I/O port.	■ When external data bus is 16 bits wide (BYTE = "L") A_0 to A_7 D(even) D(even): Data at even address ■ When external data bus is 8 bits wide (BYTE = "H") A_0 to A_7 D D: Data
P3	P P: Functions as a programmable I/O port.	■ When external data bus is 16 bits wide (BYTE = "L") $P3_0$ $\overline{WEL}$ (**Note 2**) $P3_1$ $\overline{WEH}$ (**Note 2**) $P3_2$ ALE $P3_3$ $\overline{HLDA}$ ■ When external data bus is 8 bits wide (BYTE = "H") $P3_0$ $\overline{WEL}$ (**Note 2**) $P3_1$ ("H" level output) $P3_2$ ALE $P3_3$ $\overline{HLDA}$
P4	P P: Functions as a programmable I/O port **(Note 3)**.	$P4_0$ $\overline{HOLD}$ $P4_1$ $\overline{RDY}$ $P4_2$ ϕ_1 (**Note 4**) $P4_3$ to $P4_7$ P P: Functions as a programmable I/O port.
$\overline{E}/\overline{RDE}$	$\overline{E}$ (**Note 2**)	$\overline{RDE}$ (**Note 2**)

Notes 1: When an internal area is accessed, signals $\overline{CS_0}$ to $\overline{CS_4}$ are not output. (The output level is fixed to "H.")

2: These signals are affected by the signal output disable selection bit (bit 6 at address $6C_{16}$). (Refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**)

3: Pin $P4_2$ can also function as a clock ϕ_1 output pin. (Refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**)

4: In the memory expansion mode, this pin functions as a programmable I/O port. Furthermore, it can be switched to be a clock ϕ_1 output pin when selected by software. In the microprocessor mode, this pin is affected by the signal output disable selection bit (bit 6 at address $6C_{16}$). (Refer to chapter **"12. CONNECTING EXTERNAL DEVICES."**)

EOL announced

2.5.4 Relationship between access addresses and chip select signals $\overline{CS_0}$ to $\overline{CS_4}$

Table 2.5.3 lists the relationship between access addresses and chip select signals $\overline{CS_0}$ to $\overline{CS_4}$.
Table 2.5.4 lists the relationship between the memory allocation selection bits and addresses for chip select signals $\overline{CS_0}$, $\overline{CS_1}$ in the memory expansion mode.

Table 2.5.3 Relationship between access addresses and chip select signals $\overline{CS_0}$ to $\overline{CS_4}$

Chip select signal	Area	Access addresses	
		Memory expansion mode	Microprocessor mode
$\overline{CS_0}$	The former half of bank 00_{16} except for internal memory area	(**Note**) ———	00 1000_{16} to 00 $7FFF_{16}$
$\overline{CS_1}$	•The latter half of bank 00_{16} except for internal memory area •Banks 01_{16} to 03_{16}	02 0000_{16} (**Note**) to 03 $FFFF_{16}$	00 8000_{16} to 03 $FFFF_{16}$
$\overline{CS_2}$	Banks 04_{16} to 07_{16}	04 0000_{16} to 07 $FFFF_{16}$	04 0000_{16} to 07 $FFFF_{16}$
$\overline{CS_3}$	Banks 08_{16} to $0B_{16}$	08 0000_{16} to 0B $FFFF_{16}$	08 0000_{16} to 0B $FFFF_{16}$
$\overline{CS_4}$	Banks $0C_{16}$ to $0F_{16}$	0C 0000_{16} to 0F $FFFF_{16}$	0C 0000_{16} to 0F $FFFF_{16}$

Note: This applies when each of bits 1 and 0 of the memory allocation control register (address 63_{16}) = "0." For details, refer to **Table 2.5.4.**

Table 2.5.4 Relationship between memory allocation selection bits and addresses for chip select signals $\overline{CS_0}$, $\overline{CS_1}$ in memory expansion mode

Memory allocation selection bits*			Internal ROM area	Access addresses	
b2	b1	b0		$\overline{CS_0}$	$\overline{CS_1}$
0	0	0	00100_{16} to $01FFFF_{16}$ (124 Kbytes)	———	020000_{16} to $03FFFF_{16}$
0	0	1	00200_{16} to $01FFFF_{16}$ (120 Kbytes)	00100_{16} to $001FFF_{16}$	020000_{16} to $03FFFF_{16}$
1	1	0	00800_{16} to $01FFFF_{16}$ (96 Kbytes)	00100_{16} to $007FFF_{16}$	020000_{16} to $03FFFF_{16}$
1	1	1	00800_{16} to $00FFFF_{16}$ (32 Kbytes)	00100_{16} to $007FFF_{16}$	010000_{16} to $03FFFF_{16}$

Memory allocation selection bits* : Bits 0 to 2 of the memory allocation control register (address 63_{16})

EOL announced

MEMO

EOL announced

CHAPTER 3
PROGRAMMABLE I/O PORTS

3.1 Programmable I/O ports
3.2 Port peripheral circuits
3.3 Pull-up function
3.4 Internal peripheral devices' I/O functions (Ports P42 and P5 to P8)

EOL announced

PROGRAMMABLE I/O PORTS

3.2 Port peripheral circuits

Concerning chapter “3. PROGRAMMABLE I/O PORTS,” the 7735 Group differs from the 7733 Group in the following section. Therefore, only the difference is described in this chapter:

- **3.2 Port peripheral circuits**

The following sections are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“3.1 Programmable I/O ports” (page 3-2 in part 1)**
- **“3.3 Pull-up function” (page 3-8 in part 1)**
- **“3.4 Internal peripheral devices’ I/O functions (Ports P4$_2$ and P5 to P8)” (page 3-10 in part 1)**

3.2 Port peripheral circuits

Concerning section “3.2 Port peripheral circuits,” the 7735 Group differs from the 7733 Group in the following:

- **Pin $\overline{E}$/$\overline{RDE}$ in Figure 3.2.2**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“3.2 Port peripheral circuits” (page 3-6 in part 1)**

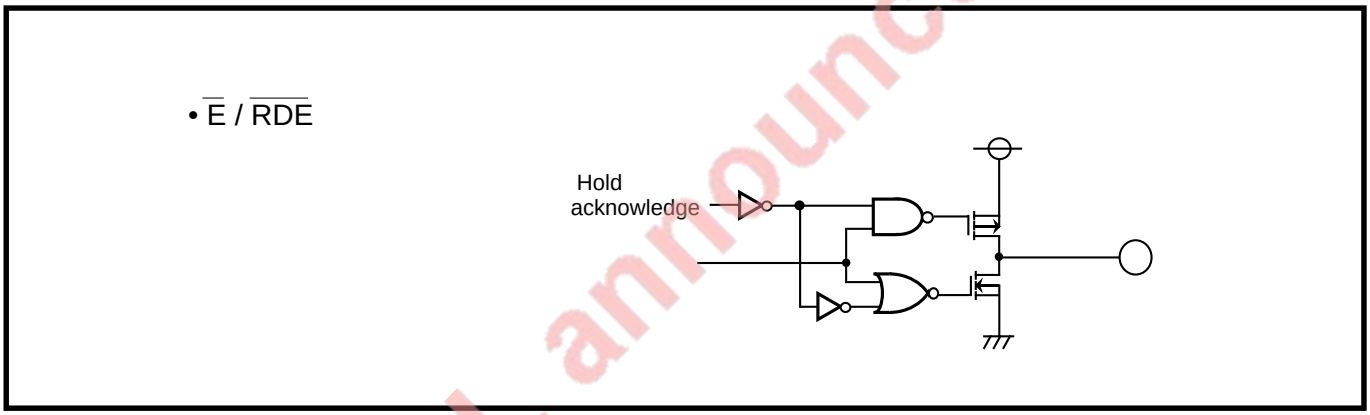


Fig. 3.2.2 Port peripheral circuits (2)

EOL announced

CHAPTER 4

INTERRUPTS

EOL announced

4.1 Overview
4.2 Interrupt sources
4.3 Interrupt control
4.4 Interrupt priority level
4.5 Interrupt priority level detection circuit
4.6 Interrupt priority level detection time
4.7 How interrupts are processed (from acceptance of interrupt request till execution of interrupt routine)
4.8 Return from interrupt routine
4.9 Multiple interrupts
4.10 External interrupts ($\overline{\text{INTi}}$ interrupt)
4.11 Precautions for interrupts

INTERRUPTS

Interrupts of the 7735 Group are the same as those of the 7733 Group. Therefore, for interrupts, refer to the corresponding sections in part 1:

- **“4.1 Overview (page 4-2 in part 1)**
- **“4.2 Interrupt sources (page 4-4 in part 1)**
- **“4.3 Interrupt control (page 4-6 in part 1)**
- **“4.4 Interrupt priority level (page 4-10 in part 1)**
- **“4.5 Interrupt priority level detection circuit (page 4-11 in part 1)**
- **“4.6 Interrupt priority level detection time (page 4-13 in part 1)**
- **“4.7 How interrupts are processed (from acceptance of interrupt request till execution of interrupt routine) (page 4-14 in part 1)**
- **“4.8 Return from interrupt routine (page 4-17 in part 1)**
- **“4.9 Multiple interrupts (page 4-17 in part 1)**
- **“4.10 External interrupts ($\overline{\text{INT}}_i$ interrupt) (page 4-19 in part 1)**
- **“4.11 Precautions for interrupts (page 4-23 in part 1)**

EOL announced

CHAPTER 5

KEY INPUT INTERRUPT FUNCTION

EOL announced

5.1 Overview
5.2 Block description
5.3 Initial setting example for related registers

KEY INPUT INTERRUPT FUNCTION

The key input interrupt function of the 7735 Group is the same as that of the 7733 Group. Therefore, the key input interrupt function, refer to the corresponding sections in part 1:

- **“5.1 Overview (page 5-2 in part 1)**
- **“5.2 Block description (page 5-3 in part 1)**
- **“5.3 Initial setting example for related registers (page 5-7 in part 1)**

EOL announced

CHAPTER 6

TIMER A

6.1 Overview
6.2 Block description
6.3 Timer mode
6.4 Event counter mode
6.5 One-shot pulse mode
6.6 Pulse width modulation (PWM) mode

EOL announced

TIMER A

Timer A of the 7735 Group is the same as that of the 7733 Group. Therefore, for timer A, refer to the corresponding sections in part 1:

- **“6.1 Overview” (page 6-2 in part 1)**
- **“6.2 Block description” (page 6-3 in part 1)**
- **“6.3 Timer mode” (page 6-9 in part 1)**
- **“6.4 Event counter mode” (page 6-19 in part 1)**
- **“6.5 One-shot pulse mode” (page 6-32 in part 1)**
- **“6.6 Pulse width modulation (PWM) mode” (page 6-41 in part 1)**

EOL announced

CHAPTER 7
TIMER B

7.1 Overview
7.2 Block description
7.3 Timer mode
7.4 Event counter mode
7.5 Pulse period/Pulse width measurement mode
7.6 Clock timer

EOL announced

TIMER B

Timer B of the 7735 Group is the same as that of the 7733 Group. Therefore, for timer B, refer to the corresponding sections in part 1:

- **“7.1 Overview” (page 7-2 in part 1)**
- **“7.2 Block description” (page 7-3 in part 1)**
- **“7.3 Timer mode” (page 7-10 in part 1)**
- **“7.4 Event counter mode” (page 7-17 in part 1)**
- **“7.5 Pulse period/Pulse width measurement mode” (page 7-25 in part 1)**
- **“7.6 Clock timer” (page 7-34 in part 1)**

EOL announced

CHAPTER 8

SERIAL I/O

8.1 Overview
8.2 Block description
8.3 Clock synchronous serial I/O mode
8.4 Clock asynchronous serial I/O (UART) mode

EOL announced

SERIAL I/O

The serial I/O of the 7735 Group is the same as that of the 7733 Group. Therefore, for serial I/O, refer to the corresponding sections in part 1:

- **“8.1 Overview” (page 8-2 in part 1)**
- **“8.2 Block description” (page 8-4 in part 1)**
- **“8.3 Clock synchronous serial I/O mode” (page 8-21 in part 1)**
- **“8.4 Clock asynchronous serial I/O (UART) mode” (page 8-44 in part 1)**

EOL announced

CHAPTER 9

A-D CONVERTER

9.1 Overview
9.2 Block description
9.3 A-D conversion method
9.4 Absolute accuracy and Differential non-linearity error
9.5 One-shot mode
9.6 Repeat mode
9.7 Single sweep mode
9.8 Repeat sweep mode
9.9 Precautions for A-D converter

EOL announced

A-D CONVERTER

The A-D converter of the 7735 Group is the same as that of the 7733 Group. Therefore, for the A-D converter, refer to the corresponding sections in part 1:

- **“9.1 Overview” (page 9-2 in part 1)**
- **“9.2 Block description” (page 9-3 in part 1)**
- **“9.3 A-D conversion method” (page 9-11 in part 1)**
- **“9.4 Absolute accuracy and Differential non-linearity error” (page 9-14 in part 1)**
- **“9.5 One-shot mode” (page 9-17 in part 1)**
- **“9.6 Repeat mode” (page 9-20 in part 1)**
- **“9.7 Single sweep mode” (page 9-23 in part 1)**
- **“9.8 Repeat sweep mode” (page 9-27 in part 1)**
- **“9.9 Precautions for A-D converter” (page 9-31 in part 1)**

EOL announced

CHAPTER 10
WATCHDOG TIMER

10.1 Block description
10.2 Operation description
10.3 Precautions for watchdog timer

EOL announced

WATCHDOG TIMER

10.2 Operation description

Concerning chapter “10. WATCHDOG TIMER,” the 7735 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

- **“10.2 Operation description”**

The following sections are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“10.1 Block description” (page 10-2 in part 1)**
- **“10.3 Precautions for watchdog timer” (page 10-10 in part 1)**

10.2 Operation description

Concerning section “10.2 Operation description,” the 7735 Group differs from the 7733 Group in the following:

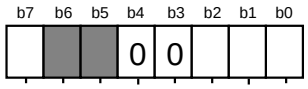
- **Figures 10.2.2 and 10.2.3**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“10.2 Operation description” (page 10-5 in part 1)**

EOL announced

In the M37735MHBXXXFP, set bit 3 of the oscillation circuit control register 1 to “0.”



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P7$_6$ functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P7$_6$ functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 4)**	Must be fixed to “0” in the mask ROM and external ROM versions **(Note 1)**.		0	RW
	Must be fixed to “0” in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to “0” **(Note 3)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing “1” to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown below.
2: Because this bit is “1” at reset, clear this bit to “0” with the initial setting program after reset.
3: The case where data “01010101_2” is written with the procedure shown below is not included.
4: For the 7733 Group, refer to **Figure 14.3.3 in part 1.**
5: ▨ represents that bits 3 to 7 are not used for the watchdog timer.

EOL announced

Fig. 10.2.2 Structure of oscillation circuit control register 1

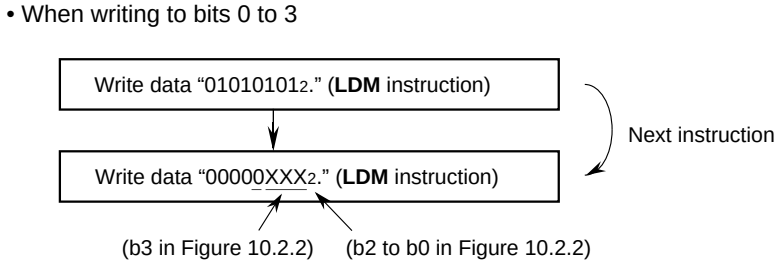


Fig. 10.2.3 Procedure for writing data to oscillation circuit control register 1

MEMO

EOL announced

CHAPTER 11
STOP AND WAIT MODES

11.1 Overview
11.2 Clock generating circuit
11.3 Stop mode
11.4 Wait mode

EOL announced

STOP AND WAIT MODES

11.2 Clock generating circuit

Concerning chapter “11. STOP AND WAIT MODES,” the 7735 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“11.2 Clock generating circuit”**
- **“11.3 Stop mode”**
- **“11.4 Wait mode”**

The following section of the 7735 Group is the same as that of the 7733 Group. Therefore, for this section, refer to part 1:

- **“11.1 Overview” (page 11-2 in part 1)**

11.2 Clock generating circuit

Concerning section “11.2 Clock generating circuit,” the 7735 Group differs from the 7733 Group in the following:

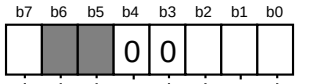
- **Figures 11.2.3 and 11.2.4**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“11.2 Clock generating circuit” (page 11-3 in part 1)**

In the M37735MHBXXXFP, be sure to set bit 3 of the oscillation circuit control register 1 to “0.”

EOL announced



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin $P7_6$ functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin $P7_6$ functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 4)**	Must be fixed to “0” in the mask ROM and external ROM versions **(Note 1)**.		0	RW
	Must be fixed to “0” in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to “0” **(Note 3)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing “1” to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 11.2.4.
2: Because this bit is “1” at reset, clear this bit to “0” with the initial setting program after reset.
3: The case where data “01010101_2” is written with the procedure shown in Figure 11.2.4. is not included.
4: For the 7733 Group, refer to **Figure 11.2.3 in part 1.**
5: ▢ represents that bits 3 to 7 are not used for the stop and wait modes.

Fig. 11.2.3 Structure of oscillation circuit control register 1

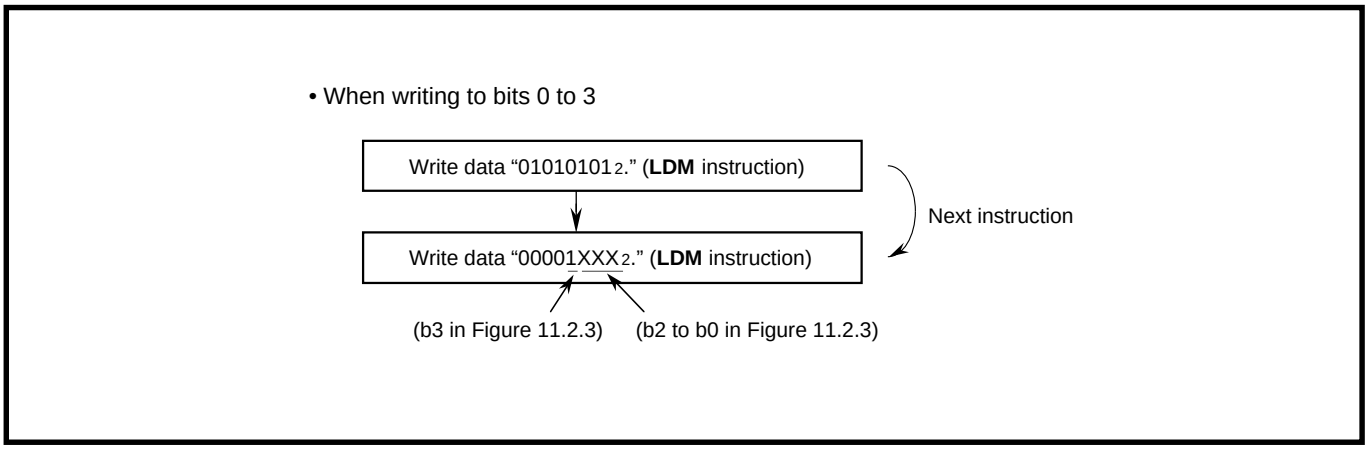


Fig. 11.2.4 Procedure for writing data to oscillation circuit control register 1

11.3 Stop mode

Concerning section "11.3 Stop mode," the 7735 Group differs from the 7733 Group in the following:

- **Table 11.3.2 and Figure 11.3.1**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"11.3 Stop mode" (page 11-6 in part 1)**

EOL announced

STOP AND WAIT MODES

11.3 Stop mode

Table 11.3.2 Pin state in stop mode

Pins	State			
	Single-chip mode	Memory expansion mode	Microprocessor mode	
			When the standby state selection bit*1 = "0"	When the standby state selection bit*1 = "1"
$\overline{E}$	■ When the signal output disable selection bit = "0," "H" level is output ■ When the signal output disable selection bit = "1," "L" level is output.	Same as in the microprocessor mode	"H" level is output.	■ When the signal output disable selection bit = "0," "H" level is output. ■ When the signal output disable selection bit = "1," "L" level is output.
$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$, $\overline{CS0}$–$\overline{CS4}$, $\overline{RSMP}$, $\overline{HLDA}$				Output levels can be set. (Refer to section **"11.3.1 Output levels of external bus and bus control signals in stop mode."**)
ALE			"L" level is output.	
A0/D0–A15/D15, A16, A17			Retains the same state in which the **STP** instruction is executed.	
P42/ϕ1	■ When the clock ϕ1 output selection bit*2 = "1" ϕ1: "L" level is output. ■ When the clock ϕ1 output selection bit = "0" P42: Retains the same state in which the **STP** instruction is executed.		■ When the signal output disable selection bit*3 = "0" ϕ1: "L" level is output. ■ When the signal output disable selection bit = "1" P42: Bit 2's value of the port P4 register is output **(Note)**.	
Ports	P0 to P8 (not including P42) : Retains the same state in which the **STP** instruction is executed.	P43 to P47, P5 to P8 :Retains the same state in which the **STP** instruction is executed.		

Standby state selection bit*1: Bit 0 at address 6D16 (Refer to **Figure 11.3.1.**)
Clock ϕ1 output selection bit*2: Bit 7 at address 5E16
(Refer to section **"12.1 Signals required for accessing external devices."**)
Signal output disable selection bit*3: Bit 6 at address 6C16
(Refer to section **"12.1 Signals required for accessing external devices."**)

Note: Make sure to set bit 2 of the port P4 direction register to "1."

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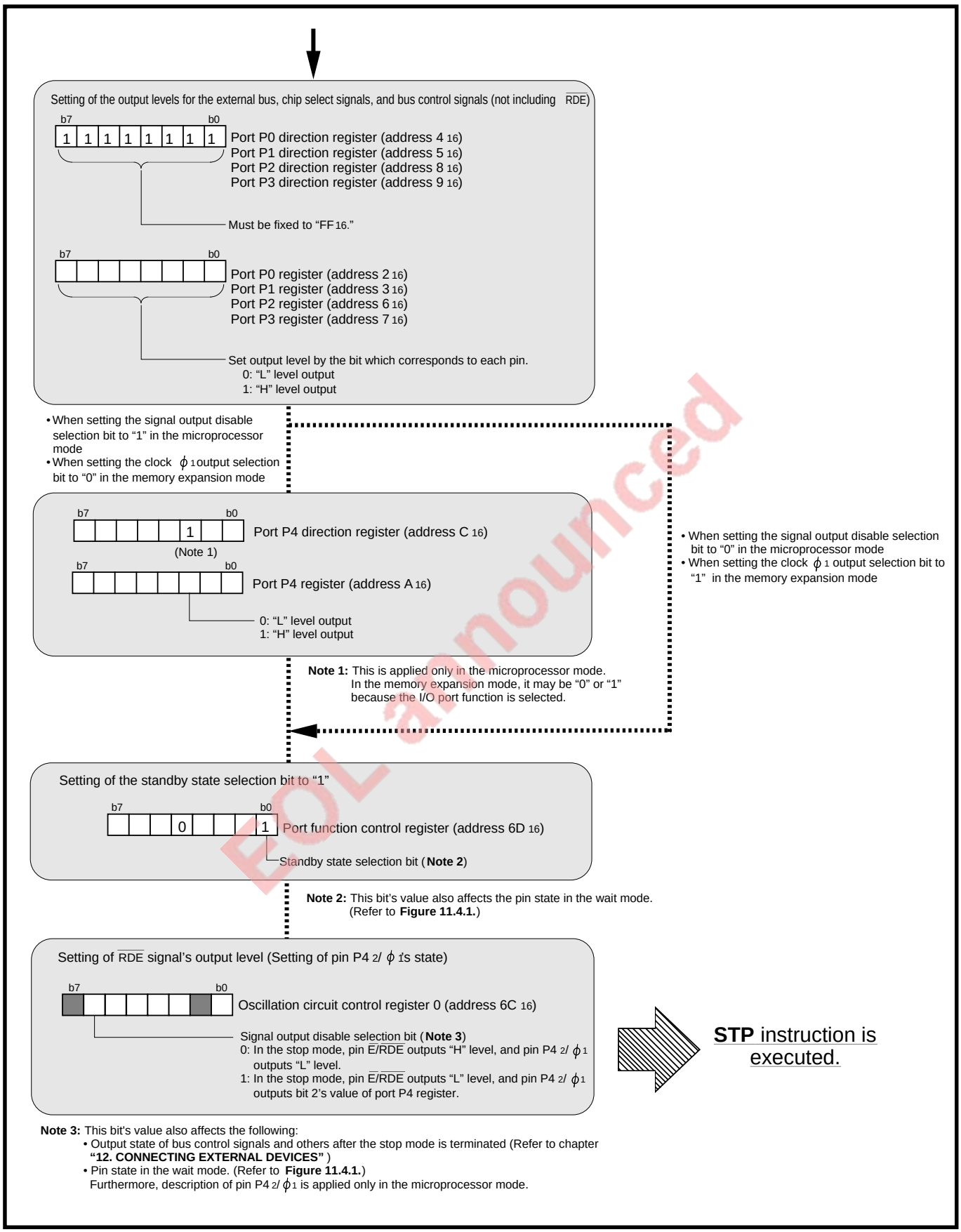


EOL announced

Fig. 11.3.1 Output level setting example in stop mode (Memory expansion or Microprocessor mode)

11.4 Wait mode

Concerning section “11.4 Wait mode,” the 7735 Group differs from the 7733 Group in the following:

- **Table 11.4.2 and Figure 11.4.1**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“11.4 Wait mode” (page 11-13 in part 1)**

EOL announced

Table 11.4.2 Pin state in wait mode

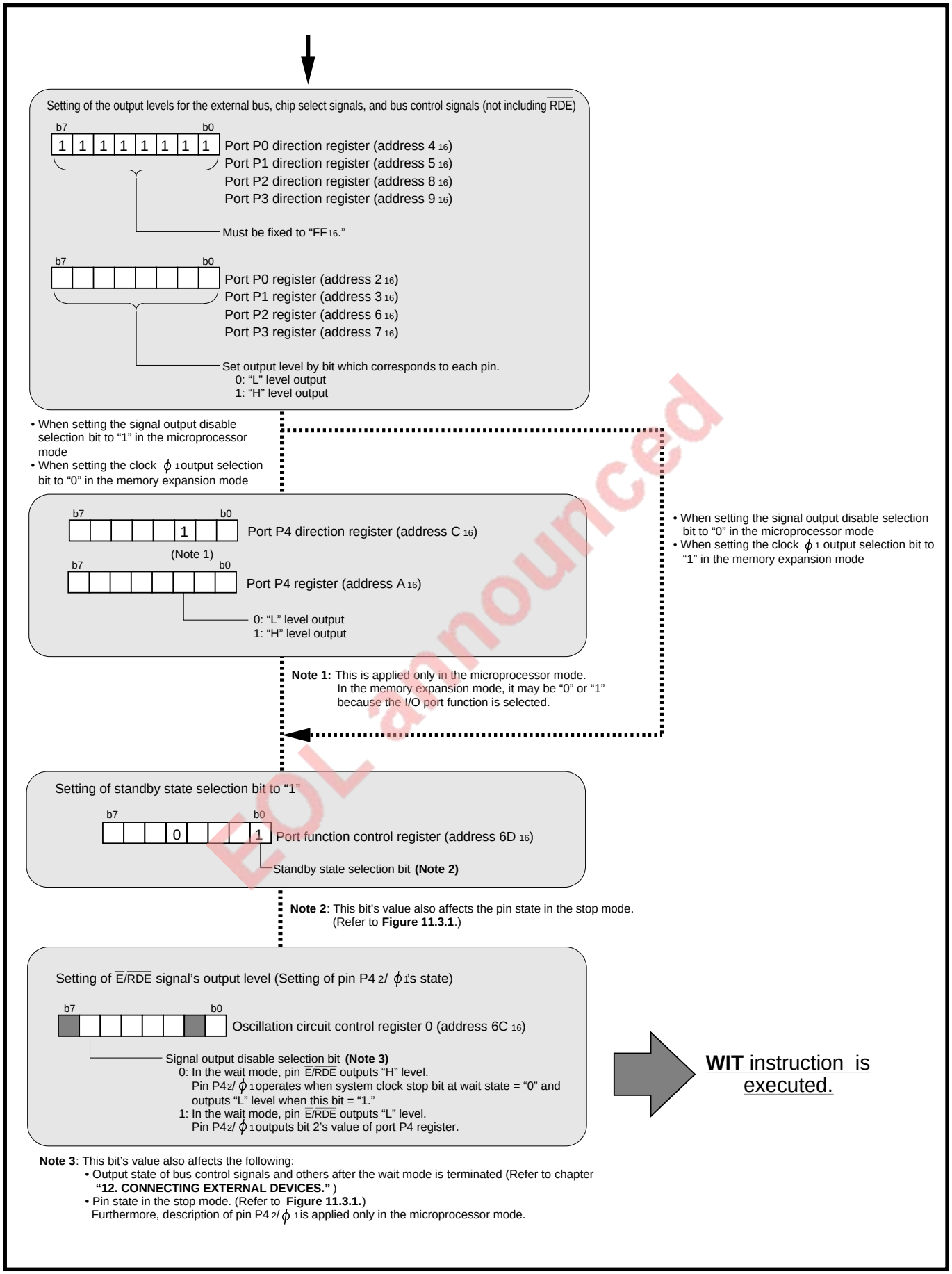
Pins	State			
	Single-chip mode	Memory expansion mode	Microprocessor mode	
			When the standby state selection bit*1 = "0"	When the standby state selection bit*1 = "1"
$\overline{E}$	■ When the signal output disable selection bit = "0," "H" level is output. ■ When the signal output disable selection bit = "1," "L" level is output.	Same as in the microprocessor mode	"H" level is output.	■ When the signal output disable selection bit = "0," "H" level is output. ■ When the signal output disable selection bit = "1," "L" level is output.
$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$, $\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$, $\overline{HLDA}$				Output level can be set. (Refer to section **"11.4.2 Output levels of external bus and bus control signals in wait mode"**)
ALE			"L" level is output.	
A_0/D_0–A_{15}/D_{15}, A_{16}, A_{17}			Retains the same state in which the **WIT** instruction is executed.	
$P4_2/\phi_1$	■ When the clock ϕ_1 output selection bit*2 = "1" ϕ_1: Operating when the system clock stop bit at wait state*4 = "0." "L" level is output when the system clock stop bit at wait state = "1." ■ When the clock ϕ_1 output selection bit = "0" $P4_2$: Retains the same state in which the **WIT** instruction is executed.		■ When the signal output disable selection bit*3 = "0" ϕ_1: Stopped when the system clock stop bit at wait state = "0." "L" level is output when the system clock stop bit at wait state = "1." ■ When the signal output disable selection bit = "1" $P4_2$: Bit 2's value of port P4 register is output **(Note)**.	
Ports	P0 to P8 (not including $P4_2$) : Retains the same state in which the **WIT** instruction is executed.		$P4_3$ to $P4_7$, P5 to P8 : Retains the same state in which the **WIT** instruction is executed.	

Standby state selection bit*1: Bit 0 at address $6D_{16}$ (Refer to **Figure 11.4.1.**)
Clock ϕ_1 output selection bit*2: Bit 7 at address $5E_{16}$
(Refer to section **"12.1 Signals required for accessing external devices."**)
Signal output disable selection bit*3: Bit 6 at address $6C_{16}$
(Refer to section **"12.1 Signals required for accessing external devices."**)
System clock stop bit at wait state*4: Bit 5 at address $6C_{16}$
(Refer to section **"11.4.1 State of clocks f_2 to f_{512} in wait mode."**)

Note: Make sure to set bit 2 of the port P4 direction register to "1."

EOL announced

11.4 Wait mode



EOL announced

Fig. 11.4.1 Output level setting example in wait mode (Memory expansion or Microprocessor mode)

CHAPTER 12
CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices
12.2 Software wait
12.3 Ready function
12.4 Hold function

EOL announced

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

Functions for connecting external devices are described in this chapter.
Reading or writing data from or to external devices are performed by the bus interface unit (BIU). (Refer to section **"2.2 Bus interface unit."**) The BIU operates on the basis of internal enable signal $\overline{E}$ (usually, internal clock ϕ divided by 2) but does not output internal enable signal $\overline{E}$ to the external. The BIU outputs signals $\overline{RDE}$, $\overline{WEL}$, and $\overline{WEH}$.
Signals $\overline{RDE}$, $\overline{WEL}$, and $\overline{WEH}$ are generated from internal enable signal $\overline{E}$ and are output at the same timing as that of internal enable signal $\overline{E}$. When external devices are accessed, the BIU outputs some of these signals, in other words, outputs only signals which are required for the access at that time.

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12.1 Signals required for accessing external devices

Functions and operations of signals required for accessing external devices are described below.
When connecting external devices which require a long access time, refer to sections **“12.2 Software wait,” “12.3 Ready function,”** and **“12.4 Hold function,”** also.
When connecting external devices, make sure that the microcomputer operates in the memory expansion or microprocessor mode. (Refer to section **“2.5 Processor modes.”**) When the microcomputer operates in these modes, ports P0 to P4 and pin $\overline{\text{E/RDE}}$ function as I/O pins of signals required for accessing external devices.
Figure 12.1.1 shows the pin configuration in the memory expansion or microprocessor mode. Table 12.1.1 lists the functions of ports P0 to P4 and pin $\overline{\text{E/RDE}}$ in the memory expansion or microprocessor mode.

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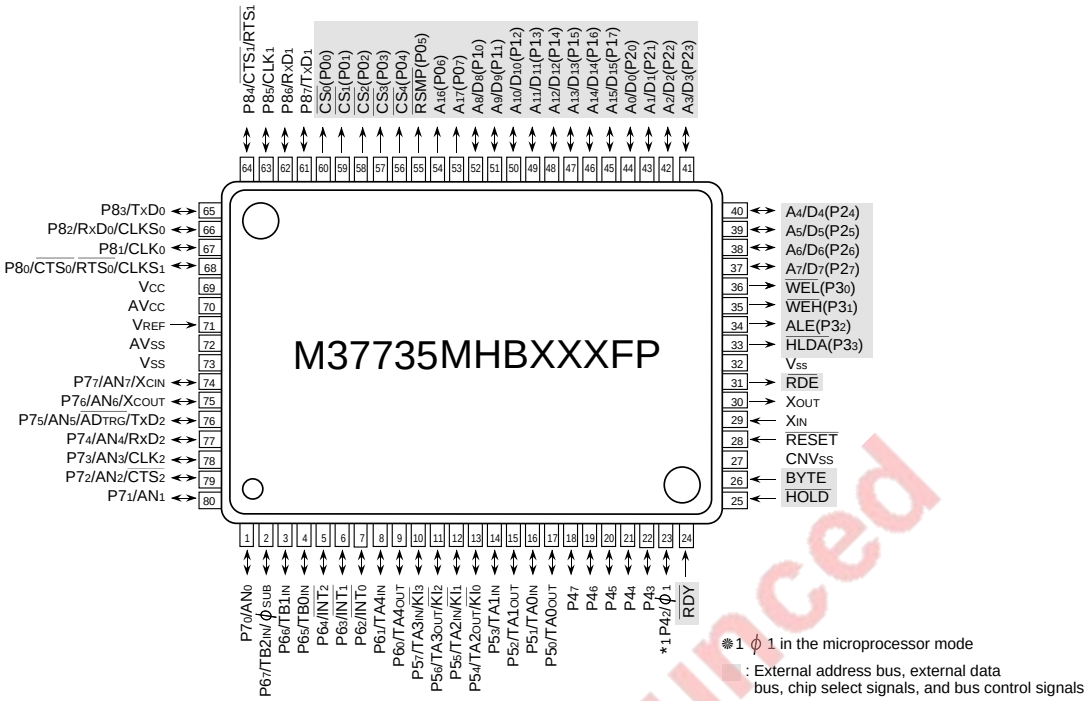
CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

When external data bus is 16 bits wide (BYTE = “L”)

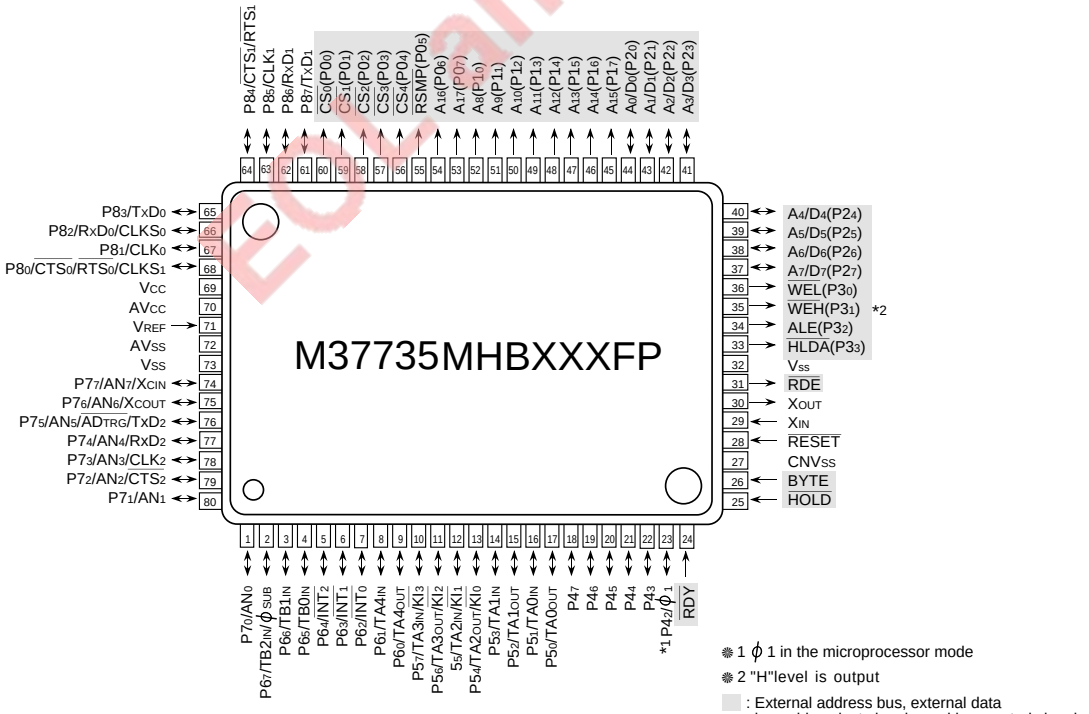


*1 ϕ 1 in the microprocessor mode

: External address bus, external data bus, chip select signals, and bus control signals

By setting the port register and port direction register which correspond to the port shown in ( ), the corresponding pin’s level can be fixed in the stop or wait mode.

When external data bus is 8 bits wide (BYTE = “H”)



*1 ϕ 1 in the microprocessor mode

*2 "H"level is output

: External address bus, external data bus, chip select signals, and bus control signals

By setting the port register and port direction register which correspond to the port shown in ( ), the corresponding pin’s level can be fixed in the stop or wait mode.

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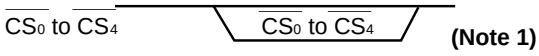
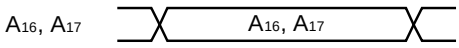
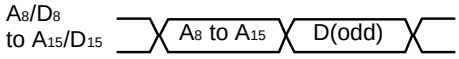
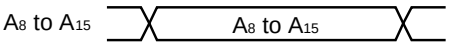
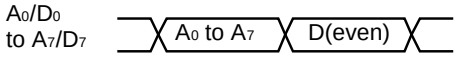
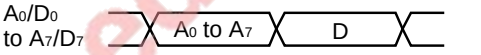
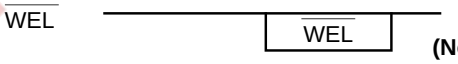
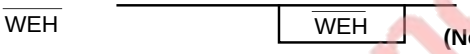
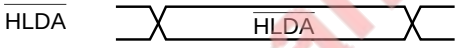
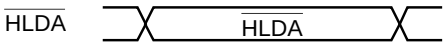
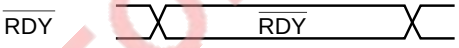
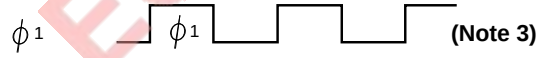
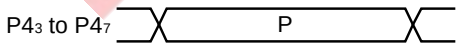
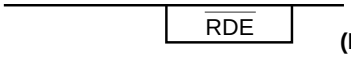
Fig. 12.1.1 Pin configuration in memory expansion or microprocessor mode (Top view)

Table 12.1.1 Functions of ports P0 to P4 and pin $\overline{E}/\overline{RDE}$ in memory expansion or microprocessor mode

Pin name \ External data bus width	16 bits (BYTE = "L")	8 bits (BYTE = "H")
$\overline{CS_0}$ to $\overline{CS_4}$	 **(Note 1)**	
$\overline{RSMP}$		
A_{16}, A_{17}		
A_8/D_8 to A_{15}/D_{15}	 D(odd) : Data at odd address	
A_0/D_0 to A_7/D_7	 D(even) : Data at even address	 D : Data
$\overline{WEL}$	**(Note 2)**	 **(Note 2)**
$\overline{WEH}$	 **(Note 2)**	("H" level output)
ALE		
$\overline{HLDA}$		
$\overline{HOLD}$		
$\overline{RDY}$		
ϕ_1	 **(Note 3)**	
$P4_3$ to $P4_7$	 P : Functions as programmable I/O port	
$\overline{E}/\overline{RDE}$	 **(Note 2)**	

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Notes 1: When the internal area is accessed, signals $\overline{CS0}$ to $\overline{CS4}$ are not output. (Output levels are fixed to "H.")

2: These signals are affected by the signal output disable selection bit (bit 6 at address 6C $_{16}$). (Refer to **Table 12.1.4**.)

3: In the memory expansion mode, this pin functions as a programmable I/O port. Furthermore, it can be switched to be a clock ϕ_1 output pin when selected by software. In the microprocessor mode, this signal is affected by the signal output disable selection bit (bit 6 at address 6C $_{16}$). (Refer to **Table 12.1.3**.)

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

12.1.1 External bus (A_0/D_0 to A_{15}/D_{15}, A_{16} and A_{17}) and chip select signals ($\overline{CS_0}$ to $\overline{CS_4}$)

The address (A_0 to A_{17}) and chip select signals are output and specify the external area. Figures 12.1.2 and 12.1.3 show the external areas specified by these signals. An area specified by a chip select signal does not the internal area. (When the internal area is accessed, the chip select signal is not output.)

Pins A_8 to A_{15} of the external address bus and pins D_0 to D_{15} of the external data bus share the same pins. When pin BYTE's level, which is described later, is "L" (in other words, when the external data bus is 16 bits wide), pins A_0/D_0 to A_{15}/D_{15} perform address output and data input/output with the time-sharing method. When pin BYTE's level is "H" (in other words, when the external data bus is 8 bits wide), pins A_0/D_0 to A_7/D_7 perform address output and data input/output with the time-sharing method and pins A_8 to A_{15} output the address.

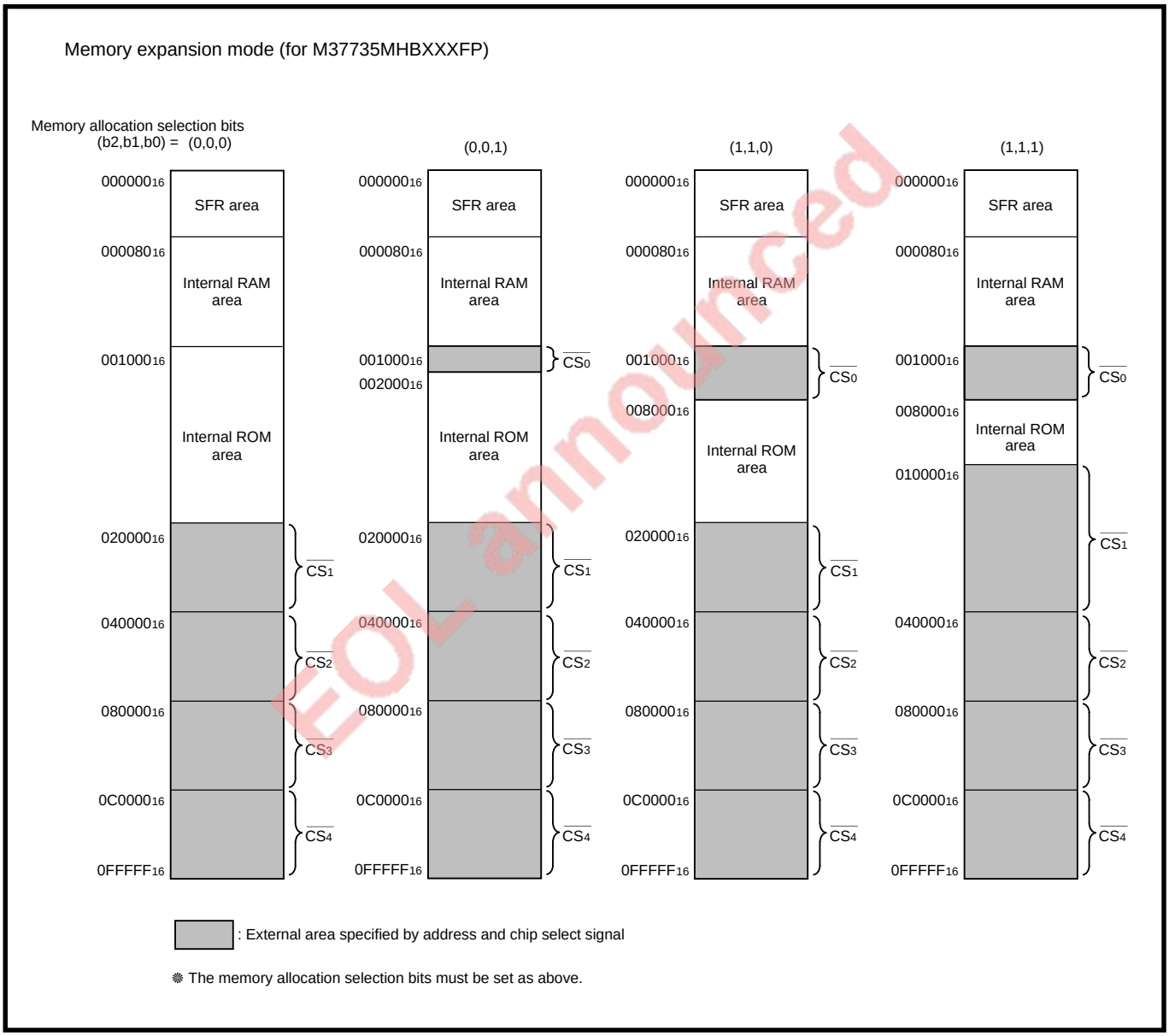

Fig. 12.1.2 External area (Memory expansion mode)

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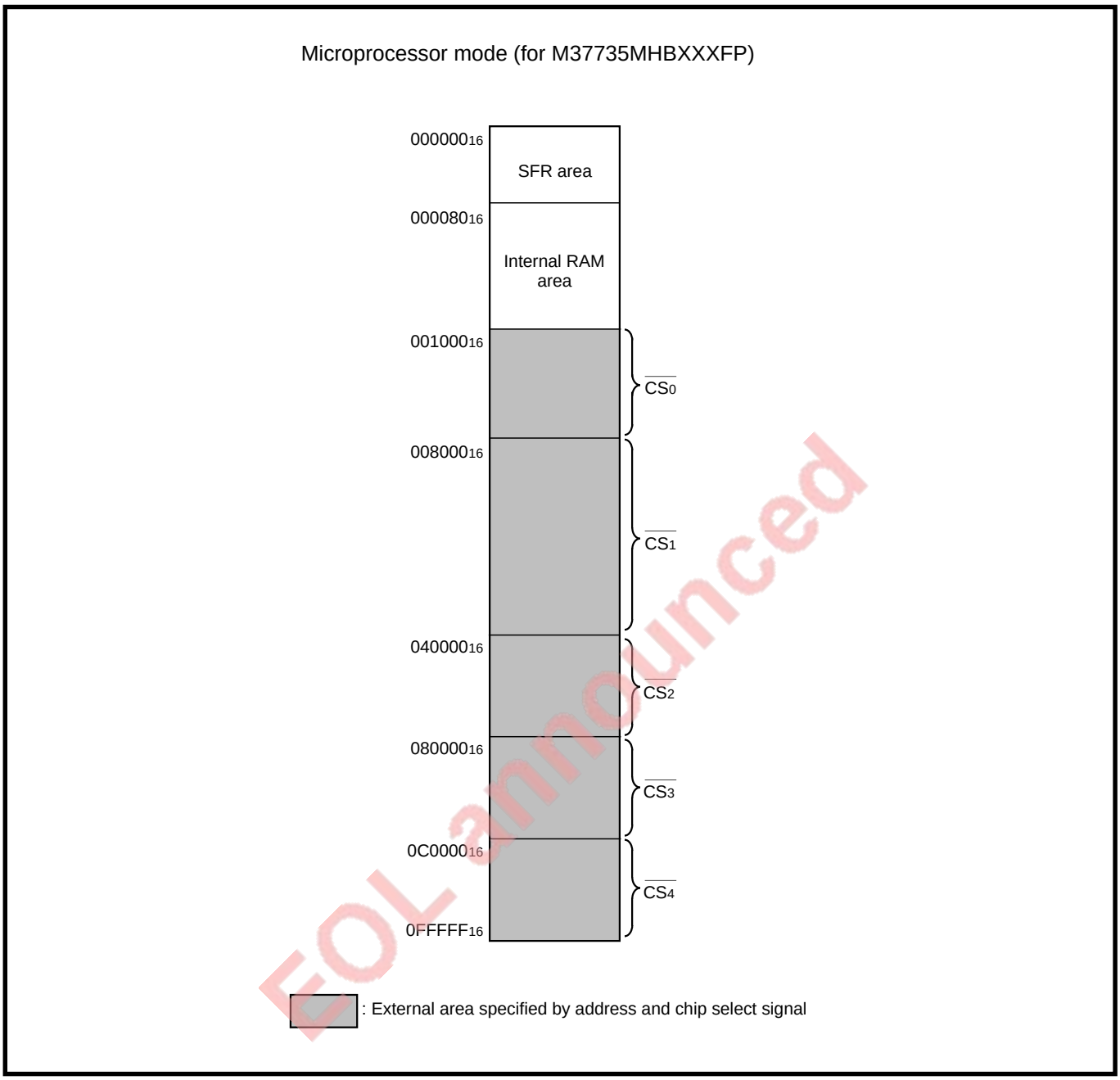

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Fig. 12.1.3 External area (Microprocessor mode)

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

12.1.2 External data bus width selection signal (Pin BYTE's level)

This signal is used to select the external data bus width from 8 bits and 16 bits. When this signal level is "L," the external data bus is 16 bits wide; when this signal level is "H," the external data bus is 8 bits wide. (Refer to **Table 12.1.1.**) This signal level must be fixed to either "H" or "L."

This signal is valid only for the external areas. (When the internal area is accessed, the data bus is always 16 bits wide.)

12.1.3 Read enable signal ($\overline{RDE}$) and Write enable signals ($\overline{WEL}$, $\overline{WEH}$)

These signals are output when data is read or written from or to the external area. When the internal area is accessed, these signals are stopped at "H" level by setting the signal output disable selection bit (bit 6 at address $6C_{16}$) to "1." (Refer to **Table 12.1.4.**)

Table 12.1.2 Functions of read enable signal and write enable signals

External data bus width	$\overline{RDE}$	$\overline{WEL}$	$\overline{WEH}$	External data bus state
16 bits (BYTE = "L")	H	H	H	———
	L	H	H	Data is read out.
	H	L	H	1-byte data is written to even address.
	H	H	L	1-byte data is written to odd address.
	H	L	L	1-word data is written.
8 bits (BYTE = "H")	H	H	H	———
	L	H	H	Data is read out.
	H	L	H	Data is written.

12.1.4 Address latch enable signal (ALE)

This signal is used to latch an address from a multiplexed signal. This multiplexed signal consists of the address and data and is input or output to or from pins A_0/D_0 to A_{15}/D_{15}, A_{16}/D_0 to A_{23}/D_7. When this signal level is "H," take the address into a latch and output it simultaneously. When this signal level is "L," retain the latched address.

12.1.5 Signals related to ready function ($\overline{RDY}$, $\overline{RSMP}$)

These signals are required to use the ready function. (Refer to section **"12.3 Ready function."**)

12.1.6 Signals related to hold function ($\overline{HOLD}$, $\overline{HLDA}$)

These signals are required to use the hold function. (Refer to section **"12.4 Hold function."**)

12.1.7 Clock ϕ_1

This signal has the same period as internal clock ϕ.

Whether clock ϕ_1 is output or stopped can be selected by software. However, the method of this selection depends on the processor mode. Table 12.1.3 lists the method to select whether to output or stop clock ϕ_1. Figure 12.1.4 shows the clock ϕ_1 output start timing.

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Table 12.1.3 Method to select whether to output or stop clock ϕ1

Processor mode	Single-chip or Memory expansion mode	Microprocessor mode
Clock ϕ1 output	Set the clock ϕ1 output selection bit*1 to "1."	Clear the signal output disable selection bit*2 to "0."
Clock ϕ1 stopped	Clear the clock ϕ1 output selection bit to "0." (Pin P42 functions as a programmable I/O port.)	Set the signal output disable selection bit to "1." **(Note)**
Remark	Clock ϕ1 is stopped after reset. The signal output disable selection bit is ignored.	Clock ϕ1 is output after reset. The clock ϕ1 output selection bit is ignored.

Clock ϕ1 output selection bit*1: Bit 7 at address 5E16

Signal output disable selection bit*2: Bit 6 at address 6C16 (Refer to **Table 12.1.4**.)

Note: When bit 2 at address C16 (Port P4 direction register) is set to "1," bit 2 of the port P4 register is output.

Table 12.1.4 Functions of signal output disable bit

Processor mode	Conditions	Each signal's state		
		Signals	Signal output disable selection bit	
			0	1
Memory expansion or Microprocessor mode	When the external area is accessed	$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$	Operating	
	When the internal area is accessed		Operating	Stopped at "H" level
	When the standby state selection bit = "1" in the stop or wait mode	$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$	Stopped at "H" level	Stopped at "L" level
			Stopped (Output levels can be set.) (Refer to **Figures 11.3.1 and 11.4.1**.)	
	When the standby state selection bit = "0" in the stop or wait mode	$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$	Stopped at "H" level	
Microprocessor mode		Clock ϕ1	Operating (independent of the ϕ1 output selection bit)	Stopped **(Note)**
Single-chip mode	When not in the stop or wait mode	Enable signal $\overline{E}$	Operating	Stopped at "L" level
	When in the stop or wait mode		Stopped at "H" level	Stopped at "L" level

❋ All functions listed in Table 12.1.4 are not emulated by a debugger.

❋ For the stop and wait modes and the standby state selection bit, refer to chapter **"11. STOP AND WAIT MODES."**

Note: When bit 2 at address C16 (Port direction register) is set to "1," bit 2 of the port P4 register is output.

:Not affected by the signal output disable selection bit.

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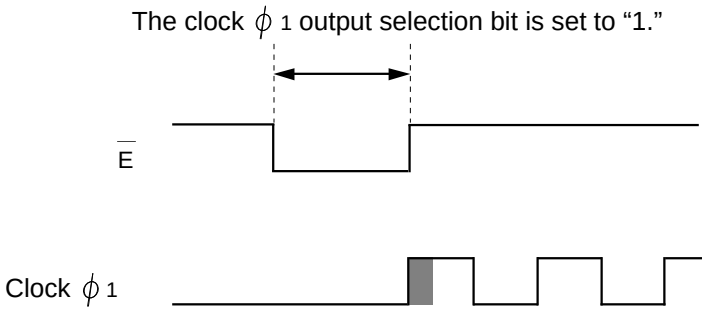
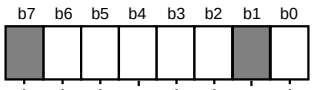
CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices



There is a possibility that the first cycle of clock ϕ 1 output is not an exact square; the shaded section may be lost.
This is applied when "1" is written to the clock ϕ 1 output selection bit while pin P4 2 outputs "L" level.

Fig. 12.1.4 Clock ϕ1 output start timing (when clock ϕ1 output selection bit is set from "0" to "1")



Oscillation circuit control register 0 (address 6C 16)

Bit	Bit name	Functions	At reset	RW
0	XCOUT drivability selection bit	0: Drivability "LOW" 1: Drivability "HIGH"	1	RW (**Note 1**)
1	Not implemented.		Un-defined	–
2	Main clock stop bit	0: Main clock oscillation or external clock input is available. 1: Main clock oscillation or external clock input is stopped.	0	RW (**Note 1**)
3	System clock selection bit	When the port-Xc selection bit = "0," 0: Main clock 1: Main clock divided by 8 When the port-Xc selection bit = "1," 0: Main clock 1: Sub clock	0	RW (**Note 2**)
4	Port-Xc selection bit	0: Operate as I/O ports (P77, P76). 1: Operate as pins XCIN and XCOUT.	0	RW (**Notes 2 and 3**)
5	System clock stop bit at wait state **(Note 4)**	0: Operates in the wait mode. 1: Stopped in the wait mode.	0	RW
6	Signal output disable selection bit	0: Output is enabled. (Refer to **Tables 12.1.3 and 12.1.4**) 1: Output is disabled.	0	RW
7	Not implemented.		Un-defined	–

Notes 1: Nothing can be written to this bit after reset. Writing to this bit is enabled when the port-Xc selection bit = "1."
2: When selecting the sub clock as the system clock, set bit 3 to "1" after setting bit 4 to "1." If the above settings are performed simultaneously, in other words, performed by executing only one instruction, only bit 3 is set to "1."
3: Although this bit can be set to "1," it cannot be cleared to "0" after this bit is once set to "1."
4: When setting the system clock stop bit at wait state to "1," perform it immediately before the **WIT** instruction is executed. Furthermore, clear this bit to "0" immediately after the wait mode is terminated.
5: ▭ represents that bits 0 to 5 and 7 are not used for access control of external area. (Functions of these bits are valid.)

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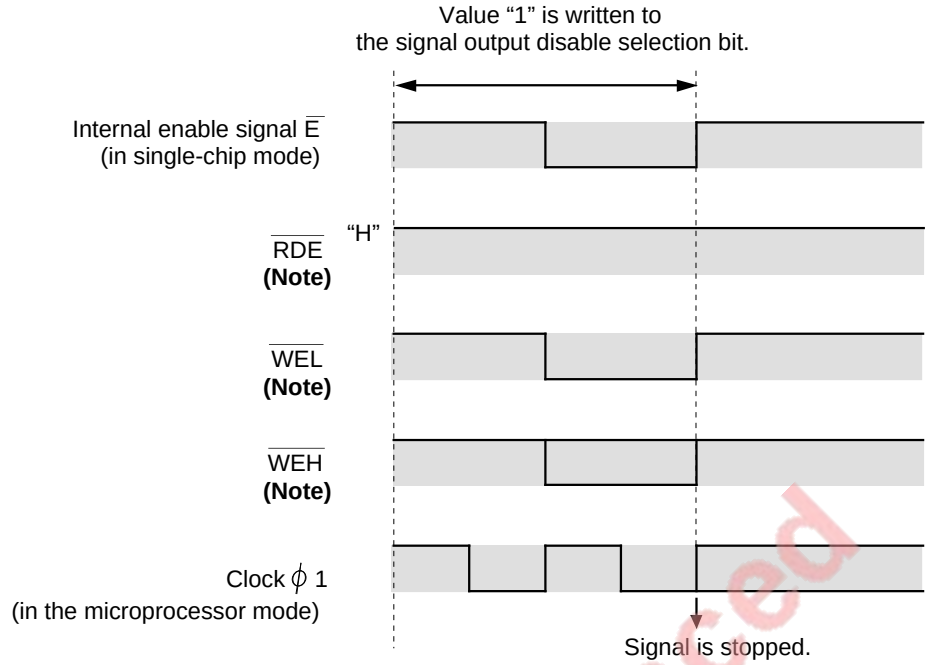
Fig. 12.1.5 Structure of oscillation circuit control register 0



Note: These signals can be stopped only when accessing internal area (in the memory expansion and microprocessor modes).

Fig. 12.1.6 Relationship between setting of signal output disable selection bit and stop timing of each signal

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CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

12.1.8 Operation of bus interface unit (BIU)

Figures 12.1.7 to 12.1.9 show operating waveform examples of signals which are input to or output from the external when accessing external devices. These waveforms are described in relation to the basic operating waveforms. (Refer to section **"2.2.3 Operation of bus interface unit (BIU)."**)

(1) When fetching an instruction into an instruction queue buffer

① When an instruction which is next fetched resides at an even address

When the external data bus is 16 bits wide, the BIU fetches two bytes of the instruction at a time with waveform (a). When the external data bus is 8 bits wide, the BIU fetches only one byte of the instruction with the first half of waveform (i).

② When an instruction which is next fetched resides at an odd address

When the external data bus is 16 bits wide, the BIU fetches only one byte of the instruction with waveform (g). When the external data bus is 8 bits wide, the BIU fetches only one byte of the instruction with the first half of waveform (i).

When branched to an odd address by executing a branch instruction or others with the 16-bit external data bus, at first, the BIU fetches one byte of an instruction with waveform (g) and then fetches instructions by the two bytes with waveform (a).

(2) When reading or writing data from or to memory • I/O

① When accessing 16-bit data which starts from an even address, waveform (a), (b), (i) or (j) is applied.
② When accessing 16-bit data which starts from an odd address, waveform (c), (d), (i) or (k) is applied.
③ When accessing 8-bit data which resides at an even address, waveform (e), (f) or the first half of waveform (i) or (j) is applied.
④ When accessing 8-bit data which resides at an odd address, waveform (g), (h) or the first half of waveform (k) is applied.

For instructions which are affected by data length flag (m) and index register length flag (x), an operation is applied as follows.:
•When "m" or "x" = "0," operation ① or ② is applied.
•When "m" or "x" = "1," operation ③ or ④ is applied.
Settings of flags "m" and "x" and selection of the external data bus width do not affect each other.

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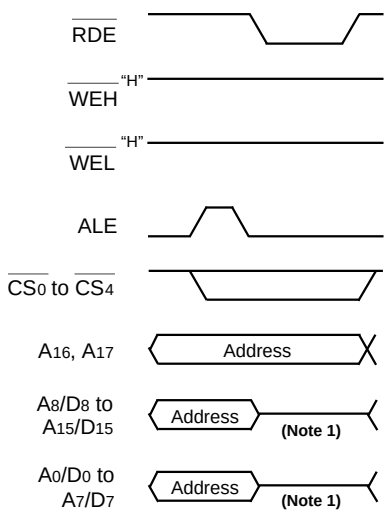
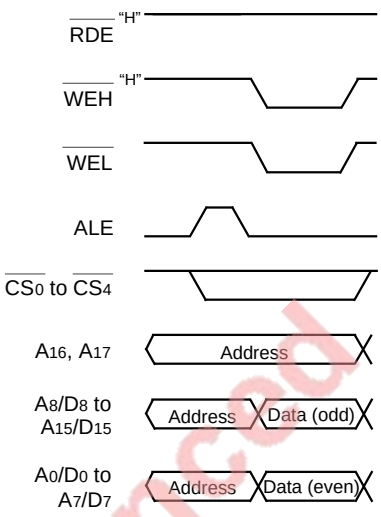
● When external data bus is 16 bits wide (BYTE = “L”)

<16-bit data access>

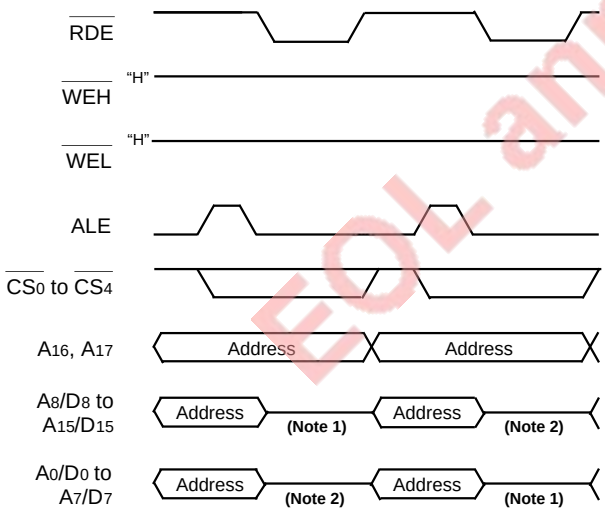
(a) Read starting from even address



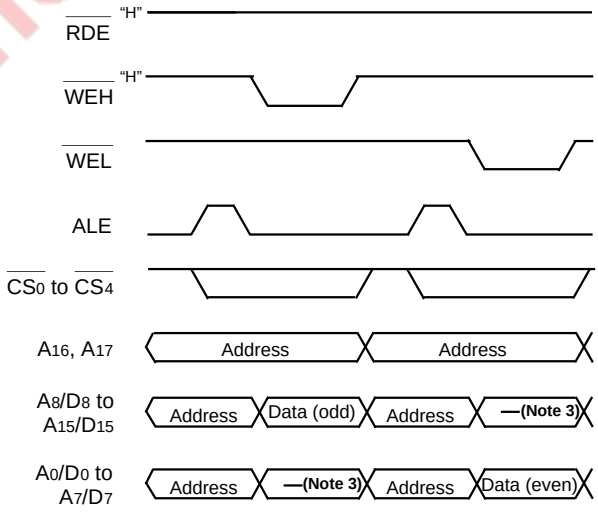
(b) Write starting from even address



(c) Read starting from odd address



(d) Write starting from odd address



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Notes 1: These pins which function as the external bus enter the floating state. While these pins are in the floating state, data on the data bus is fetched into the data buffer of the BIU.

2: These pins which function as the external bus enter the floating state. While these pins are in the floating state, data on the data bus is not fetched fetched into the data buffer of the BIU.

3: Invalid data (Undefined value)

Fig. 12.1.7 Operating waveform example of signals which are input to or output from the external (1)

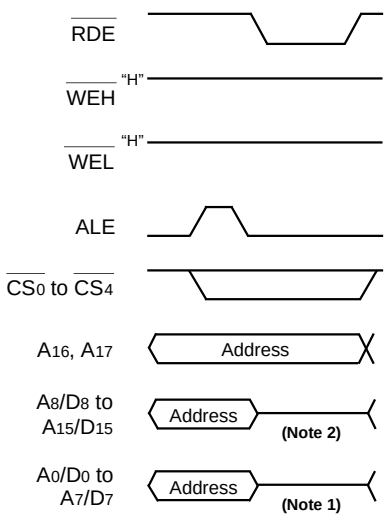
CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices

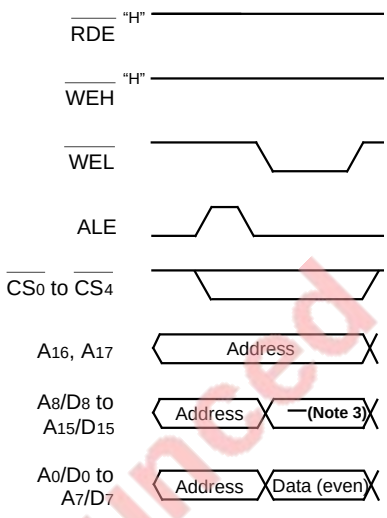
● When external data bus is 16 bits wide (BYTE = “L”)

<8-bit data access>

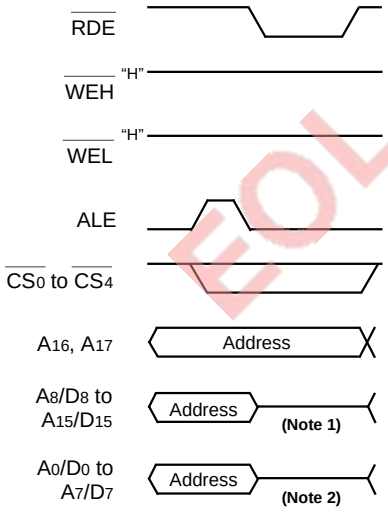
(e) Read starting from even address



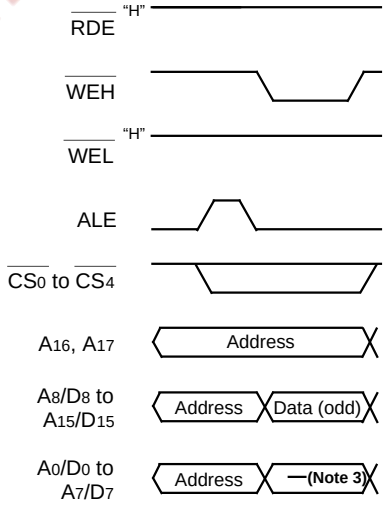
(f) Write starting from even address



(g) Read starting from odd address



(h) Write starting from odd address



EOL announced

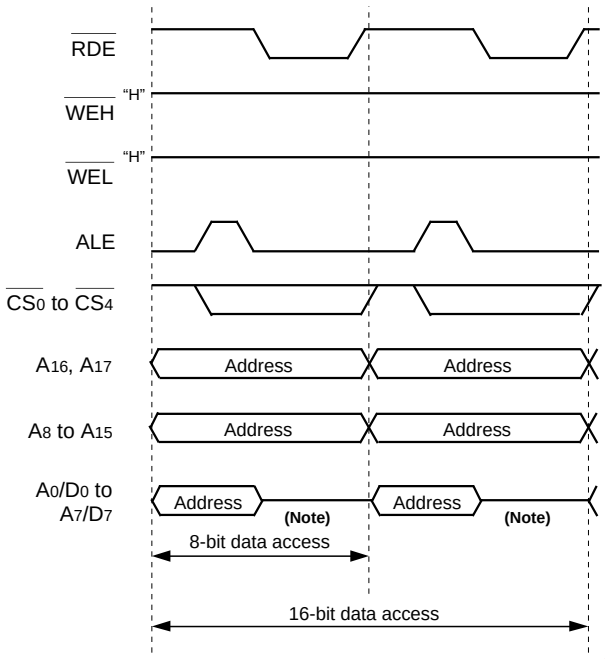
Notes 1: These pins which function as the external bus enter the floating state. While these pins are in the floating state, data on the data bus is fetched into the data buffer of the BIU.
2: These pins which function as the external bus enter the floating state. While these pins are in the floating state, data on the data bus is not fetched into the data buffer of the BIU.
3: Invalid data (Undefined value)

Fig. 12.1.8 Operating waveform example of signals which are input to or output from the external (2)

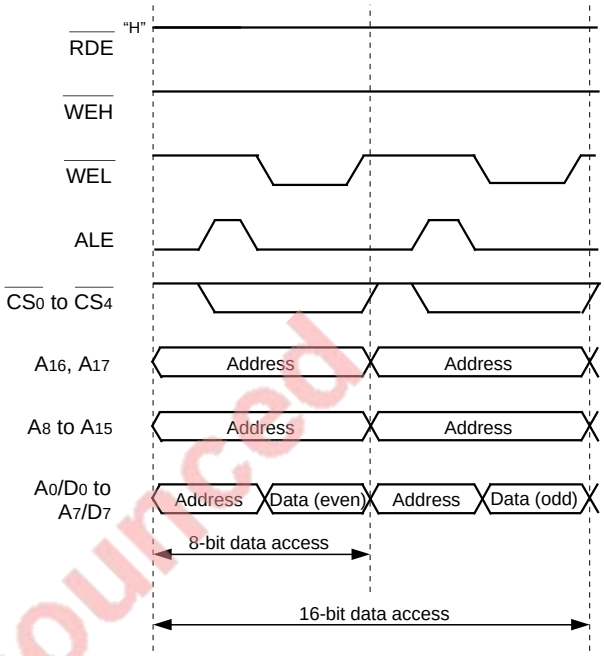
● When external data bus is 8 bits wide (BYTE = “H”)

<8/16-bit data access>

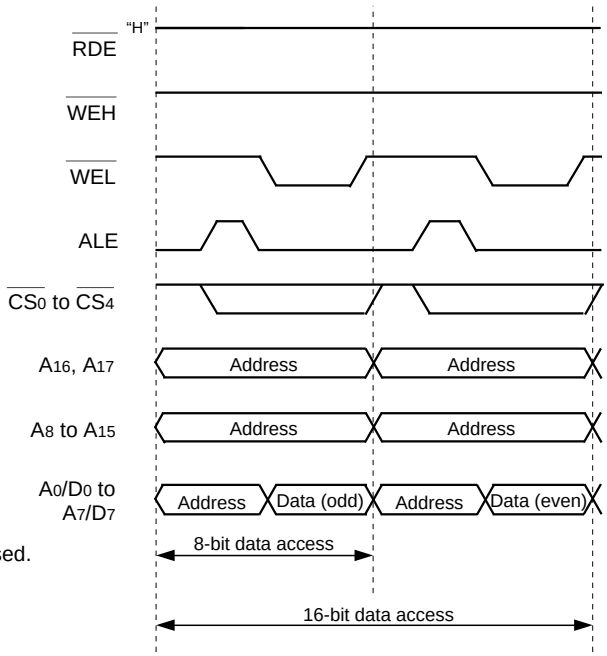
(i) Read starting from even or odd address



(j) Write starting from even address



(k) Write starting from odd address



Note: These pins which function as the external bus enter the floating state. While these pins are in the floating state, data on the data bus is fetched into the data buffer of the BIU.

✵ When 16-bit data is accessed, the low-order 8 bits of data are accessed first, and then, the high-order 8 bits are accessed.

EOL announced

Fig. 12.1.9 Operating waveform example of signals which are input to or output from the external (3)

12.2 Software wait

The software wait facilitates access to external devices which require a long access time. There are two types of software waits: wait 0 and wait 1.

The software wait is set by the wait bit (bit 2 at address $5E_{16}$) and the wait selection bit (bit 0 at address $5F_{16}$). (Refer to **Table 12.2.1.**) Figure 12.2.1 shows the structures of the processor mode register 0 (address $5E_{16}$) and processor mode register 1 (address $5F_{16}$). Figure 12.2.2 shows bus timing examples when the software wait is used.

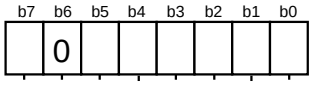
The software wait is valid only for the external area. (Access to the internal areas is always performed with no wait.)

For external devices which can not be accessed even when using the software wait, by using the ready function (signal $\overline{RSMP}$), a wait which is equivalent to 1 cycle of clock ϕ_1 can furthermore be generated. (Refer to section **"12.3 Ready function."**

Table 12.2.1 Setting method of software wait

Wait bit	Wait selection bit	Software wait	Bus cycle
1	0	Invalid (No wait)	Cycle of "internal clock ϕ divided by 2" (clock ϕ_1's cycle × 2)
0	0	Wait 0	"Cycle in the no-wait state" × 2 (clock ϕ_1's cycle × 4)
0	1	Wait 1	"Cycle in the no-wait state" × 1.5 (clock ϕ_1's cycle × 3)

EOL announced



Processor mode register 0 (address 5E 16)

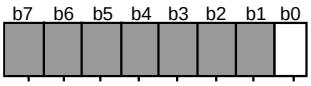
Bit	Bit name	Functions	At reset	RW
0	Processor mode bits	b1 b0 00: Single-chip mode 01: Memory expansion mode 10: Microprocessor mode 11: Do not select.	0	RW
1			0 **(Note 1)**	RW
2	Wait bit	0: Software wait is inserted when accessing external area. 1: No software wait is inserted when accessing external area.	0	RW
3	Software reset bit	Microcomputer is reset by setting this bit to "1." This bit is "0" at reading.	0	WO
4	Interrupt priority detection time selection bits	b5 b4 00: 7 cycles of ϕ 01: 4 cycles of ϕ 10: 2 cycles of ϕ 11: Do not select.	0	RW
5			0	RW
6	Must be fixed to "0."		0	RW
7	Clock ϕ_1 output selection bit **(Note 2)**	0: Clock ϕ_1 output is disabled. (P4 2 functions as a programmable /O port.) 1: Clock ϕ_1 output is enabled. (Port P4 2 functions as a clock ϕ_1 output pin.)	0	RW

Notes 1: When the Vcc-level voltage is applied to pin CNVss, this bit is set to "1" after reset. (At reading, this bit is always "1.")

2: This bit is ignored in the microprocessor mode. (It may be "0" or "1.")

3: ▨ represents that bits 3 to 6 are not used for access control of the external area. (Functions of these bits are valid.)

EOL announced

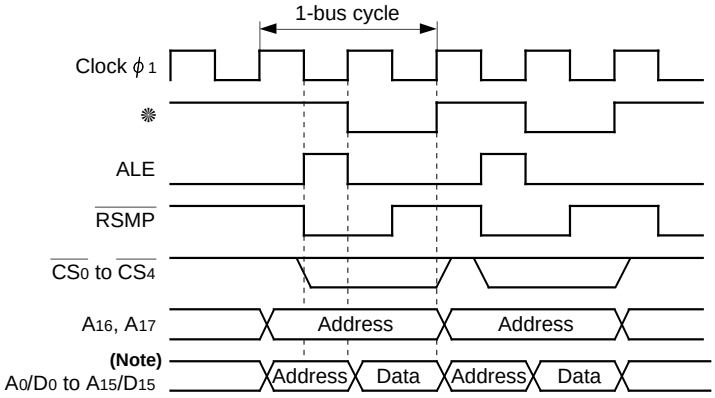


Processor mode register 1 (address 5F 16)

Bit	Bit name	Function	At reset	RW
0	Wait selection bit	0 : Wait 0 1 : Wait 1	0	RW
7 to1	Not implemented.		Un-defined	–

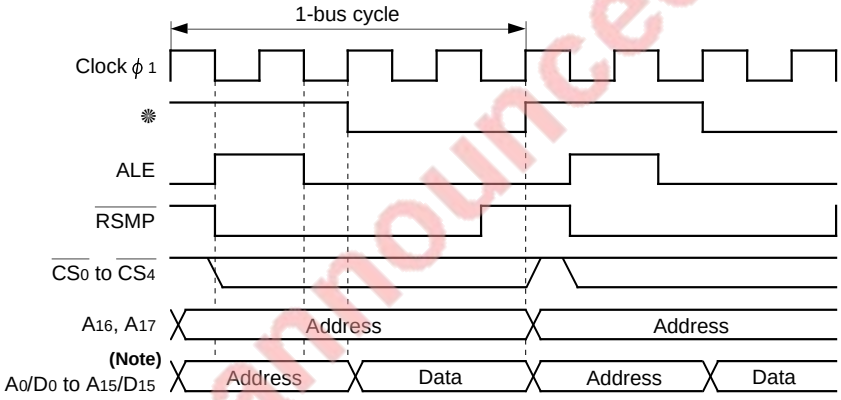
Fig. 12.2.1 Structures of processor mode register 0 and processor mode register 1

<<No wait>>

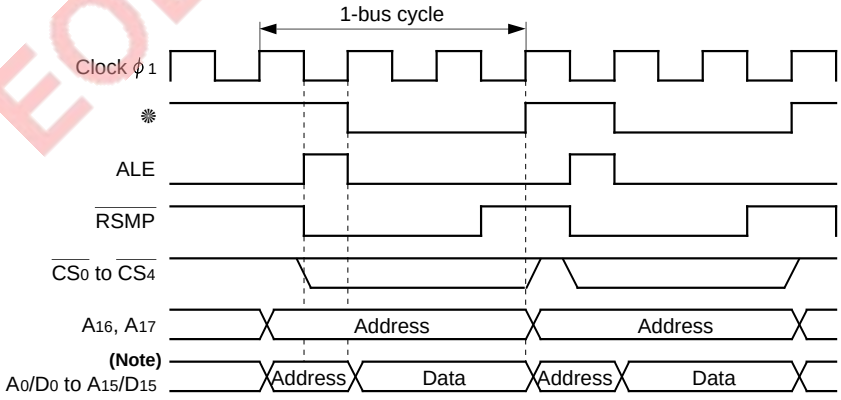


● This waveform is always applied when the internal area is accessed.

<<Wait 0>>



<<Wait 1>>



✵ One of the following is applied.:
- •One of signals RDE, WEL, and WEH
- •Signals WEL and WEH

Note: When the external data bus is 8 bits wide (BYTE = “H”), operating waveform of A 8/D8 to A15/D15 is the same as that of A16 and A17.

Fig. 12.2.2 Bus timing examples when software wait is used (BYTE = “L”).

EOL announced

12.3 Ready function

The ready function facilitates access to external devices which require a long access time.
By applying "L" level to pin $\overline{RDY}$ in the memory expansion or microprocessor mode, the microcomputer enters the ready state. While pin $\overline{RDY}$'s level is "L," this state is retained. Table 12.3.1 lists the microcomputer's state in the ready state.
In the ready state, oscillation of the oscillator does not stop. Therefore, the internal peripheral devices can operate even in the ready state. The ready function is valid for the internal and external areas.

Table 12.3.1 Microcomputer's state in ready state

Item	State
Oscillation	Operating
ϕCPU	Stopped at "L" level
$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$, $\overline{CS0}$ to $\overline{CS4}$, $\overline{HLDA}$, ALE, A0/D0 to A15/D15, A16, A17	Retains the same state in which $\overline{RDY}$ was accepted.
P43 to P47, P5 to P8 **(Note 2)**	
P42/ϕ1	In the memory expansion mode ■ When the clock ϕ1 output selection bit[*1] = "1" Outputs clock ϕ1. ■ When the clock ϕ1 output selection bit = "0" Retains the same state in which $\overline{RDY}$ was accepted. In the microprocessor mode ■ When the signal output disable selection bit[*2] = "1" Retains the same state in which $\overline{RDY}$ was accepted. ■ When the signal output disable selection bit = "0" Outputs clock ϕ1.
Timers A and B, Serial I/O, A-D converter, Watchdog timer	Operating

Clock ϕ1 output selection bit[*1]: Bit 7 at address 5E16
Signal output disable selection bit[*2]: Bit 6 at address 6C16

Notes 1: When "L" level which was input to pin $\overline{RDY}$ is sampled at one of the following timings, this signal is not accepted. (Note that ϕCPU is stopped at "L" level.)
- When the levels of signals $\overline{RDE}$, $\overline{WEL}$, and $\overline{WEH}$ are "H" while the bus is in use (Refer to ② **in Figure 12.3.2**.)
- Immediately before a wait generated by the software wait (Refer to ⑤ **in Figure 12.3.2.**)

2: This is applied when these pins function as programmable I/O ports.

EOL announced

12.3 Ready function

12.3.1 Operation in ready state

When “L” level is input to pin $\overline{RDY}$, this signal is accepted at the falling edge of clock ϕ_1 and the microcomputer enters the ready state. The ready state can be terminated by setting pin $\overline{RDY}$’s level to “H” again. When “H” level is input to pin $\overline{RDY}$, this signal is also accepted at the falling edge of clock ϕ_1 and the ready state is terminated. Figure 12.3.2 shows timings when the ready state is accepted and terminated.

When generating a wait which is equivalent to 1 cycle of clock ϕ_1 by using the ready function, use signals $\overline{RSMP}$ and $\overline{CS_n}$ (n = 0 to 4). These signals facilitate to generate a signal input to pin $\overline{RDY}$. Figure 12.3.1 shows a connection example when signal $\overline{RSMP}$ is used. Note that signal $\overline{RSMP}$ is affected by the software wait. Figure 12.3.3 shows the relationship between the software wait and signal $\overline{RSMP}$.

Refer to section **“17.1 Memory expansion”** for the way to use the ready function.

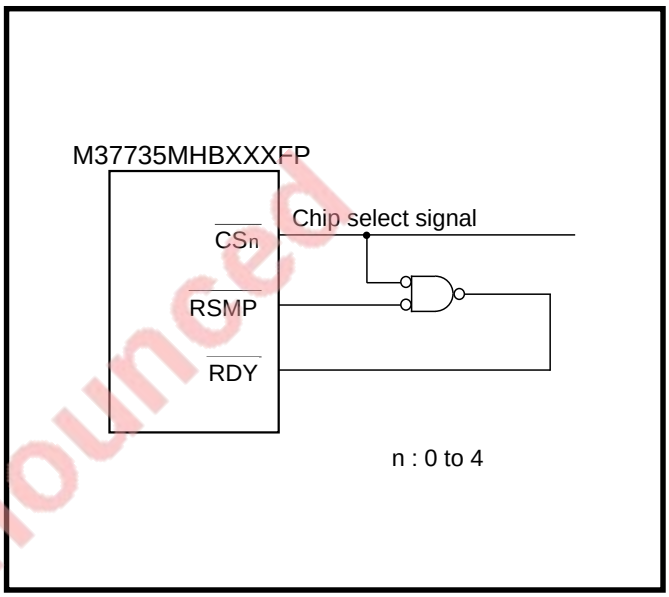
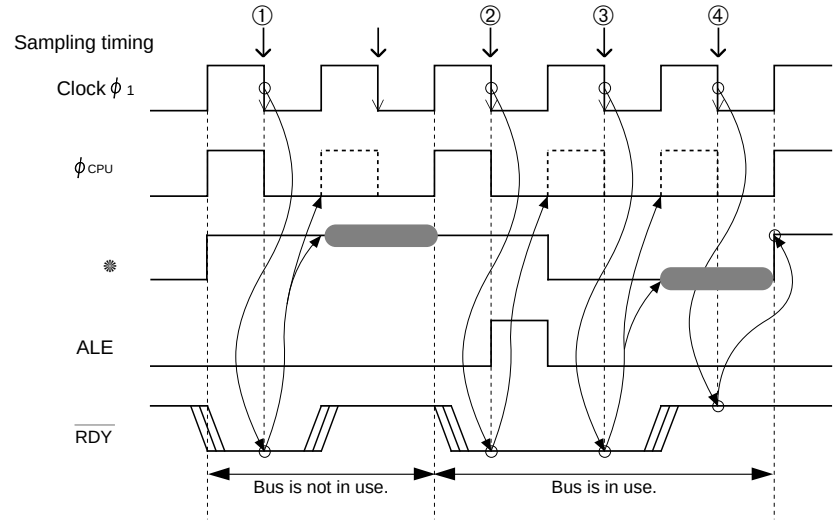


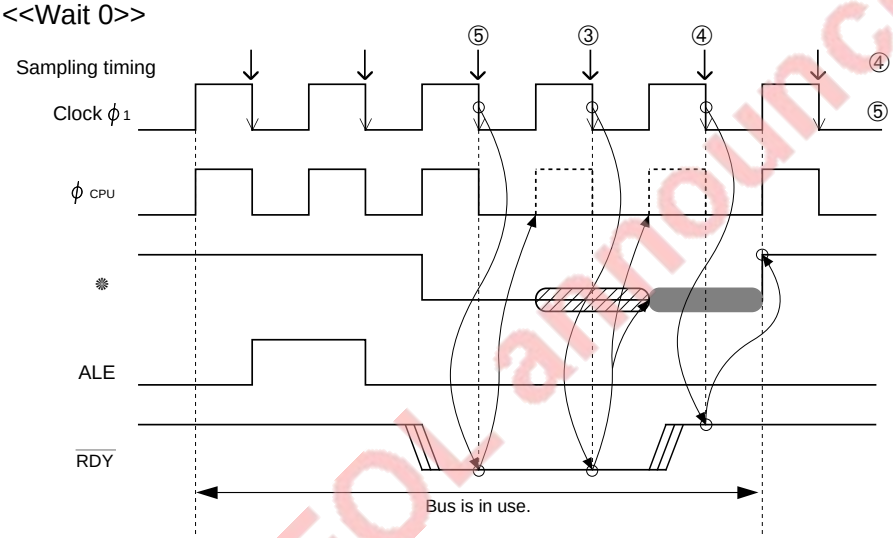
Fig. 12.3.1 Connection example when signal $\overline{RSMP}$ is used

EOL announced

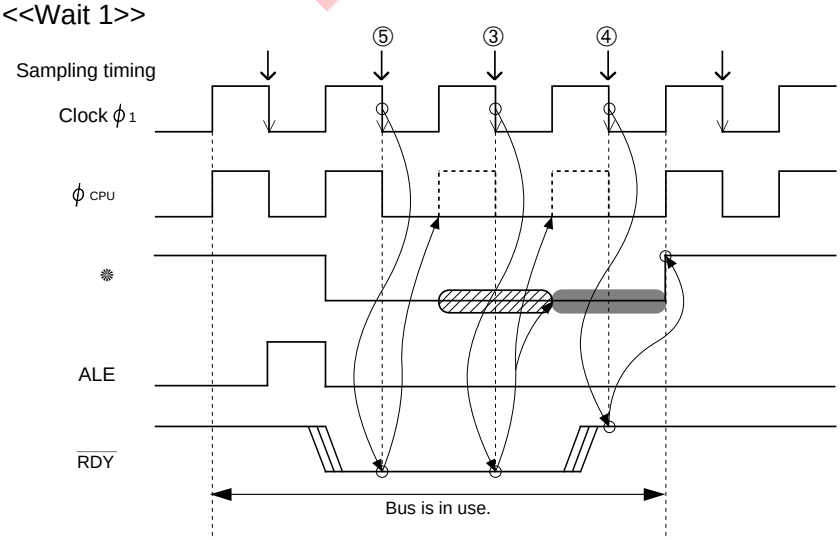
<<No wait>>



<<Wait 0>>



<<Wait 1>>



✵ One of the following is applied.:
- One of signals $\overline{RDE}$, $\overline{WEL}$, and $\overline{WEH}$
- Signals $\overline{WEL}$ and $\overline{WEH}$

: Ready state

: Software wait

① "L" level which is input to pin $\overline{RDY}$ is accepted, so that signal ✵ is stopped at "H" level for 1cycle of clock ϕ_1 (area), and ϕ_{CPU} is stopped at "L" level.

② "L" level which is input to pin $\overline{RDY}$ is not accepted, but ϕ_{CPU} is stopped at "L" level.

③ "L" level which is input to pin $\overline{RDY}$ is accepted, so that signal ✵ is stopped at "L" level for 1cycle of clock ϕ_1 (area), and ϕ_{CPU} is stopped at "L" level.

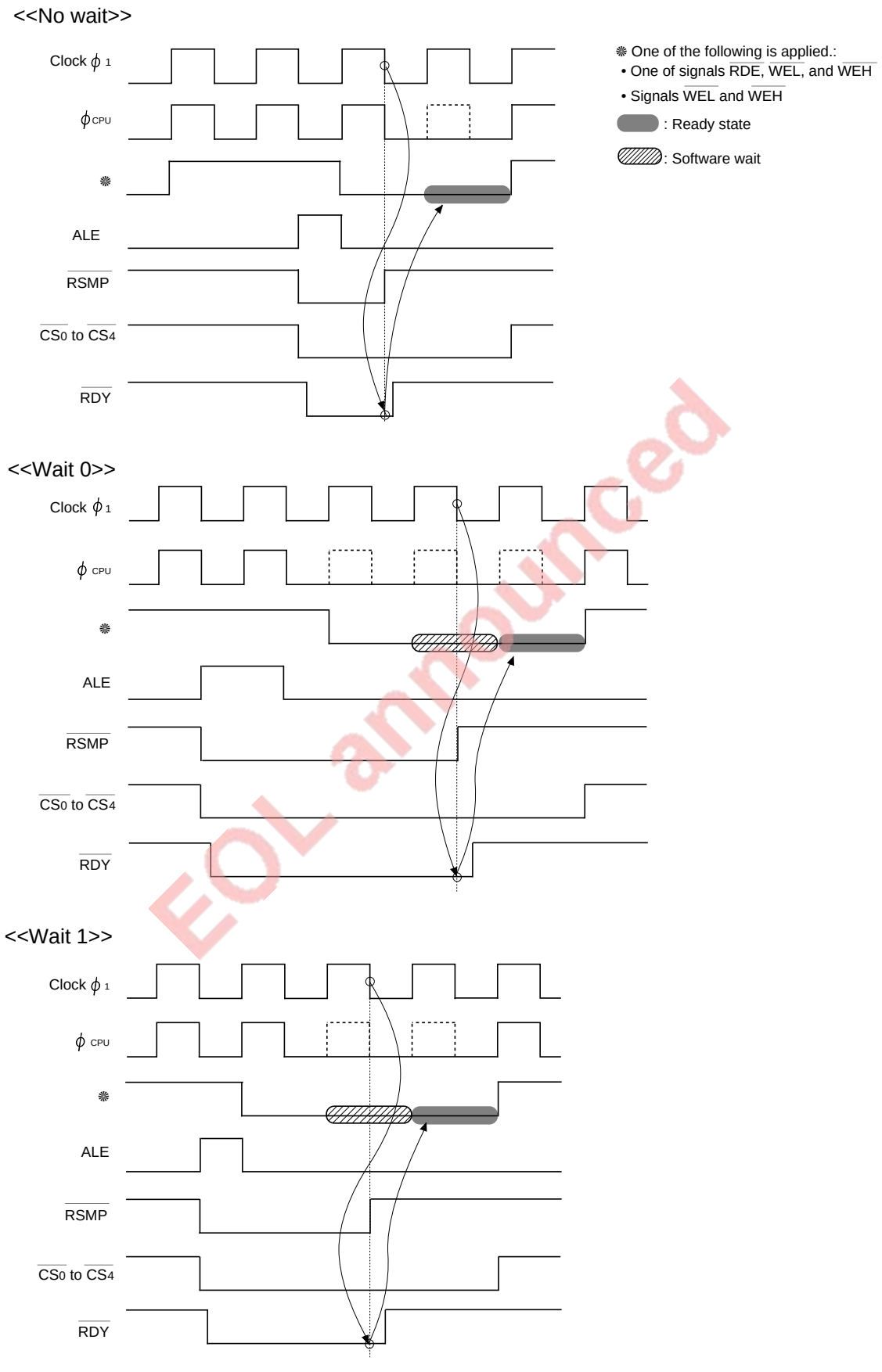
④ Ready state is terminated.

⑤ "L" level which is input to pin $\overline{RDY}$ is not accepted because it is sampled immediately before a wait generated by software wait (area), but ϕ_{CPU} is stopped at "L" level.

EOL announced

Fig. 12.3.2 Timings when ready state is accepted and terminated (when not using signal $\overline{RSMP}$)

12.3 Ready function



EOL announced

Fig. 12.3.3 Relationship between software wait and signal RSMP

12.4 Hold function

When an external circuit which accesses the bus without using the central processing unit (CPU), for example DMA, is used, it is necessary to generate a timing for transferring the right to use of the bus from the CPU to the external circuit. The hold function is used to generate this timing.

By applying "L" level to pin $\overline{HOLD}$ in the memory expansion or microprocessor mode, the microcomputer enters the hold state. While pin $\overline{HOLD}$'s level is "L," this state is retained. Table 12.4.1 lists the microcomputer's state in the hold state.

In the hold state, oscillation of the oscillator does not stop. Therefore, the internal peripheral devices can operate even in the hold state. (Note that the watchdog timer stops.)

Table 12.4.1 Microcomputer's state in hold state

Item	State
Oscillation	Operating
ϕCPU	Stopped at "L"
$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$, $\overline{CS0}$ to $\overline{CS4}$, $\overline{RSMP}$, A0/D0 to A15/D15, A16, A17	Floating
$\overline{HLDA}$, ALE	Outputs "L" level.
P42/ϕ_1	In the memory expansion mode ■ When the clock ϕ1 output selection bit[*1] = "1" Outputs clock ϕ1. ■ When the clock ϕ1 output selection bit = "0" Retains the same state in which $\overline{HOLD}$ was accepted. In the microprocessor mode ■ When the signal output disable selection bit[*2]= "1" Retains the same state in which $\overline{HOLD}$ was accepted. ■ When the signal output disable selection bit = "0" Outputs clock ϕ1.
P43 to P47, P5 to P8 **(Note)**	Retains the same state in which $\overline{HOLD}$ was accepted.
Timers A and B, Serial I/O, A-D converter	Operating
Watchdog timer	Stopped

Clock ϕ_1 output selection bit[*1]: Bit 7 at address 5E16

Signal output disable selection bit[*2]: Bit 6 at address 6C16

Note: This is applied when these pins function as programmable I/O ports.

EOL announced

CONNECTING EXTERNAL DEVICES

12.4 Hold function

12.4.1 Operation in hold state

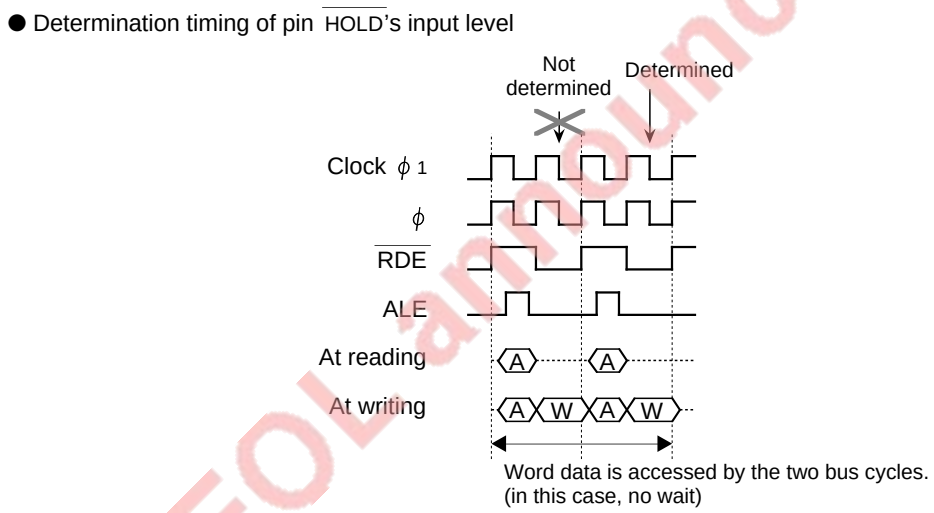
When “L” level is input to pin $\overline{\text{HOLD}}$ while the bus is not in use, this signal is accepted at the falling edge of clock $\phi 1$. When “L” level is input to pin $\overline{\text{HOLD}}$ while the bus is in use, this signal is accepted at the clock $\phi 1$’s falling edge which precedes the rising edge of signal $\overline{\text{RDE}}$, $\overline{\text{WEL}}$, or $\overline{\text{WEH}}$ by the clock $\phi 1$’s cycle divided by 2. (Refer to **Figures 12.4.2 to 12.4.6.**) Note that when word data which starts from an odd address is accessed by the two bus cycles, determination is performed only in the second bus cycle. (Refer to **Figure 12.4.1.**)

When “L” level which was input to pin $\overline{\text{HOLD}}$ is accepted, ϕCPU is stopped at the next rising edge of clock $\phi 1$. At this time, pin $\overline{\text{HLDA}}$ outputs “L” level, and so the external is informed that the microcomputer is in the hold state. After one cycle of clock $\phi 1$ has passed since pin $\overline{\text{HLDA}}$’s level becomes “L,” pins $\overline{\text{RDE}}$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$, $\overline{\text{CS}}_0$ to $\overline{\text{CS}}_4$, $\overline{\text{RSMP}}$ and the external bus enter the floating state.

The hold state can be terminated by setting pin $\overline{\text{HOLD}}$’s level to “H” again. When “H” level is input to pin $\overline{\text{HOLD}}$, this signal is accepted at the falling edge of clock $\phi 1$. When “H” level which was input to pin $\overline{\text{HOLD}}$ is accepted, pin $\overline{\text{HLDA}}$’s level goes from “L” to “H.” And then, the hold state is terminated after one cycle of clock $\phi 1$ has passed.

Figures 12.4.2 to 12.4.6 show the timing when the hold state is accepted and terminated.

❋ In the ready state, determination of pin $\overline{\text{HOLD}}$’s input level is not performed.



EOL announced

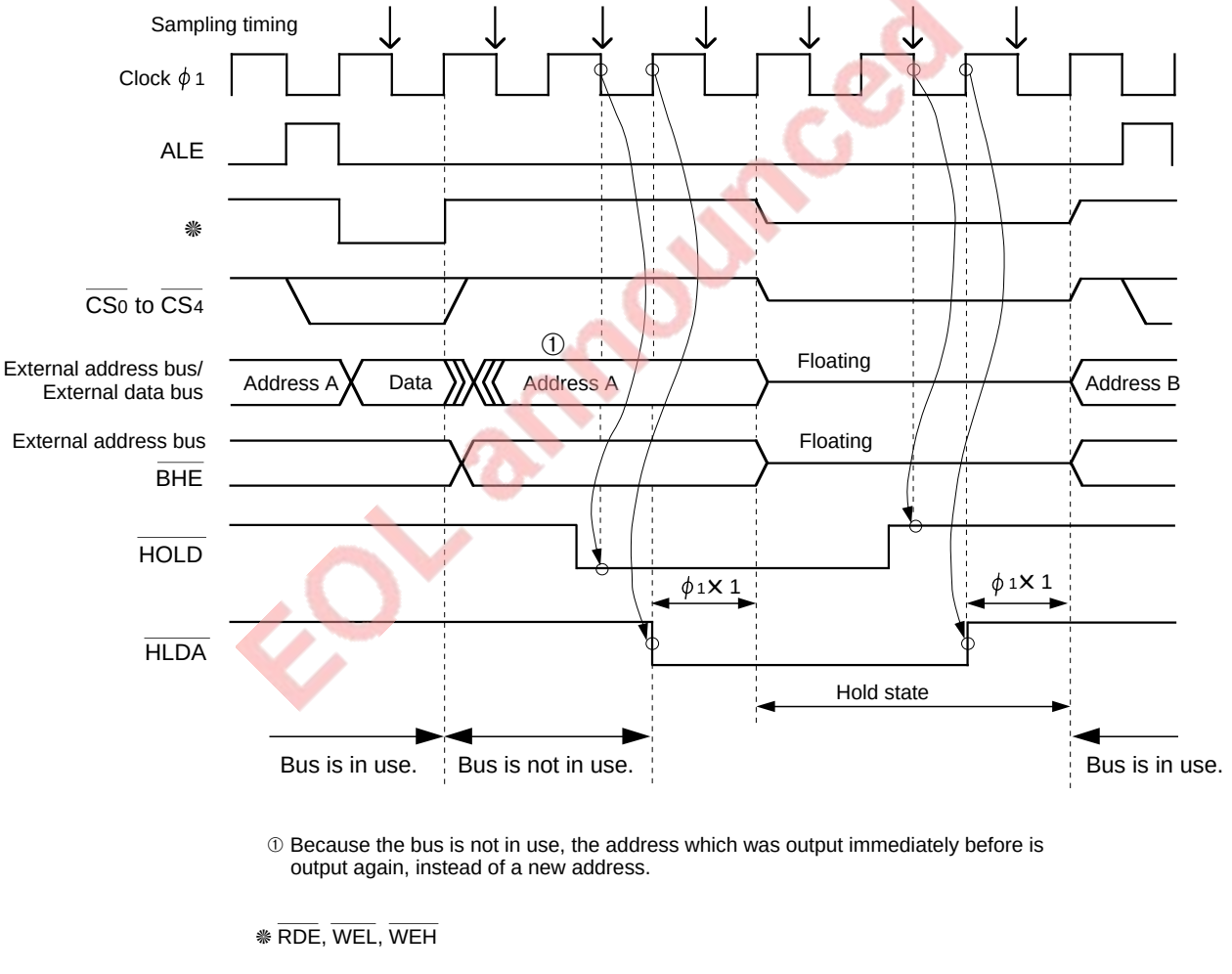
Fig.12.4.1 Determination when word data which starts from odd address is accessed by the two bus cycles

<<When "L" level is input to pin $\overline{\text{HOLD}}$ while bus is not in use>>

● State when "L" level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
Not in use	8	8, 16	No wait,
	16	8, 16	Wait 1, Wait 0

Note: The same operation is performed independent of the software wait (no wait, wait 0, or wait 1). This diagram shows the operation when no wait is selected.



① Because the bus is not in use, the address which was output immediately before is output again, instead of a new address.

✺ $\overline{\text{RDE}}$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$

EOL announced

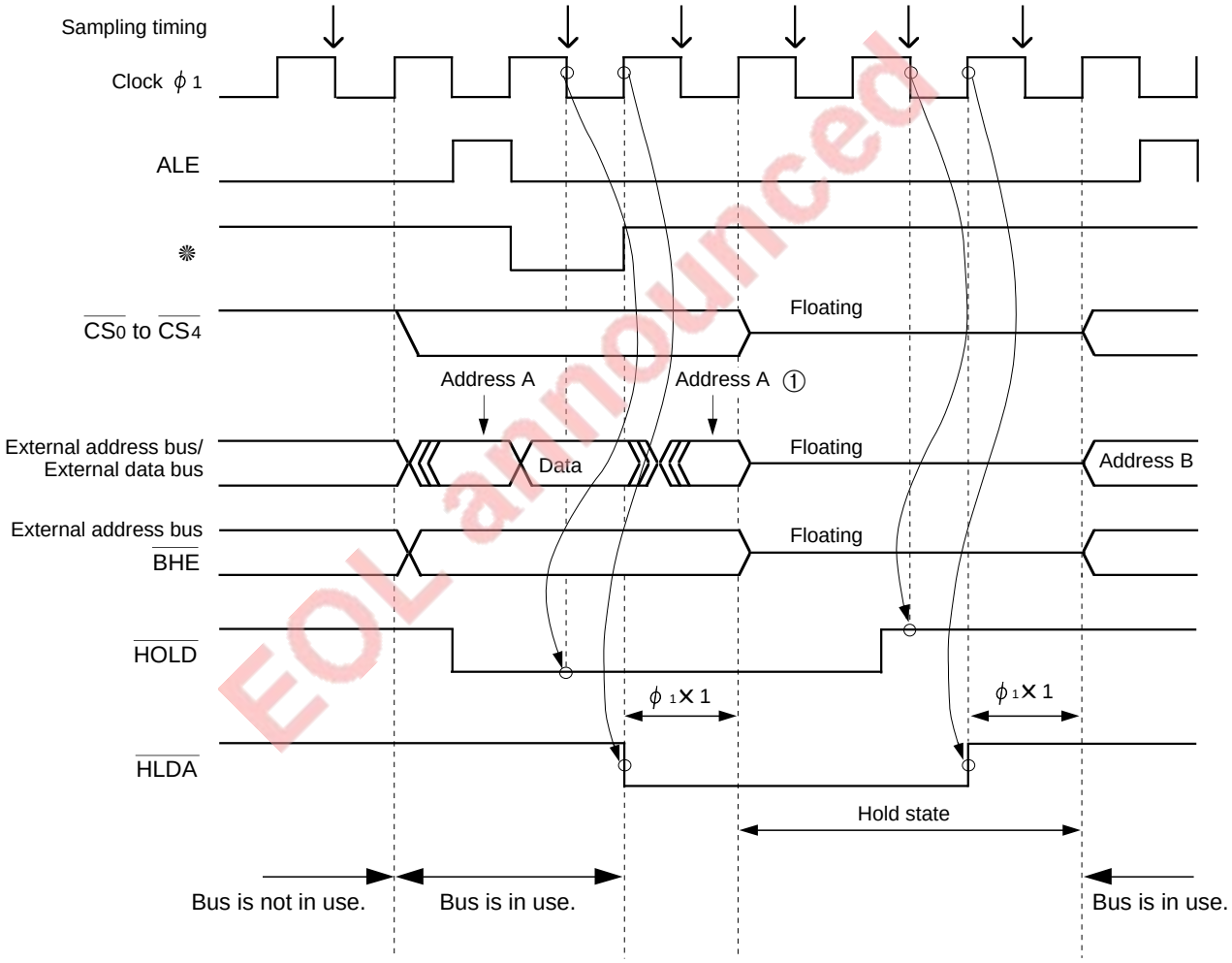
Fig. 12.4.2 Timing when hold state is accepted and terminated (1)

12.4 Hold function

<<When “L” level is input to pin $\overline{\text{HOLD}}$ while bus is in use (1)>>

● State when “L” level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	8	8, 16	No wait
	16	16 (When accessed starting from even address)	



EOL announced

① When “L” level which is input to pin $\overline{\text{HOLD}}$ is accepted, the address which was output immediately before is output again, instead of a new address.

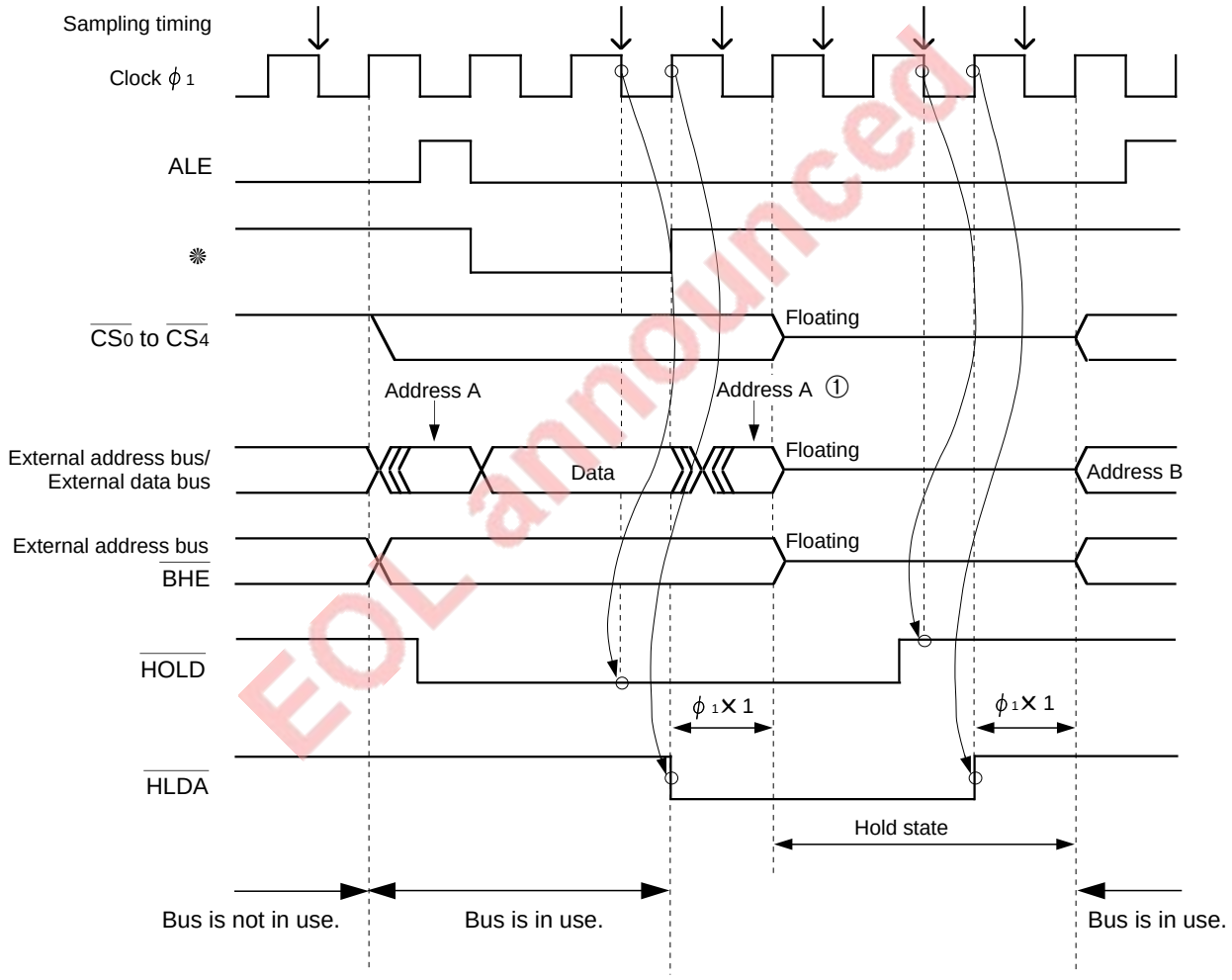
✵ $\overline{\text{RDE}}$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$

Fig. 12.4.3 Timing when hold state is accepted and terminated (2)

<<When "L" level is input to pin $\overline{\text{HOLD}}$ while bus is in use (2)>>

● State when "L" level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	8	8, 16	Wait 1
	16	16 (When accessed starting from even address)	



EOL announced

① When "L" level which is input to pin $\overline{\text{HOLD}}$ is accepted, the address which was output immediately before is output again, instead of a new address.

✺ $\overline{\text{RDE}}$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$

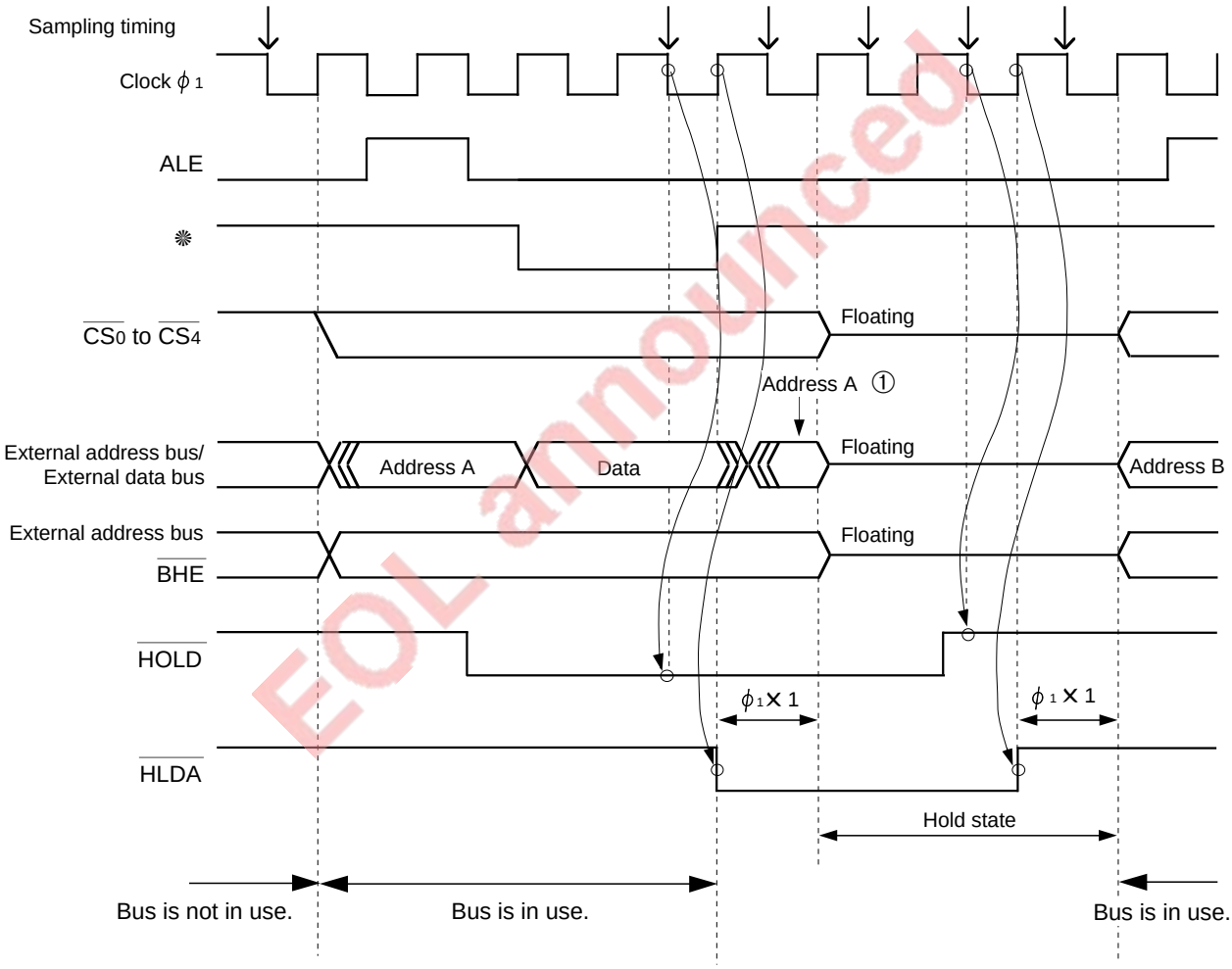
Fig. 12.4.4 Timing when hold state is accepted and terminated (3)

12.4 Hold function

<<When "L" level is input to pin $\overline{\text{HOLD}}$ while bus is in use (3)>>

● State when "L" level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	8	8, 16	Wait 0
	16	16 (When accessed starting from even address)	



EOL announced

① When "L" level which is input to pin $\overline{\text{HOLD}}$ is accepted, the address which was output immediately before is output again, instead of a new address.

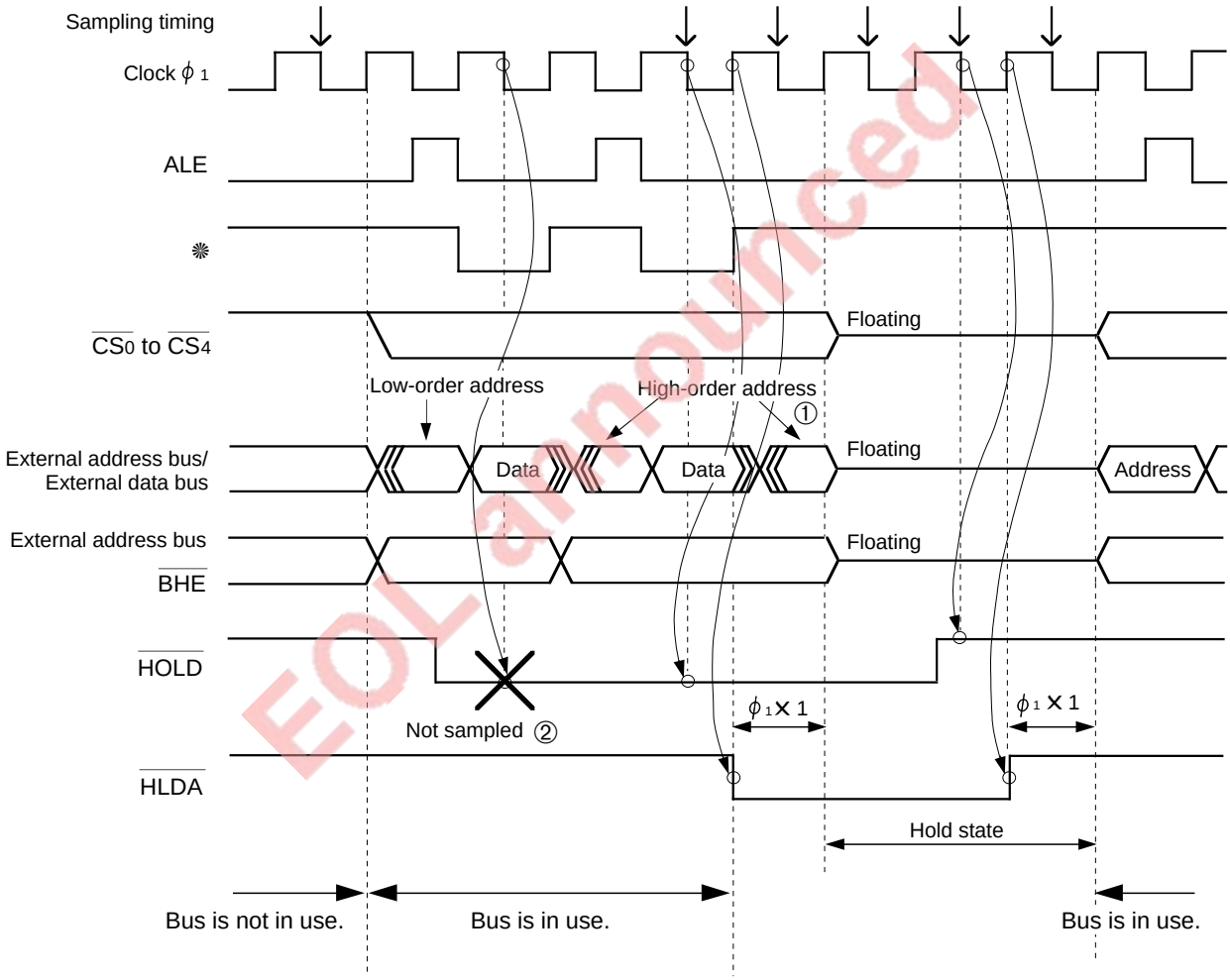
✺ $\overline{\text{RDE}}$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$

Fig. 12.4.5 Timing when hold state is accepted and terminated (4)

<<When “L” level is input to pin $\overline{\text{HOLD}}$ while bus is in use (4)>>

● State when “L” level is input to pin $\overline{\text{HOLD}}$

External data bus	Data length	External data bus width	Software wait
In use	16	8	No wait
		16 (When accessed starting from even address)	



EOL announced

① When “L” level which is input to pin $\overline{\text{HOLD}}$ is the accepted, the address which was output immediately before is output again, instead of a new address.
② Sampling is not performed until 16-bit data input/output is finished. (“L” level which is input to pin $\overline{\text{HOLD}}$ is not accepted.)

✵ $\overline{\text{RDE}}$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$

Fig. 12.4.6 Timing when hold state is accepted and terminated (5)

MEMO

EOL announced

CHAPTER 13
RESET

13.1 Hardware reset
13.2 Software reset

EOL announced

RESET

13.1 Hardware reset

Concerning chapter “RESET,” the 7735 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:
• “**13.1 Hardware reset**”

The following section of the 7735 Group is the same as that of the 7733 Group. Therefore, for this section, refer to part 1:
• **“13.2 Software reset” (page 13-12 in part 1)**

13.1 Hardware reset

Concerning section “13.1 Hardware reset,” the 7735 Group differs from the 7733 Group in the following:
• **“Table 13.1.1 Pin state while pin $\overline{\text{RESET}}$ is at “L” level”**
• **“Figure 13.1.6 State of SFR area and internal RAM area immediately after reset (4)”**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:
• **“13.1 Hardware reset” (page 13-2 in part 1)**

Table 13.1.1 Pin state while pin $\overline{\text{RESET}}$ is at “L” level

	Pin CNVSS’s level	Pin (Port) name	Pin state
Mask ROM version	VSS or VCC	P0 to P8	Floating
		$\overline{\text{E}}$/$\overline{\text{RDE}}$	“H” level is output.
Built-in PROM version	VSS	P0 to P8	Floating
		$\overline{\text{E}}$/$\overline{\text{RDE}}$	“H” level is output.
	VCC	P0, P1, P3 to P8	Floating
		P2	•Floating when “H” level is applied to both or one of pins P5$_1$ and P5$_2$ •“H” or “L” level is output when “L” level is applied to both of pins P5$_1$ and P5$_2$.
		$\overline{\text{E}}$/$\overline{\text{RDE}}$	“H” level is output.
External ROM version	VCC	A$_0$/D$_0$ to A$_7$/D$_7$, A$_8$/D$_8$ to A$_{15}$/D$_{15}$, A$_{16}$, A$_{17}$	“H” or “L” level is output.
		$\overline{\text{CS}_0}$ to $\overline{\text{CS}_4}$, $\overline{\text{WEL}}$, $\overline{\text{WEH}}$, $\overline{\text{HLDA}}$, $\overline{\text{E}}$/$\overline{\text{RDE}}$	“H” level is output.
		ALE	“L” level is output.
		ϕ_1	ϕ_1 (operating) is output.
		$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, P4$_3$ to P4$_7$, P5 to P8	Floating

EOL announced

Figure 13.1.6 for the 7735 Group differs from that for the 7733 Group only in ✻3.

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
6016	Watchdog timer register	WO	? (✻1)
6116	Watchdog timer frequency selection flag	RW	? 0
6216	(Reserved area) ✻4		?
6316	Memory allocation control register	RW	? 0 0 0 0 0
6416	UART2 transmit/receive mode register	RW	? 0 0 0 0 0 0 0
6516	UART2 baud rate register (BRG2)	WO	?
6616	UART2 transmission buffer register	WO	?
6716		WO	?
6816	UART2 transmit/receive control register 0	RO RW	? 1 0 0 0
6916	UART2 transmit/receive control register 1	RO RW RO RW	0 0 0 0 0 0 1 0
6A16	UART2 receive buffer register	RO	?
6B16		RO	0 0 0 0 0 0 0 ?
6C16	Oscillation circuit control register 0	RW(✻2) RW	? 0 0 0 0 0 ? 1
6D16	Port function control register	RW	0 0 0 0 0 0 0 0
6E16	Serial transmit control register	RW	? 0 0 ?
6F16	Oscillation circuit control register 1	WO RW	0 ? 0 ✻3 0 0 0
7016	A-D / UART2 trans./rece. interrupt control register	RW	? 0 0 0 0
7116	UART0 transmission interrupt control register	RW	? 0 0 0 0
7216	UART0 receive interrupt control register	RW	? 0 0 0 0
7316	UART1 transmission interrupt control register	RW	? 0 0 0 0
7416	UART1 receive interrupt control register	RW	? 0 0 0 0
7516	Timer A0 interrupt control register	RW	? 0 0 0 0
7616	Timer A1 interrupt control register	RW	? 0 0 0 0
7716	Timer A2 interrupt control register	RW	? 0 0 0 0
7816	Timer A3 interrupt control register	RW	? 0 0 0 0
7916	Timer A4 interrupt control register	RW	? 0 0 0 0
7A16	Timer B0 interrupt control register	RW	? 0 0 0 0
7B16	Timer B1 interrupt control register	RW	? 0 0 0 0
7C16	Timer B2 interrupt control register	RW	? 0 0 0 0
7D16	$\overline{INT_0}$ interrupt control register	RW	? 0 0 0 0 0 0
7E16	$\overline{INT_1}$ interrupt control register	RW	? 0 0 0 0 0 0
7F16	$\overline{INT_2}$/Key input interrupt control register	RW	? 0 0 0 0 0 0

✻1 Value "FFF16" is set to the watchdog timer. (Refer to section Chapter **"10. WATCHDOG TIMER."**)
✻2 For access characteristics at address 6C16, also refer to **Figure 14.3.2 in part 1.**
✻3 State immediately after reset for bit 3 at address 6F16 vary according to the microcomputer.
(Refer to **Figure 14.3.3 in part 2** ; This bit's function of the 7735 Group differs from that of the 7733 Group.)
This bit must be fixed to "0" in the 7735 Group.
✻4 Do not write data to address 6216.

■Internal RAM area (M37735MHBXXXFP: addresses 8016 to FFF16)

- At hardware reset
(not including the case where the stop or wait mode is terminated)...Undefined.
- At software reset...Retains the state immediately before reset.
- When the stop or wait mode is terminated
(when hardware reset is applied)...Retains the state immediately before the **STP** or **WIT** instruction is executed.

FCL announced

Fig. 13.1.6 State of SFR area and internal RAM area immediately after reset (4)

RESET

13.1 Hardware reset

MEMO

EOL announced

CHAPTER 14

CLOCK GENERATING CIRCUIT

14.1 Overview
14.2 Oscillation circuit example
14.3 Clock control

EOL announced

CLOCK GENERATING CIRCUIT

14.3 Clock control

Concerning chapter “14. CLOCK GENERATING CIRCUIT,” the 7735 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

- **“14.3 Clock control”**

The following sections are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“14.1 Overview” (page 14-2 in part 1)**
- **“14.2 Oscillation circuit example” (page 14-3 in part 1)**

14.3 Clock control

Concerning section “14.3 Clock control,” the 7735 Group differs from the 7733 Group in the following:

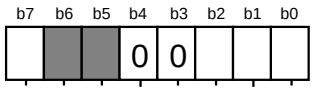
- **Figures 14.3.3 and 14.3.4**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“14.3 Clock control” (page 14-5 in part 1)**

EOL announced

In the M37735MHBXXXFP, set bit 3 of the oscillation circuit control register 1 to “0.”



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin $P7_6$ functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin $P7_6$ functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 4)**	Must be fixed to “0” in the mask ROM and external ROM versions **(Note 1)**.		0	RW
	Must be fixed to “0” in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to “0” **(Note 3)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing “1” to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 14.3.4.
2: Because this bit is “1” at reset, clear this bit to “0” with the initial setting program after reset.
3: The case where data “01010101_2” is written with the procedure shown in Figure 14.3.4 is not included.
4: For the 7733 Group, refer to Figure 14.3.3 in part 1.
5: ▭ represents that bits 3 to 7 are not used for the clock generating circuit.

EOL announced

Fig. 14.3.3 Structure of oscillation circuit control register 1

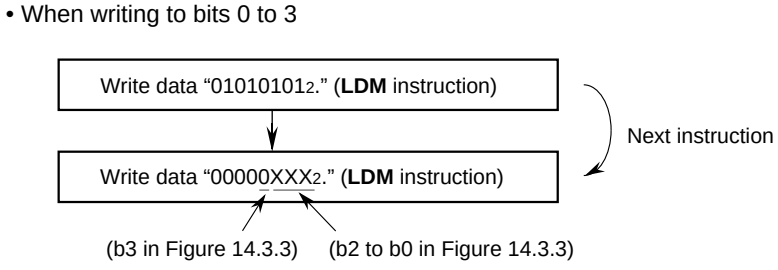


Fig. 14.3.4 Procedure for writing data to oscillation circuit control register 1

MEMO

EOL announced

CHAPTER 15
ELECTRICAL CHARACTERISTICS

EOL announced

15.1 Absolute maximum ratings
15.2 Recommended operating conditions
15.3 Electrical characteristics
15.4 A-D converter characteristics
15.5 Internal peripheral devices
15.6 Ready and Hold
15.7 Single-chip mode
15.8 Memory expansion mode and Microprocessor mode : with no wait
15.9 Memory expansion mode and Microprocessor mode : with wait 1
15.10 Memory expansion mode and Microprocessor mode : with wait 0
15.11 Measuring circuit for ports P0 to P8 and pins ϕ_1 and $\overline{E}$

ELECTRICAL CHARACTERISTICS

Electrical characteristics of the M37735MHBXXXFP are described in this chapter.
For the low voltage version, refer to section **"18.4 Electrical characteristics."**

Concerning chapter "15. ELECTRICAL CHARACTERISTICS," the 7735 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **"15.6 Ready and Hold"**
- **"15.8 Memory expansion mode and Microprocessor mode : with no wait"**
- **"15.9 Memory expansion mode and Microprocessor mode : with wait 1"**
- **"15.10 Memory expansion mode and Microprocessor mode : with wait 0"**

The following sections are the same as those of the 7733 Group. Therefore, refer to part 1:

- **"15.1 Absolute maximum ratings" (page 15-2 in part 1)**
- **"15.2 Recommended operating conditions" (page 15-3 in part 1)**
- **"15.3 Electrical characteristics" (page 15-4 in part 1)**
- **"15.4 A-D converter characteristics" (page 15-5 in part 1)**
- **"15.5 Internal peripheral devices" (page 15-6 in part 1)**
- **"15.7 Single-chip mode" (page 15-13 in part 1)**
- **"15.11 Measuring circuit for ports P0 to P8 and pins ϕ_1 and $\overline{E}$" (page 15-21 in part 1)**

EOL announced

15.6 Ready and Hold

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(RDY-\phi_1)}$	$\overline{RDY}$ input setup time	55		ns
$t_{su(HOLD-\phi_1)}$	$\overline{HOLD}$ input setup time	55		ns
$t_{h(\phi_1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi_1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Note: This is applied when the main clock division selection bit = “0” and f(f_2) = 12.5 MHz.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time	Fig. 15.11.1 in part 1		50	ns

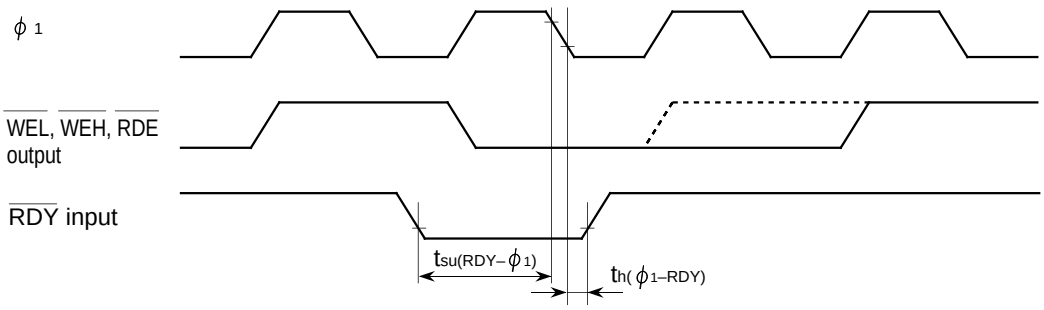
EOL announced

ELECTRICAL CHARACTERISTICS

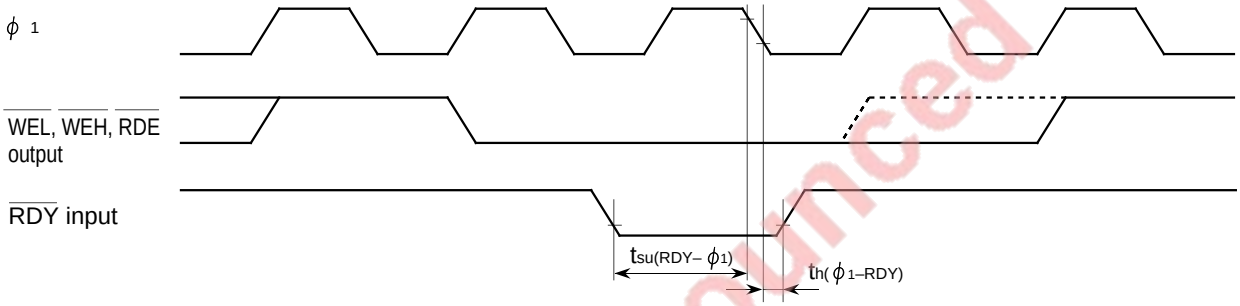
15.6 Ready and Hold

● Ready

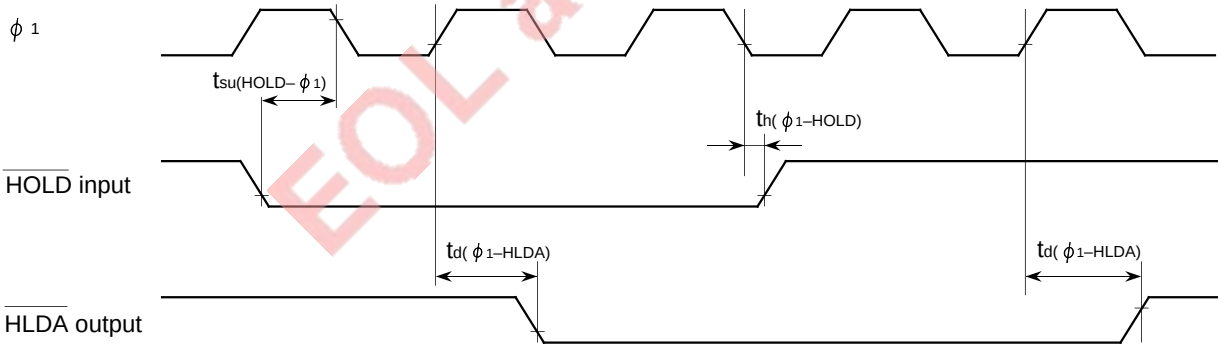
With no wait



With wait



● Hold



EOL announced

Measuring conditions

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.8 Memory expansion mode and Microprocessor mode : with no wait

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

✵ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(D–RDE)}$	Data input setup time	32		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: When the main clock division selection bit = "1," the minimum value of tc = 80 ns.
3: When the main clock division selection bit = "1," values of $tw_{(H)}$/tc and $tw_{(L)}$/tc must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	Fig. 15.11.1 in part 1	$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 28$	12		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 28$	12		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 28$	12		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 22$	18		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 18$	22		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 35$	5		ns
$t_{h(ALE–A)}$	Address hold time			9		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time			4		ns
$t_{d(WE–DQ)}$	Data output delay time				45	ns
$t_{h(WE–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 22$	18		ns
$t_{w(WE)}$	$\overline{WEL}$, $\overline{WEH}$ pulse width		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 30$	50		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				5	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 20$	20		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 32$	48		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 30$	10		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time			0	18	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

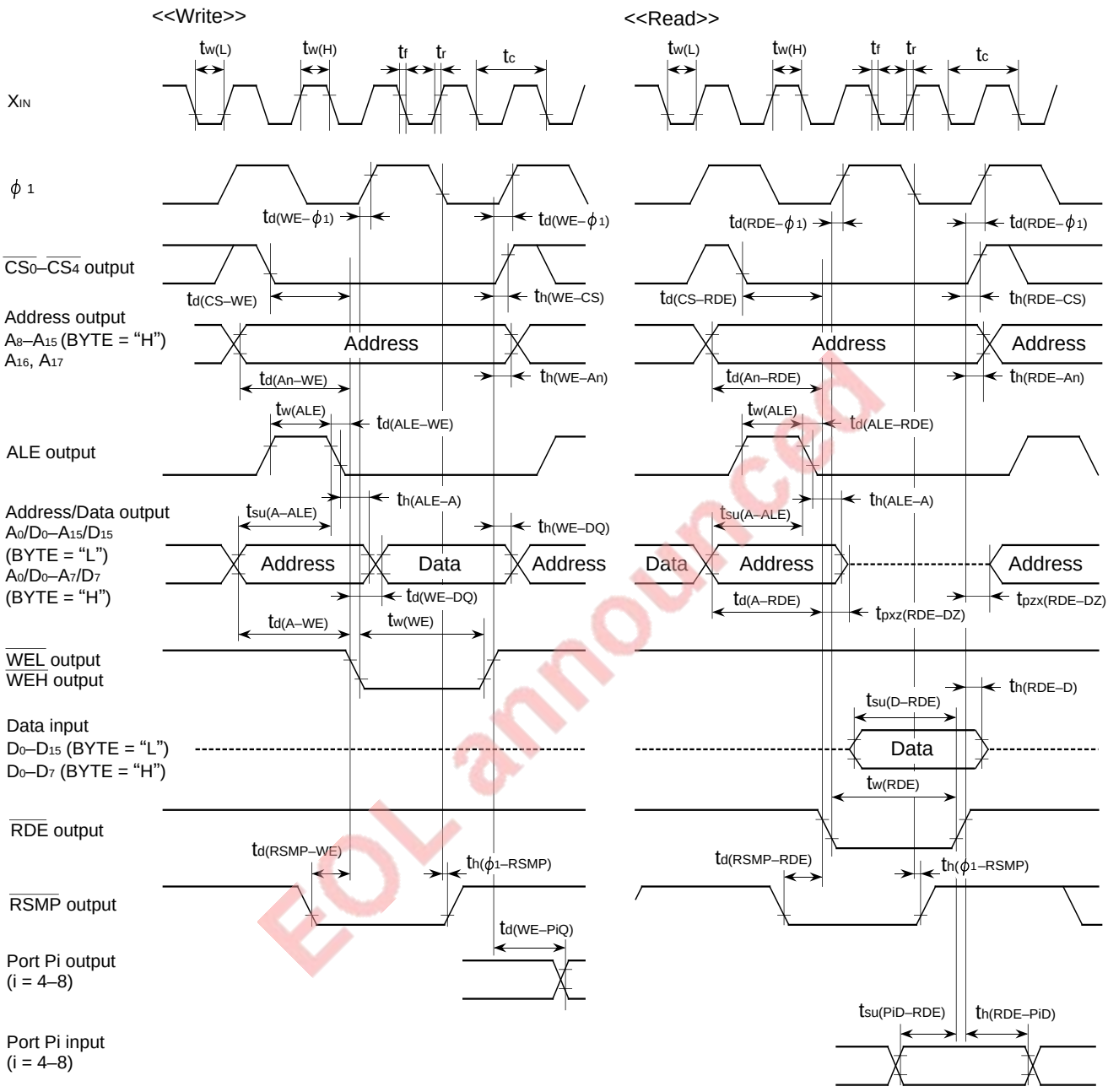
EOL announced

ELECTRICAL CHARACTERISTICS

15.8 Memory expansion mode and Microprocessor mode : with no wait

Memory expansion mode and Microprocessor mode :

With no wait (Wait bit = “1”)



Measuring conditions ($\overline{CS_0}$–$\overline{CS_4}$, A_0/D_0–A_{15}/D_{15}, A_{16}, A_{17}, ALE, $\overline{WEL}$, $\overline{WEH}$, $\overline{RDE}$, $\overline{RSMP}$)

- V_{CC} = 5 V ± 10 %
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Measuring conditions (Ports P4–P8)

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

EOL announced

15.9 Memory expansion mode and Microprocessor mode : with wait 1

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(D–RDE)}$	Data input setup time	32		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: When the main clock division selection bit = "1," the minimum value of tc = 80 ns.
3: When the main clock division selection bit = "1," values of $t_{w(H)}$/tc and $t_{w(L)}$/tc must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	Fig. 15.11.1 in part 1	$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 28$	12		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 28$	12		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 28$	12		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 22$	18		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 18$	22		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 35$	5		ns
$t_{h(ALE–A)}$	Address hold time			9		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time			4		ns
$t_{d(WE–DQ)}$	Data output delay time				45	ns
$t_{h(WE–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 22$	18		ns
$t_{w(WE)}$	$\overline{WEL}$, $\overline{WEH}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 30$	130		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				5	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 20$	20		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 32$	128		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 30$	10		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time			0	18	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

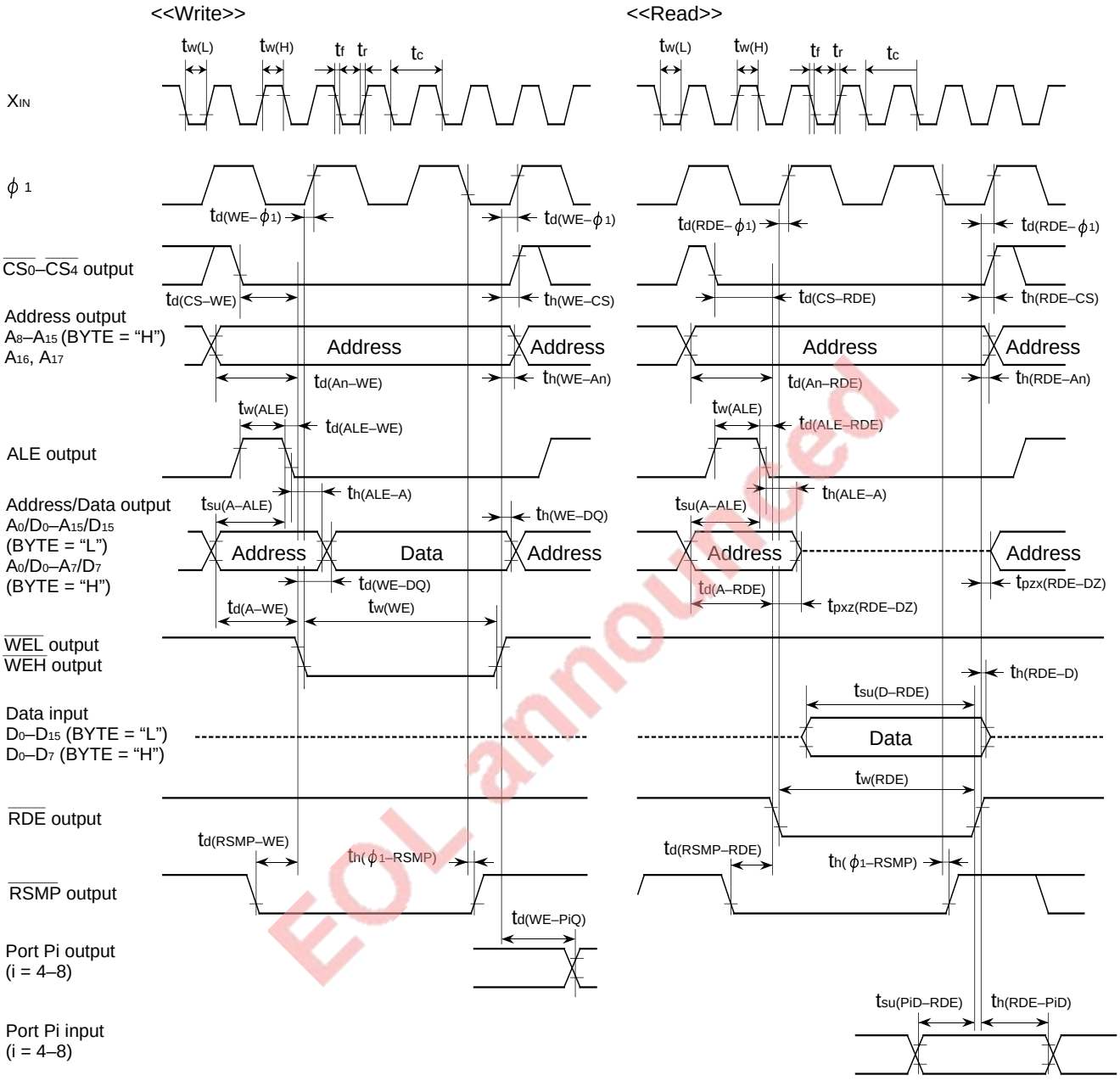
EOL announced

ELECTRICAL CHARACTERISTICS

15.9 Memory expansion mode and Microprocessor mode : with wait 1

Memory expansion mode and Microprocessor mode :

When external memory area is accessed With wait 1 (Wait bit = “0” and Wait selection bit = “1”)



EOL announced

Measuring conditions ($\overline{CS_0}$–$\overline{CS_4}$, A_0/D_0–A_{15}/D_{15}, A_{16}, A_{17}, ALE, $\overline{WEL}$, $\overline{WEH}$, $\overline{RDE}$, $\overline{RSMP}$)

- V_{CC} = 5 V ± 10 %
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Measuring conditions (Port P4–P8)

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

15.10 Memory expansion mode and Microprocessor mode : with wait 0

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(D–RDE)}$	Data input setup time	32		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: When the main clock division selection bit = "1," the minimum value of tc = 80 ns.
3: When the main clock division selection bit = "1," values of $tw_{(H)}$/tc and $tw_{(L)}$/tc must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	Fig. 15.11.1 in part 1	$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 33$	87		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time		$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 33$	87		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time		$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 45$	75		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 22$	18		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 23$	57		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 35$	45		ns
$t_{h(ALE–A)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 25$	15		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 30$	10		ns
$t_{d(WE–DQ)}$	Data output delay time				45	ns
$t_{h(WE–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 22$	18		ns
$t_{w(WE)}$	$\overline{WEL}$, $\overline{WEH}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 30$	130		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				5	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 20$	20		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 32$	128		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 30$	10		ns
$t_{d(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time			0	18	ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.
2: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1**.

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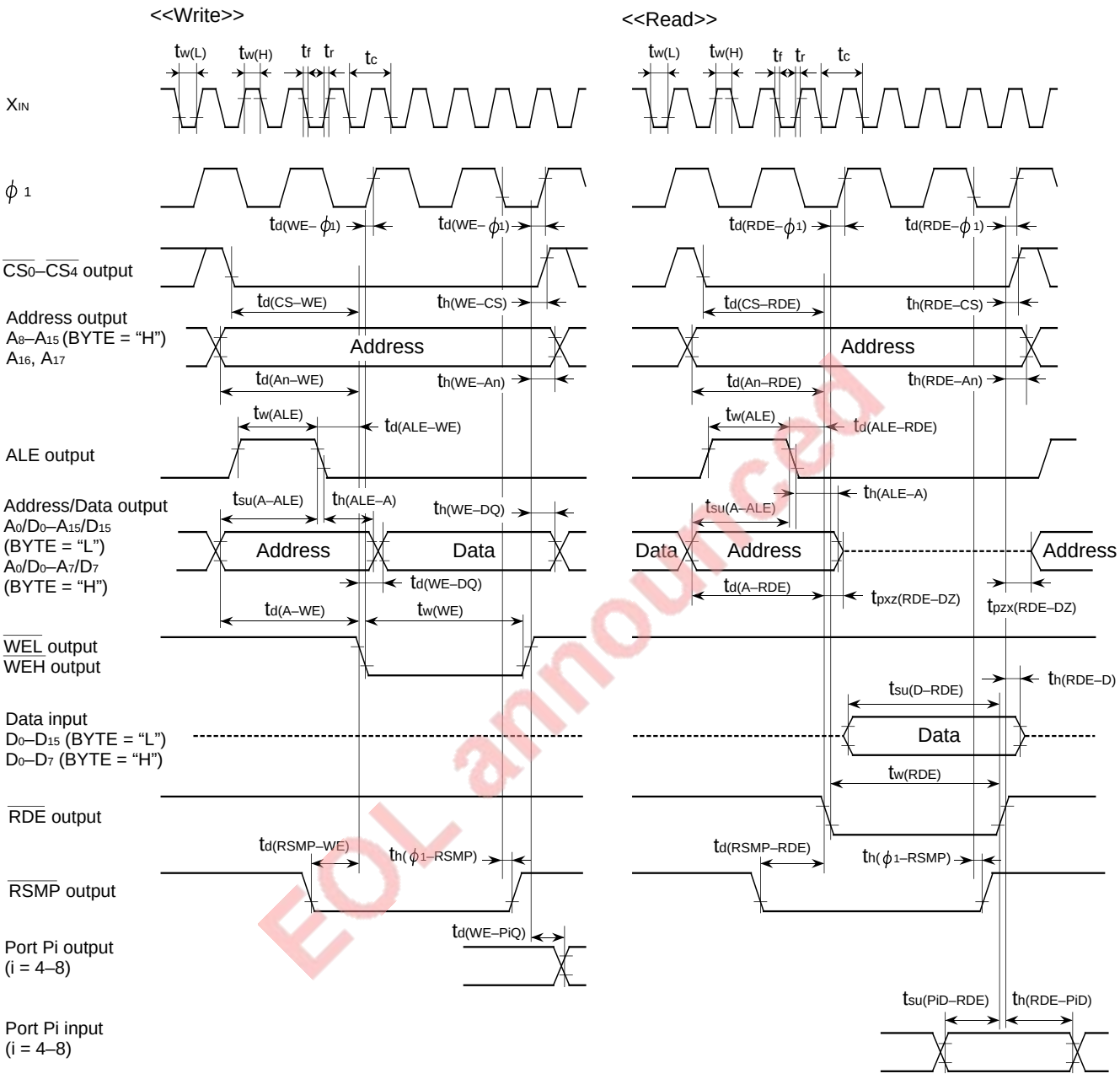
ELECTRICAL CHARACTERISTICS

15.10 Memory expansion mode and Microprocessor mode : with wait 0

Memory expansion mode and Microprocessor mode :

When external memory area is accessed with wait 0 (Wait bit = “0” and Wait selection bit = “0”)



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Measuring conditions ($\overline{CS_0}$–$\overline{CS_4}$, A_0/D_0–A_{15}/D_{15}, A_{16}, A_{17}, ALE, $\overline{WEL}$, $\overline{WEH}$, $\overline{RDE}$, $\overline{RSMP}$)

- V_{CC} = 5 V ± 10 %
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.8 V, V_{IH} = 2.5 V

Measuring conditions (Ports P4–P8)

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

CHAPTER 16

STANDARD CHARACTERISTICS

16.1 Standard characteristics

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STANDARD CHARACTERISTICS

Concerning chapter “16. STANDARD CHARACTERISTICS,” the 7735 Group is the same as the 7733 Group. Therefore, for this chapter, refer to part 1:

- **“16 STANDARD CHARACTERISTICS” (part 1)**

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CHAPTER 17
APPLICATIONS

17.1 Memory expansion
17.2 Serial I/O
17.3 Watchdog timer
17.4 Power saving
17.5 Timer B

EOL announced

APPLICATIONS

17.1 Memory expansion

Concerning chapter “17. APPLICATIONS,” the 7735 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“17.1 Memory expansion”**
- **“17.4 Power saving”**

The following sections of the 7735 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“17.2 Serial I/O” (page 17-28 in part 1)**
- **“17.3 Watchdog timer” (page 17-41 in part 1)**
- **“17.5 Timer B” (page 17-54 in part 1)**

17.1 Memory expansion

Memory • I/O expansion examples of the M37735MHBXXXFP are described below.

- For functions and operations of pins used in memory • I/O expansion, refer to chapter **“12. CONNECTING EXTERNAL DEVICES.”**
- For timing characteristics, refer to chapter **“15. ELECTRICAL CHARACTERISTICS.”**

17.1.1 Memory expansion model

Memory expansion to the external is available in the memory expansion or microprocessor mode. In the M37735MHBXXXFP, the desired memory expansion model can be selected from two models listed in Table 17.1.1. This selection depends on the level of the external data bus width selection signal (BYTE).

(1) 8-bit external data bus model

The external data bus is 8 bits wide and the accessible area can be expanded up to 1 Mbytes. The low-order 8 bits of the external address bus (A_7 to A_0) are multiplexed with the external data bus. Therefore, one 8-bit address latch is necessary in order to latch A_7 to A_0.

(2) 16-bit external data bus model

The external data bus is 16 bits wide and the accessible area can be expanded up to 1 Mbytes. The low-order 16 bits of the external address bus (A_{15} to A_0) are multiplexed with the external data bus. Therefore, two 8-bit address latches are necessary in order to latch A_7 to A_0 and A_{15} to A_8.

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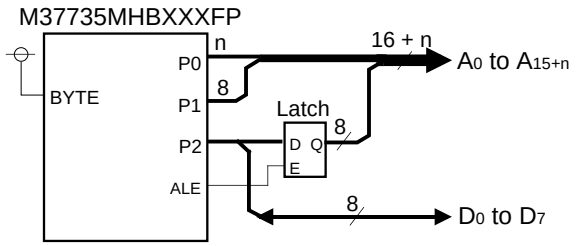
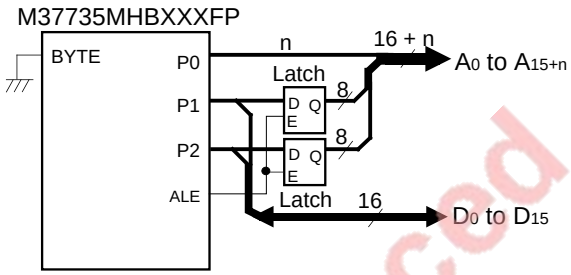
Table 17.1.1 Memory expansion models

External data bus	8 bits wide BYTE = "H"	 (n ≤ 2)
	16 bits wide BYTE = "L"	 (n ≤ 2)

- For functions and operations of pins used in memory expansion, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."** For timing characteristics, refer to chapter **"15. ELECTRICAL CHARACTERISTICS."**
- In memory expansion, the address bus can be expanded up to 18 bits wide. Accordingly, be sure to strengthen the 7735 Group's Vss line on the system. (Refer to section **"Appendix 8. Countermeasure examples against noise."**)

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APPLICATIONS

17.1 Memory expansion

17.1.2 Calculation ways for timing

When expanding memory, use a memory of which specifications satisfy the following timing requirements: address access time ($t_{a(AD)}$) and data setup time for writing data ($t_{su(D)}$). Calculation ways for $t_{a(AD)}$ and $t_{su(D)}$ are described below.

① **Address access time of external memory [$t_{a(AD)}$]**

$t_{a(AD)} = t_{d(A\text{-}RDE)} + t_{w(RDE)} - t_{su(D\text{-}RDE)}$
$- (\text{address decode time}^{*1} + \text{address latch delay time}^{*2})$

address decode time*1: time necessary for validating a chip select signal after an address is decoded
address latch delay time*2: delay time necessary for latching an address

② **Data setup time of external memory for writing data [$t_{su(D)}$]**

$t_{su(D)} = t_{w(WE)} - t_{d(WE\text{-}DQ)}$

Table 17.1.2 lists the calculation formulas and constants for each parameter in the above formulas. Figure 17.1.1 shows bus timing diagrams.

Table 17.1.2 Calculation formulas and constants for each parameter (Unit: ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{d(A\text{-}RDE)}$	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$
$t_{w(RDE)}$	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 32$	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$	
$t_{w(WE)}$	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$	
$t_{su(D\text{-}RDE)}$	32		
$t_{d(WE\text{-}DQ)}$	45		

Wait bit: Bit 2 at address $5E_{16}$
Wait selection bit: Bit 0 at address $5F_{16}$
Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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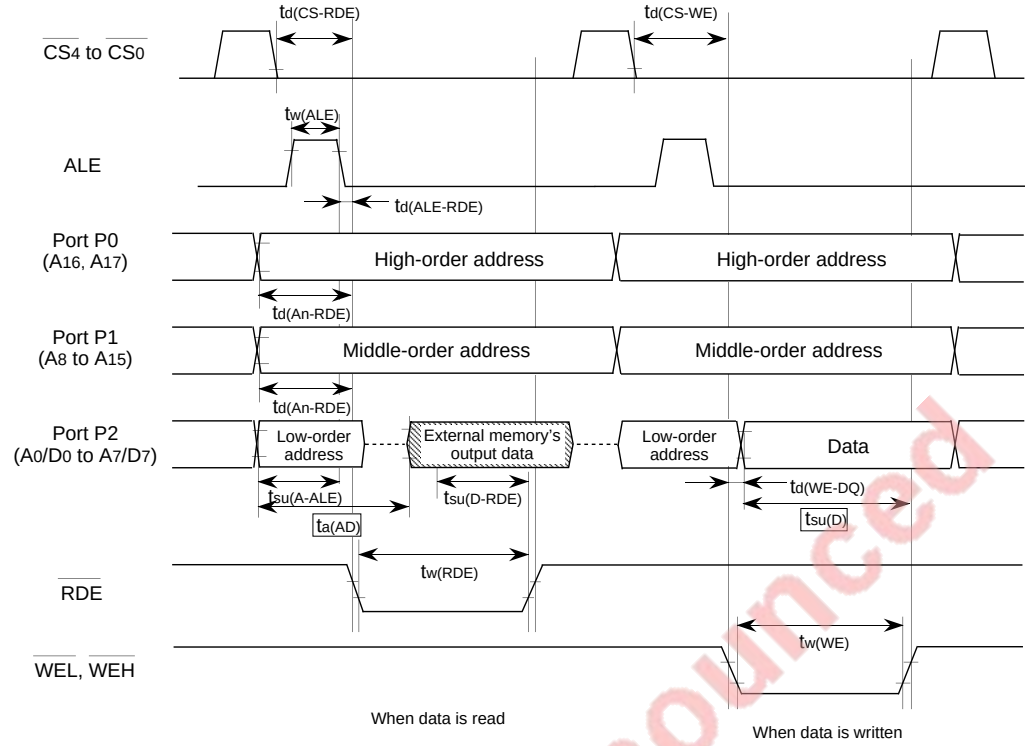
When BYTE = “H” (External data bus = 8 bits wide)



When BYTE = “L” (External data bus = 16 bits wide)

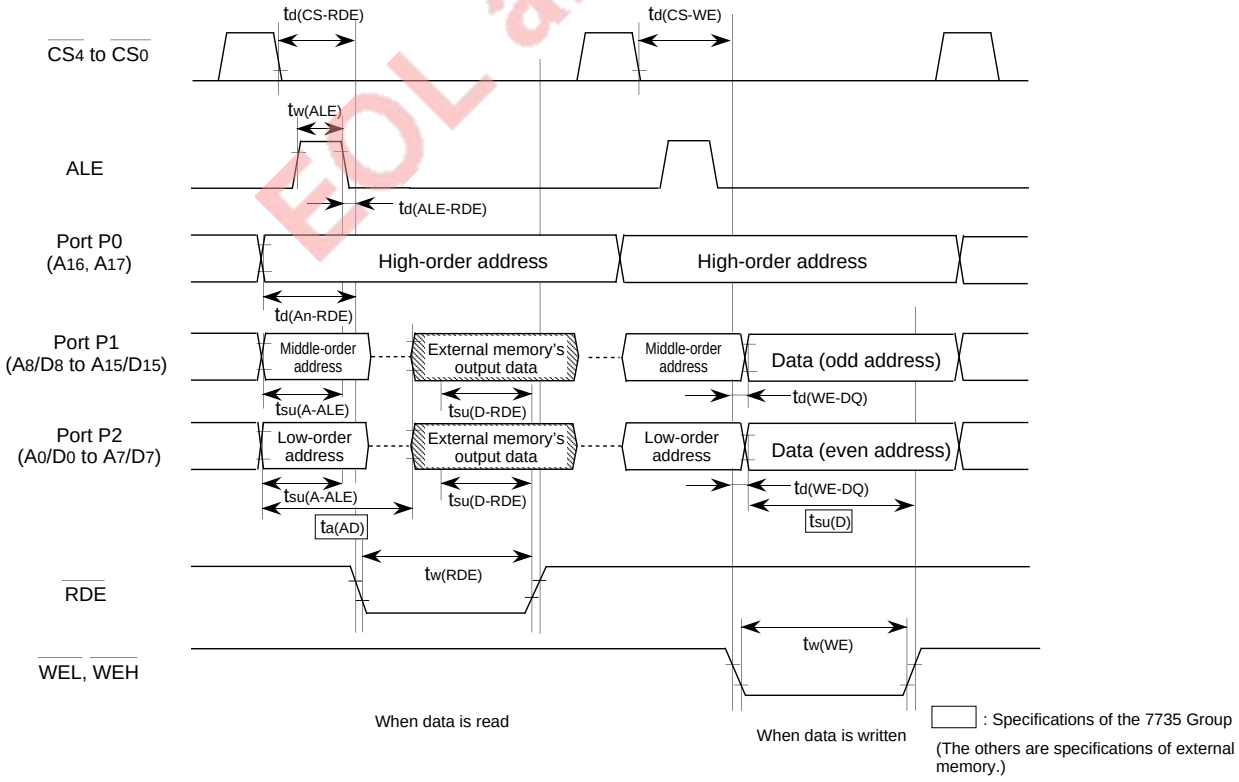


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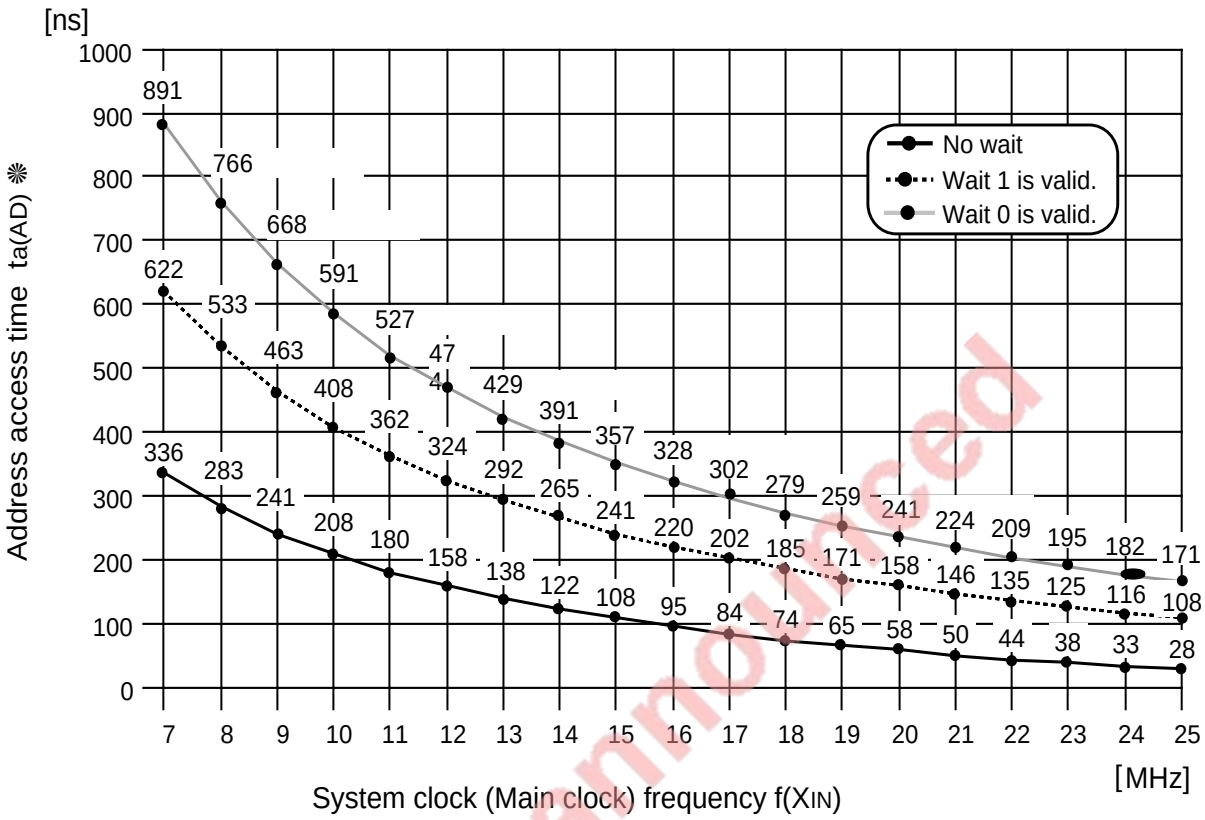
Fig. 17.1.1 Bus timing diagrams

APPLICATIONS

17.1 Memory expansion

Figure 17.1.2 shows the relationship between $t_{a(AD)}$, $t_{su(D)}$ and the system clock frequency. For $t_{a(AD)}$ in Figure 17.1.2, an address decode time and an address latch delay time are not considered. The actual $t_{a(AD)}$ is a value obtained by subtracting the above times from the value shown in Fig.17.1.2.



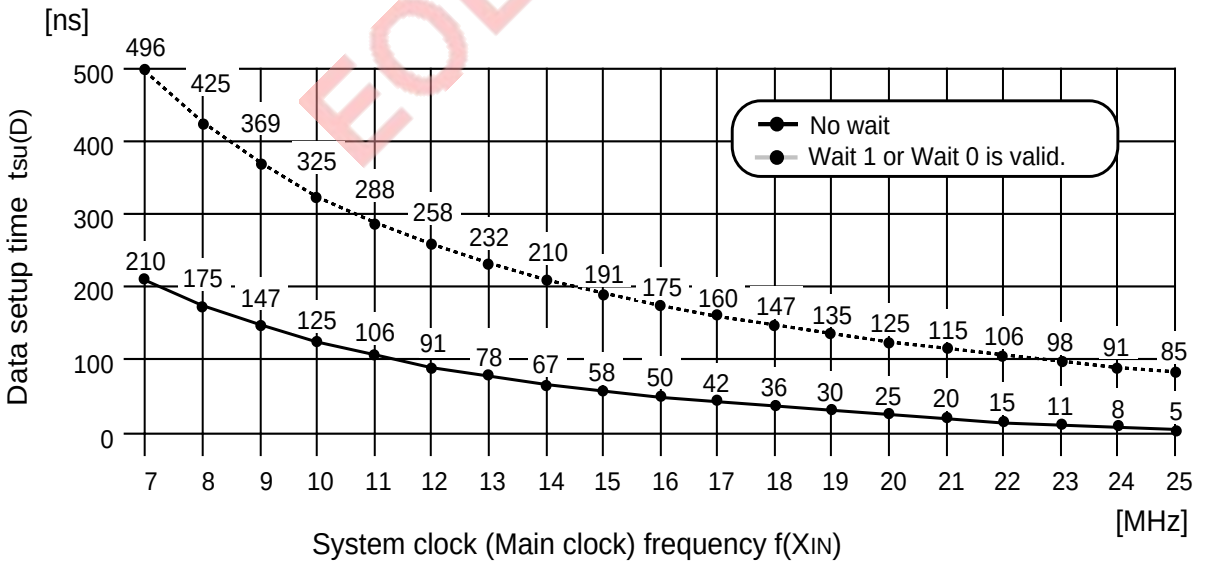


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Fig. 17.1.2 Relationship between $t_{a(AD)}$, $t_{su(D)}$ and $f(X_{IN})$

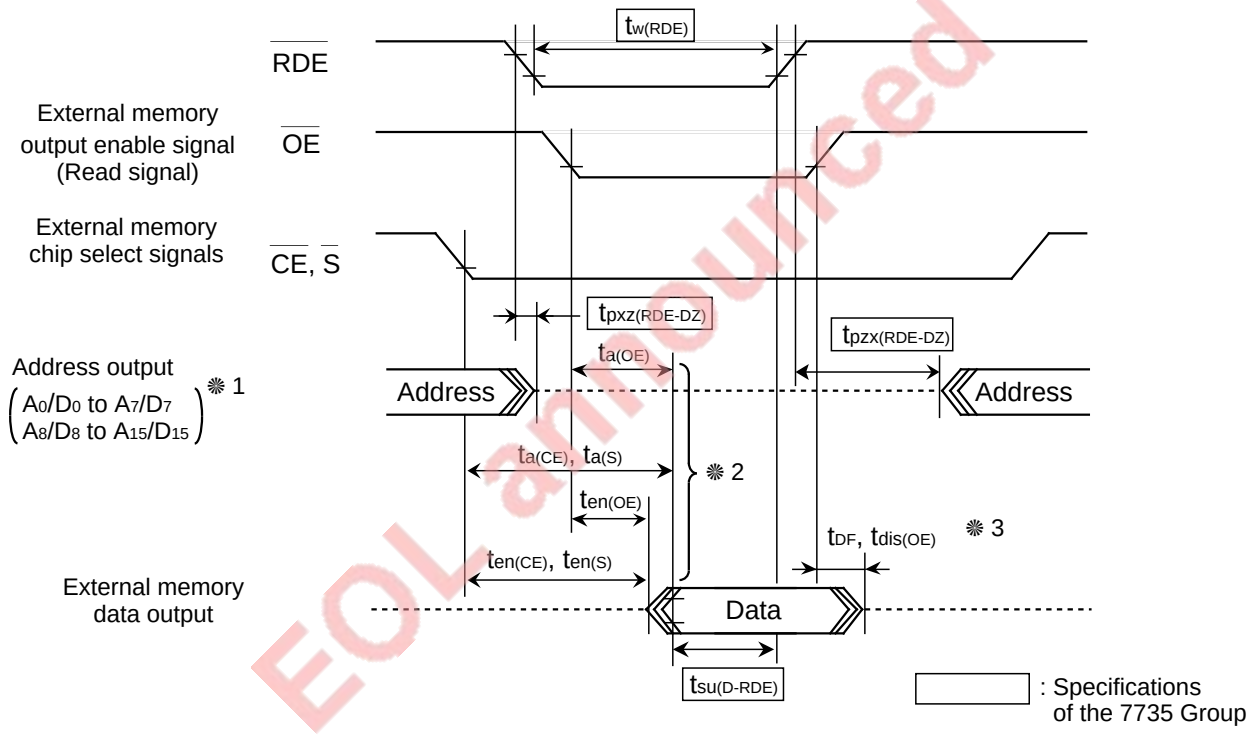
17.1.3 Points in memory expansion

(1) Timing for reading data

Figure 17.1.3 shows the timing at which data is read from an external memory.

When data is read, the external data bus enters a floating state and reads data from an external memory. The floating state of the external data bus is retained from when an interval of $t_{pxz(RDE-DZ)}$ has passed after signal $\overline{RDE}$'s falling edge until an interval of $t_{pzx(RDE-DZ)}$ has passed after signal $\overline{RDE}$'s rising edge. $t_{pxz(RDE-DZ)}$ is a constant which is independent of f(X_{IN}); $t_{pzx(RDE-DZ)}$ is a constant which is dependent on f(X_{IN}). Table 17.1.3 lists the value of $t_{pxz(RDE-DZ)}$ and the calculation formula for $t_{pzx(RDE-DZ)}$.

Note that the external data bus is multiplexed with the external address bus. Therefore, when reading data, it is necessary to consider timing to avoid collision between data being read-in and an address which is output preceding or following the data. (Refer to **"(3) Precautions on memory expansion."**)



✵ 1 This is applied when the external data bus = 16 bits wide (BYTE = "L").

✵ 2 When the external memory's specifications are smaller than $t_{pxz(RDE-DZ)}$, there is a possibility that the tail of an address collides with the head of data. → Refer to **"(3) Precautions on memory expansion."**

✵ 3 When the external memory's specifications are greater than $t_{pzx(RDE-DZ)}$, there is a possibility that the tail of data collides with the head of an address. → Refer to **"(3) Precautions on memory expansion."**

Fig. 17.1.3 Timing at which data is read from external memory

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APPLICATIONS

17.1 Memory expansion

Table 17.1.3 Value of $t_{pxz(RDE-DZ)}$ and calculation formula for $t_{pzx(RDE-DZ)}$ (Unit: ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{pxz(RDE-DZ)}$	5		
$t_{pzx(RDE-DZ)}$	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		

Wait bit: Bit 2 at address $5E_{16}$
Wait selection bit: Bit 0 at address $5F_{16}$
Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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(2) Timing for writing data

Figure 17.1.4 shows the timing for writing data to an external memory.

When data is written, the data is output from when an interval of $t_{d(WE-DQ)}$ has passed after signal $\overline{WEL}/\overline{WEH}$'s falling edge until an interval of $t_{h(WE-DQ)}$ has passed after signal $\overline{WEL}/\overline{WEH}$'s rising edge. $t_{d(WE-DQ)}$ is a constant which is independent of $f(X_{IN})$; $t_{h(WE-DQ)}$ is a constant which is dependent on $f(X_{IN})$. Table 17.1.4 lists the value of $t_{d(WE-DQ)}$ and the calculation formula for $t_{h(WE-DQ)}$.

Make sure that the data output timing for writing data satisfies the following specifications of the external memory: data setup time ($t_{su(D)}$) and data hold time ($t_{h(D)}$) for writing data.

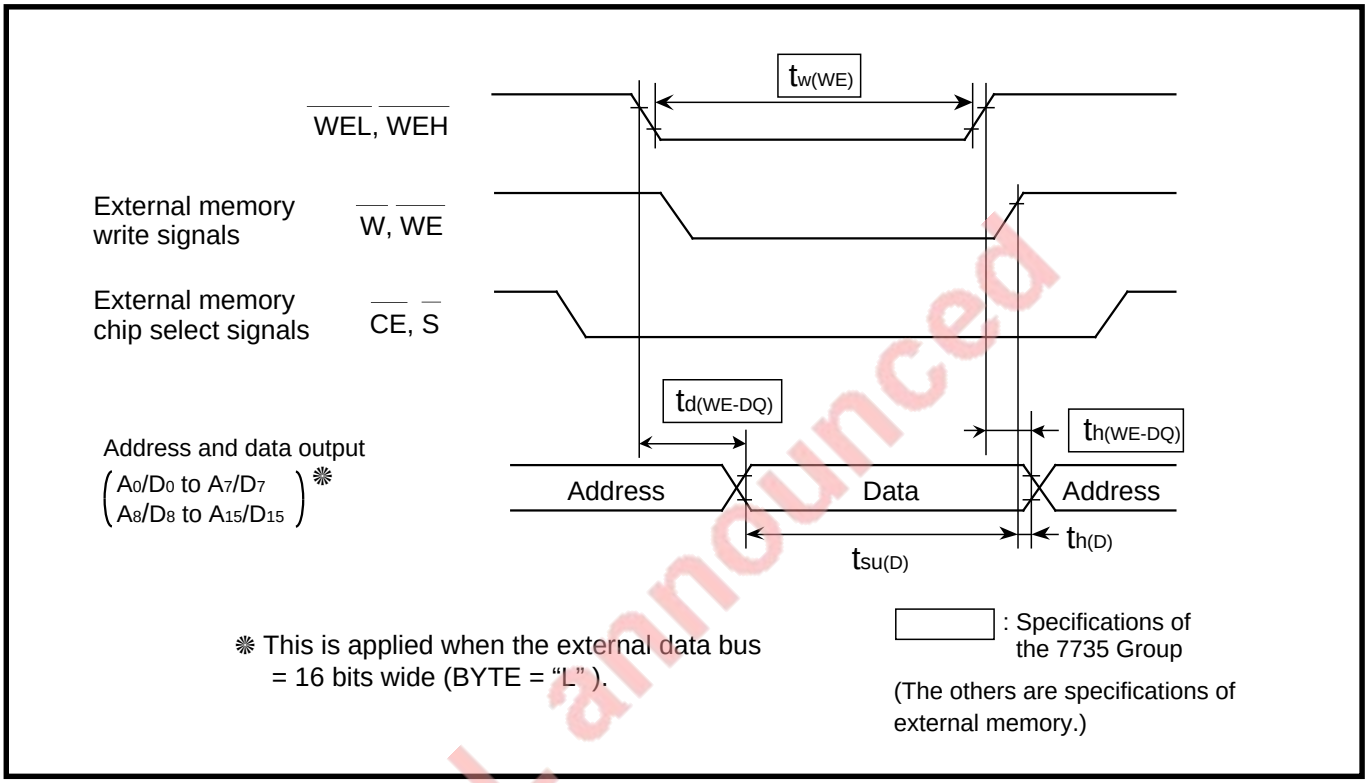

Fig. 17.1.4 Timing at which data is written to external memory

Table 17.1.4 Value of $t_{d(WE-DQ)}$ and calculation formula for $t_{h(WE-DQ)}$ (Unit: ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{d(WE-DQ)}$	45		
$t_{h(WE-DQ)}$	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		

Wait bit: Bit 2 at address $5E_{16}$

Wait selection bit: Bit 0 at address $5F_{16}$

Note: The above is applied when the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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APPLICATIONS

17.1 Memory expansion

(3) Precautions on memory expansion

When specifications of the 7735 Group do not match those of an external memory as described in the following ① to ③, some considerations about the circuit are necessary:

① When using an external memory which requires a long address access time ($t_{a(AD)}$)
② When using an external memory which outputs data within an interval of $t_{pxz(RDE-DZ)}$ after signal $\overline{RDE}$'s falling edge
③ When using an external memory which outputs data for more than an interval of $t_{pzx(RDE-DZ)}$ after signal $\overline{RDE}$'s rising edge

① **When using an external memory which requires a long address access time ($t_{a(AD)}$)**

When an external memory requires a long address access time ($t_{a(AD)}$) which does not satisfy the 7735 Group's $t_{su(D-RDE)}$, try to lower f(X_{IN}) or extend a bus cycle by inserting a wait.
There are two methods for insertion of a wait: the software wait and the ready function. For the software wait, refer to section **"12.2 Software wait"**; for the ready function, refer to section **"12.3 Ready function."**

- Wait 1 (Software wait)
  Insert a wait equivalent to one cycle of clock ϕ_1 while signal $\overline{RDE}$/$\overline{WEL}$/$\overline{WEH}$ is at "L"-level.
- Wait 0 (Software wait)
  Insert a wait equivalent to one cycle of clock ϕ_1 while signal $\overline{RDE}$/$\overline{WEL}$/$\overline{WEH}$ is at "H"- and "L"-levels.
- Ready function
  Insert a wait in an arbitrary duration.

Figure 17.1.5 shows a ready generating circuit example (with no wait). In Figure 17.1.5, when f(X_{IN}) > 20.7 MHz, the setup time for the $\overline{RDY}$ input ($t_{su(RDY-\phi_1)}$) is insufficient. In this case, refer to **the ready generating circuit example (with wait 1) shown in Figure 17.1.6.** In Figure 17.1.6, $t_{su(RDY-\phi_1)}$ is satisfied when f(X_{IN}) ≤ 25 MHz. Note that a wait generated by the ready function is also valid for the access to the internal area. Therefore, in Figures 17.1.5 and 17.1.6, areas where the wait is inserted are specified by using signals $\overline{RSMP}$ and CS_0.
For circuits where the software wait is used, refer to **Figures 17.1.2 to 17.1.5.**

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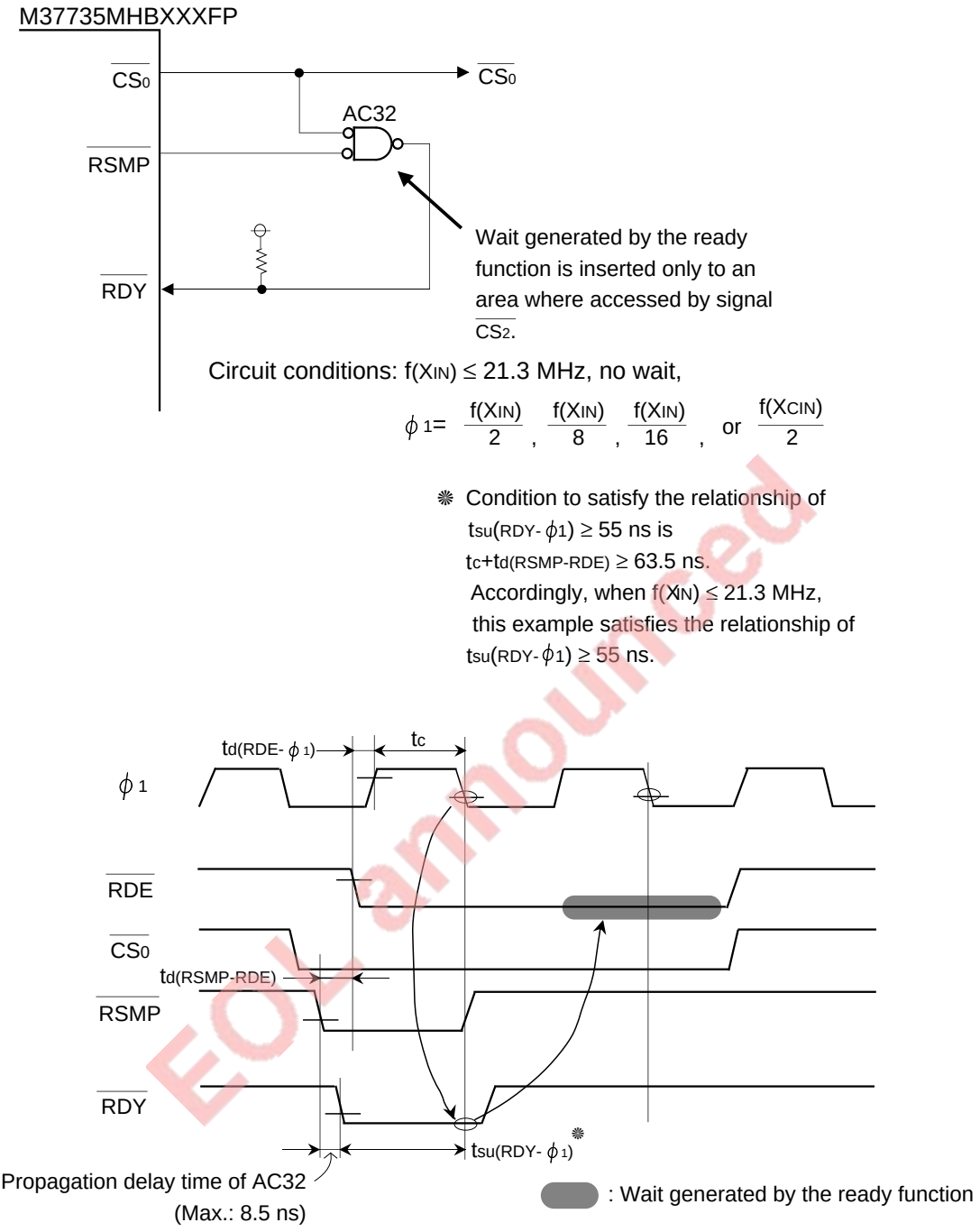

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Fig. 17.1.5 Ready generating circuit example (with no wait)

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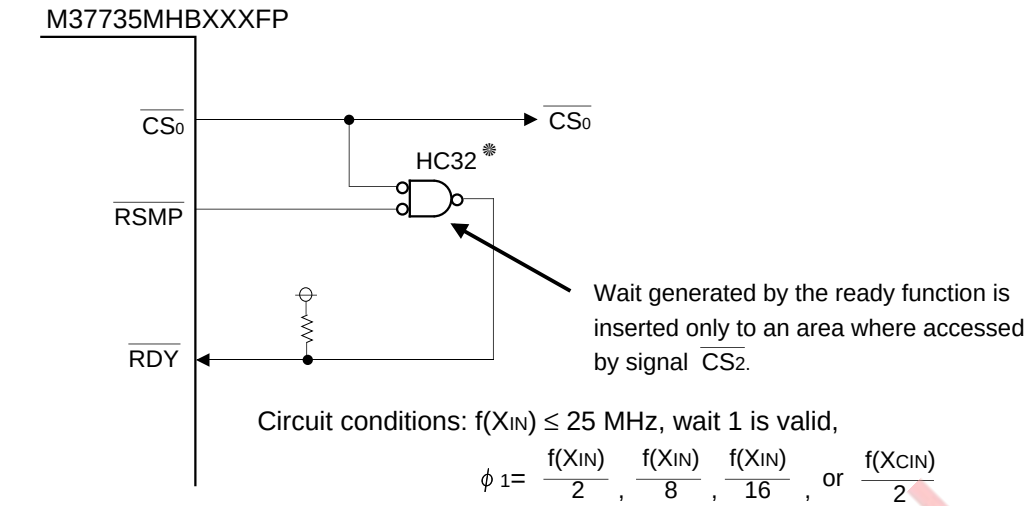
17.1 Memory expansion



Circuit conditions: $f(X_{IN}) \leq 25$ MHz, wait 1 is valid,

$$\phi_1 = \frac{f(X_{IN})}{2}, \frac{f(X_{IN})}{8}, \frac{f(X_{IN})}{16}, \text{ or } \frac{f(X_{CIN})}{2}$$

✺ Make sure that the propagation delay time is within

$$\frac{3 \times 10^9}{f(X_{IN})} + t_{d(RSMP-RDE)} - t_{su(RDY-\phi_1)}$$

(when $f(X_{IN})$ = 25 MHz, 75 ns).

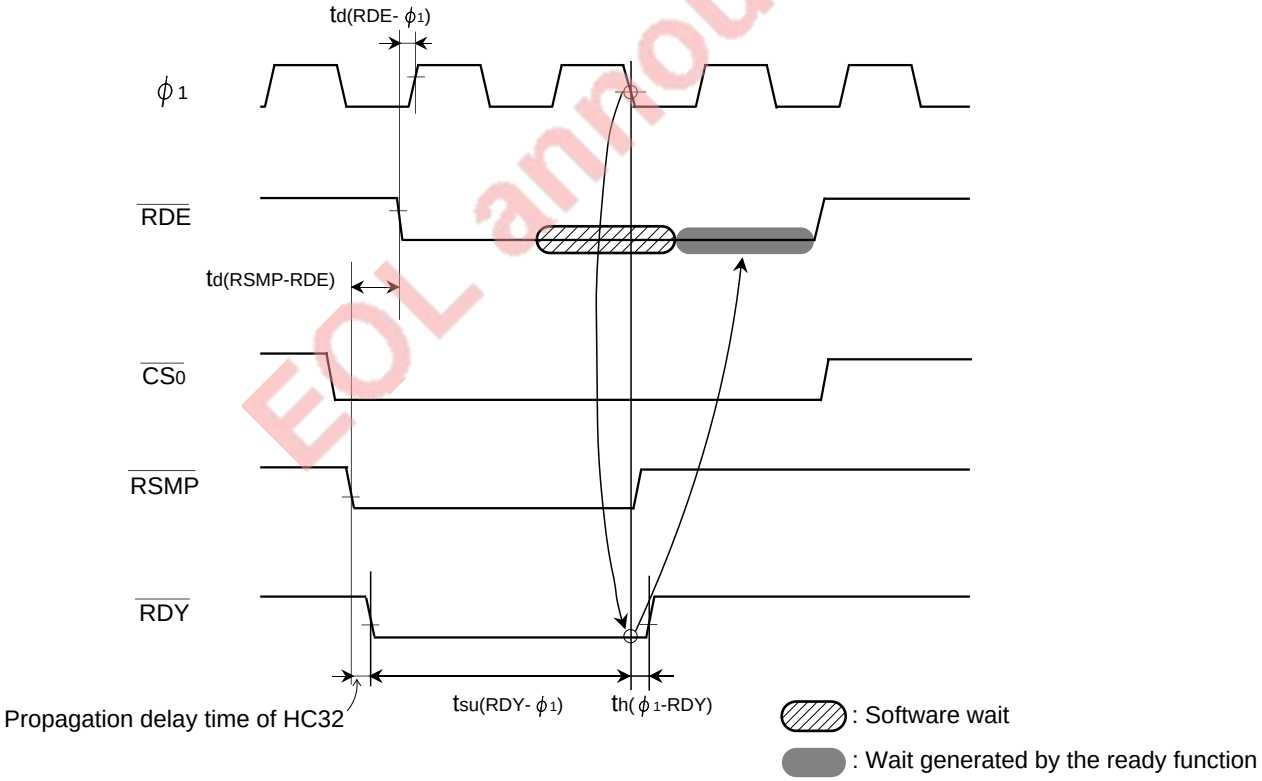


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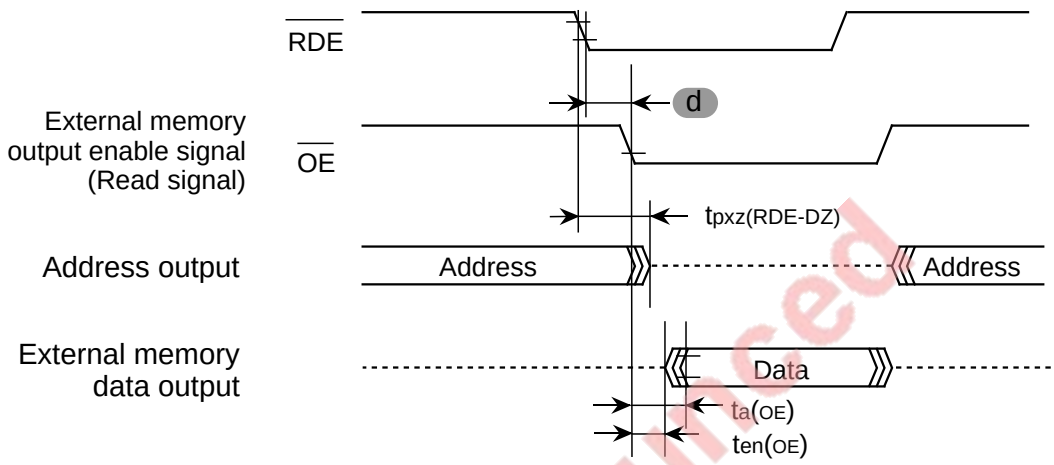
Fig. 17.1.6 Ready generating circuit example (with wait 1)

② **When using an external memory which outputs data within an interval of $t_{pxz(RDE-DZ)}$ after signal $\overline{RDE}$'s falling edge**

When there is a possibility that the tail of an address collides with the head of data because the external memory outputs data within an interval of $t_{pxz(RDE-DZ)}$ after signal $\overline{RDE}$'s falling edge, delay only the signal $\overline{RDE}$'s front falling edge and realize the relationship of $t_{pxz(RDE-DZ)}$-d < $t_{en(OE)}$. In this case, the falling edge of the read signal ($\overline{OE}$) for the memory, which is generated from signal $\overline{RDE}$, is delayed. (Refer to **Figure 17.1.7.**)



Note: When $t_{en(OE)} \leq t_{pxz(RDE-DZ)}$(= 5 ns), make sure that signal $\overline{RDE}$'s falling edge precedes signal $\overline{OE}$'s falling edge (Refer to "d") and the relationship of $t_{pxz(RED-DZ)}$-d ≤ $t_{en(OE)}$ is realized.

Fig. 17.1.7 Timing example when data output is delayed

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17.1 Memory expansion

③ **When using an external memory which outputs data for more than an interval of $t_{pzx(RDE-DZ)}$ after signal $\overline{RDE}$'s rising edge**

When there is a possibility that the tail of data collides with the head of an address because the external memory outputs the data for more than an interval of $t_{pzx(RDE-DZ)}$ after signal $\overline{RDE}$'s rising edge, try to carry out the following:

- By using bus buffers and others, delete the tail of data which is output from the memory.
- Use a memory which is made by MITSUBISHI ELECTRIC CORPORATION and can be connected without bus buffers.

Figures 17.1.8 to 17.1.11 show bus buffer usage examples and the corresponding timing diagrams. Table 17.1.5 lists memories which can be connected without bus buffers (made by MITSUBISHI ELECTRIC CORPORATION). The reason why these memories do not need buffers is that timing parameters t_{DF} or $t_{dis(OE)}$ is guaranteed. (Make sure that the read signal rises within 5 ns after signal $\overline{RDE}$'s rising edge.)

Table 17.1.5 Memories which can be connected without bus buffers (made by MITSUBISHI ELECTRIC CORPORATION)

Memory	Type	$t_{DF}/t_{dis(OE)}$ (Max.)	Usage condition
EPROM	M5M27C256AK-85, -10, -12, -15 M5M27C512AK-10, -12, -15 M5M27C100K-12, -15 M5M27C101K-12, -15 M5M27C102K-12, -15 M5M27C201K, JK-10, -12, -15 M5M27C202K, JK-10, -12, -15	15 ns (When guaranteed as kit) (**Note**)	2 • f(f_2) ≤ 20 MHz
One time PROM	M5M27C256AP, FP, VP, RV-12, -15 M5M27C512AP, FP-15 M5M27C100P-15 M5M27C101P, FP, J, VP, RV-15 M5M27C102P, FP, J, VP, RV-15 M5M27C201P, FP, J, VP, RV-12, -15 M5M27C202P, FP, J, VP, RV-12, -15		
Frash memory	M5M28F101P, FP, J, VP, RV-10, -12, -15 M5M28F102FP, J, VP, RV-10, -12, -15		
SRAM	M5M5256CP, FP, KP, VP, RV-55LL, -55XL, -70LL, -70XL, -85LL, -85XL, -10LL, -10XL		
	M5M5278CP, FP, J-20, -20L	8 ns	2 • f(f_2) ≤ 25 MHz
	M5M5278CP, FP, J-25, -25L	10 ns	
	M5M5278DP, J-12	6 ns	
	M5M5278DP, FP, J-15, -15L	7 ns	
	M5M5278DP, FP, J-20, -20L	8 ns	

Note: Specifications of the above memories are available if a comment "t_{DF}/t_{dis} = 15 ns, microcomputer and kit" is added.

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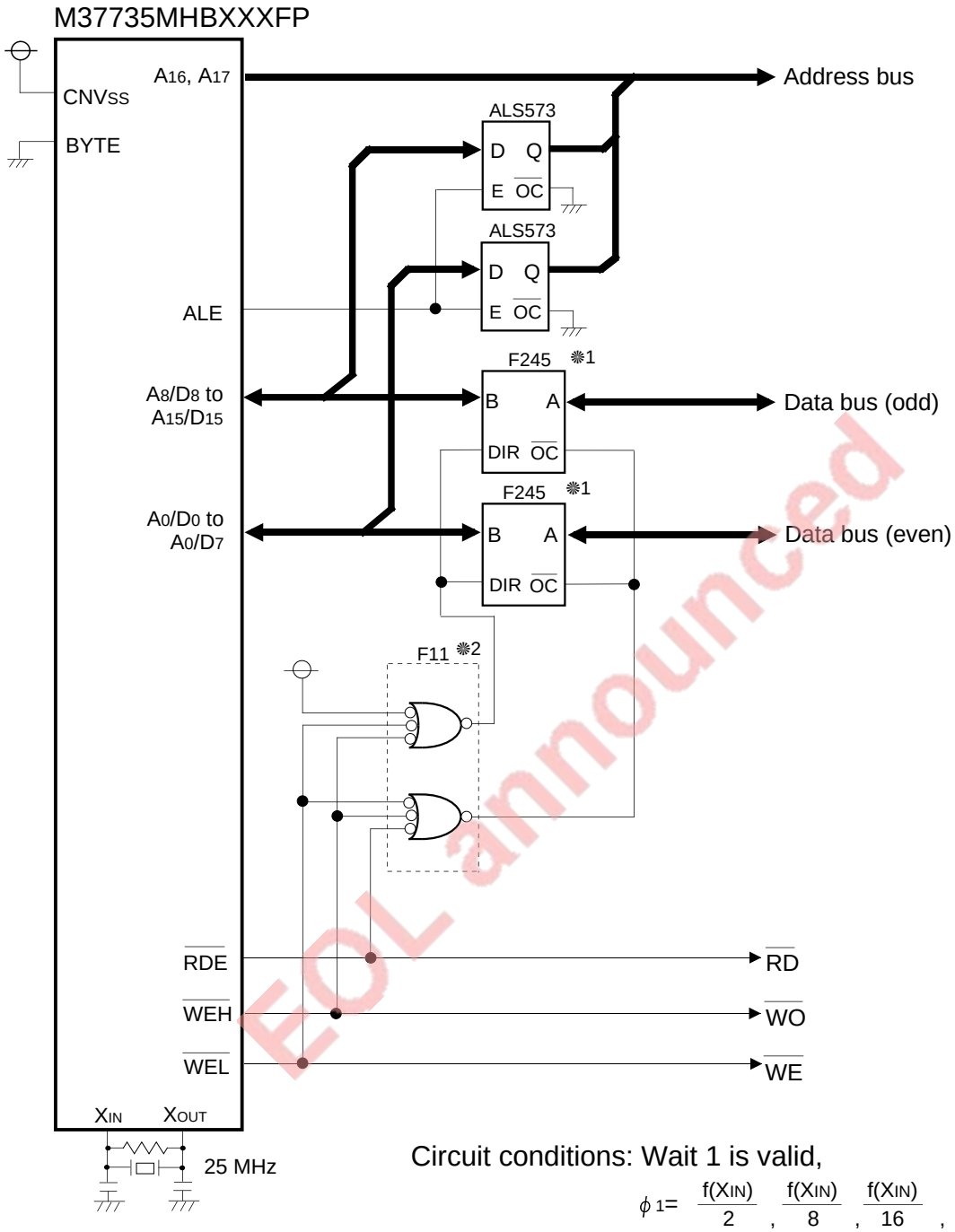

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Fig. 17.1.8 Bus buffer usage example (1)

APPLICATIONS

17.1 Memory expansion

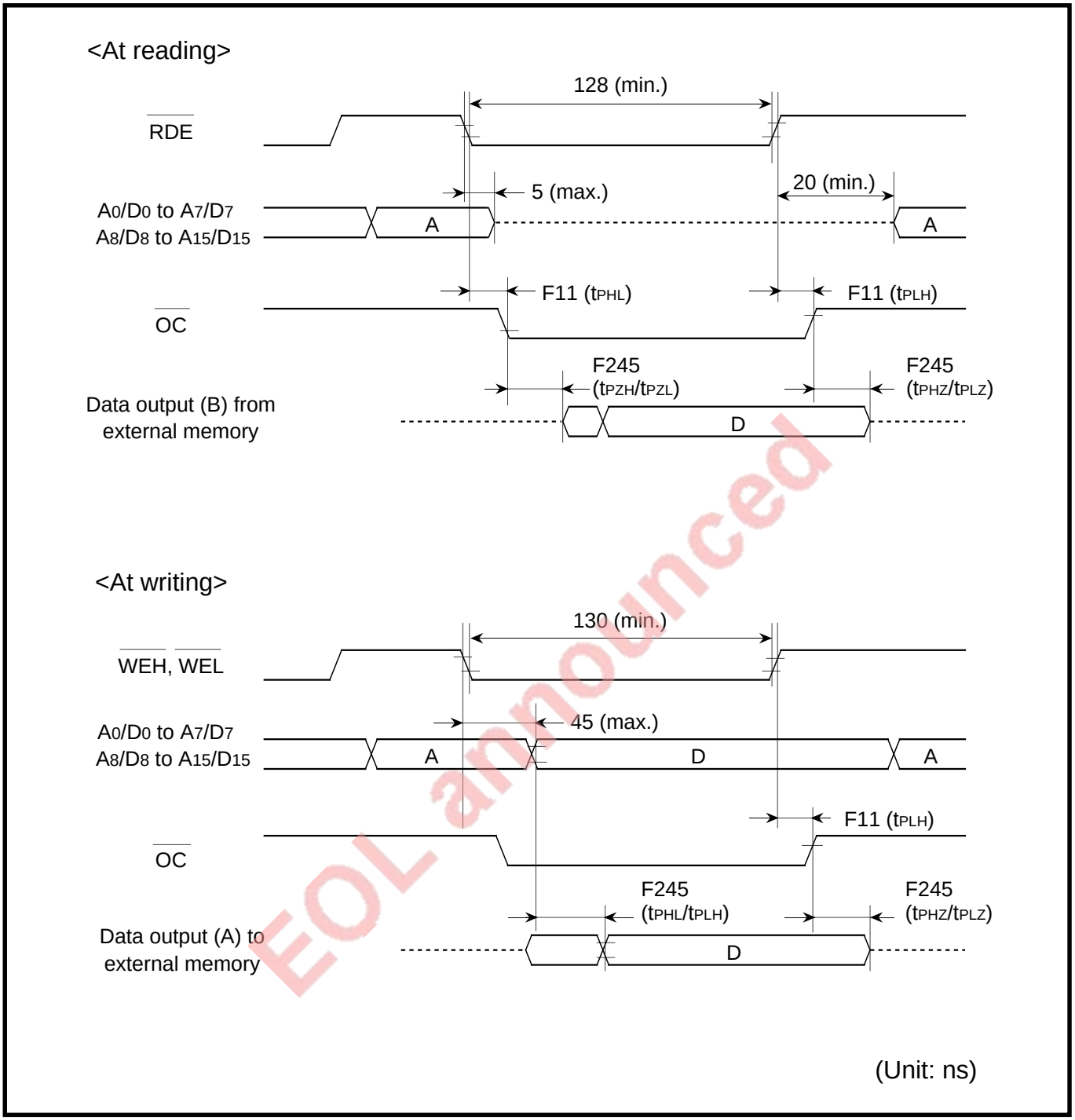

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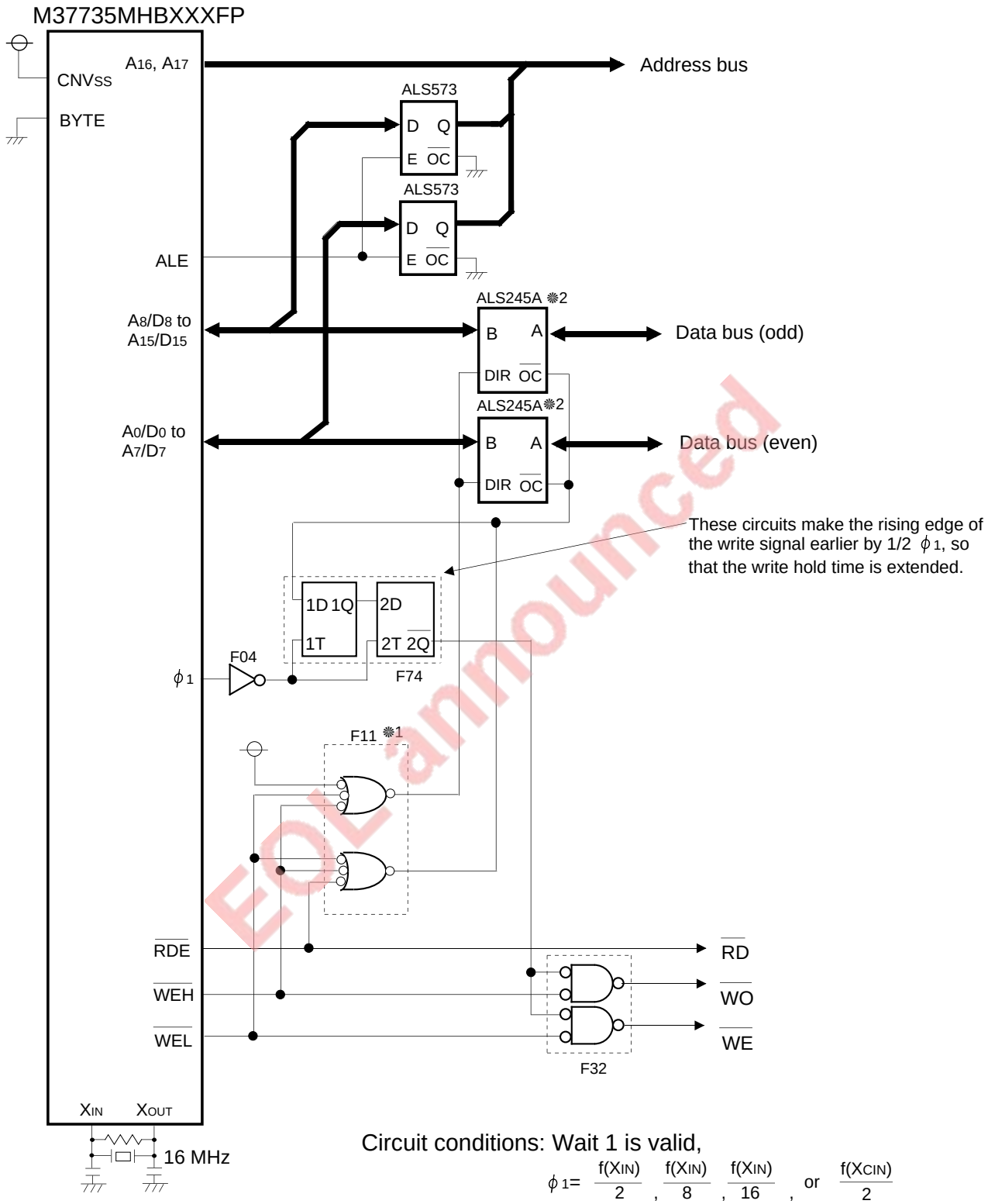
Fig. 17.1.9 Timing diagram for bus buffer usage example (1)



❋1 Make sure that the propagation delay time is 20 ns or less.

❋1, ❋2 Make sure that the following relationships are satisfied:

- The sum of propagation delay time of ❋1 and output disable time of ❋2 is 42.5 ns or less.
- The sum of propagation delay time of ❋1 and output enable time of ❋2 is 5 ns or more.

Fig. 17.1.10 Bus buffer usage example (2) (when a memory which requires a long data hold time for writing is connected)

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APPLICATIONS

17.1 Memory expansion

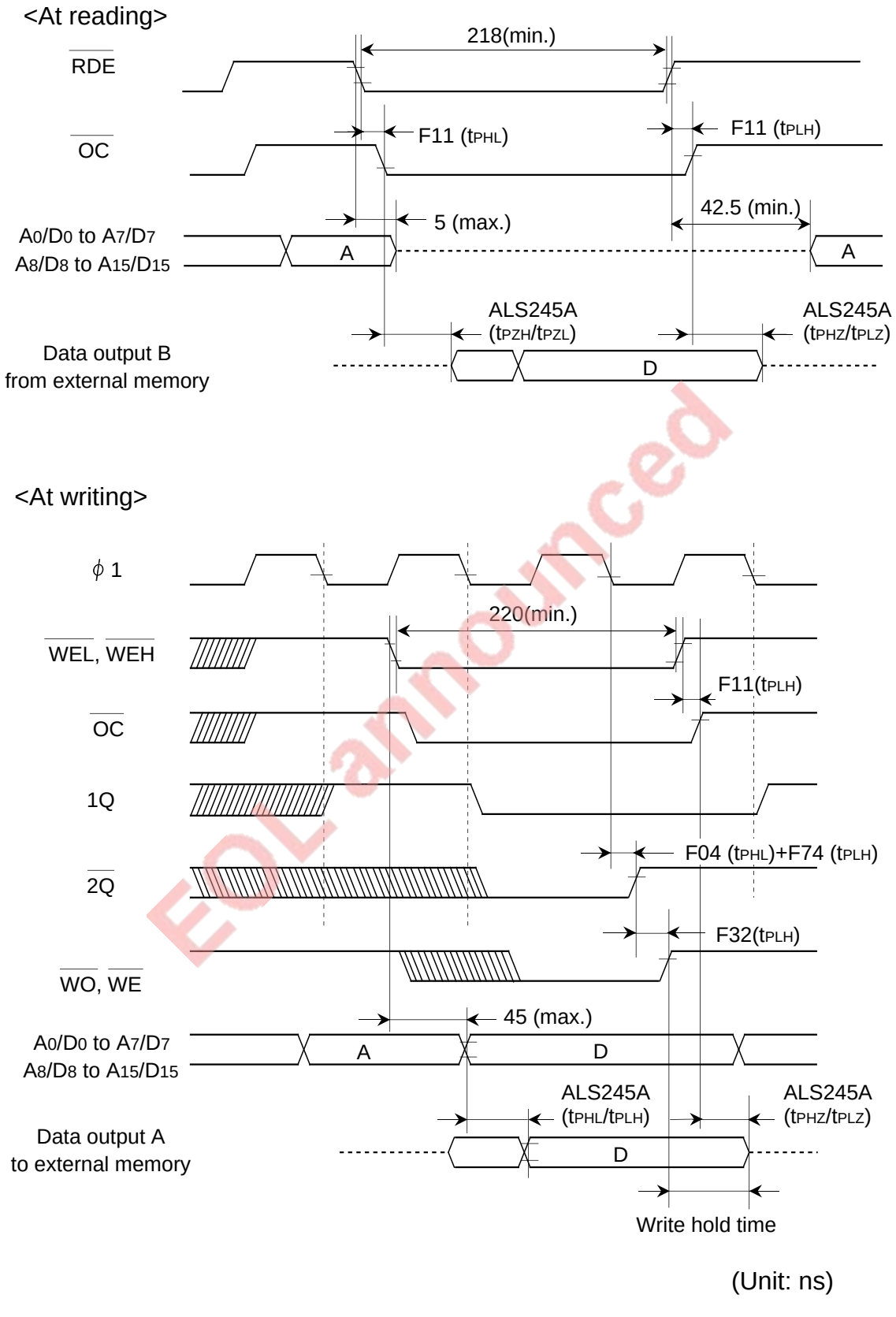

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Fig. 17.1.11 Timing diagram for bus buffer usage example (2)

17.1.4 Memory expansion example

Figure 17.1.12 shows a memory expansion example (with one 128-Kbyte ROM and two 32-Kbyte SRAMs, microprocessor mode). Figure 17.1.13 shows the corresponding timing diagram.

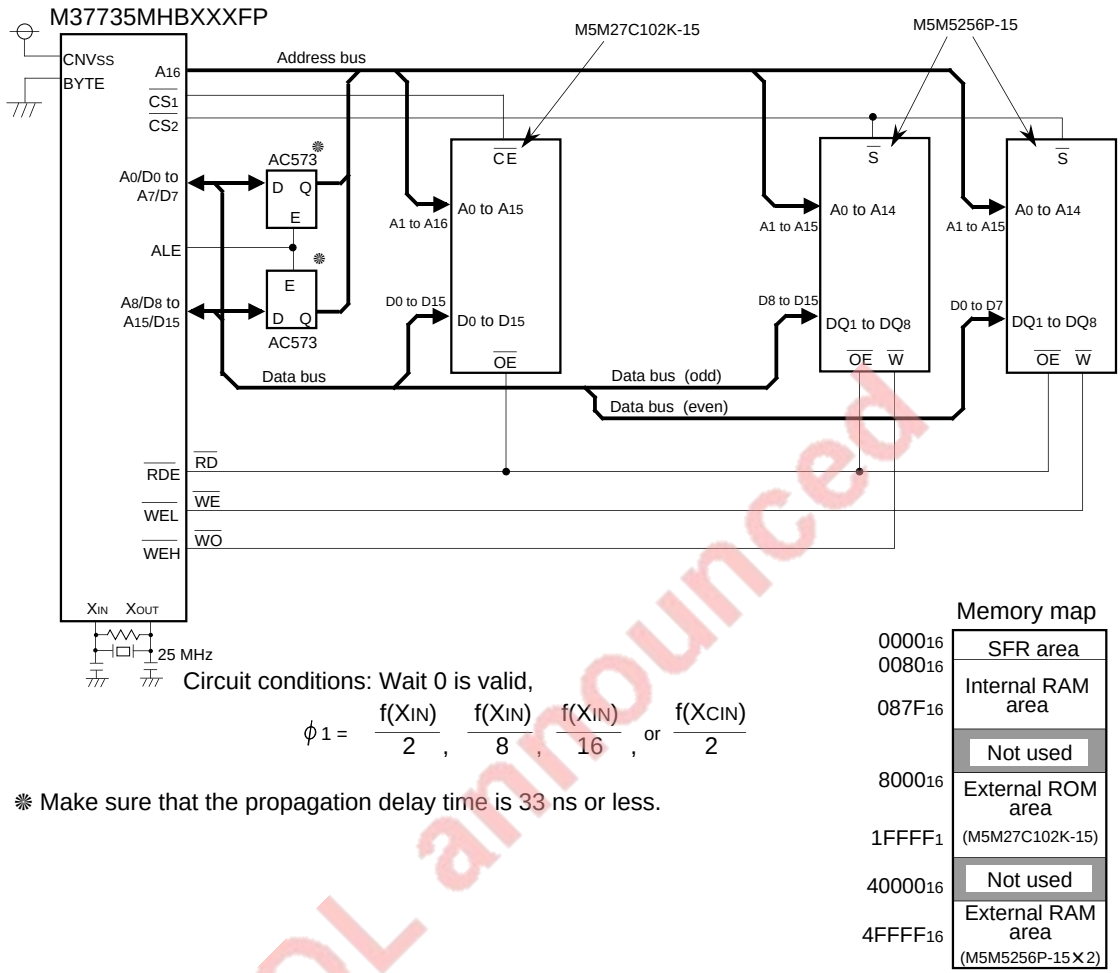

Fig. 17.1.12 ROM and SRAM expansion example

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APPLICATIONS

17.1 Memory expansion

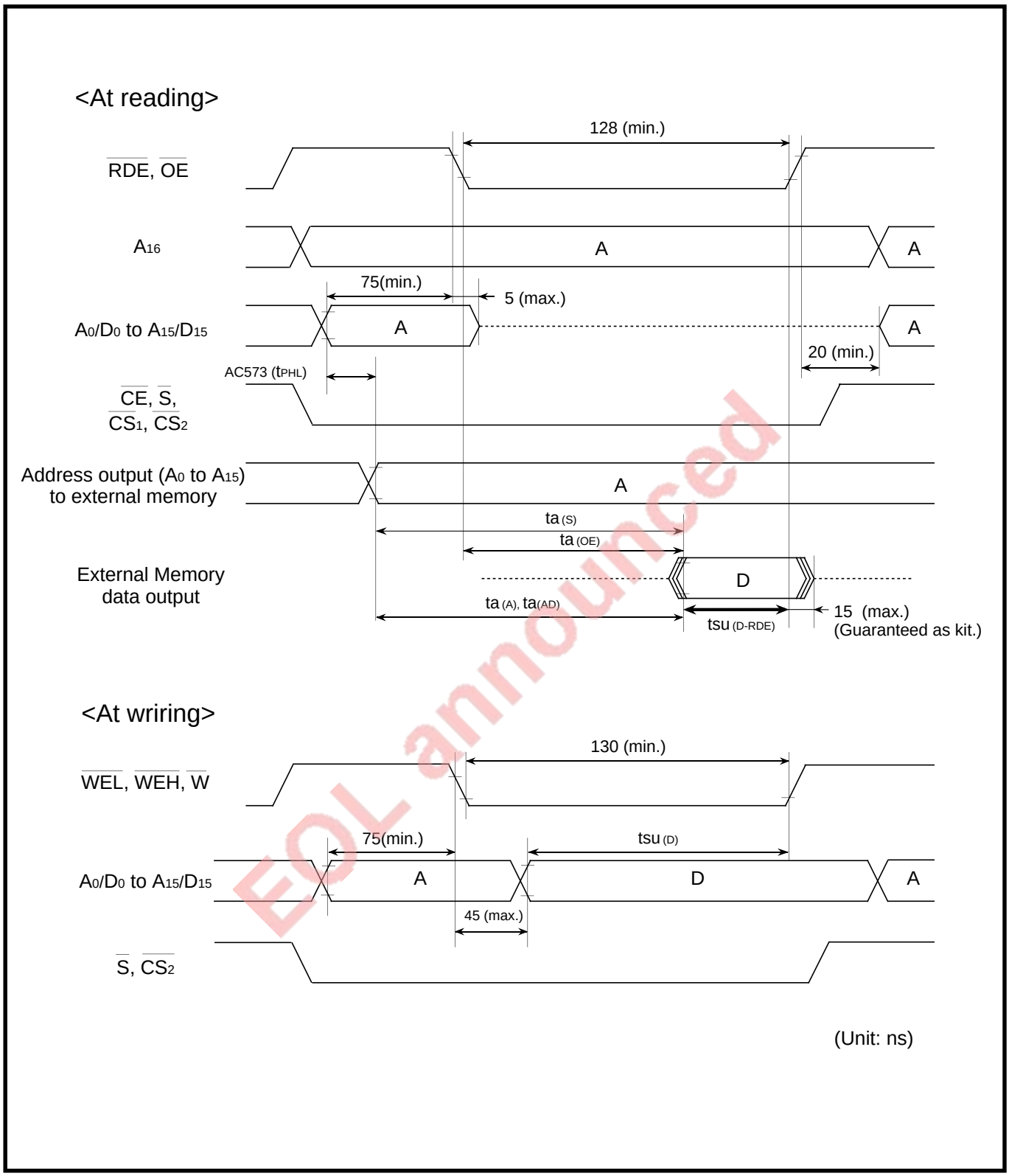

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Fig. 17.1.13 Timing diagram for ROM and SRAM expansion example

17.1.5 I/O expansion example

I/O expansion is realized with the memory-mapped method. The method and points in I/O expansion are the same as those in memory expansion.

Figure 17.1.15 shows a port expansion example using the M5M81C55P-2. In this example, the M5M81C55P-2 is connected to the external data bus and programmable I/O ports expand by 22 bits. A reset signal for an external device is supplied from port P43 and IO/$\overline{M}$ is supplied from port P44.

Note that, when f(XIN) > 10 MHz, bus buffer ALS245A or others is necessary.

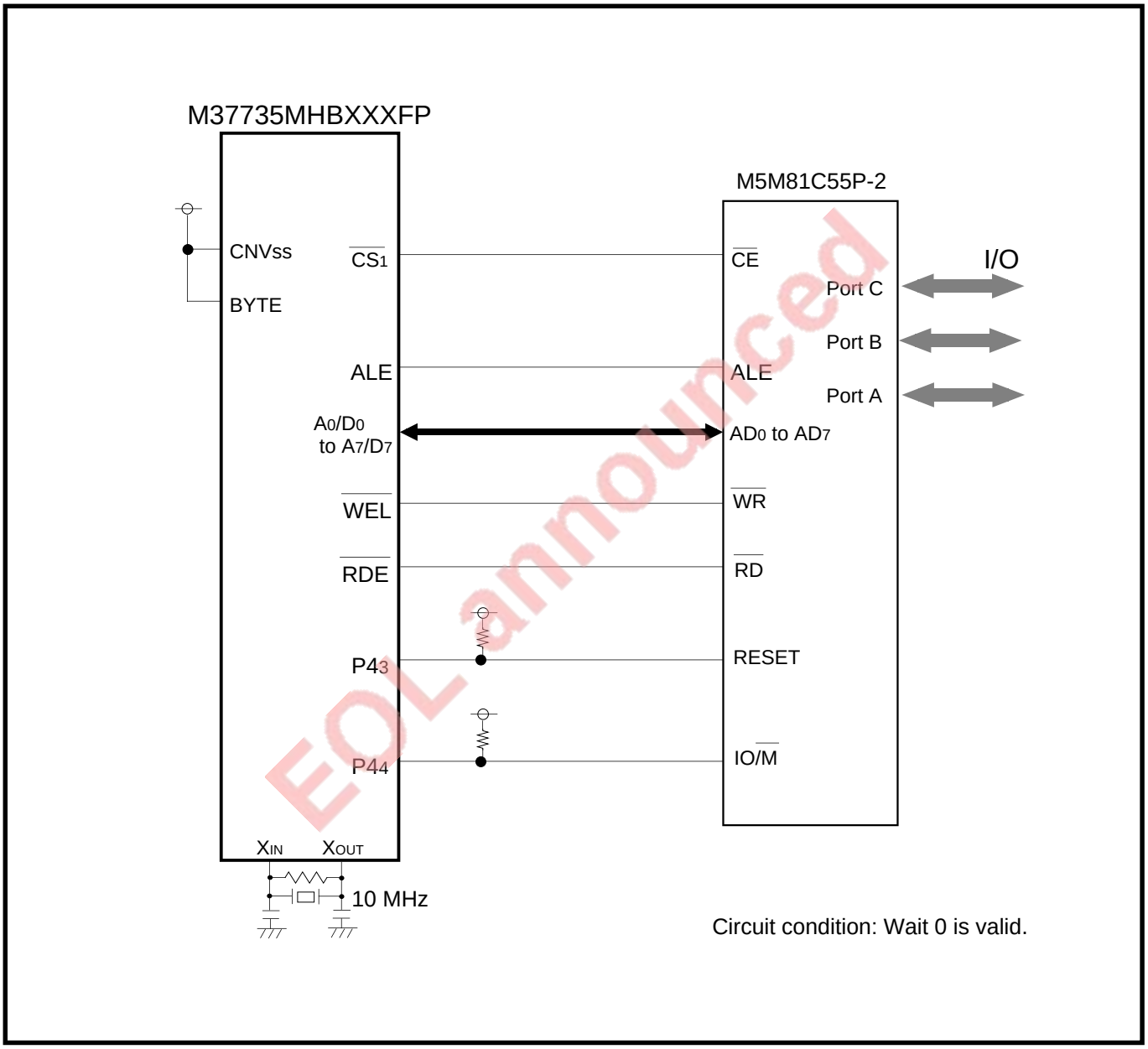

Fig. 17.1.14 Port expansion example where M5M81C55P-2 is used

17.4 Power saving

Concerning section “17.4 Power saving,” the 7735 Group differs from the 7733 Group in the following:

- **Bit 3 of the oscillation circuit control register 1 (address $6F_{16}$) must be fixed to “0.”**
- **External bus pins’ functions for ports P0 to P3**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“17.4 Power saving” (page 17-44 in part 1)**

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CHAPTER 18
LOW VOLTAGE VERSION

EOL announced

18.1 Performance overview
18.2 Pin configuration
18.3 Functional description
18.4 Electrical characteristics
18.5 Standard characteristics
18.6 Applications

LOW VOLTAGE VERSION

18.1 Performance overview

Concerning chapter “18. LOW VOLTAGE VERSION,” the 7735 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“18.1 Performance overview”**
- **“18.2 Pin configuration”**
- **“18.3 Functional description”**
- **“18.4 Electrical characteristics”**
- **“18.6 Applications”**

The following section is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“18.5 Standard characteristics”** (**page 18-27 in part 1**)

18.1 Performance overview

Concerning section “18.1 Performance overview,” the 7735 Group differs from the 7733 Group in the following:

- **Description of the memory expansion in Table 18.1.1**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“18.1 Performance overview” (page 18-3 in part 1.)**

Table 18.1.1 M37735MHLXXXHP performance overview

Items	Performance
Memory expansion	Possible (Maximum of 1 Mbytes)

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18.2 Pin configuration

Figure 18.2.1 shows the M37735MHLXXXHP pin configuration.

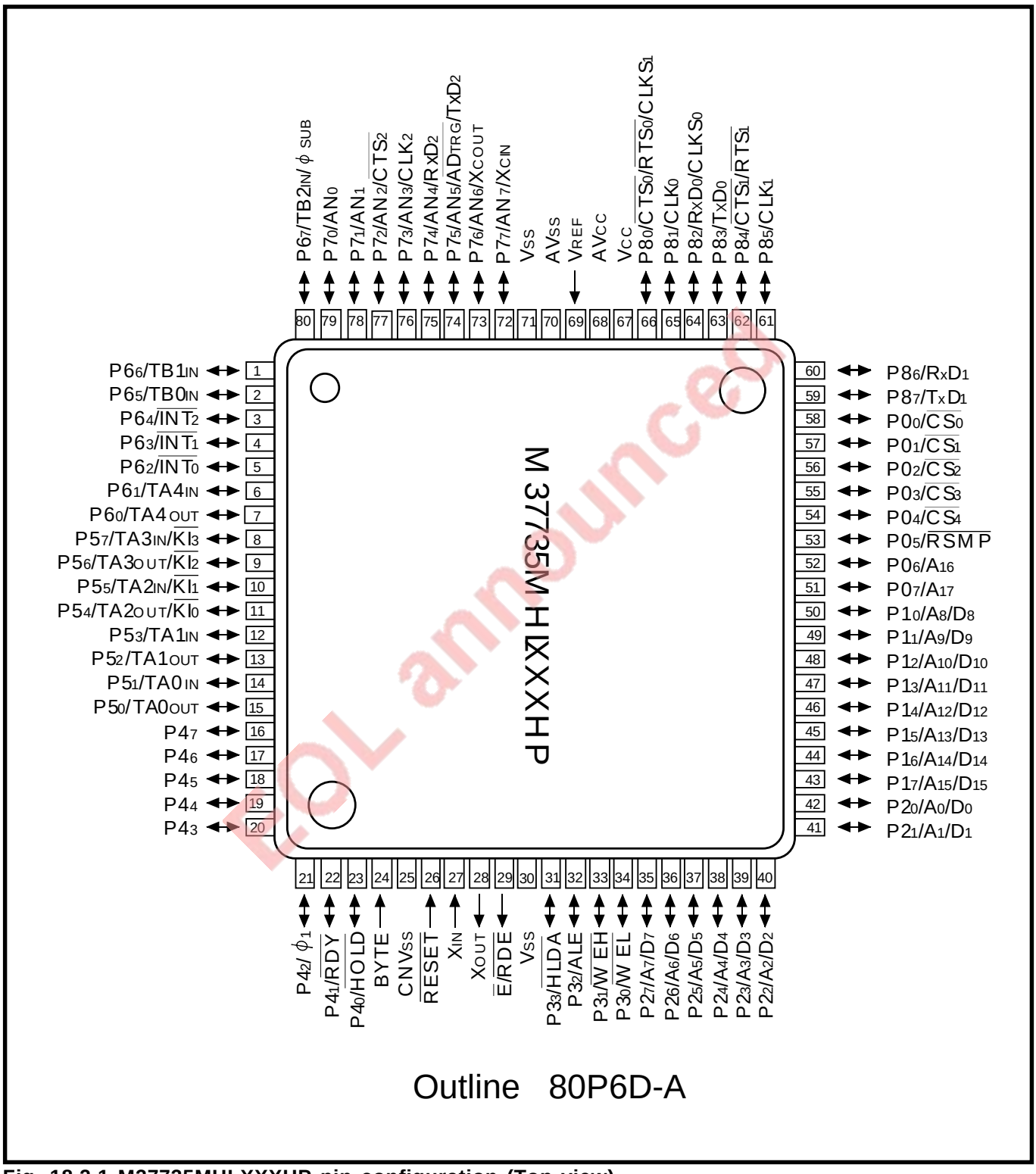

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Fig. 18.2.1 M37735MHLXXXHP pin configuration (Top view)

18.3 Functional description

The M37735MHLXXXHP has the same functions as the M37735MHBXXXFP except for the power-on reset conditions. For power-on reset conditions, refer to section "**18.3.1 Power-on reset conditions**" **in part 1.**

For the other functions, refer to the following:

- **PART 1. 7733 GROUP**
  - **"4. INTERRUPTS"**
  - **"5. KEY INPUT INTERRUPT FUNCTION"**
  - **"6. TIMER A"**
  - **"7. TIMER B"**
  - **"8. SERIAL I/O"**
  - **"9. A-D CONVERTER"**
- **PART 2. 7735 GROUP**
  - **"2. CENTRAL PROCESSING UNIT (CPU)"**
  - **"3. PROGRAMMABLE I/O PORTS"**
  - **"10. WATCHDOG TIMER"**
  - **"11. STOP AND WAIT MODES"**
  - **"12. CONNECTING EXTERNAL DEVICES"**
  - **"13. RESET"**
  - **"14. CLOCK GENERATING CIRCUIT"**

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18.4 Electrical characteristics

Concerning section "18.4 Electrical characteristic," the 7735 Group differs from the 7733 Group in the following sections:

- "**18.4.6 Ready and Hold**"
- "**18.4.8 Memory expansion mode and Microprocessor mode : with no wait**"
- "**18.4.9 Memory expansion mode and Microprocessor mode : with wait 1**"
- "**18.4.10 Memory expansion mode and Microprocessor mode : with wait 0**"

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"18.4 Electrical characteristics" (page 18-7 in part 1)**

18.4.6 Ready and Hold

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(RDY-\phi_1)}$	$\overline{RDY}$ input setup time	80		ns
$t_{su(HOLD-\phi_1)}$	$\overline{HOLD}$ input setup time	80		ns
$t_{h(\phi_1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi_1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Note: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time	Fig. 18.4.1		120	ns

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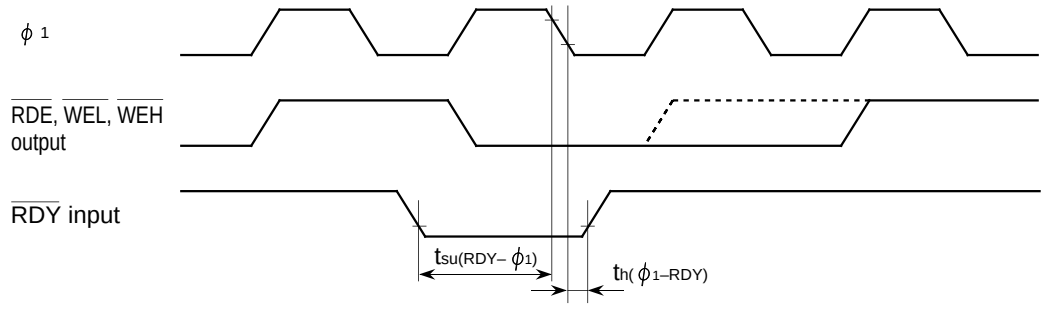
LOW VOLTAGE VERSION

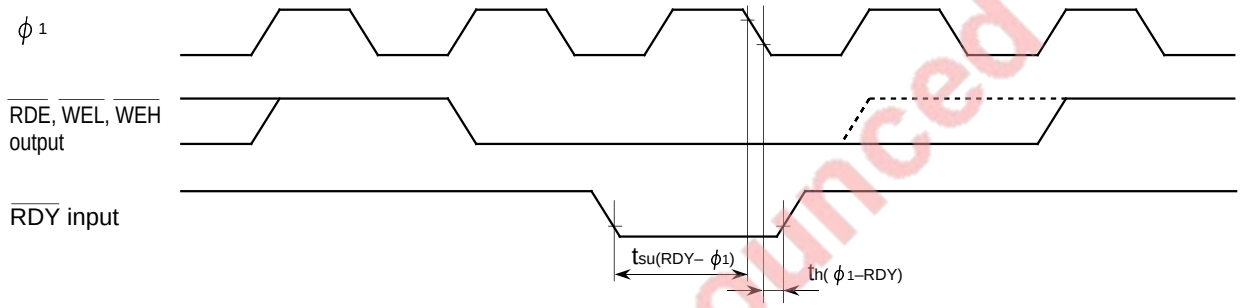
18.4 Electrical characteristics

● Ready

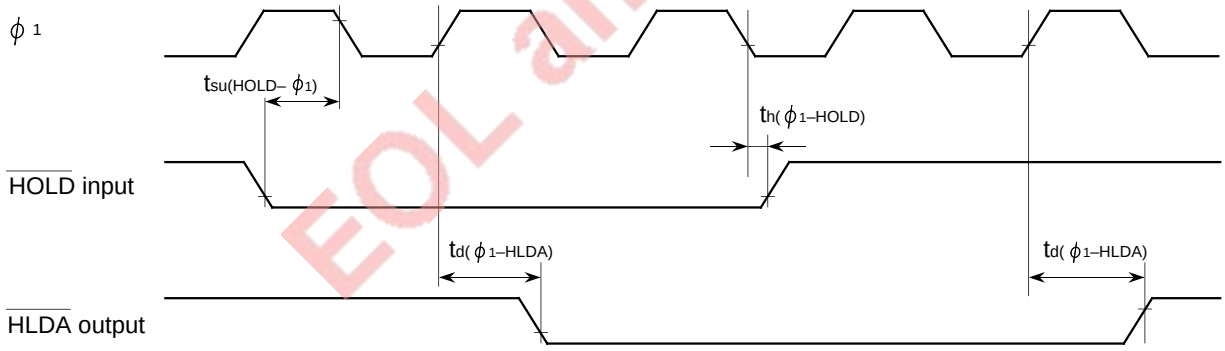
With no wait



With wait



● Hold



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Measuring conditions

- V_{CC} = 2.7 to 5.5 V
- Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

18.4.8 Memory expansion mode and Microprocessor mode : with no wait

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(D–RDE)}$	Data input setup time	80		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: When the main clock division selection bit = "1," the minimum value of t_c = 166 ns.
3: When the main clock division selection bit = "1," values of $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	Fig. 18.4.1	$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 63$	20		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 63$	20		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 63$	20		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 73$	10		ns
$t_{h(ALE–A)}$	Address hold time			9		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time			4		ns
$t_{d(WE–DQ)}$	Data output delay time				90	ns
$t_{h(WE–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{w(WE)}$	$\overline{WEL}$, $\overline{WEH}$ pulse width		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 35$	131		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				10	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 30$	53		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 38$	128		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 58$	25		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time			0	30	ns
$t_{d(\phi 1–HLDA)}$	$\overline{HLDA}$ output delay time				120	ns

Note: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1** in part 1.

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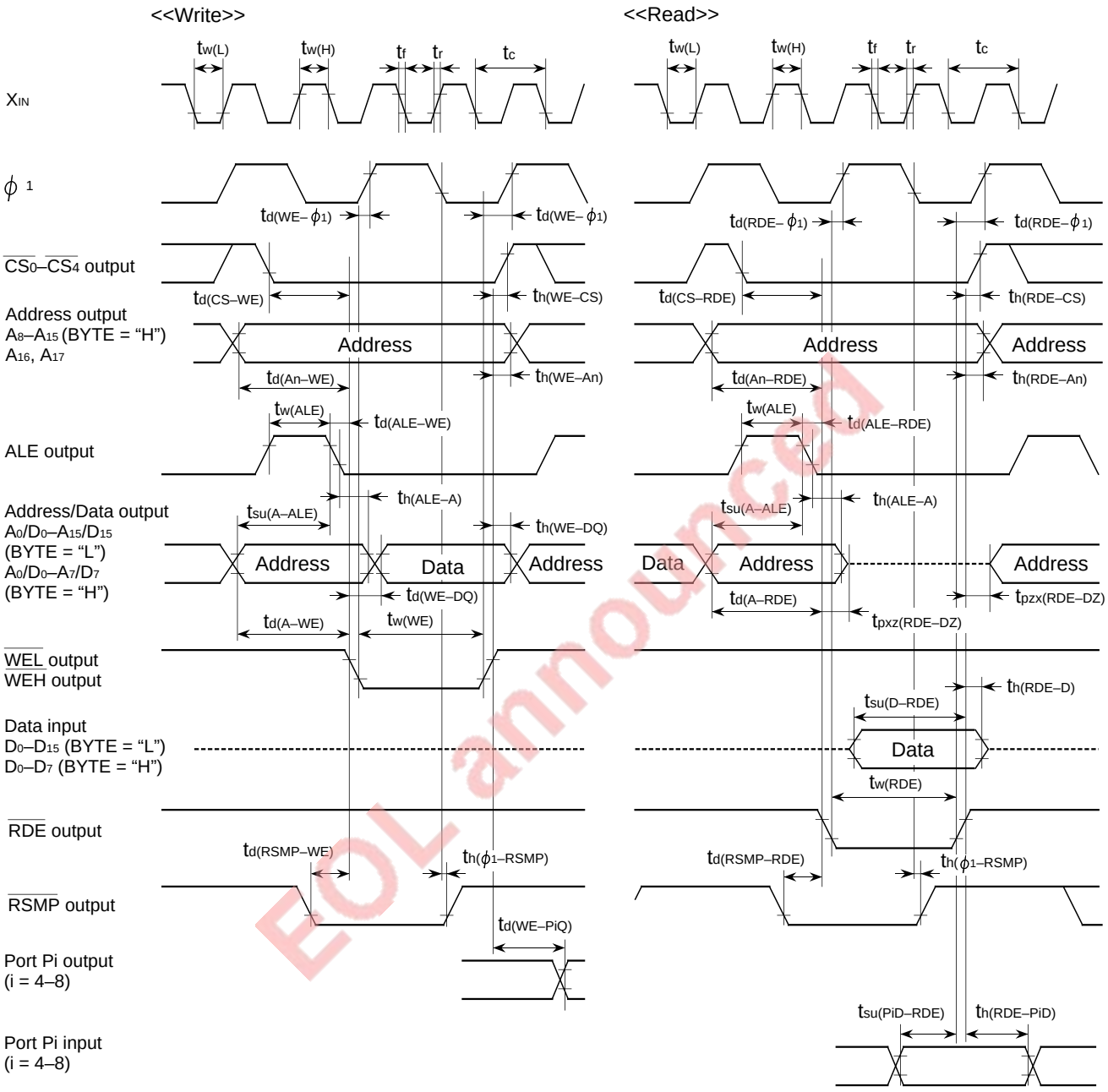
LOW VOLTAGE VERSION

18.4 Electrical characteristics

Memory expansion mode and Microprocessor mode :

With no wait (Wait bit = “1”)



Measuring conditions ($\overline{CS_0}$–$\overline{CS_4}$, A_0/D_0–A_{15}/D_{15}, A_{16}, A_{17}, ALE, $\overline{WEL}$, $\overline{WEH}$, $\overline{RDE}$, $\overline{RSMP}$)

- V_{CC} = 2.7–5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

Measuring conditions (Ports P4–P8)

- V_{CC} = 2.7–5.5 V
- Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

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18.4.9 Memory expansion mode and Microprocessor mode : with wait 1

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(D–RDE)}$	Data input setup time	80		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

2: When the main clock division selection bit = "1," the minimum value of t_c = 166 ns.

3: When the main clock division selection bit = "1," values of $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	Fig. 18.4.1	$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 63$	20		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 63$	20		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 63$	20		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 73$	10		ns
$t_{h(ALE–A)}$	Address hold time			9		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time			4		ns
$t_{d(WE–DQ)}$	Data output delay time				90	ns
$t_{h(WE–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{w(WE)}$	$\overline{WEL}$, $\overline{WEH}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 35$	298		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				10	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 30$	53		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 38$	295		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 58$	25		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time			0	30	ns
$t_{d(\phi 1–HLDA)}$	$\overline{HLDA}$ output delay time				120	ns

Note: f(f_2) represents the clock f_2 frequency.
For the relationship with the main clock and sub clock, refer to **Table 14.3.1** in part 1.

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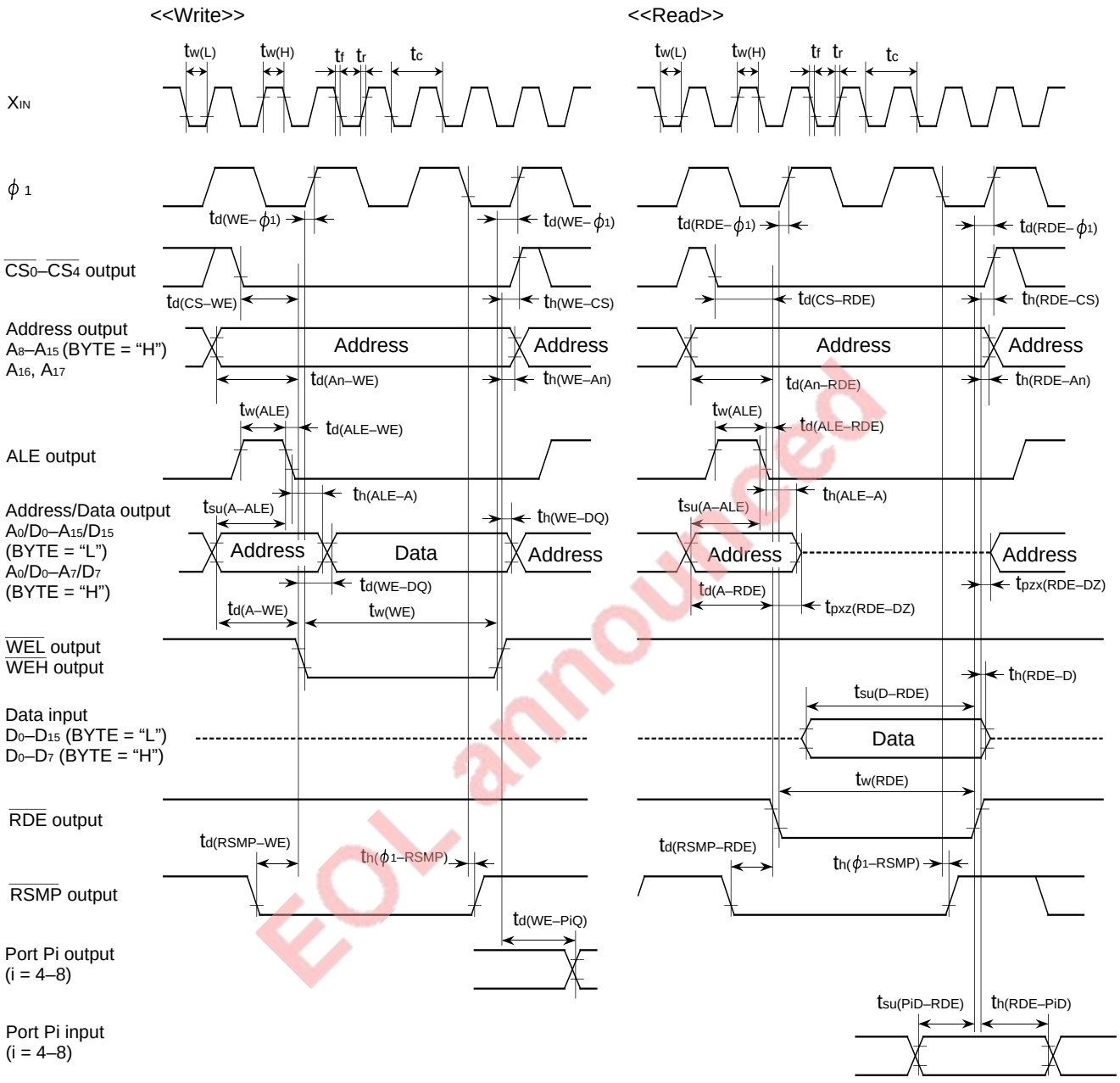
18.4 Electrical characteristics

Memory expansion mode and Microprocessor mode :

When external memory area is accessed with wait 1 (Wait bit = “0” and Wait selection bit = “1”)



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Measuring conditions ($\overline{CS_0}$–$\overline{CS_4}$, A_0/D_0–A_{15}/D_{15}, A_{16}, A_{17}, ALE, $\overline{WEL}$, $\overline{WEH}$, $\overline{RDE}$, $\overline{RSMP}$)

- V_{CC} = 2.7–5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

Measuring conditions (Ports P4–P8)

- V_{CC} = 2.7–5.5 V
- Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

18.4.10 Memory expansion mode and Microprocessor mode : with wait 0

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(D–RDE)}$	Data input setup time	80		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.
2: When the main clock division selection bit = "1," the minimum value of t_c = 166 ns.
3: When the main clock division selection bit = "1," values of $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ must be set to values from 0.45 through 0.55.

Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Conditions	Data formula (Min.)	Limits		Unit
				Min.	Max.	
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	Fig. 18.4.1	$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 68$	182		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time		$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 68$	182		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time		$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 88$	162		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{w(ALE)}$	ALE pulse width		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 43$	123		ns
$t_{su(A–ALE)}$	Address output setup time		$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 73$	93		ns
$t_{h(ALE–A)}$	Address hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{d(WE–DQ)}$	Data output delay time				90	ns
$t_{h(WE–DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 43$	40		ns
$t_{w(WE)}$	$\overline{WEL}$, $\overline{WEH}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 35$	298		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				10	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 30$	53		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width		$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 38$	295		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 58$	25		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	$\phi 1$ output delay time			0	30	ns
$t_{h(\phi 1–HLDA)}$	$\overline{HLDA}$ output delay time				120	ns

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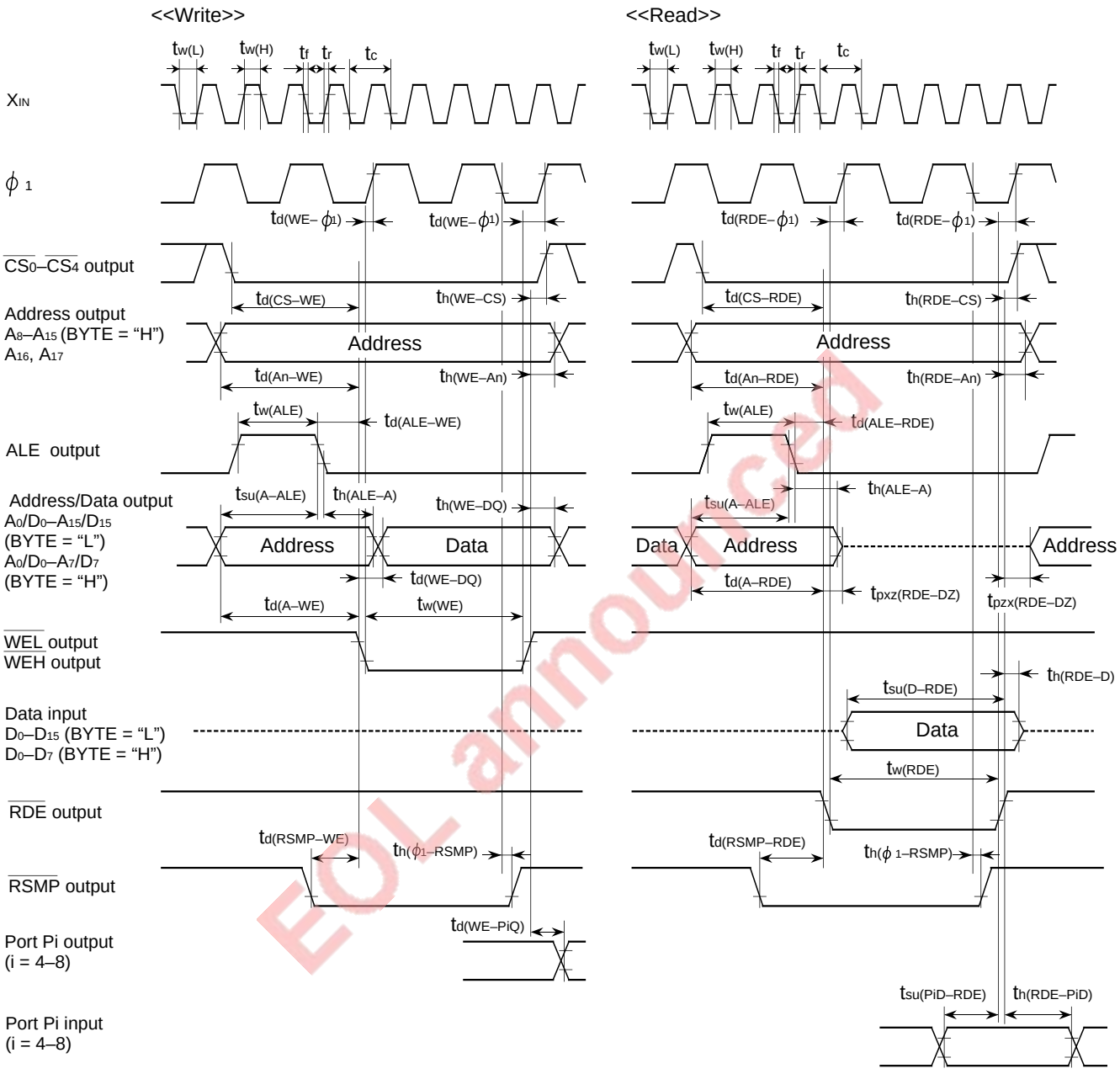
18.4 Electrical characteristics

Memory expansion mode and Microprocessor mode :

When external memory area is accessed with wait 0 (Wait bit = “0” and Wait selection bit = “0”)



Measuring conditions ($\overline{CS_0}$–$\overline{CS_4}$, A_0/D_0–A_{15}/D_{15}, A_{16}, A_{17}, ALE, $\overline{WEL}$, $\overline{WEH}$, $\overline{RDE}$, $\overline{RSMP}$)

- V_{CC} = 2.7–5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

Measuring conditions (Ports P4–P8)

- V_{CC} = 2.7–5.5 V
- Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

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18.6 Applications

Some application examples of connecting external memorys for the low voltage version are described below. For the basic description of the memory expansion, refer to chapter "**17. APPLICATIONS.**"
Applications shown here are just examples. Modify the desired application to suit the user's need and make sufficient evaluations before actually using it.

18.6.1 Memory expansion

The following items of the 7735 Group's low voltage version are the same as section "**17.1 Memory expansion**" **in part 1,** but a part of the caluculation way and constants for each parameter is different:
•Memory expansion model
•Caluculation way for address access time of external memory
•Bus timing
•Memory expansion way

① **Address access time of external memory $t_{a(AD)}$**

$t_{a(AD)} = t_{d(A\text{-}RDE)} + t_{w(RDE)} - t_{su(D\text{-}RDE)}$ – (address decode time*1 + address latch delay time*2)

address decode time*1 : time necessary for validating a chip select signal after an address is decoded
address latch delay time*2 : time necessary for latching an address

②**Data setup time of external memory for writing data $t_{su(D)}$**

$t_{su(D)} = t_{w(WE)} - t_{d(WE\text{–}DQ)}$

Table 18.6.1 lists the caluculation formulas and constants for each parameter of the low voltage version. Figure 18.6.1 shows the relationship between $t_{a(AD)}$ and $2 \bullet f(f_2)$. Figure 18.6.2 shows the relationship between $t_{su(D)}$ and $2 \bullet f(f_2)$.

Table 18.6.1 Caluculation formulas and constants for each parameter (Unit : ns)

Software wait	No wait	Wait 1	Wait 0
Wait bit	1	0	0
Wait selection bit	0 or 1	1	0
$t_{d(A\text{-}RDE)}$	$\frac{1 \times 10^9}{2 \bullet f(f_2)} - 63$		$\frac{3 \times 10^9}{2 \bullet f(f_2)} - 88$
$t_{w(RDE)}$	$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 38$	$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 38$	
$t_{w(WE)}$	$\frac{2 \times 10^9}{2 \bullet f(f_2)} - 35$	$\frac{4 \times 10^9}{2 \bullet f(f_2)} - 35$	
$t_{su(D\text{-}RDE)}$	80		
$t_{d(WE\text{-}DQ)}$	90		

Wait bit : Bit 2 at address $5E_{16}$
Wait selection bit : Bit 0 at address $5F_{16}$
Note: This is applied to the case where the system clock selection bit (bit 3 at address $6C_{16}$) = "0."

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18.6 Applications

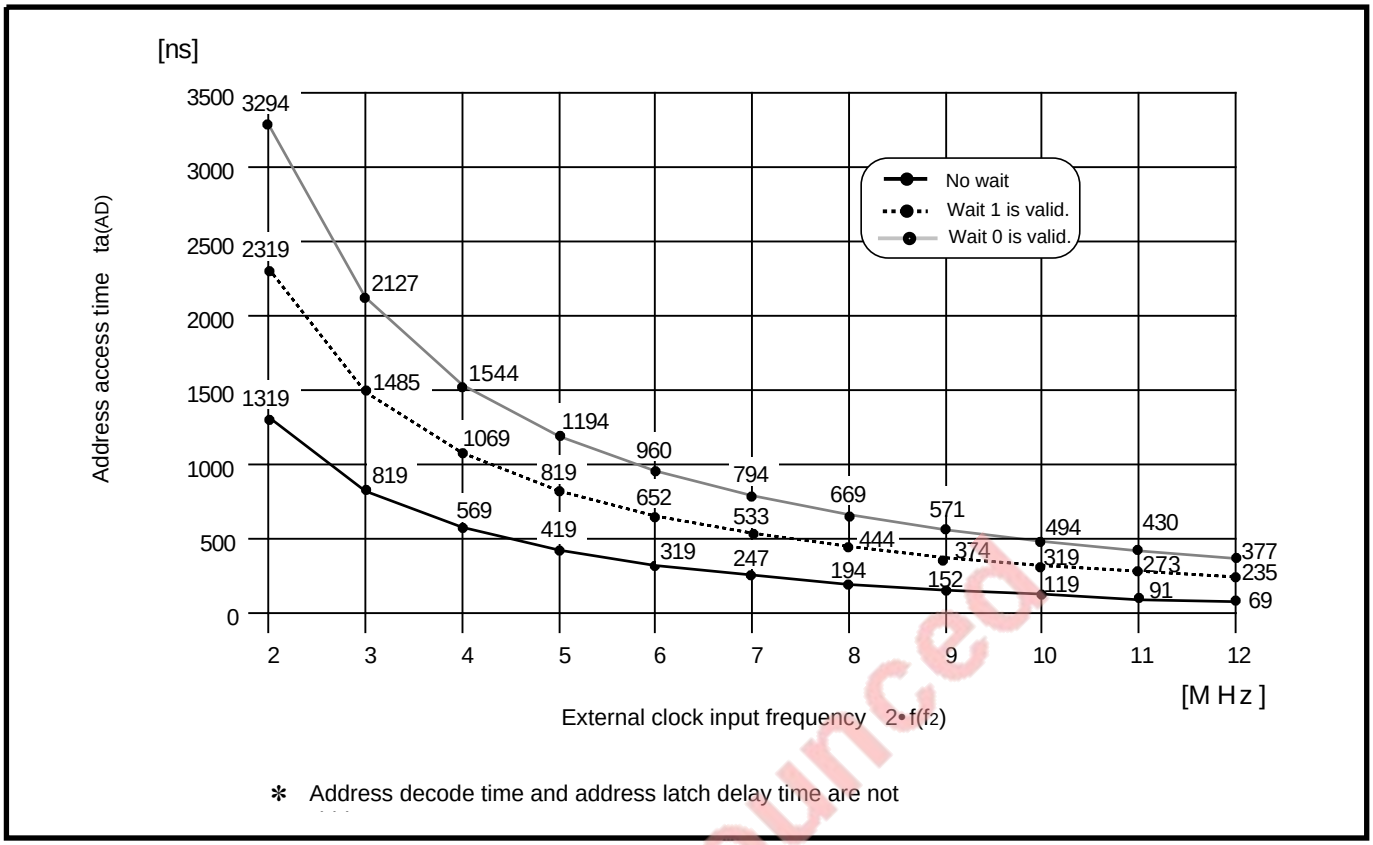


Fig. 18.6.1 Relationship between $t_{a(AD)}$ and 2•f(f2)

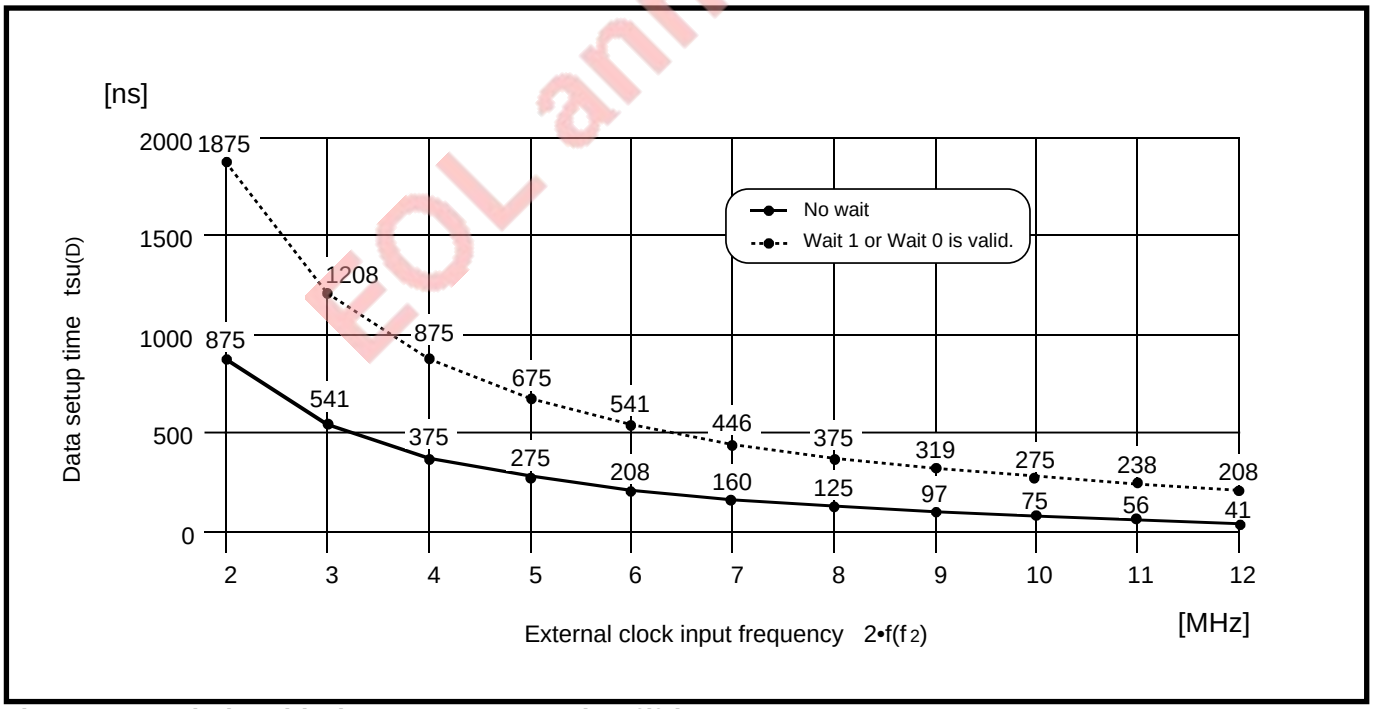


Fig. 18.6.2 Relationship between $t_{su(D)}$ and 2•f(f2)

EOL announced

18.6.2 Memory expansion example

Figure 18.6.3 shows a memory expansion example and Figure 18.6.4 shows the corresponding timing diagram.

In this example, an Atmel company's EPROM (AT27LV256R) is used as the external ROM.

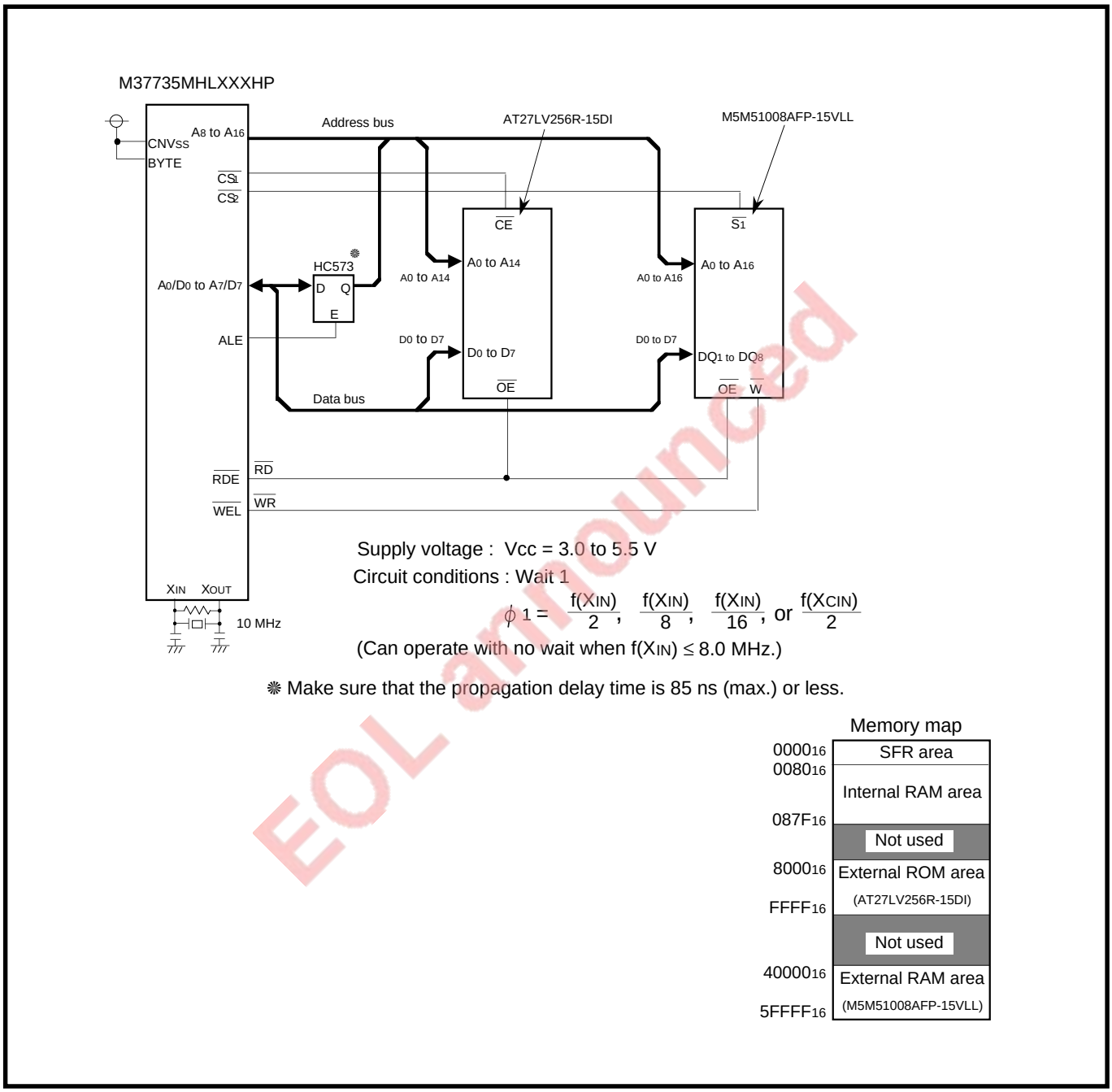
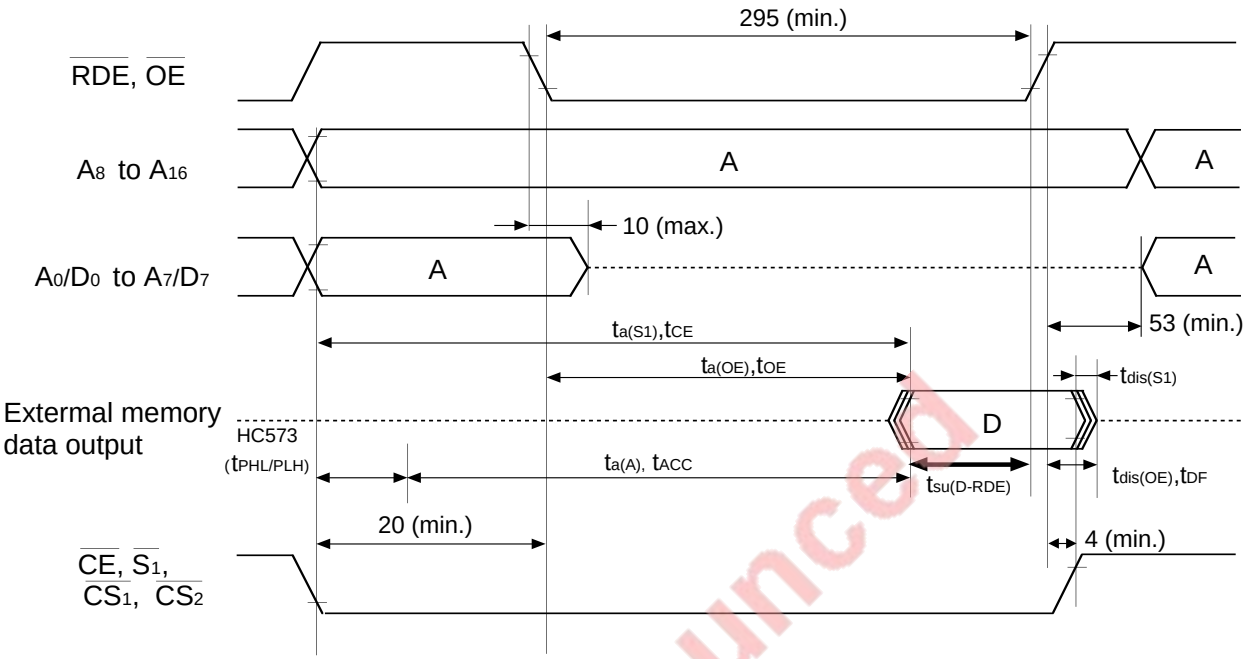


Fig. 18.6.3 Memory expansion example

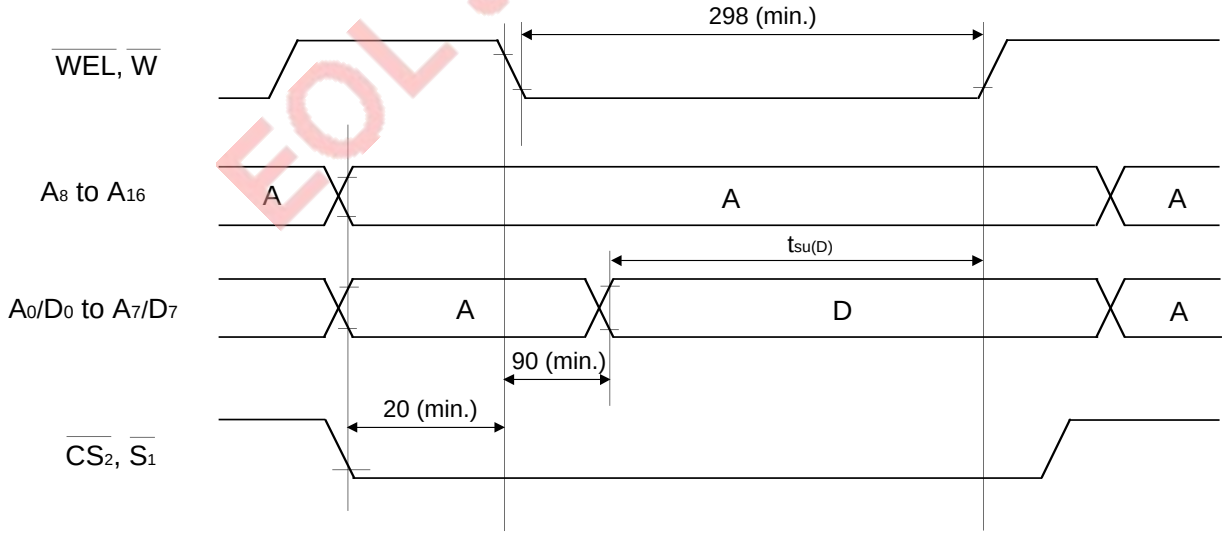
EOL announced

18.6 Applications

● At reading



●At writing



(Unit : ns)

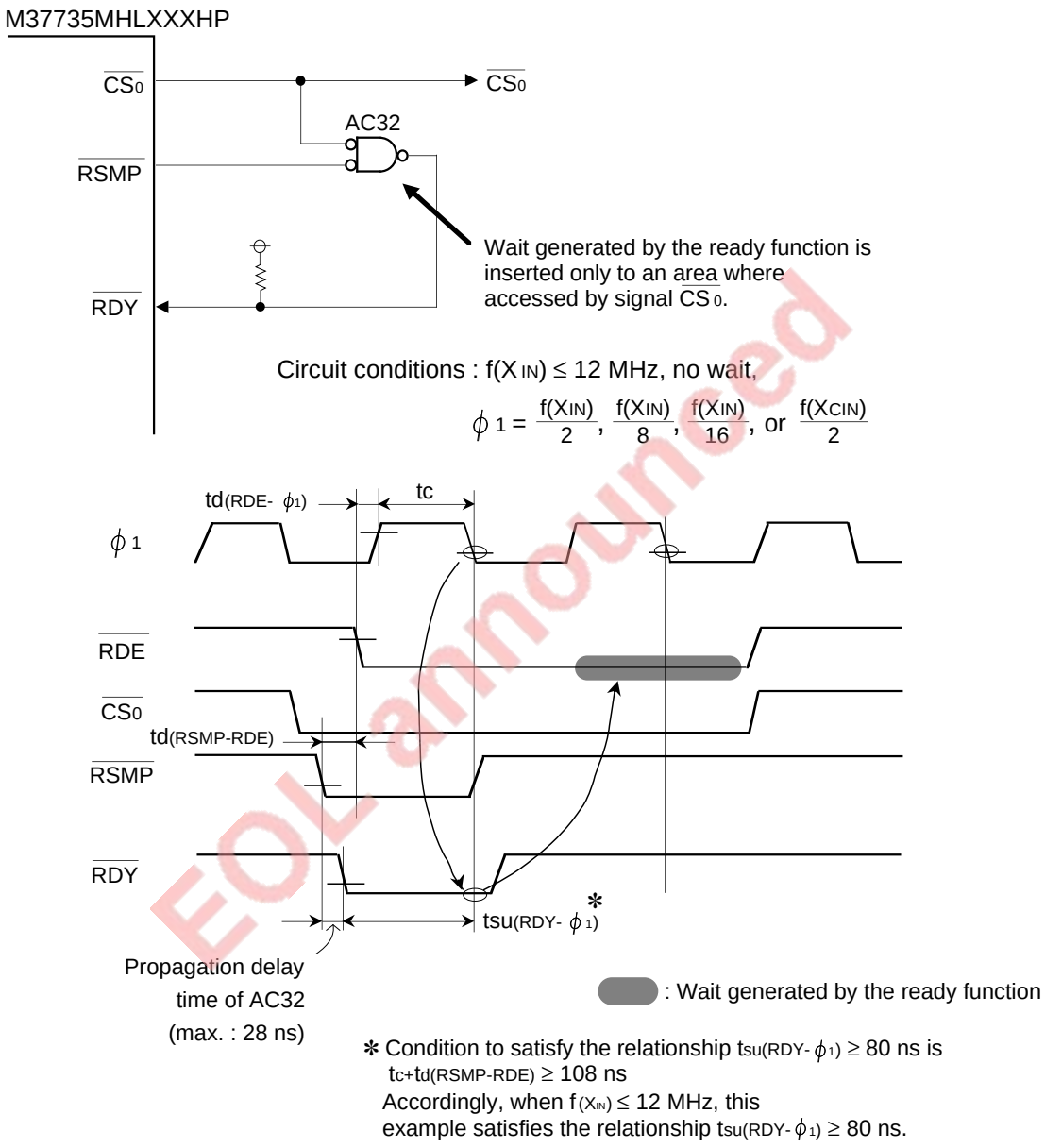
Fig. 18.6.4 Timing diagram

EOL announced

18.6.3 Ready generating circuit example

When validating “wait” only for a certain area (for example, ROM area) in Figure 18.6.3, use the ready function.

Figure 18.6.5 shows a ready generating circuit example.



EOL announced

Fig. 18.6.5 Ready generating circuit example

MEMO

EOL announced

CHAPTER 19

BUILT-IN PROM VERSION

19.1 EPROM mode
19.2 Usage precaution

EOL announced

BUILT-IN PROM VERSION

19.1 EPROM mode

Concerning chapter “19. BUILT-IN PROM VERSION,” the 7735 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

- **“19.1 EPROM mode”**

The following section of the 7735 Group is the same as that of the 7733 Group. Therefore, for this section, refer to part 1:

- **“19.2 Usage precaution” (page 19-10 in part 1)**

19.1 EPROM mode

Concerning section “19.1 EPROM mode,” the 7735 Group differs from the 7733 Group in the following:

- **Figures 19.1.1 and 19.1.2**
- **Bit 3 of the oscillation circuit control register 1 (address $6F_{16}$) is “1” at reset. After reset, this bit must be cleared to “0” in the single-chip mode. This writing must be performed with the procedure shown in Figure 14.3.4.**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“19.1 EPROM mode” (page 19-3 in part 1)**

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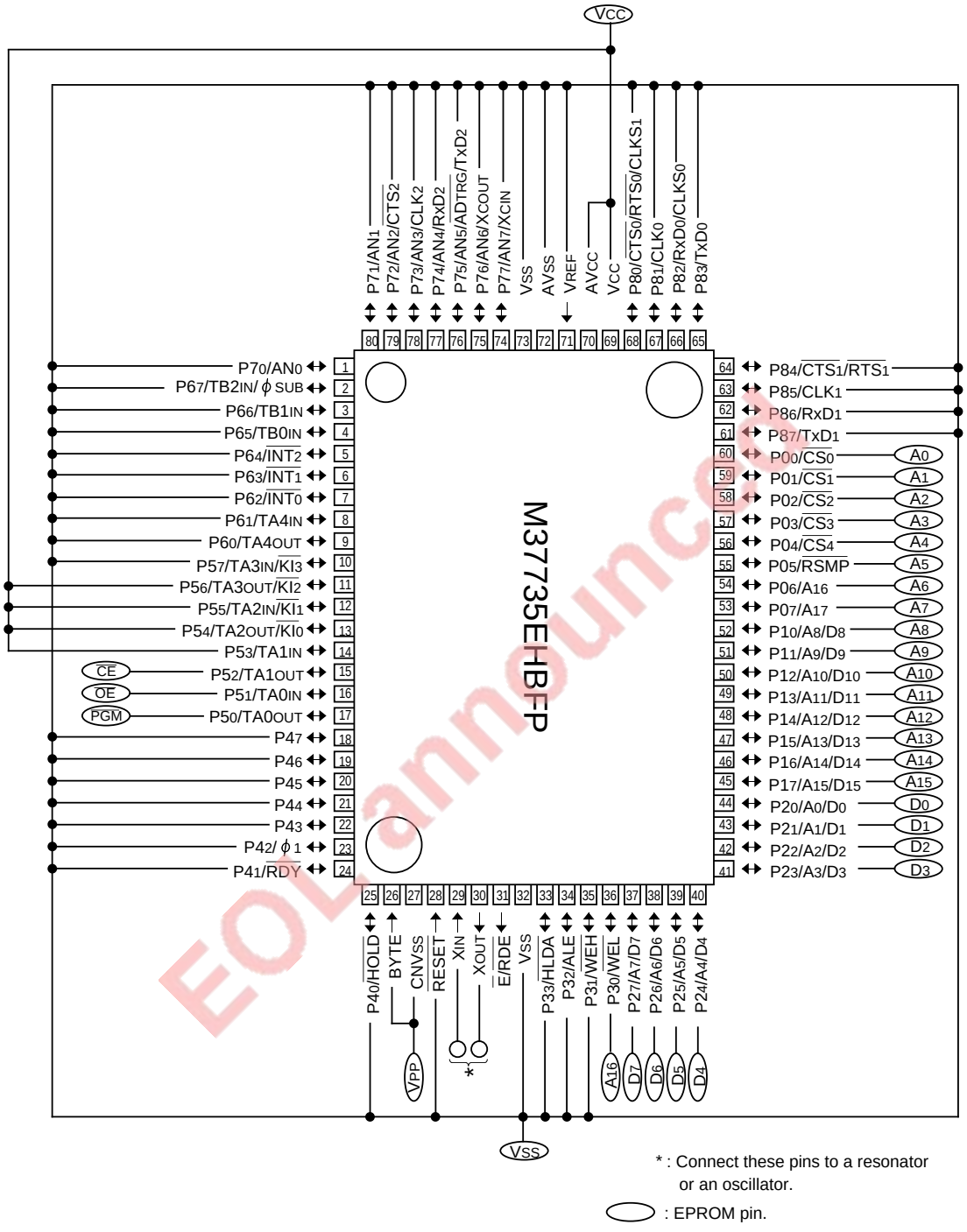


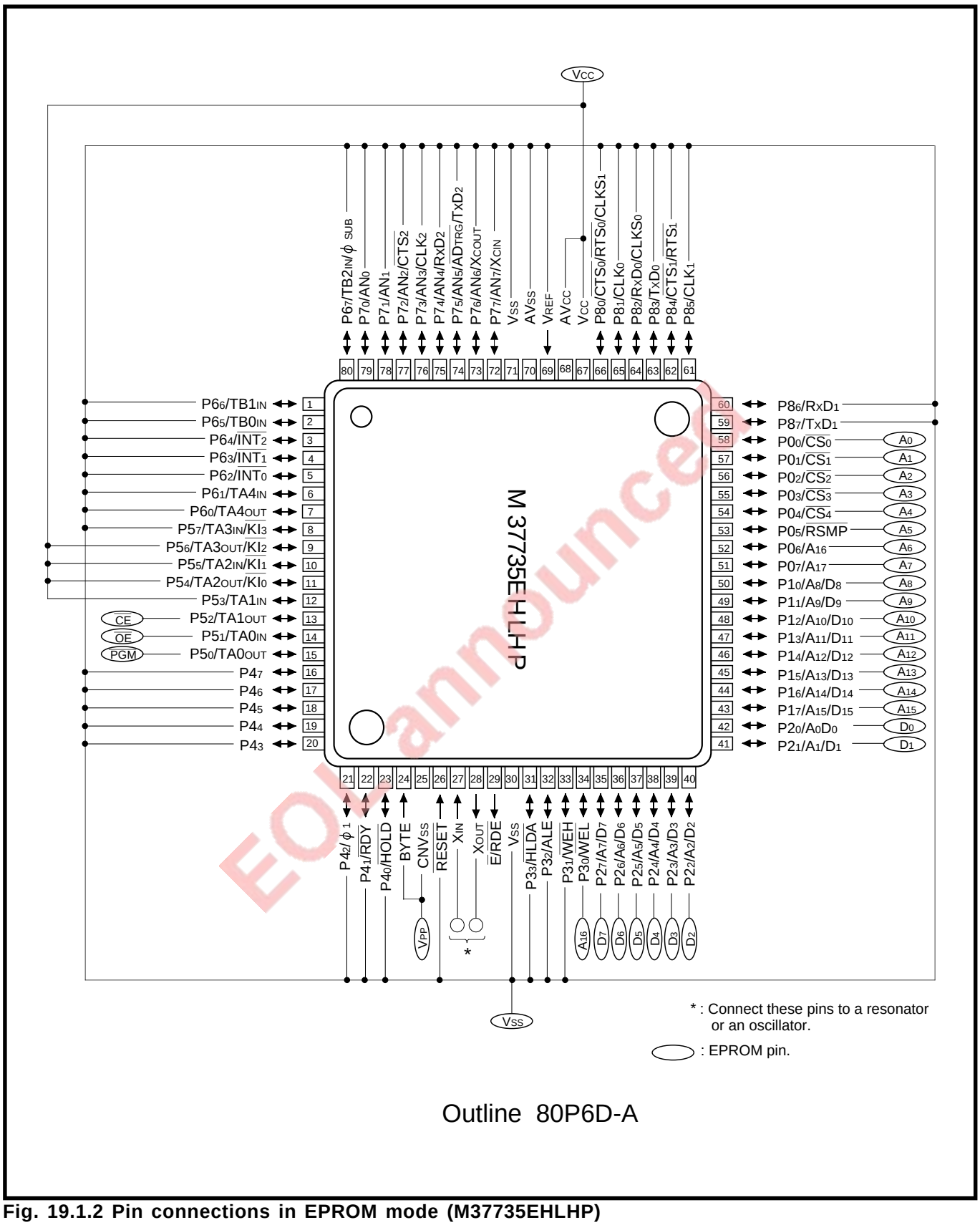
Outline 80P6N-A

Fig. 19.1.1 Pin connections in EPROM mode (M37735EHBFP)

EOL announcement

BUILT-IN PROM VERSION

19.1 EPROM mode



Outline 80P6D-A

Fig. 19.1.2 Pin connections in EPROM mode (M37735EHLHP)

CHAPTER 20

EXTERNAL ROM VERSION

20.1 Performance overview
20.2 Pin configuration
20.3 Pin description
20.4 Block description
20.5 Memory allocation
20.6 Processor modes
20.7 Timer A
20.8 Reset
20.9 Electrical characteristics
20.10 Low voltage version

EOL announced

EXTERNAL ROM VERSION

The external ROM version can operate only in the microprocessor mode.
Functions of the external ROM version differ from those of the mask ROM version in the following. Therefore, only the differences are described in this chapter:

•Memory allocation
•Operation is available only in the microprocessor mode
•ROM area change function is not available.
•Timer A has the pulse output port mode.
•Power source current and Current consumption

For the other functions, refer to the following:

- Chapters **“4. INTERRUPTS”** to **“9. A-D CONVERTER” in part 1**
- Chapter **“2. CENTRAL PROCESSING UNIT (CPU)” in part 2**
- Chapter **“3. PROGRAMMABLE I/O PORT” in part 2**
- Chapters **“10. WATCHDOG TIMER”** to **“17. APPLICATIONS” in part 2**

❋ For product expansion information of the 7735 Group, contact the appropriate office, as listed in “CONTACT ADDRESSES FOR FURTHER INFORMATION.”

EOL announced

20.1 Performance overview

Performance overview of the external ROM version differs from that of the mask ROM version in the following: memory size and current consumption. For the other items, refer to section **"1.1 Performance overview" in part 2.**

Table 20.1.1 lists the M37735S4BFP's performance overview.

Table 20.1.1 M37735S4BFP's performance overview

Items		Performance
Memory size	RAM	2048 bytes
Current consumption		57 mW (When f(XIN) = 25-MHz external square wave input, Vcc = 5 V, and the main clock is the system clock, Typ.)
		300 μW (When f(XCIN) = 32 kHz, Vcc = 5 V, the sub clock is the system clock, and the main clock is stopped, Typ.)

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20.2 Pin configuration

Figure 20.2.1 shows the M37735S4BFP pin configuration.

Note: For the low voltage version, refer to section **"20.10 Low voltage version."**

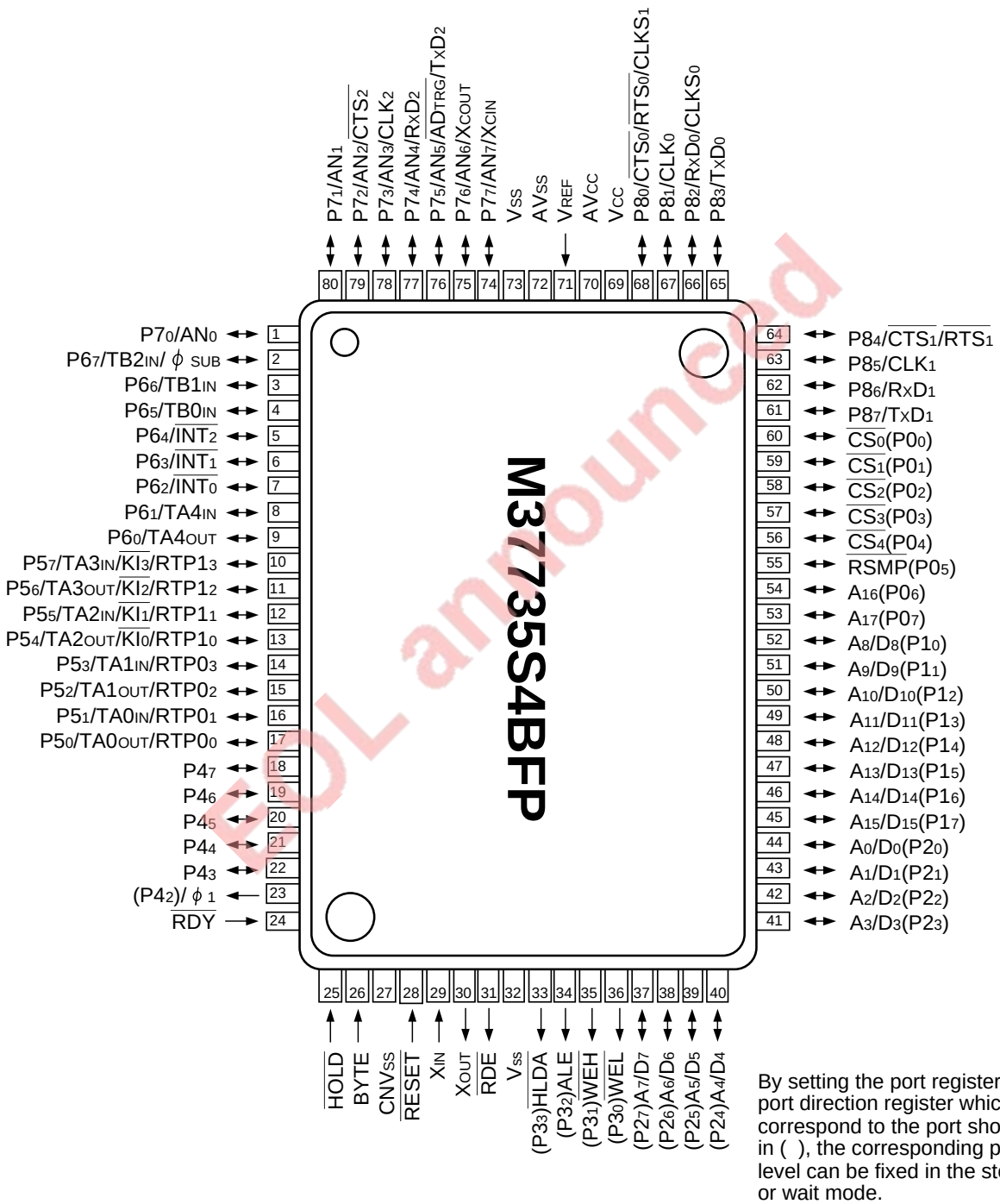

Fig. 20.2.1 M37735S4BFP pin configuration (Top view)

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20.3 Pin description

Tables 20.3.1 and 20.3.2 list the pin description.

Table 20.3.1 Pin description (1)

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source input		To pin Vcc, apply 5 V±10% (When the main clock is the system clock) or 2.7 V to 5.5 V (When the sub-clock is the system clock). To pin Vss, apply 0 V.
CNVss	CNVss	Input	Connect to pin Vcc.
$\overline{\text{RESET}}$	Reset input	Input	The microcomputer is reset when "L" level is input to this pin.
X_{IN}	Clock input	Input	Pins X_{IN} and X_{OUT} are the I/O pins of the clock generating circuit, respectively. Connect these pins via a ceramic resonator or a quartz-crystal oscillator. When an external clock is used, the clock should be input to pin X_{IN}, and pin X_{OUT} should be left open.
X_{OUT}	Clock output	Output	
$\overline{\text{RDE}}$	Read enable output	Output	This pin outputs read enable signal $\overline{\text{RDE}}$. $\overline{\text{RDE}}$'s level is "L" in the data read period of the read cycle.
BYTE	External data bus width selection input	Input	Input level to this pin determines whether the external data bus has a 16-bit width or an 8-bit width. A 16-bit width is selected when the level is "L," and an 8-bit width is selected when the level is "H."
AVcc	Analog power source input		Power source input for the A-D converter. Connect to pin Vcc.
AVss			Power source input for the A-D converter. Connect to pin Vss.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
$\overline{\text{CS}}_0$ ($P0_0$)–$\overline{\text{CS}}_4$ ($P0_4$), $\overline{\text{RSMP}}$ ($P0_5$), A_{16} ($P0_6$), A_{17} ($P0_7$)	Chip select output, Ready sampling output, Address (high-order) output	Output	These pins respectively output signals $\overline{\text{CS}}_0$–$\overline{\text{CS}}_4$, $\overline{\text{RSMP}}$, and high-order 2 bits (A_{16}, A_{17}) of address. ● Signals $\overline{\text{CS}}_0$–$\overline{\text{CS}}_4$ These signals are the chip-select signals. When the microcomputer accesses a certain area, the corresponding pin outputs "L" level. (Refer to **Figure 12.1.3.**) ● Signal $\overline{\text{RSMP}}$ This signal is the ready sampling signal and is used to generate signal $\overline{\text{RDY}}$ for accessing the external memory area.
A_8/D_8 ($P1_0$) – A_{15}/D_{15} ($P1_7$)	Address (middle-order) output/Data I/O	I/O	● When the external data bus width = 8 bits (Pin BYTE is at "H" level) Address's middle-order 8 bits (A_8–A_{15}) are output. ● When the external bus width = 16 bits (Pin BYTE pin is at "L" level) Input/Output of data (D_8–D_{15}) and output of address's middle-order 8 bits (A_8–A_{15}) are performed with the time sharing system.

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EXTERNAL ROM VERSION

20.3 Pin description

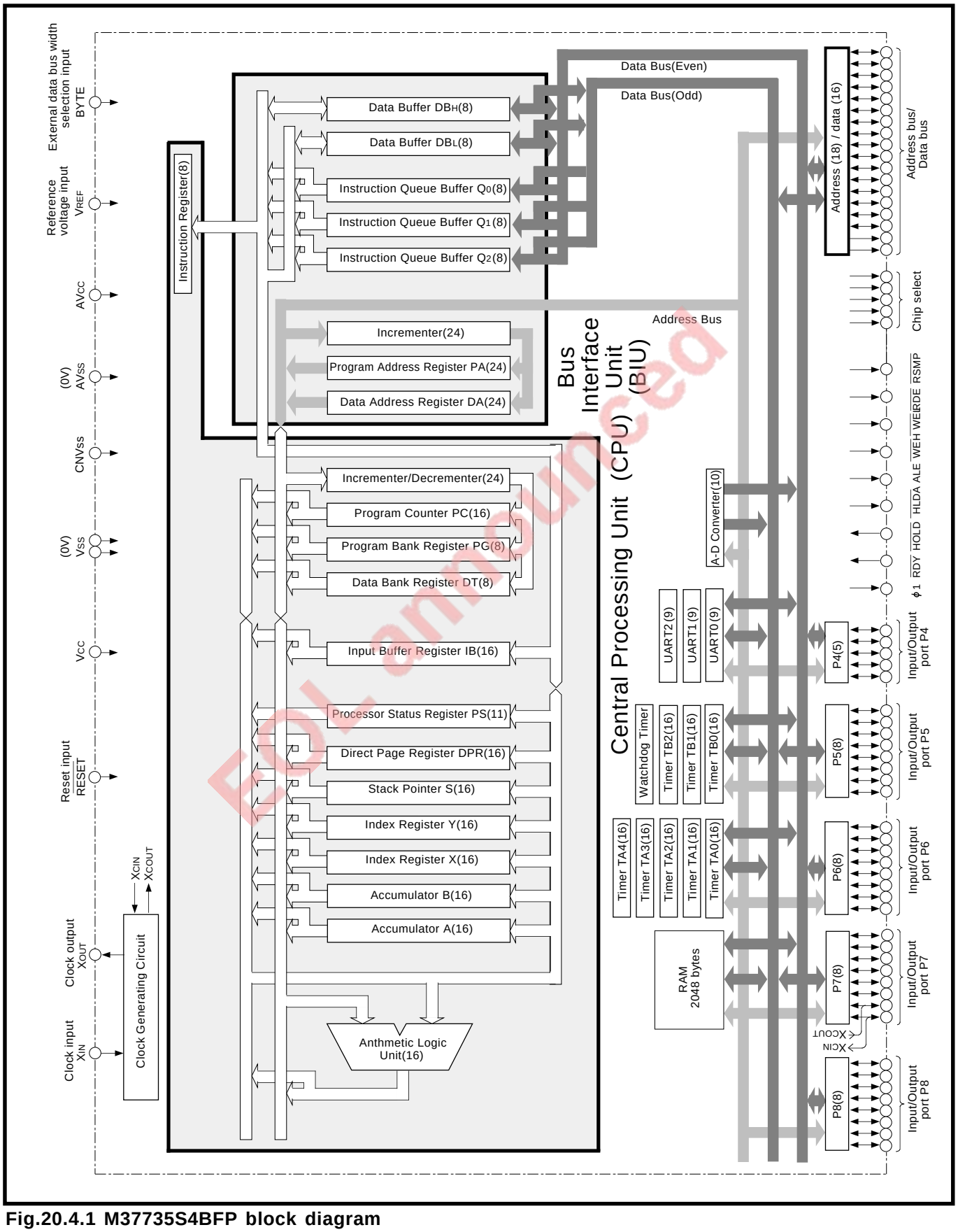
Table 20.3.2 Pin description (2)

Pin	Name	Input/Output	Functions
A_0/D_0 ($P2_0$) –A_7/D_7 ($P2_7$)	Address (low-order) output/Data (low-order) I/O	I/O	Input/Output of data (D_0–D_7) and output of address's low-order 8 bits (A_0–A_7) are performed with the time sharing system.
$\overline{WEL}$ ($P3_0$), $\overline{WEH}$ ($P3_1$), ALE ($P3_2$), $\overline{HLDA}$ ($P3_3$)	Write enable low output, Write enable high output, Address latch enable output, Hold acknowledge output	Output	These pins respectively output signals $\overline{WEL}$, $\overline{WEH}$, ALE, and $\overline{HLDA}$. ● Signals $\overline{WEL}$, $\overline{WEH}$ Signal $\overline{WEL}$ is the write enable low signal. Signal $\overline{WEH}$ is the write enable high signal. These signals' levels are "L" in the data write period of the write cycle. The operations of these signals depend on the level of pin BYTE. (Refer to **Table 12.1.1.**) ● Signal ALE This signal is used to separate the multiplexed signal which consists of an address and data to the address and data. ● Signal $\overline{HLDA}$ This signal informs the external whether this microcomputer enters the Hold state or not. In Hold state, pin $\overline{HLDA}$ outputs "L" level.
$\overline{HOLD}$, $\overline{RDY}$, ϕ_1($P4_2$),	Hold request input, Ready input, Clock output,	Input Input Output	The microcomputer is in Hold state while pin $\overline{HOLD}$'s input level is "L" and is in Ready state while pin $\overline{RDY}$'s input level is "L." The clock ϕ_1 output can be stopped by software. (Refer to chapter **"14. CLOCK GENERATING CIRCUIT."**)
$P4_3$–$P4_7$	I/O port P4	I/O	$P4_3$–$P4_7$ function as I/O ports with the same functions as port P5.
$P5_0$–$P5_7$	I/O port P5	I/O	P5 is a CMOS 8-bit I/O port and has an I/O direction register. Each pin can be programmed for input or output. It can be programmed as I/O pins for timers A0–A3, input pins ($\overline{KI_0}$–$\overline{KI_3}$) for the key input interrupt and output pins (RTP00–RTP13) for the pulse output.
$P6_0$–$P6_7$	I/O port P6	I/O	P6 is an 8-bit I/O port with the same function as port P5 and can be programmed as I/O pins for timer A4, external interrupt input pins, and input pins for timers B0–B2. $P6_7$ also functions as an output pin for the sub clock (ϕ_{SUB}).
$P7_0$–$P7_7$	I/O port P7	I/O	P7 is an 8-bit I/O port with the same function as port P5 and can be programmed as analog input pins for the A-D converter. $P7_6$ and $P7_7$ can be programmed as I/O pins (X_{COUT}, X_{CIN}) for the sub-clock (32 kHz) oscillation circuit. When using $P7_6$ and $P7_7$ as pins X_{COUT} and X_{CIN}, connect a quartz-crystal oscillator between them. $P7_2$–$P7_5$ also function as UART2's I/O pins.
$P8_0$–$P8_7$	I/O port P8	I/O	P8 is an 8-bit I/O port with the same function as port P5 and can be programmed as serial I/O's I/O pins.

EOL announced

20.4 Block description

Figure 20.4.1 shows the M37735S4BFP block diagram.



EOL announced

Fig.20.4.1 M37735S4BFP block diagram

20.5 Memory allocation

The internal area's memory allocation is described below. For details, refer to section **"2.4 Memory allocation" in part 1.** For the external area, refer to section **"20.6 Processor modes."** Figure 20.5.1 shows the M37735S4BFP's memory map and Figure 20.5.2 shows the SFR area's memory map.

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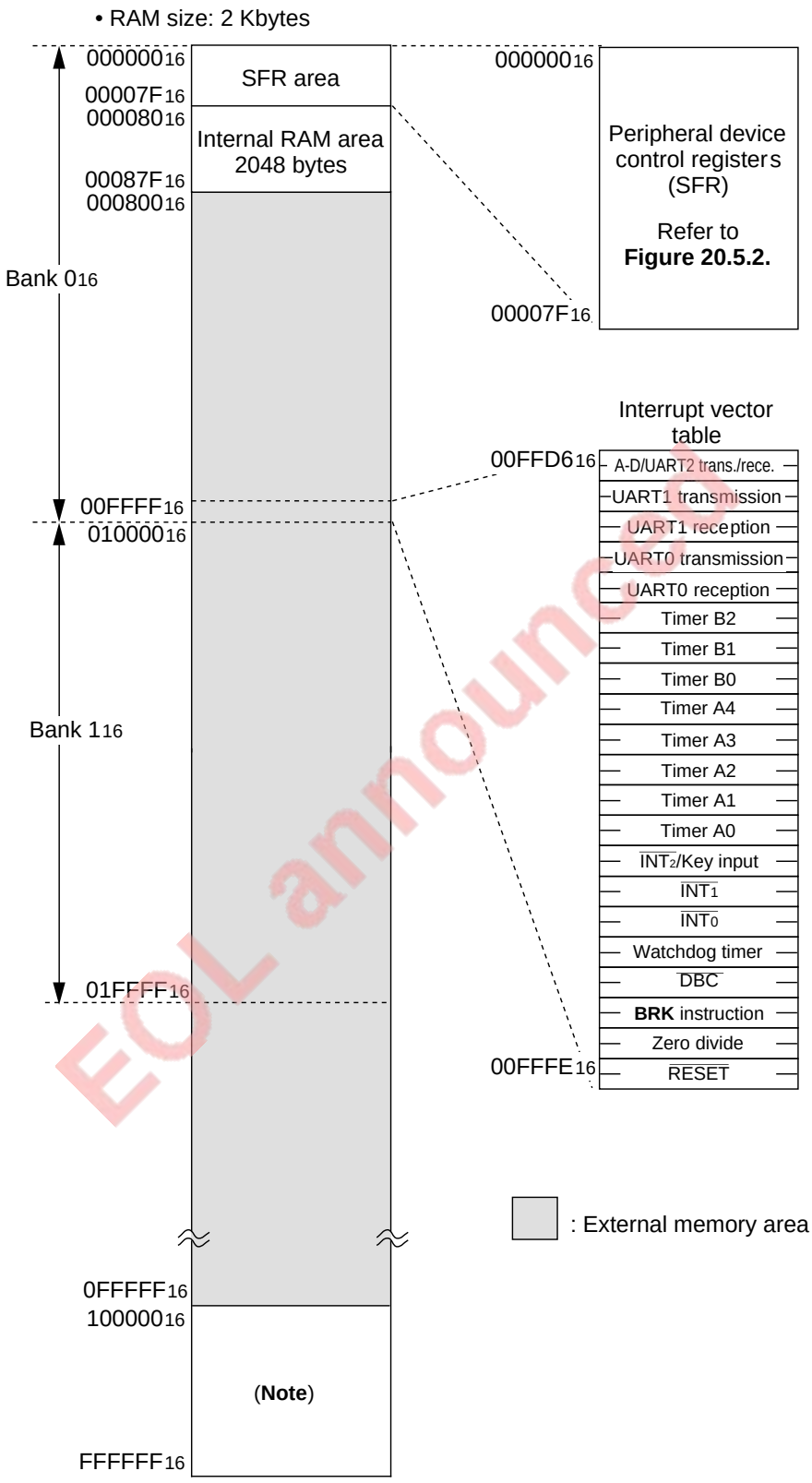


Note: Banks 10_{16} to FF_{16} cannot be accessed.

❋ For the 7735 Group's microcomputers other than the M37735S4BFP, refer to section **"Appendix 1. 7735 Group memory allocation."**

Fig. 20.5.1 M37735S4BFP's memory map

EOL announced

20.5 Memory allocation

Address (Hexadecimal notation)	
000000	
000001	
000002	Port P0 register (**Note 3**)
000003	Port P1 register (**Note 3**)
000004	Port P0 direction register (**Note 3**)
000005	Port P1 direction register (**Note 3**)
000006	Port P2 register (**Note 3**)
000007	Port P3 register (**Note 3**)
000008	Port P2 direction register (**Note 3**)
000009	Port P3 direction register (**Note 3**)
00000A	Port P4 register (**Note 3**)
00000B	Port P5 register
00000C	Port P4 direction register (**Note 3**)
00000D	Port P5 direction register
00000E	Port P6 register
00000F	Port P7 register
000010	Port P6 direction register
000011	Port P7 direction register
000012	Port P8 register
000013	
000014	Port P8 direction register
000015	
000016	
000017	
000018	
000019	
00001A	
00001B	
00001C	Pulse output data register 1 (**Note 1**)
00001D	Pulse output data register 0 (**Note 1**)
00001E	A-D control register 0
00001F	A-D control register 1
000020 000021	A-D register 0
000022 000023	A-D register 1
000024 000025	A-D register 2
000026 000027	A-D register 3
000028 000029	A-D register 4
00002A 00002B	A-D register 5
00002C 00002D	A-D register 6
00002E 00002F	A-D register 7
000030	UART 0 transmit/receive mode register
000031	UART 0 baud rate register (BRG0)
000032 000033	UART 0 transmission buffer register
000034	UART 0 transmit/receive control register 0
000035	UART 0 transmit/receive control register 1
000036 000037	UART 0 receive buffer register
000038	UART 1 transmit/receive mode register
000039	UART 1 baud rate register (BRG1)
00003A 00003B	UART 1 transmission buffer register
00003C	UART 1 transmit/receive control register 0
00003D	UART 1 transmit/receive control register 1
00003E 00003F	UART 1 receive buffer register

Address (Hexadecimal notation)	
000040	Count start flag
000041	
000042	One-shot start flag
000043	
000044	Up-down flag
000045	
000046 000047	Timer A0 register
000048 000049	Timer A1 register
00004A 00004B	Timer A2 register
00004C 00004D	Timer A3 register
00004E 00004F	Timer A4 register
000050 000051	Timer B0 register
000052 000053	Timer B1 register
000054 000055	Timer B2 register
000056	Timer A0 mode register
000057	Timer A1 mode register
000058	Timer A2 mode register
000059	Timer A3 mode register
00005A	Timer A4 mode register
00005B	Timer B0 mode register
00005C	Timer B1 mode register
00005D	Timer B2 mode register
00005E	Processor mode register 0
00005F	Processor mode register 1
000060	Watchdog timer register
000061	Watchdog timer frequency selection flag
000062	Waveform output mode register (**Note 1**)
000063	Reserved area **(Notes 1, 2)**
000064	UART2 transmit/receive mode register
000065	UART2 baud rate register (BRG2)
000066 000067	UART2 transmission buffer register
000068	UART2 transmit/receive control register 0
000069	UART2 transmit/receive control register 1
00006A 00006B	UART2 receive buffer register
00006C	Oscillation circuit control register 0
00006D	Port function control register
00006E	Serial transmit control register
00006F	Oscillation circuit control register 1
000070	A-D/UART2 trans./rece. interrupt control register
000071	UART 0 transmission interrupt control register
000072	UART 0 receive interrupt control register
000073	UART 1 transmission interrupt control register
000074	UART 1 receive interrupt control register
000075	Timer A0 interrupt control register
000076	Timer A1 interrupt control register
000077	Timer A2 interrupt control register
000078	Timer A3 interrupt control register
000079	Timer A4 interrupt control register
00007A	Timer B0 interrupt control register
00007B	Timer B1 interrupt control register
00007C	Timer B2 interrupt control register
00007D	$\overline{INT_0}$ interrupt control register
00007E	$\overline{INT_1}$ interrupt control register
00007F	$\overline{INT_2}$/Key input interrupt control register

Notes 1: Memory map of the M37735S4BFP differs from that of the M37735MHBXXXFP in addresses $1C_{16}$, $1D_{16}$, 62_{16}, and 63_{16}.
2: Writing to the reserved area is disabled.
3: These registers are used when outputting an arbitrary data in the stop or wait mode.

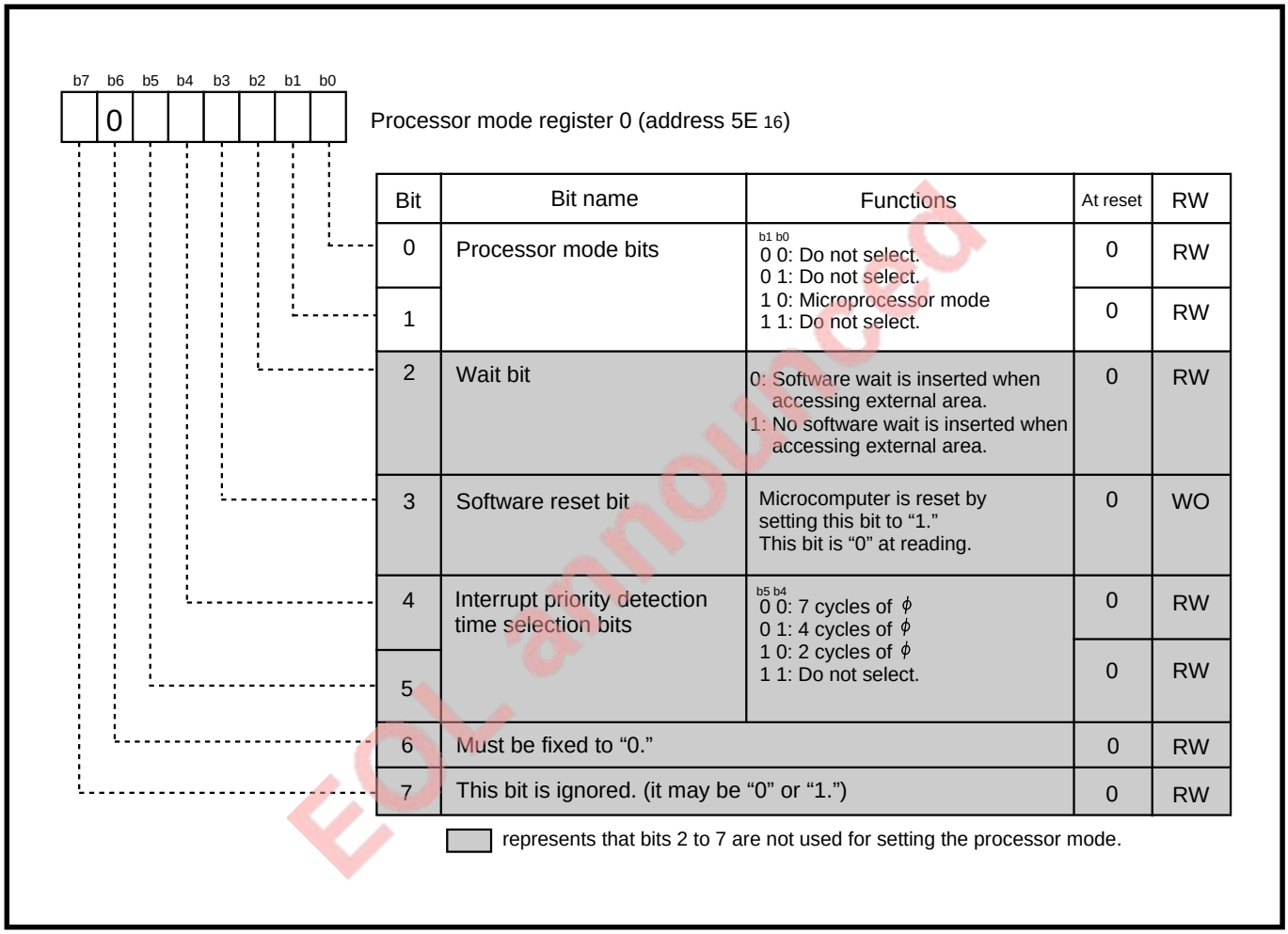
Fig. 20.5.2 SFR area's memory map

EOL announced

20.6 Processor modes

The M37735S4BFP can operate only in the microprocessor mode. For the processor mode, refer to the description of the microprocessor mode in section **"2.5 Processor modes" in part 1.**
Also, be sure to set as follows:
• Connect pin CNVss to Vcc.
• Fix the processor mode bit to "10_2."

Figure 20.6.1 shows the structure of the processor mode register 0.



Bit	Bit name	Functions	At reset	RW
0	Processor mode bits	b1 b0 0 0: Do not select. 0 1: Do not select. 1 0: Microprocessor mode 1 1: Do not select.	0	RW
1			0	RW
2	Wait bit	0: Software wait is inserted when accessing external area. 1: No software wait is inserted when accessing external area.	0	RW
3	Software reset bit	Microcomputer is reset by setting this bit to "1." This bit is "0" at reading.	0	WO
4	Interrupt priority detection time selection bits	b5 b4 0 0: 7 cycles of ϕ 0 1: 4 cycles of ϕ 1 0: 2 cycles of ϕ 1 1: Do not select.	0	RW
5			0	RW
6	Must be fixed to "0."		0	RW
7	This bit is ignored. (it may be "0" or "1.")		0	RW

represents that bits 2 to 7 are not used for setting the processor mode.

EOL announced

Fig. 20.6.1 Structure of processor mode register 0

20.7 Timer A

The timer A description of the M37735S4BFP is the same as that of the 7733 Group. For timer A description of the M37735S4BFP, refer to the following:

- **"6. TIMER A" (page 6-2 in part 1)**
- **"20.7 Timer A" (page 20-12 in part 1)**

20.8 Reset

The reset description of the M37735S4BFP differs from that of the mask ROM version in the state immediately after reset.

The state immediately after reset of the M37735S4BFP differs from that of the mask ROM version in the following addresses: addresses $1C_{16}$, $1D_{16}$, 62_{16} and 63_{16}.

Figures 20.8.1 and 20.8.2 show the state of SFR area and internal RAM area immediately after reset (1) and (4). Figure 20.8.1 corresponds to Figure 13.1.3 in part 1. Figure 20.8.2 corresponds to Figure 13.1.6 in part 1. For the other descriptions, refer to chapter **"13. RESET."**

For the pin state while pin $\overline{\text{RESET}}$ is at "L" level, refer to **Table 13.1.1**.

EOL announced

■SFR area (addresses 0_{16} to $7F_{16}$)

Abbreviations which represent access characteristics

RW : It is possible to read the bit state at reading. The written value becomes valid.
RO : It is possible to read the bit state at reading. The written value becomes invalid.
WO : The written value becomes valid. It is impossible to read the bit state.
▭ : Not implemented. It is impossible to read the bit state. The written value becomes invalid.

0 : "0" immediately after reset.
1 : "1" immediately after reset.
? : Undefined immediately after reset.

0 : Always "0" at reading
? : Always undefined at reading
0 : "0" immediately after reset. Must be fixed to "0."

Address	Register name	Access characteristics (b7 … b0)	State immediately after reset (b7 … b0)
0_{16}			?
1_{16}			?
2_{16}	Port P0 register	RW	?
3_{16}	Port P1 register	RW	?
4_{16}	Port P0 direction register	RW	00_{16}
5_{16}	Port P1 direction register	RW	00_{16}
6_{16}	Port P2 register	RW	?
7_{16}	Port P3 register	RW	0 0 0 0 ?
8_{16}	Port P2 direction register	RW	00_{16}
9_{16}	Port P3 direction register	RW	0 0 0 0 0 0 0 0
A_{16}	Port P4 register	RW	?
B_{16}	Port P5 register	RW	?
C_{16}	Port P4 direction register	RW	00_{16}
D_{16}	Port P5 direction register	RW	00_{16}
E_{16}	Port P6 register	RW	?
F_{16}	Port P7 register	RW	?
10_{16}	Port P6 direction register	RW	00_{16}
11_{16}	Port P7 direction register	RW	00_{16}
12_{16}	Port P8 register	RW	?
13_{16}			?
14_{16}	Port P8 direction register	RW	00_{16}
15_{16}			?
16_{16}			?
17_{16}			?
18_{16}			?
19_{16}			?
$1A_{16}$			?
$1B_{16}$			?
$1C_{16}$	Pulse output data register 1 ❋	WO	?
$1D_{16}$	Pulse output data register 0 ❋	WO	?
$1E_{16}$	A-D control register 0	RW	0 0 0 0 0 ? ? ?
$1F_{16}$	A-D control register 1	RW RW	? ? 0 0 0 ? 1 1

❋ The contents of addresses $1C_{16}$ and $1D_{16}$ of the M37735S4BFP differ from those of the M37735MHBXXXFP.

EOL announced

Fig. 20.8.1 State of SFR area and internal RAM area immediately after reset (1)

20.8 Reset

Address	Register name	Access characteristics b7							b0	State immediately after reset b7							b0
6016	Watchdog timer register	WO								? (✵1)							
6116	Watchdog timer frequency selection flag								RW	?							0
6216	Waveform output mode register ✵3	RW		RW			RW			0	?	0	0	0	?	0	0
6316	(Reserved area) ✵4									?							
6416	UART 2 transmit/receive mode register		RW							?	0	0	0	0	0	0	0
6516	UART 2 baud rate register (BRG2)	WO								?							
6616	UART 2 transmission buffer register	WO								?							
6716									WO	?							
6816	UART 2 transmit/receive control register 0					RO	RW			?				1	0	0	0
6916	UART 2 transmit/receive control register 1	RO					RW	RO	RW	0	0	0	0	0	0	1	0
6A16	UART 2 receive buffer register	RO								?							
6B16									RO	0	0	0	0	0	0	0	?
6C16	Oscillation circuit control register 0		RW(✵2)						RW	?	0	0	0	0	0	?	1
6D16	Port function control register	RW								0	0	0	0	0	0	0	0
6E16	Serial transmit control register			RW						?		0	0	?			
6F16	Oscillation circuit control register 1	WO			RW					0	?		0	0	0	0	0
7016	A-D / UART 2 trans./rece. interrupt control register					RW					?			0	0	0	0
7116	UART0 transmission interrupt control register					RW					?			0	0	0	0
7216	UART0 receive interrupt control register					RW					?			0	0	0	0
7316	UART1 transmission interrupt control register					RW					?			0	0	0	0
7416	UART1 receive interrupt control register					RW					?			0	0	0	0
7516	Timer A0 interrupt control register					RW					?			0	0	0	0
7616	Timer A1 interrupt control register					RW					?			0	0	0	0
7716	Timer A2 interrupt control register					RW					?			0	0	0	0
7816	Timer A3 interrupt control register					RW					?			0	0	0	0
7916	Timer A4 interrupt control register					RW					?			0	0	0	0
7A16	Timer B0 interrupt control register					RW					?			0	0	0	0
7B16	Timer B1 interrupt control register					RW					?			0	0	0	0
7C16	Timer B2 interrupt control register					RW					?			0	0	0	0
7D16	$\overline{INT_0}$ interrupt control register			RW						?	0	0	0	0	0	0	0
7E16	$\overline{INT_1}$ interrupt control register			RW						?	0	0	0	0	0	0	0
7F16	$\overline{INT_2}$/Key input interrupt control register			RW						?	0	0	0	0	0	0	0

✵**1** A value of "FFF16" is set to the watchdog timer. (Refer to Chapter **"10. WATCHDOG TIMER" in part 1.**)
✵**2** For access characteristics at address 6C16, also refer to **Figure 14.3.2 in part 1.**
✵**3** The contents of addresses 6216 and 6316 of the M37735S4BFP differ from those of the M37735MHBXXXFP.
✵**4** Do not wirte to address 6316.

■Internal RAM area (M37735S4BFP: addresses 8016 to 87F16)

●At hardware reset
(not including the case where the stop or wait mode is terminated)...Undefined.
●At software reset...Retains the state immediately before reset.
●When the stop or wait mode is terminated
(when hardware reset is used)...Retains the state immediately before the **STP** or **WIT** instruction is executed.

For announced

Fig. 20.8.2 State of SFR area and internal RAM area immediately after reset (4)

20.9 Electrical characteristics

Except for "Icc," the electrical characteristics of the M37735S4BFP are the same as those of the M37735MHBXXXFP in the microprocessor mode. For the others, refer to chapter **"15. ELECTRICAL CHARACTERISTICS."**

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
Icc	Power source current	External bus is operating, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, f(X_{IN}) = 25 MHz (Square waveform), (f(f_2) = 12.5 MHz), f(X_{CIN}) = 32.768 kHz, in operating **(Note 1)**		11.4	22.8	mA
			Vcc = 5V, f(X_{IN}) = 25 MHz (Square waveform), (f(f_2) = 1.5625 MHz), f(X_{CIN}) : Stopped, in operating **(Note 1)**		1.6	3.2	mA
			Vcc = 5V, f(X_{IN}) = 25 MHz (Square waveform), f(X_{CIN}) = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		10	20	μA
			Vcc = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, in operating **(Note 3)**		60	120	μA
			Vcc = 5 V, f(X_{IN}) : Stopped, f(X_{CIN}) : 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		5	10	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop selection bit at wait state = "1."

3: This is applied when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

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20.10 Low voltage version

Differences from the M37735S4BFP are mainly described below.

20.10.1 Performance overview

The performance overview of the low voltage version differs from that of the M37735S4BFP in the following: memory size and current consumption. For the other items, refer to section **"18.1 Performance overview."** Table 20.10.1 shows the M37735S4LHP's performance overview.

Table 20.10.1 M37735S4LHP's performance overview

Items		Performance
Memory size	RAM	2048 bytes
Current consumption		10.8 mW (When f(XIN) = 12-MHz square wave input, Vcc = 3 V, and the main clock is the system clock, Typ.)
		120 μW (When f(XCIN) = 32 kHz, Vcc = 3 V, the sub clock is the system clock, and the main clock is stopped, Typ.)

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20.10.2 Pin configuration

Figure 20.10.1 shows the M37735S4LHP pin configuration.

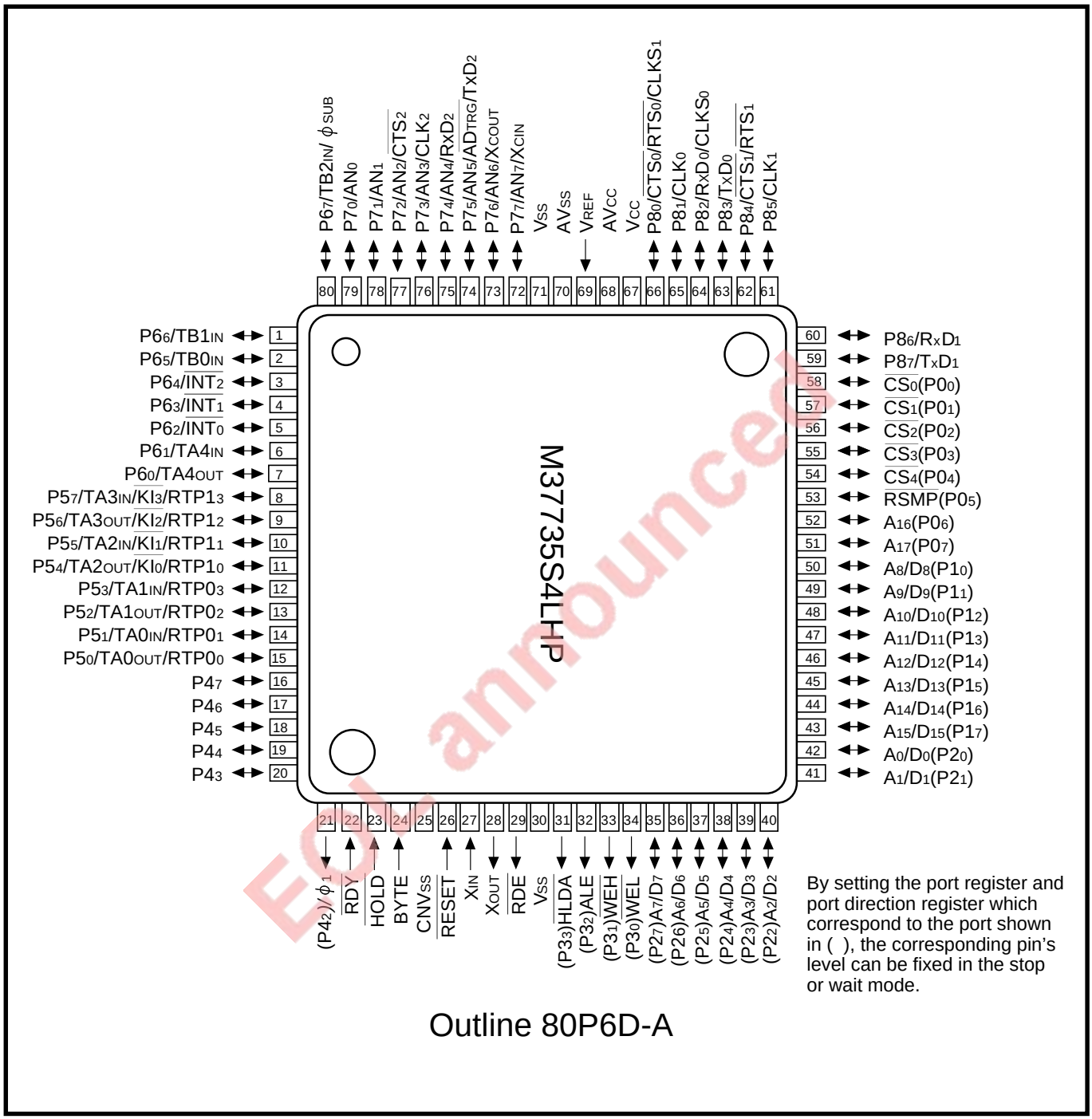

Fig. 20.10.1 M37735S4LHP pin configuration (Top view)

Eol announced

EXTERNAL ROM VERSION

20.10 Low voltage version

20.10.3 Functional description

Except for the power-on reset conditions, the M37735S4LHP has the same functions as the M37735S4BFP For the other functions, refer to the following: **"4. INTERRUPTS" to "9. A-D CONVERTER" in part 1, "2. CENTRAL PROCESSING UNIT (CPU)" in part 2, "3. PROGRAMMABLE I/O PORTS" in part 2, and "10. WATCHDOG TIMER" to "17. APPLICATIONS" in part 2.**

The power-on reset condition of the M37735S4LHP is the same as that of the M37735MHLXXXHP. For the power-on reset condition, refer to section **"18.3 Functional description" in part 1.**

20.10.4 Electrical characteristics

Except for "Icc," the electrical characteristics of the M37735S4LHP are the same as those of the M37735MHLXXXHP in the microprocessor mode. For the others, refer to section **"18.4 Electrical characteristics" in part 2**.

ELECTRICAL CHARACTERISTICS (Vcc= 5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	External bus is operating, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating **(Note 1)**		5.4	10.8	mA
			Vcc = 3 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating **(Note 1)**		3.6	7.2	mA
			Vcc = 3 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 0.75 MHz), $f(X_{CIN})$: Stopped, in operating **(Note 1)**		0.5	1.0	mA
			Vcc = 3V, $f(X_{IN})$ = 12 MHz (Square waveform), $f(X_{CIN})$ = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		6	12	μA
			Vcc = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, in operating **(Note 3)**		40	80	μA
			Vcc = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		3	6	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

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Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1."

3: This is applied when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

APPENDIX

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Appendix 1. Memory allocation of 7735 Group
Appendix 2. Memory allocation in SFR area
Appendix 3. Control registers
Appendix 4. Package outlines
Appendix 5. Hexadecimal instruction code table
Appendix 6. Machine instructions
Appendix 7. Examples of handling unused pins
Appendix 8. Countermeasure examples against noise
Appendix 9. Q & A

APPENDIX

Concerning chapter “APPENDIX,” the 7735 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“Appendix 1. Memory allocation of 7735 Group”**
- **“Appendix 2. Memory allocation in SFR area”**
- **“Appendix 3. Control registers”**
- **“Appendix 7. Examples of handling unused pins”**

Note: The following sections of the 7735 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“Appendix 4. Package outlines”** (**page 21-38 in part 1**)
- **“Appendix 5. Hexadecimal instruction code table”** (**page 21-41 in part 1**)
- **“Appendix 6. Machine instructions”** (**page 21-44 in part 1**)
- **“Appendix 8. Countermeasure examples against noise”** (**page 21-61 in part 1**)
- **“Appendix 9. Q & A”** (**page 21-71 in part 1**)

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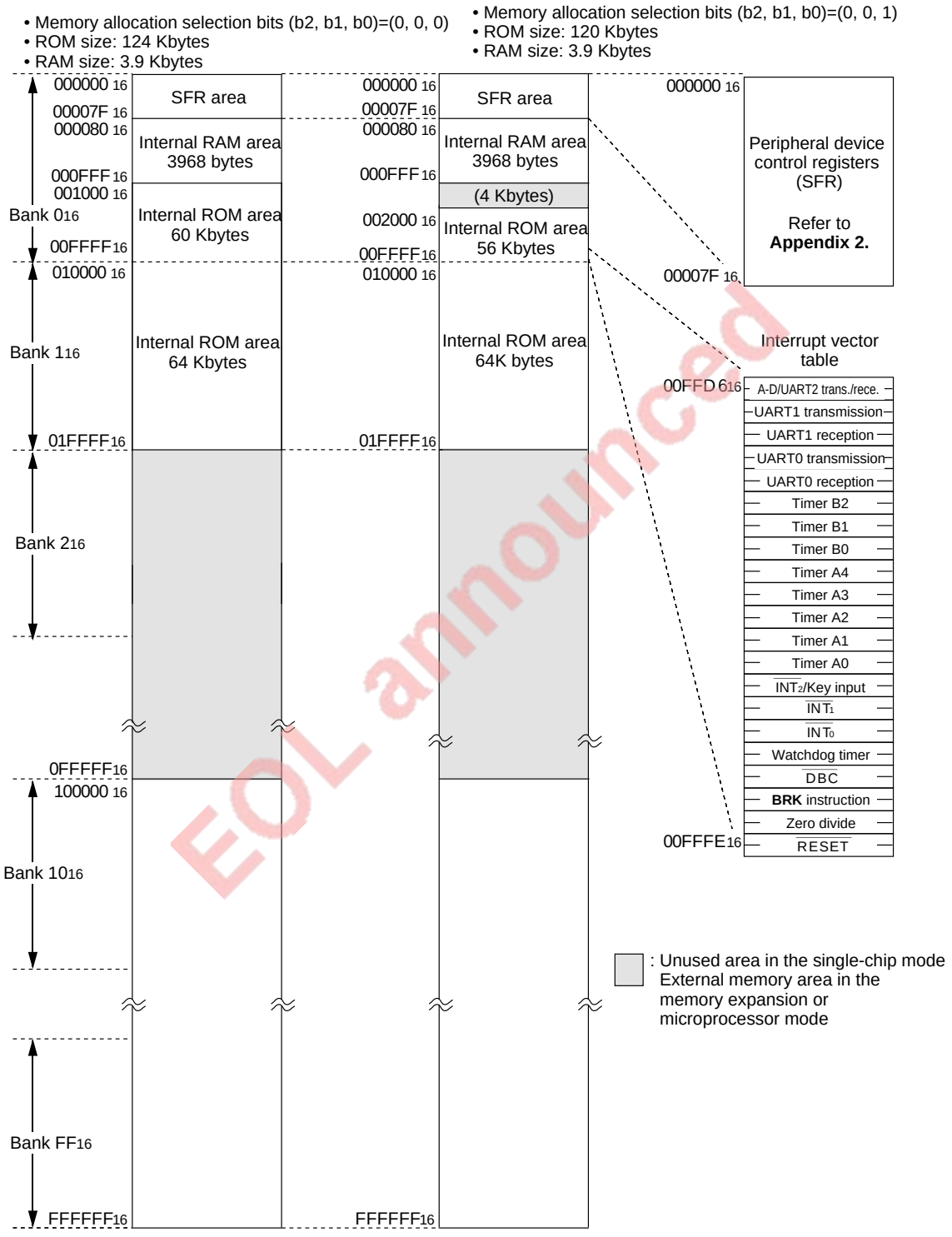
Appendix 1. Memory allocation of 7735 Group

1. M37735MHBXXXFP, M37735EHBXXXFP, M37735EHBFS, M37735MHLXXXHP, M37735EHLXXXHP



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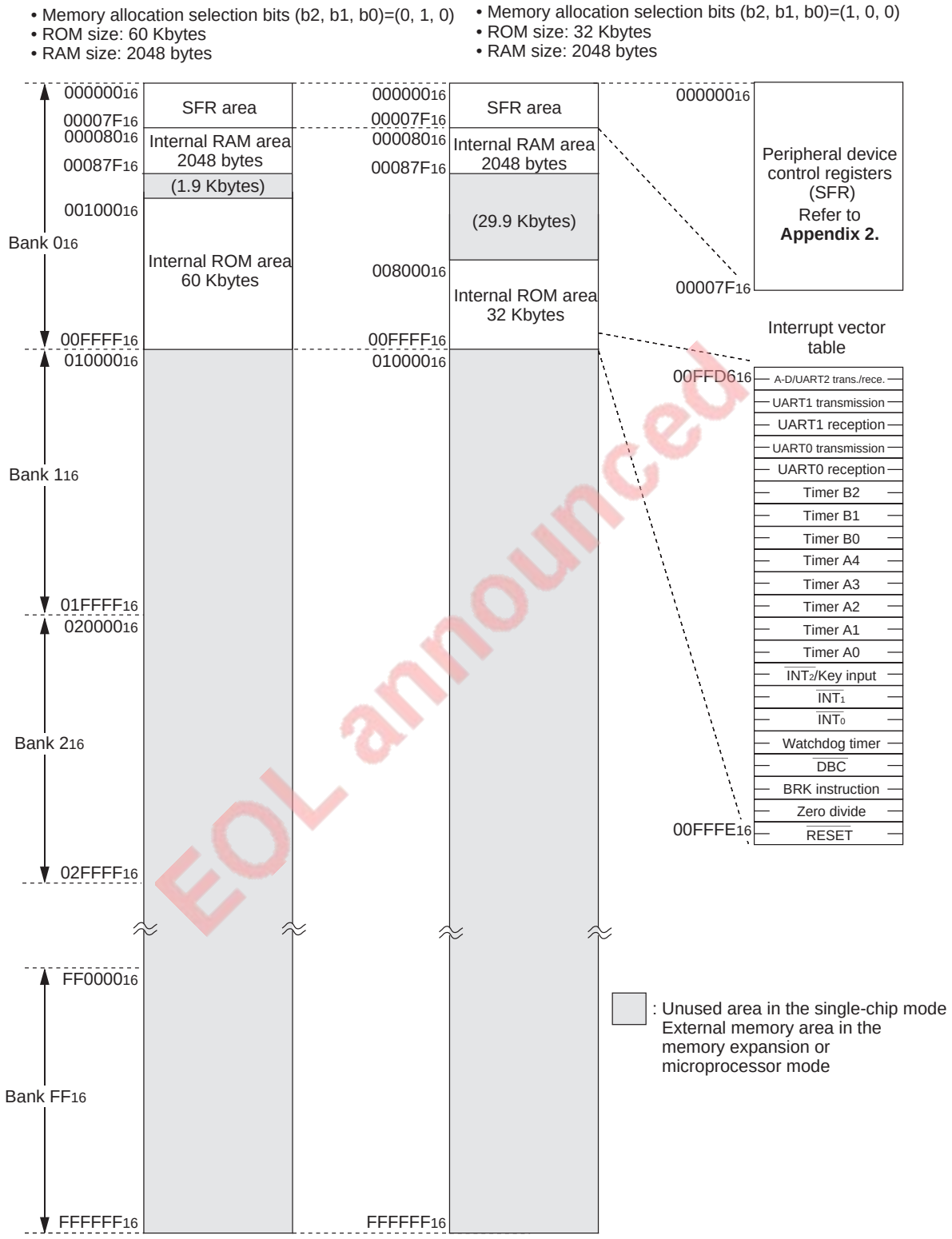
Notes 1: Access to internal ROM area is disabled in the microprocessor mode.
(Refer to section "2.5 Processor modes" in part 1.)
2: In the 7735 Group, banks 10_{16} to FF_{16} cannot be accessed.

Fig. 1 Memory allocation of M37735MHBXXXFP, M37735EHBXXXFP, M37735EHBFS, M37735MHLXXXHP, M37735EHLXXXHP (1)

APPENDIX

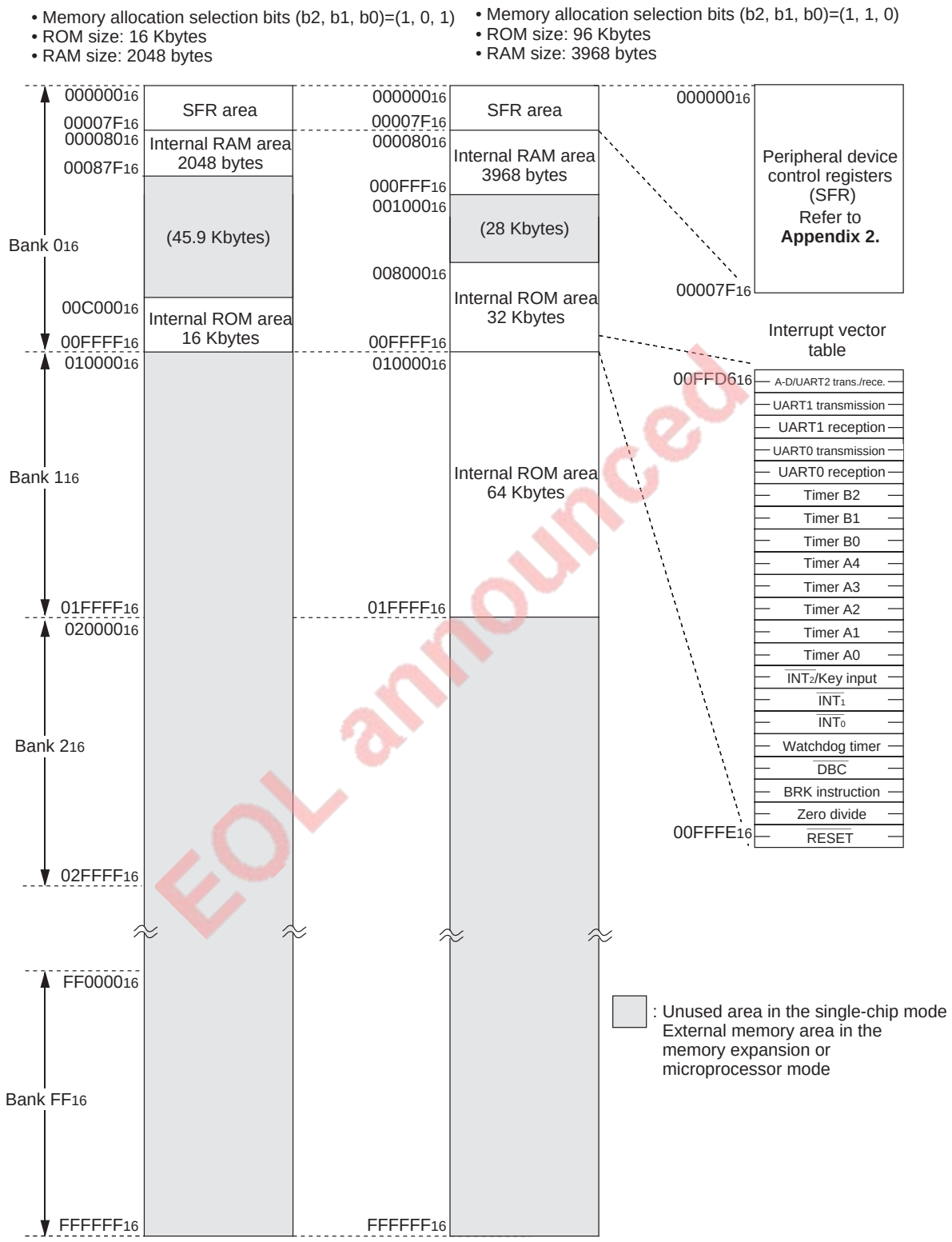
Appendix 1. Memory allocation of 7735 Group



Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)
2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 2 Memory allocation of M37735MHBXXXFP, M37735EHBXXXFP, M37735EHBFS, M37735MHLXXXHP, M37735EHLXXXHP (2)

Appendix 1. Memory allocation of 7735 Group



EOL announced

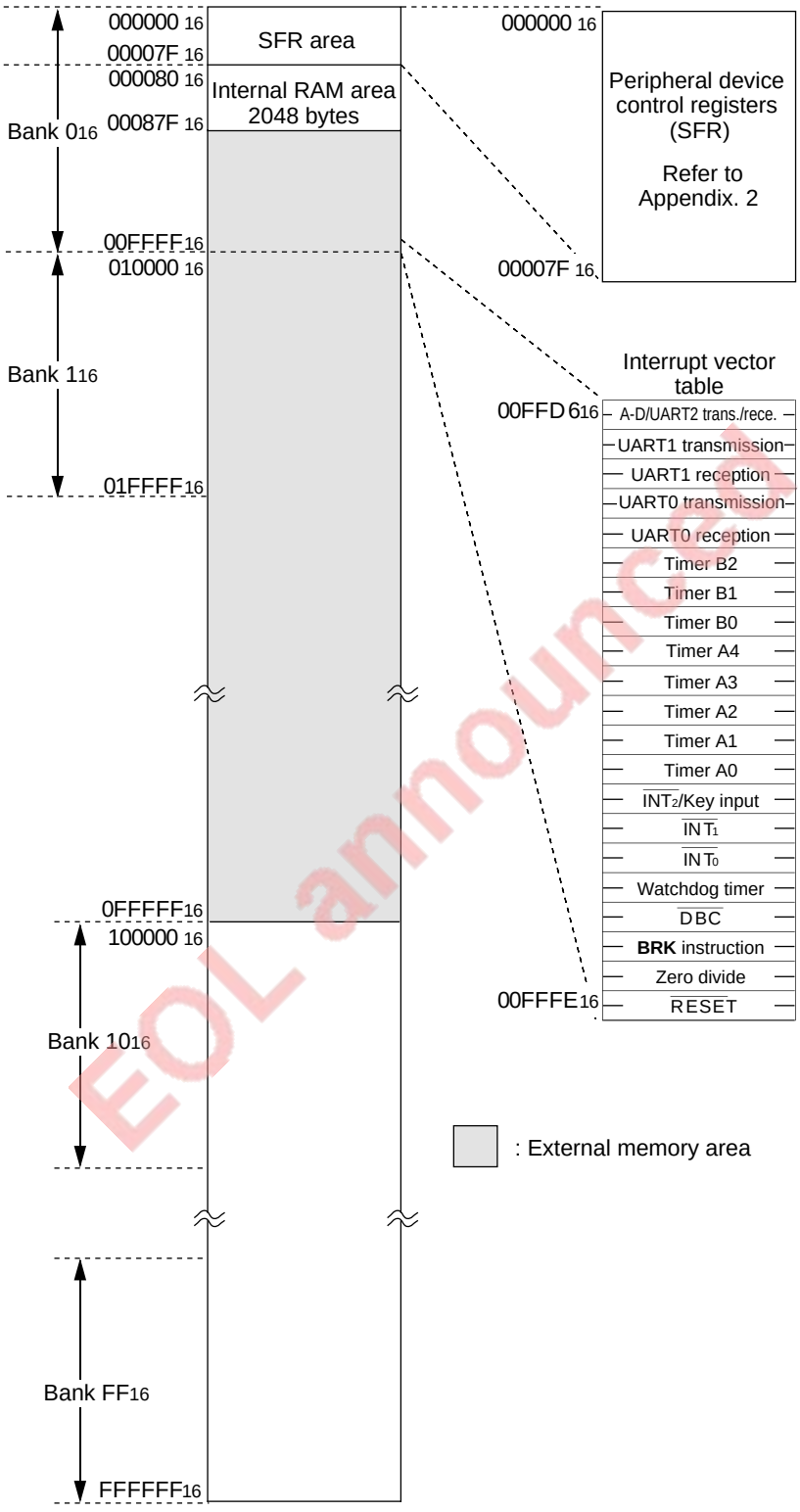
Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)
2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 3 Memory allocation of M37735MHBXXXFP, M37735EHBXXXFP, M37735EHBFS, M37735MHLXXXHP, M37735EHLXXXHP (3)

APPENDIX

Appendix 1. Memory allocation of 7735 Group

2. M37735S4BFP, M37735S4LHP



EOL announced

Notes 1: Addresses 00FFD6$_{16}$ to 00FFFF$_{16}$ are the interrupt vector table.
Be sure to set ROM to this area.
2: In the 7735 Group, banks 10$_{16}$ to FF$_{16}$ cannot be accessed.

Fig. 4 Memory allocation of M37735S4BFP, M37735S4LHP

Appendix 2. Memory allocation in SFR area

Concerning section “Appendix 2. Memory allocation in SFR area,” the 7735 Group differs from the 7733 Group in the following:

- **Address $6F_{16}$ (Refer to Figure 8.)**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“Appendix 2. Memory allocation in SFR area” (page 21-6 in part 1)**

EOL announced

APPENDIX

Appendix 2. Memory allocation in SFR area

Figure 8 differs from that of the 7733 Group only in ❋3.

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
6016	Watchdog timer register	WO	? (❋1)
6116	Watchdog timer frequency selection flag	RW	? 0
6216	(Reserved area) ❋4		?
6316	Memory allocation control register	RW	? 0 0 0 0 0
6416	UART 2 transmit/receive mode register	RW	? 0 0 0 0 0 0 0
6516	UART 2 baud rate register (BRG2)	WO	?
6616	UART 2 transmission buffer register	WO	?
6716		WO	?
6816	UART 2 transmit/receive control register 0	RO RW	? 1 0 0 0
6916	UART 2 transmit/receive control register 1	RO RW RO RW	0 0 0 0 0 0 1 0
6A16	UART 2 receive buffer register	RO	?
6B16		RO	0 0 0 0 0 0 0 ?
6C16	Oscillation circuit control register 0	RW(❋2) RW	? 0 0 0 0 0 ? 1
6D16	Port function control register	RW	0 0 0 0 0 0 0 0
6E16	Serial transmit control register	RW	0 0 0 0 ?
6F16	Oscillation circuit control register 1	WO RW	0 ? 0 ❋3 0 0 0
7016	A-D / UART 2 trans./rece. interrupt control register	RW	? 0 0 0 0
7116	UART0 transmission interrupt control register	RW	? 0 0 0 0
7216	UART0 receive interrupt control register	RW	? 0 0 0 0
7316	UART1 transmission interrupt control register	RW	? 0 0 0 0
7416	UART1 receive interrupt control register	RW	? 0 0 0 0
7516	Timer A0 interrupt control register	RW	? 0 0 0 0
7616	Timer A1 interrupt control register	RW	? 0 0 0 0
7716	Timer A2 interrupt control register	RW	? 0 0 0 0
7816	Timer A3 interrupt control register	RW	? 0 0 0 0
7916	Timer A4 interrupt control register	RW	? 0 0 0 0
7A16	Timer B0 interrupt control register	RW	? 0 0 0 0
7B16	Timer B1 interrupt control register	RW	? 0 0 0 0
7C16	Timer B2 interrupt control register	RW	? 0 0 0 0
7D16	$\overline{INT_0}$ interrupt control register	RW	? 0 0 0 0 0 0
7E16	$\overline{INT_1}$ interrupt control register	RW	? 0 0 0 0 0 0
7F16	$\overline{INT_2}$/Key input interrupt control register	RW	? 0 0 0 0 0 0

❋1 A value of "FFF16" is set to the watchdog timer. (Refer to chapter **"10. WATCHDOG TIMER."**)
❋2 For access characteristics at address 6C16, also refer to **Figure 14.3.2 in part 1.**
❋3 The state of bit 3 at address 6F16 immediately after reset depends on the product.
(Refer to **Figure 14.3.3 in part 2** : refer to **this part** because bit 3 at address 6F16 of the 7735 Group differs from that of the 7733 Group.
Fix this bit to "0" in the 7735 Group.
❋4 Do not wirte to the reserved area.
(Refer to Figure 20.8.1 for the M37733S4BFP, M37733S4LHP, M37735S4BFP, 37735S4LHP.)

■Internal RAM area (M37735MHBXXXFP: addresses 8016 to FFF16)

- At hardware reset
(not including the case where the stop or wait mode is terminated)...Undefined.
- At software reset...Retains the state immediately before reset.
- When the stop or wait mode is terminated
(when the hardware reset is used)...Retains the state immediately before the **STP** or **WIT** instruction is executed.

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Fig. 8 Memory allocation in SFR area (4)

Appendix 3. Control registers

Concerning section “Appendix 3. Control registers,” the 7735 Group differs from the 7733 Group in the following:

- **Oscillation circuit control register 1**

The other control registers are the same as those of the 7733 Group. Therefore, for the other control registers, refer to part 1:

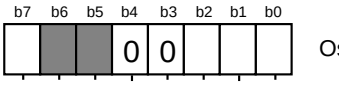
- **“Appendix 3. Control registers” (page 21-10 in part 1)**

EOL announced

APPENDIX

Appendix 3. Control registers

Oscillation circuit control register 1



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P7$_6$ functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P7$_6$ functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3 **(Note 4)**	Must be fixed to "0" in the mask ROM and external ROM versions **(Note 1)**.		0	RW
	Must be fixed to "0" in the one time PROM and EPROM versions **(Notes 1 and 2)**.		1	
4	Must be fixed to "0" **(Note 3)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing "1" to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown below.
2: Because this bit is "1" at reset, clear this bit to "0" with the initial setting program after reset.
3: The case where data "01010101_2" is written with the procedure shown below is not included.
4: For the 7733 Group, refer to **Figure 14.3.3 in part 1.**

• When performing clock prescaler reset

Write data "80_{16}." (**LDM** instruction)

• When writing to bits 0 to 3

Write data "01010101_2."(**LDM** instruction)

Next instruction

Write data "$00000XXX_2$." (**LDM** instruction)

(b2 to b0 in the above Figure)

EOL announced

Appendix 7. Examples of handling unused pins

The following are examples of handling unused pins.
These are, however, just examples. In actual use, make the necessary adaptations and properly evaluate performance according to the user's application.

1. In single-chip mode

Table 1 Examples of handling unused pins in single-chip mode

Pins	Handling example
P0–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Note 1**).
$\overline{E}$	Leave this pin open.
XOUT (**Note 2**)	
AVcc	Connect this pin to pin Vcc.
AVss, VREF, BYTE	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these ports function as input ports.
Software reliability can be enhanced when the contents of the above ports ' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.
For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).
2: This is applied when an external clock is input to pin XIN.

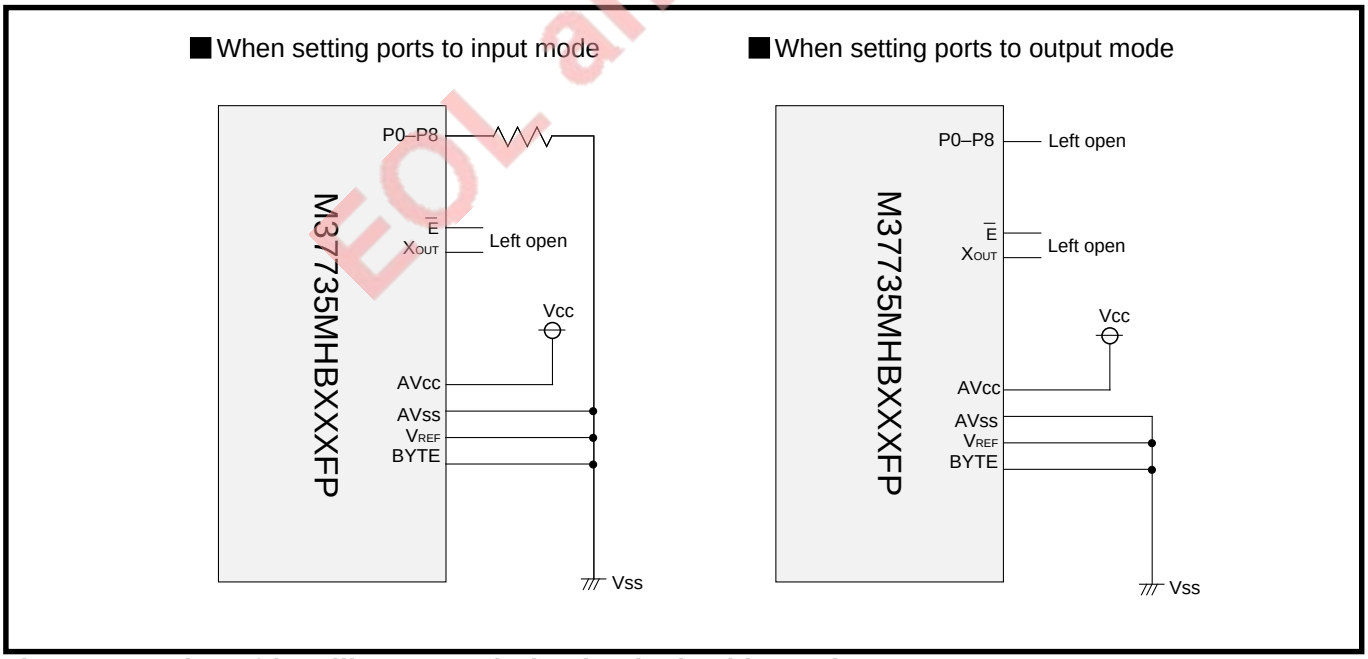


Fig. 9 Examples of handling unused pins in single-chip mode

EOL announced

APPENDIX

Appendix 7. Examples of handling unused pins

2. In memory expansion mode

Table 2 Examples of handling unused pins in memory expansion mode

Pins	Handling example
P42–P47, P5–P8 (**Note 5**)	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
$\overline{WEH}$, $\overline{WEL}$, $\overline{RDE}$, $\overline{HLDA}$, $\overline{CS0}$–$\overline{CS4}$, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
XOUT (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the memory expansion mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

4: This is applied when an external clock is input to pin XIN.

5: Set pin P42/ϕ1 as pin P42. (Clock ϕ1 output is disabled.) And then, for this pin, do the same handling as that for pins P43 to P47 and P5 to P8.

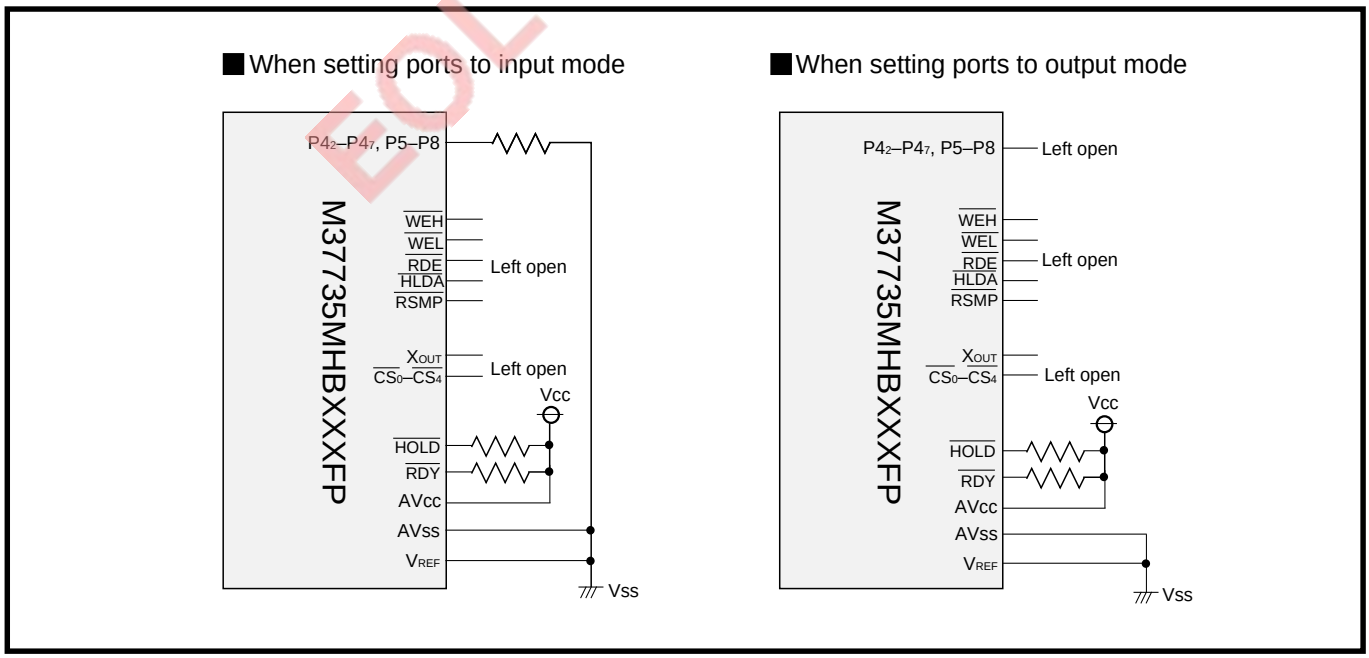


Fig. 10 Examples of handling unused pins in memory expansion mode

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3. In microprocessor mode

Table 3 Examples of handling unused pins in microprocessor mode

Pins	Handling example
P43–P47, P5–P8	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
$\overline{WEH}$, $\overline{WEL}$, $\overline{RDE}$ $\overline{HLDA}$, $\phi 1$, $\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
XOUT (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVCC	Connect this pin to pin Vcc.
AVSS, VREF	Connect these pins to pin Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the microprocessor mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.

4: This is applied when an external clock is input to pin XIN.

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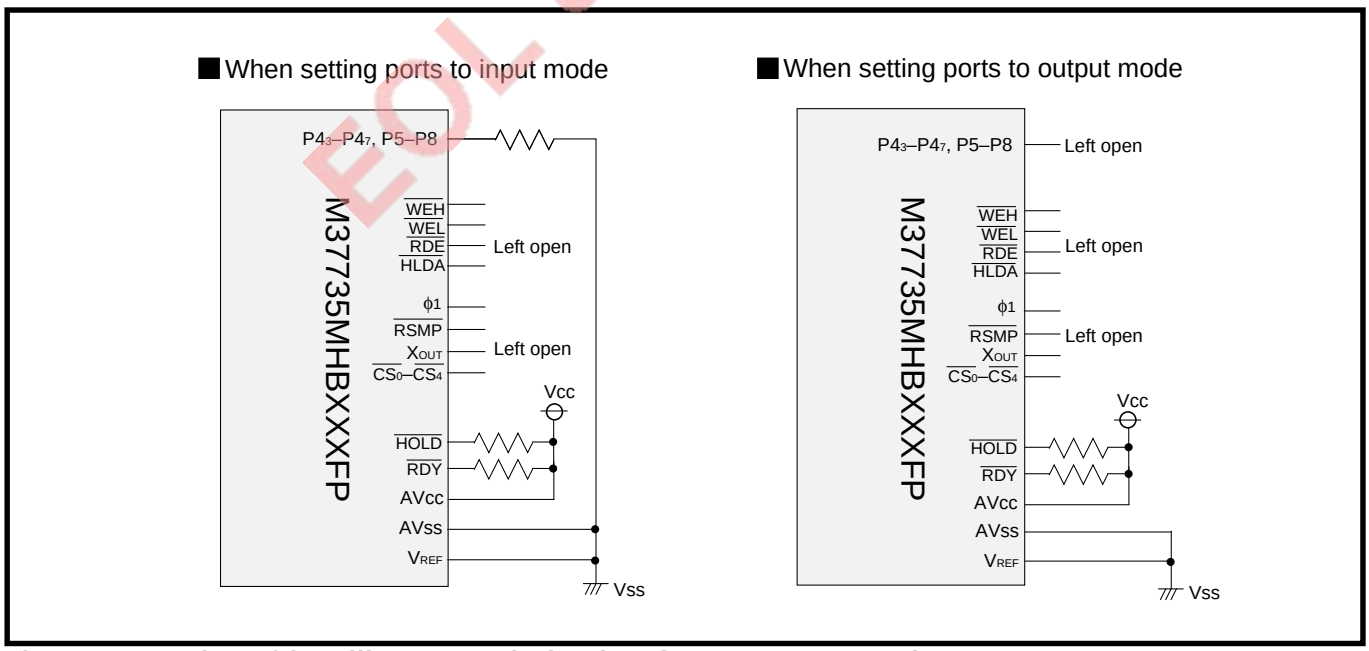

Fig. 11 Examples of handling unused pins in microprocessor mode

APPENDIX

Appendix 7. Examples of handling unused pins

MEMO

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PART 3

7736 Group

CHAPTER 1 OVERVIEW
CHAPTER 2 CENTRAL PROCESSING UNIT (CPU)
CHAPTER 3 PROGRAMMABLE I/O PORTS
CHAPTER 4 INTERRUPTS
CHAPTER 5 KEY INPUT INTERRUPT FUNCTION
CHAPTER 6 TIMER A
CHAPTER 7 TIMER B
CHAPTER 8 SERIAL I/O
CHAPTER 9 A-D CONVERTER
CHAPTER 10 WATCHDOG TIMER
CHAPTER 11 STOP AND WAIT MODES
CHAPTER 12 CONNECTING EXTERNAL DEVICES
CHAPTER 13 RESET
CHAPTER 14 CLOCK GENERATING CIRCUIT
CHAPTER 15 ELECTRICAL CHARACTERISTICS
CHAPTER 16 STANDARD CHARACTERISTICS
CHAPTER 17 APPLICATIONS
CHAPTER 18 LOW VOLTAGE VERSION
CHAPTER 19 BUILT-IN PROM VERSION
APPENDIX

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PART 3 7736 Group

The differences between the 7736 Group and the 7733 Group are mainly described below.
For the 7733 Group, refer to part **"1. 7733 Group."**
For the 7735 Group, refer to part **"2. 7735 Group."**

The 7736 Group differs from the 7733/7735 Group in the following:

- **External bus mode in the memory expansion mode and the microprocessor mode**
  (In the 7736 Group, pin BSEL's level determines the external bus mode, which is A or B.)
- **Output port P9 and I/O port P10**
  (Ports P9 and P10 are assigned only for the 7736 Group.)
- **Pin assignment for the key input interrupt**
  (In the 7736 Group, the pins are assigned to pins $P10_4$ to $P10_7$.)
- **Pin assignment for UART2**
  (In the 7736 Group, the pins are assigned to pins $P9_0$ to $P9_3$.)
- **External ROM version**
  (In the 7736 Group, there is no external ROM version.)
- **Package**
  (In the 7736 Group, the 100-pin QFP is used.)

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CHAPTER 1
OVERVIEW

1.1 Performance overview
1.2 Pin configuration
1.3 Pin description
1.4 Block diagram

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OVERVIEW

1.1 Performance overview

Concerning chapter “1. OVERVIEW,” the 7736 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“1.1 Performance overview”**
- **“1.2 Pin configuration”**
- **“1.3 Pin description”**
- **“1.4 Block diagram”**

1.1 Performance overview

Concerning section “1.1 Performance overview,” the 7736 Group differs from the 7733 Group in the following:

- **Description of the programmable I/O ports, memory expansion, and package in Table 1.1.1**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“1.1 Performance overview” (page 1-3 in part 1)**

Table 1.1.1 M37736MHBXXXGP’s performance overview

Items		Performance
Programmable I/O ports	Ports P0–P2, P4–P8, P10	8 bits × 9
	Port P3	4 bits × 1
Output port	Port P9	8 bits × 1
Memory expansion		Possible • External bus mode A: Maximum of 16 Mbytes • External bus mode B: Maximum of 1 Mbytes
Package		100-pin plastic molded QFP

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1.2 Pin configuration

Figure 1.2.1 shows the M37736MHBXXXGP pin configuration.

Note: For the low voltage version, refer to chapter **"18. LOW VOLTAGE VERSION."**

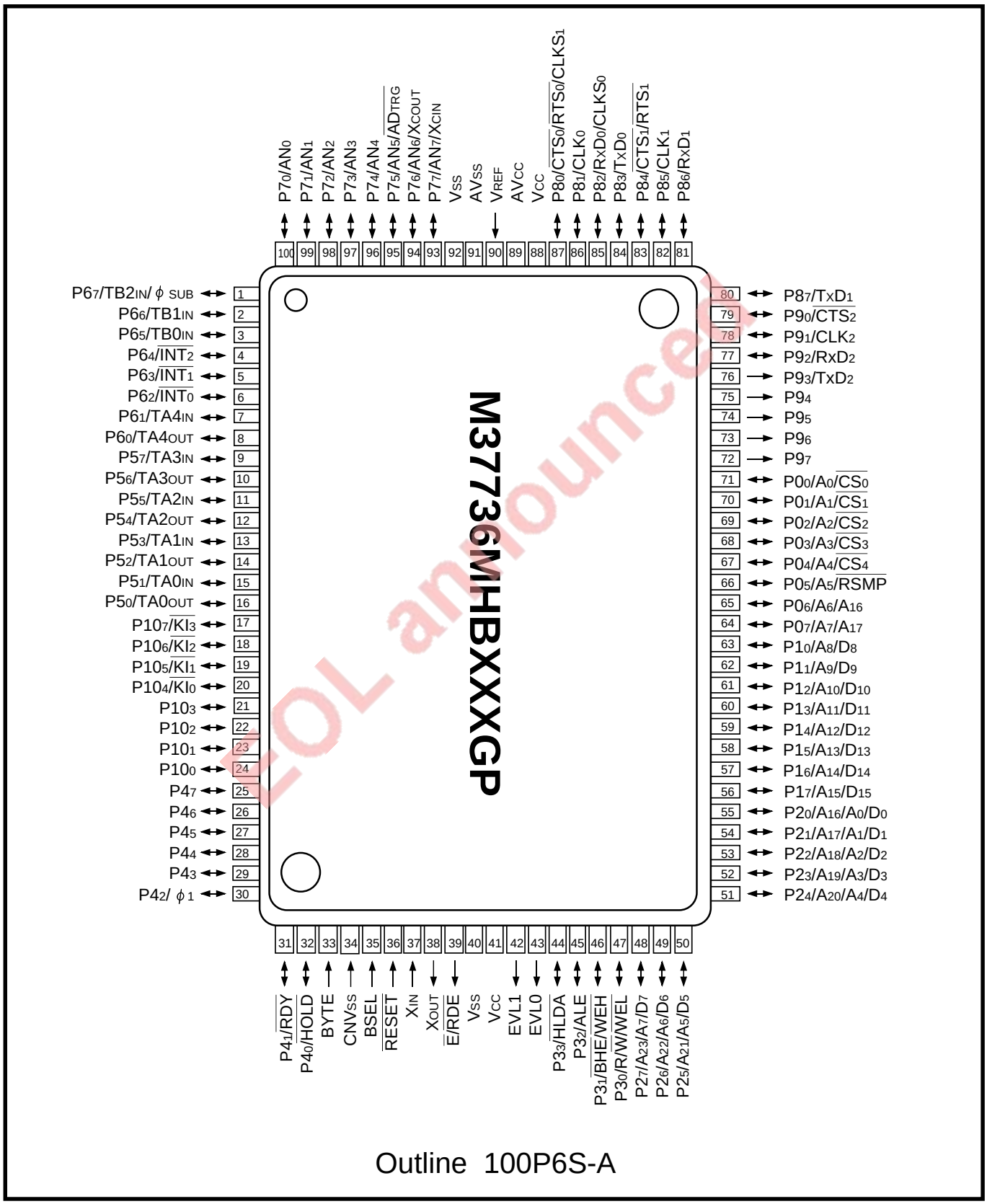

Fig. 1.2.1 M37736MHBXXXGP pin configuration (Top view)

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1.3 Pin description

Concerning section “1.3 Pin description,” the 7736 Group differs from the 7733 Group in the following:

- **“Description of pins $\overline{E}$ and BSEL in Table 1.3.1”**
- **“Description of pins $P0_0$–$P0_7$, $P2_0$–$P2_7$ and $P3_0$–$P3_3$ in Tables 1.3.2 and 1.3.3”**
- **“Description of pins $P5_0$–$P5_7$, $P7_0$–$P7_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$, EVL0 and EVL1 in Table 1.3.4”**
- **“1.3.1 Examples of handling unused pins”**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“1.3 Pin description” (page 1-5 in part 1)**

Table 1.3.1 Pin description (1)

Pin	Processor modes	External bus modes	Name	I/O	Functions
$\overline{E}$	Single-chip mode	—	Enable output	Output	Same as the 7733 Group.
	Memory expansion or Microprocessor mode	A		Output	This pin outputs internal enable signal $\overline{E}$.
		B		Output	This pin outputs read enable signal $\overline{RDE}$. $\overline{RDE}$’s level is “L” in the data read period of the read cycle.
BSEL	Single-chip mode	—	Bus select input	Input	The level of a signal which is input to this pin may be “H” or “L.”
	Memory expansion or Microprocessor mode	A, B		Input	The signal which is input to this pin determines the external bus mode. When this signal’s level is “H,” external bus mode A is selected; when this signal’s level is “L,” external bus mode B is selected.

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Table 1.3.2 Pin description (2)

Pin	Processor mode	External bus mode	Name	I/O	Functions
P0$_0$–P0$_7$	Single-chip mode	—	I/O port P0	I/O	Same as the 7733 Group.
A$_0$–A$_7$	Memory expansion or Microprocessor mode	A		Output	Address's low-order 8 bits (A$_0$–A$_7$) are output.
$\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$, A$_{16}$, A$_{17}$		B		Output	These pins respectively output signals $\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$, and address's high-order 2 bits (A$_{16}$ and A$_{17}$). ● Signals $\overline{CS_0}$–$\overline{CS_4}$ These signals are the chip select signals. When the microcomputer accesses a certain area, the corresponding pin outputs "L" level. (Refer to **Table 2.5.4.**) ● Signal $\overline{RSMP}$ This signal is the ready sampling signal and is used to generate signal $\overline{RDY}$ for accessing external memory area.
P2$_0$–P2$_7$	Single-chip mode	—	I/O port P2	I/O	Same as the 7733 Group.
A$_{16}$/D$_0$–A$_{23}$/D$_7$	Memory expansion or Microprocessor mode	A		Output	Input/Output of data (D$_0$–D$_7$) and output of address's high-order 8 bits (A$_{16}$–A$_{23}$) are performed with the time sharing method.
A$_0$/D$_0$–A$_7$/D$_7$		B		Output	Input/Output of data (D$_0$–D$_7$) and output of address's low-order 8 bits (A$_0$–A$_7$) are performed with the time sharing method.

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1.3 Pin description

Table 1.3.3 Pin description (3)

Pin	Processor mode	External bus mode	Name	I/O	Functions
$P3_0$–$P3_3$	Single-chip mode	—	I/O port P3	I/O	Same as the 7733 Group.
R/$\overline{W}$, $\overline{BHE}$, ALE, $\overline{HLDA}$	Memory expansion or Microprocessor mode	A		Output	These pins respectively output signals R/$\overline{W}$, $\overline{BHE}$, ALE, and $\overline{HLDA}$. ● Signal R/$\overline{W}$ This signal indicates the data bus state. When this signal level is "H," a data bus is in the read state. When this signal level is "L," a data bus is in the write state. ● Signal $\overline{BHE}$ This signal's level is "L" when the microcomputer accesses an odd address. ● Signal ALE This signal is used to separate the multiplexed signal which consists of an address and data to the address and the data. ● Signal $\overline{HLDA}$ This signal informs the external whether this microcomputer enters the Hold state or not. In Hold state, pin $\overline{HLDA}$ outputs "L" level.
$\overline{WEL}$, $\overline{WEH}$, ALE, $\overline{HLDA}$		B		Output	These pins respectively output signals $\overline{WEL}$, $\overline{WEH}$, ALE, and $\overline{HLDA}$. ● Signal $\overline{WEL}$, $\overline{WEH}$ Signal $\overline{WEL}$ is the write enable low signal. Signal $\overline{WEH}$ is the write enable high signal. These signals' levels are "L" in the data write period of the write cycle. The operations of these signals depend on the level of pin BYTE. (Refer to **Table 12.1.1 in part 2.**) ● Signal ALE This signal is the same as that in external bus mode A. ● Signal $\overline{HLDA}$ This signal is the same as that in external bus mode A.

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Table 1.3.4 Pin description (4)

Pin	Processor mode	External bus mode	Name	I/O	Functions
$P5_0$–$P5_7$	Single-chip mode	—	I/O port P5	I/O	P5 is an 8-bit I/O port with the same function as port P0 and can be programmed as I/O pins for timers A0–A3.
	Memory expansion or Microprocessor mode	A, B			
$P7_0$–$P7_7$	Single-chip mode	—	I/O port P7	I/O	P7 is an 8-bit I/O port with the same function as port P0 and can be programmed as analog input pins for the A-D converter. $P7_6$ and $P7_7$ can be programmed as I/O pins (X_{COUT}, X_{CIN}) for the sub-clock (32 kHz) oscillation circuit. When using $P7_6$ and $P7_7$ as pins X_{COUT} and X_{CIN}, connect a quartz-crystal oscillator between them. When inputting an external clock, input the clock from pin X_{CIN}.
	Memory expansion or Microprocessor mode	A, B			
$P9_0$–$P9_7$	Single-chip mode	—	Output port P9	Output	P9 is an 8-bit output-only port. After reset, P9 enters a floating state. When data is written to the port P9 register, P9 starts outputting **(Note)**. $P9_0$–$P9_3$ also function as UART2's I/O pins.
	Memory expansion or Microprocessor mode	A, B			
$P10_0$–$P10_7$	Single-chip mode	—	I/O port P10	I/O	P10 is an 8-bit I/O port with the same function as port P0. Pins 10_4–10_7 can be programmed as input pins ($\overline{KI_0}$–$\overline{KI_3}$) for the key input interrupt.
	Memory expansion or Microprocessor mode	A, B			
EVL0, EVL1	Single-chip mode	—	———	Output	Leave these pins open.
	Memory expansion or Microprocessor mode	A, B			

Note: After reset, be sure to write data to the port P9 latch.

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OVERVIEW

1.3 Pin description

1.3.1 Examples of handling unused pins

The following are examples of handling unused pins.
These are, however, just examples. In actual use, make the necessary adaptations and properly evaluate performance according to the user's application.

(1) In single-chip mode

Table 1.3.5 Examples of handling unused pins in single-chip mode

Pins	Handling example
P0–P8, P10	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins open after they are set to the output mode (**Note 1**).
P9	Leave these pins open after writing data to the port P9 register (**Note 3**).
$\overline{E}$, $\overline{RDE}$	Leave this pin open.
EVL0, EVL1	
XOUT (**Note 2**)	
AVcc	Connect this pin to pin Vcc.
AVss, VREF, BYTE	Connect these pins to pin Vss.
BSEL	Connect this pin to pin Vcc or Vss.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until the they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these ports function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.
For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).
2: This is applied when an external clock is input to pin XIN.
3: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

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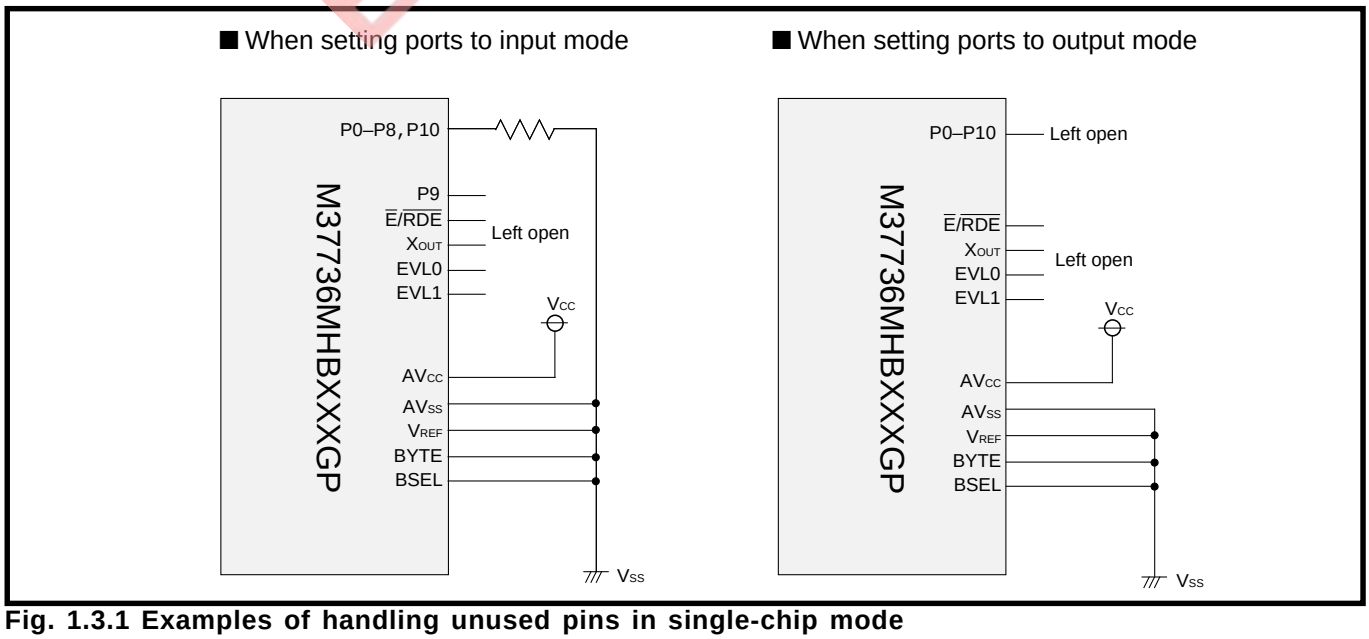

Fig. 1.3.1 Examples of handling unused pins in single-chip mode

(2) In memory expansion mode (External bus mode A)

Table 1.3.6 Examples of handling unused pins in memory expansion mode (External bus mode A)

Pins	Handling example
P42–P47, P5–P8, P10 (**Note 7**)	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 8**).
BHE (**Note 3**), ALE (**Note 4**), $\overline{\text{HLDA}}$	Leave these pins open. (**Note 5**)
XOUT (**Note 6**)	Leave this pin open.
$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the memory expansion mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

6: This is applied when an external clock is input to pin XIN.

7: Set pin P42/ϕ1 as pin P42. (Clock ϕ1 output is disabled.) And then, for this pin, do the same handling as that for pins P43 to P47, P5 to P8 and P10.

8: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

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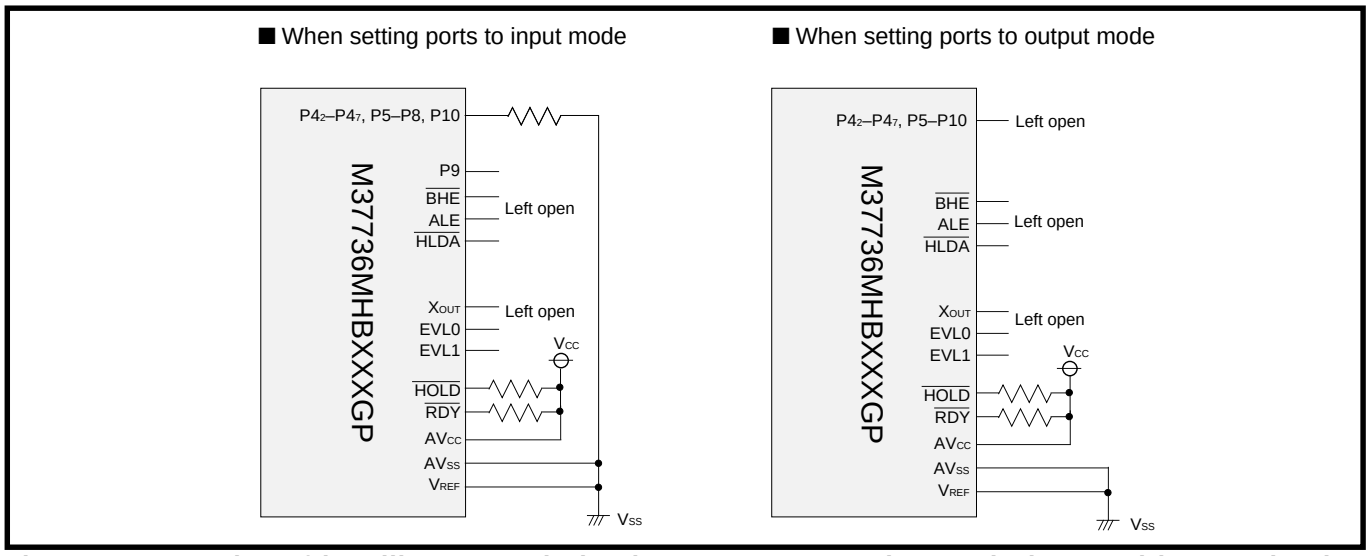

Fig. 1.3.2 Examples of handling unused pins in memory expansion mode (External bus mode A)

1.3 Pin description

(3) In memory expansion mode (External bus mode B)

Table 1.3.7 Examples of handling unused pins in memory expansion mode (External bus mode B)

Pins	Handling example
$P4_2$–$P4_7$, P5–P8, P10 (**Note 5**)	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 6**).
$\overline{WHE}$, $\overline{WHL}$, $\overline{RDE}$, $\overline{HLDA}$, $\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
X_{OUT} (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, V_{REF}	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the memory expansion mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

4: This is applied when an external clock is input to pin X_{IN}.

5: Set pin $P4_2/\phi_1$ as pin $P4_2$. (Clock ϕ_1 output is disabled.) And then, for this pin, do the same handling as that for pins $P4_3$ to $P4_7$, P5 to P8 and P10.

6: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

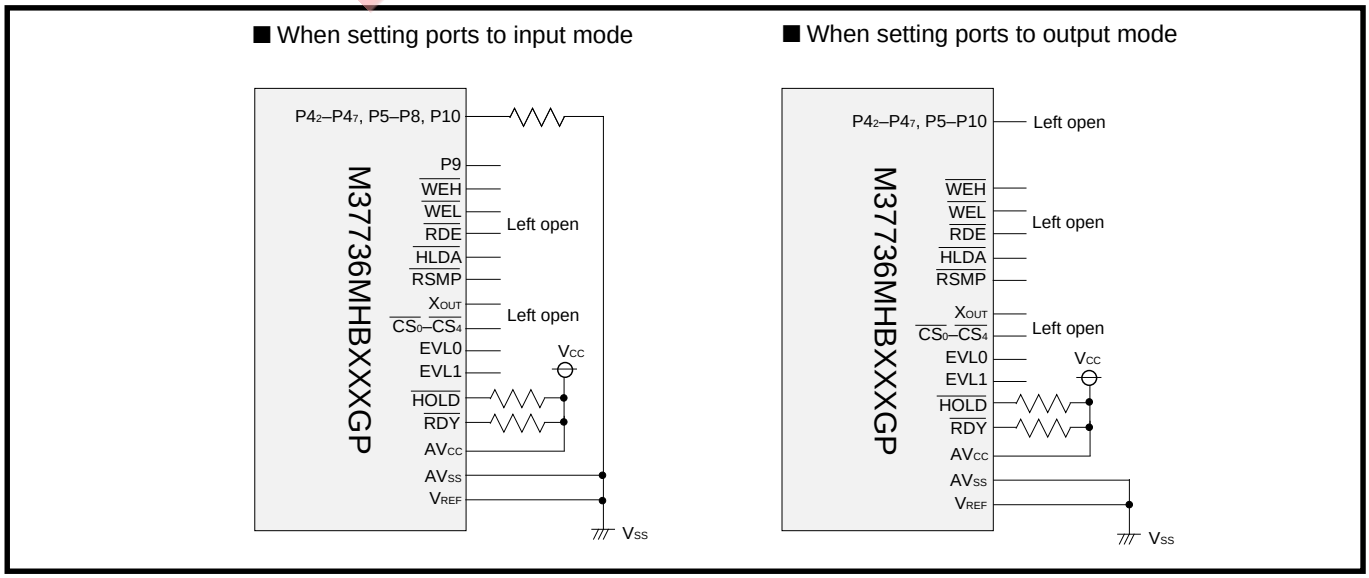

Fig. 1.3.3 Examples of handling unused pins in memory expansion mode (External bus mode B)

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(4) In microprocessor mode (External bus mode A)

Table 1.3.8 Examples of handling unused pins in microprocessor mode (External bus mode A)

Pins	Handling example
P43–P47, P5–P8, P10	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 7**).
BHE (**Note 3**), ALE (**Note 4**), $\overline{\text{HLDA}}$, ϕ_1	Leave these pins open. (**Note 3**)
XOUT (**Note 6**)	Leave this pin open.
$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVCC	Connect this pin to pin Vcc.
AVSS, VREF	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the microprocessor mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.

6: This is applied when an external clock is input to pin XIN.

7: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

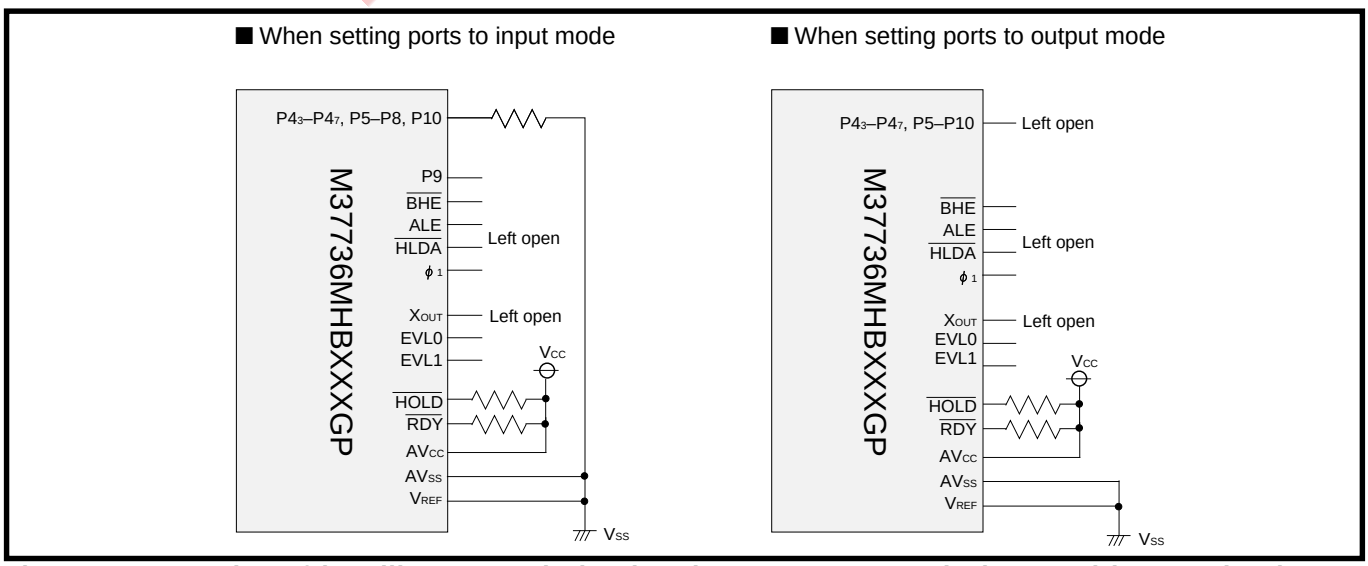

Fig. 1.3.4 Examples of handling unused pins in microprocessor mode (External bus mode A)

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(5) In microprocessor mode (External bus mode B)

Table 1.3.9 Examples of handling unused pins in microprocessor mode (External bus mode B)

Pins	Handling example
P43–P47, P5–P8, P10	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 5**).
$\overline{WHE}$, $\overline{WHL}$, $\overline{RDE}$, $\overline{HLDA}$, ϕ_1, CS_0–CS_4, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
XOUT (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVCC	Connect this pin to pin Vcc.
AVSS, VREF	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the microprocessor mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.

4: This is applied when an external clock is input to pin XIN.

5: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

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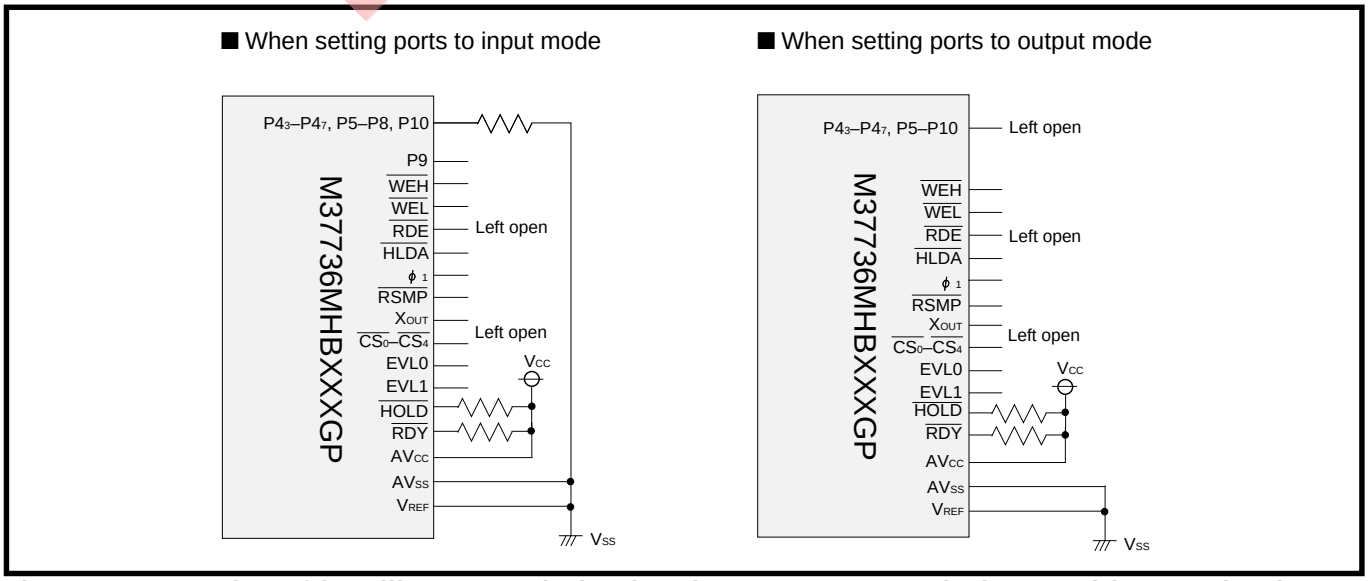

Fig. 1.3.5 Examples of handling unused pins in microprocessor mode (External bus mode B)

1.4 Block diagram

Figure 1.4.1 shows the M37736MHBXXXGP block diagram.

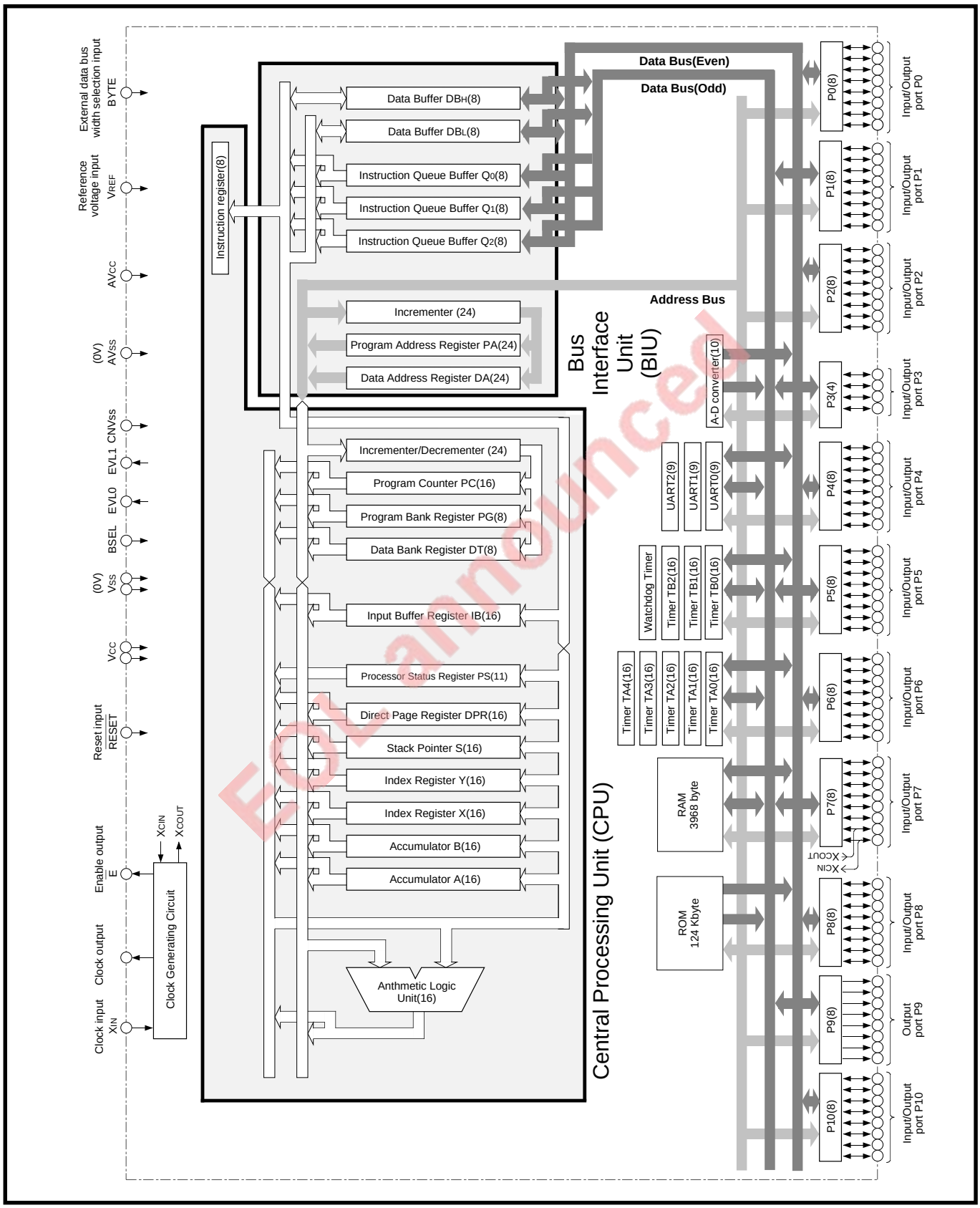

Fig. 1.4.1 M37736MHBXXXGP block diagram

OVERVIEW

1.4 Block diagram

MEMO

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CHAPTER 2

CENTRAL PROCESSING UNIT (CPU)

2.1 Central processing unit
2.2 Bus interface unit
2.3 Accessible area
2.4 Memory allocation
2.5 Processor modes

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CENTRAL PROCESSING UNIT (CPU)

2.5 Processor modes

Concerning chapter “2. CENTRAL PROCESSING UNIT (CPU),” the 7736 Group differs from the 7733 Group in the following section. Therefore, only the differences are described below:

- **“2.5 Processor modes”**

The following sections of the 7736 Group differ depending on the external bus mode, which is A or B:

- **“2.2 Bus interface unit”**
  External bus mode A (page 2–10 in part 1)
  External bus mode B (page 2–2 in part 2)
- **“2.3 Accessible area”**
  External bus mode A (page 2–16 in part 1)
  External bus mode B (page 2–5 in part 2)

The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to the part 1:

- **“2.1 Central processing unit” (page 2–2 in part 1)**
- **“2.4 Memory allocation” (page 2–18 in part 1)**

2.5 Processor modes

Concerning section “2.5 Processor modes,” the 7736 Group differs from the 7733 Group in the following:

- **“Figure 2.5.2”**

The following differ depending on the external bus mode. Therefore, refer to the corresponding part:

- **Figure 2.5.1 and Table 2.5.1**
  External bus mode A (Figure 2.5.1 and Table 2.5.1 in part 1)
  External bus mode B (Figure 2.5.1 and Table 2.5.1 in part 2)

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“2.5 Processor modes” (page 2–23 in part 1)**

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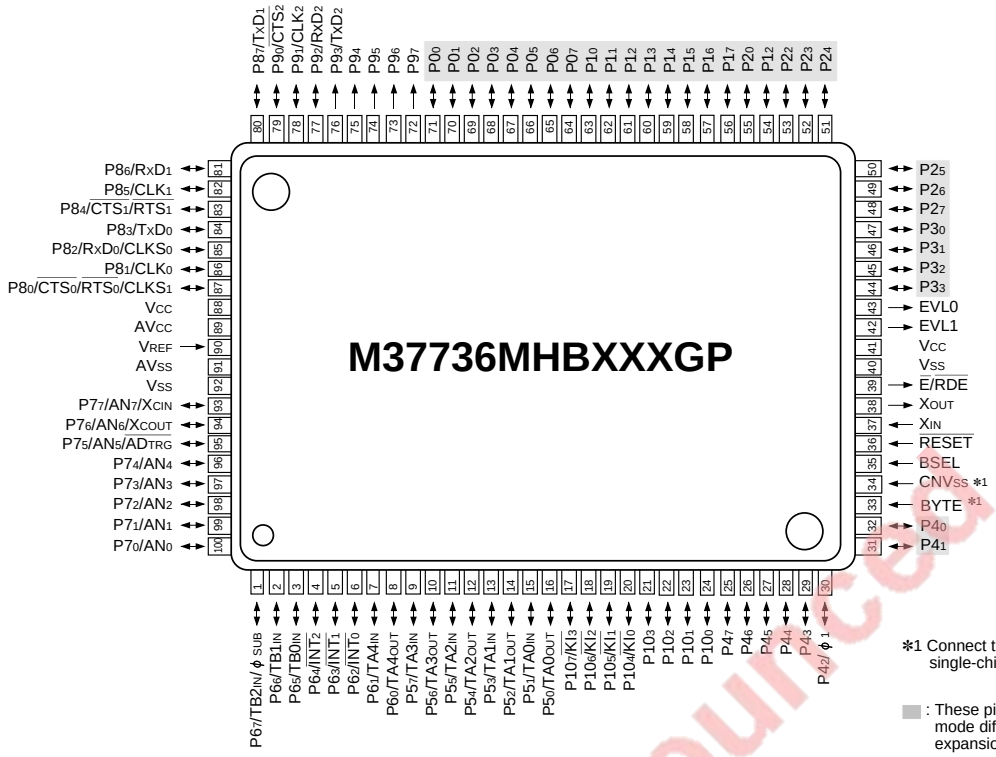
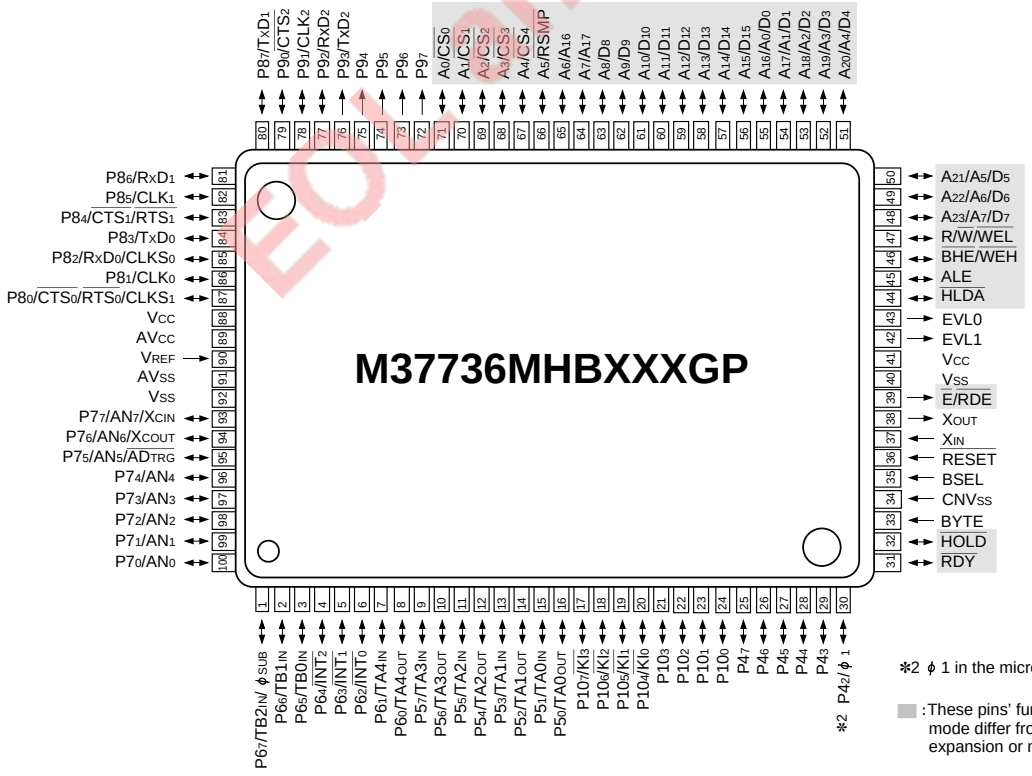
<Single-Chip mode>



*1 Connect this pin to Vss in the single-chip mode.

: These pins' functions in the single-chip mode differ from those in the memory expansion or microprocessor mode.

<Memory expansion and Microprocessor modes>



*2 φ 1 in the microprocessor mode

: These pins' functions in the single-chip mode differ from those in the memory expansion or microprocessor mode.

Fig. 2.5.2 Pin configuration in each processor mode (Top view)

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MEMO

EOL announced

CHAPTER 3

PROGRAMMABLE I/O PORTS

EOL announced

3.1 Programmable I/O ports and Output-only ports
3.2 Port peripheral circuits
3.3 Pull-up function
3.4 Internal peripheral devices' I/O functions (Ports $P4_2$, P5 to P8, $P9_0$ to $P9_3$, and $P10_4$ to $P10_7$)

PROGRAMMABLE I/O PORTS

3.1 Programmable I/O ports and Output-only ports

Functions of all ports in the single-chip mode and those of ports $P4_3$ to $P4_7$ and P5 to P10 in the memory expansion or the microprocessor mode are described below. For more information about ports P0 to P4, whose functions depend on the processor mode, refer to section **"2.5 Processor modes"** and chapter **"12. CONNECTING EXTERNAL DEVICES."**

3.1 Programmable I/O ports and Output-only ports

The 7736 Group has 76 programmable I/O ports (P0 to P8 and P10) and 8 output-only ports (P9).
Each of programmable I/O ports has a port direction register and a port register in the SFR area. Each output-only port has a port register in the SFR area. Figure 3.1.1 shows the memory map of port direction registers and port registers.
Note that ports $P4_2$, P5 to P8, $P9_0$ to $P9_3$ and $P10_4$ to $P10_7$ also function as I/O pins for internal peripheral devices. For details, refer to section **"3.4 Internal peripheral devices' I/O functions"** and the corresponding functional description.

addresses	
2_{16}	Port P0 register
3_{16}	Port P1 register
4_{16}	Port P0 direction register
5_{16}	Port P1 direction register
6_{16}	Port P2 register
7_{16}	Port P3 register
8_{16}	Port P2 direction register
9_{16}	Port P3 direction register
A_{16}	Port P4 register
B_{16}	Port P5 register
C_{16}	Port P4 direction register
D_{16}	Port P5 direction register
E_{16}	Port P6 register
F_{16}	Port P7 register
10_{16}	Port P6 direction register
11_{16}	Port P7 direction register
12_{16}	Port P8 register
13_{16}	Port P9 register
14_{16}	Port P8 direction register
15_{16}	
16_{16}	Port P10 register
17_{16}	
18_{16}	Port P10 direction register

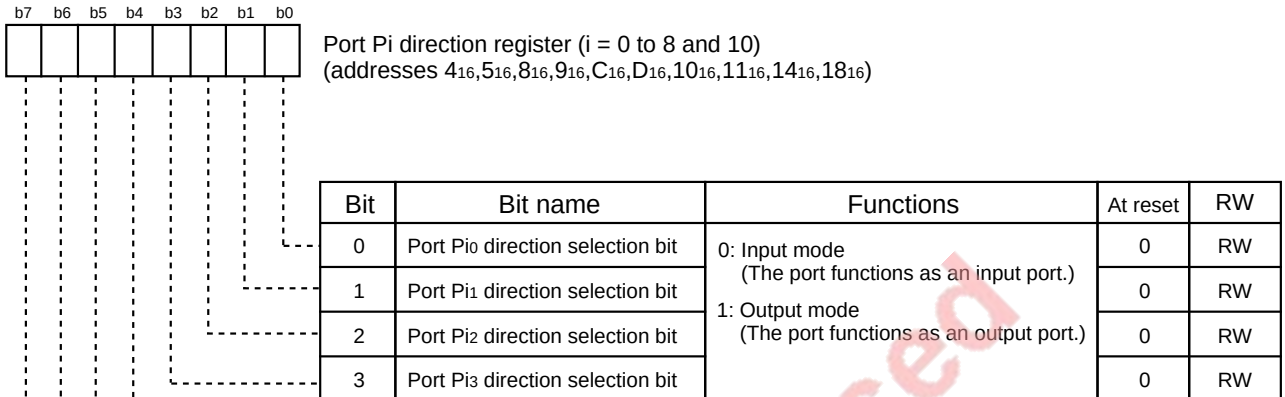
EOL announced

Fig. 3.1.1 Memory map of port direction registers and port registers

3.1.1 Port Pi direction register

This register determines the direction of programmable I/O ports. Each bit of this register corresponds to one specified pin.

Figure 3.1.2 shows the structure of the port Pi (i = 0 to 8 and 10) direction register.



Port Pi direction register (i = 0 to 8 and 10)
(addresses 4_{16},5_{16},8_{16},9_{16},C_{16},D_{16},10_{16},11_{16},14_{16},18_{16})

Bit	Bit name	Functions	At reset	RW
0	Port P_{i0} direction selection bit	0: Input mode (The port functions as an input port.) 1: Output mode (The port functions as an output port.)	0	RW
1	Port P_{i1} direction selection bit		0	RW
2	Port P_{i2} direction selection bit		0	RW
3	Port P_{i3} direction selection bit		0	RW
4	Port P_{i4} direction selection bit		0	RW
5	Port P_{i5} direction selection bit		0	RW
6	Port P_{i6} direction selection bit		0	RW
7	Port P_{i7} direction selection bit		0	RW

Note: Writing to bits 4 to 7 of the port P3 direction register is invalid and these bits are fixed to “0” when they are read.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Corresponding pin	P_{i7}	P_{i6}	P_{i5}	P_{i4}	P_{i3}	P_{i2}	P_{i1}	P_{i0}

EOL announced

Fig. 3.1.2 Structure of port Pi (i = 0 to 8 and 10) direction register

PROGRAMMABLE I/O PORTS

3.1 Programmable I/O ports and Output-only ports

3.1.2 Port Pi register

Data is input from or output to the external by writing or reading data to or from a port register. A port register consists of a port latch, which holds the output data, and a circuit, which reads the pin state. Each bit of the port register corresponds to one specified pin. Figure 3.1.3 shows the structure of the port Pi (i = 0 to 10) register.

(1) How to output data from programmable I/O port

① Set the corresponding bit of the port direction register to the output mode.
② Write data to the corresponding bit of the port register, and then the data is written into the port latch.
③ Data which is set in the port latch is output.

When a bit of a port register which corresponds to a port set for the output mode is read out, the contents of the port latch, instead of pin state, is read out. Accordingly, output data can correctly be read out without influence of external load, etc. (Refer to **Figures 3.2.1 and 3.2.2**)

(2) How to input data from programmable I/O port

① Set the corresponding bit of the port direction register to the input mode.
② The pin enters a floating state.
③ When reading the corresponding bit of the port register in state ②, data which is input from the pin can be read in.

When data is written to a port register which corresponds to a port set for the input mode, the data is written only into the port latch and not output to the external. Pins retain a floating state.

(3) How to output data from output-only port

① Write data to the corresponding bit of the port register, and then the data is written into the port latch.
② Data which is set in the port latch is output.

When a bit of a port register which corresponds to a port is read out, the contents of the port latch, instead of pin state, is read out. Accordingly, output data can correctly be read out without influence of external load, etc. (Refer to **Figures 3.2.1 and 3.2.2**)

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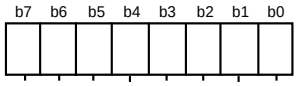


Port Pi register (i = 0 to 10)
(addresses 2_{16},3_{16},6_{16},7_{16},A_{16},B_{16},E_{16},F_{16},12_{16},13_{16},16_{16})

Bit	Bit name	Functions	At reset	RW
0	Port Pi_0's pin	Data is input from or output to a pin by reading/writing from/to the corresponding bit. 0: "L" level 1: "H" level	Undefined	RW
1	Port Pi_1's pin		Undefined	RW
2	Port Pi_2's pin		Undefined	RW
3	Port Pi_3's pin		Undefined	RW
4	Port Pi_4's pin		Undefined	RW
5	Port Pi_5's pin		Undefined	RW
6	Port Pi_6's pin		Undefined	RW
7	Port Pi_7's pin		Undefined	RW

Notes 1: Writing to bits 4 to 7 of the port P3 register is invalid and these bits are fixed to "0" when they are read.
2: After reset, be sure to write data to the port P9 register.

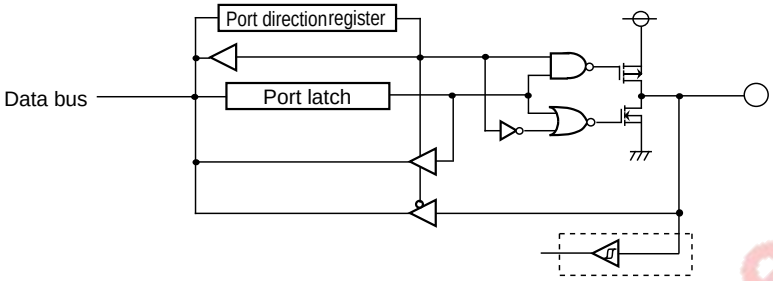
Fig. 3.1.3 Structure of port Pi (i = 0 to 10) register

EOL announced

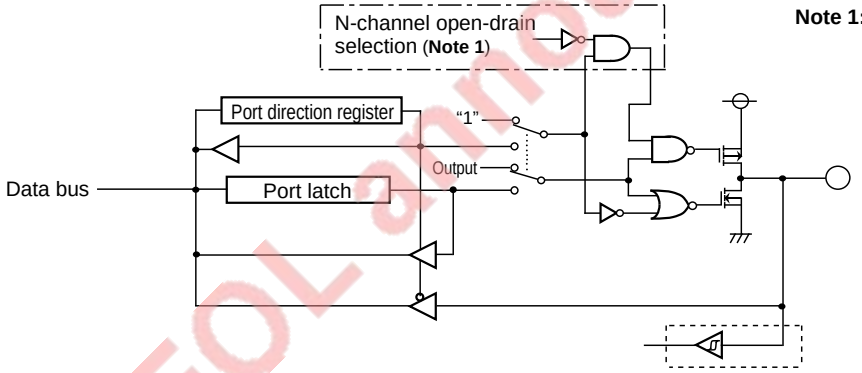
3.2 Port peripheral circuits

Figures 3.2.1 and 3.2.2 show the port peripheral circuits.

• Ports $P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_3$, $P4_3$ to $P4_6$, $P10_0$ to $P10_3$ (Inside dotted-line not included)
Ports $P4_0$/HOLD, $P4_1$/RDY, $P4_7$, $P5_1$/TA0IN, $P5_3$/TA1IN, $P5_5$/TA2IN, $P5_7$/TA3IN, $P6_1$/TA4IN, $P6_5$/TB0IN to $P6_7$/TB2IN/ ϕSUB, $P8_6$/RxD1 (Inside dotted-line included)



•Ports $P8_3$/TxD0, $P8_7$/TxD1 (Inside dotted-line not included, and shaded area included)
Ports $P5_0$/TA0OUT, $P5_2$/TA1OUT, $P5_4$/TA2OUT, $P5_6$/TA3OUT, $P6_0$/TA4OUT, $P8_2$/RxD0/CLKS0 (Inside dotted-line included, and shaded area not included)
Ports $P4_2$/ ϕ_1 (Inside dotted-line not included, and shaded area not included)



Note 1: Valid only when used as pin TxDj for serial I/O.

•Ports $P6_2$/$\overline{INT_0}$ to $P6_4$/$\overline{INT_2}$ (Inside dotted-line included)
Ports $P10_4$/KI_0 to $P10_7$/KI_3 (Inside dotted-line not included)

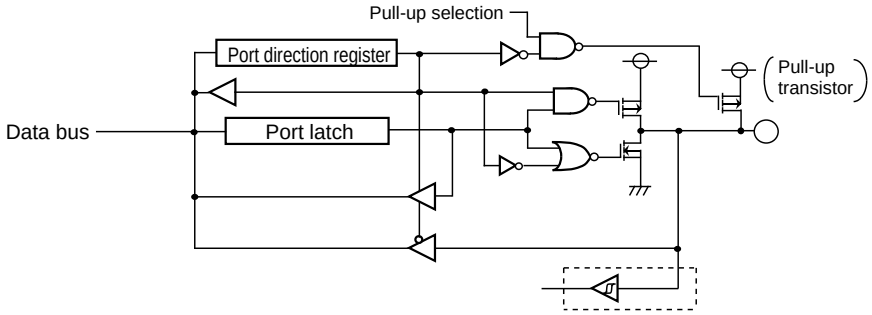


Fig. 3.2.1 Port peripheral circuits (1)

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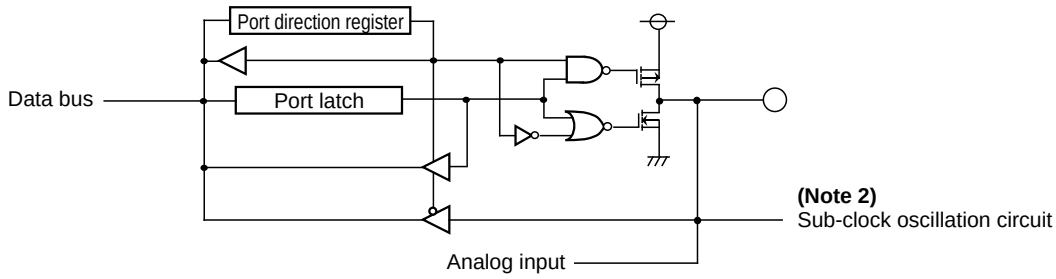
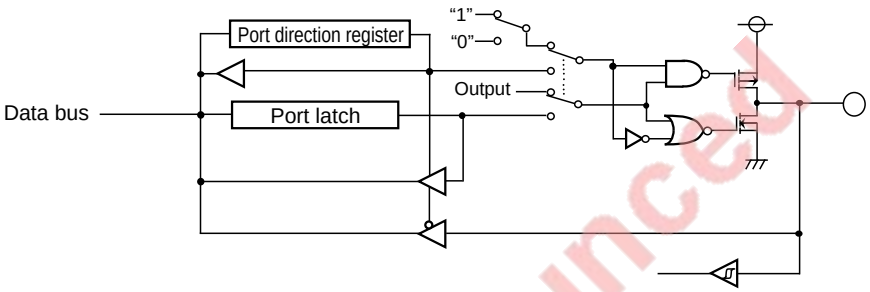
•Ports P7$_0$/AN$_0$ to P7$_7$/AN$_7$/XCIN

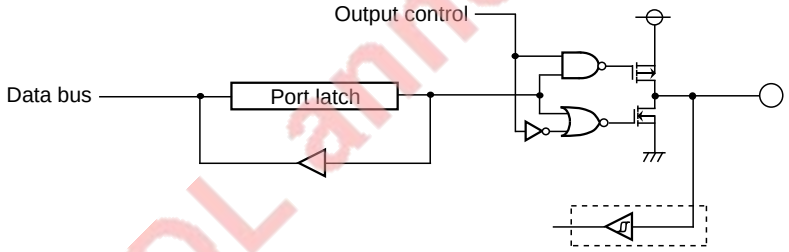


Note 2: The sub-clock oscillation circuit is present only in ports P7$_6$ and P7$_7$

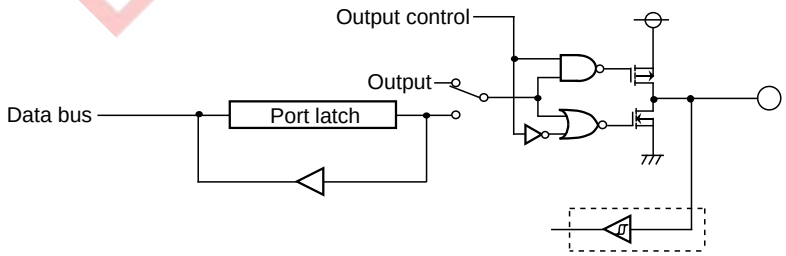
•Ports P8$_0$/$\overline{\text{CTS}_0}$/$\overline{\text{RTS}_0}$/CLKS$_1$, P8$_1$/CLK$_0$, P8$_4$/$\overline{\text{CTS}_1}$/$\overline{\text{RTS}_1}$, P8$_5$/CLK$_1$



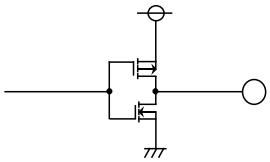
•Ports P9$_0$/$\overline{\text{CTS}_2}$, P9$_2$/RxD$_2$ (Inside dotted-line included)
Ports P9$_4$ to P9$_7$ (Inside dotted-line not included)



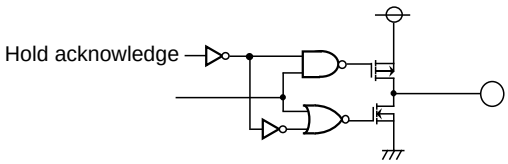
•Port P9$_1$/CLK$_2$ (Inside dotted-line included)
Port P9$_3$/TxD$_2$ (Inside dotted-line not included)



•$\overline{\text{E}}$ (External bus mode A)



•$\overline{\text{E}}$ / $\overline{\text{RDE}}$ (External bus mode B)



EOL announced

Fig. 3.2.2 Port peripheral circuits (2)

3.3 Pull-up function

3.3.1 Pull-up function for ports P10$_4$ to P10$_7$ ($\overline{KI_0}$ to $\overline{KI_3}$)

Ports P10$_4$ to P10$_7$ ($\overline{KI_0}$ to $\overline{KI_3}$) can be pulled high by setting the port P10 pull-up selection bit (bit 6 at address 6D$_{16}$). Figure 3.3.1 shows the structure of the port function control register.
When pulling ports P10$_4$ to P10$_7$ high, clear bits 4 to 7 at address 18$_{16}$ (Port P10 direction register) to “0.”

3.3.2 Pull-up function for ports P6$_2$ to P6$_4$ ($\overline{INT_0}$ to $\overline{INT_2}$)

Ports P6$_2$ and P6$_3$ ($\overline{INT_0}$ and $\overline{INT_1}$) can be pulled high by setting the port P6 pull-up selection bit 0 (bit 3 at address 6D$_{16}$). Port P6$_4$ ($\overline{INT_2}$) can be pulled high by setting the port P6 pull-up selection bit 1 (bit 5 at address 6D$_{16}$). Figure 3.3.1 shows the structure of the port function control register.
When pulling ports P6$_2$ to P6$_4$ high, clear bits 2 to 4 at address 10$_{16}$ (port P6 direction register) to “0.”

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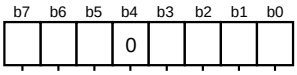


Port function control register (address $6D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Standby state selection bit	0: Pins P0 to P3 are used for the external bus output. 1: Pins P0 to P3 are used for the port output.	0	RW
1	Sub-clock output selection bit/ Timer B2 clock source selection bit	•Port-Xc selection bit* = "0" (when the sub clock is not used) Timer B2 (event counter mode) clock source selection **(Note 1)** 0: $TB2_{IN}$ input (event counter mode) 1: Main clock divided by 32 (clock timer) •Port-Xc selection bit = "1" (when the sub clock is used) Sub-clock output selection 0: Pin $P6_7/TB2_{IN}/\phi_{SUB}$ functions as a programmable I/O port. 1: Sub clock ϕ_{SUB} is output from pin $P6_7/TB2_{IN}/\phi_{SUB}$.	0	RW
2	Timer B1 internal connect selection bit **(Note 2)**	0: No internal connection 1: Internal connection with timer B2	0	RW
3	Port P6 pull-up selection bit 0	0: No pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$ 1: With pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$	0	RW
4	Must be fixed to "0."		0	RW
5	Port P6 pull-up selection bit 1	•Key input interrupt selection bit = "0" 0: No pull-up for pin $P6_4/\overline{INT_2}$ 1: With pull-up for pin $P6_4/\overline{INT_2}$ •Key input interrupt selection bit = "1" 0: Pin $P6_4/\overline{INT_2}$ is a port with no pull-up. 1: Pin $P6_4/\overline{INT_2}$ is an input pin with pull-up and is used for the key input interrupt.	0	RW
6	Port P10 pull-up selection bit	0: No pull-up for pins $P10_4/\overline{KI_0}$ to $P10_7/\overline{KI_3}$ 1: With pull-up for pins $P10_4/\overline{KI_0}$ to $P10_7/\overline{KI_3}$	0	RW
7	Key input interrupt selection bit	0: $\overline{INT_2}$ interrupt 1: Key input interrupt	0	RW

Port-Xc selection bit* : Bit 4 of the oscillation circuit control register 0 (address $6C_{16}$)

Notes 1: When the port-Xc selection bit = "0" and timer B2 operates in the timer mode or the pulse period /pulse width measurement mode, bit 1 is invalid.
2: When timer B1 operates in the event counter mode, bit 2 is valid.
3: ▭ represents that bits 0 to 2, 4 and 7 are not used for the pull-up function.

EOL announced

Fig. 3.3.1 Structure of port function control register

3.4 Internal peripheral devices' I/O functions (Ports P42, P5 to P8, P90 to P93 and P104 to P107)

Ports P42, P5 to P8, P90 to P93 and P104 to P107 also function as I/O pins for the internal peripheral devices. Table 3.4.1 lists correspondence between each port and internal peripheral devices' I/O pin. For internal peripheral devices' I/O functions, refer to the corresponding functional description. For the clock ϕ1 output pin, refer to chapter **"12. CONNECTING EXTERNAL DEVICES."** For the sub-clock oscillation circuit's I/O pins, refer to chapter **"14. CLOCK GENERATING CIRCUIT."**

Table 3.4.1 Correspondence between each port and internal peripheral devices' I/O pin

Port	Internal peripheral devices' I/O pin
P42	Clock ϕ1 output pin
P50, P60, P61	Timer A's I/O pins
P62 to P64	Input pins for external interrupts
P65, P66	Timer B's input pins
P67	Timer B's input pin/Clock ϕSUB output pin
P70, P75	A-D converter's input pins
P76, P77	A-D converter's input pins/Sub-clock oscillation circuit's I/O pins
P8, P90 to P93	I/O pins for serial I/O
P104 to P107	Input pins for the key input interrupt function

EOL announced

CHAPTER 4

INTERRUPTS

EOL announced

4.1 Overview
4.2 Interrupt sources
4.3 Interrupt control
4.4 Interrupt priority level
4.5 Interrupt priority level detection circuit
4.6 Interrupt priority level detection time
4.7 How interrupts are processed (from acceptance of interrupt request till execution of interrupt routine)
4.8 Return from interrupt routine
4.9 Multiple interrupts
4.10 External interrupts ($\overline{\text{INTi}}$ interrupt)
4.11 Precautions for interrupts

INTERRUPTS

Interrupts of the 7736 Group are the same as those of the 7733 Group. Therefore, for interrupts, refer to the corresponding sections in part 1:

- **“4.1 Overview (page 4-2 in part 1)**
- **“4.2 Interrupt sources (page 4-4 in part 1)**
- **“4.3 Interrupt control (page 4-6 in part 1)**
- **“4.4 Interrupt priority level (page 4-10 in part 1)**
- **“4.5 Interrupt priority level detection circuit (page 4-11 in part 1)**
- **“4.6 Interrupt priority level detection time (page 4-13 in part 1)**
- **“4.7 How interrupts are processed (from acceptance of interrupt request till execution of interrupt routine) (page 4-14 in part 1)**
- **“4.8 Return from interrupt routine (page 4-17 in part 1)**
- **“4.9 Multiple interrupts (page 4-17 in part 1)**
- **“4.10 External interrupts ($\overline{\text{INT}}_i$ interrupt) (page 4-19 in part 1)**
- **“4.11 Precautions for interrupts (page 4-23 in part 1)**

EOL announced

CHAPTER 5

KEY INPUT INTERRUPT FUNCTION

5.1 Overview
5.2 Block description
5.3 Initial setting example for related registers

EOL announced

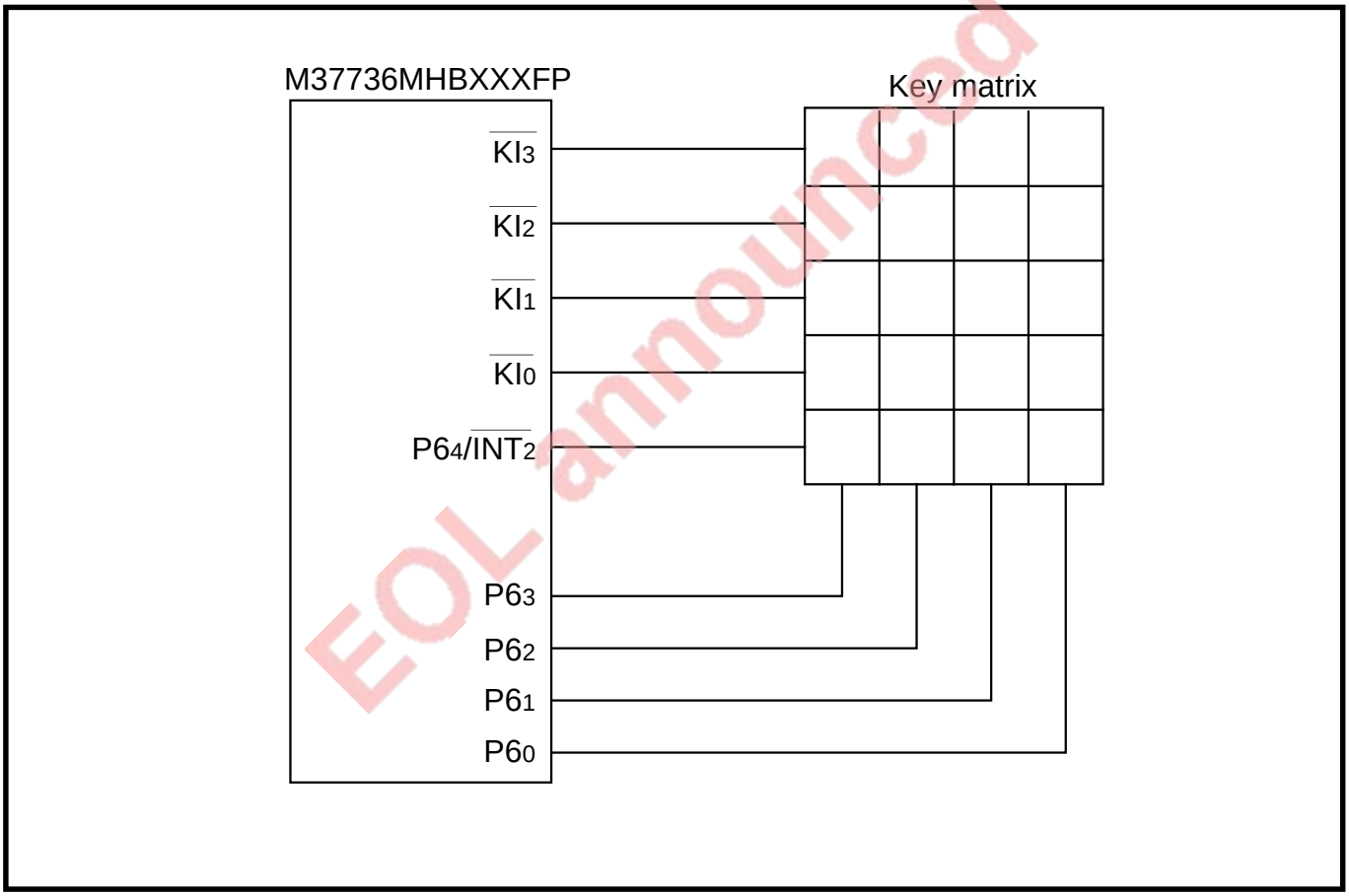
KEY INPUT INTERRUPT FUNCTION

5.1 Overview

The key input interrupt function is used to generate an interrupt request when one of the input levels of four or five pins falls. By using this function when terminating the stop or wait mode, the key-on wakeup can be realized.
For the way to terminate the stop or wait mode, refer to section **"17.4 Power saving."**
For the stop and wait modes, refer to chapter **"11. STOP AND WAIT MODES."**

5.1 Overview

A key input interrupt request occurs when one of the input levels of pins $\overline{KI_0}$ to $\overline{KI_3}$ falls. Therefore, by configuring an external key matrix shown in Figure 5.1.1, an interrupt request can be generated only by pushing a key. Pins $\overline{KI_0}$ to $\overline{KI_3}$ can be pulled high by software and the same function can also be selected for port $P6_4$. Therefore, when using the key input interrupt function, whether to use four pins (pins $\overline{KI_0}$ to $\overline{KI_3}$) or five pins (pins $\overline{KI_0}$ to $\overline{KI_3}$ and $P6_4$) can be selected.
The key input interrupt and the $\overline{INT_2}$ interrupt share the same interrupt vector addresses and interrupt control register.



EOL announced

Fig. 5.1.1 Key matrix example when key input interrupt function is used

5.2 Block description

Figure 5.2.1 shows the block diagram for the key input interrupt function.

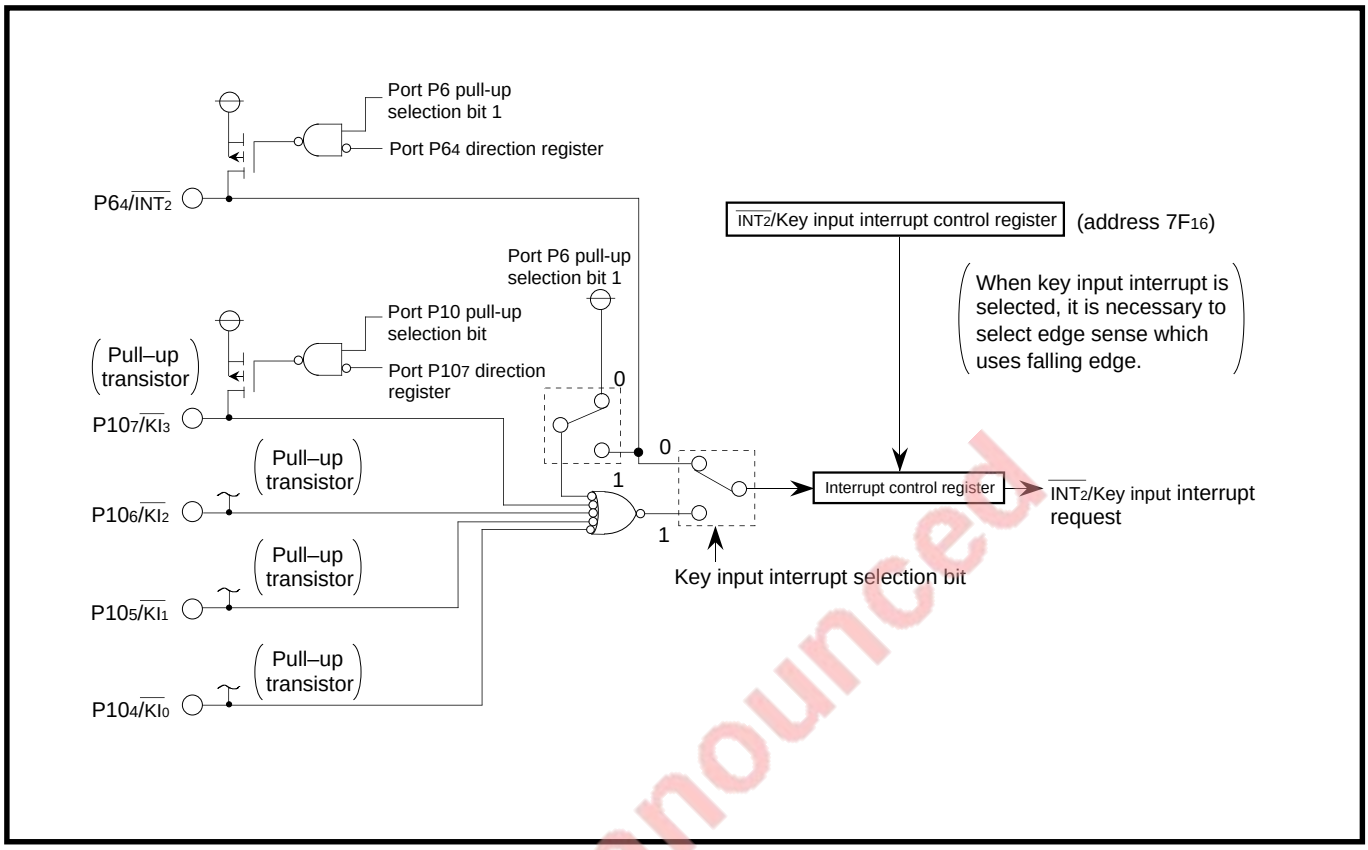


Fig. 5.2.1 Block diagram for key input interrupt function

5.2.1 Pins $\overline{KI_0}$ to $\overline{KI_3}$ and P64/$\overline{INT_2}$

When the key input interrupt function is selected, pins P104 to P107 become input pins for the key input interrupt ($\overline{KI_0}$ to $\overline{KI_3}$).

When selecting the key input interrupt function, clear all of bits 4 to 7 at address 18_{16} (Port P10 direction register) to "0."

When bits 4 to 7 at address 16_{16} (Port P10 register) are read out, the status of pins $\overline{KI_0}$ to $\overline{KI_3}$ can be read in. When using pin P64/$\overline{INT_2}$ as an input pin for the key input interrupt, set both of bits 5 and 7 at address $6D_{16}$ to "1" and bit 4 at address 10_{16} (Port P6 direction register) to "0." When bit 4 at address $E6_{16}$ (Port P6 register) is read out, the status of pin P64/$\overline{INT_2}$ can be read in.

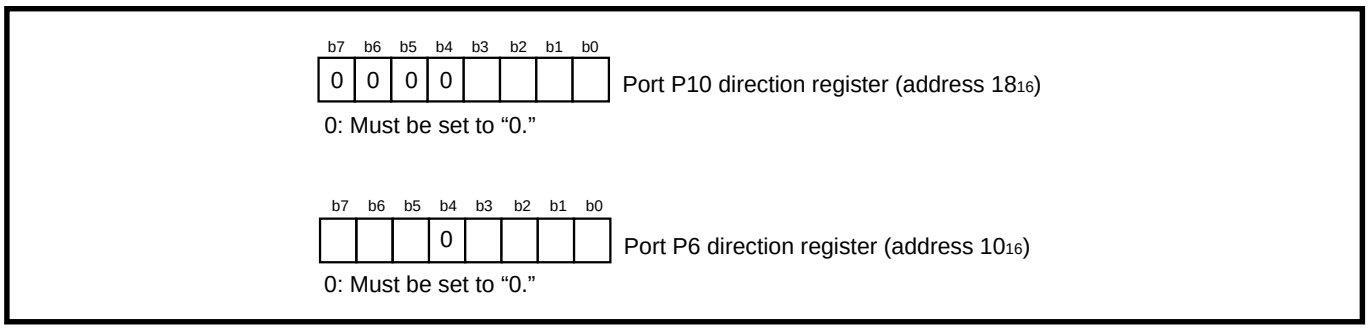


Fig. 5.2.2 Port P10 and P6 direction registers when key input interrupt function is selected

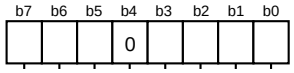
EOL announced

KEY INPUT INTERRUPT FUNCTION

5.2 Block description

5.2.2 Port function control register

Figure 5.2.3 shows the structure of the port function control register.



Port function control register (address $6D_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Standby state selection bit	0: Pins P0 to P3 are used for the external bus output. 1: Pins P0 to P3 are used for the port output.	0	RW
1	Sub-clock output selection bit/ Timer B2 clock source selection bit	•Port-Xc selection bit* = "0" (when the sub clock is not used) Timer B2 (event counter mode) clock source selection **(Note 1)** 0: $TB2_{IN}$ input (event counter mode) 1: Main clock divided by 32 (clock timer) •Port-Xc selection bit = "1" (when the sub clock is used) Sub-clock output selection 0: Pin $P6_7/TB2_{IN}/\phi_{SUB}$ functions as a programmable I/O port. 1: Sub clock ϕ_{SUB} is output from pin $P6_7/TB2_{IN}/\phi_{SUB}$.	0	RW
2	Timer B1 internal connect selection bit **(Note 2)**	0: No internal connection 1: Internal connection with timer B2	0	RW
3	Port P6 pull-up selection bit 0	0: No pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$ 1: With pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$	0	RW
4	Must be fixed to "0."		0	RW
5	Port P6 pull-up selection bit 1	•Key input interrupt selection bit = "0" 0: No pull-up for pin $P6_4/\overline{INT_2}$ 1: With pull-up for pin $P6_4/\overline{INT_2}$ •Key input interrupt selection bit = "1" 0: Pin $P6_4/\overline{INT_2}$ is a port with no pull-up. 1: Pin $P6_4/\overline{INT_2}$ is an input pin with pull-up and is used for the key input interrupt.	0	RW
6	Port P10 pull-up selection bit	0: No pull-up for pins $P10_4/\overline{KI_0}$ to $P10_7/\overline{KI_3}$ 1: With pull-up for pins $P10_4/\overline{KI_0}$ to $P10_7/\overline{KI_3}$	0	RW
7	Key input interrupt selection bit	0: $\overline{INT_2}$ interrupt 1: Key input interrupt	0	RW

Port-Xc selection bit* : Bit 4 of the oscillation circuit control register 0 (address $6C_{16}$)

Notes 1: When the port-Xc selection bit = "0" and timer B2 operates in the timer mode or the pulse period /pulse width measurement mode, bit 1 is invalid.
2: When timer B1 operates in the event counter mode, bit 2 is valid.
3: ▭ represents that bits 0 to 4 are not used for the key input interrupt function.

Fig. 5.2.3 Structure of port function control register

EOL announced

(1) Port P6 pull-up selection bit (bit 5)

When using pin P64/$\overline{INT_2}$ as an input pin for the key input interrupt, set this bit to "1." When this bit is set to "1," pin P64/$\overline{INT_2}$ is pulled high.

(2) Port P10 pull-up selection bit (bit 6)

This is a bit to pull pins $\overline{KI_0}$ to $\overline{KI_3}$ high. When configuring a key matrix, there is no need to connect pull-up transistors externally if this bit is set to "1," in other words, if pins $\overline{KI_0}$ to $\overline{KI_3}$ are set to be pulled high.

(3) Key input interrupt selection bit (bit 7)

This is a bit to select the key input interrupt function.

The key input interrupt and the $\overline{INT_2}$ interrupt share the same interrupt vector addresses and interrupt control register. When this bit is set to "1," the key input interrupt function is selected. When this bit = "1" and bit 5 (Port P6 pull-up selection bit) = "0," pin P6 4/$\overline{INT_2}$ is a programmable I/O port. (At this time, the $\overline{INT_2}$ interrupt cannot be used.) When both of this bit and bit 5 (Port P6 pull-up selection bit 1) are "1," pin P64/$\overline{INT_2}$ can be used for the key input interrupt.

EOL announced

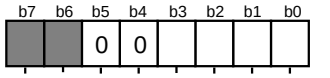
KEY INPUT INTERRUPT FUNCTION

5.2 Block description

5.2.3 Interrupt function

The key input interrupt and the $\overline{INT_2}$ interrupt share the same interrupt vector addresses and interrupt control register. Specify addresses FFF0$_{16}$ and FFF1$_{16}$ (in order words, the vector addresses for the $\overline{INT_2}$/key input interrupt) as the interrupt vector addresses; specify the $\overline{INT_2}$/key input interrupt control register (address 7F$_{16}$) as the interrupt control register. Figure 5.2.4 shows the structure of the $\overline{INT_2}$/key input interrupt control register when the key input interrupt function is selected.

The operation at accepting a key input interrupt request is the same as that at accepting an $\overline{INT_2}$ interrupt request.



$\overline{INT_2}$/key input interrupt control register (address 7F$_{16}$)

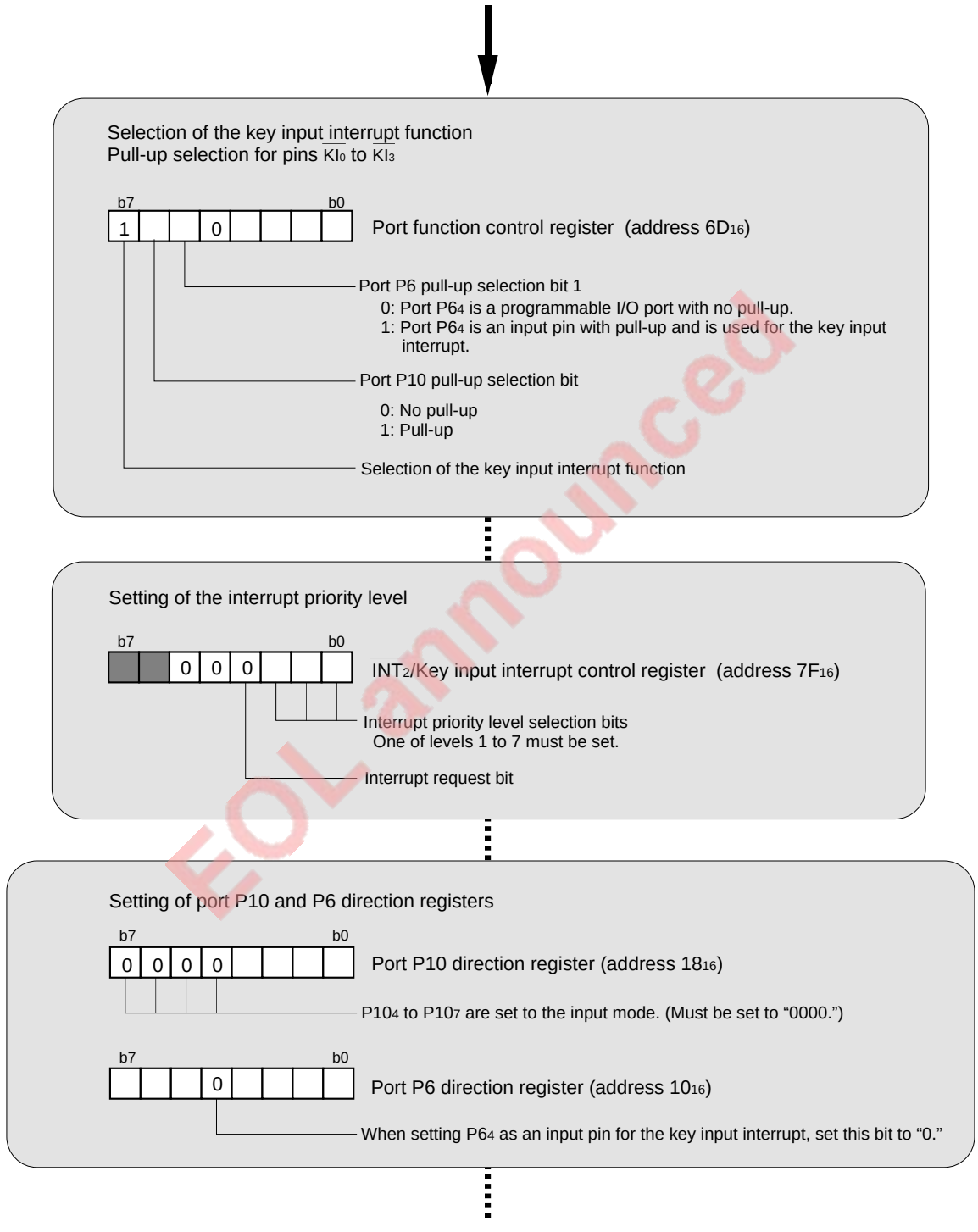
Bit	Bit name	Functions	At reset	RW
0	Interrupt priority level selection bits	b2 b1 b0 0 0 0: Level 0 (Interrupt is disabled.) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	0	RW
1			0	RW
2			0	RW
3	Interrupt request bit	0: No interrupt request has occurred. 1: Interrupt request has occurred.	0	RW
4	Must be fixed to "0."		0	RW
5			0	RW
6	Not implemented.		Undefined	—
7			Undefined	—

Fig. 5.2.4 Structure of $\overline{INT_2}$/key input interrupt control register when key input interrupt function is selected

EOL announced

5.3 Initial setting example for related registers

Figure 5.3.1 shows an initial setting example for registers related to the key input interrupt function.



EOL announced

❋ In order to enable the key input interrupt, the interrupt disable flag (I) must be set to "0" and the processor interrupt priority level (IPL) must be a value smaller than the INT2/key input interrupt's priority level. (Refer to chapter **"4. INTERRUPTS" in part 1.**)

Fig. 5.3.1 Initial setting example for registers related to key input interrupt function

5.3 Initial setting example for related registers

MEMO

EOL announced

CHAPTER 6

TIMER A

6.1 Overview
6.2 Block description
6.3 Timer mode
6.4 Event counter mode
6.5 One-shot pulse mode
6.6 Pulse width modulation (PWM) mode

EOL announced

TIMER A

Timer A of the 7736 Group is the same as that of the 7733 Group. Therefore, for timer A, refer to the corresponding sections in part 1:

- **“6.1 Overview” (page 6-2 in part 1)**
- **“6.2 Block description” (page 6-3 in part 1)**
- **“6.3 Timer mode” (page 6-9 in part 1)**
- **“6.4 Event counter mode” (page 6-19 in part 1)**
- **“6.5 One-shot pulse mode” (page 6-32 in part 1)**
- **“6.6 Pulse width modulation (PWM) mode” (page 6-41 in part 1)**

EOL announced

CHAPTER 7
TIMER B

7.1 Overview
7.2 Block description
7.3 Timer mode
7.4 Event counter mode
7.5 Pulse period/Pulse width measurement mode
7.6 Clock timer

EOL announced

TIMER B

Timer B of the 7736 Group is the same as that of the 7733 Group. Therefore, for timer B, refer to the corresponding sections in part 1:

- **“7.1 Overview” (page 7-2 in part 1)**
- **“7.2 Block description” (page 7-3 in part 1)**
- **“7.3 Timer mode” (page 7-10 in part 1)**
- **“7.4 Event counter mode” (page 7-17 in part 1)**
- **“7.5 Pulse period/Pulse width measurement mode” (page 7-25 in part 1)**
- **“7.6 Clock timer” (page 7-34 in part 1)**

EOL announced

CHAPTER 8

SERIAL I/O

8.1 Overview
8.2 Block description
8.3 Clock synchronous serial I/O mode
8.4 Clock asynchronous serial I/O (UART) mode

EOL announced

SERIAL I/O

8.2 Block description

In the 7736 Group, the UART2's input pins are independent of pins $P7_2$ to $P7_5$ and are multiplexed with pins $P9_0$ to $P9_3$. Therefore, concerning chapter "8. SERIAL I/O," the 7736 Group differs from the 7733 Group in the following sections. Only the differences are described in this chapter:

- **"8.2 Block description"**
- **"8.3 Clock synchronous serial I/O mode"**
- **"8.4 Clock asynchronous serial I/O (UART) mode"**

The following section of the 7736 Group is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"8.1 Overview"(page 8-2 in part 1)**

8.2 Block description

Concerning section "8.2 Block description," the 7736 Group differs from the 7733 Group in the following:

- **8.2.9 Port P8 direction register**

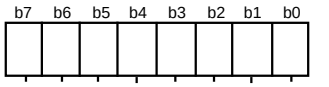
The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"8.2 Block description" (page 8-4 in part 1)**

EOL announced

8.2.9 Port P8 direction register

I/O pins of UARTi are multiplexed with ports P8 and P9. When using pins $P8_2$ and $P8_6$ as serial data input pins (RxDi), set the corresponding bits of the port P8 direction register to "0" to set this port for the input mode. When using pins $P8_0$, $P8_1$, $P8_3$–$P8_5$ and $P8_7$ as UARTi's I/O pins ($\overline{CTSi}/\overline{RTSi}$, CLKi, TxDi), these pins are forcibly set as the UARTi's I/O pins, regardless of the port P8 direction register's contents. Also, as for $CLKS_0$ and $CLKS_1$, refer to section **"8.3.1 (4) Number of transfer clock output pins (UART0)" in part 1.** Figure 8.2.16 shows the relationship between the port P8 direction register and UARTi's I/O pins.
When using UART2, pins $P9_0$–$P9_3$ are forcibly set as the UART2's input or output pins.
Note that the functions of the UARTi's I/O pins can be switched by software. For details, refer to the description of each operating mode.



Port P8 direction register (address 14_{16})

Bit	Corresponding pin name	Functions	At reset	RW
0	Pin $P8_0/\overline{CTS_0}/\overline{RTS_0}/CLKS_1$	0: Input mode 1: Output mode When using pins $P8_2$ and $P8_6$ as serial data's input pins (RxD_0, RxD_1), set the corresponding bits to "0."	0	RW
1	Pin $P8_1/CLK_0$		0	RW
2	Pin $P8_2/RxD_0/CLKS_0$		0	RW
3	Pin $P8_3/TxD_0$		0	RW
4	Pin $P8_4/\overline{CTS_1}/\overline{RTS_1}$		0	RW
5	Pin $P8_5/CLK_1$		0	RW
6	Pin $P8_6/RxD_1$		0	RW
7	Pin $P8_7/TxD_1$		0	RW

Note: For pins $CLKS_0$ and $CLKS_1$, refer to section **"8.3.1 (4) Number of transfer clock output pins (UART0)" in part 1.**

Fig. 8.2.16 Relationship between port P8 direction register and UARTi's I/O pins

EOL announced

8.3 Clock synchronous serial I/O mode

Concerning section "8.3 Clock synchronous serial I/O mode," the 7736 Group differs from the 7733 Group in the following:

- **Table 8.3.2**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"8.3 Clock synchronous serial I/O mode" (page 8-21 in part 1)**

Table 8.3.2 Functions of I/O pins in clock synchronous serial I/O mode

Pin name	Functions	Method of selection
TxDi (P8$_3$, P8$_7$, P9$_3$)	Serial data output	(They output dummy data when only reception is performed.)
RxD$_0$ (P8$_2$), RxD$_1$ (P8$_6$)	Serial data input	Port P8 direction register's corresponding bits ="0" (It can be used as an input port when only transmission is performed.)
RxD$_2$ (P9$_2$)		(It can be used as an output port when only transmission is performed.)
CLKi (P8$_1$, P8$_5$, P9$_1$)	Transfer clock output	Internal/External clock selection bit = "0"
	Transfer clock input	Internal/External clock selection bit = "1"
$\overline{CTS_0}$/$\overline{RTS_0}$ (P8$_0$), $\overline{CTS_1}$/$\overline{RTS_1}$ (P8$_4$) (**Note 1**)	$\overline{CTS}$ input	$\overline{CTS}$/$\overline{RTS}$ enable bit = "0" $\overline{CTS}$/$\overline{RTS}$ function selection bit = "0"
	$\overline{RTS}$ output	$\overline{CTS}$/$\overline{RTS}$ enable bit = "0" $\overline{CTS}$/$\overline{RTS}$ function selection bit = "1"
	Programmable I/O port	$\overline{CTS}$/$\overline{RTS}$ enable bit = "1"
$\overline{CTS_2}$ (P9$_0$)	$\overline{CTS}$ input	$\overline{CTS}$ enable bit = "0"
	Programmable I/O port	$\overline{CTS}$ enable bit = "1"

Port P8 direction register: Address 14$_{16}$
Internal/External clock selection bit: Bit 3 at addresses 30$_{16}$, 38$_{16}$, and 64$_{16}$
$\overline{CTS}$/$\overline{RTS}$ enable bit: Bit 4 at addresses 34$_{16}$ and 3C$_{16}$
$\overline{CTS}$/$\overline{RTS}$ function selection bit: Bit 2 at addresses 34$_{16}$ and 3C$_{16}$
$\overline{CTS}$ enable bit: Bit 2 at address 68$_{16}$

❋ Pin TxDi outputs "H" level from when a UARTi's operating mode is selected until transfer starts. (Pin TxDi is in a floating state when N-channel open-drain output is selected.)
❋ In UART0, multiple transfer clock output pins can be used. (Refer to **Table 8.3.3 in part 1.**)

Notes 1: The $\overline{RTS}$ output function is not assigned for UART2.
2: As for CLKS$_0$ and CLKS$_1$, refer to section **"8.3.1 (4) Number of transfer clock output pins (UART0)" in part 1.**

Preliminary Notification

8.4 Clock asynchronous serial I/O (UART) mode

Concerning section "8.4 Clock asynchronous serial I/O (UART) mode," the 7736 Group differs from the 7733 Group in the following:

- **Table 8.4.2**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"8.4 Clock asynchronous serial I/O (UART) mode" (page 8-44 in part 1)**

Table 8.4.2 Functions of I/O pins in UART mode

Pin name	Functions	Method of selection
TxDi (P8$_3$, P8$_7$, P9$_3$)	Serial data output	(They cannot be used as programmable I/O ports.)
RxD$_0$ (P8$_2$), RxD$_1$ (P8$_6$)	Serial data input	Port P8 direction register's corresponding bit = "0" (It can be used as an input port when only transmission is performed.)
RxD$_2$ (P9$_2$)	Serial data input	(It can be used as an output port when only transmission is performed.)
CLKi (P8$_1$, P8$_5$, P9$_1$)	Programmable I/O port	Internal/External clock selection bit = "0"
	BRGi count source input	Internal/External clock selection bit = "1"
$\overline{CTS_0}/\overline{RTS_0}$ (P8$_0$) $\overline{CTS_1}/\overline{RTS_1}$ (P8$_4$) **(Note)**	$\overline{CTS}$ input	$\overline{CTS}/\overline{RTS}$ enable bit = "0" $\overline{CTS}/\overline{RTS}$ function selection bit = "0"
	$\overline{RTS}$ output	$\overline{CTS}/\overline{RTS}$ enable bit = "0" $\overline{CTS}/\overline{RTS}$ function selection bit = "1"
	Programmable I/O port	$\overline{CTS}/\overline{RTS}$ enable bit = "1"
$\overline{CTS_2}$ (P9$_0$)	$\overline{CTS}$ input	$\overline{CTS}$ enable bit = "0"
	Programmable I/O port	$\overline{CTS}$ enable bit = "1"

Port P8 direction register: Address 14$_{16}$
Internal/External clock selection bit: Bit 3 at addresses 30$_{16}$, 38$_{16}$, and 64$_{16}$
$\overline{CTS}/\overline{RTS}$ enable bit: Bit 4 at addresses 34$_{16}$ and 3C$_{16}$
$\overline{CTS}/\overline{RTS}$ function selection bit: Bit 2 at addresses 34$_{16}$ and 3C$_{16}$
$\overline{CTS}$ enable bit: Bit 2 at addresses 68$_{16}$

❋ Pin TxDi outputs "H" level while not transmitting after a UARTi's operating mode is selected.
(Pin TxDi is in a floating state when N-channel open-drain output is selected.)

Note: The $\overline{RTSi}$ output function is not assigned for UART2.

ED announced

MEMO

EOL announced

CHAPTER 9

A-D CONVERTER

9.1 Overview
9.2 Block description
9.3 A-D conversion method
9.4 Absolute accuracy and Differential non-linearity error
9.5 One-shot mode
9.6 Repeat mode
9.7 Single sweep mode
9.8 Repeat sweep mode
9.9 Precautions for A-D converter

EOL announced

A-D CONVERTER

9.1 Overview

In the 7736 Group, the A-D converter's input pins are independent of UART2's I/O pins.
Therefore, concerning chapter "9. A-D CONVERTER," the 7736 Group differs from the 7733 Group in the following section. Only the differences are described in this chapter:

- **"9.2 Block description"**

The following sections of the 7736 group are the same as those of the 7733 Group. Therefore, refer to part 1:

- **"9.1 Overview" (page 9-2 in part 1)**
- **"9.3 A-D conversion method" (page 9-11 in part 1)**
- **"9.4 Absolute accuracy and Differential non-linearity error" (page 9-14 in part 1)**
- **"9.5 One-shot mode" (page 9-17 in part 1)**
- **"9.6 Repeat mode" (page 9-20 in part 1)**
- **"9.7 Single sweep mode" (page 9-23 in part 1)**
- **"9.8 Repeat sweep mode" (page 9-27 in part 1)**
- **"9.9 Precautions for A-D converter" (page 9-31 in part 1)**

9.2 Block description

Concerning section "9.2 Block description," the 7736 Group differs from the 7733 Group in the following:

- **9.2.5 Port P7 direction register**

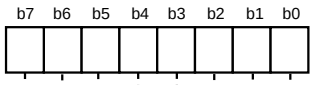
The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **"9.2 Block description" (page 9-3 in part 1)**

EOL announced

9.2.5 Port P7 direction register

Input pins of the A-D converter are multiplexed with port P7. When using these pins as A-D converter's input pins, set the corresponding bits of the port P7 direction register to "0" to set these ports for the input mode. Figure 9.2.6 shows the relationship between the port P7 direction register and I/O pins of the sub-clock oscillation circuit and peripheral functions.



Port P7 direction register (address 11_{16})

Bit	Corresponding bit's name	Functions	At reset	RW
0	Pin AN_0	0: Input mode 1: Output mode When using these pins as A-D converter's input pins, set the corresponding bits to "0."	0	RW
1	Pin AN_1		0	RW
2	Pin AN_2		0	RW
3	Pin AN_3		0	RW
4	Pin AN_4		0	RW
5	Pin $AN_5/\overline{ADTRG}$		0	RW
6	Pin AN_6/X_{COUT}		0	RW
7	Pin AN_7/X_{CIN}		0	RW

Fig. 9.2.6 Relationship between port P7 direction register and I/O pins of sub-clock oscillation circuit and peripheral functions

Analog input pins AN_6 and AN_7 function as the port P7's I/O pins and also function as I/O pins of the sub-clock oscillation circuit. For the pin which is forcedly set to the output mode when the function for the sub-clock oscillation circuit is selected, analog input is disabled. (Refer to **"Table 9.2.3."**)

Table 9.2.3 Port P7's pin which is forcedly set to output mode

Pin	Conditions where pin is forcedly set to output mode
$P7_6/AN_6/X_{COUT}$	Sub-clock oscillation circuit is operating by itself. (bit 4 at address $6C_{16}$ = "1" and bit 2 at address $6F_{16}$ = "0")

EOL announced

MEMO

EOL announced

CHAPTER 10
WATCHDOG TIMER

10.1 Block description
10.2 Operation description
10.3 Precautions for watchdog timer

EOL announced

WATCHDOG TIMER

10.2 Operation description

Concerning chapter “10. WATCHDOG TIMER,” the 7736 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

- **“10.2 Operation description”**

The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“10.1 Block description” (page 10-2 in part 1)**
- **“10.3 Precautions for watchdog timer” (page 10-10 in part 1)**

10.2 Operation description

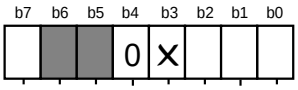
Concerning section “10.2 Operation description,” the 7736 Group differs from the 7733 Group in the following:

- **Figure 10.2.2**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“10.2 Operation description” (page 10-5 in part 1)**

EOL announced



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3	This bit is ignored.		1	RW
4	Must be fixed to “0” **(Note 2)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing “1” to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 10.2.3 in part 1.
2: The case where data “01010101_2” is written with the procedure shown in Figure 10.2.3 in part 1 is not included.
3: ▭ represents that bits 3 to 7 are not used for the watchdog timer.

Fig. 10.2.2 Structure of oscillation circuit control register 1

CHAPTER 11

STOP AND WAIT MODES

11.1 Overview
11.2 Clock generating circuit
11.3 Stop mode
11.4 Wait mode

EOL announced

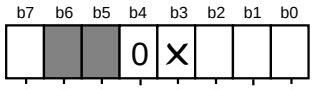
STOP AND WAIT MODES

11.2 Clock generating circuit

Concerning chapter “11. STOP AND WAIT MODES” of the 7736 Group, description differs depending on the external bus mode.
In external bus mode A, refer to the corresponding sections in part 1; in external bus mode B, refer to the corresponding sections in part 2. Note that, for the structure of the oscillation circuit control register 1, refer to **Figure 11.2.3 in part 3.**

- **“11.1 Overview”**
  External bus modes A and B (page 11-2 in part 1)
- **“11.2 Clock generating circuit”**
  External bus mode A (page 11-3 in part 1)
  External bus mode B (page 11-2 in part 2)
- **“11.3 Stop mode”**
  External bus mode A (page 11-6 in part 1)
  External bus mode B (page 11-3 in part 2)
- **“11.4 Wait mode”**
  External bus mode A (page 11-13 in part 1)
  External bus mode B (page 11-6 in part 2)

EOL announced



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3	This bit is ignored.		1	RW
4	Must be fixed to “0” **(Note 2)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing “1” to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 11.2.4 in part 1.
2: The case where data “01010101_2” is written with the procedure shown in Figure 11.2.4 in part 1 is not included.
3: ▭ represents that bits 3 to 7 are not used for the stop and wait modes.

Fig. 11.2.3 Structure of oscillation circuit control register 1

CHAPTER 12

CONNECTING EXTERNAL DEVICES

12.1 Signals required for accessing external devices
12.2 Software wait
12.3 Ready function
12.4 Hold function

EOL announced

CONNECTING EXTERNAL DEVICES

Concerning chapter “12. CONNECTING EXTERNAL DEVICES,” the 7736 Group differs depending on the external bus mode.
In external bus mode A, refer to the corresponding sections in part 1; in external bus mode B, refer to the corresponding sections in part 2.

- **“12.1 Signals required for accessing external devices”**
  External bus mode A (12-2 in part 1)
  External bus mode B (page 12-3 in part 2)
- **“12.2 Software wait”**
  External bus mode A (page 12-13 in part 1)
  External bus mode B (page 12-16 in part 2)
- **“12.3 Ready function”**
  External bus mode A (page 12-16 in part 1)
  External bus mode B (page 12-19 in part 2)
- **“12.4 Hold function”**
  External bus mode A (page 12-19 in part 1)
  External bus mode B (page 12-23 in part 2)

EOL announced

CHAPTER 13
RESET

13.1 Hardware reset
13.2 Software reset

EOL announced

RESET

13.1 Hardware reset

Concerning chapter “RESET,” the 7736 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

• “**13.1 Hardware reset**”

The following section of the 7736 Group is the same as that of the 7733 Group. Therefore, for this section, refer to part 1:

• **“13.2 Software reset” (page 13-12 in part 1)**

13.1 Hardware reset

Concerning section “13.1 Hardware reset,” the 7736 Group differs from the 7733 Group in the following:

• **Table 13.1.1**

• **Figure 13.1.6 for external bus mode B (Note)**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

• **“13.1 Hardware reset” (page 13-2 in part 1)**

Note: In external bus mode A, Figure 13.1.6 of the 7736 Group is the same as that of the 7733 Group.

Table 13.1.1 Pin state while pin $\overline{\text{RESET}}$ is at “L” level

	Pin CNVss's level	Pin (Port) name	Pin state
Mask ROM version	Vss or Vcc	P0 to P10	Floating
		$\overline{\text{E}}/\overline{\text{RDE}}$	“H” level is output.
Built-in PROM version	Vss	P0 to P10	Floating
		$\overline{\text{E}}/\overline{\text{RDE}}$	“H” level is output.
	Vss	P0, P1, P3 to P10	Floating
		P2	•Floating when “H” level is applied to both or one of pins $P5_1$ and $P5_2$ •“H” or “L” level is output when “L” level is applied to both of pins $P5_1$ and $P5_2$.
		$\overline{\text{E}}/\overline{\text{RDE}}$	“H” level is output.

EOL announced

Figure 13.1.6 for the 7736 Group differs from that for the 7733 Group only in bit 3 at address 6F16.

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
6016	Watchdog timer register	WO	? (*1)
6116	Watchdog timer frequency selection flag	RW	? 0
6216	(Reserved area) *3		?
6316	Memory allocation control register	RW	? 0 0 0 0 0
6416	UART2 transmit/receive mode register	RW	? 0 0 0 0 0 0 0
6516	UART2 baud rate register (BRG2)	WO	?
6616	UART2 transmission buffer register	WO	?
6716		WO	?
6816	UART2 transmit/receive control register 0	RO RW	? 1 0 0 0
6916	UART2 transmit/receive control register 1	RO RW RO RW	0 0 0 0 0 0 1 0
6A16	UART2 receive buffer register	RO	?
6B16		RO	0 0 0 0 0 0 0 ?
6C16	Oscillation circuit control register 0	RW(*2) RW	? 0 0 0 0 0 ? 1
6D16	Port function control register	RW	0 0 0 0 0 0 0 0
6E16	Serial transmit control register	RW	? 0 0 ?
6F16	Oscillation circuit control register 1	WO RW	0 ? 0 *3 0 0 0
7016	A-D / UART2 trans./rece. interrupt control register	RW	? 0 0 0 0
7116	UART0 transmission interrupt control register	RW	? 0 0 0 0
7216	UART0 receive interrupt control register	RW	? 0 0 0 0
7316	UART1 transmission interrupt control register	RW	? 0 0 0 0
7416	UART1 receive interrupt control register	RW	? 0 0 0 0
7516	Timer A0 interrupt control register	RW	? 0 0 0 0
7616	Timer A1 interrupt control register	RW	? 0 0 0 0
7716	Timer A2 interrupt control register	RW	? 0 0 0 0
7816	Timer A3 interrupt control register	RW	? 0 0 0 0
7916	Timer A4 interrupt control register	RW	? 0 0 0 0
7A16	Timer B0 interrupt control register	RW	? 0 0 0 0
7B16	Timer B1 interrupt control register	RW	? 0 0 0 0
7C16	Timer B2 interrupt control register	RW	? 0 0 0 0
7D16	$\overline{INT_0}$ interrupt control register	RW	? 0 0 0 0 0 0
7E16	$\overline{INT_1}$ interrupt control register	RW	? 0 0 0 0 0 0
7F16	$\overline{INT_2}$/Key input interrupt control register	RW	? 0 0 0 0 0 0

FOL announced

*1 Value "FFF16" is set to the watchdog timer. (Refer to chapter **"10. WATCHDOG TIMER" in part 1.**)
*2 For access characteristics at address 6C16, also refer to **Figure 14.3.2 in part 1.**
*3 Do not write data to address 6216.

■Internal RAM area (M37736MHBXXXFP: addresses 8016 to FFF16)

- At hardware reset
  (not including the case where the stop or wait mode is terminated)...Undefined.
- At software reset...Retains the state immediately before reset.
- When the stop or wait mode is terminated
  (when hardware reset is applied)...Retains the state immediately before the **STP** or **WIT** instruction is executed.

Fig. 13.1.6 State of SFR area and internal RAM area immediately after reset (4)

RESET

13.1 Hardware reset

MEMO

EOL announced

CHAPTER 14

CLOCK GENERATING CIRCUIT

14.1 Overview
14.2 Oscillation circuit example
14.3 Clock control

EOL announced

CLOCK GENERATING CIRCUIT

14.3 Clock control

Concerning chapter “14. CLOCK GENERATING CIRCUIT,” the 7736 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

- **“14.3 Clock control”**

The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“14.1 Overview” (page 14-2 in part 1)**
- **“14.2 Oscillation circuit example” (page 14-3 in part 1)**

14.3 Clock control

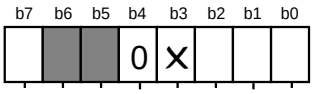
Concerning section “14.3 Clock control,” the 7736 Group differs from that of the 7733 Group in the following:

- **Figure 14.3.3**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1.

- **“14.3 Clock control” (page 14-5 in part 1)**

EOL announced



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3	This bit is ignored.		1	RW
4	Must be fixed to “0” **(Note 2)**.		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing “1” to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 14.3.4 in part 1.
2: The case where data “01010101_2” is written with the procedure shown in Figure 14.3.4 in part 1 is not included.
3: ☐ represents that bits 3 to 7 are not used for the clock generating circuit.

Fig. 14.3.3 Structure of oscillation circuit control register 1

CHAPTER 15
ELECTRICAL CHARACTERISTICS

EOL announced

15.1 Absolute maximum ratings
15.2 Recommended operating conditions
15.3 Electrical characteristics
15.4 A-D converter characteristics
15.5 Internal peripheral devices
15.6 Ready and Hold
15.7 Single-chip mode
15.8 Memory expansion mode and Microprocessor mode : with no wait
15.9 Memory expansion mode and Microprocessor mode : with wait 1
15.10 Memory expansion mode and Microprocessor mode : with wait 0
15.11 Measuring circuit for ports P0 to P10 and pins ϕ_1 and $\overline{E}$

ELECTRICAL CHARACTERISTICS

15.1 Absolute maximum ratings

Electrical characteristics of the M37736MHBXXXGP are described in this chapter.

Concerning chapter "15. ELECTRICAL CHARACTERISTICS," the 7736 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **"15.1 Absolute maximum ratings"**
- **"15.2 Recommended operating conditions"**
- **"15.3 Electrical characteristics"**
- **"15.7 Single-chip mode"**
- **"15.11 Measuring circuit for ports P0 to P10 and pins ϕ_1 and $\overline{E}$"**

The following sections of the 7736 Group differ depending on the external bus mode. In external bus mode A, refer to the corresponding sections in part 1; in external bus mode B, refer to the corresponding sections in part 2.

- **"15.6 Ready and Hold"**
  External bus mode A (page 15-11 in part 1)
  External bus mode B (page 15-3 in part 2)
- **"15.8 Memory expansion mode and Microprocessor mode : with no wait"**
  External bus mode A (page 15-15 in part 1)
  External bus mode B (page 15-5 in part 2)
- **"15.9 Memory expansion mode and Microprocessor mode : with wait 1"**
  External bus mode A (page 15-17 in part 1)
  External bus mode B (page 15-7 in part 2)
- **"15.10 Memory expansion mode and Microprocessor mode : with wait 0"**
  External bus mode A (page 15-19 in part 1)
  External bus mode B (page 15-9 in part 2)

The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **"15.4 A-D converter characteristics" (page 15-5 in part 1)**
- **"15.5 Internal peripheral devices" (page 15-6 in part 1)**

EOL announced

15.1 Absolute maximum ratings

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to 7	V
AVcc	Analog power source voltage		–0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to 12	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, V_{REF}, X_{IN}, BSEL		–0.3 to Vcc+0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$, X_{OUT}, $\overline{E}$		–0.3 to Vcc+0.3	V
P_d	Power dissipation	Ta = 25 °C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 150	°C

15.2 Recommended operating conditions

Recommended operating conditions (Vcc = 5 V ± 10 %, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Power source voltage	$f(X_{IN})$:Operating	4.5	5.0	5.5	V
		$f(X_{IN})$:Stopped, $f(X_{CIN})$ = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL, X_{CIN} **(Note 3)**	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL, X_{CIN} **(Note 3)**	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0		0.16 Vcc	V
$I_{OH\ (peak)}$	High-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$			–10	mA
$I_{OH\ (avg)}$	High-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$			–5	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_4$–$P10_7$			10	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P4_4$–$P4_7$, $P10_0$–$P10_3$			20	mA
$I_{OL\ (avg)}$	Low-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_4$–$P10_7$			5	mA
$I_{OL\ (avg)}$	Low-level average output current	$P4_4$–$P4_7$, $P10_0$–$P10_3$			15	mA
$f(X_{IN})$	Main-clock oscillation frequency **(Note 4)**				25	MHz
$f(X_{CIN})$	Sub-clock oscillation frequency			32.768	50	kHz

EOL announced

Notes 1: Average output current is the average value in an interval of 100 ms.

2: The sum of I_{OL}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH}(peak) for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL}(peak) for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I_{OH}(peak) for ports P4, P5, P6, and P7 must be 80 mA or less.

3: Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1."

4: The maximum value of $f(X_{IN})$ = 12.5 MHz when the main clock division selection bit = "1."

ELECTRICAL CHARACTERISTICS

15.3 Electrical characteristics

15.3 Electrical characteristics

Electrical characteristics (Vcc = 5 V, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz, unless otherwise noted)

Symbol	Parameter		Measuring conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$	I_{OH} = –10 mA	3			V
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	I_{OH} = –400 μA	4.7			V
V_{OH}	High-level output voltage	$P3_0$–$P3_2$	I_{OH} = –10 mA	3.1			V
			I_{OH} = –400 μA	4.8			
V_{OH}	High-level output voltage	$\overline{E}$	I_{OH} = –10 mA	3.4			V
			I_{OH} = –400 μA	4.8			
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_5$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_4$–$P10_7$	I_{OL} = 10 mA			2	V
V_{OL}	Low-level output voltage	$P4_4$–$P4_7$, $P10_0$–$P10_3$	I_{OL} = 20 mA			2	V
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	I_{OL} = 2 mA			0.45	V
V_{OL}	Low-level output voltage	$P3_0$–$P3_2$	I_{OL} = 10 mA			1.9	V
			I_{OL} = 2 mA			0.43	
V_{OL}	Low-level output voltage	$\overline{E}$	I_{OL} = 10 mA			1.6	V
			I_{OL} = 2 mA			0.4	
V_{T+}–V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$–$TA4_{IN}$, $TB0_{IN}$–$TB2_{IN}$, $\overline{INT0}$–$\overline{INT2}$, $\overline{ADTRG}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS2}$, $CLK0$, $CLK1$, $CLK2$, $\overline{KI0}$–$\overline{KI3}$		0.4		1	V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$		0.2		0.5	V
V_{T+}–V_{T-}	Hysteresis	X_{IN}		0.1		0.4	V
V_{T+}–V_{T-}	Hysteresis	X_{CIN} (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL	V_I = 5 V			5	μA
I_{IL}	Low-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_3$, $P6_0$, $P6_1$, $P6_5$– $P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_3$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL	V_I = 0 V			–5	μA
I_{IL}	Low-level input current	$P6_2$–$P6_4$, $P10_4$–$P10_7$,	V_I = 0 V, without a pull-up transistor			–5	μA
			V_I = 0 V, with a pull-up transistor	–0.25	–0.5	–1.0	mA
V_{RAM}	RAM hold voltage		When clock is stopped	2			V

Not announced

ELECTRICAL CHARACTERISTICS (Vcc= 5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	In single-chip mode, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, $f(X_{IN})$ = 25 MHz (Square waveform), ($f(f_2)$ = 12.5 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating **(Note 1)**		9.5	19	mA
			Vcc = 5V, $f(X_{IN})$ = 25 MHz (Square waveform), ($f(f_2)$ = 1.5625 MHz), $f(X_{CIN})$: Stopped, in operating **(Note 1)**		1.3	2.6	mA
			Vcc = 5V, $f(X_{IN})$ = 25 MHz (Square waveform), $f(X_{CIN})$ = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		10	20	μA
			Vcc = 5 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, in operating **(Note 3)**		50	100	μA
			Vcc = 5 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		5	10	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop selection bit at wait state = "1."

3: This is applied when the CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

ECL announced

15.7 Single-chip mode

Timing requirements (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	40		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	15		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns
$t_{su(P0D–E)}$	Port P0 input setup time	60		ns
$t_{su(P1D–E)}$	Port P1 input setup time	60		ns
$t_{su(P2D–E)}$	Port P2 input setup time	60		ns
$t_{su(P3D–E)}$	Port P3 input setup time	60		ns
$t_{su(P4D–E)}$	Port P4 input setup time	60		ns
$t_{su(P5D–E)}$	Port P5 input setup time	60		ns
$t_{su(P6D–E)}$	Port P6 input setup time	60		ns
$t_{su(P7D–E)}$	Port P7 input setup time	60		ns
$t_{su(P8D–E)}$	Port P8 input setup time	60		ns
$t_{su(P10D–E)}$	Port P10 input setup time	60		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns
$t_{h(E–P10D)}$	Port P10 input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.

2: When the main clock division selection bit = "1," the minimum value of tc = 80 ns.

3: When the main clock division selection bit = "1," values of $tw_{(H)}$/tc and $tw_{(L)}$/tc must be set to values from 0.45 through 0.55.

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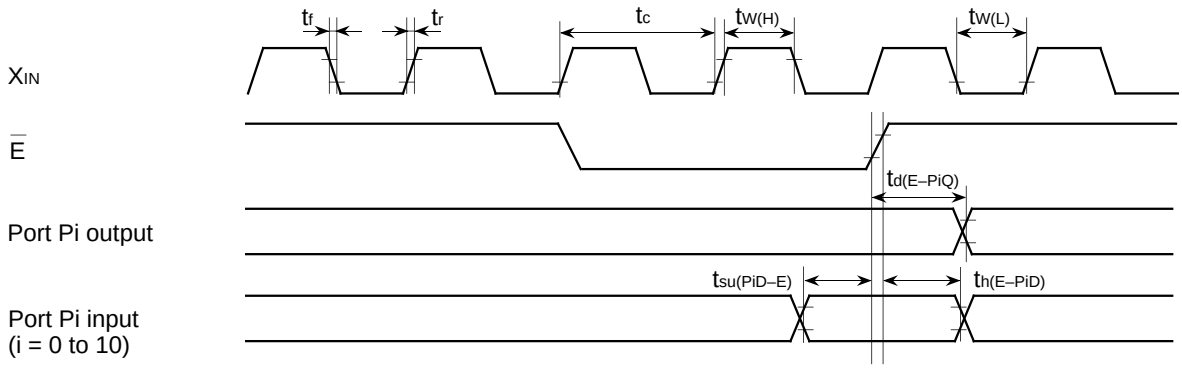
Switching characteristics (Vcc = 5 V ± 10 %, Vss = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 25 MHz **(Note)**, unless otherwise noted)

Symbol	Parameter	Measuring conditions	Limits		Unit
			Min.	Max.	
$t_{d(E–P0Q)}$	Port P0 data output delay time	Fig. 15.11.1		80	ns
$t_{d(E–P1Q)}$	Port P1 data output delay time			80	ns
$t_{d(E–P2Q)}$	Port P2 data output delay time			80	ns
$t_{d(E–P3Q)}$	Port P3 data output delay time			80	ns
$t_{d(E–P4Q)}$	Port P4 data output delay time			80	ns
$t_{d(E–P5Q)}$	Port P5 data output delay time			80	ns
$t_{d(E–P6Q)}$	Port P6 data output delay time			80	ns
$t_{d(E–P7Q)}$	Port P7 data output delay time			80	ns
$t_{d(E–P8Q)}$	Port P8 data output delay time			80	ns
$t_{d(E–P9Q)}$	Port P9 data output delay time			80	
$t_{d(E–P10Q)}$	Port P10 data output delay time			80	

Note: This is applied when the main clock division selection bit = "0" and f(f_2) = 12.5 MHz.

Single-chip mode



Measuring conditions

- V_{CC} = 5 V ± 10 %
- Input timing voltage : V_{IL} = 1.0 V, V_{IH} = 4.0 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

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15.11 Measuring circuit for ports P0 to P10 and pins ϕ_1 and $\overline{E}$

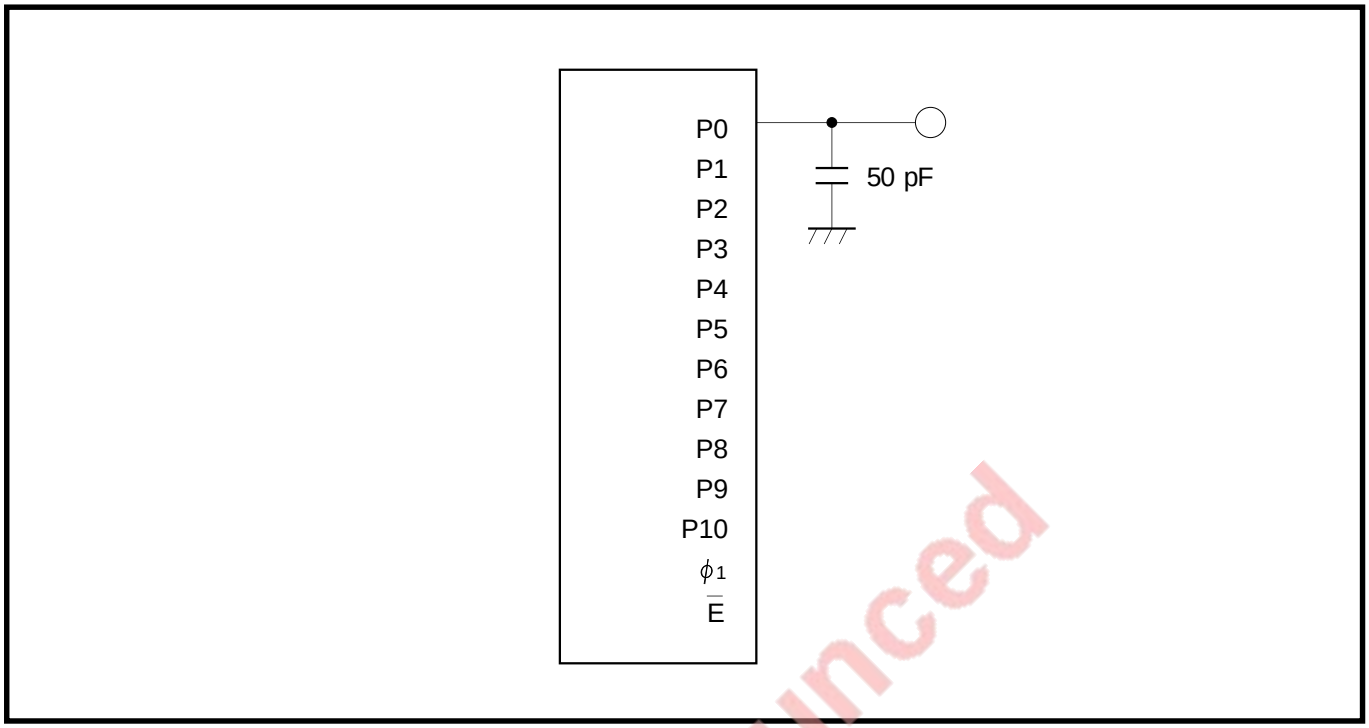


Fig. 15.11.1 Measuring circuit for ports P0 to P10 and pins ϕ_1 and $\overline{E}$

EOL announced

CHAPTER 16

STANDARD CHARACTERISTICS

16.1 Standard characteristics

EOL announced

STANDARD CHARACTERISTICS

16.1 Standard characteristics

Concerning chapter “16. STANDARD CHARACTERISTICS,” the 7736 Group differs from the 7733 Group in the following sections. Therefore, only the deferences are described in this chapter:

- **“16.1.1 Programmable I/O port (CMOS output) standard characteristics: P0 to P3, $P4_0$ to $P4_3$, P5 to P9, and $P10_4$ to $P10_7$**
- **“16.1.2 Programmable I/O port (CMOS output) standard characteristics: $P4_4$ to $P4_7$ and $P10_0$ to $P10_3$**

The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“16.1.3 Icc–f(X_{IN}) standard characteristics” (page 16-4 in part 1)**
- **“16.1.4 A-D converter standard characteristics” (page 16-5 in part 1)**

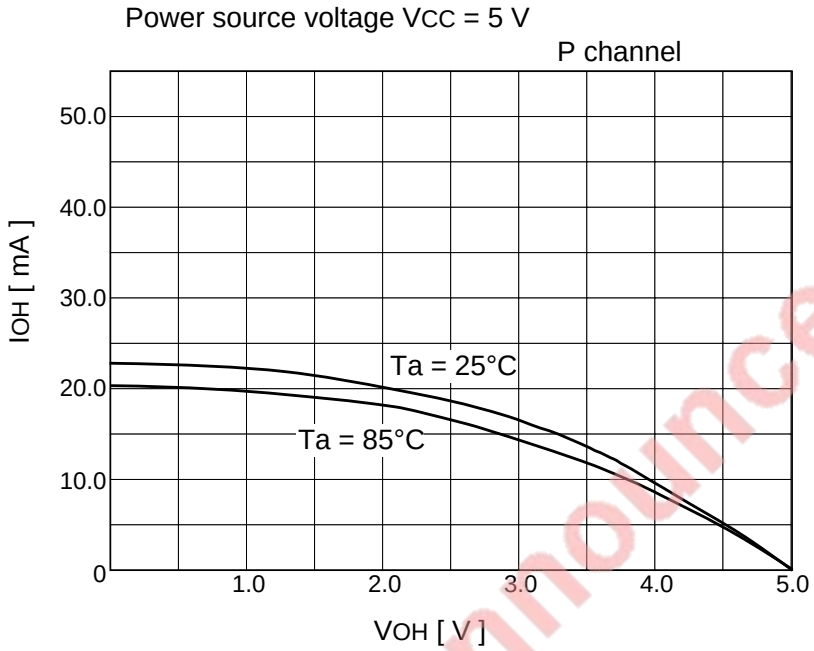
EOL announced

16.1 Standard characteristics

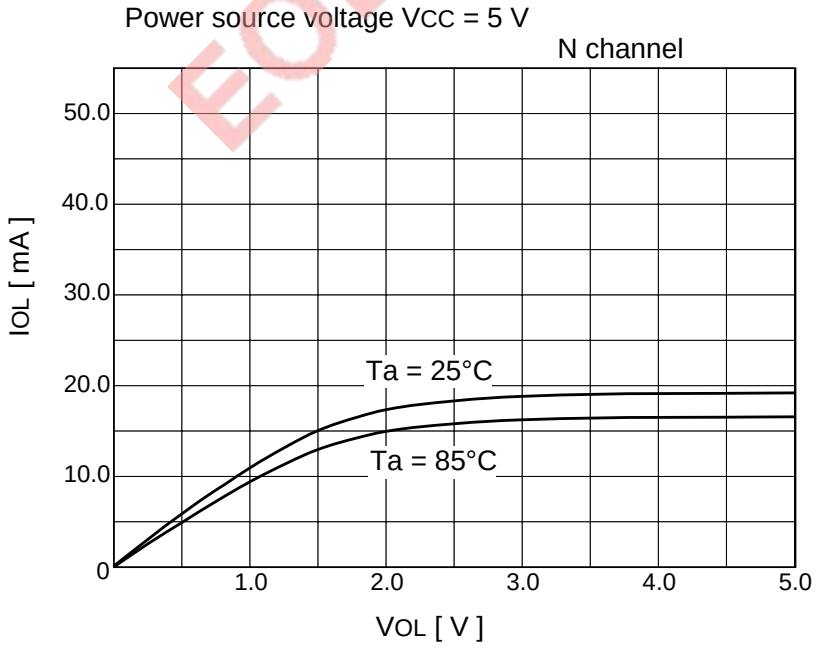
Standard characteristics described below are characteristic examples of the M37736MHBXXXGP and are not guaranteed. For each parameter's limits, refer to chapter **"15. ELECTRICAL CHARACTERISTICS."**

16.1.1 Programmable I/O port (CMOS output) standard characteristics: P0 to P3, $P4_0$ to $P4_3$, P5 to P9, and $P10_4$ to $P10_7$

(1) P-channel I_{OH}–V_{OH} characteristics



(2) N-channel I_{OL}–V_{OL} characteristics



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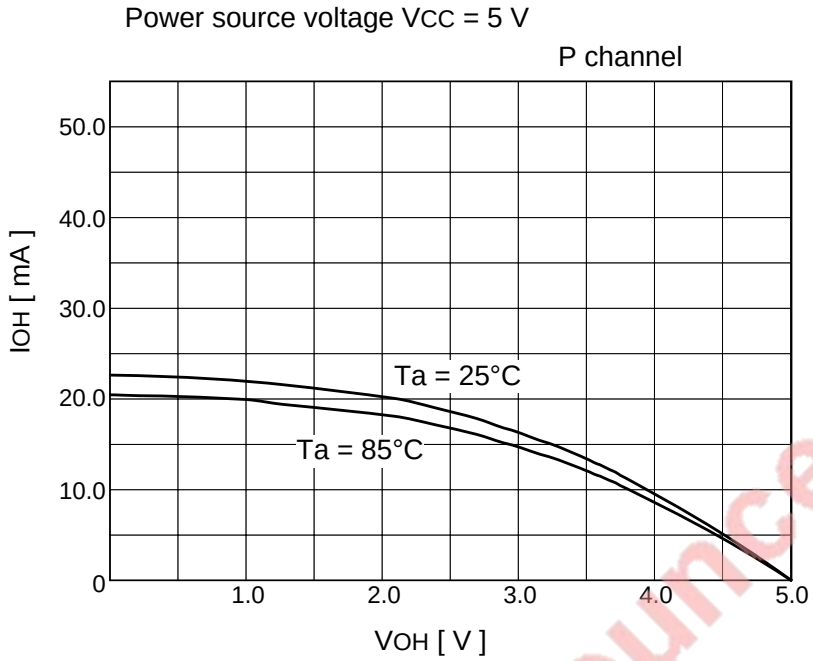
STANDARD CHARACTERISTICS

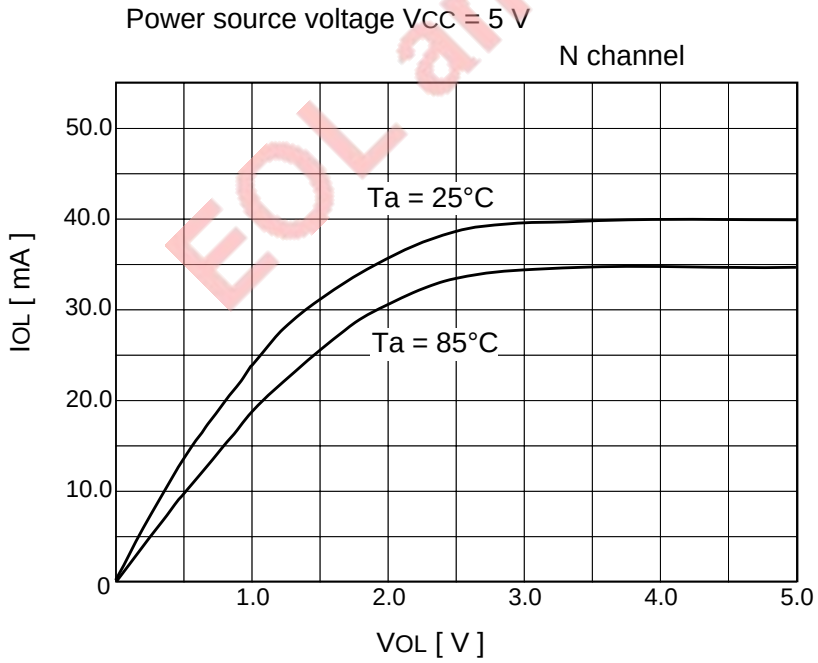
16.1 Standard characteristics

16.1.2 Programmable I/O port (CMOS output) standard characteristics: $P4_4$ to $P4_7$ and $P10_0$ to $P10_3$

(1) P-channel I_{OH}–V_{OH} characteristics



(2) N-channel I_{OL}–V_{OL} characteristics



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CHAPTER 17
APPLICATIONS

17.1 Memory expansion
17.2 Serial I/O
17.3 Watchdog timer
17.4 Power saving
17.5 Timer B

EOL announced

APPLICATIONS

Concerning chapter “17. APPLICATIONS,” the 7736 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

- **“17.4 Power saving”**

The following section of the 7736 Group differs depending on the external bus mode, which is A or B:

- **“17.1 Memory expansion”**
  External bus mode A (page 17–2 in part 1)
  External bus mode B (page 17–2 in part 2)

The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“17.2 Serial I/O” (page 17–28 in part 1)**
- **“17.3 Watchdog timer” (page 17–41 in part 1)**
- **“17.5 Timer B” (page 17–54 in part 1)**

EOL announced

17.4 Power saving

Power saving examples (in other words, examples to save power consumption) with the stop or wait mode used in external bus mode A are described below. The following examples differ from examples in external bus mode B only in external bus pins allocated to ports P0 to P3. Therefore, for power saving in external bus mode B, refer to this section.

17.4.1 Power saving example with stop mode used

In this example, power saving is realized by using the stop mode. The stop mode is terminated by using the key input interrupt function.

(1) Specifications

① The microcomputer operates in the single-chip mode.
② Pins $P10_0$ to $P10_3$ are used as output pins for the key matrix scanning.
Input pins ($\overline{KI0}$ to $\overline{KI3}$) for the key input interrupt function are used as key input pins.
Pins $\overline{KI0}$ to $\overline{KI3}$ are pulled high by using the pull-up function.
③ The initial output levels of pins $P10_0$ to $P10_3$ are “L.”
④ When a key input interrupt request occurs owing to a key push, the key data is read-in. (This reading is surely performed independent of power saving.)
⑤ In the stop mode, interrupts other than a key input interrupt are disabled.
⑥ An external clock is used as the main clock.

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APPLICATIONS

17.4 Power saving

(2) Initial settings for related registers

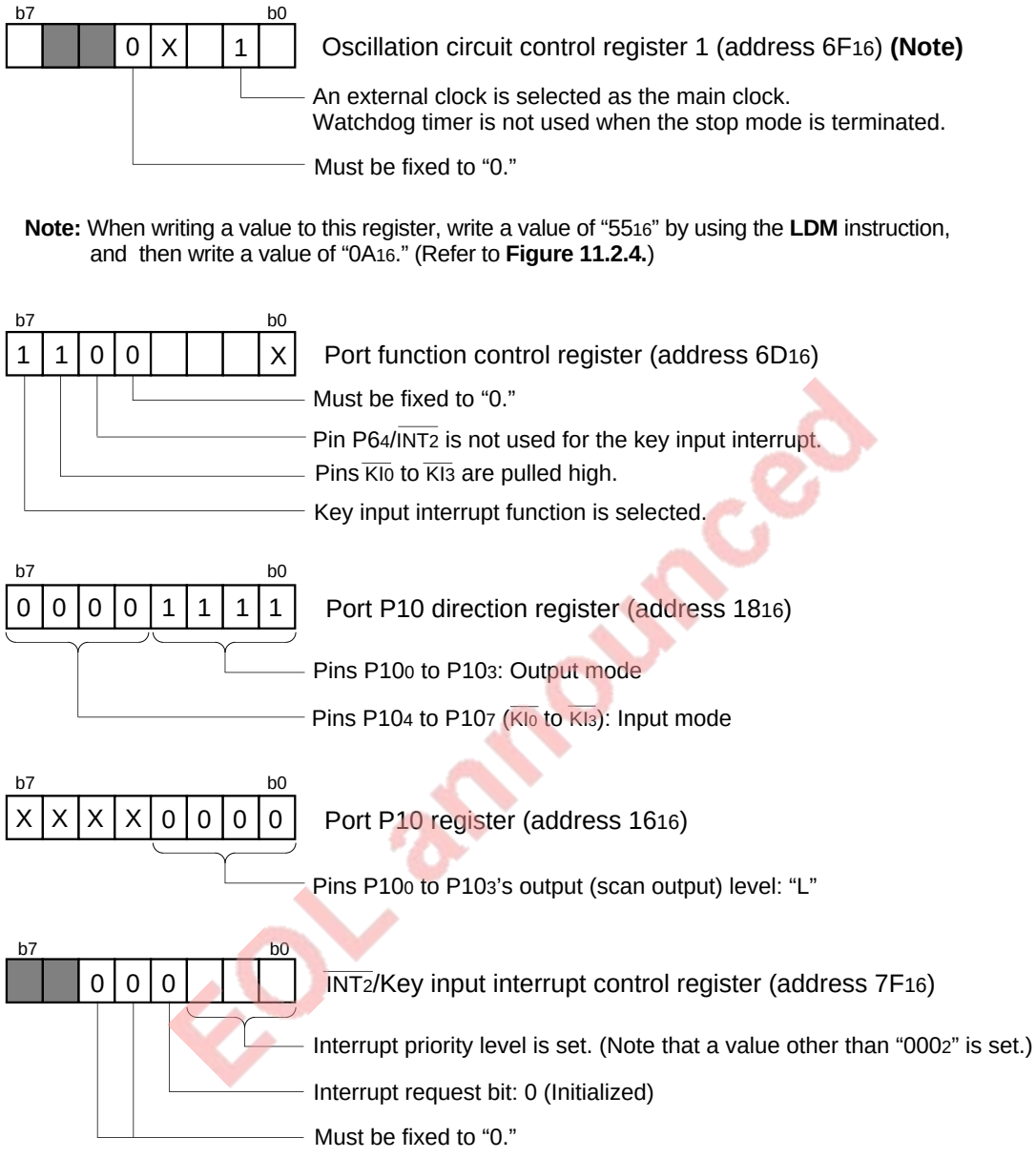

Fig. 17.4.1 Initial settings for related registers

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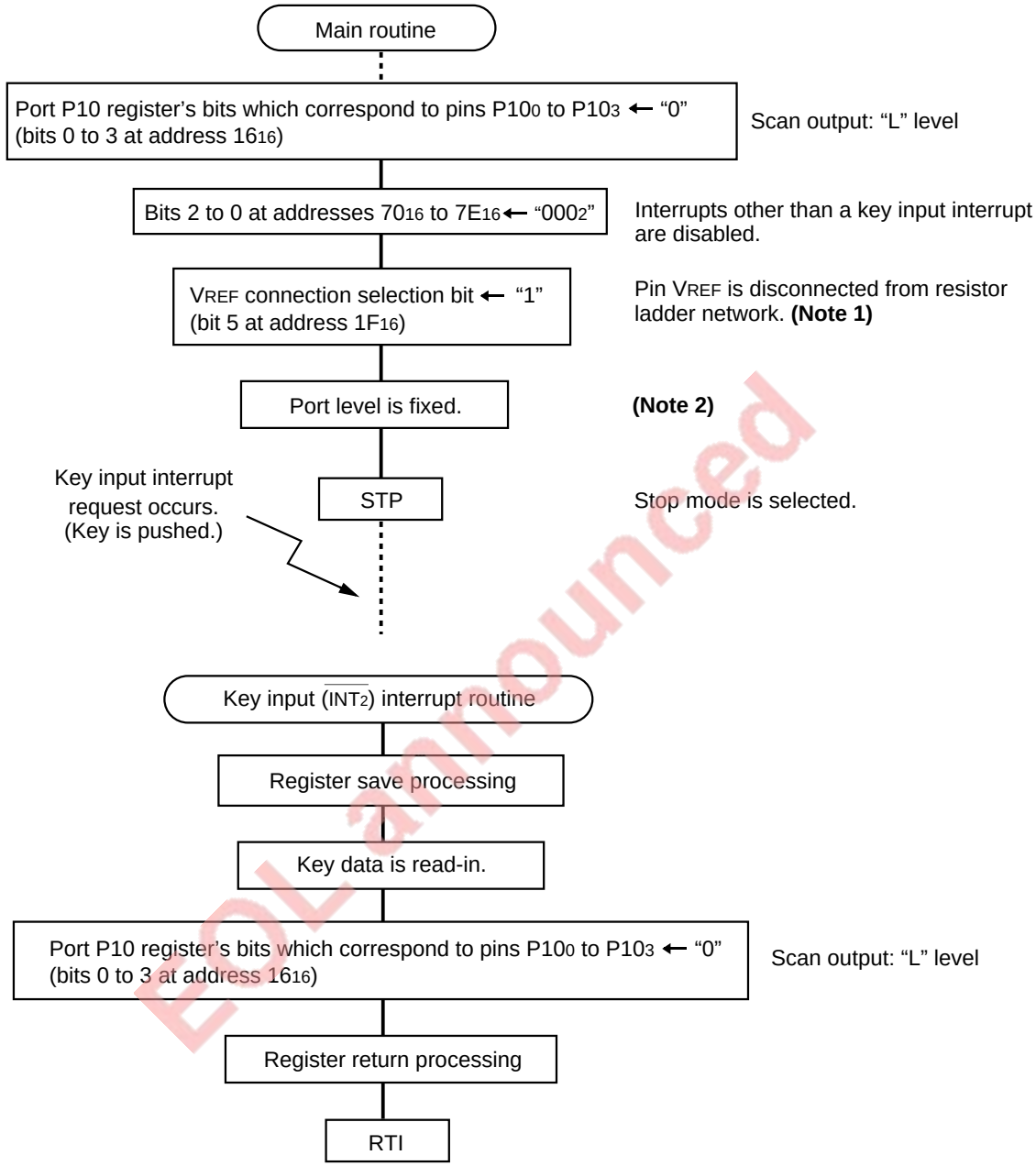
(3) Approximate flowchart



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Notes 1: When pin V_{REF} and resistor ladder network are connected, current flows into the resistor ladder network. When using the A-D converter after the stop mode is terminated, do as follows:
q Reconnect pin V_{REF} and resistor ladder network.
w And then, start A-D conversion after a period of 1 μs or more passed.

2: When a port is connected to an external device and so on, there is a possibility that current consumption increases according to the port's level. In order to avoid this problem, do as follows:
•When output mode is selected: Fix the port's level to a level where no current flows into the external.
•When input mode is selected : Pull the port high or low via a resistor. (Floating state is disabled.)

Fig. 17.4.2 Approximate flowchart

17.4 Power saving

(4) Settings for performing power saving in memory expansion or microprocessor mode

In the memory expansion or microprocessor mode, when saving power consumption, it is necessary to fix the I/O pins' levels of the external bus and bus control signals in the stop mode. For this purpose, set the standby state selection bit to "1."

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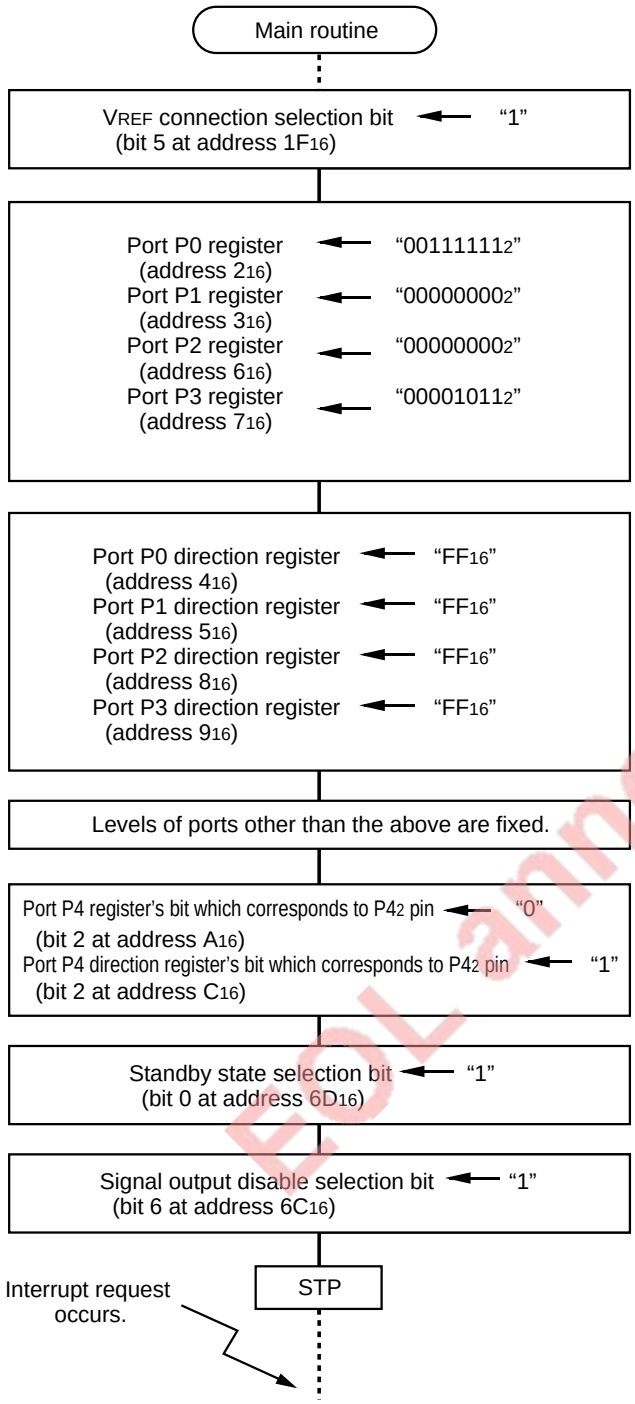

Pin VREF is disconnected from resistor ladder network.

I/O pins' levels of external bus, chip-select signals and bus control signals in the stop mode are set.
(These levels can be set by the corresponding port register's bits.)
In this example, I/O pins for "L"-active signals are set to "H" and the other pins are set to "L."

Ports which correspond to I/O pins of external bus, chip-select signals and bus control signals: Output mode
(This setting is done in order to output a value set to a port register in the stop mode)

Pin ϕ_1's state in the stop mode is set **(Note)**.
In this example, "L" level output is set.

Standby state selection bit: "1"
(In the stop mode, a value which is set to the corresponding port register is output from an I/O pin of the external bus, chip-select signals or bus control signals.)

Pin $\overline{E}$'s output level in the stop mode is set.
In this example, it is set to "L."

Stop mode is selected.

Note: Regardless of this setting, in the following cases, pin ϕ_1 outputs "L" level in the stop mode:
- When the signal output disable selection bit is set to "0" in the microprocessor mode
- When the clock ϕ_1 output selection bit is set to "1" in the memory expansion mode

Fig. 17.4.3 Fixing I/O pins' levels of external bus and bus control signals (Microprocessor mode)

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APPLICATIONS

17.4 Power saving

17.4.2 Power saving example with wait mode used

In this example, power saving is realized by using the wait mode. While power is saved, the clock function is realized by using the clock timer (Timer B2).

(1) Specifications

① The microcomputer operates in the single-chip mode.
② The frequency of the sub clock (f(XCIN)) = 32.768 kHz. An external clock is used as the sub clock.
③ Clock counting is performed by using the clock timer. (An interrupt request occurs every second.)
④ When an $\overline{INT_0}$ interrupt request occurs **(Note)**, the wait mode is terminated.
Note: An interrupt request occurs at every falling edge of the signal input from pin $\overline{INT_0}$.
⑤ In the wait mode, interrupts other than the following interrupts are disabled.
•Timer B2 interrupt
•$\overline{INT_0}$ interrupt
⑥ An external input is used as the main clock.

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(2) Initial settings for related registers

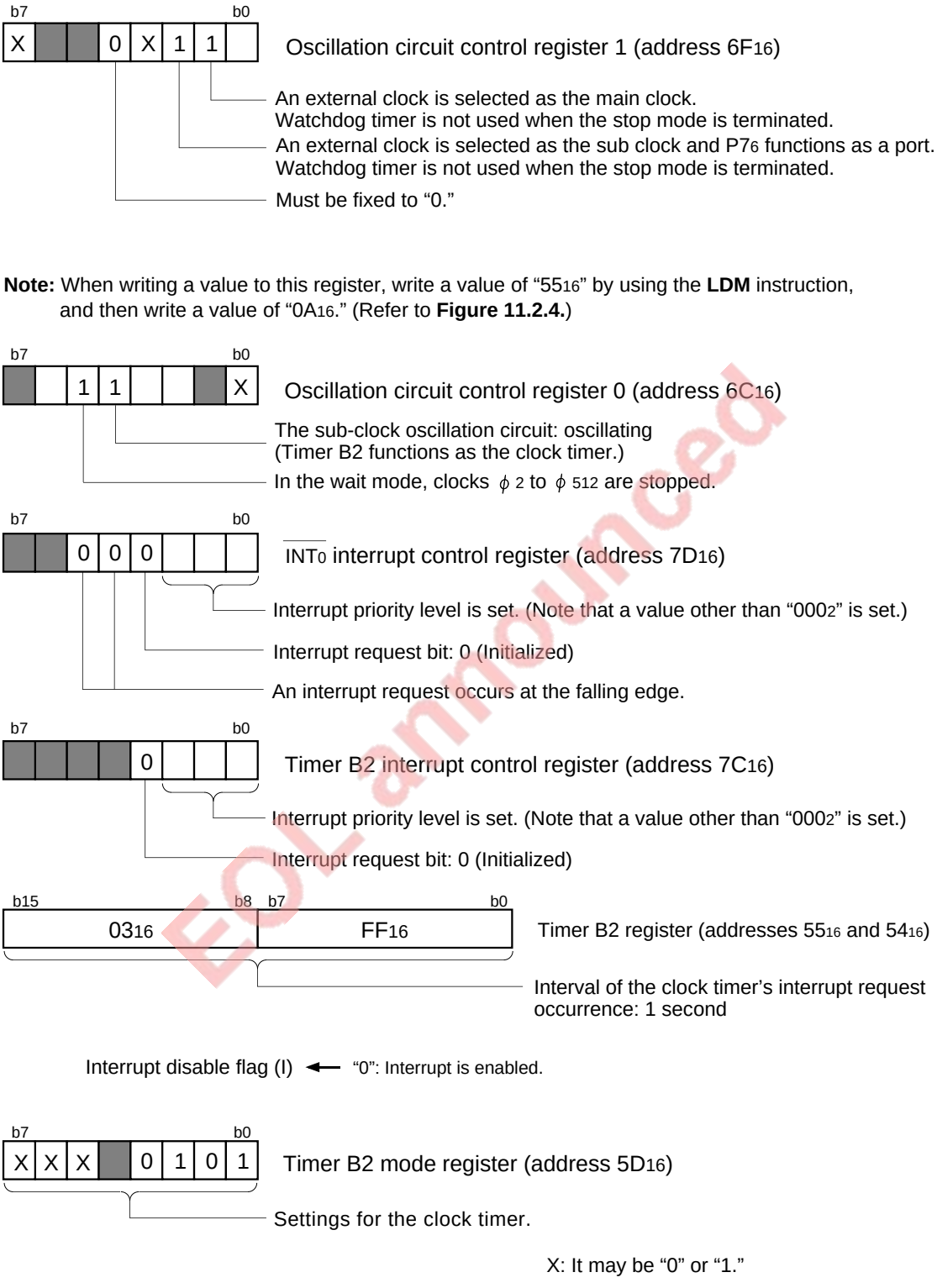

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Fig. 17.4.4 Initial settings for related registers

APPLICATIONS

17.4 Power saving

(3) Approximate flowchart

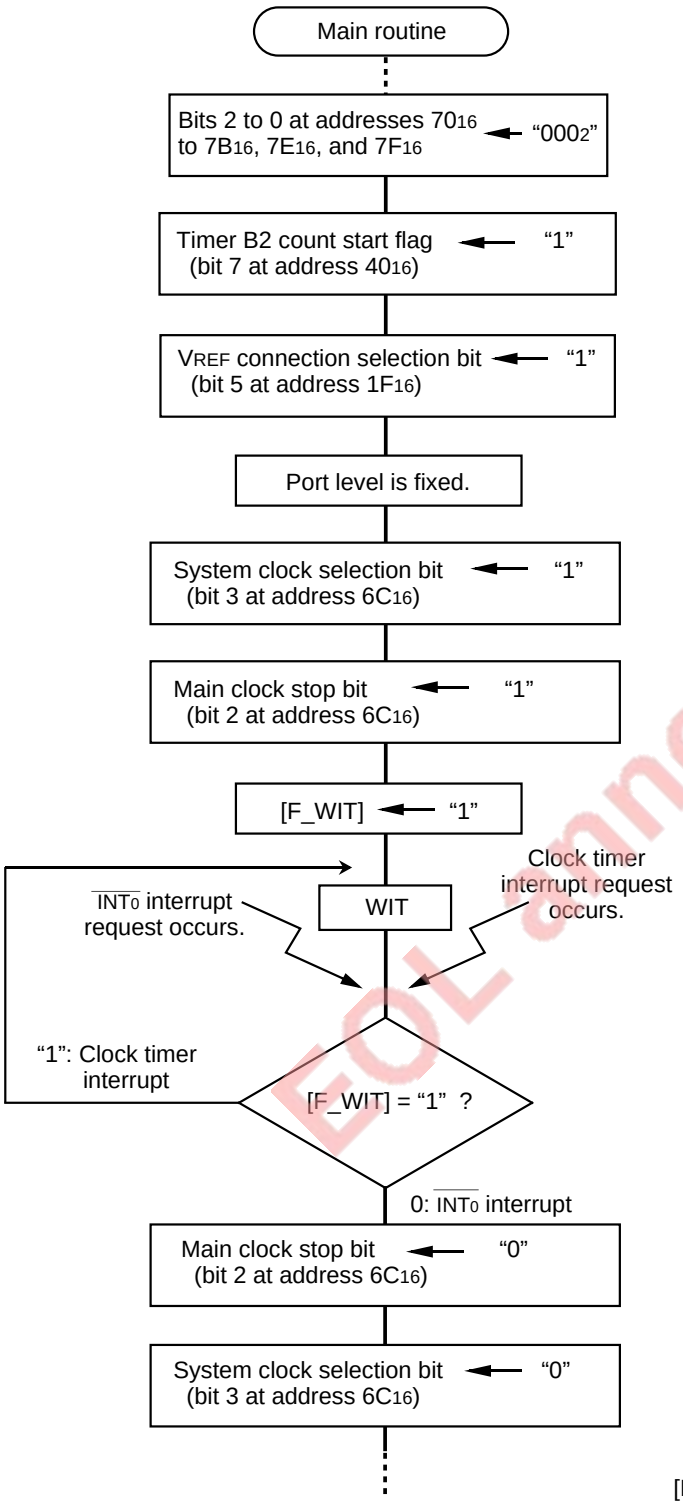

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Fig. 17.4.5 Approximate flowchart (1)

Notes 1: When pin V_{REF} and resistor ladder network are connected, current flows into the resistor ladder network.
When using the A-D converter after the wait mode is terminated, do as follows:
q Reconnect pin V_{REF} and resistor ladder network.
w And then, start A-D conversion after a period of 1 µs or more passed.

2: When a port is connected to an external device and so on, there is a possibility that current consumption increases according to the port's level.
In order to avoid this problem, do as follows:
•When output mode is selected: Fix the port's level to a level where no current flows into the external.
•When input mode is selected: Pull the port high or low via a resistor. (Floating state is disabled.)

3: Do not switch the system clock until oscillation of a clock which is input from the external is stabilized.

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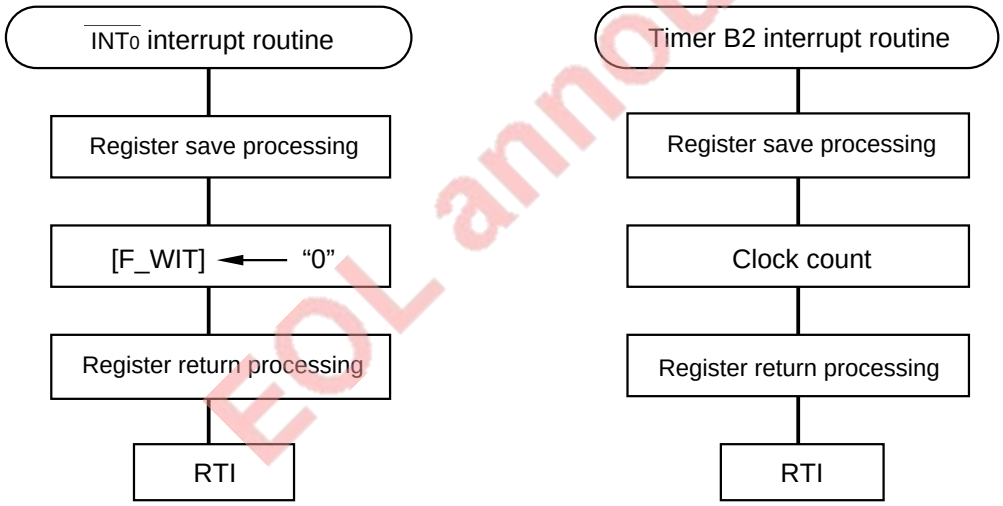

[F_WIT]: Flag used to determine whether an $\overline{INT_0}$ interrupt request has occurred or not

Fig. 17.4.6 Approximate flowchart (2)

APPLICATIONS

17.4 Power saving

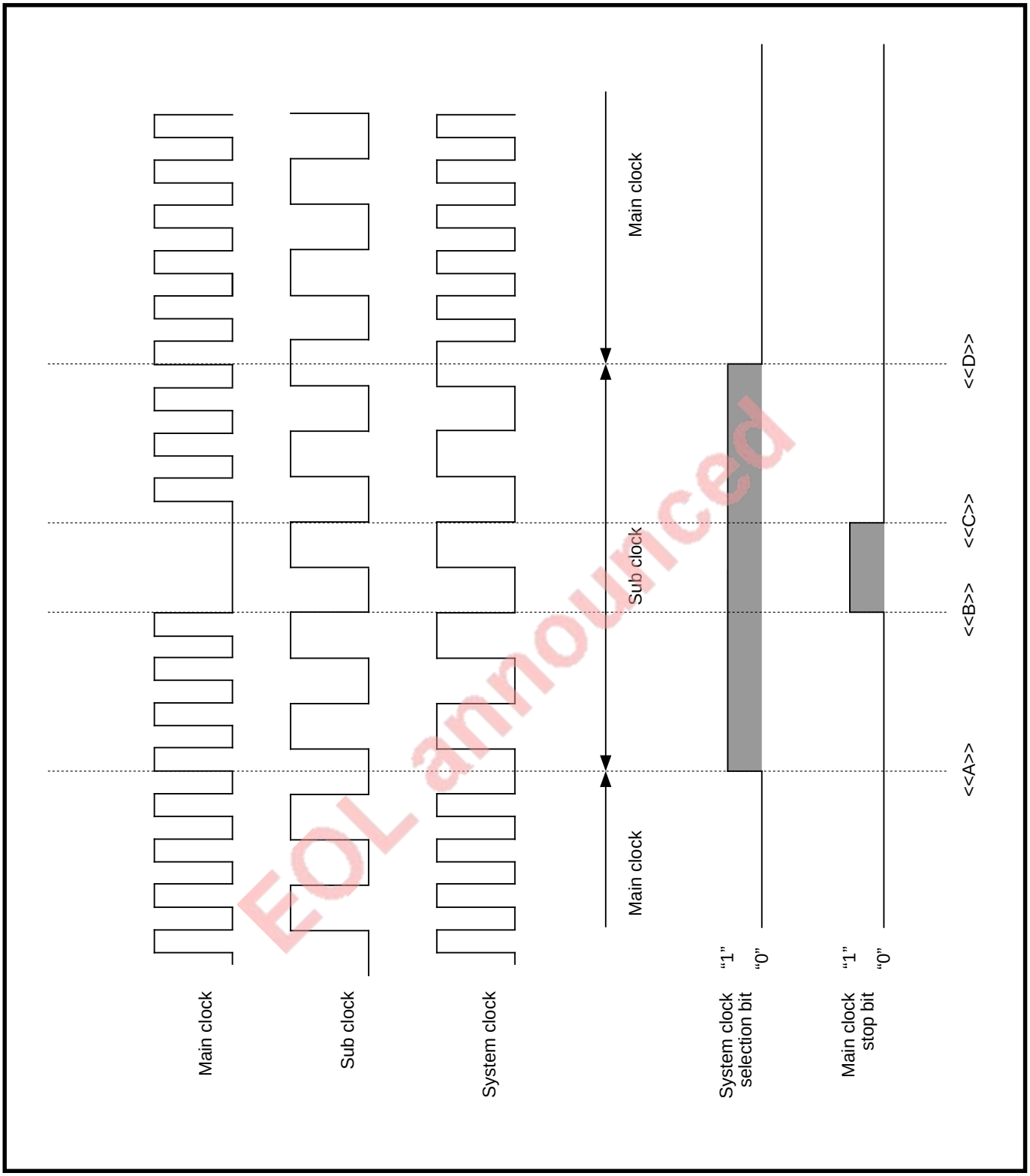

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Fig. 17.4.7 State of main clock, sub clock, and system clock

CHAPTER 18
LOW VOLTAGE VERSION

18.1 Performance overview
18.2 Pin configuration
18.3 Functional description
18.4 Electrical characteristics
18.5 Standard characteristics
18.6 Applications

EOL announced

LOW VOLTAGE VERSION

Concerning chapter “18. LOW VOLTAGE VERSION,” the 7736 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this chapter:

- **“18.1 Performance overview”**
- **“18.2 Pin configuration”**
- **“18.3 Functional description”**
- **“18.4 Electrical characteristics”**
- **“18.5 Standard characteristics”**
- **“18.6 Applications”**

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18.1 Performance overview

Concerning section “18.1 Performance overview,” the 7736 Group differs from the 7733 Group in the following:

• TABLE 18.1.1: programmable I/O ports, output port, memory expansion, and package

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

• “18.1 Performance overview” (page 18-3 in part 1)

Table 18.1.1 M37736MHLXXXHP performance overview

Items		Performance
Programmable I/O ports	Ports P0–P2, P4–P8, P10	8 bits × 8
	Port P3	4 bits × 1
Output port	Port P9	8 bits × 1
Memory expansion		Possible • External bus mode A: Maximum of 16 Mbytes • External bus mode B: Maximum of 1 Mbytes
Package		100-pin plastic molded fine-pitch QFP

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18.2 Pin configuration

Figure 18.2.1 shows the M37736MHLXXXHP pin configuration.

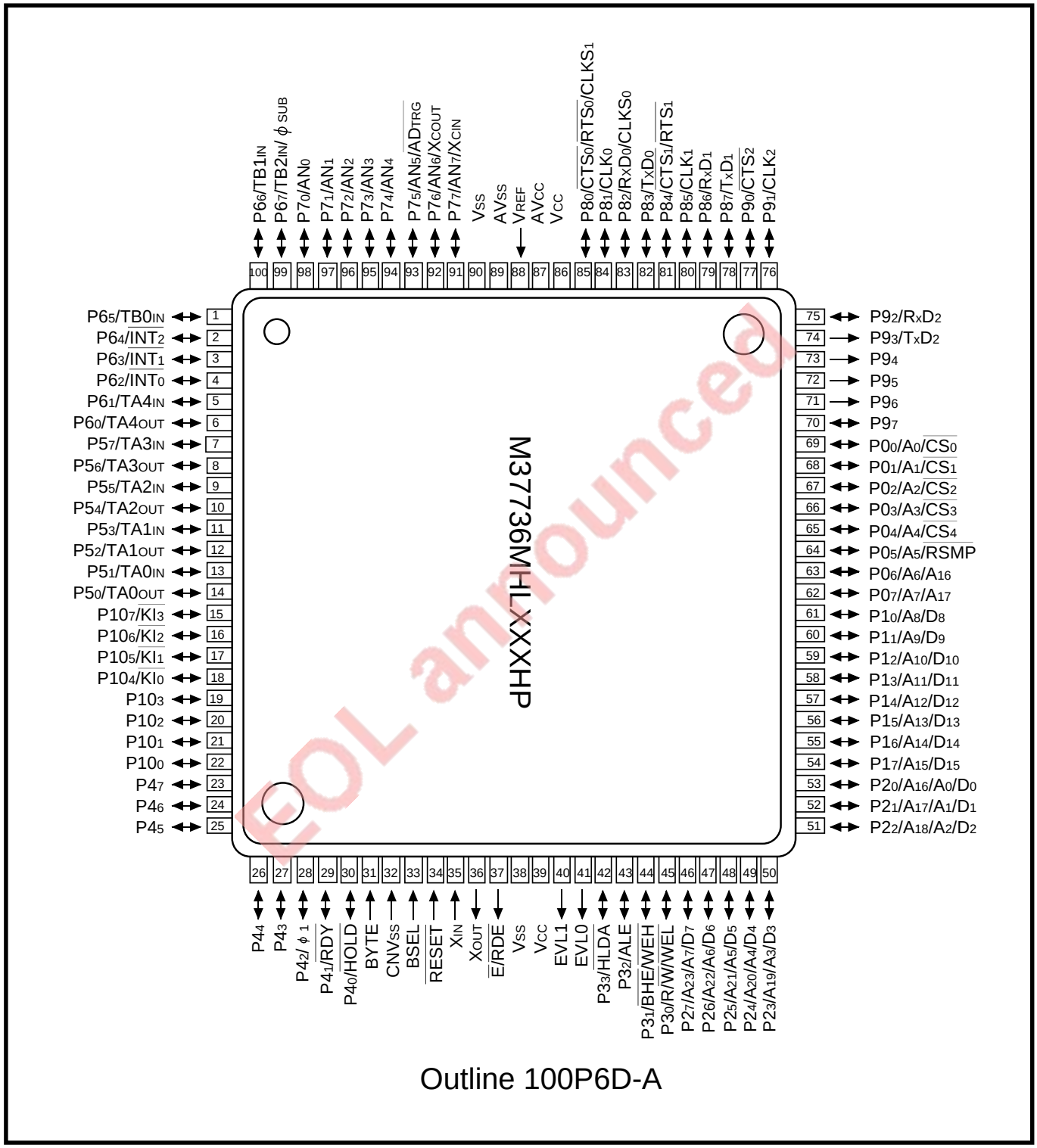

Fig. 18.2.1 M37736MHLXXXHP pin configuration (Top view)

18.3 Functional description

The M37736MHLXXXHP has the same functions as the M37736MHBXXXGP except for the power-on reset conditions. For the power-on reset conditions, refer to section **18.3.1 in part 1.**

For the other functions, refer to the corresponding chapters in parts 2 and 3:

- **Part 2 : Chapters “4. INTERRUPTS” to “9. A-D CONVERTER”**
- **Part 3 : Chapters “2. CENTRAL PROCESSING UNIT,” “3. PROGRAMMABLE I/O PORTS,” “8. SERIAL I/O” to “14. CLOCK GENERATING CIRCUIT”**

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LOW VOLTAGE VERSION

18.4 Electrical characteristics

Concerning section “18.4 Electrical characteristics,” the 7736 Group differs from the 7733 Group in the following sections:

- “**18.4.1 Absolute maximum ratings**”
- “**18.4.2 Recommended operating conditions**”
- “**18.4.3 Electrical characteristics**”
- “**18.4.7 Single-chip mode**”
- “**18.4.11 Measuring circuit for ports P0 to P10 and pins ϕ_1 and $\overline{E}$**”

The following sections of the 7736 Group differ depending on the external bus mode. In external bus mode A, refer to the corresponding sections in part 1; in external bus mode B, refer to the corresponding sections in part 2.

- **“18.4.6 Ready and Hold”**
  External bus mode A (page 18-16 in part 1)
  External bus mode B (page 18-5 in part 2)
- **“18.4.8 Memory expansion mode and Microprocessor mode : with no wait”**
  External bus mode A (page 18-20 in part 1)
  External bus mode B (page 18-7 in part 2)
- **“18.4.9 Memory expansion mode and Microprocessor mode : with wait 1”**
  External bus mode A (page 18-22 in part 1)
  External bus mode B (page 18-9 in part 2)
- **“18.4.10 Memory expansion mode and Microprocessor mode : with wait 0”**
  External bus mode A (page 18-24 in part 1)
  External bus mode B (page 18-11 in part 2)

The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, for these sections, refer to part 1:

- **“18.4.4 A-D converter characteristics” (page 18-10 in part 1)**
- **“18.4.5 Internal peripheral devices” (page 18-11 in part 1)**

EOL announced

18.4.1 Absolute maximum ratings

Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to 7	V
AVcc	Analog power source voltage		–0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to 12	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, V_{REF}, X_{IN}, BSEL		–0.3 to Vcc+0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$, X_{OUT}, $\overline{E}$		–0.3 to Vcc+0.3	V
P_d	Power dissipation	Ta = 25 °C	200	mW
T_{opr}	Operating temperature		–40 to 85	°C
T_{stg}	Storage temperature		–65 to 150	°C

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LOW VOLTAGE VERSION

18.4 Electrical characteristics

18.4.2 Recommended operating conditions

Recommended operating conditions (Vcc = 2.7 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Power source voltage	$f(X_{IN})$:Operating	2.7		5.5	V
		$f(X_{IN})$:Stopped, $f(X_{CIN})$ = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL, X_{CIN} **(Note 3)**	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, X_{IN}, $\overline{RESET}$, CNVss,BYTE, BSEL, X_{CIN} **(Note 3)**	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0		0.2 Vcc	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and microprocessor mode)	0		0.16 Vcc	V
$I_{OH\ (peak)}$	High-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$			–10	mA
$I_{OH\ (avg)}$	High-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$			–5	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_4$–$P10_7$			10	mA
$I_{OL\ (peak)}$	Low-level peak output current	$P4_4$–$P4_7$, $P10_0$–$P10_3$			16	mA
$I_{OL\ (avg)}$	Low-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_4$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_4$–$P10_7$			5	mA
$I_{OL\ (avg)}$	Low-level average output current	$P4_4$–$P4_7$, $P10_0$–$P10_3$			12	mA
$f(X_{IN})$	Main-clock oscillation frequency **(Note 4)**				12	MHz
$f(X_{CIN})$	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1: Average output current is the average value of an interval of 100 ms.

2: The sum of I_{OL}(peak) for ports P0, P1, P2, P3, P8 and P9 must be 80 mA or less, the sum of I_{OH}(peak) for ports P0, P1, P2, P3, P8 and P9 must be 80 mA or less, the sum of I_{OL}(peak) for ports P4, P5, P6, P7 and P10 must be 100 mA or less, and the sum of I_{OH}(peak) for ports P4, P5, P6, P7 and P10 must be 80 mA or less.

3: Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1."

4: The maximum value of $f(X_{IN})$ = 6 MHz when the main clock division selection bit = "1."

EOL announced

18.4.3 Electrical characteristics

Electrical characteristics (Vcc = 5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_0$–$P10_7$	Vcc = 5 V, I_{OH} = –10 mA		3			V
			Vcc = 3 V, I_{OH} = –1 mA		2.5			
V_{OH}	High-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	Vcc = 5 V, I_{OH} = –400 μA		4.7			V
V_{OH}	High-level output voltage	$P3_0$–$P3_2$	Vcc = 5 V, I_{OH} = –10 mA		3.1			V
			Vcc = 5 V, I_{OH} = –400 μA		4.8			
			Vcc = 3 V, I_{OH} = –1 mA		2.6			
V_{OH}	High-level output voltage	$\overline{E}$	Vcc = 5 V, I_{OH} = –10 mA		3.4			V
			Vcc = 5 V, I_{OH} = –400 μA		4.8			
			Vcc = 3 V, I_{OH} = –1 mA		2.6			
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_5$, $P8_0$–$P8_7$, $P9_0$–$P9_7$, $P10_4$–$P10_7$	Vcc = 5 V, I_{OL} = 10 mA				2	V
			Vcc = 3 V, I_{OL} = 1 mA				0.5	
V_{OL}	Low-level output voltage	$P4_4$–$P4_7$, $P5_0$–$P5_3$	Vcc = 5 V, I_{OL} = 16 mA				1.8	V
			Vcc = 3 V, I_{OL} = 10 mA				1.5	
V_{OL}	Low-level output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_3$	Vcc = 5 V, I_{OL} = 2 mA				0.45	V
V_{OL}	Low-level output voltage	$P3_0$–$P3_2$	Vcc = 5 V, I_{OL} = 10 mA				1.9	V
			Vcc = 5 V, I_{OL} = 2 mA				0.43	
			Vcc = 3 V, I_{OL} = 1 mA				0.4	
V_{OL}	Low-level output voltage	$\overline{E}$	Vcc = 5 V, I_{OL} = 10 mA				1.6	V
			Vcc = 5 V, I_{OL} = 2 mA				0.4	
			Vcc = 3 V, I_{OL} = 1 mA				0.4	
V_{T+}–V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$–$TA4_{IN}$, $TB0_{IN}$–$TB2_{IN}$, $\overline{INT0}$–$\overline{INT2}$, AD_{TRG}, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS2}$, $CLK0$, $CLK1$, $CLK2$, $\overline{KI0}$–$\overline{KI3}$	Vcc = 5 V		0.4		1	V
			Vcc = 3 V		0.1		0.7	
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$		Vcc = 5 V		0.2		0.5	V
			Vcc = 3 V		0.1		0.4	
V_{T+}–V_{T-}	Hysteresis X_{IN}		Vcc = 5 V		0.1		0.4	V
			Vcc = 3 V		0.06		0.26	
V_{T+}–V_{T-}	Hysteresis X_{CIN} (When external clock is input)		Vcc = 5 V		0.1		0.4	V
			Vcc = 3 V		0.06		0.26	
I_{IH}	High-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL	Vcc = 5 V, V_I = 5 V				5	μA
			Vcc = 3 V, V_I = 3 V				4	
I_{IL}	Low-level input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$, $P6_1$, $P6_5$– $P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL	Vcc = 5 V, V_I = 0 V				–5	μA
			Vcc = 3 V, V_I = 0 V				–4	
I_{IL}	Low-level input current	$P6_2$–$P6_4$, $P10_4$–$P10_7$	V_I = 0 V, without a pull-up transistor	Vcc = 5 V			–5	μA
				Vcc = 3 V			–4	
			V_I = 0 V, with a pull-up transistor	Vcc = 5 V	–0.25	–0.5	–1.0	mA
				Vcc = 3 V	–0.08	–0.18	–0.35	
V_{RAM}	RAM hold voltage		When clock is stopped		2			V

EOL announced

LOW VOLTAGE VERSION

18.4 Electrical characteristics

ELECTRICAL CHARACTERISTICS (Vcc= 5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Measuring conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	In single-chip mode, output pins are open, and the other pins are connected to Vss.	Vcc = 5 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating **(Note 1)**		4.5	9	mA
			Vcc = 3 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating **(Note 1)**		3	6	mA
			Vcc = 3 V, $f(X_{IN})$ = 12 MHz (Square waveform), ($f(f_2)$ = 0.75 MHz), $f(X_{CIN})$: Stopped, in operating **(Note 1)**		0.4	0.8	mA
			Vcc = 3V, $f(X_{IN})$ = 12 MHz (Square waveform), $f(X_{CIN})$ = 32.768 kHz, when the **WIT** instruction is executed **(Note 2)**		6	12	μA
			Vcc = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, in operating **(Note 3)**		30	60	μA
			Vcc = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$: 32.768 kHz, when the **WIT** instruction is executed **(Note 4)**		3	6	μA
			Ta = 25 °C, when clock is stopped			1	μA
			Ta = 85 °C, when clock is stopped			20	μA

Soon announced

Notes 1: This is applied when the main clock external input selection bit = "1," the main clock division selection bit = "0," and the signal output disable selection bit = "1."

2: This is applied when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1."

3: This is applied when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

4: This is applied when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1."

18.4.7 Single-chip mode

Timing requirements (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note 1)**, unless otherwise noted)

❋ The rise/fall time of an input signal must be 100 ns or less, unless otherwise noted.

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time **(Note 2)**	83		ns
$t_{w(H)}$	External clock input high-level pulse width **(Note 3)**	33		ns
$t_{w(L)}$	External clock input low-level pulse width **(Note 3)**	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns
$t_{su(P0D–E)}$	Port P0 input setup time	200		ns
$t_{su(P1D–E)}$	Port P1 input setup time	200		ns
$t_{su(P2D–E)}$	Port P2 input setup time	200		ns
$t_{su(P3D–E)}$	Port P3 input setup time	200		ns
$t_{su(P4D–E)}$	Port P4 input setup time	200		ns
$t_{su(P5D–E)}$	Port P5 input setup time	200		ns
$t_{su(P6D–E)}$	Port P6 input setup time	200		ns
$t_{su(P7D–E)}$	Port P7 input setup time	200		ns
$t_{su(P8D–E)}$	Port P8 input setup time	200		ns
$t_{su(P10D–E)}$	Port P10 input setup time	200		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns
$t_{h(E–P10D)}$	Port P10 input hold time	0		ns

Notes 1: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

2: When the main clock division selection bit = "1," the minimum value of tc = 166 ns.

3: When the main clock division selection bit = "1," values of $t_{w(H)}$/tc and $t_{w(L)}$/tc must be set to values from 0.45 through 0.55.

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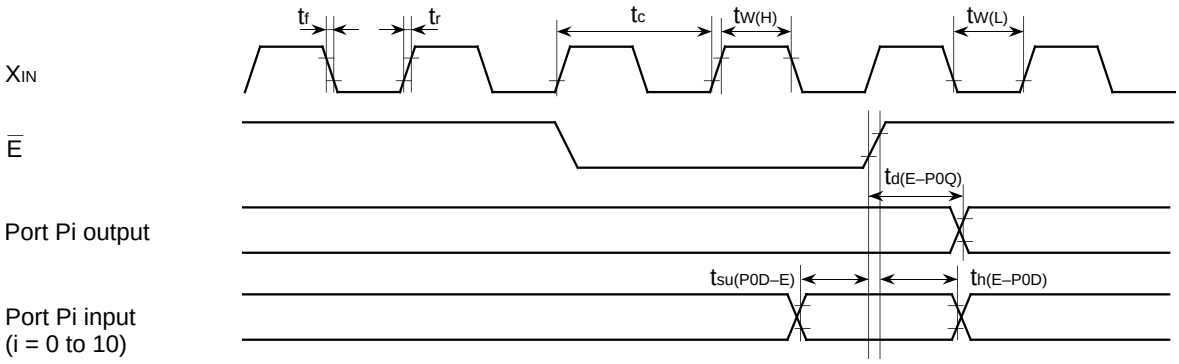
Switching characteristics (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, f(X_{IN}) = 12 MHz **(Note)**, unless otherwise noted)

Symbol	Parameter	Measuring conditions	Limits		Unit
			Min.	Max.	
$t_{d(E–P0Q)}$	Port P0 data output delay time	Fig. 18.4.1		300	ns
$t_{d(E–P1Q)}$	Port P1 data output delay time			300	ns
$t_{d(E–P2Q)}$	Port P2 data output delay time			300	ns
$t_{d(E–P3Q)}$	Port P3 data output delay time			300	ns
$t_{d(E–P4Q)}$	Port P4 data output delay time			300	ns
$t_{d(E–P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(E–P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(E–P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(E–P8Q)}$	Port P8 data output delay time			300	ns
$t_{d(E–P9Q)}$	Port P9 data output delay time			300	ns
$t_{d(E–P10Q)}$	Port P10 data output delay time			300	ns

Note: This is applied when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

18.4 Electrical characteristics

Single-chip mode



Measuring conditions

•V_{CC} = 2.7 to 5.5 V

•Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}

•Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

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18.4.11 Measuring circuit for ports P0 to P10 and pins ϕ_1 and $\overline{E}$

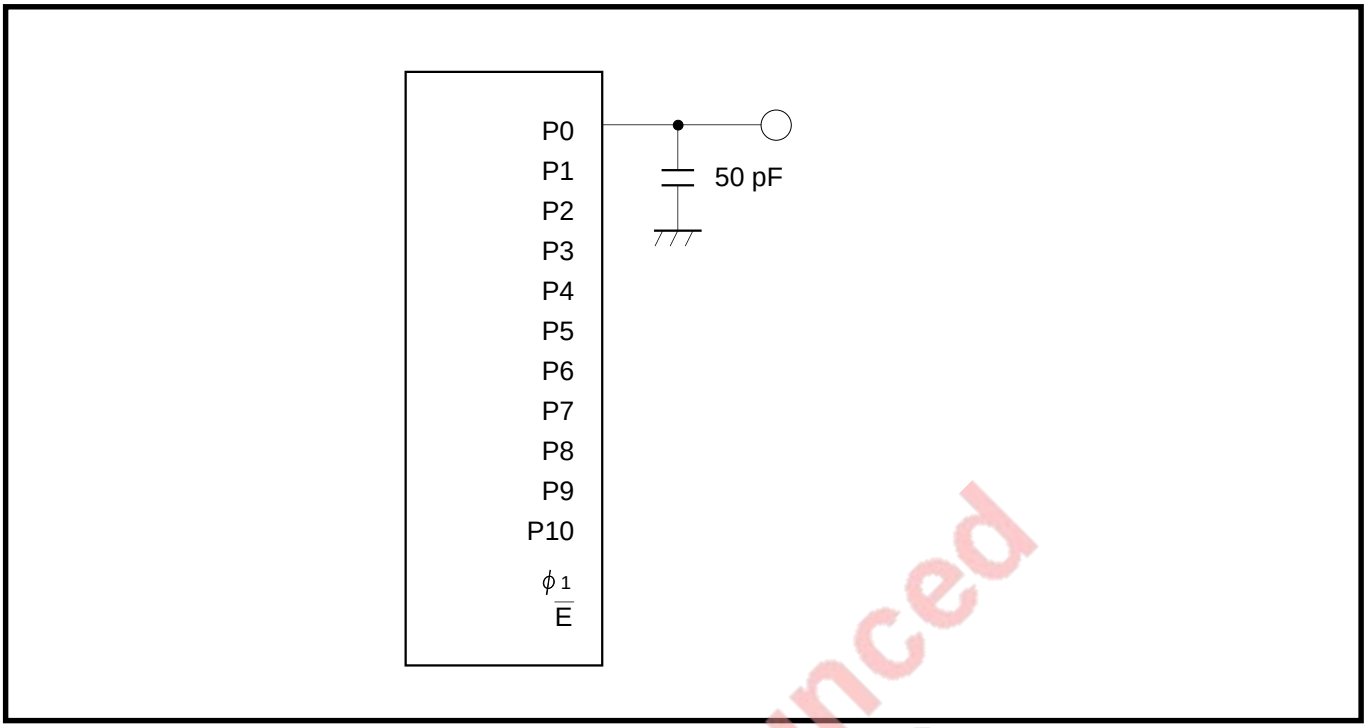


Fig. 18.4.1 Measuring circuit for ports P0 to P10 and pins ϕ_1 and $\overline{E}$

EOL announced

18.5 Standard characteristics

Concerning section "18.5 Standard characteristics," the 7736 Group differs from the 7733 Group in the following sections. Therefore, only the differences are described in this section:

- **"18.5.1 Programmable I/O port (CMOS output) standard characteristics: P0 to P3, $P4_0$ to $P4_3$, P5 to P9, and $P10_4$ to $P10_7$**
- **"18.5.2 Programmable I/O port (CMOS output) standard characteristics: $P4_4$ to $P4_7$ and $P10_0$ to $P10_3$**

The other description is the same as that of the 7736 Group. Therefore, refer to part 1:

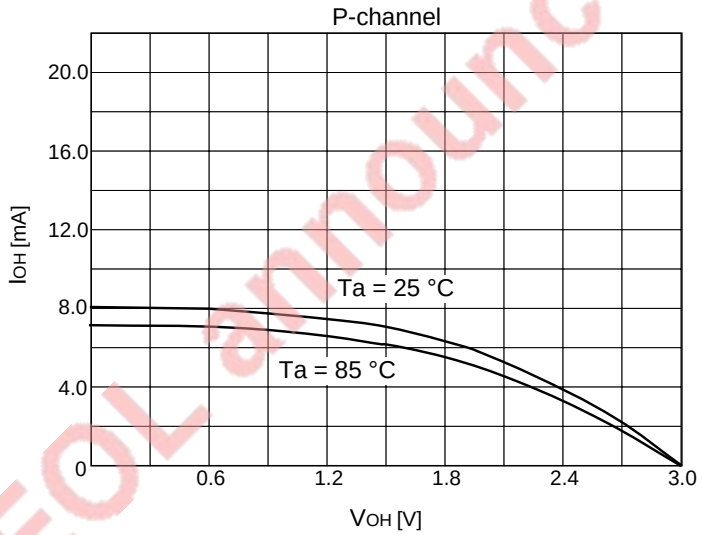
- **"18.5 Standard characteristics" (page 18-27 in part 1)**

Standard characteristics described below are characteristics examples of the M37736MHLXXXHP and are not guaranteed. For each parameter's limits, refer to section **"18.4 Electrical characteristics."**

18.5.1 Programmable I/O port (CMOS output) standard characteristics: Ports P0 to P3, $P4_0$–$P4_3$, P5–P9 and $P10_4$–$P10_7$

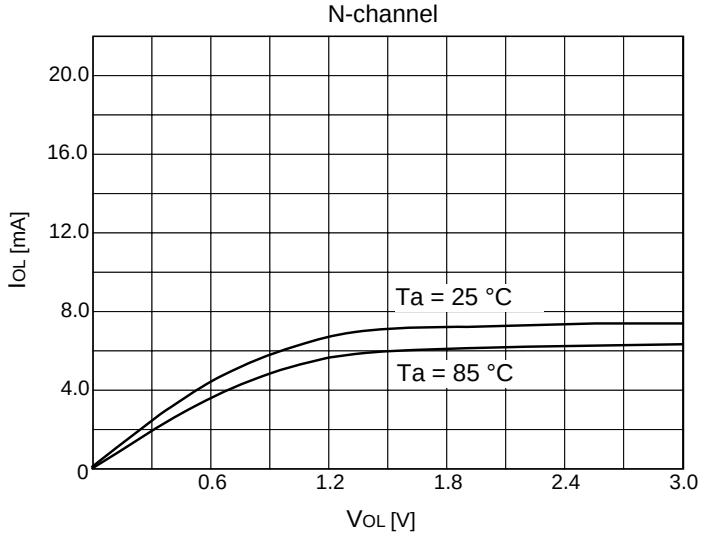
(1) P-channel I_{OH}–V_{OH} characteristics

Power source voltage V_{CC} = 3 V



(2) N-channel I_{OL}–V_{OL} characteristics

Power source voltage V_{CC} = 3 V



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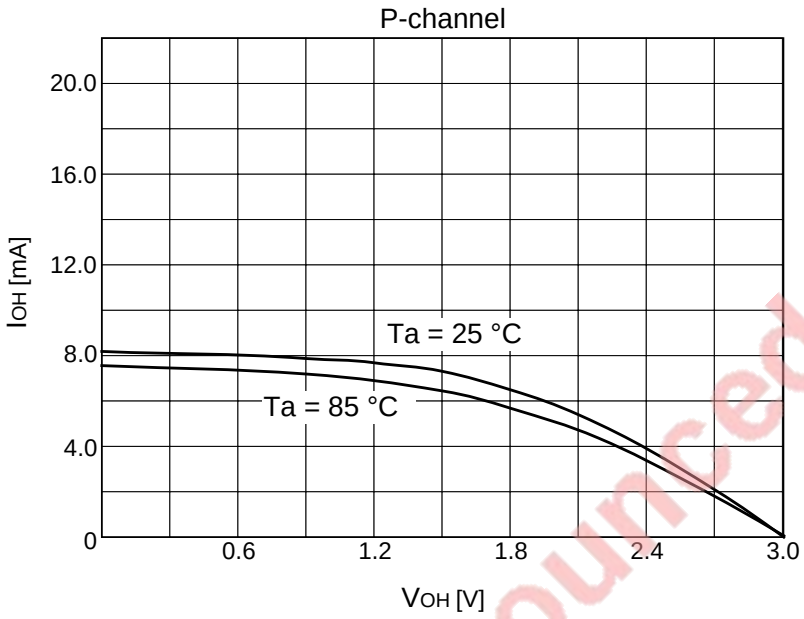
18.5.2 Programmable I/O port (CMOS output) standard characteristics: Ports P4$_4$ to P4$_7$ and P5$_0$ to P5$_3$

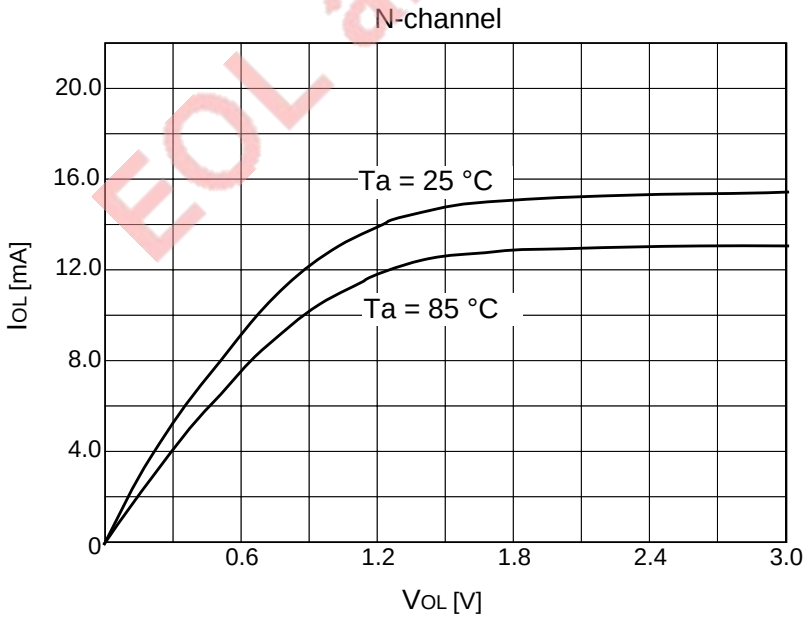
(1) P-channel I_{OH}–V_{OH} characteristics

Power source voltage V_{CC} = 3 V



(2) N-channel I_{OL}–V_{OL} characteristics

Power source voltage V_{CC} = 3 V



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18.6 Applications

In external bus mode A, section “18.6 Applications” is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“18.6 Applications” (page 18-32 in part 1)**

In external bus mode B, section “18.6 Applications” is the same as that of the 7735 Group. Therefore, refer to part 2:

- **“18.6 Applications” (page 18-13 in part 2)**

EOL announced

CHAPTER 19

BUILT-IN PROM VERSION

19.1 EPROM mode
19.2 Usage precaution

EOL announced

BUILT-IN PROM VERSION

19.1 EPROM mode

Concerning chapter “19. BUILT-IN PROM VERSION,” the 7736 Group differs from the 7733 Group in the following section. Therefore, only the differences are described in this chapter:

- **“19.1 EPROM mode”**

The following section is the same as that of the 7733 Group. Therefore, for this section, refer to part 1:

- **“19.2 Usage precaution” (page 19-10 in part 1)**

19.1 EPROM mode

Concerning section “19.1 EPROM mode,” the 7736 Group differs from the 7733 Group in the following:

- **Table 19.1.1**
- **Figures 19.1.1 and 19.1.2**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“19.1 EPROM mode” (page 19-3 in part 1)**

Table 19.1.1 Pin description in EPROM mode

Pin	Name	Input/Output	Functions
$P9_0$–$P9_7$	Input port P9	Input	Connect to Vss.
$P10_0$–$P10_7$	Input port P10	Input	Connect to Vss.
BSEL	Bus select input	Input	Connect to pin Vcc.
EVL0, EVL1	—	Output	Left open.

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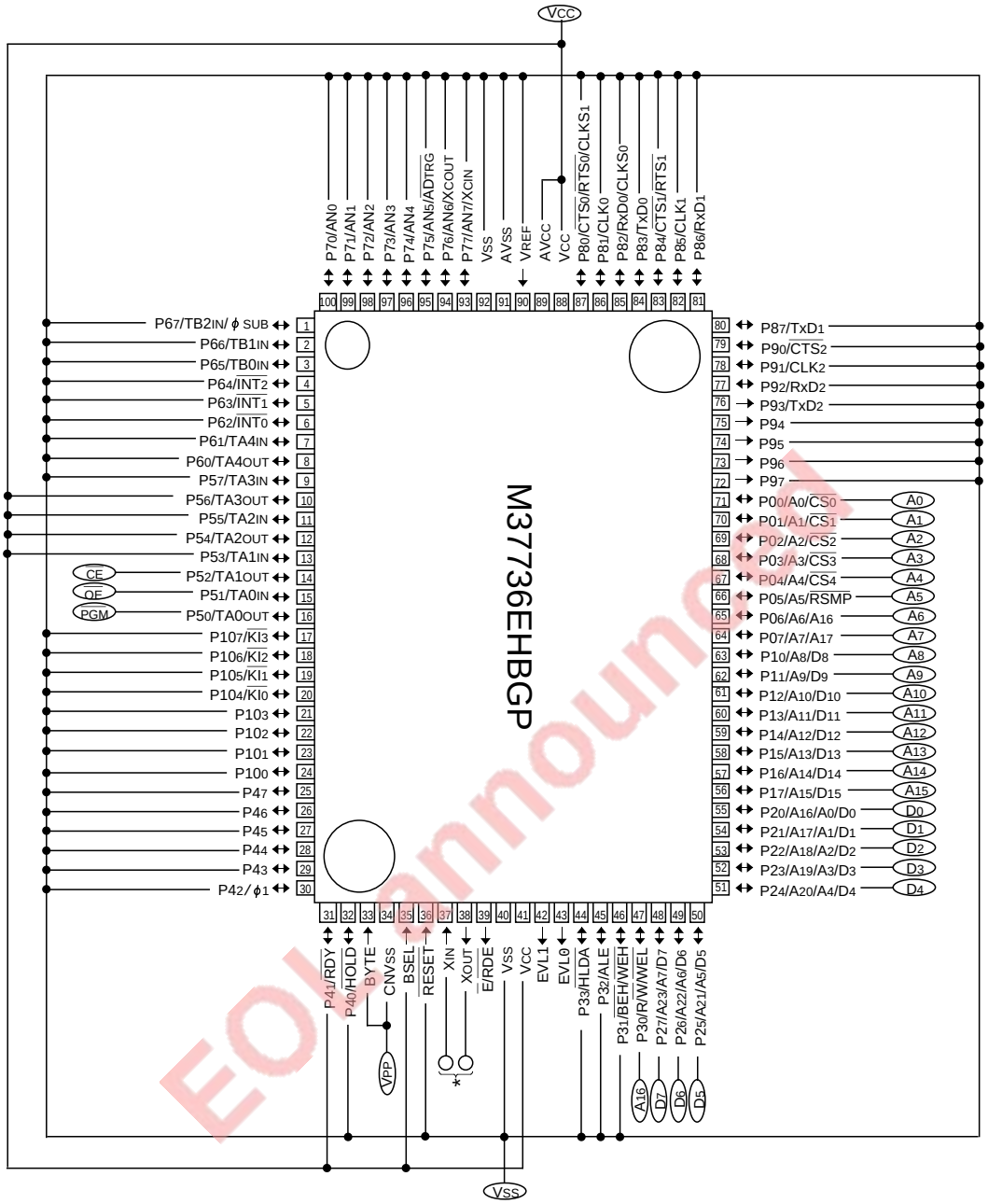


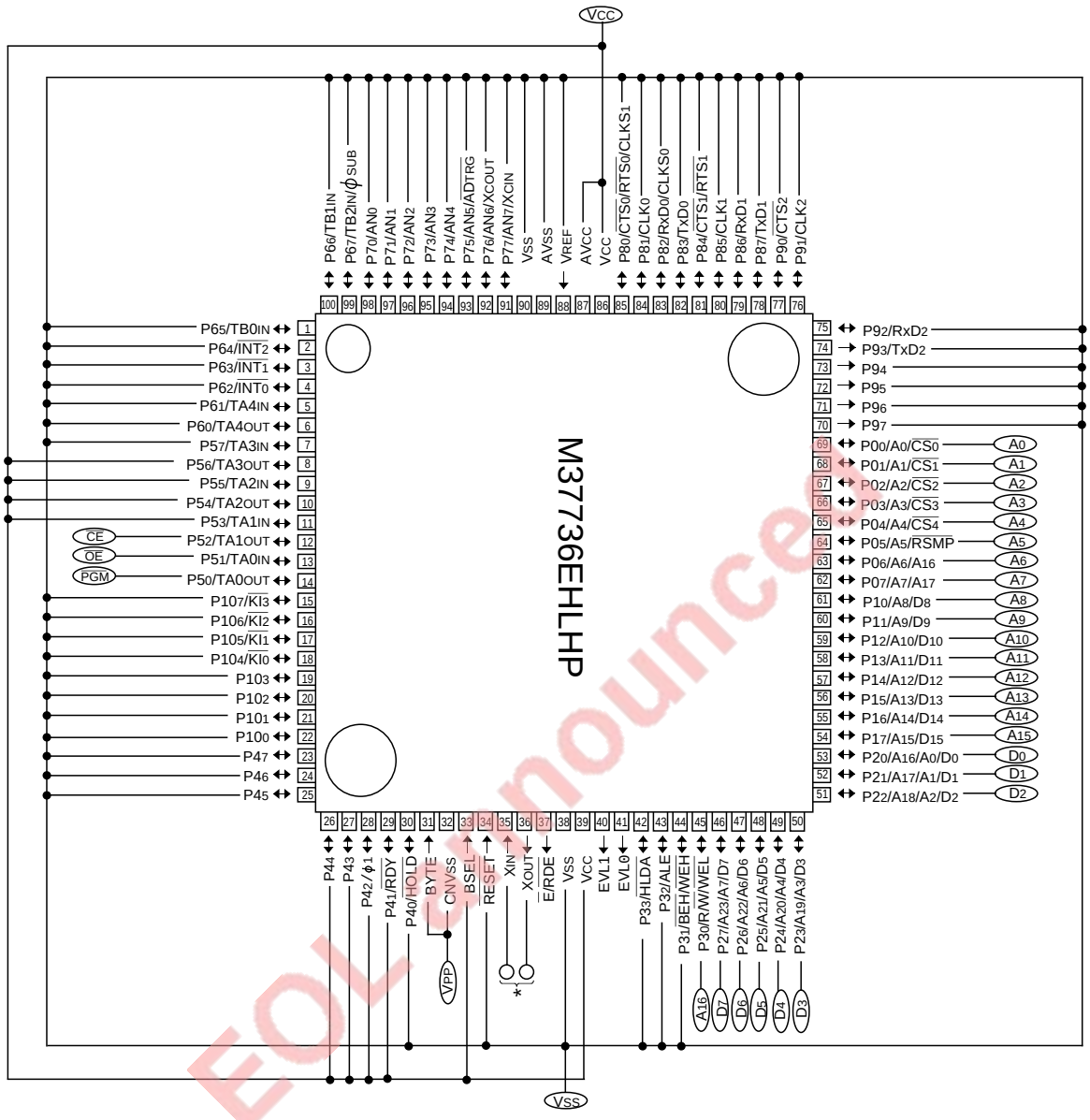
Outline 100P6S-A

Fig. 19.1.1 Pin connections in EPROM mode (M37736EHBGP)

EOL announced

BUILT-IN PROM VERSION

19.1 EPROM mode



Outline 100P6D-A

EOL announced

Fig. 19.1.2 Pin connections in EPROM mode (M37736EHLHP)

APPENDIX

Appendix 1. Memory allocation of 7736 Group
Appendix 2. Memory allocation in SFR area
Appendix 3. Control registers
Appendix 4. Package outlines
Appendix 5. Hexadecimal instruction code table
Appendix 6. Machine instructions
Appendix 7. Examples of handling unused pins
Appendix 8. Countermeasure examples against noise
Appendix 9. Q & A

EOL announced

APPENDIX

Concerning chapter “APPENDIX,” the 7736 Group differs from the 7733 Group in the following secti
Therefore, only the differences are described in this chapte r:

- **“Appendix 1. Memory allocation of 7736 Group”**
- **“Appendix 2. Memory allocation in SFR area”**
- **“Appendix 3. Control registers”**
- **“Appendix 4. Package outlines”**
- **“Appendix 7. Examples of handling unused pins”**

Note: The following sections of the 7736 Group are the same as those of the 7733 Group. Therefore, these sections, refer to part 1:

- **“Appendix 5. Hexadecimal instruction code table” (page 21-41 in part 1)**
- **“Appendix 6. Machine instructions” (page 21-44 in part 1)**
- **“Appendix 8. Countermeasure examples against noise” (page 21-61 in part 1)**
- **“Appendix 9. Q & A” (page 21-71 in part 1)**

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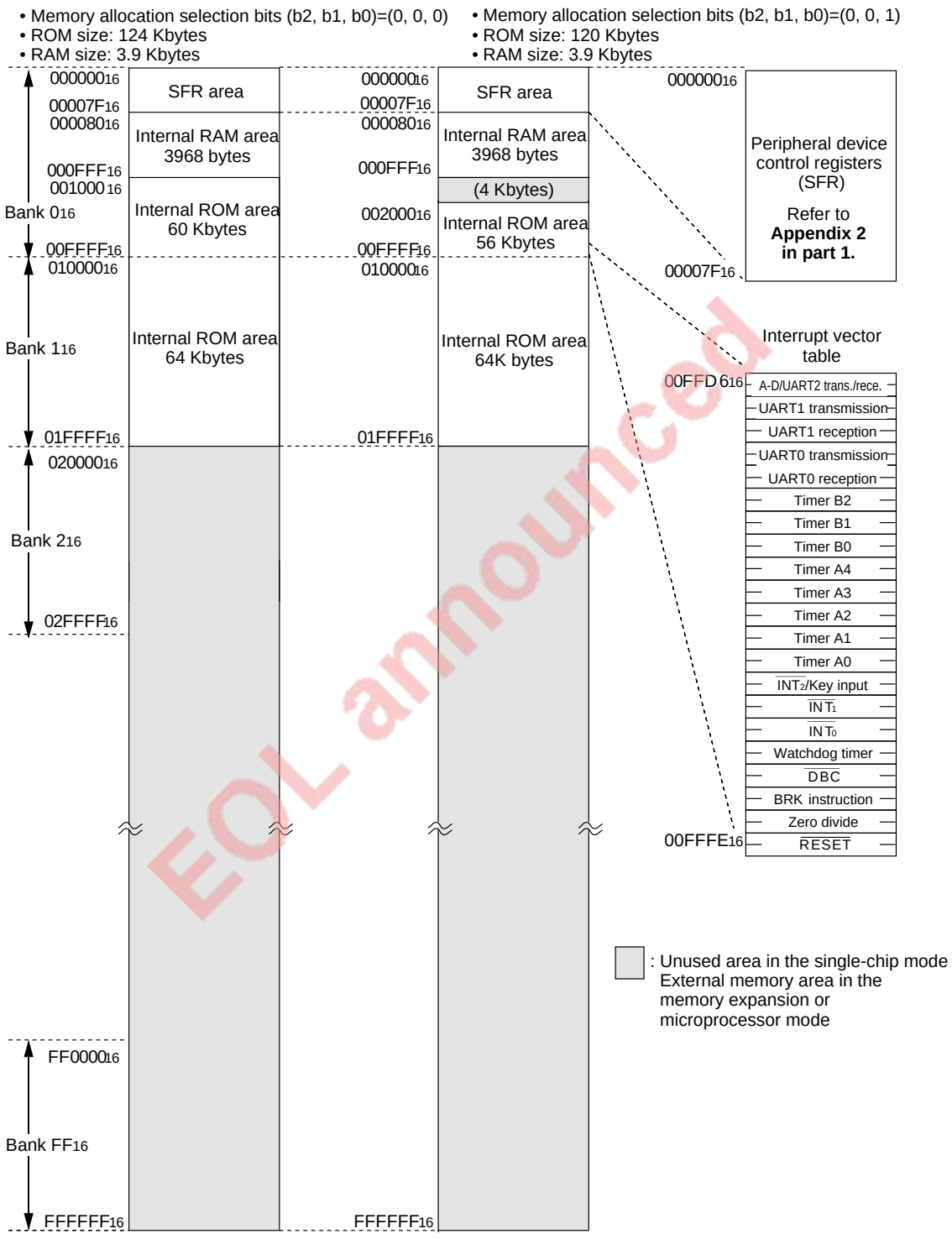
Appendix 1. Memory allocation of 7736 Group

1. M37736MHBXXXGP, M37736EHBXXXGP, M37736EHBGS, M37736MHLXXXHP, M37736EHLXXXHP



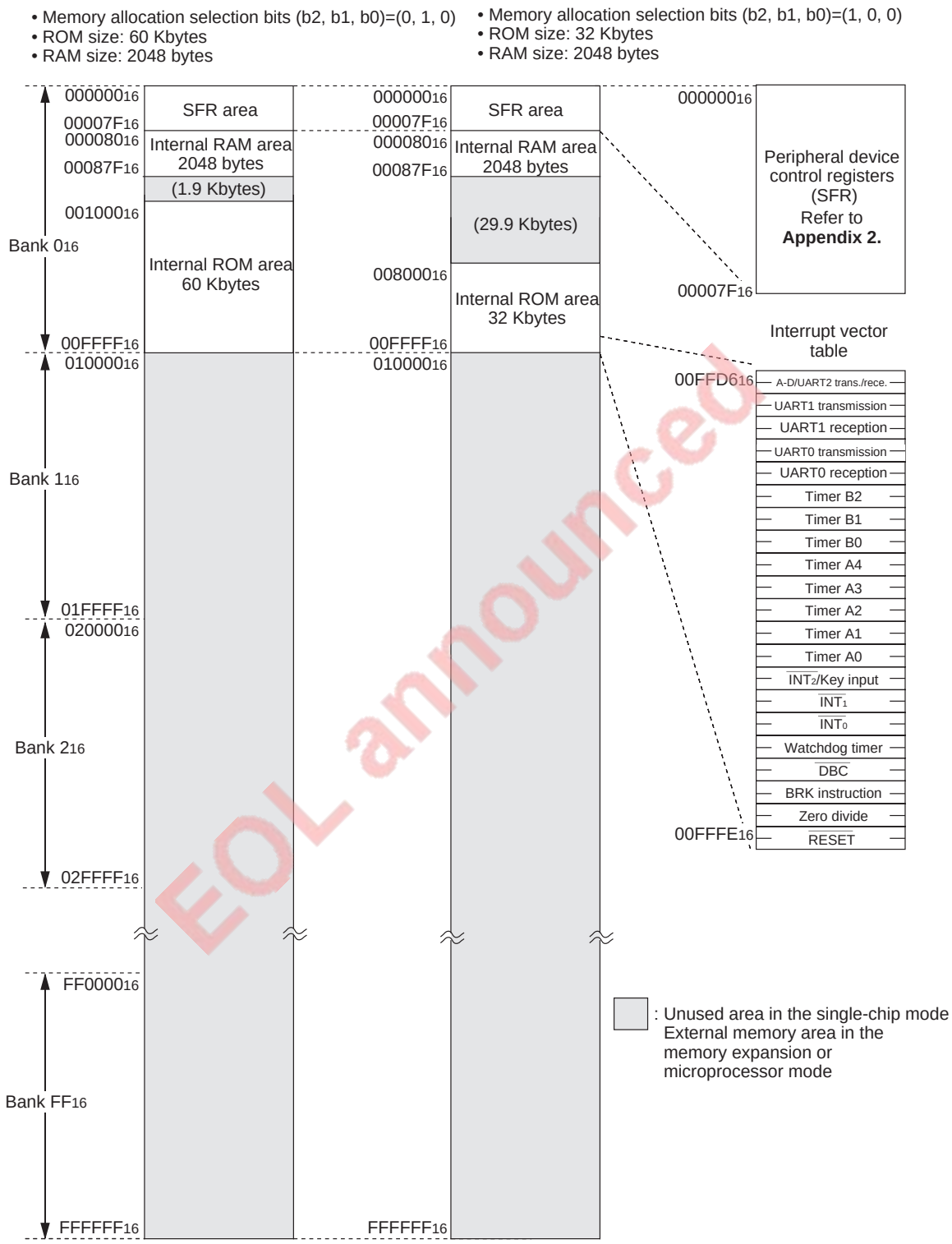
Notes 1: Access to internal ROM area is disabled in the microprocessor mode.
(Refer to section **"2.5 Processor modes" in part 1**.)
2: In external bus mode B, banks 10_{16} to FF_{16} cannot be accessed.

Fig. 1 Memory allocation of M37736MHBXXXGP, M37736EHBXXXGP, M37736EHBGS, M37736MHLXXXHP, M37736EHLXXXHP (1)

EOL announced

APPENDIX

Appendix 1. Memory allocation of 7736 Group

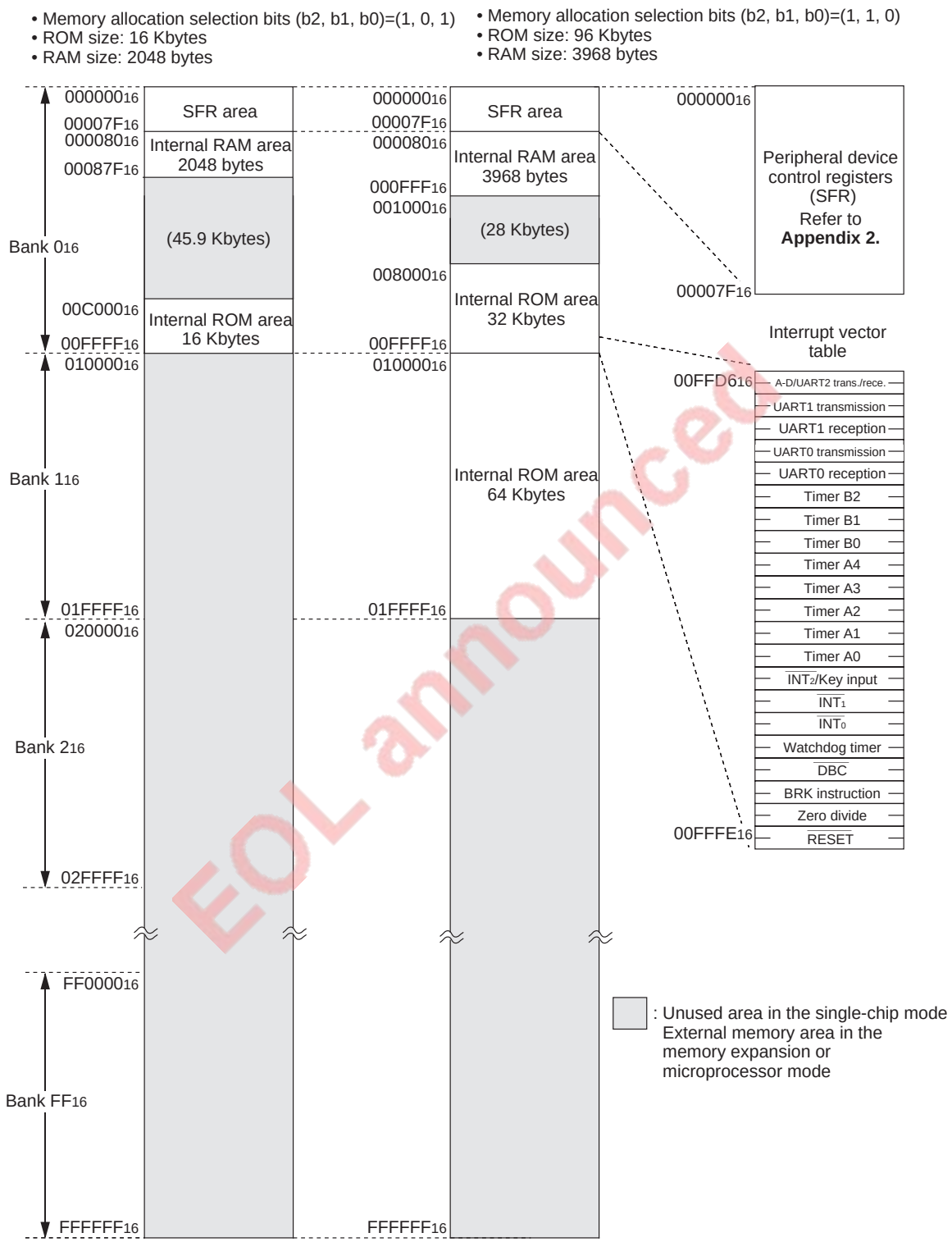


EOL announced

Notes 1: Access to internal ROM area is disabled in the microprocessor mode. (Refer to section **"2.5 Processor modes."**)
2: Banks 10₁₆ to FF₁₆ cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 2 Memory allocation of M37736MHBXXXGP, M37736EHBXXXGP, M37736EHBGS, M37736MHLXXXHP, M37736EHLXXXHP (2)

Appendix 1. Memory allocation of 7736 Group



EOL announced

Notes 1: Access to internal ROM area is disabled in the microprocessor mode.
(Refer to section **"2.5 Processor modes."**)
2: Banks 10₁₆ to FF₁₆ cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Fig. 3 Memory allocation of M37736MHBXXXGP, M37736EHBXXXGP, M37736EHBGS, M37736MHLXXXHP, M37736EHLXXXHP (3)

APPENDIX

Appendix 2. Memory allocation in SFR area

Concerning section “Appendix 2. Memory allocation in SFR area,” the 7736 Group differs from the 7733 Group in the following:

- **Address $6F_{16}$ (Refer to Figure 8.)**

The other description is the same as that of the 7733 Group. Therefore, refer to part 1:

- **“Appendix 2. Memory allocation in SFR area” (page 21-6 in part 1)**

EOL announced

Address	Register name	Access characteristics b7 b0	State immediately after reset b7 b0
6016	Watchdog timer register		? (✺1)
6116	Watchdog timer frequency selection flag	RW	? 0
6216	(Reserved area) (✺3)		?
6316	Memory allocation control register	RW	? 0 0 0 0 0
6416	UART 2 transmit/receive mode register	RW	? 0 0 0 0 0 0 0
6516	UART 2 baud rate register (BRG2)	WO	?
6616	UART 2 transmission buffer register	WO	?
6716		WO	?
6816	UART 2 transmit/receive control register 0	RO RW	? 1 0 0 0
6916	UART 2 transmit/receive control register 1	RO RW RO RW	0 0 0 0 0 0 1 0
6A16	UART 2 receive buffer register	RO	?
6B16		RO	0 0 0 0 0 0 0 ?
6C16	Oscillation circuit control register 0	RW(✺2) RW	? 0 0 0 0 0 ? 1
6D16	Port function control register	RW	0 0 0 0 0 0 0 0
6E16	Serial transmit control register	RW	0 0 0 0 ?
6F16	Oscillation circuit control register 1	WO RW	0 ? 0 1 0 0 0
7016	A-D / UART 2 trans./rece. interrupt control register	RW	? 0 0 0 0
7116	UART0 transmission interrupt control register	RW	? 0 0 0 0
7216	UART0 receive interrupt control register	RW	? 0 0 0 0
7316	UART1 transmission interrupt control register	RW	? 0 0 0 0
7416	UART1 receive interrupt control register	RW	? 0 0 0 0
7516	Timer A0 interrupt control register	RW	? 0 0 0 0
7616	Timer A1 interrupt control register	RW	? 0 0 0 0
7716	Timer A2 interrupt control register	RW	? 0 0 0 0
7816	Timer A3 interrupt control register	RW	? 0 0 0 0
7916	Timer A4 interrupt control register	RW	? 0 0 0 0
7A16	Timer B0 interrupt control register	RW	? 0 0 0 0
7B16	Timer B1 interrupt control register	RW	? 0 0 0 0
7C16	Timer B2 interrupt control register	RW	? 0 0 0 0
7D16	$\overline{INT_0}$ interrupt control register	RW	? 0 0 0 0 0 0
7E16	$\overline{INT_1}$ interrupt control register	RW	? 0 0 0 0 0 0
7F16	$\overline{INT_2}$/Key input interrupt control register	RW	? 0 0 0 0 0 0

✺1 A value of "FFF16" is set to the watchdog timer. (Refer to chapter **"10. WATCHDOG TIMER" in part 1.**)
✺2 For access characteristics at address 6C16, also refer to **Figure 14.3.2 in part 1.**
✺3 Do not wirte to the reserved area.

EOL announced

■Internal RAM area (M37736MHBXXXGP: addresses 8016 to FFF16)

- At hardware reset
  (not including the case where the stop or wait mode is terminated)...Undefined.
- At software reset...Retains the state immediately before reset.
- When the stop or wait mode is terminated
  (when the hardware reset is used)...Retains the state immediately before the **STP** or **WIT** instruction is executed.

Fig. 8 Memory allocation in SFR area (4)

APPENDIX

Appendix 3. Control registers

Concerning section “Appendix 3. Control registers,” the 7736 Group differs from the 7733 Group in the following:

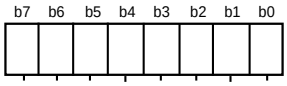
- **Port Pi register**
- **Port Pi direction register**
- **Port function control register**
- **Oscillation circuit control register 1**

The other control registers are the same as those of the 7733 Group. Therefore, for the other control registers, refer to part 1:

- **“Appendix 3. Control registers” (page 21-10 in part 1)**

EOL announced

Port Pi register



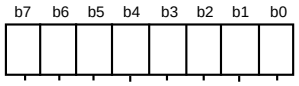
Port Pi register (i = 0 to 10)
(addresses 2_{16},3_{16},6_{16},7_{16},A_{16},B_{16},E_{16},F_{16},12_{16},13_{16},16_{16})

Bit	Bit name	Functions	At reset	RW
0	Port Pi_0's pin	Data is input from or output to a pin by reading/writing from/to the corresponding bit. 0: "L" level 1: "H" level	Undefined	RW
1	Port Pi_1's pin		Undefined	RW
2	Port Pi_2's pin		Undefined	RW
3	Port Pi_3's pin		Undefined	RW
4	Port Pi_4's pin		Undefined	RW
5	Port Pi_5's pin		Undefined	RW
6	Port Pi_6's pin		Undefined	RW
7	Port Pi_7's pin		Undefined	RW

Notes 1: Writing to bits 4 to 7 of the port P3 register is invalid and these bits are fixed to "0" when they are read.
2: After reset, be sure to write data to the port P9 register.

EOL announced

Port Pi direction register



Port Pi direction register (i = 0 to 8 and 10)
(addresses 4_{16},5_{16},8_{16},9_{16},C_{16},D_{16},10_{16},11_{16},14_{16},18_{16})

Bit	Bit name	Functions	At reset	RW
0	Port Pi_0 direction selection bit	0: Input mode (The port functions as an input port.) 1: Output mode (The port functions as an output port.)	0	RW
1	Port Pi_1 direction selection bit		0	RW
2	Port Pi_2 direction selection bit		0	RW
3	Port Pi_3 direction selection bit		0	RW
4	Port Pi_4 direction selection bit		0	RW
5	Port Pi_5 direction selection bit		0	RW
6	Port Pi_6 direction selection bit		0	RW
7	Port Pi_7 direction selection bit		0	RW

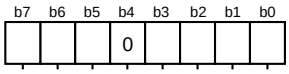
Note: Writing to bits 4 to 7 of the port P3 direction register is invalid and these bits are fixed to "0" when they are read.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Corresponding pin	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0

APPENDIX

Appendix 3. Control registers

Port function control register



Port function control register (address $6D_{16}$)

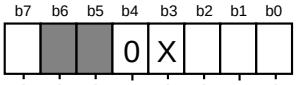
Bit	Bit name	Functions	At reset	RW
0	Standby state selection bit	0: Pins P0 to P3 are used for the external bus output. 1: Pins P0 to P3 are used for the port output.	0	RW
1	Sub-clock output selection bit/ Timer B2 clock source selection bit	•Port-Xc selection bit* = "0" (when the sub clock is not used) Timer B2 (event counter mode) clock source selection **(Note 1)** 0: $TB2_{IN}$ input (event counter mode) 1: Main clock divided by 32 (clock timer) •Port-Xc selection bit = "1" (when the sub clock is used) Sub-clock output selection 0: Pin $P6_7/TB2_{IN}/\phi_{SUB}$ functions as a programmable I/O port. 1: Sub clock ϕ_{SUB} is output from pin $P6_7/TB2_{IN}/\phi_{SUB}$.	0	RW
2	Timer B1 internal connect selection bit **(Note 2)**	0: No internal connection 1: Internal connection with timer B2	0	RW
3	Port P6 pull-up selection bit 0	0: No pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$ 1: With pull-up for pins $P6_2/\overline{INT_0}$ and $P6_3/\overline{INT_1}$	0	RW
4	Must be fixed to "0."		0	RW
5	Port P6 pull-up selection bit 1	•Key input interrupt selection bit = "0" 0: No pull-up for pin $P6_4/\overline{INT_2}$ 1: With pull-up for pin $P6_4/INT_2$ •Key input interrupt selection bit = "1" 0: Pin $P6_4/\overline{INT_2}$ is a port with no pull-up. 1: Pin $P6_4/INT_2$ is an input pin with pull-up and is used for the key input interrupt.	0	RW
6	Port P10 pull-up selection bit	0: No pull-up for pins $P10_4/\overline{KI_0}$ to $P10_7/\overline{KI_3}$ 1: With pull-up for pins $P10_4/\overline{KI_0}$ to $P10_7/\overline{KI_3}$	0	RW
7	Key input interrupt selection bit	0: $\overline{INT_2}$ interrupt 1: Key input interrupt	0	RW

Port-Xc selection bit* : Bit 4 of the oscillation circuit control register 0 (address $6C_{16}$)

Notes 1: When the port-Xc selection bit = "0" and timer B2 operates in the timer mode or the pulse period /pulse width measurement mode, bit 1 is invalid.
2: When timer B1 operates in the event counter mode, bit 2 is valid.

EOL announced

Oscillation circuit control register 1



Oscillation circuit control register 1 (address $6F_{16}$)

Bit	Bit name	Functions	At reset	RW
0	Main clock division selection bit **(Note 1)**	0: Main clock is divided by 2. 1: Main clock is not divided by 2.	0	RW
1	Main clock external input selection bit **(Note 1)**	0: Main-clock oscillation circuit is operating by itself. Watchdog timer is used when terminating stop mode. 1: Main clock is input from the external. Watchdog timer is not used when terminating stop mode.	0	RW
2	Sub clock external input selection bit **(Note 1)**	0: Sub-clock oscillation circuit is operating by itself. Pin P76 functions as pin X_{COUT}. Watchdog timer is used when terminating stop mode. 1: Sub clock is input from the external. Pin P76 functions as a programmable I/O port. Watchdog timer is not used when terminating stop mode.	0	RW
3	This bit is ignored.		1	RW
4	Must be fixed to "0" **(Note 2).**		0	RW
5	Not implemented.		Undefined	—
6	Not implemented.		Undefined	—
7	Clock prescaler reset bit	By writing "1" to this bit, clock prescaler is initialized.	0	WO

Notes 1: When writing to this register, follow the procedure shown in Figure 10.2.3.

2: The case where data "01010101_2" is written with the procedure shown in Figure 10.2.3 is not included.

EOL announced

• When performing clock prescaler reset

Write data "80_{16}." (**LDM** instruction)

• When writing to bits 0 to 3

Write data "01011101_2." (**LDM** instruction)

Next instruction

Write data "$00000XXX_2$." (**LDM** instruction)

(b2 to b0 in Figure 10.2.2)

APPENDIX

Appendix 4. Package outlines

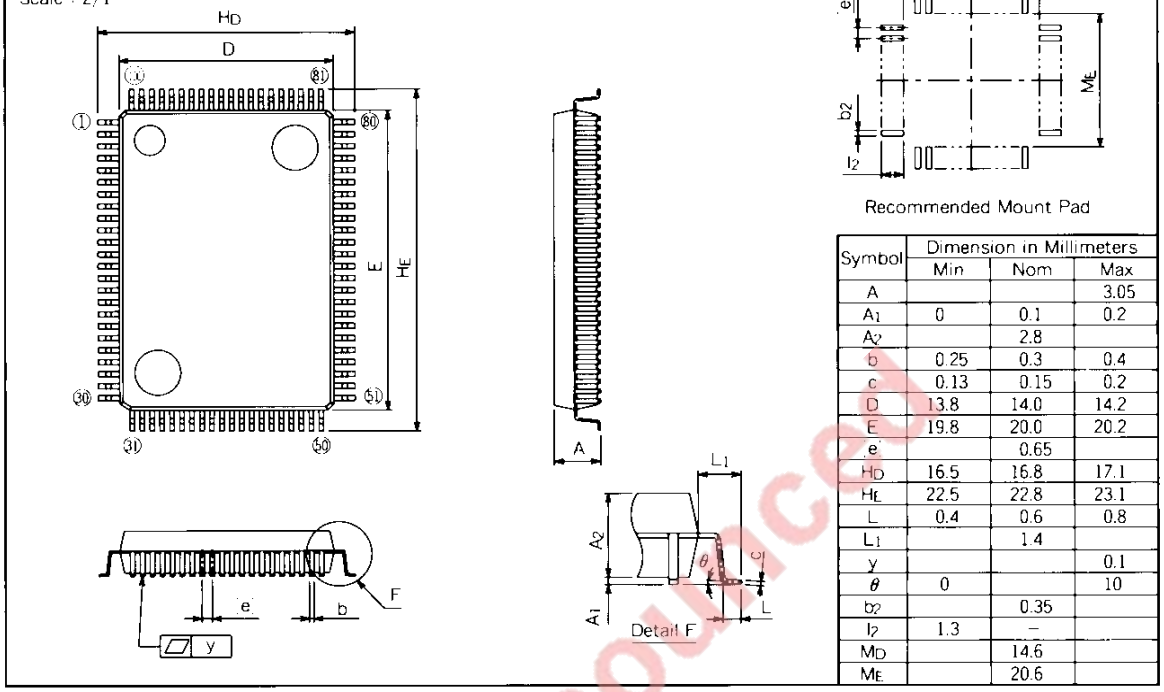
Appendix 4. Package outlines

100P6S−A

Plastic 100pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65		1.58	Alloy 42

Scale : 2/1



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A			3.05
A_1	0	0.1	0.2
A_2		2.8	
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e		0.65	
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1		1.4	
y			0.1
θ	0		10
b_2		0.35	
l_2	1.3	–	
M_D		14.6	
M_E		20.6	

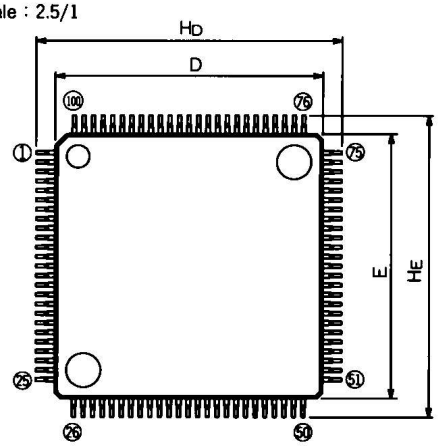
EOL announced

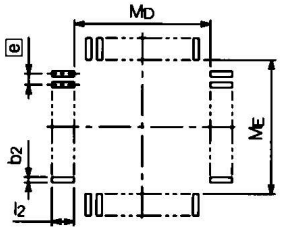
100P6D−A

Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	—	0.62	Alloy 42

Scale : 2.5/1





Recommended Mount Pad

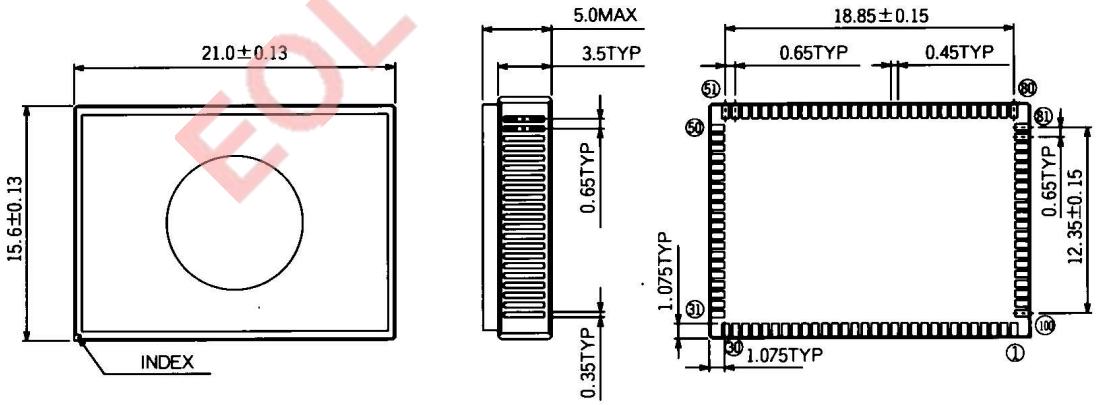
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	—	0.5	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
L	0.3	0.5	0.7
L_1	—	1.0	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	1.0	—	—
M_D	—	14.4	—
M_E	—	14.4	—

100D0

Glass seal 100pin QFN

EIAJ Package Code	JEDEC Code	Weight(g)
—	—	

Scale : 2/1



EOL announced

APPENDIX

Appendix 7. Examples of handling unused pins

Appendix 7. Examples of handling unused pins

The following are examples of handling unused pins.
These are, however, just examples. In actual use, make the necessary adaptations and properly evaluate performance according to the user's application.

1. In single-chip mode

Table 1 Examples of handling unused pins in single-chip mode

Pins	Handling example
P0–P8, P10	Connect these pins to pin Vcc or Vss via resistors after the pins are set to the input mode, or leave these pins open after they are set to the output mode (**Note 1**).
P9	Leave these pins open after writing data to the port P9 register (**Note 3**).
$\overline{E}$, $\overline{RDE}$	Leave this pin open.
EVL0, EVL1	
XOUT (**Note 2**)	
AVcc	Connect this pin to pin Vcc.
AVss, VREF, BYTE	Connect these pins to pin Vss.
BSEL	Connect this pin to pin Vcc or Vss.

Notes 1: When leaving these pins open after they are set to the outpu these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power sou ports function as input ports.
Software reliability can be enhanced when the contents of th ' direction registers are set periodically. This is because these contents may be chan which occurs owing to noise, etc.
For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

2: This is applied when an external clock is input to pin XIN.

3: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

EOL announced

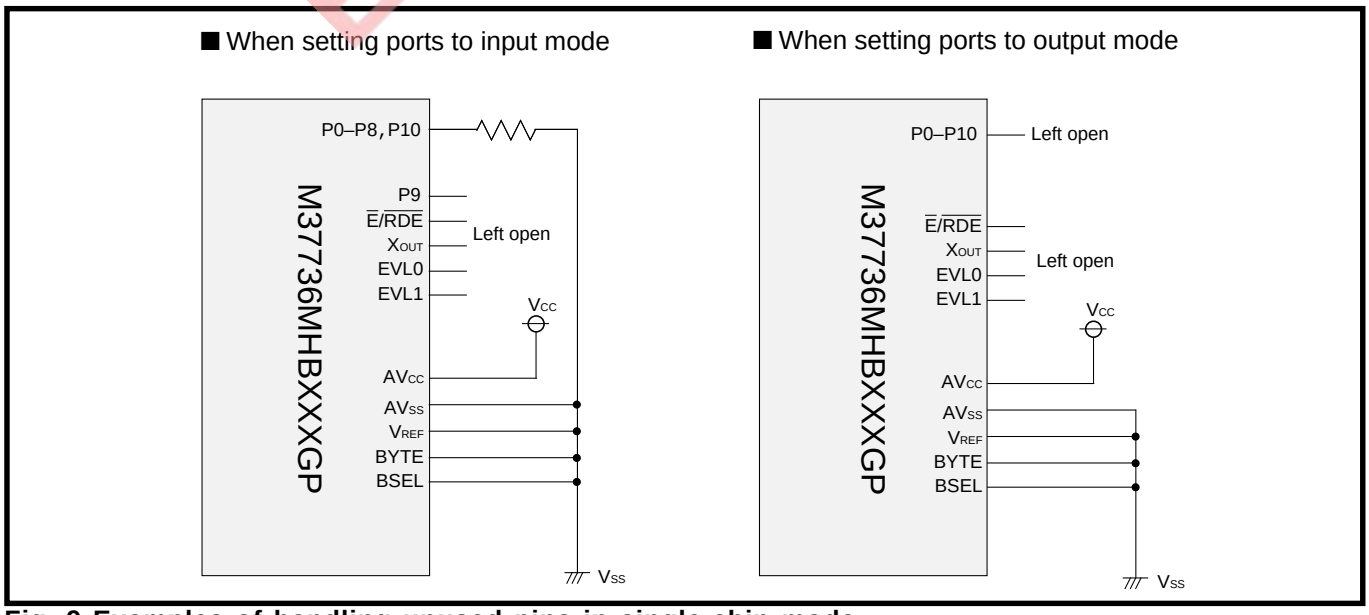


Fig. 9 Examples of handling unused pins in single-chip mode

2. In memory expansion mode (External bus mode A)

Table 2 Examples of handling unused pins in memory expansion mode (External bus mode A)

Pins	Handling example
P42–P47, P5–P8, P10 (**Note 7**)	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 8**).
BHE (**Note 3**), ALE (**Note 4**), $\overline{\text{HLDA}}$	Leave these pins open. (**Note 5**)
XOUT (**Note 6**)	Leave this pin open.
$\overline{\text{HOLD}}$, $\overline{\text{RDY}}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the memory expansion mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

6: This is applied when an external clock is input to pin XIN.

7: Set pin P42/ϕ1 as pin P42. (Clock ϕ1 output is disabled.) And then, for this pin, do the same handling as that for pins P43 to P47, P5 to P8 and P10.

8: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

EOL announced

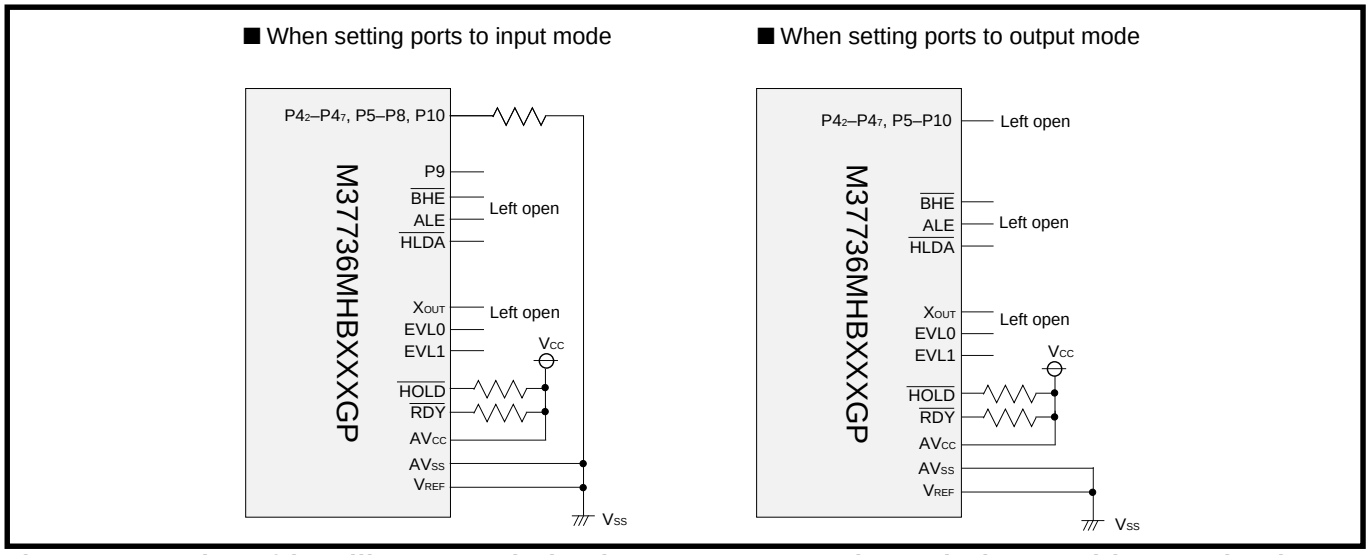


Fig. 10 Examples of handling unused pins in memory expansion mode (External bus mode A)

APPENDIX

Appendix 7. Examples of handling unused pins

3. In memory expansion mode (External bus mode B)

Table 3 Examples of handling unused pins in memory expansion mode (External bus mode B)

Pins	Handling example
P42–P47, P5–P8, P10 (**Note 5**)	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 6**).
$\overline{WHE}$, $\overline{WHL}$, $\overline{RDE}$, $\overline{HLDA}$, $\overline{CS0}$–$\overline{CS4}$, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
XOUT (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVcc	Connect this pin to pin Vcc.
AVss, VREF	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports. Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the memory expansion mode by software. Therefore, a voltage level of this pin is undefined and the power source current may increase while this pin functions as an input port.

4: This is applied when an external clock is input to pin XIN.

5: Set pin P42/ϕ1 as pin P42. (Clock ϕ1 output is disabled.) And then, for this pin, do the same handling as that for pins P43 to P47, P5 to P8 and P10.

6: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

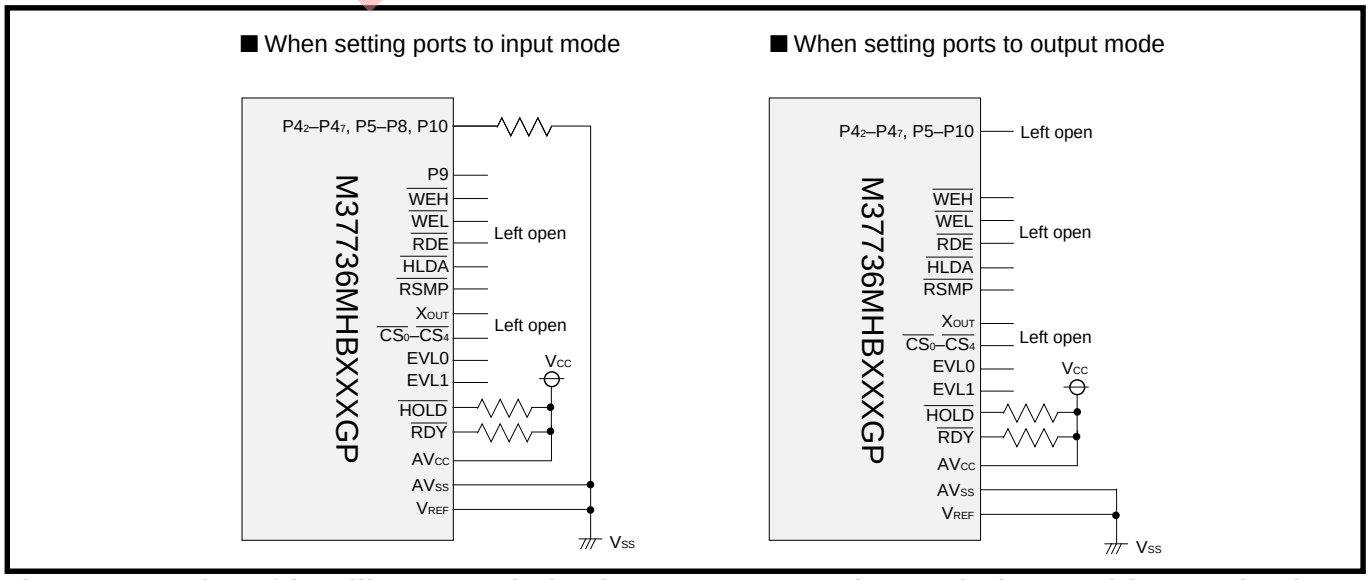


Fig. 11 Examples of handling unused pins in memory expansion mode (External bus mode B)

EOL announced

4. In microprocessor mode (External bus mode A)

Table 4 Examples of handling unused pins in microprocessor mode (External bus mode A)

Pins	Handling example
$P4_3$–$P4_7$, P5–P8, P10	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 7**).
BHE (**Note 3**), ALE (**Note 4**), $\overline{HLDA}$, ϕ_1	Leave these pins open. (**Note 3**)
X_{OUT} (**Note 6**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AV_{CC}	Connect this pin to pin Vcc.
AV_{SS}, V_{REF}	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: This is applied when "H" level is input to pin BYTE.

4: This is applied when "H" level is input to pin BYTE and the accessible area has a capacity of 64 Kbytes.

5: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the microprocessor mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.

6: This is applied when an external clock is input to pin X_{IN}.

7: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

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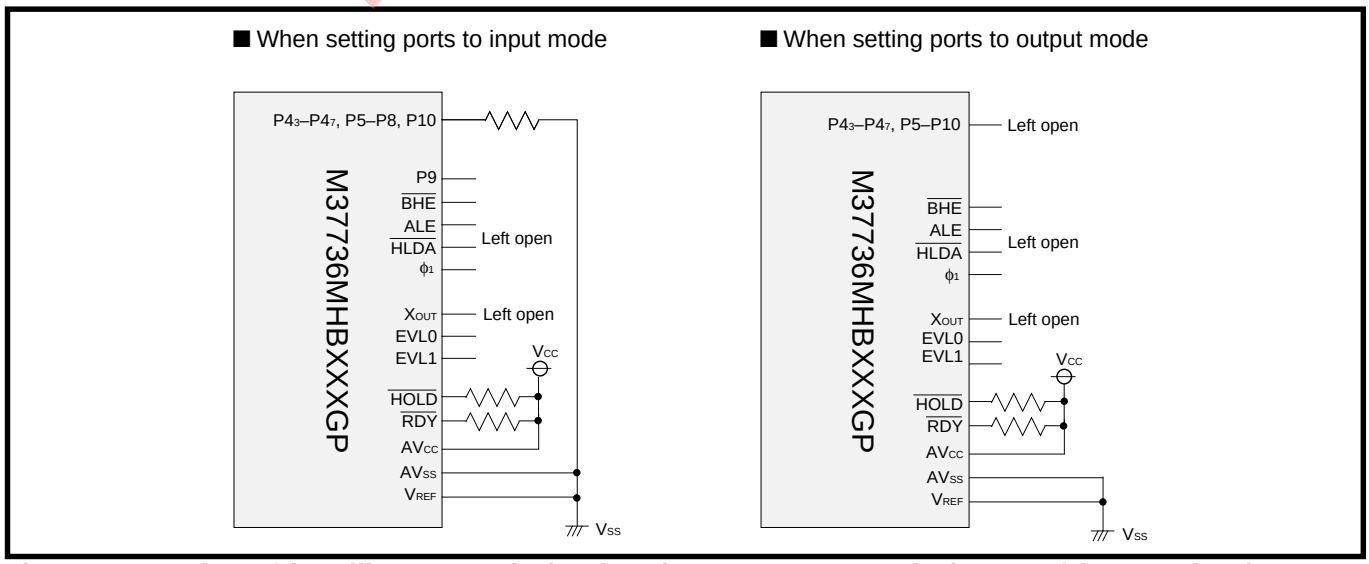

Fig. 12 Examples of handling unused pins in microprocessor mode (External bus mode A)

APPENDIX

Appendix 7. Examples of handling unused pins

5. In microprocessor mode (External bus mode B)

Table 5 Examples of handling unused pins in microprocessor mode (External bus mode B)

Pins	Processing example
P43–P47, P5–P8, P10	Connect these pins to pin Vcc or Vss via resistors after these pins are set to the input mode, or leave these pins after they are set to the output mode (**Notes 1 and 2**).
P9	Leave these pins open after writing data to the port P9 register (**Note 5**).
$\overline{WHE}$, $\overline{WHL}$, $\overline{RDE}$, $\overline{HLDA}$, ϕ_1, $\overline{CS_0}$–$\overline{CS_4}$, $\overline{RSMP}$	Leave these pins open. (**Note 3**)
XOUT (**Note 4**)	Leave this pin open.
$\overline{HOLD}$, $\overline{RDY}$	Connect these pins to pin Vcc via resistors after these pins are set to the input mode. (These pins are pulled high.) (**Note 2**)
AVCC	Connect this pin to pin Vcc.
AVSS, VREF	Connect these pins to pin Vss.
EVL0, EVL1	Leave these pins open.

Notes 1: When leaving these pins open after they are set to the output mode, note the following: these pins function as input ports from reset until they are switched to the output mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.
Software reliability can be enhanced when the contents of the above ports' direction registers are set periodically. This is because these contents may be changed by noise, a program runaway which occurs owing to noise, etc.

2: For unused pins, use the shortest possible wiring (within 20 mm from the microcomputer's pins).

3: When Vss level is applied to pin CNVss, note the following: these pins function as input ports from reset until the processor mode is switched to the microprocessor mode by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while these pins function as input ports.

4: This is applied when an external clock is input to pin XIN.

5: When leaving port P9 pins open after writing data to the port P9 register, note the following: these pins are in a floating state from reset until the data is written to the port P9 register by software. Therefore, voltage levels of these pins are undefined and the power source current may increase while they are in a floating state.

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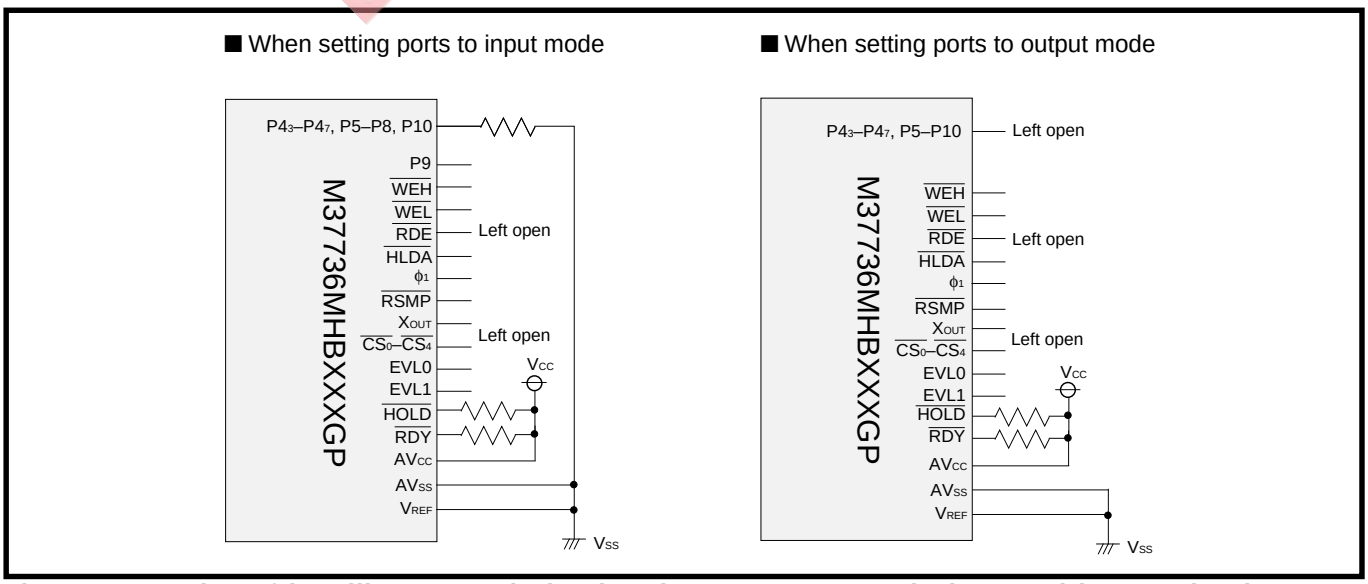

Fig. 13 Examples of handling unused pins in microprocessor mode (External bus mode B)

GLOSSARY

This section briefly explains the terms used in this user's manual. Note that the terms defined here are applied to this manual only.

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Term	Meaning		Relevant term
Access	*verb* *noun*	Means one of the following: reading out, writing to, and both of them.	
Accessible area	*noun*	An accessible memory area. Its capacity is one of the following; a maximum of 16 Mbytes (for the 7733 Group or external bus mode A of the 7736 Group) and a maximum of 1 Mbytes (for the 7735 Group or external bus mode B of the 7736 Group).	Access
Access characteristics	*noun*	Indicates whether accessible or not.	Access
Branch	*verb*	Means moving the program's execution point (in other words, address) to another location regardless of conditions.	
Bus control signal	*noun*	A generic name for ALE, $\overline{E}$, $\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$, $\overline{RDY}$, $\overline{HOLD}$, $\overline{HLDA}$, BYTE, and $\overline{RSMP}$ signals	
Count down /Countdown	*verb/ noun*	Means decrementing by 1 and counting.	Count up/Countup
Count source	*noun*	A signal which is counted by timers A, B, BRG, and the watchdog timer. It is f_2, f_{16}, f_{64}, or f_{512}, which is selected by the count source selection bits, etc.	
Count up/Countup	*verb/ noun*	Means incrementing by 1 and counting.	Count down /Countdown
Counter contents(value)	*noun*	A value which can be read out when the timer Ai (Bi) register is read out. Note that, at the reload timing, it is the reloaded value ("n"), and not "$FFFF_{16}$" or "0000_{16}."	
$\overline{CS}$	*noun*	Chip select signal (for the 7735 Group or external bus mode B of the 7736 Group)	
Event counter	*noun*	Timer which correctly counts the number of external pulses without using a divider	Internal area
External area	*noun*	An accessible area for external devices. It has a capacity of 1 Mbytes.	
External bus	*noun*	A generic name for the external address bus and the external data bus	
External device	*noun*	A device connected externally to the microcomputer. A generic name for a memory, an I/O, and a peripheral IC.	
Fetch	*verb*	Means taking an op-code and operand from an instruction queue buffer into the CPU.	Prefetch
Gate function (of timer)	*noun*	A function which allows the user to control the count source input of a timer	External area
Internal area	*noun*	An accessible internal area. A generic name for areas of the internal RAM, internal ROM, and SFR.	
Interrupt routine	*noun*	A routine which is automatically executed when an interrupt request is accepted. Set the start address of this routine into the interrupt vector table.	
Key input interrupt	*noun*	An interrupt which is generated by a key input	
Key matrix	*noun*	Switches which are arranged in lattice-like form	Scan output
Key-on wakeup	*noun*	A function which terminates the stop or the wait mode by using the key input	Stop mode /Wait mode
LSB first	*noun*	A kind of data transfer format of serial I/O. It means transferring LSB (in other words, the least significant bit) first.	MSB first
Main clock	*noun*	A clock which is input from pin X_{IN}	
MSB first	*noun*	A kind of data transfer format of serial I/O. It means transferring MSB (in other words, the most significant bit) first.	LSB first

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Term	Meaning		Relevant term
Overflow	*noun*	A state where the result obtained by the countup is greater than the counter resolution	Underflow Countup/Count up
Power saving	*noun*	Means saving the power consumption by using the stop or wait mode, etc.	Stop mode Wait mode
Prefetch	*verb*	Means taking an op-code and operand from a memory into an instruction queue buffer.	Fetch
Pull-down	*noun*	Means connecting with Vss line for stabilizing its I/O level.	Pull-up
Pull-up	*noun*	Means connecting with Vcc line for stabilizing its I/O level.	Pull-down
Read-modify-write instruction	*noun*	An instruction which reads the contents of SFR and RAM, modifies them, and writes them back to the same addresses. They are the **ASL**, **CLB**, **DEC**, **INC**, **LSR**, **ROL**, **ROR**, and **SEB** instructions	
Return input	*noun*	Input signal from the key matrix to the microcomputer. It is used to detect a key input	Scan output
Scan output	*noun*	Output signal from the microcomputer to the key matrix. It is used to detect a key input.	Return input Key matrix
Signal required for accessing external device	*noun*	A generic name for a bus control signal, an address bus signal, a data bus signal, and a chip select signal. (Note that the chip select signal is only for the 7735 Group or external bus mode B of the 7736 Group.)	Bus control signal
Stop mode	*noun*	A state where all of the oscillation circuits stop operating and the program execution is stopped. By executing the **STP** instruction, the microcomputer enters the stop mode.	Wait mode
Sub clock	*noun*	A clock which is input from pin XCIN	Main clock
Synchronizing clock	*noun*	A transfer clock for the clock synchronous serial I/O	
System clock	*noun*	One of the following: the main clock, which is input from pin XIN or the sub clock, which is input from pin XCIN **Note:** In the microcomputers other than the 7733/7735/7736 Group, definition of “system clock” may be different.	Internal clock ϕ
UART	*noun*	Clock asynchronous serial I/O. When it is used as the name of a functional block, this term also means the serial I/O which can be switched to the clock synchronous serial I/O.	Clock synchronous serial I/O
Underflow	*noun*	A state where the result obtained by the countdown is greater than the counter resolution	Overflow Count down/Countdown
Wait mode	*noun*	A state where one or more oscillation circuits are operating (in other words, they are oscillating), however, the program execution is stopped. By executing the **WIT** instruction, the microcomputer enters the wait mode.	Stop mode

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REVISION DESCRIPTION LIST	7733/7735/7736 Group User's Manual

<table>
<tr><th>Rev. No.</th><th colspan="3">Revision Description</th><th>Rev. date</th></tr>
<tr><td>1.00</td><td colspan="3">First Edition</td><td>970425</td></tr>
<tr><td>2.00</td><td colspan="3">The following are revised.</td><td>980731</td></tr>
<tr><td></td><td>Page</td><td>Previous Version</td><td>Revised Version</td><td></td></tr>
<tr><td></td><td>PART 1
P2-8
(2) Bit 1:
Zero flag (Z)</td><td>This flag is ignored for an addition instruction in the decimal mode (the ADC instruction).</td><td>This flag is ignored for an addition and subtraction instructions (the ADC and the SBC instructions) in the decimal mode.</td><td></td></tr>
<tr><td></td><td>PART 1
P2-19
Fig. 2.4.1

PART 1
P21-30</td><td>Functions
b2 b1 b0 ROM size (addresses)
0 0 0 : 124 K (001000_{16} ‘$01FFFF_{16}$)
0 0 1 : 120 K (002000_{16} ‘$01FFFF_{16}$)
0 1 0 : Do not select.
0 1 1 : Do not select.
1 0 0 : Do not select.
1 0 1 : Do not select.
1 1 0 : 96 K (008000_{16} ‘$01FFFF_{16}$)
1 1 1 : 32 K (008000_{16} ‘$00FFFF_{16}$)</td><td>Functions
b2 b1 b0 ROM size RAM size
0 0 0 : 124 Kbytes, 3968 bytes
0 0 1 : 120 Kbytes, 3968 bytes
0 1 0 : 60 Kbytes, 2048 bytes
0 1 1 : Do not select.
1 0 0 : 32 Kbytes, 2048 bytes
1 0 1 : 16 Kbytes, 2048 bytes
1 1 0 : 96 Kbytes, 3968 bytes
1 1 1 : Do not select.</td><td></td></tr>
<tr><td></td><td></td><td>Notes 1: •••••
2: When changing these bits, this change must be performed in an area which is internal ROM area before and after this change, for example addresses 008000_{16} to $00FFFF_{16}$. Also, when changing these bits, be sure to follow the procedure listed below.
3: In the M37733S4BFP, M37733S4LHP, M37735S4BFP, or M37735S4LHP, writing to address 63_{16} is disabled.</td><td>Notes 1: •••••
2: When changing these bits, this change must be performed in an area which is internal ROM area before and after this change, for example addresses $00C000_{16}$ to $00FFFF_{16}$. Also, when changing these bits, be sure to follow the procedure listed below.
3: This figure is applied only to the H37733MHBXXXFP. For the other microcomputers, please refer to the latest datasheets on the English document CD-ROM or our Web site.</td><td></td></tr>
<tr><td></td><td>PART 1
P2-21
Fig. 2.4.3

PART 1
P21-3
Fig. 2

PART 2
P21-4
Fig. 2

PART 3
P20-4
Fig. 2</td><td>Omitted.</td><td>Refer to pages 2 and 3.</td><td></td></tr>
<tr><td></td><td>PART 1
P6-47
Line 23</td><td>2: When the counter operates as an 8-bit pulse width modulator, pin TAiOUT outputs “L” level of which width is the same as the PWM pulse’s “H” level width which was set. And then, pin TAiOUT starts the PWM pulse output.</td><td>2: When the counter operates as an 8-bit pulse width modulator, after a trigger occurs, pin TAiOUT outputs “L” level of which width is the same as the PWM pulse’s “H” level width which was set. And then, pin TAiOUT starts the PWM pulse output.</td><td></td></tr>
</table>

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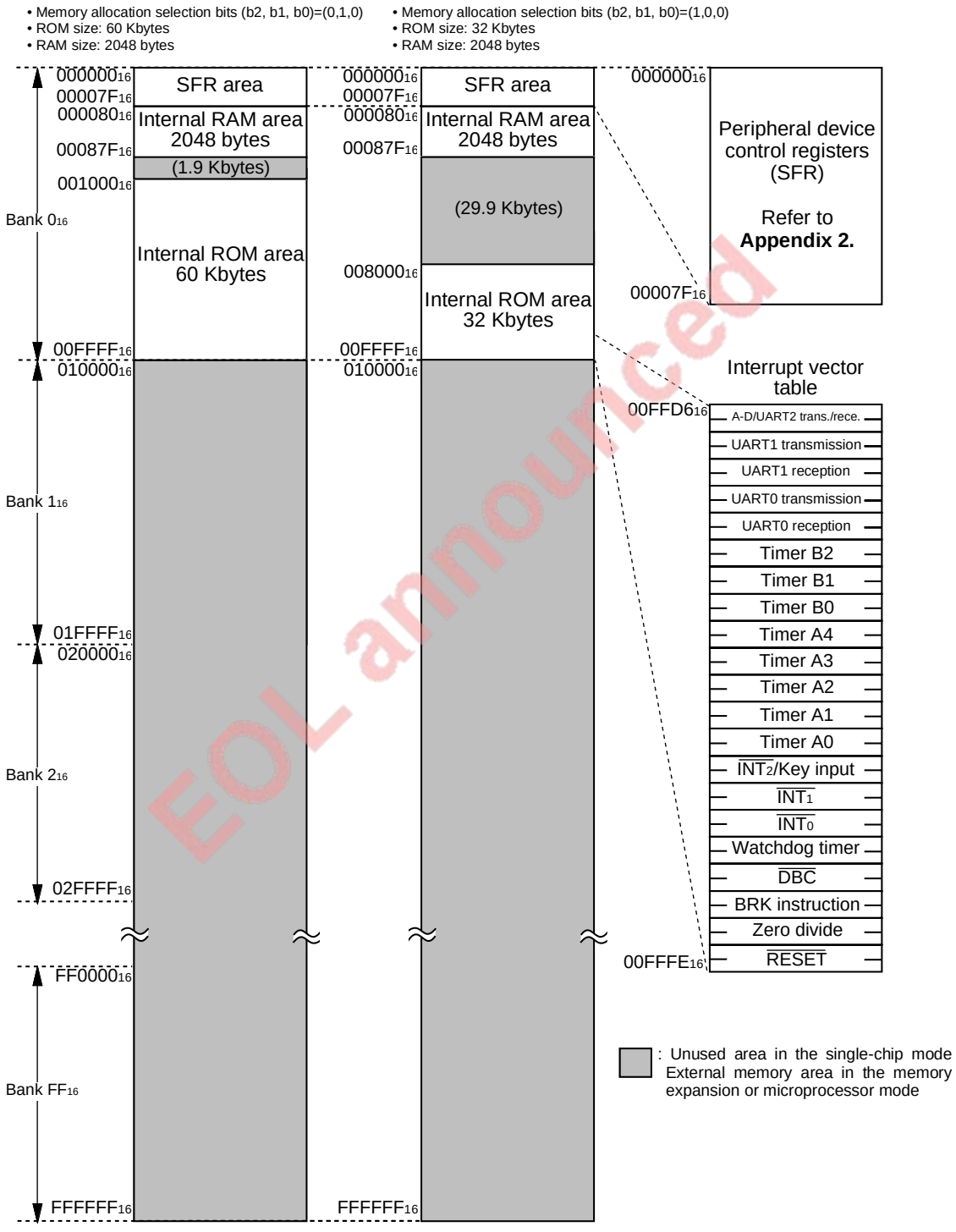
Revised Version



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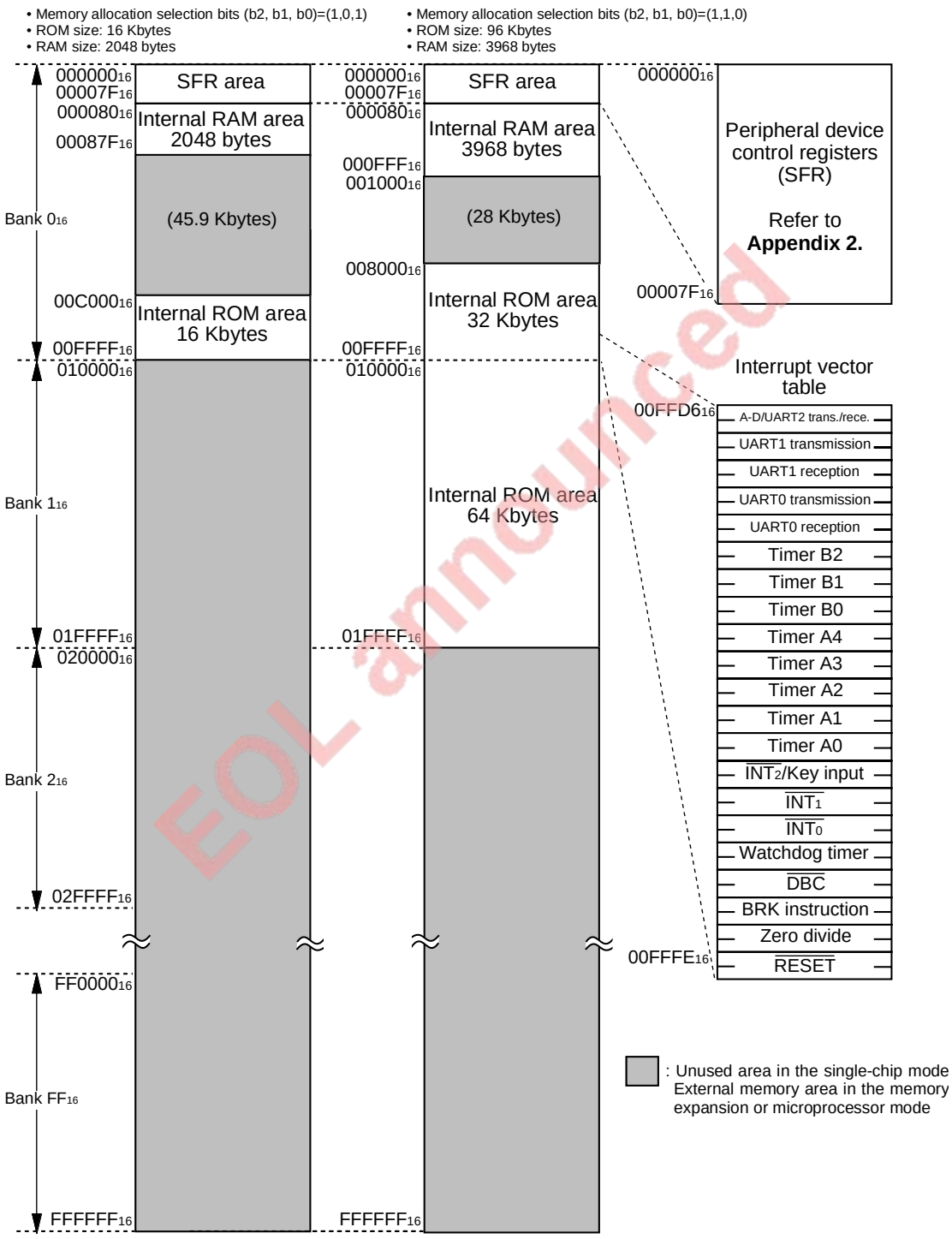
Notes 1: Access to internal ROM area is disabled in the microprocessor mode.
(Refer to section **"2.5 Processor modes."**)
2: Banks 10_{16} to FF_{16} cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

Revised Version



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Notes 1: Access to internal ROM area is disabled in the microprocessor mode.
(Refer to section **"2.5 Processor modes."**)
2: Banks 10₁₆ to FF₁₆ cannot be accessed in the 7735 Group and in external bus mode B of the 7736 Group.

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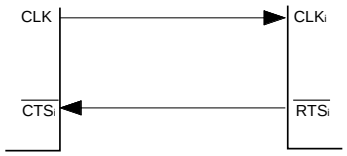
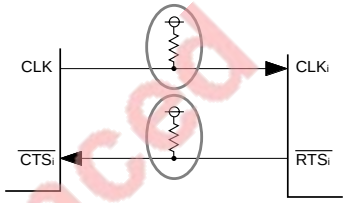
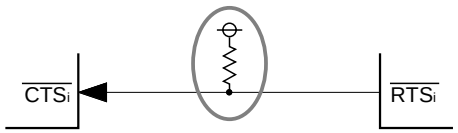
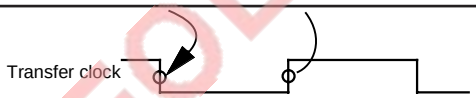
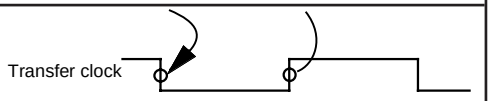
Rev. No.	Revision Description			Rev. date
2.00	Page	Previous Version	Revised Version	980731
	PART 1 P7-31 Line 7	The timer Bi overflow flag is cleared to "0" when a value is written to the timer Bi mode register with the count start flag = "1."	The timer Bi overflow flag is cleared to "0" at the next count timing of the count source when a value is written to the timer Bi mode register with the count start flag = "1."	
	PART 1 P8-40 Fig.8.3.13			
	PART 1 P8-46 Table 8.4.4	14400 | f2 | 52(3F16) | 14490.57 | 53(4016) | 14467.59	14400 | f2 | 52(3416) | 14490.57 | 53(3516) | 14467.59	
	PART 1 P8-59 Line 2	And then, reception is started when ST is detected.	And then, the transfer clock is generated when ST is detected, and reception is started.	
	PART 1 P8-59 Fig.8.4.11			
	PART 1 P8-60 Fig. 8.4.12	 Reception is started at the falling edge of start bit.	 The transfer clock is generated at the falling edge of start bit, and reception is started.	
	PART 1 P8-62 Line 20	⑤ For the slave microcomputer whose address matches bits 6 to 0 in the receive data, clear the sleep mode. (Do not terminate the sleep mode for the other slave microcomputers.)	⑤ For the slave microcomputer whose address matches bits 6 to 0 in the receive data, terminate the sleep mode. (Do not terminate the sleep mode for the other slave microcomputers.)	
	PART 1 P11-17 Table 11.4.3	Interrupt: Conditions for each function which generates interrupt request when clocks f2 and f512 are stopped: A-D conversion interrupt: Disabled when clocks f2 and f512 are not stopped: A-D conversion interrupt: Enabled	Interrupt: Conditions for each function which generates interrupt request when clocks f2 and f512 are stopped: A-D conversion interrupt: Disabled when clocks f2 and f512 are not stopped: A-D conversion interrupt: Enabled in one-shot mode and single sweep mode	

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<table>
<tr><th>Rev. No.</th><th colspan="3">Revision Description</th><th>Rev. date</th></tr>
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<tr><td></td><td>PART 1
P19-4
Table 19.1.3</td><td>
<table>
<tr><th colspan="3">Memory allocation selection bits</th><th rowspan="2">Programmable area</th></tr>
<tr><th>b2</th><th>b1</th><th>b0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>01000_{16}–$1FFFF_{16}$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>02000_{16}–$1FFFF_{16}$</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>08000_{16}–$1FFFF_{16}$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>08000_{16}–$0FFFF_{16}$</td></tr>
</table>
</td><td>
<table>
<tr><th colspan="3">Memory allocation selection bits</th><th rowspan="2">Programmable area</th></tr>
<tr><th>b2</th><th>b1</th><th>b0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>01000_{16}–$1FFFF_{16}$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>02000_{16}–$1FFFF_{16}$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>01000_{16}–$0FFFF_{16}$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>08000_{16}–$0FFFF_{16}$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>$0C000_{16}$–$0FFFF_{16}$</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>08000_{16}–$1FFFF_{16}$</td></tr>
</table>
</td></tr>
<tr><td></td><td>PART 1
P21-80</td><td>
A
② When writing data to the oscillation circuit control register 1
……
• When initializing the clock prescaler
Write data "80_{16}." (LDM instruction)
↓
Clock prescaler is reset.
• When writing to bits 0 to 2
Write data "01010101_{16}." (LDM instruction)
↓
Write data "$0000\underline{0}XXX_{16}$." (LDM instruction) ← Next instruction
↓
Bits 0 to 2 are set.
③ When writing data to the memory allocation control register
……
Write data "01010101_{16}." (LDM instruction)
↓
Write data "$0000\underline{1}XXX_{16}$." (LDM instruction) ← Next instruction
↓
Bits 0 to 2 are set.
</td><td>
A
② When writing data to the oscillation circuit control register 1
……
• When initializing the clock prescaler
Write data "80_{16}." (LDM instruction)
↓
Clock prescaler is reset.
• When writing to bits 0 to 2
Write data "01010101_{2}." (LDM instruction)
↓
Write data "$0000\underline{1}XXX_{2}$." (LDM instruction) <u>(Note)</u> ← Next instruction
↓
Bits 0 to 2 are set.
<u>Note:</u> <u>In the case of the 7735 Group, write data "$00000XXX_{2}$."</u>
③ When writing data to the memory allocation control register
……
Write data "01010101_{2}." (LDM instruction)
↓
Write data "$0000\underline{0}XXX_{2}$." (LDM instruction) ← Next instruction
↓
Bits 0 to 2 are set.
</td></tr>
<tr><td></td><td>PART 1
P21-82
Line 18</td><td>••••• addresses $00\underline{8}000_{16}$ to $00FFFF_{16}$.</td><td>••••• addresses $00\underline{C}000_{16}$ to $00FFFF_{16}$.</td><td></td></tr>
</table>

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USER'S MANUAL
7733 Group/7735 Group/7736 Group

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Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan