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82571EB/82572EI Gigabit Ethernet Controller

Networking Silicon

Product Datasheet

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Revision 1.2
August 2006

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Revision History

Date	Revision	Notes
Oct 2002	0.15	Initial Release
Feb 2003	0.5	Revised ballout, added package drawing, added visual pin descriptions, changed some ball names to “EXP” ball naming convention.
Aug 2003	0.6	• Updated power specifications. • Changed names to “PE” naming convention • Revised signal descriptions, pinout information tables, and ballout grid. • Modified LAN disable ballout to cover A-0 (DEV_DIS_N) and B-0 (DEV_OFF_N). • Removed integrated Baseboard Management Controller.
Oct 2003	0.75	• Updated operating temperature • Changed DEV_DIS_N pin (A Stepping) to RSVD_NC • Corrected LED descriptions in signal descriptions in signal descriptions • Added Absolute Maximum Ratings • Added General Operating Conditions • Added Power Specifications • Added voltage Ramp and Sequencing Recommendations • Added DC I/O Specifications • Added Timing Specifications • Edited Thermal Characteristics
May 2004	0.85	• Section 4.4, Figure 2; Section 4.5.1.1;Section 4.5.1.2, Figure 5; Section 4.5.2, Figure 6; Section 5.1, Figure 7; Section 5.1, Figure 8; Section 5.4, Figure 9, ball T6 changed to PERST_N.
January 2005	0.90	• Included 82572EI information • Updated signal names • Updated power numbers
May 2005	0.92	• Corrected 1.1V Operating Range in Table 2
Nov 2005	1.0	• Changed document status to “Intel Confidential,” updated power values, made minor corrections to text
March 2006	1.1	• Corrected pinlists • Pin A7 DEVICE_DIS_N has been moved to Reserved and No Connect Signals; this pin is now Reserved. Refer to 82571EB/82571EI Design Guide for guidance on proper connection. • Pin R4 LAN_PWR_GOOD has been moved to Reserved and No Connect Signals; this pin is now Reserved. Refer to 82571EB/82571EI Design Guide for guidance on proper connection.
August 2006	1.2	• Corrected signal mames, minor text corrections

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1.0 Introduction

The Intel 82571EB Gigabit Ethernet Controller is a single, compact component with two fully integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) ports. The Intel 82572EI Gigabit Ethernet Controller is a single-port version of the controller in the same package. These devices use the PCI Express* architecture (Rev. 1.0a). The Intel 82571EB/82572EI enables dual- or single-port Gigabit Ethernet implementation in a very small area and can be used for server and workstation network designs with critical space constraints.

The Intel 82571EB/82572EI provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). Ports also contain a Serializer-Deserializer (SERDES) to support 1000Base-SX/LX (optical fiber) and Gigabit backplane applications. In addition to managing MAC and PHY Ethernet layer functions, the controller manages PCI Express packet traffic across its transaction, link, and physical/logical layers.

The Intel 82571EB/82572EI's on-board System Management Bus (SMB) ports enable network manageability implementations required by information technology personnel for remote control and alerting via the LAN. With SMB, management packets can be routed to or from a management processor. The SMB ports enable industry standards, such as Alert Standard Format (ASF) 2.0, to be implemented using the 82571EB/82572EI controller. In addition, on-chip ASF 2.0 circuitry provides alerting and remote control capabilities with standardized interfaces. Enhanced pass-through capabilities also allow system remote control over standardized interfaces.

The 82571EB/82572EI Gigabit Ethernet Controller with PCI Express architecture is designed for high performance and low memory latency. The device is optimized to connect to a system Memory Control Hub (MCH) using four PCI Express lanes. Alternatively, the 82571EB/82572EI controller can connect to an I/O Control Hub (ICH6 & 7) that has a PCI Express interface.

Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. Combining a parallel and pipe-lined logic architecture optimized for Gigabit Ethernet and independent transmit and receive queues, the 82571EB/82572EI controller efficiently handles packets with minimum latency. The 82571EB/82572EI controller includes advanced interrupt handling features. The 82571EB/82572EI uses efficient ring buffer descriptor data structures, with up to 64 packet descriptors cached on chip. A large 48 KByte per port on-chip packet buffer maintains superior performance. In addition, using hardware acceleration, the controller offloads tasks from the host, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The 82571EB/82572EI is packaged in a 17 mm X 17 mm, 256-ball grid array.

1.1 Document Scope

This document contains targeted datasheet specifications for the 82571EB/82572EI Gigabit Ethernet Controller, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

1.2 Reference Documents

This application assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82571EB/82572EI Gigabit Ethernet Controller Design Guide, AP-447. Intel Corporation.
- Intel Ethernet Controllers Timing Device Selection Guide, AP-419. Intel Corporation.
- PCI Express Base Specification, Revision 1.0a. PCI Special Interest Group.
- PCI Express Card Electromechanical Specification, Revision 1.0a. PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Revision 1.1. PCI Special Interest Group.
- IEEE Standard 802.3, 2000 Edition. Institute of Electrical and Electronics Engineers (IEEE). This version incorporates various IEEE standards previously published separately.

1.3 Block Diagram

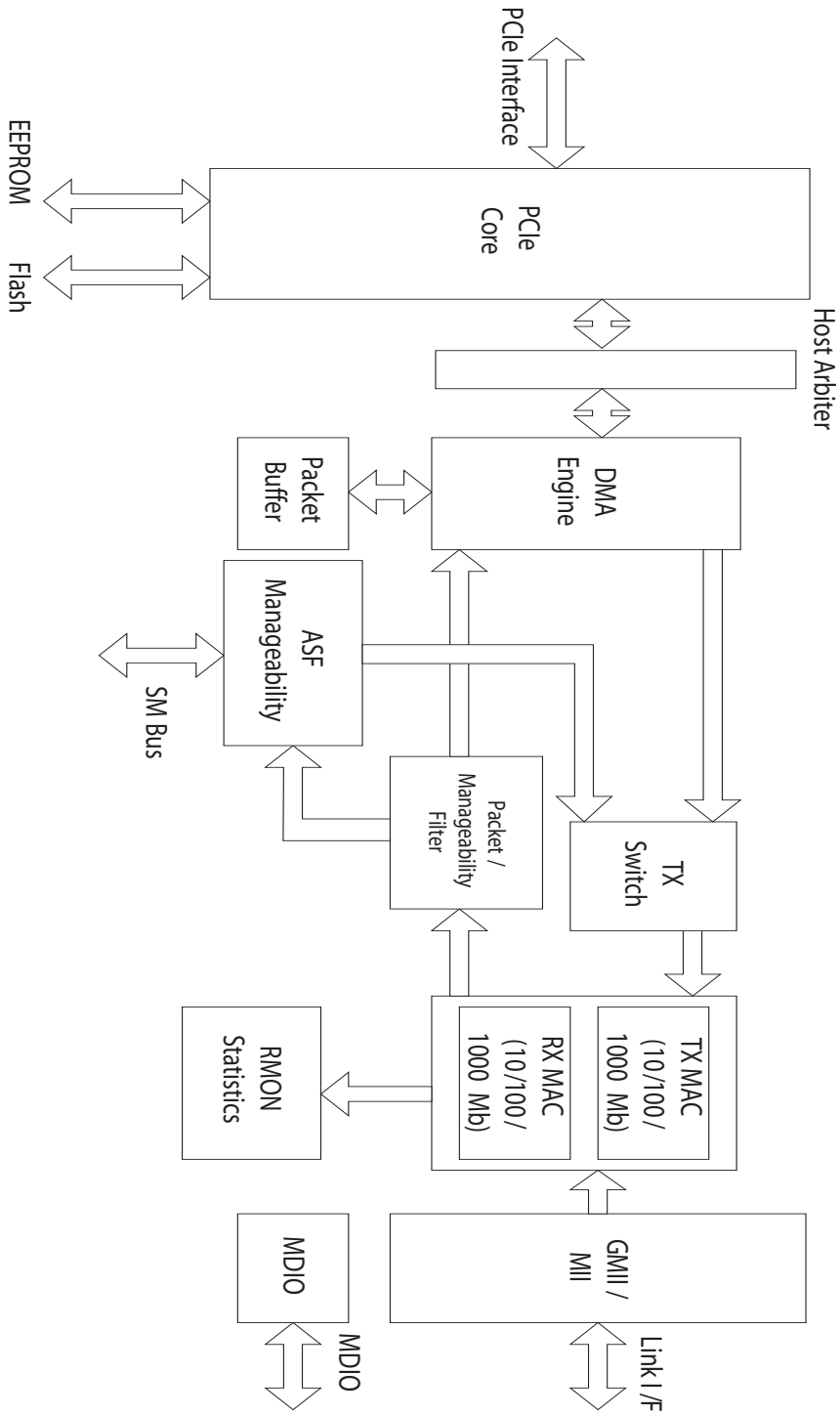

Figure 1. 82571EB/82572EI Gigabit Ethernet Controller Block Diagram (Single Port Shown)

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2.0 Features of the 82571EB/82572EI Gigabit Ethernet Controller

2.1 PCI Express Features

Features	Benefits
Uses x4 PCI Express interface on MCH device	• Bus sharing not required • Low latency path to memory • Relieves congestion for IO devices
Peak bandwidth 2 GB/s in each direction per PCI Express lane	• Supports Gigabit Ethernet at full wire speed
PCI Express Power Management	• Compatible extensions to PCI power management and ACPI • PE_WAKE_n available for wakeup event
High bandwidth density per pin	• Less congested board routing

2.2 MAC-Specific Features

Features	Benefits
Optimized transmit and receive queues	• Network packets handled without waiting or buffer overflow.
IEEE 802.3x compliant flow control support with software controllable pause times and threshold values	• Control over the transmissions of pause frames through software or hardware triggering • Frame loss reduced from receive overruns
Caches up to 64 packet descriptors (per queue)	• Efficient use of PCI Express bandwidth
Separate transmit queue per port	• Efficient packet prioritization
Programmable host memory receive buffers (256 Bytes to 16 KBytes) and cache line size (64 Bytes to 128 Bytes)	• Efficient use of PCI Express bandwidth
Wide, pipelined internal data path architecture	• Low latency data handling • Superior DMA transfer rate performance
Dual 48 KByte configurable Transmit and Receive FIFO buffers	• No external FIFO memory requirements • FIFO size adjustable to application
Descriptor ring management hardware for transmit and receive	• Simple software programming model
Optimized descriptor fetching and write-back mechanisms	• Efficient system memory and use of PCI Express bandwidth
Mechanism available for reducing interrupts generated by transmit and receive operations	• Maximizes system performance and throughput
Supports transmission and reception of packets up to 9 kB	• Enables jumbo frames

2.3 PHY Specific Features

Features	Benefits
Integrated PHY for 10/100/1000 Mbps operation	• Smaller footprint and lower power dissipation compared to multi-chip MAC and PHY solutions
IEEE 802.3ab Auto-Negotiation support	• Automatic link configuration including speed, duplex, and flow control
IEEE 802.3ab PHY compliance and compatibility	• Robust operation over the installed base of Category-5 (CAT-5) twisted pair cabling
State-of-the-art DSP architecture implements digital adaptive equalization, echo cancellation, and cross-talk cancellation	• Robust performance in noisy environments • Tolerance of common electrical signal impairments
PHY cable correction and diagnostics	• Improved end-user troubleshooting • Tolerance of common wiring faults
• Low-Power Link-Up (LPLU) • Smart Speed • Smart Power-Down	• Enables link in low-power mode • Reacts to various link speeds

2.4 Host Offloading Features

Features	Benefits
Transmit and receive IP, TCP and UDP checksum off-loading capabilities	• Lower CPU utilization
Transmit TCP segmentation	• Increased throughput and lower CPU utilization • Large send offload feature (in Microsoft* Windows* XP) compatible
IPv6 Offloading	• Checksum and segmentation capability extended to new standard packet type
Advanced packet filtering	• 16 exact matched packets (unicast or multicast) • 4096-bit hash filter for multicast frames • Promiscuous (unicast and multicast) transfer mode support • Optional filtering of invalid frames
IEEE 802.1q VLAN support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags	• Ability to create multiple virtual LAN segments
Descriptor ring management hardware for transmit and receive	• Optimized fetching and write-back mechanisms for efficient system memory and PCI bandwidth usage
9 kB jumbo frame support	• High throughput for large data transfers on networks supporting jumbo frames

2.5 Manageability Features

Features	Benefits
Manageability features: • Two SMBus ports one with Fast Management Link Capability • Alerting Standards Format 1.0 and 2.0 • Advanced Power Management (Wake on LAN)	• Alerting and control via standardized interfaces • Network management flexibility • Manageability data transfers up to 8 Mb/s peak rate
On-board microcontroller	• Enables effective ASF 2.0 implementations • Promotes customized designs • Allows packets routing to and from either LAN port and a server management processor • Supports serial text and keyboard redirection • Supports remote floppy/CD
Preboot eXecution Environment (PXE) Flash interface support (32-bit nd 64-bit)	• Local Flash interface for PXE image
Compliance with PCI Power Management 1.1 and ACPI 2.0 register set compliant including: • D0 and D3 power states • Network Device Class Power Management Specification 1.1	• PCI power management capability requirements for PC and embedded applications
SNMP and RMON statistic counters	• Easy system monitoring with industry standard consoles
SDG 3.0, WfM 3.0, and PC2001 compliance	• Remote network management capabilities through DMI 2.0 and SNMP software
Wake on LAN support	• Packet recognition and wake-up for NIC and LOM applications without software configuration

2.6 Additional Device Features

Features	Benefits
82571EB: Two complete Gigabit Ethernet connections in a single device	• Inherent dual port teaming ability • High availability using one port for failover • Higher throughput than single Gigabit Ethernet port • Lower latency due to one electrical load on the bus • Saves critical board space • Reduced multi-port Gigabit Ethernet costs
Integrated SERDES	• Supports backplane and fiber applications as well as copper-based Gigabit
Four activity and link indication outputs (per port) that directly drive LEDs	• Link and activity indications (10, 100, and 1000 Mbps) on each port
Programmable LED functionality	• Software definable function (speed, link, and activity) and blinking allowing flexible LED implementations
Internal PLL for clock generation can use a 25 MHz crystal	• Lower component count and system cost

Features	Benefits
JTAG (IEEE 1149.1) Test Access Port built in silicon	• Simplified testing using boundary scan
Four software definable pins per port	• Additional flexibility for LEDs or other low speed I/O devices
Provides loopback capabilities	• Validates silicon integrity

2.7 Technology Features

Features	Benefits
256-pin Flip-Chip Ball Grid Array (FC-BGA) package	• 17 mm X 17 mm component occupies only 28% more board space than a single port device
Implemented in 90 nm CMOS process	• Offers lowest geometry to minimize power and size while maintaining Intel quality and reliability standards
Operating temperature: 1000BASE-T, 0° C to 55° C (with thermal management) 1000BASE-T, 0° C to 70° C (with increased thermal management) 1000BASE-SX/LX (or SERDES backplane), 0°C to 70° C Storage temperature 65° C to 140° C	• Simple thermal design
Typical targeted power dissipation: ~3.50 W @ D0 1000 Mbps ~0.78mW @ D3 100 Mbps (wakeup enabled) ~0.36mW @ D3 wakeup disabled	• Minimizes impact of incorporating Gigabit instead of Fast Ethernet.

3.0 Signal Descriptions

Note: The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

3.1 Signal Type Definitions

The signals of the 82571EB/82572EI controller are electrically defined as follows:

Name	Definition
I	**Input.** Standard input only digital signal.
O	**Output.** Standard output only digital signal.
TS	**Tri-state.** Bi-directional three-state digital input/output signal.
OD	**Open Drain.** Wired-OR with other agents. The signaling agent asserts the OD signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may require two or three clock periods to fully restore the signal to the de-asserted state.
A	**Analog.** PCI Express*, SERDES, or, PHY analog signal.
A(I)	**Analog-Input.** Standard input only analog signal.
A(O)	**Analog-Output.** Standard output only analog signal.
P	**Power.** Power connection, voltage reference, or other reference connection.

3.2 PCI Express Interface

Symbol	Type	Name and Function
PERn[3:0] PERp[3:0]	A(I)	**High Speed Serial Receive Data.** These signals connect to corresponding PETn and PETp signals on a system motherboard or a PCI Express connector. Series AC coupling capacitors are required at the transmitter end. The PCI Express differential inputs are clocked at 2.5 Gb/s.
PETn[3:0] PETp[3:0]	A(O)	**High Speed Serial Transmit Data.** These signals connect to corresponding PERn and PERp signals on a system motherboard or a PCI Express connector. Series AC coupling capacitors are required at the 82571EB/82572EI controller end. The PCI Express differential outputs are clocked at 2.5 Gb/s.
PE_RCOMPp PE_RCOMPn	P	**High Speed Serial Impedance Compensation.** Connect the recommended resistor value across these balls. Refer to the 82571EB/82572EI Design Guide for the recommended value.
PE_CLKp PE_CLKn	I	**100 MHz Differential Clock for the PCI Express Interface.** The reference clock is furnished by the system and has a 300 ppm frequency tolerance.
PE_RSTn	I	**PCI Express Reset.** When the signal is low, all PCI Express functions are held in reset. When the signal is high, it denotes that main power is available to the 82571EB/82572EI controller and the reference clock is running. In systems with a PCI Express add-in card, this signal routes to the connector.

3.3 Power Management Signals

Symbol	Type	Name and Function
AUX_PWR	I	**Auxiliary Power Present.** If the Auxiliary Power signal is high, then auxiliary power is present and the 82571EB/82572EI device should support the $D3_{cold}$ power state.
LAN0_DIS_N LAN1_DIS_N/ RSVD_B8	I	**LAN Disables 0 and 1.** Disables individual Ethernet ports. State is latched upon a rising edge of PERST_N or a PCI Express reset event. This pin has an internal pull-up resistor.
DEV_OFF_N	I	**Device Off.** Asynchronously disables Ethernet controller, including voltage regulator control outputs if selected in CTRL_EXT. This pin has an internal pull-up resistor.
PE_WAKEn	OD	**Wake.** The 82571EB/82572EI device drives this signal low when it receives a wake-up event and either the PME Enable bit in the Power Management Control/Status Register or the Advanced Power Management Enable (APME) bit of the Wake-up Control Register (WUC) is 1b.

3.4 SMB and Fast Management Link Bus Signals

Symbol	Type	Name and Function
SMBCLK0/FLBMCK SMBCLK1	I/O	**SMB Clock.** The SMB Clock signals are open drain signals for the serial SMB interface (Ports A and B). Alternatively, when SMB Port A is configured for a Fast Management Link Bus, SMB Clock A becomes the Fast Management Link Bus Master Clock. The Fast Management Link Bus can be clocked up to 6.5 MHz.
SMBD0/FLBMD SMBD1	I/O	**SMB Data.** The SMB Data signals are open drain signals for the serial SMB interface (Ports A and B). Alternatively, when SMB Port A is configured for a Fast Management Link Bus, SMB Data A becomes Fast Management Link Bus Master Data.
SMBALRT_N/ PCI_PWR_GOOD	I/O	**SMB Alert.** The SMB Alert signal is an open drain signal for serial SMB Port A. In ASF mode, this signal acts as a power good input. It acts as an alert input in 82559 compatible mode.
FLBSD	O	**Fast Management Link Bus Slave Data.** When SMB Port A is configured for a Fast Management Link Bus, this signal becomes the serial data path for slave data from the 82571EB/82572EI controller.
FLBINTEX	O	**Fast Management Link Bus Interrupt Extension.** Driven by the 82571EB/82572EI controller as a slave to alert the master to read data. Alternatively, it signals the master to extend the low phase of the clock.

3.5 EEPROM and Serial FLASH Interface Signals

Symbol	Type	Name and Function
EE_DI	O	**EEPROM Data Input.** The EEPROM Data Input pin is used for output to the SPI EEPROM memory device.
EE_DO	I	**EEPROM Data Output.** The EEPROM Data Output pin is used for input from the SPI EEPROM memory device. The EE_DO includes an internal pull-up resistor.
EE_CS_N	O	**EEPROM Chip Select.** The EEPROM Chip Select signal is used to enable the device.
EE_SK	O	**EEPROM Serial Clock.** The EEPROM Shift Clock provides the clock rate for the SPI EEPROM interface, which is approximately 2 MHz.
FLSH_CE_N	O	**FLASH Chip Enable Output.** Used to enable FLASH device.
FLSH_SCK	O	**FLASH Serial Clock Output**.
FLSH_SI	O	**FLASH Serial Data Input.** This pin is an output to the memory device.
FLSH_SO	I	**FLASH Serial Data Output.** This pin is an input from the memory device.

3.6 LED Signals

Symbol	Type	Name and Function
LED0_0	O	**LED0_0.** Programmable LED output for Port A. As the Link LED, it indicates link connectivity on Port A.
LED0_1	O	**LED0_1.** Programmable LED output for Port A. As the Activity LED, it flashes to indicate receive activity on Port A for packets destined for this node.
LED0_2	O	**LED0_2.** Programmable LED output for Port A. As the Link 100 LED, it indicates link at 100 Mbps for Port A.
LED0_3	O	**LED0_3.** Programmable LED output for Port A. As the Link 1000 LED, it indicates link at 1000 Mbps for Port A.
LED1_0/ RSVD_P8	O	**LEDB0_N.** Programmable LED output for Port B. As the Link LED, it indicates link connectivity on Port B. (82571 EB only.)
LED1_1/ RSVD_R8	O	**LED1_1.** Programmable LED output for Port B. As the Activity LED, it flashes to indicate receive activity on Port B for packets destined for this node. (82571 EB only.)
LED1_2/ RSVD_T8	O	**LED1_2.** Programmable LED output for Port B. As the Link 100 LED, it indicates link at 100 Mbps for Port B. (82571 EB only.)
LED1_3/ RSVD_P9	O	**LED1_3.** Programmable LED output for Port B. As the Link 1000 LED, it indicates link at 1000 Mbps for Port B. (82571 EB only.)

3.7 Other Signals

Symbol	Type	Name and Function
SDP0_1 SDP0_2 SDP0_3 SDP0_4 SDP1_1/RSVD_P6 SDP1_2/RSVD_B6 SDP1_3/RSVD_C6 SDP1_4/RSVD_R6	TS	**Software Defined Pin.** The Software Defined Pins are programmable with respect to input and output capability. SDP0_3 and SDP1_3 may optionally be configured as interrupt inputs. SDP signals default to inputs upon power-up, but may be configured differently by the EEPROM.

3.8 Crystal Signals

Symbol	Type	Name and Function
XTAL1	I	**Crystal One.** The Crystal One pin is a 25 MHz input signal. It should be connected to a parallel resonant crystal with a frequency tolerance of 30 ppm or better. The other end of the crystal should be connected to XTAL2. Optionally, an oscillator can be connected to XTAL 1. See the design guide for more information..
XTAL2	O	**Crystal Two.** Crystal Two is the output of an internal oscillator circuit used to drive a crystal into oscillation.

3.9 PHY Analog Signals

Port 0

Symbol	Type	Name and Function
RBIAS0p RBIAS0n	P	**Bias Resistors.** These are the reference connections for the Media Dependent Interface. The recommended resistor value should be connected across the positive/negative pair, even if the MDI interface is not used. Refer to the 82571EB/82572EI Design Guide for the recommended value.
MDI_PLUS0_0 MDI_MINUS0_0	A	**Media Dependent Interface [0].** **1000BASE-T**: In MDI configuration, these correspond to BI_DA+/-, and in MDI-X configuration, they correspond to BI_DB+/-. **100BASE-TX**: In MDI configuration, these are used for the transmit pair, and in MDI-X configuration, they are used for the receive pair. **10BASE-T**: In MDI configuration, they are used for the transmit pair, and in MDI-X configuration, used for the receive pair.

Symbol	Type	Name and Function
MDI_PLUS0_1 MDI_MINUS0_1	A	**Media Dependent Interface [1].** **1000BASE-T**: In MDI configuration, these correspond to BI_DB+/-, and in MDI-X configuration, they correspond to BI_DA+/-. **100BASE-TX**: In MDI configuration, they are used for the receive pair, and in MDI-X configuration, they are used for the transit pair. **10BASE-T**: In MDI configuration, they are used for the receive pair, and in MDI-X configuration, they are used for the transit pair.
MDI_PLUS0_2 MDI_MINUS0_2	A	**Media Dependent Interface [2].** **1000BASE-T**: In MDI configuration, these correspond to BI_DC+/-, and in MDI-X configuration, they correspond to BI_DD+/-. **100BASE-TX**: Unused. **10BASE-T**: Unused.
MDI_PLUS0_3 MDI_MINUS0_3	A	**Media Dependent Interface [3].** **1000BASE-T**: In MDI configuration, these correspond to BI_DD+/-, and in MDI-X configuration, they correspond to BI_DC+/-. **100BASE-TX**: Unused. **10BASE-T**: Unused.

Port 1 (82571EB Only)

Symbol	Type	Name and Function
RBIAS1p/ RSVD_M14 RBIAS1n/ RSVD_N14	P	**Bias Resistors.** These are the reference connections for the Media Dependent Interface. The recommended resistor value should be connected across the positive/negative pair, even if the MDI interface is not used. Refer to the 82571EB/82572EI Design Guide for the recommended value.
MDI_PLUS1_0/ RSVD_T14 MDI_MINUS1_0/ RSVD_R14	A	**Media Dependent Interface [0].** **1000BASE-T**: In MDI configuration, these correspond to BI_DA+/-, and in MDI-X configuration, they correspond to BI_DB+/-. **100BASE-TX**: In MDI configuration, they are used for the transmit pair, and in MDI-X configuration, they are used for the receive pair. **10BASE-T**: In MDI configuration, they are used for the transmit pair, and in MDI-X configuration, they are used for the receive pair.
MDI_PLUS1_1/ RSVD_T15 MDI_MINUS1_1/ RSVD_R15	A	**Media Dependent Interface [1].** **1000BASE-T**: In MDI configuration, these correspond to BI_DB+/-, and in MDI-X configuration, they correspond to BI_DA+/-. **100BASE-TX**: In MDI configuration, they are used for the receive pair, and in MDI-X configuration, they are used for the transit pair. **10BASE-T**: In MDI configuration, they are used for the receive pair, and in MDI-X configuration, they are used for the transit pair.
MDI_PLUS1_2/ RSVD_P16 MDI_MINUS1_2/ RSVD_P15	A	**Media Dependent Interface [2].** **1000BASE-T**: In MDI configuration, these correspond to BI_DC+/-, and in MDI-X configuration, they correspond to BI_DD+/-. **100BASE-TX**: Unused. **10BASE-T**: Unused.
MDI_PLUS1_3/ RSVD_N16 MDI_MINUS1_3/ RSVD_N15	A	**Media Dependent Interface [3].** **1000BASE-T**: In MDI configuration, these correspond to BI_DD+/-, and in MDI-X configuration, they correspond to BI_DC+/-. **100BASE-TX**: Unused. **10BASE-T**: Unused.

3.10 Serializer / Deserializer Signals

Symbol	Type	Name and Function
SRDSI_0_PLUS SRDSI_0_MINUS SRDSI_1_PLUS/ RSVD_M16 SRDSI_1_MINUS/ RSVD_L16	A(I)	**SERDES Receive Pairs.** Signals SRDSI_0_PLUS and SRDSI_0_MINUS make the differential receive pair for the 1.25 GHz serial interface for Port 0. For serializer/ deserializer operation, the inputs should be coupled to ECL voltage levels. Signals SRDSI_1_PLUS and SRDSI_1_MINUS make the differential receive pair for the 1.25 GHz serial interface for Port 1. For serializer/deserializer operation, the inputs should be coupled to ECL voltage levels. If the SERDES interface is not used, these pins should not be connected.
SRDSO_0_PLUS SRDSO_0_MINUS SRDSO_1_PLUS/ RSVD_K15 SRDSO_1_MINUS /RSVD_L15	A(O)	**SERDES Transmit Pairs.** Signals SRDSO_0_PLUS and SRDSO_0_MINUS make the differential transmit pair for the 1.25 GHz serial interface for Port 0. For serializer/ deserializer operation, the outputs drive the LVPECL voltage levels. Signals SRDSO_1_PLUS and SRDSO_1_MINUS make the differential transmit pair for the 1.25 GHz serial interface for Port 1. For serializer/deserializer operation, the outputs drive the LVPECL voltage levels. If the SERDES interface is not used, these pins should not be connected.
SRDSA_SIG_DET SRDSB_SIG_DET/ RSVD_C4	I	**Signal Detects.** These pins (SRDSA_SIG_DET for Port 0; SRDSB_SIG_DET for Port 1) indicate whether the SERDES signals (connected to the 1.25 GHz serial interface) have been detected by the optical transceivers. If the SERDES interface is not used, the SIG_DET inputs can be left unconnected.
SRDS_RCOMPp SRDS_RCOMPn	A	**SERDES Impedance Compensation.** Connect the recommended resistor value across these balls, even if not using the SERDES interface. Refer to the 82571EB/82572EI Design Guide for the recommended value.

3.11 Test Interface Signals

Symbol	Type	Name and Function
JTCK	I	**JTAG Test Access Port Clock.**
JTDI	I	**JTAG Test Access Port Test Data In.**
JTDO	O	**JTAG Test Access Port Test Data Out.**
JTMS	I	**JTAG Test Access Port Mode Select.**

Symbol	Type	Name and Function
IEEE_TEST0p IEEE_TEST0n IEEE_TEST1p/ RSVD_R13 IEEE_TEST1n/ RSVD_T13	O	**IEEE Analog Test Pins.** Differential outputs providing reference clocks for IEEE PHY conformance verification. For prototype testing, connect each pair to two-pin headers. For production systems, leave pins unconnected.
THERM_Dp THERM_Dn	O	**Thermal Diode Reference.** Can be used to measure the Si temperature.
TEST_EN	I	**Factory Test Pin.** Attach a 1 KΩ pull-down resistor to ground for normal operation.

3.12 Power Supply Connections

3.12.1 Digital and Analog Supplies

Symbol	Type	Name and Function
VCC33	P	**3.3V Digital Power Supply.** For I/O circuits.
VCC18	P	**1.8V Analog Power Supply.** For PHY analog, PHY I/O, PCI Express analog, and Phase Lock Loop circuits, Connect all 1.8V pins to a single power supply.
VCC11	P	**1.1V Digital Power Supply.** For core digital, PHY digital, PCI Express digital and clock circuits, connect all 1.1V pins to a single power supply.

3.12.2 Grounds, Reserved Pins and No Connects

Symbol	Type	Name and Function
VSSA	P	**Analog Ground.** Connects to PHY analog circuits. Connect directly to analog ground.
VSS	P	**Digital Ground.** Connects to core and digital I/O. Connect to GND.
RSVD_ pin#	P	**Reserved Pin.** These pins are reserved by Intel and may have factory test functions. For normal operation, do not connect any circuitry to these pins (allow them to “float”). Some special configurations may require pull-up or pull-down resistors on these pins. Please refer to the 82571EB/82572EI design guide for more information.
NC_pin#	P	**No Connect.** This pin is not connected internally.

4.0 Voltage, Temperature, and Timing Specifications

4.1 Targeted Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[a]

Symbol	Parameter	Min	Max	Unit
VCC(3.3)	DC supply voltage on 3.3V pins with respect to VSS	VSS - 0.5	4.6	V
VCC(1.8)	DC supply voltage on 1.8V pins with respect to VSS[b]	VSS - 0.3	2.5	V
VCC(1.1)	DC supply voltage on 1.1V pins with respect to VSS[b]	VSS - 0.2	1.7	V
V_I / V_O	3.3V I/O Voltage 1.8V I/O Voltage 1.1V I/O Voltage	VSS - 0.5 VSS - 0.3 VSS - 0.2	4.6 2.5 1.7	V
I_O	DC output current	N/A	30	mA
$T_{storage}$	Storage temperature range	-65	140	°C
	ESD per MIL_STD-883 Test Method 3015, Specification 2001V Latchup Over/Undershoot: 150 mA, 125° C	N/A	VDD overstress: VDD(3.3) * (7.2 V)	V

a. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded for an indefinite duration. These values should not be used as the limits for normal device operations.
b. During normal device power up and power down, the 1.8V and 1.1V supplies must not ramp before the 3.3V supply.

4.2 Targeted Recommended Operating Conditions

4.2.1 General Operating Conditions

Table 2. Recommended Operating Conditions [a]

Symbol	Parameter	Min	Max	Unit
VCC(3.3)	DC supply voltage on 3.3V pins	3.0	3.6	V
VCC(1.8)	DC supply voltage on 1.8V pins[b, c]	1.71	1.89	V
VCC(1.1)	DC supply voltage on 1.1V pins	1.045	1.155	V
tR / tF	Input rise/fall time (normal input)	0	200	ns
T_a	Operating temperature range (ambient)	0	55[d]	°C
T_J	Junction temperature	N/A	≤110	°C

a. Sustained operation of the device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent damage. Device functionality to stated DC and AC limits is not guaranteed, if conditions exceed recommended operating conditions.
b. See Section 4.2.2 for voltage ramp and sequencing recommendations.
c. Operation with internal voltage regulator control of PNP pass transistor may exceed this range due to 82571EB process skew tracking.
d. 1000BASE-T designs require thermal management (heatsink and/or forced air flow) to achieve 0° to 55° C operation. Increased thermal management can increase this temperature range to 0° to 70° C. Applications using the SERDES interface are rated for 0° to 70° C without thermal management.

4.2.2 Voltage Ramps

Table 3. 3.3V Supply Voltage Ramp

Parameter	Description	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100[a]	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any time between 10% to 90%	24	28000	mV/ms
Operational Range	Voltage range for normal operating conditions	3	3.6	V
Ripple	Maximum voltage ripple at a bandwidth equal to 50 MHz	N/A	70	$mV_{peak-peak}$
Overshoot Settling Time	Overshoot time upon ramp[b]	N/A	0.05	ms
Overshoot	Maximum voltage allowed[b]	N/A	100	mV

a. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
b. Excessive overshoot can affect long term reliability.

Table 4. 1.8V Supply Voltage Ramp

Parameter	Description	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100[a]	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any time between 10% to 90%	14	60000	mV/ms
Operational Range	Voltage range for normal operating conditions	1.71	1.89	V
Ripple	Maximum voltage ripple at a bandwidth equal to 1 MHz	N/A	40	$mV_{peak-peak}$
Overshoot SettlingTime	Overshoot time upon ramp[b]	N/A	0.1	ms
Overshoot	Maximum voltage allowed[b]	N/A	100	mV

a. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
b. Excessive overshoot can affect long term reliability.

Table 5. 1.1V Supply Voltage Ramp

Parameter	Description	Min	Max	Unit
Rise Time	Time from 10% to 90% mark	0.1	100[a]	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any time between 10% to 90%	7.6	33600	mV/ms
Operational Range	Voltage range for normal operating conditions	1.045	1.155	V

Table 5. 1.1V Supply Voltage Ramp

Ripple	Maximum voltage ripple at a bandwidth equal to 1 MHz	N/A	40	$mV_{peak-peak}$
Overshoot SettlingTime	Overshoot time upon ramp[b]	N/A	0.05	ms
Overshoot	Maximum voltage allowed[b]	N/A	100	mV

a. Good design practices achieve voltage ramps to within the regulation bands in approximately 20 ms or less.
b. Excessive overshoot can affect long term reliability.

4.2.3 Voltage Power Sequencing Options

To meet 375 mA inrush current requirements (not including external capacitors) the ramp time should be 5 ms -100 ms on all power rails. For faster ramps (100 us - 5 ms), expect higher inrush current due to the high charging current of the decoupling capacitors of 3.3V, 1.8V and 1.1V rails.

4.3 DC Specifications

Table 6. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VCC(3.3)	DC supply voltage on 3.3V pins		3.00	3.30	3.60	V
VCC(1.8)	DC supply voltage on 1.8V pins		1.71	1.80	1.89	V
VCC(1.1)	DC supply voltage on 1.1V pins		1.045	1.100	1.155	V

4.3.4 Power Specifications--82571EB

Table 7. D0a--Active Link

	D0a--Active Link					
	@10 Mbps	@100 Mbps	@ 1000 Mbps (copper)		@ 1000 Mbps (SERDES)	
	Typ Icc (mA)[a]	Typ Icc (mA)[a]	Typ Icc (mA)[a]	Max Icc (mA)[a]	Typ Icc (mA)[a]	Max Icc (mA)[b]
3.3V	26	26	26	34	42	46
1.8V	350	399	893	913	254	282
1.1V	370	456	1022	1520	529	1002
Total Device Power	1.12W	1.31W	2.82W	3.43W	1.18W	1.76W

a. Typical conditions: operating temperature (T_A) = 25 C, nominal voltages and continuous network traffic at link speed at full duplex.

b. Maximum conditions: maximum operating temperature (T_J) values, typical voltage values and continuous network traffic at link speed at full duplex.

Table 8. D0a--Idle Link L0s Only

	D0a--Idle Link L0s Only			
	Unplugged--no link	**@10Mbps**	**@100Mbps**	**@1000Mbps (copper)**
	Typ Icc (mA)[a]			
3.3V	26	26	26	26
1.8V	130	123	306	837
1.1V	332	334	414	839
Total Device Power	0.69W	0.67W	1.10W	2.52W

a. Typical conditions: room temperature (TA)=25C, nominal voltages and idle network (no traffic) at full duplex

Table 9. D3cold

	D3cold - wake-up enabled		D3cold-wake disabled (no link)
	@10 Mbps	**@100 Mbps**	
	Typ Icc (mA)[a, b]	Typ Icc (mA)[a, b]	Typ Icc (mA)[a b]
3.3V	26	26	26
1.8V	74	243	76
1.1V	133	236	123
Total Device Power	0.37W	0.78W	0.36W

a. D3 Cold activated on a Windows Server 2003 OS--using Hbernate mode
b. L0s enable, L1 disabled

Table 10. D(r) Unintialized

	D(r) Uninitialized	
	Disabled through LAN_DIS_N Typ Icc (mA)	Disabled through DEV_OFF_N Typ Icc (mA)
3.3V	26	26
1.8V	63	68
1.1V	130	83
Total Device Power	0.34W	0.30W

4.3.5 Power Specifications--82572EI

Table 11. D0a--Active Link

	D0a--Active Link			
	@10 Mbps	@100 Mbps	@ 1000 Mbps (copper)	
	Typ Icc (mA)[a]	Typ Icc (mA)[a]	Typ Icc (mA)[a]	Max Icc (mA)[a]
3.3V	26	26	26	34
1.8V	210	211	484	502
1.1V	291	232	494	1023
Total Device Power	0.78W	0.72W	1.50W	2.14W

a. Typical conditions: operating temperature (T_A) = 25 C, nominal voltages and continuous network traffic at link speed at full duplex.

Table 12. D0a--Idle Link

	D0a--Idle Link L0s Only			
	Unplugged--no link	**@10Mbps**	**@100Mbps**	**@1000Mbps (copper)**
	Typ Icc (mA)[a]			
3.3V	26	26	26	26
1.8V	111	102	199	425
1.1V	176	179	218	839
Total Device Power[b]	0.48W	0.47W	0.68W	1.77W

a. Typical conditions: room temperature (TA)=25C, nominal voltages and idle network (no traffic) at full duplex
b. LOs enabled; L1 disabled

Table 13. D3cold

	D3cold - wake-up enabled		D3cold-wake disabled; unplugged, no link
	@10 Mbps	**@100 Mbps**	
	Typ Icc (mA)[a, b]	Typ Icc (mA)[a, b]	Typ Icc (mA)[a b]
3.3V	26	26	26
1.8V	77	173	84
1.1V	120	163	110
Total Device Power	0.36W	0.58W	0.36W

a. D3 Cold activated on a Windows Server 2003 OS--using Hbernate mode
b. LOs enabled, L1 disabled

Table 14. D(r) Unintialized

	D(r) Uninitialized	
	Disabled through LAN_DIS_N Typ Icc (mA)	**Disabled through DEV_OFF_N Typ Icc (mA)**
3.3V	26	26

Table 14. D(r) Unintialized

	D(r) Uninitialized	
	Disabled through LAN_DIS_N Typ Icc (mA)	Disabled through DEV_OFF_N Typ Icc (mA)
1.8V	60	68
1.1V	114	83
Total Device Power	0.32W	0.30W

4.3.6 I/O Characteristics

Table 15. I/O Characteristics[a]

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage		2.0	N/A	VCC(3.3) + 0.5	V
V_{IL}	Input low voltage		-0.5	N/A	0.8	V
I_{IN}	Input current	V_{IN} = VDD(3.3) or V_{SS}	-15	N/A	15	µA
V_{OH}	Output high voltage	I_{OH} = -16 mA V_{CC} = Min	2.4	N/A	N/A	V
		I_{OH} = -100 µA V_{CC} = Min	V_{CC} - 0.02	N/A	N/A	
V_{OL}	Output low voltage	I_{OL} = 16 mA V_{CC} = Min	N/A	N/A	0.4	V
		I_{OL} = 100 µA V_{CC} = Min	N/A	N/A	0.2	
I_{OZ}	Off-state output leakage current	$V_O = V_{CC}$ or V_{SS}	-10	N/A	10	µA
C_{IN}[b]	Input capacitance		N/A	2.5	N/A	pF
PU	Internal pull-up		2.6	N/A	5.5	kΩ

a. The input buffer also has hysteresis > 160 mV.
b. C_{in}= 2.5 pF(maximum input capacitance), C_{out} = 16 pF (characterized max output load capacitance per 160 MHz).

4.4 Targeted AC Characteristics

Table 16. 25 MHz Clock Input Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f0	Frequency	N/A	25.000	N/A	MHz
df0	Frequency Variation	-50	N/A	+50	ppm
Dc	Duty Cycle	40	N/A	60	%
tr	Rise Time	N/A	N/A	5	ns
tf	Fall Time	N/A	N/A	5	ns
Jptp	Clock Jitter (peak-to-peak)[a]	N/A	N/A	250	ps
C_{in}	Input Capacitance	N/A	20	N/A	pF
T	Operating Temperature	N/A	N/A	70	°C
Aptp	Input clock amplitude (peak-to-peak)	1.0	1.2	1.3	V
Vcm	Clock common mode	N/A	0.6	N/A	V

a. Clock jitter is defined according to the recommendations of part 40.6.1.2.5 IEEE 1000Base-T Standard (at least 10^5 clock edges, filtered by HPF with cut off frequency of 5000 Hz).

Table 17. Reference Crystal Specification Requirements

Specification	Value
Vibrational Mode	Fundamental
Nominal Frequency	25.000 MHz at 25 °C
Frequency Tolerance	• ±30 ppm recommended • ±50 ppm across the entire operating temperature range (required by IEEE specifications)
Temperature Stability	+/- 30 ppm at 0 °C to 70 °C
Calibration Mode	Parallel
Load Capacitance	20 pF to 24 pF
Shunt Capacitance	6 pF maximum
Series Resistance, Rs	50 Ω maximum
Drive Level	0.5 mW maximum
Aging	+/- 5.0 ppm per year maximum
Insulation Resistance	500 MΩ minimum at DC 100 V
Board Capacitance	4 pF
External Capacitors	27 pF
Board Resistance	0.1 Ω

Table 18. Link Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
fGTX[a]	GTX_CLK frequency	N/A	125	N/A	MHz

a. GTX_CLK is used externally for test purposes only.

Table 19. EEPROM Interface Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
fSK	SPI EEPROM Clock	N/A	2	2.1	MHz

Table 20. AC Test Loads for General Output Pins

Symbol	Parameter	Min	Typ	Max	Unit
C_L	Capacitance of test load	N/A	16	N/A	pF

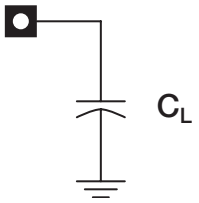

Figure 2. AC Test Loads for General Output Pins

4.5 Targeted Timing Specifications

Note: Timing specifications are preliminary and subject to change. Verify with your local Intel sales office that you have the latest information before finalizing a design.

4.5.1 PCI Express Interface

4.5.1.1 Differential Transmitter (TX) Output Specifications

Table 21. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak to Peak Output Voltage	0.800	N/A	1.2	V
$V_{TX\text{-}DE\text{-}RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
$T_{TX\text{-}EYE}$	Minimum TX Eye Width	0.70	N/A	N/A	UI
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX Output Rise/Fall Time	0.125	N/A	N/A	UI
$V_{TX\text{-}CM\text{-}ACp}$	RMS AC Peak Common Mode Output Voltage	N/A	N/A	20	mV
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	N/A	25	mV
$V_{TX\text{-}IDLE\text{-}DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	N/A	20	mV

Table 21. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Typ	Max	Units
$V_{TX\text{-}RCV\text{-}DETECT}$	The amount of voltage change allowed during Receiver Detectoin	N/A	N/A	600	mV
$RL_{TX\text{-}DIFF}$	Differential Return Loss	12	N/A	N/A	dB
$RL_{TX\text{-}CM}$	Common Mode Return Loss	6	N/A	N/A	dB
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX\text{-}SKEW}$	Lane-toLane Output Skew	N/A	N/A	500 + 2 UI	ps

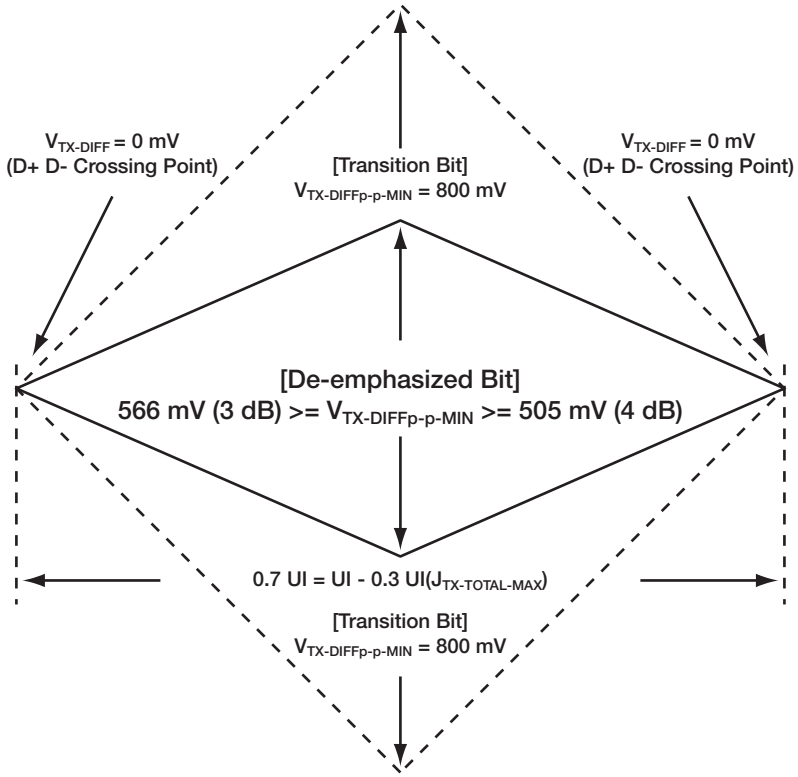

Figure 3. PCI Express Transmitter Eye Diagram

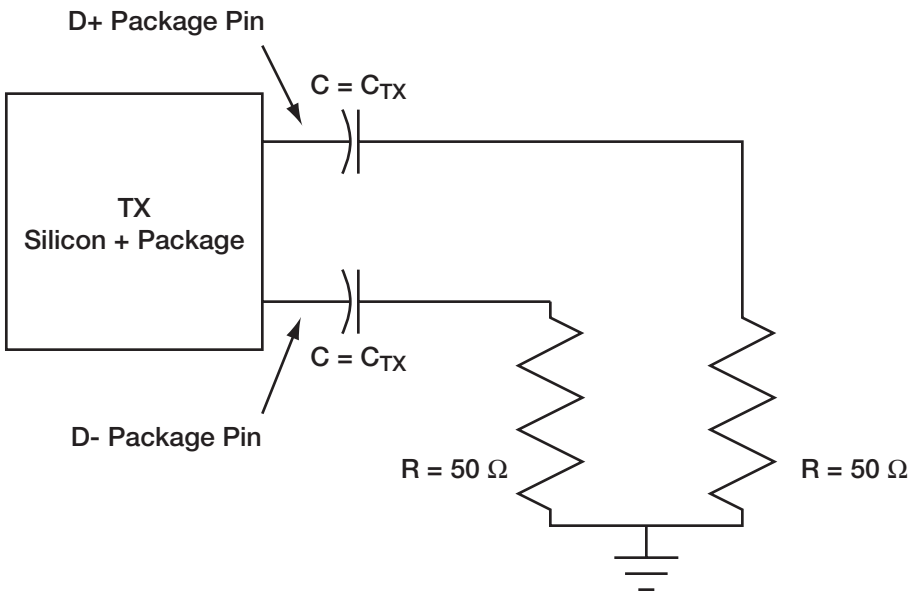

Figure 4. PCI Express Transmitter Test Load

4.5.1.2 Differential Receiver (RX) Input Specifications

Table 22. Differential Receiver (RX) Output Specifications

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Peak to Peak Output Voltage	0.175	N/A	1.2	V
$R_{TX\text{-}EYE}$	Minimum RX Eye Width	0.4	N/A	N/A	UI
$V_{RX\text{-}CM\text{-}ACp}$	AC Peak Common Mode Input Voltage	N/A	N/A	150	mV
$RL_{RX\text{-}DIFF}$	Differential Return Loss	15	N/A	N/A	dB
$RL_{RX\text{-}CM}$	Common Mode Return Loss	6	N/A	N/A	dB
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance	80	100	120	Ω
$L_{RX\text{-}SKEW}$	Total Skew	N/A	N/A	20	ns

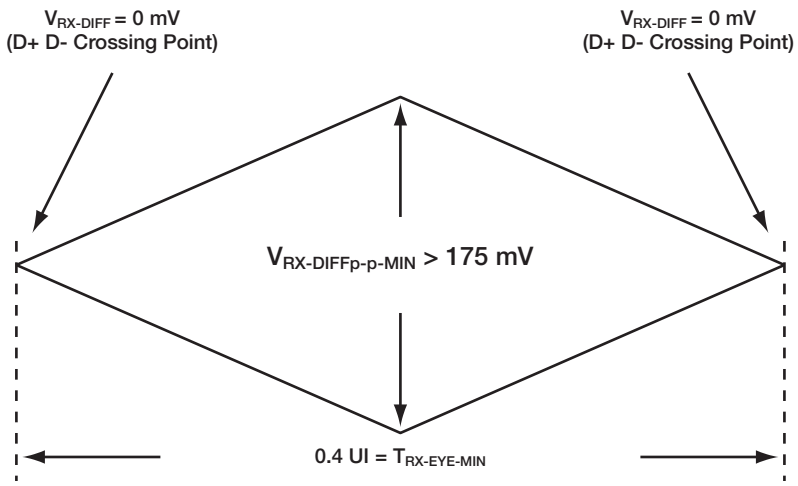

Figure 5. PCI Express Receiver Eye Diagram

4.5.2 EEPROM Interface

Table 23. EEPROM Interface Time Specifications

Symbol	Parameter	Min	Typ	Max	Units
t_{SCK}	SCK clock frequency	0	2	2.1	MHz
t_{RI}	Input rise time	N/A	2.5 ns	2	µs
t_{FI}	Input fall time	N/A	2.5 ns	2	µs
t_{WH}	SCK high time[a]	200	250	N/A	ns
t_{WH}	SCK low time[a]	200	250	N/A	ns
t_{CS}	CS high time	250	N/A	N/A	ns
t_{CSS}	CS setup time	250	N/A	N/A	ns
t_{CSH}	CS hold time	250	N/A	N/A	ns
t_{SU}	Data-in setup time	50	N/A	N/A	ns
t_{H}	Data-in hold time	50	N/A	N/A	ns
t_{V}	Output Valid	0	N/A	200	ns
t_{HO}	Output hold time	0	N/A	N/A	ns
t_{DIS}	Output disable time	N/A	N/A	250	ns
t_{WC}	Write cycle time	N/A	N/A	10	ms

a. 50% duty cycle.

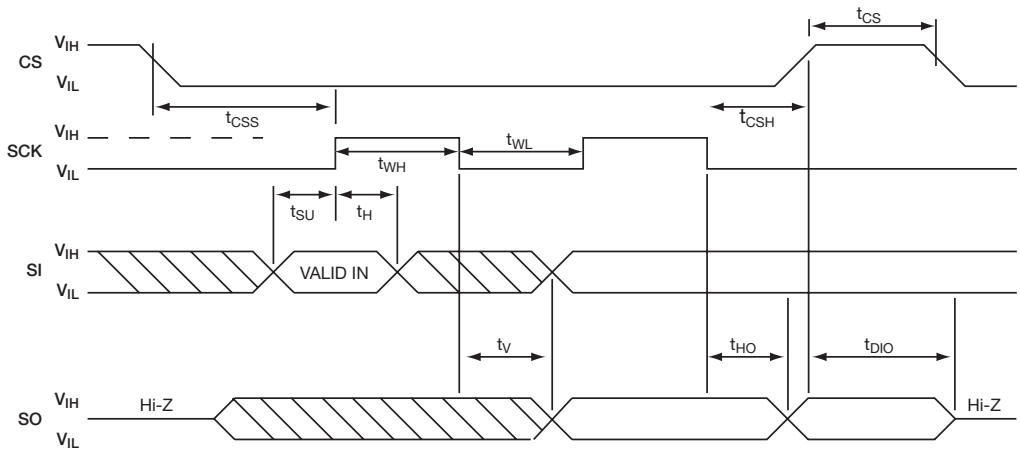

Figure 6. EEPROM Interface Time Diagram

4.5.3 FLASH Interface

Table 24. FLASH Interface Time Specifications

Symbol	Parameter	Min	Typ	Max	Units
t_{SCK}	SCK clock frequency	0	15.625	20	MHz
t_{RI}	Input rise time	N/A	2.5 ns	20	ns
t_{FI}	Input fall time	N/A	2.5 ns	20	ns
t_{WH}	SCK high time[a]	20	32	N/A	ns
t_{WH}	SCK low time[a]	20	32	N/A	ns
t_{CS}	CS high time	25	N/A	N/A	ns
t_{CSS}	CS setup time	25	N/A	N/A	ns
t_{CSH}	CS hold time	250	N/A	N/A	ns
t_{SU}	Data-in setup time	5	N/A	N/A	ns
t_H	Data-in hold time	5	N/A	N/A	ns
t_V	Output Valid	0	N/A	20	ns
t_{HO}	Output hold time	0	N/A	N/A	ns
t_{DIS}	Output disable time	N/A	N/A	100	ns
t_{EC}	Erase cycle time per sector	N/A	60	100	µs

a. 50% duty cycle.

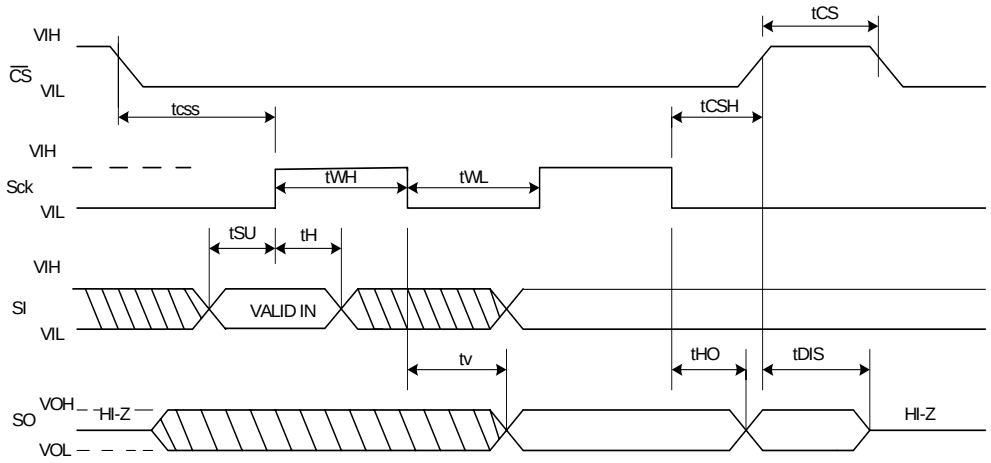

Figure 7. FLASH Interface Time Diagram

5.0 Package and Pinout Information

This section describes the 82571EB/82572EI device physical characteristics. The pin number-to-signal mapping is indicated beginning with Table 25.

Note: The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

5.1 Package Information

The 82571EB/82572EI device is a 256-lead flip-chip ball grid array (FC-BGA) measuring 17 mm by 17 mm. The nominal ball pitch is 1 mm. See Figure 9.

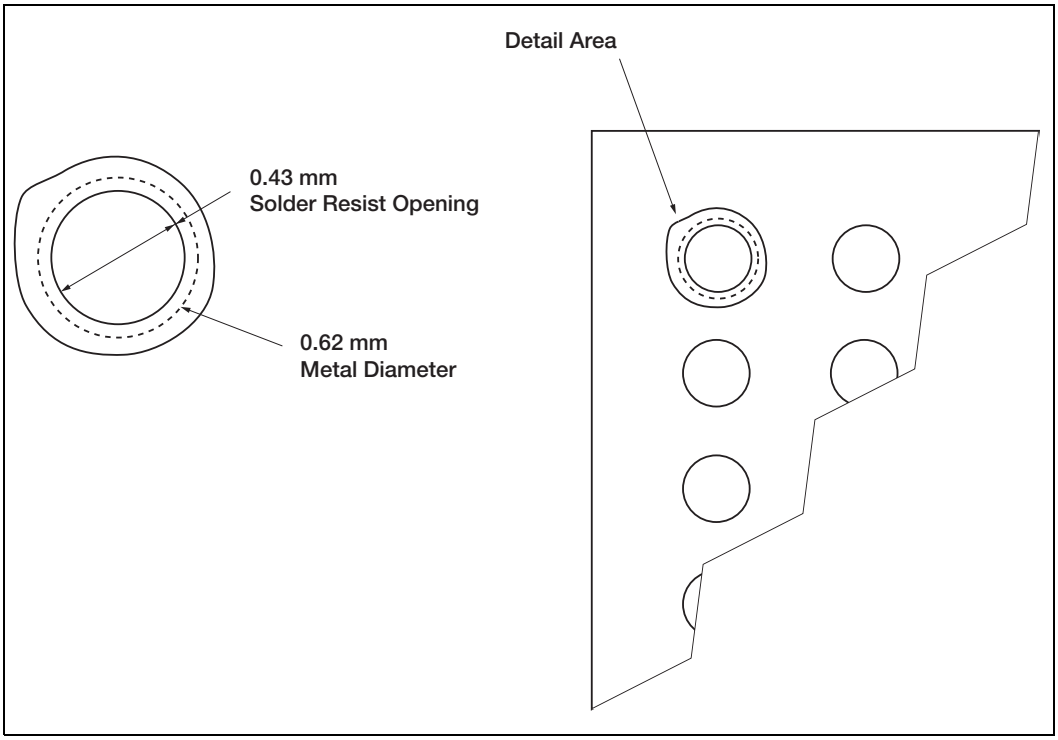

Figure 8. 82571EB/82572EI Controller FC-BGA Package Ball Pad Dimensions

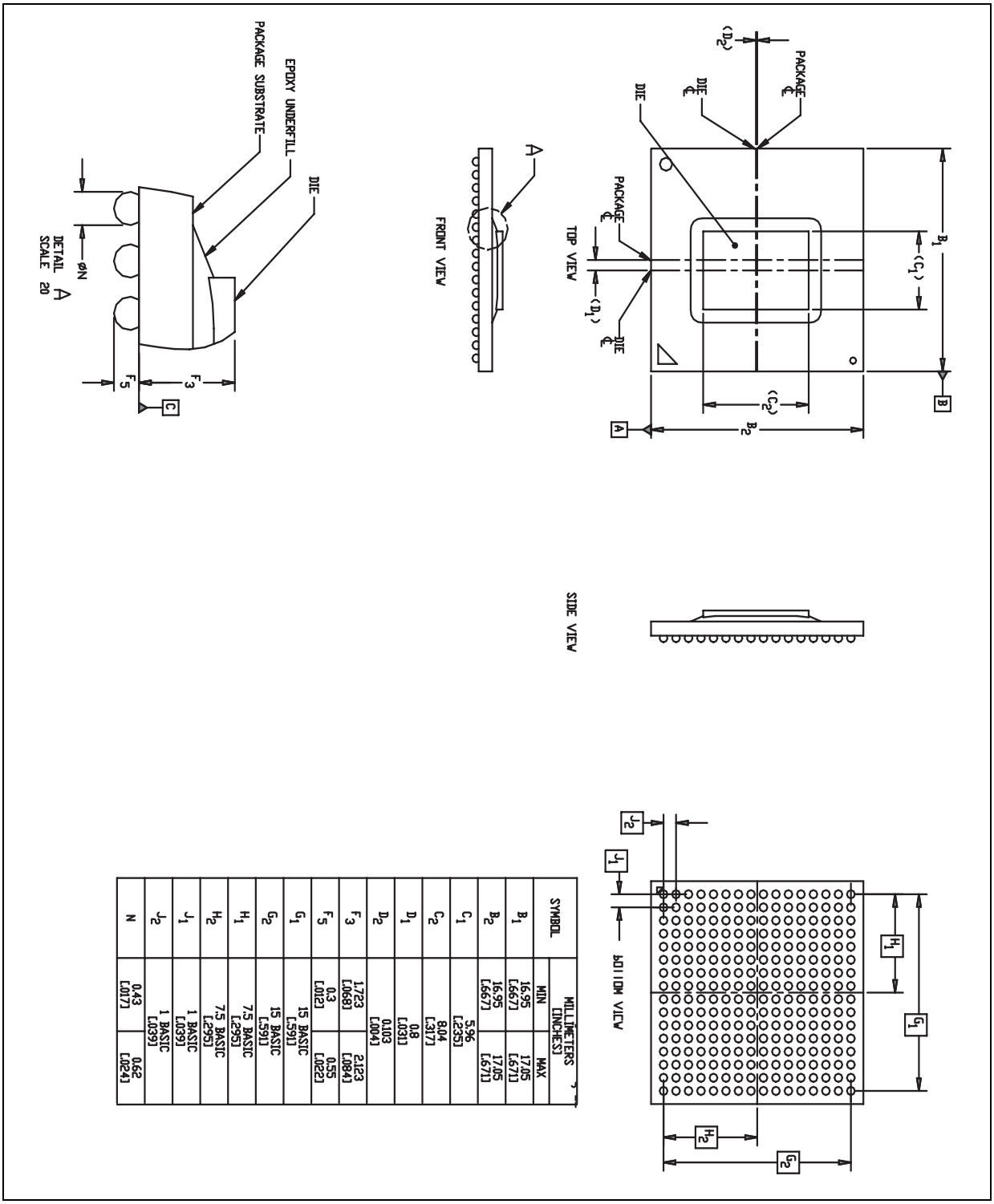

Figure 9. 82571EB/82572EI Mechanical Specifications

5.2 Thermal Specification

The 82571EB/82572EI device is specified for operation when the ambient temperature (T_A) is within the range of 0° C to 55° C. For more information about the thermal characteristics of the device, including operation outside of this range, please refer to the *82571EB/82572EB Thermal Application Note, AP-490*

5.3 Pinout Information

Signal names apply to both the 82571EB and the 82572EI unless there is a "/", which indicates that the the first name is for the 82571EB and the second name is for the 82572EI.

Table 25. PCI Express Signals

Signal	Pin	Signal	Pin	Signal	Pin
PERn0	R2	PERn3	B1	PETn2	D2
PERp0	T2	PERp3	C1	PETp2	E2
PERn1	M2	PETn0	P1	PETn3	A2
PERp1	N2	PETp0	R1	PETp3	B2
PERn2	E1	PETn1	L1	PE_RCOMPn	G2
PERp2	F1	PETp1	M1	PE_RCOMPp	H2
PE_CLKn	J2	PE_CLKp	K2	PE_RSTn	T6

Table 26. Power Management Signals

Signal	Pin	Signal	Pin
LAN0_DIS_N	B7	PE_WAKEn	P11
LAN1_DIS_N/ RSVD_B8	B8	AUX_PWR	C8
DEV_OFF_N	T3		

Table 27. SMB/Fast Management Link Bus Signals

Signal	Pin	Signal	Pin	Signal	Pin
SMBCLK0/ FLBMCK	T12	SMBCLK1	P13	SMBALRT_N/ PCI_PWR_GOOD	R11
SMBD0/FLBMD	R12	SMBD1	P12	FLBSD	P7
				FLBINTEX	R7

Table 28. EEPROM and Serial FLASH Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
EE_SK	B12	EE_CS_N	C13	FLSH_SI	T9
EE_DO	A12	FLSH_SCK	R10	FLSH_SO	R9
EE_DI	C12	FLSH_CE_N	P10		

Table 29. LED Signals

Signal	Pin	Signal	Pin	Signal	Pin
LED0_0	B11	LED0_1	C11	LED1_3/RSVD_P9	P9
LED0_2	B10	LED1_0/RSVD_P8	P8	LED1_1/RSVD_R8	R8
LED0_3	C10	LED1_2/RSVD_T8	T8		

Table 30. Other Signals

Signal	Pin	Signal	Pin
SDP0_0	B9	SDP1_0/RSVD_P6	P6
SDP0_1	A9	SDP1_1/RSVD_B6	B6
SDP0_2	C9	SDP1_2/RSVD_C6	C6
SDP0_3	A8	SDP1_3/RSVD_R6	R6

Table 31. PHY and SERDES Signals

Signal	Pin	Signal	Pin	Signal	Pin
MDI_MINUS0_0	B14	MDI_MINUS1_3/ RSVD_N15	N15	SRDSI_0_MINUS	F16
MDI_PLUS0_0	A14	MDI_PLUS1_3/ RSVD_N16	N16	SRDSI_0_PLUS	E16
MDI_MINUS0_1	B15	RBIAS0n	D14	SRDSO_1_MINUS/ RSVD_L15	L15
MDI_PLUS0_1	A15	RBIAS0p	E14	SRDSO_1_PLUS/ RSVD_K15	K15
MDI_MINUS0_2	C15	RBIAS1n/ RSVD_N14	N14	SRDSB_SIG_DET/ RSVD_C4	C4
MDI_PLUS0_2	C16	RBIAS1p/ RSVD_M14	M14	SRDSI_1_MINUS/ RSVD_L16	L16
MDI_MINUS0_3	D15	SRDSO_0_MINUS	F15	SRDSI_1_PLUS/ RSVD_M16	M16
MDI_PLUS1_2/ RSVD_P16	P16	SRDSO_0_PLUS	G15	SRDSA_SIG_DET	B4

Signal	Pin	Signal	Pin	Signal	Pin
MDI_PLUS0_3	D16	MDI_MINUS1_0/ RSVD_R14	R14	SRDS_RCOMPn	H14
MDI_PLUS1_1/ RSVD_T15	T15	MDI_PLUS1_0/ RSVD_T14	T14	SRDS_RCOMPp	H15
MDI_MINUS1_2/ RSVD_P15	P15	MDI_MINUS1_1/ RSVD_R15	R15		

Table 32. Test Interface Signals

Signal	Pin	Signal	Pin	Signal	Pin
JTCK	P4	IEEE_TEST0n	A13	THERM_Dp	D4
JTDI	R3	IEEE_TEST0p	B13	THERM_Dn	D5
JTDO	P5	IEEE_TEST1n/ RSVD_T13	T13		
JTMS	P3	IEEE_TEST1p/ RSVD_R13	R13		
TEST_EN	R5				

Table 33. Crystal Signals

Signal	Pin
XTAL1	J16
XTAL2	H16

Table 34. Power Signals

Signal	Pin	Signal	Pin	Signal	Pin
VCC33	A4	VCC18	M4	VCC11	M9
VCC33	A10	VCC18	M5	VCC11	M13
VCC33	D7	VCC18	K4	VCC11	E12
VCC33	D9	VCC11	E7	VCC11	F13
VCC33	N7	VCC11	E9	VCC11	G12
VCC33	N9	VCC11	E13	VCC11	K12
VCC33	T5	VCC11	F7	VCC11	L13
VCC33	T11	VCC11	F9	VCC11	M12
VCC18	E10	VCC11	G7	VCC11	F12
VCC18	F10	VCC11	G9	VCC11	L12
VCC18	G10	VCC11	H7	VCC11	J4
VCC18	H10	VCC11	H9	VCC11	J5
VCC18	J10	VCC11	J7	VCC11	N4
VCC18	K10	VCC11	J9	VCC11	N5
VCC18	L10	VCC11	K7		
VCC18	M10	VCC11	K9		
VCC18	H4	VCC11	L7		
VCC18	H5	VCC11	L9		
VCC18	K5	VCC11	M7		

Table 35. Ground Signals

Signal	Pin	Signal	Pin	Signal	Pin
VSSA	A1	VSSA	H13	VSS	A5
VSSA	A16	VSSA	J3	VSS	A11
VSSA	B16	VSSA	J11	VSS	D6
VSSA	C2	VSSA	J12	VSS	D8
VSSA	C14	VSSA	J13	VSS	D10
VSSA	D1	VSSA	K1	VSS	E5
VSSA	D3	VSSA	K3	VSS	E6
VSSA	D11	VSSA	K11	VSS	E8
VSSA	D12	VSSA	K13	VSS	F5
VSSA	D13	VSSA	K14	VSS	F6
VSSA	E3	VSSA	K16	VSS	F8
VSSA	E4	VSSA	L2	VSS	G6
VSSA	E11	VSSA	L3	VSS	G8
VSSA	E15	VSSA	L4	VSS	H6
VSSA	F2	VSSA	L5	VSS	H8
VSSA	F3	VSSA	L11	VSS	J6
VSSA	F4	VSSA	L14	VSS	J8
VSSA	F11	VSSA	M3	VSS	K6
VSSA	F14	VSSA	M11	VSS	K8
VSSA	G1	VSSA	M15	VSS	L6
VSSA	G3	VSSA	N1	VSS	L8
VSSA	G4	VSSA	N3	VSS	M6
VSSA	G5	VSSA	N11	VSS	M8
VSSA	G11	VSSA	N12	VSS	N6
VSSA	G13	VSSA	N13	VSS	N8
VSSA	G14	VSSA	P2	VSS	N10
VSSA	G16	VSSA	P14	VSS	T4
VSSA	H3	VSSA	R16	VSS	T10
VSSA	H11	VSSA	T1		
VSSA	H12	VSSA	T16		

Table 36. Reserved and No Connect Signals

Note: These pins are reserved by Intel and may have factory test functions. For normal operation, do not connect any circuitry to these pins (allow them to “float”). Some configurations may require pull-up or pull-down resistors on these pins. Please refer to the 82571EB/82572EI design guide for more information.

Signal	Pin
RSVD_A3	A3
RSVD_ A6	A6
DEVICE_DIS_N	A7
RSVD_B3	B3
RSVD_ B5	B5
RSVD_ C3	C3
RSVD_ C5	C5
RSVD_ C7	C7
RSVD_H1	H1
RSVD_J1	J1
RSVD_J14	J14
RSVD_J15	J15
LAN_PWR_GOOD	R4
NC_T7	T7

Table 37. Signal Names in Pin Order (Sheet 1 of 8)

Signal Name	Pin
VSSA	A1
PETn3	A2
RSVD_A3	A3
VCC33	A4
VSS	A5
RSVD_A6	A6
DEVICE_DIS_N	A7
SDP0_3	A8
SDP0_1	A9
VCC33	A10
VSS	A11
EE_DO	A12
IEEE_TEST0n	A13
MDI_PLUS0_0	A14
MDI_PLUS0_1	A15
VSSA	A16

Table 37. Signal Names in Pin Order (Sheet 2 of 8)

Signal Name	Pin
PERn3	B1
PETp3	B2
RSVD_B3	B3
SRDSA_SIG_DET	B4
RSVD_B5	B5
SDP1_1/RSVD_B6	B6
LAN0_DIS_N	B7
LAN1_DIS_N/RSVD_B8	B8
SDP0_0	B9
LED0_2	B10
LED0_0	B11
EE_SK	B12
IEEE_TEST0p	B13
MDI_MINUS0_0	B14
MDI_MINUS0_1	B15
VSSA	B16
PERp3	C1
VSSA	C2
RSVD_C3	C3
SRDSB_SIG_DET/RSVD_C4	C4
RSVD_C5	C5
SDP1_2/RSVD_C6	C6
RSVD_C7	C7
AUX_PWR	C8
SDP0_2	C9
LED0_3	C10
LED0_1	C11
EE_DI	C12
EE_CS_N	C13
VSSA	C14
MDI_MINUS0_2	C15
MDI_PLUS0_2	C16
VSSA	D1
PETn2	D2
VSSA	D3
THERM_Dp	D4
THERM_Dn	D5
VSS	D6

Table 37. Signal Names in Pin Order (Sheet 3 of 8)

Signal Name	Pin
VCC33	D7
VSS	D8
VCC33	D9
VSS	D10
VSSA	D11
VSSA	D12
VSSA	D13
RBIAS0n	D14
MDI_MINUS0_3	D15
MDI_PLUS0_3	D16
PERn2	E1
PETp2	E2
VSSA	E3
VSSA	E4
VSS	E5
VSS	E6
VCC11	E7
VSS	E8
VCC11	E9
VCC18	E10
VSSA	E11
VCC11	E12
VCC11	E13
RBIAS0p	E14
VSSA	E15
SRDSI_0_PLUS	E16
PERp2	F1
VSSA	F2
VSSA	F3
VSSA	F4
VSS	F5
VSS	F6
VCC11	F7
VSS	F8
VCC11	F9
VCC18	F10
VSSA	F11
VCC11	F12

Table 37. Signal Names in Pin Order (Sheet 4 of 8)

Signal Name	Pin
VCC11	F13
VSSA	F14
SRDSO_0_MINUS	F15
SRDSI_0_MINUS	F16
VSSA	G1
PE_RCOMPn	G2
VSSA	G3
VSSA	G4
VSSA	G5
VSS	G6
VCC11	G7
VSS	G8
VCC11	G9
VCC18	G10
VSSA	G11
VCC11	G12
VSSA	G13
VSSA	G14
SRDSO_0_PLUS	G15
VSSA	G16
RSVD_H1	H1
PE_RCOMPp	H2
VSSA	H3
VCC18	H4
VCC18	H5
VSS	H6
VCC11	H7
VSS	H8
VCC11	H9
VCC18	H10
VSSA	H11
VSSA	H12
VSSA	H13
SRDS_RCOMPn	H14
SRDS_RCOMPp	H15
XTAL2	H16
RSVD_J1	J1
PE_CLKn	J2

Table 37. Signal Names in Pin Order (Sheet 5 of 8)

Signal Name	Pin
VSSA	J3
VCC11	J4
VCC11	J5
VSS	J6
VCC11	J7
VSS	J8
VCC11	J9
VCC18	J10
VSSA	J11
VSSA	J12
VSSA	J13
RSVD_J14	J14
RSVD_J15	J15
XTAL1	J16
VSSA	K1
PE_CLKp	K2
VSSA	K3
VCC18	K4
VCC18	K5
VSS	K6
VCC11	K7
VSS	K8
VCC11	K9
VCC18	K10
VSSA	K11
VCC11	K12
VSSA	K13
VSSA	K14
SRDSO_1_PLUS/RSVD_K15	K15
VSSA	K16
PETn1	L1
VSSA	L2
VSSA	L3
VSSA	L4
VSSA	L5
VSS	L6
VCC11	L7
VSS	L8

Table 37. Signal Names in Pin Order (Sheet 6 of 8)

Signal Name	Pin
VCC11	L9
VCC18	L10
VSSA	L11
VCC11	L12
VCC11	L13
VSSA	L14
SRDSO_1_MINUS/RSVD_L15	L15
SRDSI_1_MINUS/RSVD_L16	L16
PETp1	M1
PERn1	M2
VSSA	M3
VCC18	M4
VCC18	M5
VSS	M6
VCC11	M7
VSS	M8
VCC11	M9
VCC18	M10
VSSA	M11
VCC11	M12
VCC11	M13
RBIAS1p/RSVD_M14	M14
VSSA	M15
SRDSI_1_PLUS/RSVD_M16	M16
VSSA	N1
PERp1	N2
VSSA	N3
VCC11	N4
VCC11	N5
VSS	N6
VCC33	N7
VSS	N8
VCC33	N9
VSS	N10
VSSA	N11
VSSA	N12
VSSA	N13
RBIAS1n/RSVD_N14	N14

Table 37. Signal Names in Pin Order (Sheet 7 of 8)

Signal Name	Pin
MDI_MINUS1_3/RSVD_N15	N15
MDI_PLUS1_3/RSVD_N16	N16
PETn0	P1
VSSA	P2
JTMS	P3
JTCK	P4
JTDO	P5
SDP1_0/RSVD_P6	P6
FLBSD	P7
LED1_0/RSVD_P8	P8
LED1_3/RSVD_P9	P9
FLSH_CE_N	P10
PE_WAKEn	P11
SMBD1	P12
SMBCLK1	P13
VSSA	P14
MDI_MINUS1_2/RSVD_P15	P15
MDI_PLUS1_2/RSVD_P16	P16
PETp0	R1
PERn0	R2
JTDI	R3
LAN_PWR_GOOD	R4
TEST_EN	R5
SDP1_3/RSVD_R6	R6
FLBINTEX	R7
LED1_1/RSVD_R8	R8
FLSH_SO	R9
FLSH_SCK	R10
SMBALRT_N/PCI_PWR_GOOD	R11
SMBD0/FLBMD	R12
IEEE_TEST1p/RSVD_R13	R13
MDI_MINUS1_0/RSVD_R14	R14
MDI_MINUS1_1/RSVD_R15	R15
VSSA	R16
VSSA	T1
PERp0	T2
DEV_OFF_N	T3
VSS	T4

Table 37. Signal Names in Pin Order (Sheet 8 of 8)

Signal Name	Pin
VCC33	T5
PE_RSTn	T6
NC_T7	T7
LED1_2/RSVD_T8	T8
FLSH_SI	T9
VSS	T10
VCC33	T11
SMBCLK0/FLBMCK	T12
IEEE_TEST1n/RSVD_T13	T13
MDI_PLUS1_0/RSVD_T14	T14
MDI_PLUS1_1/RSVD_T15	T15
VSSA	T16

5.4 Visual Pin Assignments

	A	B	C	D	E	F	G	H
16	VSSA	VSSA	MDI_ PLUS0_2	MDI_ PLUS0_3	SRDSI_0 _PLUS	SRDSI_0 _MINUS	VSSA	XTAL2
15	MDI_PLUS0_1	MDI_ MINUS0_1	MDI_ MINUS0_2	MDI_ MINUS0_3	VSSA	SRDSO_0 _MINUS	SRDSO_0 _PLUS	SRDS_RCOMPp
14	MDI_PLUS0_0	MDI_MINUS0_0	VSSA	RBIAS0n	RBIAS0p	VSSA	VSSA	SRDS_RCOMPn
13	IEEE_TEST0n	IEEE_TEST0p	EE_CS_N	VSSA	VCC11	VCC11	VSSA	VSSA
12	EE_DO	EE_SK	EE_DI	VSSA	VCC11	VCC11	VCC11	VSSA
11	VSS	LED0_0	LED0_1	VSSA	VSSA	VSSA	VSSA	VSSA
10	VCC33	LED0_2	LED0_3	VSS	VCC18	VCC18	VCC18	VCC18
9	SDP0_1	SDP0_0	SDP0_2	VCC33	VCC11	VCC11	VCC11	VCC11
8	SDP0_3	LAN1_DIS_N/ RSVD_B8	AUX_PWR	VSS	VSS	VSS	VSS	VSS
7	DEVICE_DIS_N	LAN0_DIS_N	RSVD_C7	VCC33	VCC11	VCC11	VCC11	VCC11
6	RSVD_A6	SDP1_1/ RSVD_B6	SDP1_2/ RSVD_C6	VSS	VSS	VSS	VSS	VSS
5	VSS	RSVD_B5	RSVD_C5	THERM_ Dn	VSS	VSS	VSSA	VCC18
4	VCC33	SRDSA_SIG_DET	SRDSB_SIG_DET/ RSVD_C4	THERM_ Dp	VSSA	VSSA	VSSA	VCC18
3	RSVD_A3	RSVD_B3	RSVD_C3	VSSA	VSSA	VSSA	VSSA	VSSA
2	PETn3	PETp3	VSSA	PETn2	PETp2	VSSA	PE_RCOMPn	PE_RCOMPp
1	VSSA	PERn3	PERp3	VSSA	PERn2	PERp2	VSSA	RSVD_H1

Figure 10. 82571EB/82572EI Visual Pin Assignment pt.1 (Top View)

J	K	L	M	N	P	R	T	
XTAL1	VSSA	SRDSI_1_MINUS/ RSVD_L16	SRDSI_1_PLUS/ RSVD_M16	MDI_PLUS1_3/ RSVD_N16	MDI_PLUS1_2/ RSVD_P16	VSSA	VSSA	**16**
RSVD_J15	SRDSO_1_ PLUS/RSVD_K15	SRDSO_1_ MINUS/RSVD_L15	VSSA	MDI_MINUS1_3/ RSVD_N15	MDI_MINUS1_2 /RSVD_P15	MDI_MINUS1_1/ RSVD_15	MDI_PLUS1_1 /RSVD_T15	**15**
RSVD_J14	VSSA	VSSA	RBIAS1p/ RSVD_M14	RBIAS1n/ RSVD_N14	VSSA	MDI_MINUS1_0/ RSVD_R14	MDI_PLUS1_0 /RSVD_T14	**14**
VSSA	VSSA	VCC11	VCC11	VSSA	SMBCLK1	IEEE_TEST1p/ RSVD_R13	IEEE_TEST1n/ RSVD_T13	**13**
VSSA	VCC11	VCC11	VCC11	VSSA	SMBD1	SMBD0/FLBMD	SMBCLK0/ FLBMCK	**12**
VSSA	VSSA	VSSA	VSSA	VSSA	PE_WAKEn	SMBALRT_N/ PCI_PWR_GOOD	VCC33	**11**
VCC18	VCC18	VCC18	VCC18	VSS	FLSH_CE_N	FLSH_SCK	VSS	**10**
VCC11	VCC11	VCC11	VCC11	VCC33	LED1_3/ RSVD_P9	FLSH_SO	FLSH_SI	**9**
VSS	VSS	VSS	VSS	VSS	LED1_0/ RSVD_P8	LED1_1/ RSVD_R8	LED1_2/ RSVD_T8	**8**
VCC11	VCC11	VCC11	VCC11	VCC33	FLBSD	FLBINTEX	NC_T7	**7**
VSS	VSS	VSS	VSS	VSS	SDP1_0/ RSVD_P6	SDP1_3/ RSVD_R6	PE_RSTn	**6**
VCC11	VCC18	VSSA	VCC18	VCC11	JTDO	TEST_EN	VCC33	**5**
VCC11	VCC18	VSSA	VCC18	VCC11	JTCK	RSVD	VSS	**4**
VSSA	VSSA	VSSA	VSSA	VSSA	JTMS	JTDI	DEV_OFF_N	**3**
PE_CLKn	PE_CLKp	VSSA	PERn1	PERp1	VSSA	PERn0	PERp0	**2**
RSVD_J1	VSSA	PETn1	PETp1	VSSA	PETn0	PETp0	VSSA	**1**

Figure 11. 82571EB/82572EI Visual Pin Assignment pt.2 (Top View)

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