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Intel® 82801CA I/O Controller Hub 3-S (ICH3-S)

Datasheet

March 2002

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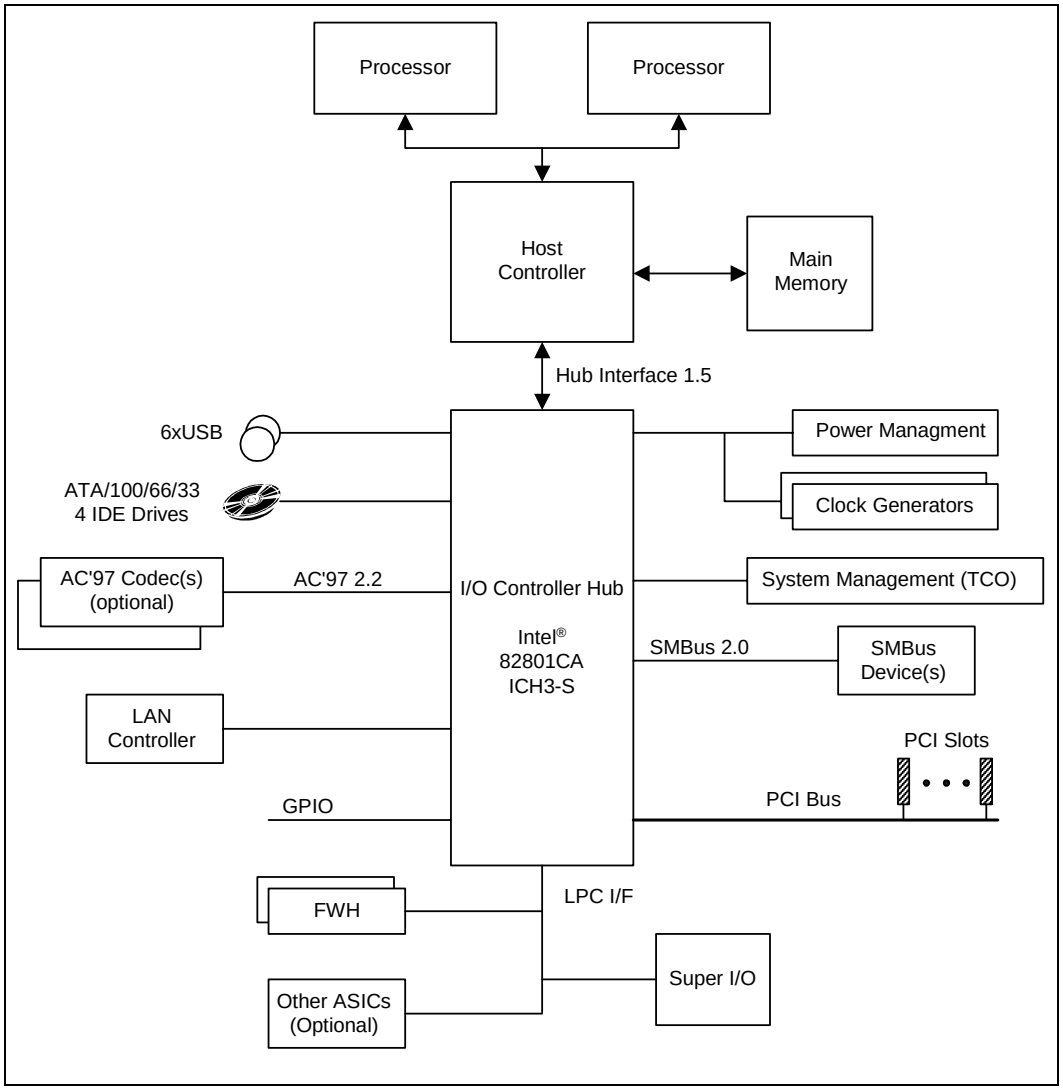
Intel® 82801CA ICH3-S Features

- PCI Bus Interface
  - — Supports PCI Rev 2.2 Specification at 33 MHz
  - — 133 MByte/sec maximum throughput
  - — Supports up to 6 master devices on PCI
  - — One PCI REQ/GNT pair can be given higher arbitration priority (intended for external IEEE 1394 host controller)
- Integrated LAN Controller
  - — WfM 2.0 Compliant
  - — Interface to discrete Platform LAN Connect component
  - — 10/100 Mbit/sec Ethernet support
- Integrated IDE Controller
  - — New: Supports "Native Mode" Register and Interrupt support
  - — Independent timing of up to 4 drives, with separate IDE connections for Primary and Secondary cables
  - — Ultra ATA/100/66/33, BMIDE and PIO modes
- USB
  - — New: Includes 3 UHCI Host Controllers, increasing the number of external ports to six
  - — Supports wake-up from sleeping states S1-S4
  - — Supports legacy Keyboard/Mouse software
- AC'97 Link for Audio and Telephony CODECs
  - — *Audio Codec '97*, Revision 2.2 compliant
  - — Independent bus master logic for 5 channels (PCM In/Out, Mic Input, Modem In/Out)
  - — Separate independent PCI functions for Audio and Modem
  - — Support for up to six channels of PCM audio output (full AC3 decode)
  - — Supports wake-up events
- Interrupt Controller
  - — Support up to 8 PCI interrupt pins
  - — Supports PCI 2.2 Message Signaled Interrupts
  - — Two cascaded 82C59 with 15 interrupts
  - — Integrated I/O APIC capability with 24 interrupts
  - — Supports Serial Interrupt Protocol
  - — Supports Processor System Bus interrupt delivery
- 1.8 V operation with 3.3 V I/O
  - — 5V tolerant buffers on IDE, PCI, USB Over-current and Legacy signals
- Timers Based on 82C54
  - — System timer, Refresh request, Speaker tone output
- External Glue Integration
  - — Integrated Pull-up, Pull-down and Series Termination resistors on IDE, processor interface, and USB
- Power Management Logic
  - — ACPI 1.0 compliant
  - — ACPI-defined power states (C1–C2, S3–S5)
  - — ACPI Power Management Timer
  - — PME# support
  - — SMI# generation
  - — All registers readable/restorable for proper resume from 0 V suspend states
  - — Support for APM-based legacy power management for non-ACPI implementations
- Firmware Hub (FWH) Interface supports BIOS Memory size up to 8 MB
- Low Pin count (LPC) Interface
  - — Allows connection of legacy ISA and X-Bus devices such as Super I/O
  - — Supports two Master/DMA devices.
- Enhanced DMA Controller
  - — Two cascaded 8237 DMA controllers
  - — PCI DMA: Supports PC/PCI—Includes two PC/PCI REQ#/GNT# pairs
  - — Supports LPC DMA
  - — Supports DMA Collection Buffer to provide Type-F DMA performance for all DMA channels
- Real-Time Clock
  - — 256-byte battery-backed CMOS RAM
- System TCO Reduction Circuits
  - — Timers to generate SMI# and Reset upon detection of system hang
  - — Timers to detect improper processor reset
  - — Integrated processor frequency strap logic
  - — New: Supports ability to disable external devices
- SMBus
  - — Host interface allows processor to communicate via SMBus
  - — Slave interface allows an external Microcontroller to access system resources
  - — Compatible with most 2-Wire components that are also I^2C* compatible
  - — New: Supports SMBus 2.0 Specification
- GPIO
  - — TTL, Open-Drain, Inversion
- New: Package 31x31 mm 421 BGA

The Intel® 82801CA ICH3-S may contain design defects or errors known as errata which may cause the products to deviate from published specifications. Current characterized errata are available on request.

Intel® ICH3-S System Configuration



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Revision History

Revision	Change Descriptions	Date
-001	Initial Release.	February 2002
-002	Added Appendix B, Register Bit Index	March 2002

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Introduction 1

1.1 About This Datasheet

This datasheet is intended for Original Equipment Manufacturers and BIOS vendors that create ICH3-Server based products. Throughout this datasheet, all references to ICH3 refer to the Intel® 82801CA ICH3-S part. This datasheet assumes a working knowledge of the vocabulary and principles of USB, IDE, AC '97, SMBus, PCI, ACPI, and LPC. Although some details of these features are described within this datasheet, refer to the individual industry specifications listed in Table 1-1 for the complete details.

Table 1-1. Industry Specifications

Specification	Location
LPC	http://developer.intel.com/design/chipsets/industry/lpc.htm
AC '97	http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec
WfM	http://developer.intel.com/ial/WfM/usesite.htm
SMBus	http://www.smbus.org/specs/
PCI	http://www.pcisig.com/
USB	http://www.usb.org
ACPI	http://www.teleport.com/~acpi/

Chapter 1. Introduction
Chapter 1 introduces the ICH3 and provides information on datasheet organization.

Chapter 2. Signal Description
Chapter 2 provides a detailed description of each ICH3 signal. Signals are arranged according to interface and details are provided as to the drive characteristics (Input/Output, Open Drain, etc.) of all signals.

Chapter 3. ICH3 Power Planes and Pin States
Chapter 3 provides a complete list of signals, their associated power well, their logic level in each suspend state, and their logic level before and after reset.

Chapter 4. ICH3 and System Clock Domains
Chapter 4 provides a list of each clock domain associated with the ICH3 in an ICH3 based system.

Chapter 5. Functional Description
Chapter 5 provides a detailed description of the functions in the ICH3. All PCI buses, devices and functions in this datasheet are abbreviated using the following nomenclature; Bus:Device:Function. This datasheet abbreviates buses as B0 and B1, devices as D8, D29, D30 and D31 and functions as F0, F1, F2, F3, F4, F5, and F6. For example, Device 31 Function 5 is abbreviated as D31:F5, Bus 1 Device 8 Function 0 is abbreviated as B1:D8:F0. Generally, the bus number will not be used, and can be considered to be Bus 0. Note that the ICH3's external PCI bus is typically Bus 1, but may be assigned a different number depending upon system configuration.

Chapter 6. Register, Memory and I/O Address Maps
Chapter 7 provides an overview of the registers, fixed I/O ranges, variable I/O ranges and memory ranges decoded by the ICH3.

Chapter 7. LAN Controller Registers
Chapter 7 provides a detailed description of all registers that reside in the ICH3's integrated LAN Controller. The integrated LAN Controller resides on the ICH3's external PCI bus (typically Bus 1) at Device 8, Function 0 (B1:D8:F0).

Chapter 8. Hub Interface to PCI Bridge Registers
Chapter 8 provides a detailed description of all registers that reside in the Hub Interface to PCI bridge. This bridge resides at Device 30, Function 0 (D30:F0).

Chapter 9. LPC Bridge Registers
Chapter 9 provides a detailed description of all registers that reside in the LPC bridge. This bridge resides at Device 31, Function 0 (D31:F0). This function contains registers for many different units within the ICH3 including DMA, Timers, Interrupts, CPU Interface, GPIO, Power Management, System Management and RTC.

Chapter 10. IDE Controller Registers
Chapter 10 provides a detailed description of all registers that reside in the IDE controller. This controller resides at Device 31, Function 1 (D31:F1).

Chapter 11. USB 1.1 Controller Registers
Chapter 11 provides a detailed description of all registers that reside in the three UHCI host controllers. These controllers reside at Device 29, Functions 0, 1 and 2 (D29:F0/F1/F2).

Chapter 12. SMBus Controller Registers
Chapter 12 provides a detailed description of all registers that reside in the SMBus controller. This controller resides at Device 31, Function 3 (D31:F3).

Chapter 13. AC '97 Audio Controller Registers
Chapter 13 provides a detailed description of all registers that reside in the audio controller. This controller resides at Device 31, Function 5 (D31:F5). Note that this section of the datasheet does not include the native audio mixer registers. Accesses to the mixer registers are forwarded over the AC-link to the codec where the registers reside.

Chapter 14. AC '97 Modem Controller Registers
Chapter 14 provides a detailed description of all registers that reside in the modem controller. This controller resides at Device 31, Function 6 (D31:F6). Note that this section of the datasheet does not include the modem mixer registers. Accesses to the mixer registers are forwarded over the AC-link to the codec where the registers reside.

Chapter 15. Pinout Definition
Chapter 15 provides a table of each signal and its ball assignment in the 421 BGA package.

Chapter 16. Electrical Characteristics
Chapter 16 provides all AC and DC characteristics including detailed timing diagrams.

Chapter 17. Package Information
Chapter 17 provides drawings of the physical dimensions and characteristics of the 421 BGA package.

Chapter 18. Testability
Chapter 18 provides details about the implementation of test modes provided in the ICH3.

Index
This datasheet ends with indexes of registers and register bits.

1.2 Overview

The ICH3 provides extensive I/O support. Functions and capabilities include:

- *PCI Local Bus Specification*, Revision 2.2-compliant with support for 33 MHz PCI operations.
- PCI slots (supports up to 6 Req/Gnt pairs)
- ACPI Power Management Logic Support
- Enhanced DMA Controller, Interrupt Controller, and Timer Functions
- Integrated IDE controller supports Ultra ATA100/66/33
- USB host interface with support for 6 USB ports; 3 UHCI host controllers
- Integrated LAN Controller
- *System Management Bus (SMBus) Specification*, Version 2.0 with additional support for I^2C devices
- *Audio Codec '97*, Revision 2.2 specification (a.k.a., *AC '97 Component Specification*, Rev. 2.2) Compliant Link for Audio and Telephony codecs (up to 6 channels)
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Alert On LAN* (AOL) and Alert On LAN 2* (AOL2)

The ICH3 incorporates a variety of PCI functions that are divided into three logical devices (29, 30, and 31) on PCI Bus 0 and one device on Bus 1. Device 30 is the Hub Interface-To-PCI bridge. Device 31 contains all the other PCI functions, except the USB Controllers and the LAN Controller, as shown in Table 1-2. The LAN controller is located on Bus 1.

Table 1-2. PCI Devices and Functions

Bus:Device:Function	Function Description
Bus 0:Device 30:Function 0	Hub Interface to PCI Bridge
Bus 0:Device 31:Function 0	PCI to LPC Bridge
Bus 0:Device 31:Function 1	IDE Controller
Bus 0:Device 31:Function 3	SMBus Controller
Bus 0:Device 31:Function 5	AC '97 Audio Controller
Bus 0:Device 31:Function 6	AC '97 Modem Controller
Bus 0:Device 29:Function 0	USB UHCI Controller #1
Bus 0:Device 29:Function 1	USB UHCI Controller #2
Bus 0:Device 29:Function 2	New: USB UHCI Controller #3
Bus n:Device 8:Function 0	LAN Controller

The following sub-sections provide an overview of the ICH3-S capabilities.

Hub Architecture

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC ’97 and Ultra ATA/100, coupled with the existing USB, I/O requirements could impact PCI bus performance. The chipset’s *hub interface architecture* ensures that the I/O subsystem; both PCI and the integrated I/O features (IDE, AC ‘97, USB, etc.), receive adequate bandwidth. By placing the I/O bridge on the hub interface (instead of PCI), the hub architecture ensures that both the I/O functions integrated into the ICH3 and the PCI peripherals obtain the bandwidth necessary for peak performance.

PCI Interface

The ICH3 PCI interface provides a 33 MHz, Rev. 2.2 compliant implementation. All PCI signals are 5 V tolerant, except PME#. The ICH3 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH3 requests.

IDE Interface (Bus Master Capability and Synchronous DMA Mode)

The fast IDE interface supports up to four IDE devices providing an interface for IDE hard disks and CD ROMs. Each IDE device can have independent timings. The IDE interface supports PIO IDE transfers up to 16 Mbytes/sec and Bus Master IDE transfers up 100 Mbytes/sec. It does not consume any ISA DMA resources. The IDE interface integrates 16x32-bit buffers for optimal transfers.

The ICH3’s IDE system contains two independent IDE signal channels. They can be electrically isolated independently. They can be configured to the standard primary and secondary channels (four devices). There are integrated series resistors on the data and control lines (see Section 5.15, “IDE Controller (D31:F1)” on page 5-161 for details).

Low Pin Count (LPC) Interface

The ICH3 implements an LPC Interface as described in the LPC 1.0 specification. The Low Pin Count (LPC) Bridge function of the ICH3 resides in PCI Device 31:Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, Interrupt Controllers, Timers, Power Management, System Management, GPIO, and RTC.

Note that in the current chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost Super I/O designs.

Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The DMA controller incorporates the logic of two 82C37 DMA controllers, with seven independently programmable channels. Channels 0–3 are hardwired to 8-bit, count-by-byte transfers, and channels 5–7 are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers.

The ICH3 supports two types of DMA (LPC and PC/PCI). DMA via LPC is similar to ISA DMA. LPC DMA and PC/PCI DMA use the ICH3's DMA controller. The PC/PCI protocol allows PCI-based peripherals to initiate DMA cycles by encoding requests and grants via two PC/PCI REQ#/GNT# pairs.

LPC DMA is handled through the use of the LDRQ# lines from peripherals and special encodings on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface. Channels 0–3 are 8 bit channels. Channels 5–7 are 16 bit channels. Channel 4 is reserved as a generic bus master request.

The timer/counter block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the system timer function, and speaker tone. The 14.31818 MHz oscillator input provides the clock source for these three counters.

The ICH3 provides an ISA-Compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the ICH3 supports a serial interrupt scheme.

All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the platform.

Advanced Programmable Interrupt Controller (APIC)

In addition to the standard ISA compatible Programmable Interrupt Controller (PIC) described in the previous section, the ICH3 incorporates the Advanced Programmable Interrupt Controller (APIC).

Universal Serial Bus (USB) Controller

The USB controller provides support for the Universal Host Controller Interface (UHCI). This includes support that allows legacy software to use a USB-based keyboard and mouse. The ICH3 is USB Revision 1.1 compliant. The ICH3 contains three UHCI USB Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of six USB ports. See Section 5.16, "USB 1.1 Controllers (D29:F0, F1 and F2)" on page 5-172 for details.

LAN Controller

The ICH3's integrated LAN Controller includes a 32-bit PCI controller that provides enhanced scatter-gather bus mastering capabilities and enables the LAN Controller to perform high speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 KB each help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN Controller to transmit data with minimum interframe spacing (IFS).

The LAN Controller can operate in either full duplex or half duplex mode. In full duplex mode the LAN Controller adheres with the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism. See Section 5.2, "LAN Controller (B1:D8:F0)" on page 5-71 for details.

RTC

The ICH3 contains a Motorola* MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a separate 3 V lithium battery that provides up to seven years of protection.

The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC also supports a date alarm that allows for scheduling a wake up event up to 30 days in advance, rather than just 24 hours in advance.

GPIO

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on ICH3 configuration.

Enhanced Power Management

The ICH3's power management functions include enhanced clock control, local and global monitoring support for 14 individual devices, and various low-power (suspend) states (e.g., Suspend-to-DRAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states. The ICH3 contains full support for the Advanced Configuration and Power Interface (ACPI) Specification.

System Management Bus (SMBus 2.0)

The ICH3 contains an SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices. Special I^2C commands are implemented.

The ICH3's SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). Also, the ICH3 supports slave functionality, including the Host Notify protocol. Hence, the host controller supports 8 command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification*, Version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

Manageability

The ICH3 integrates several functions designed to manage the system and lower the total cost of ownership (TC0) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

- **TCO Timer.** The ICH3's integrated programmable TC0 Timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.
- **Processor Present Indicator.** The ICH3 looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH3 will reboot the system at the safe-mode frequency multiplier.
- **ECC Error Reporting.** When detecting an ECC error, the host controller has the ability to send one of several messages to the ICH3. The host controller can instruct the ICH3 to generate either an SMI#, NMI, SERR#, or TCO interrupt.
- **Function Disable.** The ICH3 provides the ability to disable the following functions: AC '97 Modem, AC '97 Audio, IDE, LAN USB, or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disable functions.
- **Intruder Detect.** The ICH3 provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The ICH3 can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.
- **SMBus 2.0.** The ICH3 integrates an SMBus controller that provides an interface to manage peripherals (e.g., serial presence detection (SPD) and thermal sensors) with host notify capabilities.
- **Alert On LAN*.** The ICH3 supports Alert On LAN* and Alert On LAN* 2. In response to a TCO event (intruder detect, thermal event, processor not booting) the ICH3 sends a message over the SMBus. A LAN controller can decode this SMBus message and send a message over the network to alert the network manager.

AC ’97 2.2 Controller

The *Audio Codec ’97*, Revision 2.2 specification defines a digital interface that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC) or both an AC and an MC. The AC ’97 specification defines the interface between the system logic and the audio or modem codec, known as the *AC ’97 Digital Link*.

The ICH3’s AC ’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC ’97 digital link. The use of the ICH3-integrated AC ’97 digital link reduces cost and eases migration from ISA.

By using an audio codec, the AC ’97 digital link allows for cost-effective, high-quality, integrated audio on Intel’s chipset-based platform. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC ’97. The ICH3-integrated digital link allows several external codecs to be connected to the ICH3. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec. The digital link is expanded to support two audio codecs or a combination of an audio and modem codec.

The modem implementations for different countries must be taken into consideration, because telephone systems may vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser.

The digital link in the ICH3 is compliant with the *Audio Codec ’97*, Revision 2.2 specification, so it supports two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality, two-speaker audio solution. Wake on Ring from Suspend also is supported with the appropriate modem codec.

The ICH3 expands the audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Subwoofer, for a complete surround-sound effect. ICH3 has expanded support for two audio codecs on the AC ’97 digital link.

Signal Description 2

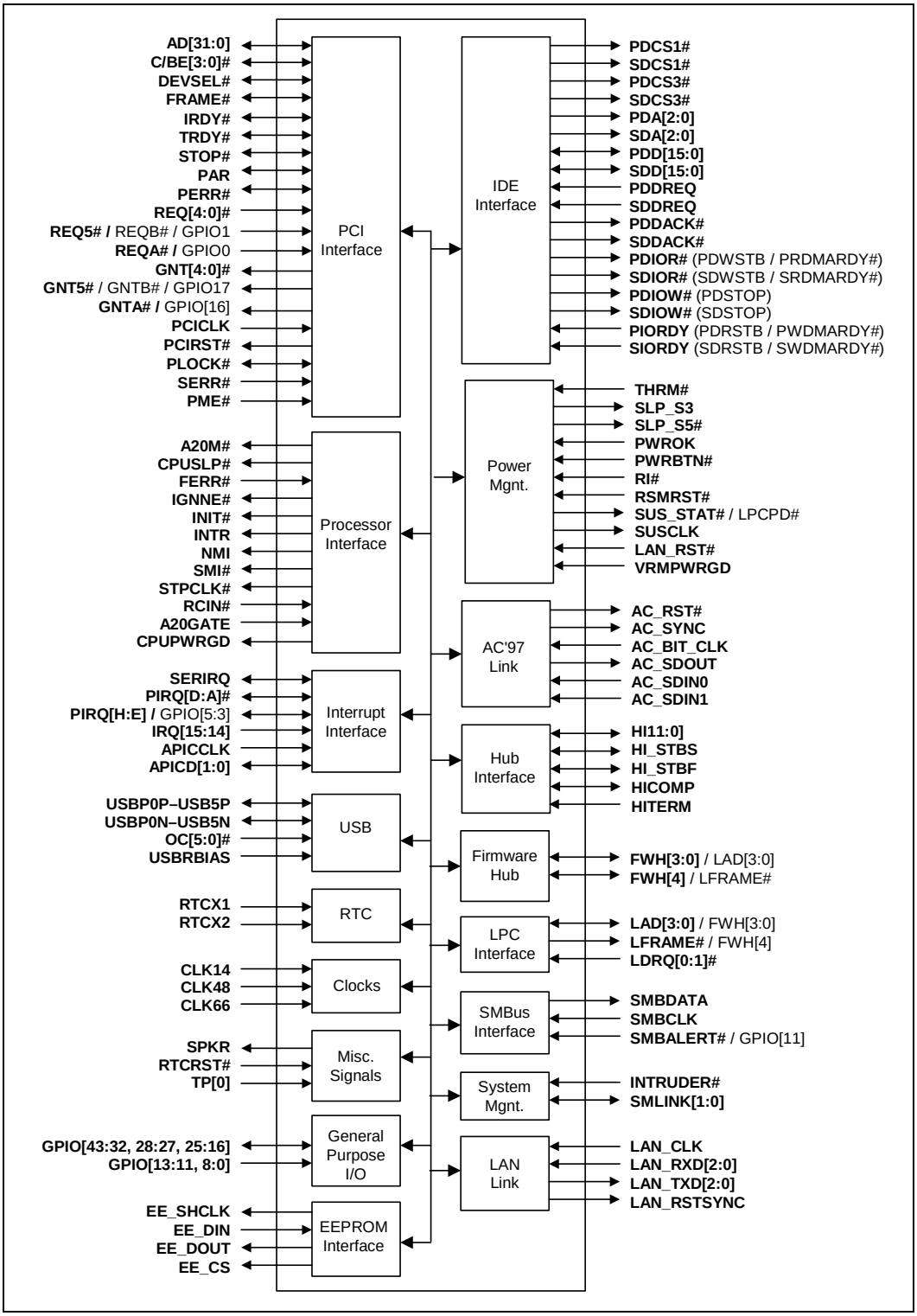
This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface (see Figure 2-1).

The "#" symbol at the end of the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input Pin
O	Output Pin
OD	Open Drain Output Pin.
I/O	Bi-directional Input / Output Pin.

Figure 2-1. Intel® 82801CA ICH3-S Simplified Block Diagram



2.1 Hub Interface to Host Controller

Table 2-1. Hub Interface Signals

Name	Type	Description
HI[11:0]	I/O	**Hub Interface Signals**
HI_STBF	I/O	**Hub Interface Strobe Complement:** First strobe signal used to transmit and receive data through the hub interface.
HI_STBS	I/O	**Hub Interface Strobe:** Second strobe signal used to transmit and receive data through the hub interface.
HICOMP	I/O	**Hub Interface Compensation:** Used for hub interface buffer compensation.
HITERM	I	**Hub Interface Termination:** Analog input used to control the voltage swing and impedance strength of hub interface pins. The expected voltage is **700 mv**. **NOTE:** Refer to the platform design guide for resistor values and routing guidelines.

2.2 Link to LAN Connect

Table 2-2. LAN Connect Interface Signals

Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** Driven by the LAN Connect component. Frequency range is 5 to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

2.3 EEPROM Interface

Table 2-3. EEPROM Interface Signals

Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock**: Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In**: Transfers data from the EEPROM to the ICH3. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out**: Transfers data from the ICH3 to the EEPROM.
EE_CS	O	**EEPROM Chip Select**: Chip select signal to the EEPROM.

2.4 Firmware Hub Interface

Table 2-4. Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0] / LAD[3:0]	I/O	**Firmware Hub Signals.** Muxed with LPC address signals.
FWH[4] / LFRAME#	I/O	**Firmware Hub Signals.** Muxed with LPC LFRAME# signal.

2.5 PCI Interface

Table 2-5. PCI Interface Signals

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH3 will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0 0 0 0 Interrupt Acknowledge 0 0 0 1 Special Cycle 0 0 1 0 I/O Read 0 0 1 1 I/O Write 0 1 1 0 Memory Read 0 1 1 1 Memory Write 1 0 1 0 Configuration Read 1 0 1 1 Configuration Write 1 1 0 0 Memory Read Multiple 1 1 1 0 Memory Read Line 1 1 1 1 Memory Write and Invalidate All command encodings not shown are reserved. The ICH3 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH3 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH3 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH3 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH3-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH3 until driven by a Target device.
FRAME#	I/O	**Cycle Frame:** The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH3 when the ICH3 is the target, and FRAME# is an output from the ICH3 when the ICH3 is the Initiator. FRAME# remains tri-stated by the ICH3 until driven by an Initiator.

Table 2-5. PCI Interface Signals (Continued)

Name	Type	Description
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH3's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH3 has valid data present on AD[31:0]. During a read, it indicates the ICH3 is prepared to latch data. IRDY# is an input to the ICH3 when the ICH3 is the Target and an output from the ICH3 when the ICH3 is an Initiator. IRDY# remains tri-stated by the ICH3 until driven by an Initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the ICH3's ability as a Target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH3, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH3, as a Target is prepared to latch data. TRDY# is an input to the ICH3 when the ICH3 is the Initiator and an output from the ICH3 when the ICH3 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH3 until driven by a target.
STOP#	I/O	**Stop:** STOP# indicates that the ICH3, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH3, as an Initiator, to stop the current transaction. STOP# is an output when the ICH3 is a Target and an input when the ICH3 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH3.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH3 counts the number of “1”s within the 36 bits plus PAR and the sum is always even. The ICH3 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH3 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH3 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH3 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH3 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH3 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. ICH3 checks parity when it is the Target of a PCI write transaction. If a parity error is detected, the ICH3 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH3 drives PERR# when it detects a parity error. The ICH3 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[4:0]# **REQ[5]# /** REQ[B]# / GPIO[1]	I	**PCI Requests:** Supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. **NOTE:** REQ[0]# is programmable to have improved arbitration latency for supporting PCI-based 1394 controllers.
GNT[4:0]# **GNT[5]# /** GNT[B]# / GPIO[17]#	O	**PCI Grants:** Supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed for PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pull-up.
PCICLK	I	**PCI Clock:** 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. **NOTE:**
PCIRST#	O	**PCI Reset:** ICH3 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH3 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) Register. The ICH3 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH3 drives PCIRST# active a minimum of 1 ms when initiated through the RC Register.

Table 2-5. PCI Interface Signals (Continued)

Name	Type	Description
PLOCK#	I/O	**PCI Lock:** Indicates an exclusive bus operation and may require multiple transactions to complete. ICH3 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH3 has the ability to generate an NMI, SMI#, or interrupt.
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH3 may drive PME# active due to an internal wake event. The ICH3 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
REQ[A]# / GPIO[0] **REQ[B]# /** REQ[5]# / GPIO[1]	I	**PC/PCI DMA Request [B:A]:** This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy Intel® 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. REQ[B]# can instead be used as the sixth PCI bus request.
GNT[A]# / GPIO[16] **GNT[B]#** / GNT[5]# / GPIO[17]	O	**PC/PCI DMA Acknowledges [B: A]:** This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA Master cycles over the PCI bus. This is used by devices such as PCI based Super/IO or audio codecs which need to perform legacy Intel 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the sixth PCI bus master grant output. These signal have internal pull-up resistors.

2.6 IDE Interface

Table 2-6. IDE Interface Signals

Name	Type	Description
PDCS1#, **SDCS1#**	O	**Primary and Secondary IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, **SDCS3#**	O	**Primary and Secondary IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDA[2:0], **SDA[2:0]**	O	**Primary and Secondary IDE Device Address:** These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.
PDD[15:0], **SDD[15:0]**	I/O	**Primary and Secondary IDE Device Data:** These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, **SDDREQ**	I	**Primary and Secondary IDE Device DMA Request:** These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, **SDDACK#**	O	**Primary and Secondary IDE Device DMA Acknowledge:** These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each is asserted by the ICH3 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR# / (PDWSTB / PRDMARDY#) **SDIOR# /** (SDWSTB / SRDMARDY#)	O	**Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the PDD or SDD lines. Data is latched by the ICH3 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). **Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk):** This is the data write strobe for writes to disk. When writing to disk, ICH3 drives valid data on rising and falling edges of PDWSTB or SDWSTB. **Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk):** This is the DMA ready for reads from disk. When reading from disk, ICH3 deasserts PRDMARDY# or SRDMARDY# to pause burst data transfers.
PDIOW# / (PDSTOP) **SDIOW# /** (SDSTOP)	O	**Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). **Primary and Secondary Disk Stop (Ultra DMA):** ICH3 asserts this signal to terminate a burst.
PIORDY / (PDRSTB / PWDMARDY#) **SIORDY /** (SDRSTB / SWDMARDY#)	I	**Primary and Secondary I/O Channel Ready (PIO):** This signal will keep the strobe active (PDIOR# or SDIOR# on reads, PDIOW# or SDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. **Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk)**: When reading from disk, ICH3 latches data on rising and falling edges of this signal from the disk. **Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk)**: When writing to disk, this is de-asserted by the disk to pause burst data transfers.

2.7 LPC Interface

Table 2-7. LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** Internal pull-ups are provided.
LFRAME# / FWH[4]	O	**LPC Frame:** Indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	I	**LPC Serial DMA/Master Request Inputs:** Used to request DMA or bus master access. Typically connected to external Super I/O device. An internal pull-up resistor is provided on these signals.

2.8 Interrupt Interface

Table 2-8. Interrupt Signals

Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IRQ[15:14]	I	**Interrupt Request 15–14:** These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the Primary controller and IRQ15 is used by the drives connected to the Secondary controller.
APICCLK	I	**APIC Clock:** This clock operates up to 33.33 MHz.
APICD[1:0]	I/OD	**APIC Data:** These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs the data is valid on the rising edge of APICCLK. As outputs, new data is driven from the rising edge of the APICCLK.

2.9 USB Interface

Table 2-9. USB Interface Signals

Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port 1:0 Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports are routed to USB 1.1 Controller #1. **NOTE:** No external resistors are required on these signals. The ICH3 integrates 15 kΩ pull-downs and provides an effective output driver impedance of 45 Ω which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port 3:2 Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 2 and 3. These ports are routed to USB 1.1 Controller #2. **NOTE:** No external resistors are required on these signals. The ICH3 integrates 15 kΩ pull-downs and provides an effective output driver impedance of 45 Ω which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP5N	I/O	**Universal Serial Bus Port 5:4 Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports are routed to USB 1.1 Controller #3. **NOTE:** No external resistors are required on these signals. The ICH3 integrates 15 kΩ pull-downs and provides an effective output driver impedance of 45 Ω that requires no external series resistor.
OC[5:0]#	I	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.
USBRBIAS	I	**USB Resistor Bias:** Analog connection for an external 18.2 Ω resistor (± 1%) to ground, used to set transmit current and internal load resistors.

2.10 Power Management Interface

Table 2-10. Power Management Interface Signals

Name	Type	Description
THRM#	I	**Thermal Alarm:** Active low signal generated by external hardware to start the Hardware clock throttling mode. Can also generate an SMI# or an SCI.
SLP_S3#	O	**S3 Sleep Control:** Power plane control. Shuts off power to all non-critical systems when transistioning to S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S5#	O	**S5 Sleep Control:** Power plane control. The signal is used to shut power off to all non-critical systems when in the S4 (Suspend To Disk) or S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH3 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH3 asserts PCIRST#. **NOTE:** PWROK must deassert for a minimum of 3 RTC clock periods in order for the ICH3 to fully reset the power and properly generate the PCIRST# output
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override will occur even if the system is in the S1–S4 states. This signal has an internal pull-up resistor.

Table 2-10. Power Management Interface Signals (Continued)

Name	Type	Description
RI#	I	**Ring Indicate:** From the modem interface. Can be enabled as a wake event, and this is preserved across power failures.
RSMRST#	I	**Resume Well Reset:** Used for resetting the resume power plane logic.
LAN_RST#	I	**LAN Reset:** This signal must be asserted at least 10 ms after the resume well power (VccSus3_3 and VccSus1_8) is valid. When deasserted, this signal is an indication that the resume well power is stable.
SUS_STAT#	O	**Suspend Status:** This signal is asserted by the ICH3 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes.
SUSCLK	O	**Suspend Clock:** Output of the RTC generator circuit to use by other chips for refresh clock.
VRMPWRGD	I	**VRM Power Good:** This should be connected to be the processor's VRM Power Good.

2.11 Processor Interface

Table 2-11. Processor Interface Signals

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active. **Speed Strap:** During the reset sequence, ICH3 drives A20M# high if the corresponding bit is set in the FREQ_STRP Register.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH3 can optionally assert the CPUSLP# signal when going to the S1 state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH3 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH3 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events (this functionality is independent of the General Control Register bit setting).
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH3 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **Speed Strap:** During the reset sequence, ICH3 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP Register.

Table 2-11. Processor Interface Signals (Continued)

Name	Type	Description
INIT#	O	**Initialization:** INIT# is asserted by the ICH3 for 16 PCI clocks to reset the processor. ICH3 can be configured to support CPU BIST. In that case, INIT# will be active when PCIRST# is active.
INTR	O	**Processor Interrupt:** INTR is asserted by the ICH3 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. **Speed Strap:** During the reset sequence, ICH3 drives INTR high if the corresponding bit is set in the FREQ_STRP Register.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH3 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. **Speed Strap:** During the reset sequence, ICH3 drives NMI high if the corresponding bit is set in the FREQ_STRP Register.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH3 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH3 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH3's other sources of INIT#. When the ICH3 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. Note that the ICH3 will ignore RCIN# assertion during transitions to the S1, S3, S4 and S5 states.
A20GATE	I	**A20 Gate:** From the keyboard controller. Acts as an alternative method to force the A20M# signal active. Saves the external OR gate needed with various other PCIsets.
CPUPWRGD	OD	**CPU Power Good:** Should be connected to the processor's PWRGOOD input. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH3's PWROK and VRMPWRGD signals.

2.12 SMBus Interface

Table 2-12. SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up is required.
SMBALERT#/ GPIO[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

2.13 System Management Interface

Table 2-13. System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** Can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK[0] corresponds to an SMBus Clock signal, and SMLINK[1] corresponds to an SMBus Data signal.

2.14 Real Time Clock Interface

Table 2-14. Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** Connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** Connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

2.15 Other Clocks

Table 2-15. Other Clocks

Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. Runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states .
CLK48	I	**48 MHz Clock:** Used to run the USB controller. Runs at 48 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK66	I	**66 MHz Clock:** Used to run the hub interface. Runs at 66 MHz. This clock is permitted to stop during S3 (or lower) states .

2.16 Miscellaneous Signals

Table 2-16. Miscellaneous Signals

Name	Type	Description
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally “ANDed” with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap. See Section 2.20.1for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCON3 Register). **NOTES:** 1. Clearing CMOS in an ICH3-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Unless entering the XOR Chain Test Mode, the RTCRST# input must always be high when all other RTC power planes are on
TP[0]	I	**Test Point:** This signal must have an external pull-up to VccSus3_3.

2.17 AC ’97 Link

Table 2-17. AC ’97 Link Signals

Name	Type	Description
AC_RST#	O	**AC ’97 Reset:** Master H/W reset to external Codec(s)
AC_SYNC	O	**AC ’97 Sync:** 48 kHz fixed rate sample sync to the Codec(s)
AC_BIT_CLK	I	**AC ’97 Bit Clock:** 12.288 MHz serial data clock generated by the external Codec(s). This signal has an integrated pull-down resistor.
AC_SDOUT	O	**AC ’97 Serial Data Out:** Serial TDM data output to the Codec(s) **NOTE:** AC_SDOUT is sampled at the rising edge of PWROK as a functional strap. See Section 2.20.1 for more details.
AC_SDIN[1:0]	I	**AC ’97 Serial Data In 0:** Serial TDM data inputs from the Codecs.

2.18 General Purpose I/O

Table 2-18. General Purpose I/O Signals

Name	Type	Description
GPIO[47:44]	I/O	Not implemented.
GPIO[43:38]	I/O	Can be input or output. Main power well.
GPIO[37:32]	I/O	Can be input or output. Main power well.
GPIO[31:29]	O	Not implemented.
GPIO[28:27]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[26]	I/O	Not implemented.
GPIO[25]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[24]	I/O	Can be input or output. Resume power well.
GPIO[23]	O	Fixed as output only. Main power well.
GPIO[22]	OD	Fixed as output only. Main power well.
GPIO[21]	O	Fixed as output only. Main power well. .
GPIO[20]	O	Fixed as output only. Main power well.
GPIO[19]	O	Fixed as output only. Main power well.
GPIO[18]	O	Fixed as output only. Main power well.
GPIO[17:16]	O	Fixed as Output only. Main Power Well. Can be used instead as PC/PCI GNT[B:A]#. GPIO[17] can also alternatively be used for PCI GNT[5]#. Integrated pull-up resistor.
GPIO[15:14]	I	Not implemented.
GPIO[13:12]	I	Fixed as Input only. Resume Power Well. Unmuxed.
GPIO[11]	I	Fixed as Input only. Resume Power Well. Can be used instead as SMBALERT#.
GPIO[10:9]	I	Not implemented.
GPIO[8]	I	Fixed as Input only. Resume Power Well. Unmuxed.
GPIO[7]	I	Fixed as Input only. Main power well. Unmuxed.
GPIO[6]	I	Fixed as Input only. Main power well.
GPIO[5:2]	I	Fixed as Input only. Main power well. Can be used instead as PIRQ[H:E]#.
GPIO[1:0]	I	Fixed as Input only. Main Power Well. Can be used instead as PC/PCI REQ[B:A]#. GPIO[1] can also alternatively be used for PCI REQ[5]#.

NOTE: Only GPIO[7:0] are 5 V tolerant.

2.19 Power and Ground

Table 2-19. Power and Ground Signals

Name	Description
Vcc3_3	3.3 V supply for Core well I/O buffers (15 pins). This power may be shut off in S3, S5 or G3 states.
Vcc1_8	1.8 V supply for Core well logic (12 pins). This power may be shut off in S3, S5 or G3 states.
V5REF[2:1]	Reference for 5V tolerance on Core well inputs. This power may be shut off in S3, S5 or G3 states.
HIREF	0.9 V reference for the hub interface. This power is shut off in S3, S5 or G3 states.
VccSus3_3	3.3 V supply for Resume well I/O buffers (8 pins). This power is not expected to be shut off unless the system is unplugged.
VccSus1_8	1.8 V supply for Resume well logic (13 pins). This power is not expected to be shut off unless the system is unplugged.
V5REF_Sus[2:1]	Reference for 5 V tolerance on Resume well inputs. This power is not expected to be shut off unless the system is unplugged. **NOTE:** See platform design guide for V5REF_Sus connectivity.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH3-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap.
VBIAS	RTC well bias voltage. The DC reference voltage applied to this pin sets a current that is mirrored throughout the oscillator and buffer circuitry. See Section 2.20.4.
V_CPU_IO	Powered by the same supply as the processor I/O voltage (3 pins). This supply is used to drive the processor I/F outputs.
Vss	Grounds (104 pins).

2.20 Pin Straps

2.20.1 Functional Straps

The following signals are used for static configuration. They are sampled at the rising edge of PWROK to select configurations, and then revert later to their normal usage. To invoke the associated mode, the signal should be driven at least 4 PCI clocks prior to the time it is sampled.

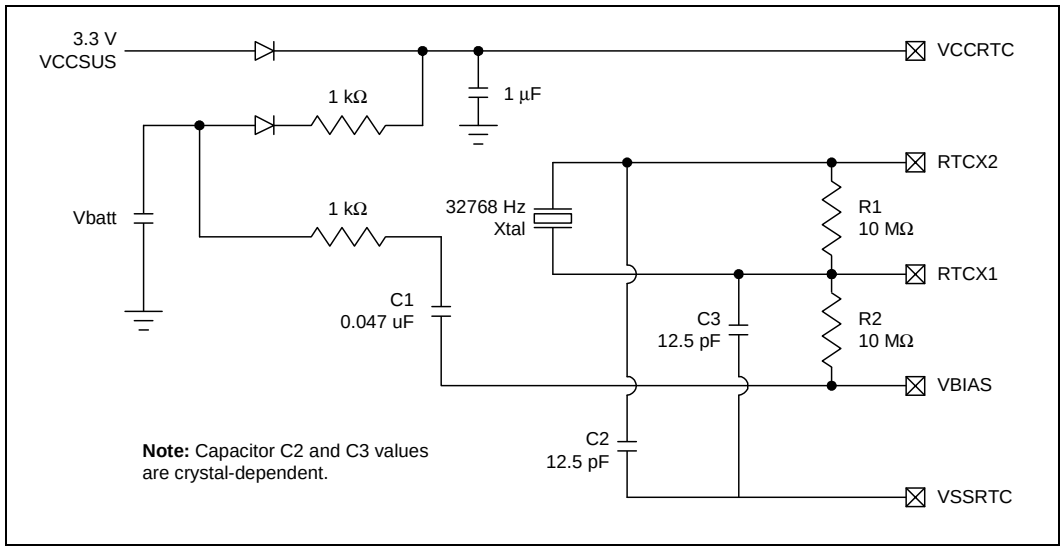
Table 2-20. Functional Strap Definitions

Signal	Usage	When Sampled	Comment
AC_SDOUT	Safe Mode	Rising Edge of PWROK	The signal has a weak internal pull-down. If the signal is sampled high, the ICH3 will set the processor speed strap pins for safe mode. Refer to processor specification for speed strapping definition. The status of this strap is readable via the SAFE_MODE bit (bit 2, D31: F0, Offset D4h).
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but *do not populate the resistor*.
GNT[A]#	Top-Swap Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “Top-Swap” mode (ICH3 will invert A16 for all cycles targeting FWH BIOS space). The status of this strap is readable via the Top-Swap bit (bit 13, D31: F0, Offset D4h). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT[A]# being pulled down.
DPSLPVR	Hub Interface Termination Scheme (Normal vs. Enhanced)	Rising Edge of PWROK	Low (default)–Hub Interface 1.0 series or Hub Interface 1.5 parallel termination High (external pull-up to Vcc1_8)–Not supported in ICH3.
HICOMP	Hub Interface Scheme (HI 1.5)	Rising Edge of PWROK	External pull-up to Vcc1_8. **NOTE:** See the platform design guide for resistor values and routing guidelines for each hub interface mode.
SPKR	No Reboot	Rising Edge of PWROK	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the “No Reboot” mode (ICH3 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h).

2.20.2 External RTC Circuitry

To reduce RTC well power consumption, the ICH3 implements an internal oscillator circuit that is sensitive to step voltage changes in VccRTC and VBIAS. Figure 2-2 shows the circuitry required to condition these voltages to ensure correct operation of the ICH3 RTC.

Figure 2-2. Required External RTC Circuit



2.20.3 V5REF / Vcc3_3 Sequencing Requirements

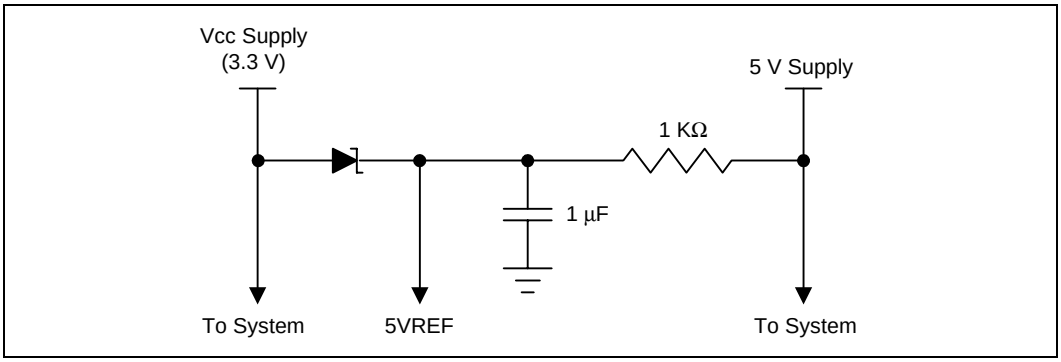
V5REF is the reference voltages for 5 V tolerance on inputs to the ICH3. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must be powered down after Vcc3_3 or before Vcc3_3 within 0.7 V. The rule must be followed to ensure the safety of the ICH3.

Caution: If this rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail.

Figure 2-3 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to the standby rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a reulst, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

Figure 2-3. Example V5REF Sequencing Circuit



2.20.4 Test Signals

2.20.4.1 Test Mode Selection

When PWROK is active (high) for at least 76 PCI clocks, driving RTCRST# active (low) for a number of PCI clocks (33 MHz) will activate a particular test mode a specified in Table 2-21.

Note: RTCRST# may be driven low any time after PCIRST is inactive. Refer to Section 18.1, "Test Mode Description" on page 18-487 for a detailed description of the ICH3-S test modes.

Table 2-21. Test Mode Selection

Number of PCI Clocks RTCRST# driven low after PWROK active	Test Mode
<4	No Test Mode Selected
4	XOR Chain 1
5	XOR Chain 2
6	XOR Chain 3
7	XOR Chain 4
8	All "Z" (Tri-state Mode)
9–42	Reserved. DO NOT ATTEMPT
>42	No Test Mode Selected

Power Planes and Pin States 3

This chapter provides the 82801CA ICH3-S power plane and pin states.

3.1 Power Planes

Table 3-1. Intel® ICH3 Power Planes

Plane	Description
Main I/O (3.3 V)	**Vcc3_3:** Powered by the main power supply or battery. When the system is in the S3, S4, S5, or G3 state, this plane is assumed to be shut off.
Main Logic (1.8 V)	**Vcc1_8:** Powered by the main power supply or battery. When the system is in the S3, S4, S5, or G3 state, this plane is assumed to be shut off.
Resume I/O (3.3 V Standby)	**VccSUS3_3:** Powered by the main power supply or battery in S0–S1 states. Powered by the trickle power supply or main battery When the system is in the S3, S4, S5, state. Assumed to be shut off only when in the G3 state (system is unplugged).
Resume Logic (1.8 V Standby)	**VccSUS1_8:** Powered by the main power supply or battery in S0–S1 states. Powered by the trickle power supply or main battery when the system is in the S3, S4, S5, state. Assumed to be shut off only when in the G3 state (system is unplugged).
CPU I/F (1.3 ~ 2.5V)	**V_CPU_IO:** Powered by the main power supply or battery via processor voltage regulator. When the system is in the S3, S4, S5, or G3 state, this plane is assumed to be shut off.
RTC	**VccRTC:** When other power is available (from the main supply or main battery[1]), external diode coupling will provide power to reduce the drain on the RTC battery. Assumed to operate from 3.3 V down to 2.0 V.

3.2 Integrated Pull-Ups and Pull-Downs

Table 3-2. Integrated Pull-Up and Pull-Down Resistors

Signal	Resistor Type	Nominal Value	Notes
EE_DIN	pull-up	24 kΩ	1
EE_DOUT	pull-up	24 kΩ	1
GNT[B:A]# / GNT[5]# / GPIO[17:16]	pull-up	24 kΩ	1
LAD[3:0]# / FWH[3:0]#	pull-up	24 kΩ	1
LDRQ[1:0]	pull-up	24 kΩ	1
PME#	pull-up	24 kΩ	1
PWRBTN#	pull-up	24 kΩ	1
SPKR	pull-down	24 kΩ	1, 5
AC_BIT_CLK	pull-down	20 kΩ	2, 6
AC_SDIN[1:0]	pull-down	20 kΩ	2
AC_SDOUT	pull-down	20 kΩ	2, 6
AC_SYNC	pull-down	20 kΩ	2, 5
LAN_RXD[2:0]	pull-up	9 kΩ	3
PDD[7] / SDD[7]	pull-down	5.9 kΩ	4
PDDREQ / SDDREQ	pull-down	5.9 kΩ	4
DPRSLPVR	pull-down	20 kΩ	2
LAN_CLK	pull-down	1 MΩ	
USB[5:0][P:N]	pull-down	15 kΩ	

NOTES:
1. Simulation data shows that these resistor values can range from 18 kΩ to 42 kΩ.
2. Simulation data shows that these resistor values can range from 13 kΩ to 38 kΩ.
3. Simulation data shows that these resistor values can range from 6 kΩ to 14 kΩ.
4. Simulation data shows that these resistor values can range from 4.3 kΩ to 20 kΩ.
5. The pull-up or pull-down on this signal is only enabled at boot/reset for strapping function.
6. This pull-down is enabled when either the ACLINK Shut Off bit in the AC '97 Global Control Register is set or when both function 5 and function 6 of Dev 31 are hidden (disabled).

3.3 IDE Integrated Series Termination Resistors

Table 3-3 shows the ICH3 IDE signals that have integrated series termination resistors.

Table 3-3. IDE Series Termination Resistors

Signal	Integrated Series Termination Resistor Value
PDD[15:0], SDD[15:0, PDIOW#, SDIOW#, PDIOR#, PDIOW#, PDREQ, SDREQ, PDDACK#, SDDACK#, PIORDY, SIORDY, PDA[2:0], SDA[2:0], PDCS1#, SDCS1#, PDCS3#, SDCS3#, IRQ14, IRQ15	approximately 33 Ω (See Note)

NOTE: Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.

3.4 Output and I/O Signals Planes and States

Table 3-4 shows the power plane associated with the output and I/O signals, as well as the state at various times. Within the tables, the following terms are used:

"High-Z"	Tri-state. ICH3 not driving the signal high or low.
"High"	ICH3 is driving the signal to a logic 1
"Low"	ICH3 is driving the signal to a logic 0
"Defined"	Driven to a level that is defined by the function (will be high or low)
"Undefined"	ICH3 is driving the signal, but the value is indeterminate.
"Running"	Clock is toggling or signal is transitioning because function not stopping
"Off"	The power plane is off, so ICH3 is not driving

Note that the signal levels are the same in S4 and S5.

Table 3-4. Power Plane and States for Output and I/O Signal

Signal Name	Power Plane	During PCIRST#[4] / RSMRST#[5]	Immediately after PCIRST#[4] / RSMRST#[5]	S1	S3	S4/S5
PCI Bus						
AD[31:0]	Main I/O	High-Z	Undefined	Defined	Off	Off
C/BE#[3:0]	Main I/O	High-Z	Undefined	Defined	Off	Off
DEVSEL#	Main I/O	High-Z	High-Z	High-Z	Off	Off
FRAME#	Main I/O	High-Z	High-Z	High-Z	Off	Off
GNT[0:4]#	Main I/O	High	High	High	Off	Off
GNT[A], GNT[5]#/ GNT[B]#	Main I/O	High-Z with internal pull-up	High	High	Off	Off
IRDY#, TRDY#	Main I/O	High-Z	High-Z	High-Z	Off	Off
PAR	Main I/O	High-Z	Undefined	Defined	Off	Off
PCIRST#	Resume I/O	Low	High	High	Low	Low
PERR#	Main I/O	High-Z	High-Z	High-Z	Off	Off
PLOCK#	Main I/O	High-Z	High-Z	High-Z	Off	Off
STOP#	Main I/O	High-Z	High-Z	High-Z	Off	Off
LPC Interface						
LAD[3:0]	Main I/O	High	High	High	Off	Off
LFRAME#	Main I/O	High	High	High	Off	Off

Table 3-4. Power Plane and States for Output and I/O Signal (Continued)

Signal Name	Power Plane	During PCIRST#[4] / RSMRST#[5]	Immediately after PCIRST#[4] / RSMRST#[5]	S1	S3	S4/S5
LAN Connect and EEPROM Interface						
EE_CS	Resume I/O	Low	Running	Defined	Defined	Defined
EE_DOUT	Resume I/O	High	High	Defined	Defined	Defined
EE_SHCLK	Resume I/O	Low	Running	Defined	Defined	Defined
LAN_RSTSYNC	Resume I/O	High	Defined	Defined	Defined	Defined
LAN_TXD[2:0]	Resume I/O	Low	Defined	Defined	Defined	Defined
IDE Interface						
PDA[2:0], SDA[2:0]	Main I/O	Undefined	Undefined	Undefined	Off	Off
PDCS1#, PDCS3#	Main I/O	High	High	High	Off	Off
PDD[15:8], SDD[15:8], PDD[6:0], SDD[6:0]	Main I/O	High-Z	High-Z	High-Z	Off	Off
PDD[7], SDD[7]	Main I/O	Low	Low	Low	Off	Off
PDDACK#, SDDACK#	Main I/O	High	High	High	Off	Off
PDIOR#, PDIOW#	Main I/O	High	High	High	Off	Off
SDCS1#, SDCS3#	Main I/O	High	High	High	Off	Off
SDIOR#, SDIOW#	Main I/O	High	High	High	Off	Off
Interrupts						
PIRQ[A:H]#	Main I/O	High-Z	High-Z	High-Z	Off	Off
SERIRQ	Main I/O	High-Z	High-Z	High-Z	Off	Off
APICD[1:0]	Main I/O	High-Z	High-Z	High-Z	Off	Off
USB Interface						
USBP[5:0][P,N]	Resume I/O	Low	Low	Low	Low	Low
Power Management						
SLP_S3#	Resume I/O	Low	High	High	Low	Low
SLP_S5#	Resume I/O	Low	High	High	High	Low
SUS_STAT#	Resume I/O	Low	High after PWROK rises	High	Low	Low
SUSCLK	Resume I/O	Low	Running			

Table 3-4. Power Plane and States for Output and I/O Signal (Continued)

Signal Name	Power Plane	During PCIRST#[4] / RSMRST#[5]	Immediately after PCIRST#[4] / RSMRST#[5]	S1	S3	S4/S5
CPU Interface						
A20M#	CPU I/O	See Note 1	High	High	Off	Off
CPUPWRGD	Main I/O	See Note 3	High-Z	High-Z	Off	Off
CPUSLP#	CPU I/O	High	High	Defined	Off	Off
IGNNE#	CPU I/O	See Note 1	High	High	Off	Off
INIT#	CPU I/O	High	High	High	Off	Off
INTR	CPU I/O	See Note 1	Low	Low	Off	Off
NMI	CPU I/O	See Note 1	Low	Low	Off	Off
SMI#	CPU I/O	High	High	High	Off	Off
STPCLK#	CPU I/O	High	High	Low	Off	Off
SMBus Interface						
SMBCLK, SMBDATA	Resume I/O	High-Z	High-Z	Defined	Defined	Defined
System Management Interface						
SMLINK[1:0]	Resume I/O	High-Z	High-Z	Defined	Defined	Defined
Miscellaneous Signals						
SPKR	Main I/O	Low with internal pull-down	Low	Defined	Off	Off
AC'97 Interface						
AC_RST#	Resume I/O	Low	Low	Cold Reset Bit (High)	Low	Low
AC_SDOUT	Main I/O	Low	Running	Low	Off	Off
AC_SYNC	Main I/O	Low	Running	Low	Off	Off
Unmuxed GPIO Signals						
GPIO[18]	Main I/O	High	See Note 2	Defined	Off	Off
GPIO[19:20]	Main I/O	High	High	Defined	Off	Off
GPIO[21]	Main I/O	High	High	Defined	Off	Off
GPIO[22]	Main I/O	High-Z	High-Z	Defined	Off	Off
GPIO[23]	Main I/O	Low	Low	Defined	Off	Off
GPIO[24]	Resume I/O	Low	Low	Defined	Defined	Defined
GPIO[25]	Resume I/O	High	High	Defined	Defined	Defined
GPIO[27:28]	Resume I/O	High	High	Defined	Defined	Defined
GPIO[43:32]	Main I/O	High	High	Defined	Off	Off

NOTES:
1. ICH3 sets these signals at reset for CPU frequency strap.
2. GPIO[18] will toggle at a frequency of approximately 1Hz when the ICH3 comes out of reset
3. CPUPWRGD is an open-drain output that represents a logical AND of the ICH3's VRMPWRGD and PWROK signals, and thus will be driven low by ICH3 when either VRMPWRGD or PWROK are inactive. During boot, or during a hard reset with power cycling, CPUPWRGD will be expected to transition from low to High-Z.
4. The states of main I/O signals are taken at the times During PCIRST# and Immediately after PCIRST#.
5. The states of resume I/O signals are taken at the times During RSMRST# and Immediately after RSMRST#

3.5 Power Planes for Input Signals

Table 3-5 shows the power plane associated with each input signal, as well as what device drives the signal at various times. Valid states include:

- High
- Low
- Static: Will be high or low, but will not change
- Driven: Will be high or low, and is allowed to change
- Running: For input clocks

Table 3-5. Power Plane for Input Signals

Signal Name	Power Well	Driver During Reset	S1	S3	S5
A20GATE	Main I/O	External Microcontroller	Static	Low	Low
AC_BIT_CLK	Main I/O	AC'97 Codec	Low	Low	Low
AC_SDIN[1:0]	Resume I/O	AC'97 Codec	Low	Low	Low
APICCLK	Main I/O	Clock Generator	Running	Low	Low
CLK14	Main I/O	Clock Generator	Running	Low	Low
CLK48	Main I/O	Clock Generator	Running	Low	Low
CLK66	Main Logic	Clock Generator	Running	Low	Low
EE_DIN	Resume I/O	EEPROM component	Driven	Driven	Driven
FERR#	Main I/O	CPU	Static	Low	Low
INTRUDER#	RTC	External Switch	Driven	Driven	Driven
IRQ[15:14]	Main I/O	IDE	Static	Low	Low
LAN_CLK	Resume I/O	LAN Connect component	Driven	Driven	Driven
LAN_RXD[2:0]	Resume I/O	LAN Connect component	Driven	Driven	Driven
LDRQ[0]#	Main I/O	LPC Devices	High	Low	Low
LDRQ[1]#	Main I/O	LPC Devices	High	Low	Low
OC[5:0]#	Resume I/O	External Pull-Ups	Driven	Driven	Driven
PCICLK	Main I/O	Clock Generator	Running	Low	Low
PDDREQ	Main I/O	IDE Device	Static	Low	Low
PIORDY	Main I/O	IDE Device	Static	Low	Low
PME#	Resume I/O	Internal Pull-Up	Driven	Driven	Driven
PWRBTN#	Resume I/O	Internal Pull-Up	Driven	Driven	Driven
PWROK	RTC	System Power Supply	Driven	Low	Low
RCIN#	Main I/O	External Microcontroller	High	Low	Low
REQ[0:5]#	Main I/O	PCI Master	Driven	Low	Low
REQ[B:A]#	Main I/O	PC/PCI Devices	Driven	Low	Low
RI#	Resume I/O	Serial Port Buffer	Driven	Driven	Driven
LAN_RST#	Resume I/O	External RC circuit	High	High	High
RSMRST#	RTC	External RC circuit	High	High	High
RTCRST#	RTC	External RC circuit	High	High	High

Table 3-5. Power Plane for Input Signals (Continued)

Signal Name	Power Well	Driver During Reset	S1	S3	S5
SDDREQ	Main I/O	IDE Drive	Static	Low	Low
SERR#	Main I/O	PCI Bus Peripherals	High	Low	Low
SIORDY	Main I/O	IDE Drive	Static	Low	Low
SMBALERT#	Resume I/O	External pull-up	Driven	Driven	Driven
THRM#	Main I/O	Thermal Sensor	Driven	Low	Low
USBRBIAS	Resume I/O	External Pull-down	Used	Used	Used
VRMPWRGD	Main I/O	CPU Voltage Regulator	High	Low	Low

NOTES:
1. LAN Connect and EEPROM signals will either be “Driven” or “Low” in S3–S5 states depending upon whether or not the LAN power planes are active.

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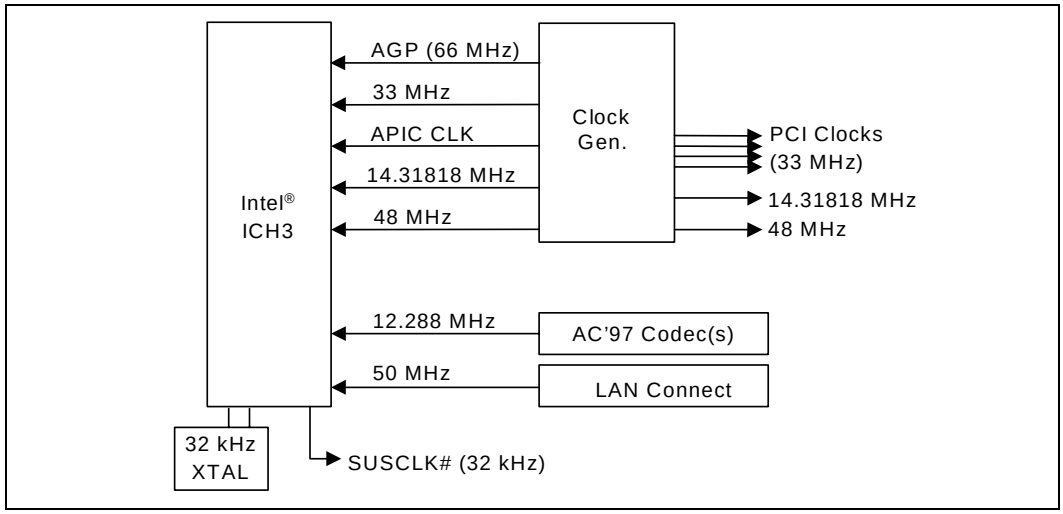
Intel® ICH3 and System Clock Domains4

Table 4-1 describes the system clock domains. Figure 4-1 shows the assumed connection of the various system components, including the clock generator. For complete details of the system clocking solution refer to the system's clock generator component specification.

Table 4-1. Intel® ICH3 and System Clock Domains

Clock Domain	Frequency	Source	Usage
ICH3 CLK66	66 MHz	Main Clock Generator	Hub I/F, processor I/F, AGP. Shut off during S3 or below .
ICH3 PCICLK	33 MHz	Main Clock Generator	Free-running PCI Clock to ICH3. This clock remains on during S0 and S1 state, and is expected to be shut off during S3 or below in server configurations or .
System PCI	33 MHz	Main Clock Generator	PCI Bus, LPC I/F. These only go to external PCI and LPC devices.
ICH3 CLK48	48 MHz	Main Clock Generator	Super I/O, USB Controllers. Expected to be shut off during S3 or below .
ICH3 CLK14	14.31818 MHz	Main Clock Generator	Expected to be shut off during S4 or below.
ICH3 AC_BIT_CLK	12.288 MHz	AC '97 Codec	AC '97 Link. Generated by AC '97 Codec. Can be shut by codec in D3. Expected to be shut off during S3 or below.
ICH3 APICCLK	33.33 MHz	Main Clock Generator	Used for ICH3-processor interrupt messages. Operates up to 33.33 MHz. Expected to be shut off during S3 or below.
LAN_CLK	5 to 50 MHz	LAN Connect Component	Generated by the LAN Connect component. Expected to be shut off during S3 or below.

Figure 4-1. Conceptual System Clock Diagram



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Functional Description 5

5.1 Hub Interface to PCI Bridge (D30:F0)

The hub interface to PCI Bridge resides in PCI Device 30, Function 0 on bus #0. This portion of the ICH3 implements the buffering and control logic between PCI and the hub interface. The arbitration for the PCI bus is handled by this PCI device. The PCI decoder in this device must decode the ranges for the hub interface. All register contents will be lost when core well power is removed.

5.1.1 PCI Bus Interface

The ICH3 PCI interface provides a 33 MHz, *PCI Local Bus Specification*, Rev. 2.2 compliant implementation. All PCI signals are 5 V tolerant. The ICH3 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH3 requests.

Note that most transactions targeted to the ICH3 will first appear on the external PCI bus before being claimed back by the ICH3. The exceptions are I/O cycles involving USB, IDE, and AC ’97. These transactions will complete over the hub interface without appearing on the external PCI bus. Configuration cycles targeting USB, IDE or AC ’97 will appear on the PCI bus. If the ICH3 is programmed for positive decode, the ICH3 will claim the cycles appearing on the external PCI bus in medium decode time. If the ICH3 is programmed for subtractive decode, the ICH3 will claim these cycles in subtractive time. If the ICH3 is programmed for subtractive decode, these cycles can be claimed by another positive decode agent out on PCI. This architecture enables the ability to boot off of a PCI card that positively decodes the boot cycles. In order to boot off a PCI card it is necessary to keep the ICH3 in subtractive decode mode. When booting off a PCI card, the BOOT_STS bit (bit 2, TCO2 Status Register) will be set.

Note: The ICH3’s AC ’97, IDE and USB Controllers can not perform peer to peer traffic.

Note: Poor performing PCI devices that cause long latencies (numerous retries) to processor-to-PCI Locked cycles may starve isochronous transfers between USB or AC ’97 devices and memory. This will result in overrun or underrun, causing reduced quality of the isochronous data, such as audio.

Note: PCI configuration write cycles, initiated by the processor, with the following characteristics will be converted to a Special Cycle with the Shutdown message type.

- Device Number (AD[15:11]) = 11111
- Function Number (AD[10:8]) = 111’
- Register Number (AD[7:2]) = 000000’
- Data = 00h
- Bus number matches secondary bus number

Note: If the processor issues a locked cycle to a resource that is too slow (e.g., PCI), the ICH3 will not allow upstream requests to be performed until the cycle completion. This may be critical for isochronous buses which assume certain timing for their data flow, such as AC ’97 or USB. Devices on these buses may suffer from underrun if the asynchronous traffic is too heavy. Underrun means that the same data is sent over the bus while ICH3 is not able to issue a request for the next data. Snoop cycles are not permitted while the Processor System Bus is locked.

Note: Locked cycles are assumed to be rare. Locks by PCI targets are assumed to exist for a short duration (a few microseconds at most). If a system has a very large number of locked cycles and some that are very long, then the system will definitely experience underruns and overruns. The units most likely to have problems are the AC '97 controller and the USB controllers. Other units could get underruns/overruns, but are much less likely. The IDE controller (due to its stalling capability on the cable) should not get any underruns or overruns.

5.1.2 PCI-to-PCI Bridge Model

From a software perspective, the ICH3 contains a PCI-to-PCI bridge. This bridge connects the hub interface to the PCI bus. By using the PCI-to-PCI bridge software model, the ICH3 can have its decode ranges programmed by existing plug-and-play software such that PCI ranges do not conflict with AGP and graphics aperture ranges in the Host controller.

5.1.3 IDSEL to Device Number Mapping

When addressing devices on the external PCI bus (with the PCI slots) the ICH3 will assert one address signal as an IDSEL. When accessing device 0, the ICH3 will assert AD16. When accessing Device 1, the ICH3 will assert AD17. This mapping continues all the way up to device 15 where the ICH3 asserts AD31. Note that the ICH3’s internal functions (AC ’97, IDE, USB, and PCI Bridge) are enumerated like they are on a separate PCI bus (the hub interface) from the external PCI bus. The integrated LAN Controller is Device 8 on the ICH3’s PCI bus, and hence it uses AD24 for IDSEL

5.1.4 SERR# Functionality

There are several internal and external sources that can cause SERR#. The ICH3 can be programmed to cause an NMI based on detecting that an SERR# condition has occurred. The NMI can also be routed to instead cause an SMI#. Note that the ICH3 does not drive the external PCI bus SERR# signal active onto the PCI bus. The external SERR# signal is an input into the ICH3 driven only by external PCI devices. The conceptual logic diagrams in Figure 5-1 and Figure 5-2 illustrate all sources of SERR#, along with their respective enable and status bits. Figure 5-3 shows how the ICH3 error reporting logic is configured for NMI# generation.

Figure 5-1. Primary Device Status Register Error Reporting Logic

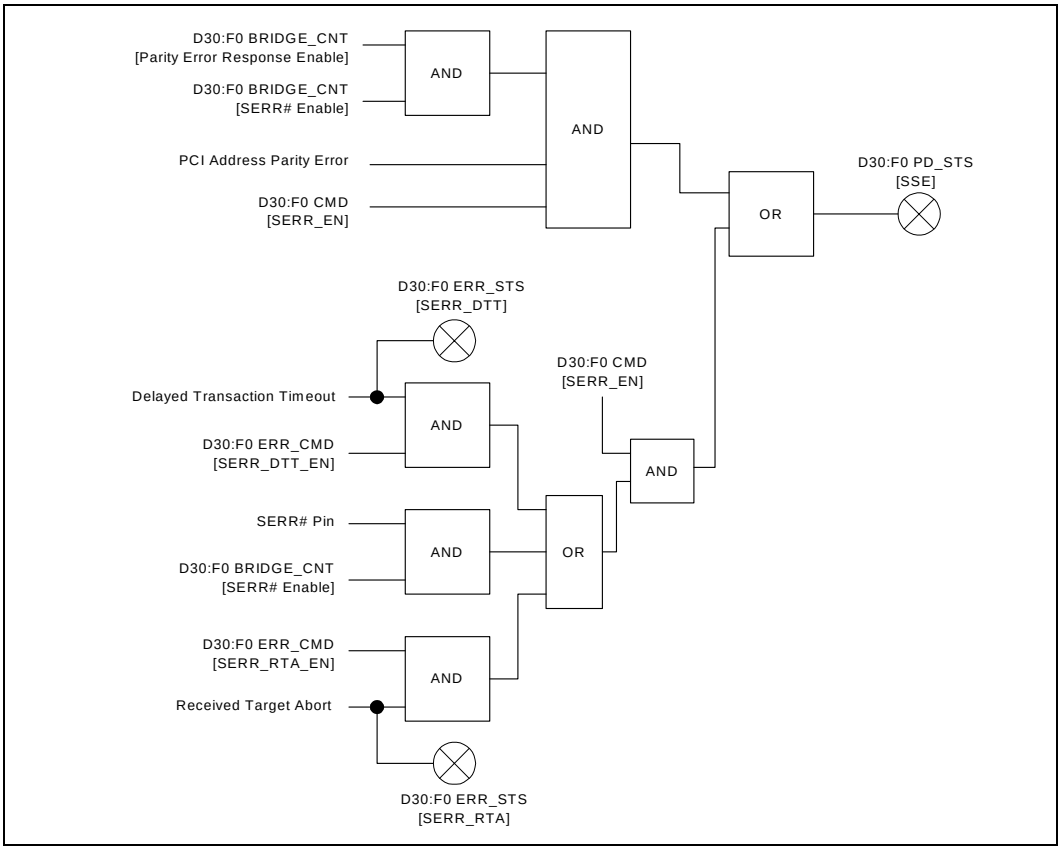


Figure 5-2. Secondary Status Register Error Reporting Logic

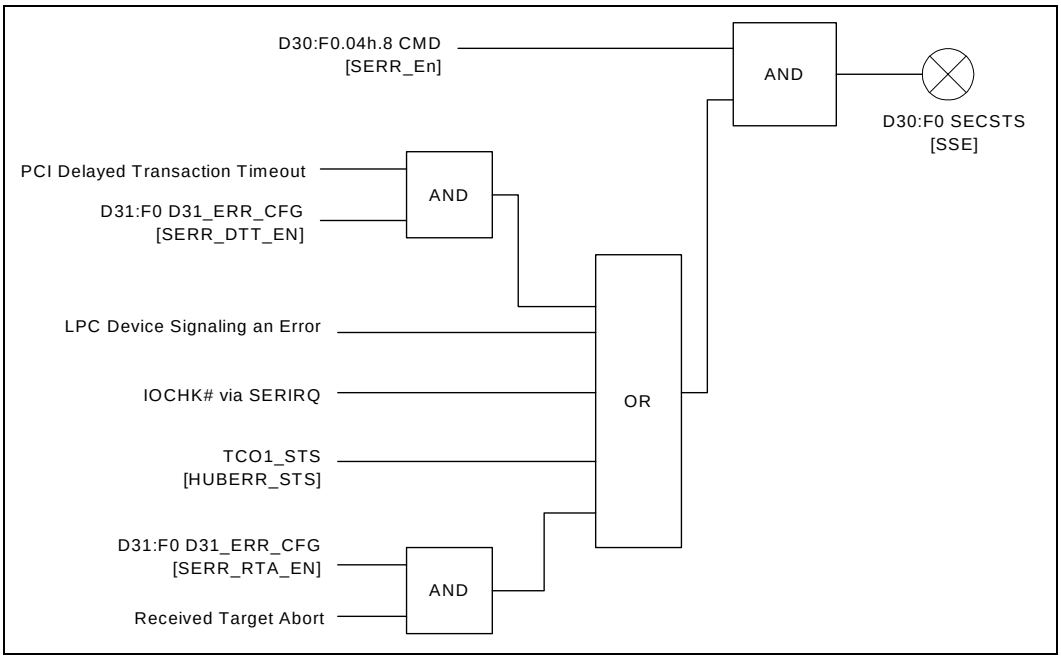
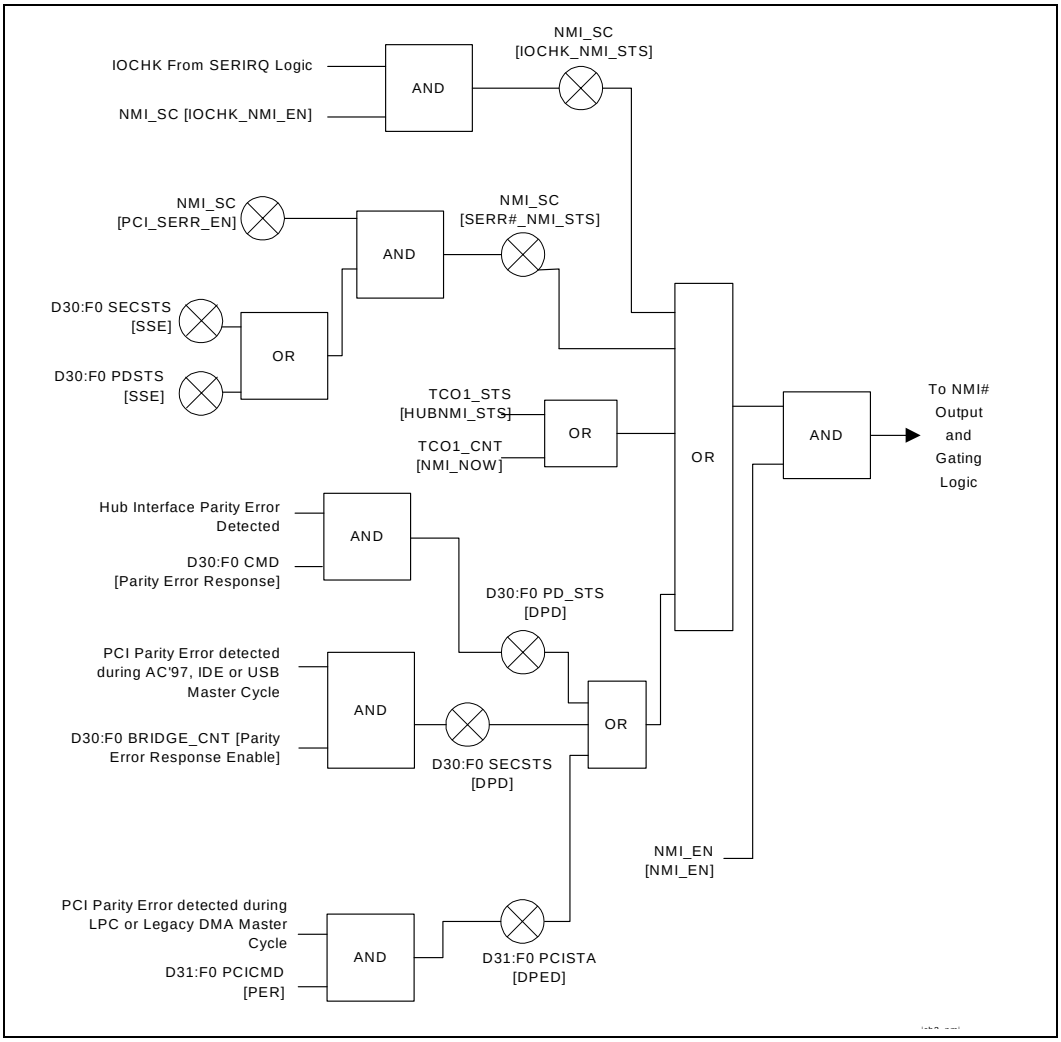


Figure 5-3. NMI# Generation Logic



5.1.5 Parity Error Detection

The ICH3 can detect and report different parity errors in the system. The ICH3 can be programmed to cause an NMI (or SMI# if NMI is routed to SMI#) based on detecting a parity error. The conceptual logic diagram in Figure 5-3 details all the parity errors that the ICH3 can detect, along with their respective enable bits, status bits, and the results.

Note: If NMIs are enabled, and parity error checking on PCI is also enabled, then parity errors will cause an NMI. Some operating systems will not attempt to recover from this NMI, since it considers the detection of a PCI error to be a catastrophic event.

5.1.6 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based “configuration space” that allows each device to contain up to 8 functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the ICH3. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The ICH3 only supports Mechanism #1.

Configuration cycles for PCI Bus #0 devices #2 through #31, and for PCI Bus numbers greater than 0 will be sent towards the ICH3 from the host controller. The ICH3 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus number registers of its P2P bridge to determine if the configuration cycle is meant for Primary PCI or a downstream PCI bus.

5.1.6.1 Type 0 to Type 0 Forwarding

When a Type 0 configuration cycle is received on hub interface to any function, the ICH3 forwards these cycles to PCI and then reclaims them. The ICH3 uses address bits AD[15:13] to communicate the ICH3 device numbers in Type 0 configuration cycles. If the Type 0 cycle on hub interface specifies any device number other than 29, 30 or 31, the ICH3 will not set any address bits in the range AD[31:11] during the corresponding transaction on PCI. Table 5-1 shows the device number translation.

Table 5-1. Type 0 Configuration Cycle Device Number Translation

Device # In Hub Interface Type 0 Cycle	AD[31:11] During Address Phase of Type 0 Cycle on PCI
0 through 28	0000000000000000_00000b
29	0000000000000000_00100b
30	0000000000000000_01000b
31	0000000000000000_10000b

The ICH3 logic will generate single dword configuration read and write cycles on the PCI bus. The ICH3 will generate a Type 0 configuration cycle for configurations to the bus number matching the PCI bus. Type 1 configuration cycles will be converted to Type 0 cycles in this case. If the cycle is targeting a device behind an external bridge, the ICH3 will run a Type 1 cycle on the PCI bus.

5.1.6.2 Type 1 to Type 0 Conversion

When the bus number for the Type 1 configuration cycle matches the PCI (Secondary) bus number, the ICH3 will convert the address as follows:

1. For device numbers 0 through 15, only one bit of the PCI address [31:16] will be set. If the device number is 0, AD[16] is set; if the device number is 1, AD[17] is set; etc.
2. The ICH3 will always drive 0s on bits AD[15:11] when converting Type 1 configurations cycles to Type 0 configuration cycles on PCI.
3. Address bits [10:1] will also be passed unchanged to PCI.
4. Address bit 0 will be changed to 0’.

5.1.7 PCI Dual Address Cycle (DAC) Support

The ICH3 supports Dual Address Cycle (DAC) format on PCI for cycles from PCI initiators to main memory. This allows PCI masters to generate an address up to 44 bits. The size of the actual supported memory space will be determined by the memory controller and the processor.

The DAC mode is only supported for PCI adapters and is not supported for any of the internal PCI masters (IDE, LAN, USB 1.1, AC'97, 8237 DMA, etc.).

When a PCI master wants to initiate a cycle with an address above 4 GB, it uses the following behavioral rules (See PCI 2.2 Specification, Section 3.9 for more details):

1. On the first clock of the cycle (when FRAME# is first active), the peripheral uses the DAC encoding on the C/BE# signals. This unique encoding is 1101.
2. Also during the first clock, the peripheral drives the AD[31:0] signals with the low address.
3. On the second clock, the peripheral drives AD[31:0] with the high address. The address is right justified: A[43:32] appear on AD[12:0]. The value of AD[31:13] is expected to be 0; however, the ICH3 ignores these bits. The C/BE# signals indicate the bus command type (Memory Read, Memory Write, etc.)
4. The rest of the cycle proceeds normally.

5.2 LAN Controller (B1:D8:F0)

The ICH3's integrated LAN Controller includes a 32-bit PCI controller that provides enhanced scatter-gather bus mastering capabilities and enables the LAN Controller to perform high speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 KB each help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN Controller to transmit data with minimum interframe spacing (IFS).

The ICH3 integrated LAN Controller can operate in either full duplex or half duplex mode. In full duplex mode the LAN Controller adheres with the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The integrated LAN Controller also includes an interface to a serial (4-pin) EEPROM. The EEPROM provides power-on initialization for hardware and software configuration parameters.

From a software perspective, the integrated LAN Controller appears to reside on the secondary side of the ICH3's virtual PCI-to-PCI Bridge (see Section 5.1.2). This is typically Bus 1, but may be assigned a different number, depending upon system configuration.

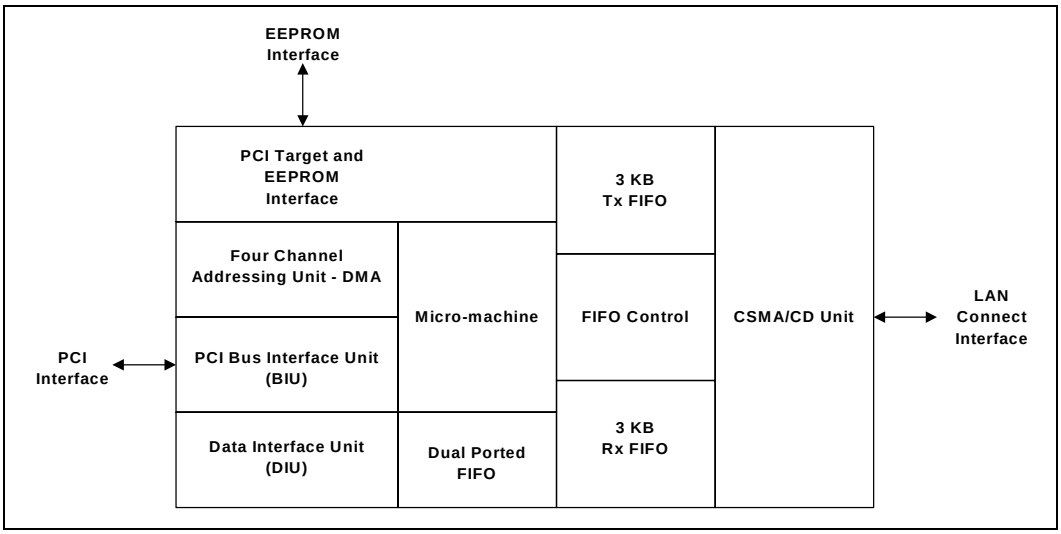
5.2.1 Feature Summary

- Compliance with Advanced Configuration and Power Interface and PCI Power Management standards
- Support for wake-up on interesting packets and link status change
- Support for remote power-up using Wake on LAN* (WOL) technology
- Deep power-down mode support
- Support of Wired for Management (WfM), Rev 2.0
- Backward compatible software with Intel 82557, 82558, and 82559
- TCP/UDP checksum off load capabilities
- Support for Intel's Adaptive Technology

5.2.2 LAN Controller Architectural Overview

Figure 5-4 is a high level block diagram of the ICH3 integrated LAN Controller. It is divided into four main subsystems: a Parallel subsystem, a FIFO subsystem and the Carrier-Sense Multiple Access with Collision Detect (CSMA/CD) unit.

Figure 5-4. Integrated LAN Controller Block Diagram



5.2.2.1 Parallel Subsystem

The parallel subsystem is broken down into several functional blocks: a PCI bus master interface, a micromachine processing unit and its corresponding microcode ROM, and a PCI Target Control/ EEPROM/ interface. The parallel subsystem also interfaces to the FIFO subsystem, passing data (such as transmit, receive, and configuration data) and command and status parameters between these two blocks.

The PCI bus master interface provides a complete interface to the PCI bus and is compliant with the *PCI Local Bus Specification*, Revision 2.2. The LAN Controller provides 32 bits of addressing and data, as well as the complete control interface to operate on the PCI bus. As a PCI target, it follows the PCI configuration format which allows all accesses to the LAN Controller to be automatically mapped into free memory and I/O space upon initialization of a PCI system. For processing of transmit and receive frames, the integrated LAN Controller operates as a master on the PCI bus, initiating zero wait-state transfers for accessing these data parameters.

The LAN Controller Control/Status Register Block is part of the PCI target element. The Control/ Status Register block consists of the following LAN Controller internal control registers: System Control Block (SCB), PORT, EEPROM Control and Management Data Interface (MDI) Control.

The micromachine is an embedded processing unit contained in the LAN Controller that enables Adaptive Technology. The micromachine accesses the LAN Controller's microcode ROM, working its way through the opcodes (or instructions) contained in the ROM to perform its functions. Parameters accessed from memory, such as pointers to data buffers, are also used by the micromachine during the processing of transmit or receive frames by the LAN Controller. A typical micromachine function is to transfer a data buffer pointer field to the LAN Controller's DMA unit for direct access to the data buffer. The micromachine is divided into two units, Receive Unit and Command Unit which includes transmit functions. These two units operate independently and concurrently. Control is switched between the two units according to the microcode instruction

flow. The independence of the Receive and Command units in the micromachine allows the LAN Controller to execute commands and receive incoming frames simultaneously, with no real-time processor intervention.

The LAN Controller contains an interface to an external serial EEPROM. The EEPROM is used to store relevant information for a LAN connection such as node address, as well as board manufacturing and configuration information. Both read and write accesses to the EEPROM are supported by the LAN Controller. Information on the EEPROM interface is detailed in Section 5.2.4.

5.2.2.2 FIFO Subsystem

The ICH3 LAN Controller FIFO subsystem consists of a 3-KB transmit FIFO and 3-KB receive FIFO. Each FIFO is unidirectional and independent of the other. The FIFO subsystem serves as the interface between the LAN Controller parallel side and the serial CSMA/CD unit. It provides a temporary buffer storage area for frames as they are either being received or transmitted by the LAN Controller, which improves performance:

- Transmit frames can be queued within the transmit FIFO, allowing back-to-back transmission within the minimum Interframe Spacing (IFS).
- The storage area in the FIFO allows the LAN Controller to withstand long PCI bus latencies without losing incoming data or corrupting outgoing data.
- The ICH3 LAN Controller's transmit FIFO threshold allows the transmit start threshold to be tuned to eliminate underruns while concurrent transmits are being performed.
- The FIFO subsection allows extended PCI zero wait-state burst accesses to or from the LAN Controller for both transmit and receive frames since the transfer is to the FIFO storage area rather than directly to the serial link.
- Transmissions resulting in errors (collision detection or data underrun) are retransmitted directly from the LAN Controller's FIFO, increasing performance and eliminating the need to re-access this data from the host system.
- Incoming runt receive frames (in other words, frames that are less than the legal minimum frame size) can be discarded automatically by the LAN Controller without transferring this faulty data to the host system.

5.2.2.3 Serial CSMA/CD Unit

The CSMA/CD unit of the ICH3 LAN Controller allows it to be connected to the 82562ET/EM 10/100 Mbps Ethernet LAN Connect components or the 82562EH 1 Mbps HomePNA*-compliant LAN Connect component. The CSMA/CD unit performs all of the functions of the 802.3 protocol such as frame formatting, frame stripping, collision handling, deferral to link traffic, etc. The CSMA/CD unit can also be placed in a full duplex mode which allows simultaneous transmission and reception of frames.

5.2.3 LAN Controller PCI Bus Interface

As a Fast Ethernet Controller, the role of the ICH3 integrated LAN Controller is to access transmitted data or deposit received data. The LAN Controller, as a bus master device, will initiate memory cycles via the PCI bus to fetch or deposit the required data.

In order to perform these actions, the LAN Controller is controlled and examined by the processor via its control and status structures and registers. Some of these control and status structures reside in the LAN Controller and some reside in system memory. For access to the LAN Controller's Control/Status Registers (CSR), the LAN Controller acts as a slave (in other words, a target device). The LAN Controller serves as a slave also while the processor accesses the EEPROM.

5.2.3.1 Bus Slave Operation

The ICH3 integrated LAN Controller serves as a target device in one of the following cases:

- Processor accesses to the LAN Controller System Control Block (SCB) Control/Status Registers (CSR)
- Processor accesses to the EEPROM through its CSR
- Processor accesses to the LAN Controller PORT address via the CSR
- Processor accesses to the MDI control register in the CSR

The size of the CSR memory space is 4 KB in the memory space and 64 bytes in the I/O space. The LAN Controller treats accesses to these memory spaces differently.

Control/Status Register (CSR) Accesses

The integrated LAN Controller supports zero wait-state single cycle memory or I/O mapped accesses to its CSR space. Separate BARs request 4 KB of memory space and 64 bytes of I/O space to accomplish this. Based on its needs, the software driver will use either memory or I/O mapping to access these registers. The LAN Controller provides 4 valid KB of CSR space, which include the following elements:

- System Control Block (SCB) registers
- PORT register
- EEPROM control register
- MDI control register
- Flow control registers

In the case of accessing the CSRs, the processor is the initiator and the LAN Controller is the target.

Read Accesses: The processor, as the initiator, drives address lines AD[31:0], the command and byte enable lines C/BE#[3:0] and the control lines IRDY# and FRAME#. As a slave, the LAN Controller controls the TRDY# signal and provides valid data on each data access. The LAN Controller allows the processor to issue only one read cycle when it accesses the CSRs, generating a disconnect by asserting the STOP# signal. The processor can insert wait-states by deasserting IRDY# when it is not ready.

Write Accesses: The processor, as the initiator, drives the address lines AD[31:0], the command and byte enable lines C/BE#[3:0] and the control lines IRDY# and FRAME#. It also provides the LAN Controller with valid data on each data access immediately after asserting IRDY#. The LAN

Controller controls the TRDY# signal and asserts it from the data access. The LAN Controller allows the processor to issue only one I/O write cycle to the CSRs, generating a disconnect by asserting the STOP# signal. This is true for both memory mapped and I/O mapped accesses.

Retry Premature Accesses

The LAN Controller responds with a Retry to any configuration cycle accessing the LAN Controller before the completion of the automatic read of the EEPROM. The LAN Controller may continue to Retry any configuration accesses until the EEPROM read is complete. The LAN Controller does not enforce the rule that the retried master must attempt to access the same address again in order to complete any delayed transaction. Any master access to the LAN Controller after the completion of the EEPROM read will be honored.

Error Handling

Data Parity Errors: The LAN Controller checks for data parity errors while it is the target of the transaction. If an error was detected, the LAN Controller always sets the detected parity error bit in the PCI configuration status register, bit 15. The LAN Controller also asserts PERR#, if the parity error response bit is set (PCI configuration command register, bit 6). The LAN Controller does not attempt to terminate a cycle in which a parity error was detected. This gives the initiator the option of recovery.

Target-Disconnect: The LAN Controller prematurely terminate a cycle in the following cases:

- After accesses to its CSR
- After accesses to the configuration space

System Error: The LAN Controller reports parity error during the address phase using the SERR# pin. If the SERR# enable bit in the PCI configuration command register or the parity error response bit are not set, the LAN Controller only sets the detected parity error bit (PCI configuration status register, bit 15). If SERR# enable and parity error response bits are both set, the LAN Controller sets the signaled system error bit (PCI configuration status register, bit 14) as well as the detected parity error bit and asserts SERR# for one clock.

The LAN Controller, when detecting system error, will claim the cycle if it was the target of the transaction and continue the transaction as if the address was correct.

Note: The LAN Controller will report a system error for any error during an address phase, whether or not it is involved in the current transaction.

5.2.3.2 Bus Master Operation

As a PCI Bus Master, the ICH3 integrated LAN Controller initiates memory cycles to fetch data for transmission or deposit received data and for accessing the memory resident control structures. The LAN Controller performs zero wait-state burst read and write cycles to the host main memory. For bus master cycles, the LAN Controller is the initiator and the host main memory (or the PCI host bridge, depending on the configuration of the system) is the target.

The processor provides the LAN Controller with action commands and pointers to the data buffers that reside in host main memory. The LAN Controller independently manages these structures and initiates burst memory cycles to transfer data to and from them. The LAN Controller uses the Memory Read Multiple (MR Multiple) command for burst accesses to data buffers and the Memory Read Line (MR Line) command for burst accesses to control structures. For all write

accesses to the control structure, the LAN Controller uses the Memory Write (MW) command. For write accesses to data structure, the LAN Controller may use either the Memory Write or Memory Write and Invalidate (MWI) commands.

Read Accesses: The LAN Controller performs block transfers from host system memory in order to perform frame transmission on the serial link. In this case, the LAN Controller initiates zero wait-state memory read burst cycles for these accesses. The length of a burst is bounded by the system and the LAN Controller's internal FIFO. The length of a read burst may also be bounded by the value of the Transmit DMA Maximum Byte Count in the Configure command. The Transmit DMA Maximum Byte Count value indicates the maximum number of transmit DMA PCI cycles that will be completed after an LAN Controller internal arbitration.

The LAN Controller, as the initiator, drives the address lines AD[31:0], the command and byte enable lines C/BE#[3:0] and the control lines IRDY# and FRAME#. The LAN Controller asserts IRDY# to support zero wait-state burst cycles. The target signals the LAN Controller that valid data is ready to be read by asserting the TRDY# signal.

Write Accesses: The LAN Controller performs block transfers to host system memory during frame reception. In this case, the LAN Controller initiates memory write burst cycles to deposit the data, usually without wait-states. The length of a burst is bounded by the system and the LAN Controller's internal FIFO threshold. The length of a write burst may also be bounded by the value of the Receive DMA Maximum Byte Count in the Configure command. The Receive DMA Maximum Byte Count value indicates the maximum number of receive DMA PCI transfers that will be completed before the LAN Controller internal arbitration.

The LAN Controller, as the initiator, drives the address lines AD[31:0], the command and byte enable lines C/BE#[3:0] and the control lines IRDY# and FRAME#. The LAN Controller asserts IRDY# to support zero wait-state burst cycles. The LAN Controller also drives valid data on AD[31:0] lines during each data phase (from the first clock and on). The target controls the length and signals completion of a data phase by deassertion and assertion of TRDY#.

- **Cycle Completion:** The LAN Controller completes (terminates) its initiated memory burst cycles in the following cases:
- **Normal Completion:** All transaction data has been transferred to or from the target device (for example, host main memory).
- **Backoff:** Latency Timer has expired and the bus grant signal (GNT#) was removed from the LAN Controller by the arbiter, indicating that the LAN Controller has been preempted by another bus master.
- **Transmit or Receive DMA Maximum Byte Count:** The LAN Controller burst has reached the length specified in the Transmit or Receive DMA Maximum Byte Count field in the Configure command block.
- **Target Termination:** The target may request to terminate the transaction with a target-disconnect, target-retry, or target-abort. In the first two cases, the LAN Controller initiates the cycle again. In the case of a target-abort, the LAN Controller sets the received target-abort bit in the PCI Configuration Status field (PCI configuration status register, bit 12) and does not re-initiate the cycle.
- **Master Abort:** The target of the transaction has not responded to the address initiated by the LAN Controller (in other words, DEVSEL# has not been asserted). The LAN Controller simply deasserts FRAME# and IRDY# as in the case of normal completion.
- **Error Condition:** In the event of parity or any other system error detection, the LAN Controller completes its current initiated transaction. Any further action taken by the LAN Controller depends on the type of error and other conditions.

Memory Write and Invalidate

The LAN Controller has four Direct Memory Access (DMA) channels. Of these four channels, the Receive DMA is used to deposit the large number of data bytes received from the link into system memory. The Receive DMA uses both the Memory Write (MW) and the Memory Write and Invalidate (MWI) commands. In order to use MWI, the LAN Controller must guarantee the following:

1. Minimum transfer of one cache line
2. Active byte enable bits (or BE[3:0]# are all low) during MWI access
3. The LAN Controller may cross the cache line boundary only if it intends to transfer the next cache line too.

In order to ensure the above conditions, the LAN Controller may use the MWI command only under the following conditions:

1. The Cache Line Size (CLS) written in the CLS Register during PCI configuration is 8 or 16 dwords.
2. The accessed address is cache line aligned.
3. The LAN Controller has at least 8 or 16 dwords of data in its receive FIFO.
4. There are at least 8 or 16 dwords of data space left in the system memory buffer.
5. The MWI enable bit in the PCI configuration command register, bit 4, should is set to 1b.
6. The MWI enable bit in the LAN Controller Configure command should is set to 1b.

If any one of the above conditions does not hold, the LAN Controller will use the MW command. If a MWI cycle has started and one of the conditions is no longer valid (for example, the data space in the memory buffer is now less than CLS), then the LAN Controller terminates the MWI cycle at the end of the cache line. The next cycle will be either a MW or MWI cycle depending on the conditions listed above.

If the LAN Controller started a MW cycle and reached a cache line boundary, it either continues or terminates the cycle depending on the terminate write on cache line configuration bit of the LAN Controller Configure command (byte 3, bit 3). If this bit is set, the LAN Controller terminates the MW cycle and attempts to start a new cycle. The new cycle is a MWI cycle if this bit is set and all of the above listed conditions are met. If the bit is not set, the LAN Controller continues the MW cycle across the cache line boundary if required.

Read Align

The Read Align feature enhances the LAN Controller’s performance in cache line oriented systems. In these particular systems, starting a PCI transaction on a non-cache line aligned address may cause low performance.

In order to resolve this performance anomaly, the LAN Controller attempts to terminate transmit DMA cycles on a cache line boundary and start the next transaction on a cache line aligned address. This feature is enabled when the read align enable bit is set in the LAN Controller Configure command (byte 3, bit 2).

If this bit is set, the LAN Controller operates as follows:

- When the LAN Controller is almost out of resources on the transmit DMA (i.e., the transmit FIFO is almost full), it attempts to terminate the read transaction on the nearest cache line boundary when possible.
- When the arbitration counter's feature is enabled (i.e., the Transmit DMA Maximum Byte Count value is set in the Configure command), the LAN Controller switches to other pending DMAs on cache line boundary only.

Note the following:

- This feature is not recommended for use in non-cache line oriented systems since it may cause shorter bursts and lower performance.
- This feature should be used only when the CLS Register in PCI Configuration space is set to 8 or 16.
- The LAN Controller reads all control data structures (including Receive Buffer Descriptors) from the first dword (even if it is not required) in order to maintain cache line alignment.

Error Handling

Data Parity Errors: As an initiator, the LAN Controller checks and detects data parity errors that occur during a transaction. If the parity error response bit is set (PCI configuration command register, bit 6), the LAN Controller also asserts PERR# and sets the data parity detected bit (PCI configuration status register, bit 8). In addition, if the error was detected by the LAN Controller during read cycles, it sets the detected parity error bit (PCI configuration status register, bit 15).

5.2.3.3 PCI Power Management

Enhanced support for the power management standard, *PCI Local Bus Specification*, Revision 2.2, is provided in the ICH3 integrated LAN Controller. The LAN Controller supports a large set of wake-up packets and the capability to wake the system from a low power state on a link status change. The LAN Controller enables the host system to be in a sleep state and remain virtually connected to the network.

After a power management event or link status change is detected, the LAN Controller will wake the host system. The sections below describe these events, the LAN Controller power states, and estimated power consumption at each power state.

Power States

The LAN Controller contains power management registers for PCI, and implements all four power states as defined in the *Power Management Network Device Class Reference Specification, Revision 1.0*. The four states, D0 through D3, vary from maximum power consumption at D0 to the minimum power consumption at D3. PCI transactions are only allowed in the D0 state, except for host accesses to the LAN Controller's PCI configuration registers. The D1 and D2 power management states enable intermediate power savings while providing the system wake-up capabilities. In the D3 cold state, the LAN Controller can provide wake-up capabilities. Wake-up indications from the LAN Controller are provided by the Power Management Event (PME#) signal.

- D0 Power State

  As defined in the *Network Device Class Reference Specification*, the device is fully functional in the D0 power state. In this state, the LAN Controller receives full power and should be providing full functionality. In the LAN Controller the D0 state is partitioned into two substates, D0 Uninitialized (D0u) and D0 Active (D0a).

  D0u is the LAN Controller's initial power state following a PCI RST#. While in the D0u state, the LAN Controller has PCI slave functionality to support its initialization by the host and supports Wake on LAN mode. Initialization of the CSR, Memory, or I/O base address registers in the PCI Configuration space switches the LAN Controller from the D0u state to the D0a state.

  In the D0a state, the LAN Controller provides its full functionality and consumes its nominal power. In addition, the LAN Controller supports wake on link status change (see Section 5.2.3.5). While it is active, the LAN Controller requires a nominal PCI clock signal (in other words, a clock frequency greater than 16 MHz) for proper operation. The LAN Controller supports a dynamic standby mode. In this mode, the LAN Controller is able to save almost as much power as it does in the static power-down states. The transition to or from standby is done dynamically by the LAN Controller and is transparent to the software.

- D1 Power State

  In order for a device to meet the D1 power state requirements, as specified in the *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 1.0, it must not allow bus transmission or interrupts; however, bus reception is allowed. Therefore, device context may be lost and the LAN Controller does not initiate any PCI activity. In this state, the LAN Controller responds only to PCI accesses to its configuration space and system wake-up events.

  The LAN Controller retains link integrity and monitors the link for any wake-up events such as wake-up packets or link status change. Following a wake-up event, the LAN Controller asserts the PME# signal.

- D2 Power State

  The ACPI D2 power state is similar in functionality to the D1 power state. In addition to D1 functionality, the LAN Controller can provide a lower power mode with wake-on-link status change capability. The LAN Controller may enter this mode if the link is down while the LAN Controller is in the D2 state. In this state, the LAN Controller monitors the link for a transition from an invalid to a valid link.

  The sub-10 mA state due to an invalid link can be enabled or disabled by a configuration bit in the Power Management Driver Register (PMDR). The LAN Controller will consume in D2 <10 mA regardless of the link status. It is the LAN Connect component that consumes much less power during link down, hence LAN Controller in this state can consume <10 mA.

- D3 Power State

  In the D3 power state, the LAN Controller has the same capabilities and consumes the same amount of power as it does in the D2 state. However, it enables the PCI system to be in the B3 state. If the PCI system is in the B3 state (in other words, no PCI power is present), the LAN

Controller provides wake-up capabilities. If PME is disabled, the LAN Controller does not provide wake-up capability or maintain link integrity. In this mode the LAN Controller consumes its minimal power.

The LAN Controller enables a system to be in a sub-5 Watt state (low power state) and still be virtually connected. More specifically, the LAN Controller supports full wake-up capabilities while it is in the D3 cold state. The LAN Controller is in the ICH3 resume well, and thus is connected to an auxiliary power source (V AUX), which enables it to provide wake-up functionality while the PCI power is off.

5.2.3.4 PCI Reset Signal

The PCIRST# signal may be activated in one of the following cases:

- During S3–S5 states
- Due to a CF9h reset

If PME# is enabled (in the PCI power management registers), PCIRST# assertion does not affect any PME# related circuits (in other words, PCI power management registers and the wake-up packet would not be affected). While PCIRST# is active, the LAN Controller ignores other PCI signals. The configuration of the LAN Controller registers associated with ACPI wake events is not affected by PCIRST#.

The integrated LAN Controller uses the PCIRST# or the PWROK signal as an indication to ignore the PCI interface. Following the deassertion of PCIRST#, the LAN Controller PCI Configuration Space, MAC configuration, and memory structure are initialized while preserving the PME# signal and its context.

5.2.3.5 Wake-Up Events

There are two types of wake-up events: “Interesting” Packets and Link Status Change. These two events are detailed below.

Note: If the Wake on LAN bit in the EEPROM is not set, wake-up events are supported only if the PME enable bit in the Power Management Control/Status Register (PMCSR) is set. However, if the Wake on LAN bit in the EEPROM is set, and Wake on Magic Packet* or Wake on Link Status Change are enabled, the power management enable bit is ignored with respect to these events. In the latter case, PME# would be asserted by these events.

“Interesting” Packet Event

In the power-down state, the LAN Controller is capable of recognizing “interesting” packets. The LAN Controller supports pre-defined and programmable packets that can be defined as any of the following:

- ARP Packets (with Multiple IP addresses)
- Direct Packets (with or without type qualification)
- Magic Packet
- Neighbor Discovery Multicast Address Packet (‘ARP’ in IPv6 environment)
- NetBIOS over TCP/IP (NBT) Query Packet (under IPv4)
- Internetwork Package Exchange* (IPX) Diagnostic Packet

This allows the LAN Controller to handle various packet types. In general, the LAN Controller supports programmable filtering of any packet in the first 128 bytes.

When the LAN Controller is in one of the low power states, it searches for a predefined pattern in the first 128 bytes of the incoming packets. The only exception is the Magic Packet, which is scanned for the entire frame. The LAN Controller will classify the incoming packets as one of the following categories:

- **No Match:** The LAN Controller discards the packet and continues to process the incoming packets.
- **TCO Packet:** The LAN Controller implements perfect filtering of TCO packets. After a TCO packet is processed, the LAN Controller is ready for the next incoming packet. TCO packets are treated as any other wake-up packet and may assert the PME# signal if configured to do so.
- **Wake-Up Packet:** The LAN Controller is capable of recognizing and storing the first 128 bytes of a wake-up packet. If a wake-up packet is larger than 128 bytes, its tail is discarded by the LAN Controller. After the system is fully powered-up, software has the ability to determine the cause of the wake-up event via the PMDR and dump the stored data to the host memory.

  Magic Packets are an exception. The Magic Packets may cause a power management event and set an indication bit in the PMDR; however, it is not stored by the LAN Controller for use by the system when it is woken up.

Link Status Change Event

The LAN Controller link status indication circuit is capable of issuing a PME on a link status change from a valid link to an invalid link condition or vice versa. The LAN Controller reports a PME link status event in all power states. If the Wake on LAN bit in the EEPROM is not set, the PME# signal is gated by the PME enable bit in the PMCSR and the CSMA Configure command.

5.2.3.6 Wake on LAN* (Preboot Wake-Up)

The LAN Controller enters Wake on LAN mode after reset if the Wake on LAN bit in the EEPROM is set. At this point, the LAN Controller is in the D0u state.

When the LAN Controller is in Wake on LAN mode:

- The LAN Controller scans incoming packets for a Magic Packet and asserts the PME# signal for 52 ms when a one is detected in Wake on LAN mode.
- The Activity LED changes its functionality to indicates that the received frame passed Individual Address (IA) filtering or broadcast filtering.
- The PCI configuration registers are accessible to the host.

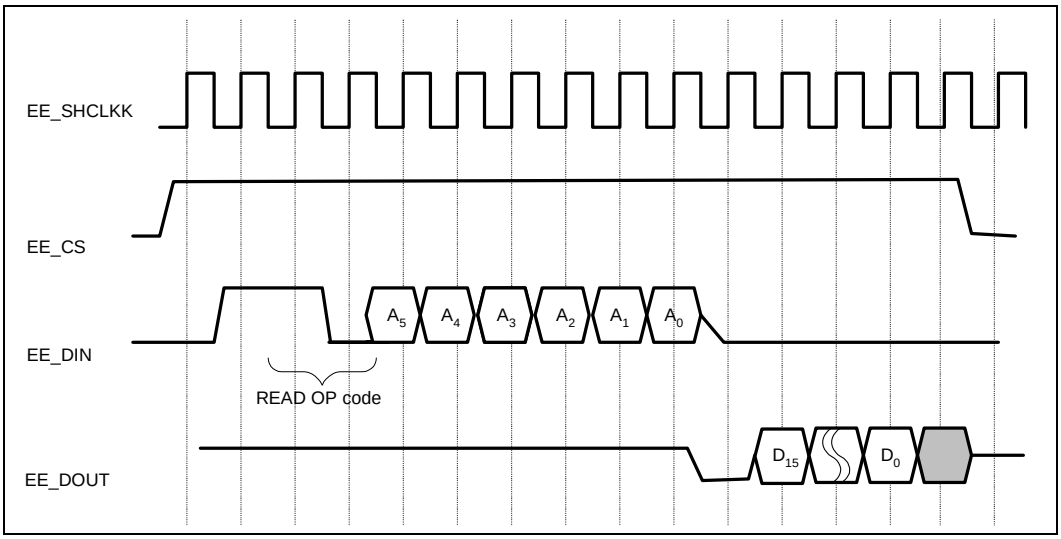
The LAN Controller switches from Wake on LAN mode to the D0a power state following a setup of the Memory or I/O base address registers in the PCI Configuration space.

5.2.4 Serial EEPROM Interface

The serial EEPROM stores configuration data for the ICH3 integrated LAN Controller and is a serial in/serial out device. The LAN Controller supports a 64-register or 256-register size EEPROM and automatically detects the EEPROM's size. The EEPROM should operate at a frequency of at least 1 MHz.

All accesses, either read or write, are preceded by a command instruction to the device. The address field is six bits for a 64-register EEPROM or eight bits for a 256-register EEPROM. The end of the address field is indicated by a dummy zero bit from the EEPROM, which indicates the entire address field has been transferred to the device. An EEPROM read instruction waveform is shown in Figure 5-5.

Figure 5-5. 64-Word EEPROM Read Instruction Waveform



The LAN Controller performs an automatic read of seven words (0h, 1h, 2h, Ah, Bh, Ch and Dh) of the EEPROM after the deassertion of Reset.

5.2.5 CSMA/CD Unit

The ICH3 integrated LAN Controller CSMA/CD unit implements both the IEEE 802.3 Ethernet 10 Mbps and IEEE 802.3u Fast Ethernet 100 Mbps standards. It also supports the 1 Mbps Home Phone line Networking Alliance (HomePNA*) specification effort. It performs all the CSMA/CD protocol functions such as transmission, reception, collision handling, etc. The LAN Controller CSMA/CD unit interfaces to the 82562ET/EM 10/100 Mbps Ethernet or the 82562EH 1 Mbps HomePNA*-compliant LAN Connect component through the ICH3's LAN Connect interface signals.

5.2.5.1 Full Duplex

When operating in full-duplex mode the LAN Controller can transmit and receive frames simultaneously. Transmission starts regardless of the state of the internal receive path. Reception starts when the LAN Connect component detects a valid frame on its receive differential pair. The ICH3 integrated LAN Controller also supports the IEEE 802.3x flow control standard, when in full-duplex mode.

The LAN Controller operates in either half-duplex mode or full-duplex mode. For proper operation, both the LAN Controller CSMA/CD module and the discrete LAN Connect component must be set to the same duplex mode. The CSMA duplex mode is set by the LAN Controller Configure command or forced by automatically tracking the mode in the LAN Connect component. Following reset, the CSMA will default to automatically track the LAN Connect component duplex mode.

The selection of duplex operation (full or half) and flow control is done in two levels: MAC and LAN Connect.

5.2.5.2 Flow Control

The LAN Controller supports IEEE 802.3x frame based flow control frames only in both full duplex and half duplex switched environments. The LAN Controller flow control feature is not intended to be used in shared media environments.

Flow control is optional in full-duplex mode and is selected through software configuration. There are three modes of flow control that can be selected: frame-based transmit flow control, frame-based receive flow control, and none.

5.2.5.3 Address Filtering Modifications

The LAN Controller can be configured to ignore one bit when checking for its Individual Address (IA) on incoming receive frames. The address bit, known as the Upper/Lower (U/L) bit, is the second least significant bit of the first byte of the IA. This bit may be used, in some cases, as a priority indication bit. When configured to do so, the LAN Controller passes any frame that matches all other 47 address bits of its IA, regardless of the U/L bit value.

This configuration only affects the LAN Controller specific IA and not multicast, multi-IA or broadcast address filtering. The LAN Controller does not attribute any priority to frames with this bit set, it simply passes them to memory regardless of this bit.

5.2.5.4 VLAN Support

The LAN Controller supports the IEEE 802.1 standard VLAN. All VLAN flows will be implemented by software. The LAN Controller supports the reception of long frames, specifically frames longer than 1518 bytes, including the CRC, if software sets the long receive OK bit in the Configuration command. Otherwise, “long” frames are discarded.

5.2.6 Media Management Interface

The management interface allows the processor to control the LAN Connect component via a control register in the ICH3 integrated LAN Controller. This allows the software driver to place the LAN Connect in specific modes such as full duplex, loopback, power down, etc., without the need for specific hardware pins to select the desired mode. This structure allows the LAN Controller to query the LAN Connect component for status of the link. This register is the MDI control register and resides at offset 10h in the LAN Controller CSR. The MDI registers reside within the LAN Connect component, and are described in detail in the LAN Connect component's datasheet. The processor writes commands to this register and the LAN Controller reads or writes the control/ status parameters to the LAN Connect component through the MDI register.

5.2.7 TCO Functionality

The ICH3 integrated LAN controller supports management communication to reduce Total Cost of Ownership (TCO). It has a System Management Bus (SMB) on which the LAN controller is a slave device. The SMB is used as an interface between the LAN controller and the integrated host controller. An EEPROM of 256 words is required to support the heartbeat command.

5.2.7.1 Receive Functionality

In the power-up state, the LAN controller transfers TCO packets to the host as any other packet. These packets include a new status indication bit in the Receive Frame Descriptor (RFD) status register and have a specific port number indicating TCO packet recognition. In the power-down state, the TCO packets are treated as wake-up packets. The ICH3 integrated LAN controller asserts the PME# signal and delivers the first 120 bytes of the packet to the host.

5.2.7.2 Transmit Functionality

The ICH3 integrated LAN controller supports the Heartbeat (HB) Transmission command from the SMB interface. The send HB Packet command includes a system health status issued by the integrated system controller. The LAN controller computes a matched checksum and CRC and will transmit the HB packet from its serial EEPROM. The HB packet size and structure are not limited as long as it fits within the EEPROM size. In this case, the EEPROM size is 256 words to enable the storage of the HB packet (the first 64 words are used for driver specific data).

Note: On the SMB, the send Heartbeat Packet command is not normally used in the D0 power state. The one exception in which it is used in the D0 state is when the system is hung. In normal operating mode, the heartbeat packets are transmitted through the ICH3 integrated LAN controller software similar to other packets.

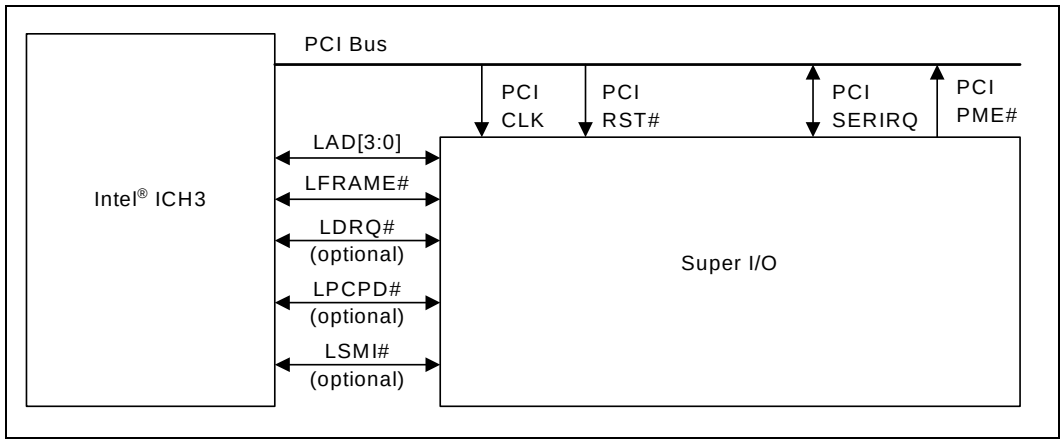
5.3 LPC Bridge (w/ System and Management Functions) (D31:F0)

The LPC Bridge function of the ICH3 resides in PCI Device 31:Function 0. In addition to the LPC bridge function, D31:F0 contains other functional units including DMA, Interrupt Controllers, Timers, Power Management, System Management, GPIO, and RTC. In this chapter, registers and functions associated with other functional units (power management, GPIO, USB, IDE, etc.) are described in their respective Sections.

5.3.1 LPC Interface

The ICH3 implements an LPC I/F as described in the *Low Pin Count (LPC) Interface Specification*, Revision 1.0. The LPC I/F to the ICH3 is shown in Figure 5-6. Note that the ICH3 implements all of the signals that are shown as optional, but peripherals are not required to do so.

Figure 5-6. LPC Interface Diagram



5.3.1.1 LPC Cycle Types

The ICH3 implements all of the cycle types described in the *Low Pin Count (LPC) Interface Specification*, Revision 1.0. Table 5-2 shows the cycle types supported by the ICH3.

Table 5-2. LPC Cycle Types Supported

Cycle Type	Comment
Memory Read	Single: 1 byte only
Memory Write	Single: 1 byte only
I/O Read	1 byte only. ICH3 breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers. See Note 1 below.
I/O Write	1 byte only. ICH3 breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers. See Note 1 below.
DMA Read	Can be 1, or 2 bytes
DMA Write	Can be 1, or 2 bytes
Bus Master Read	Can be 1, 2, or 4 bytes. (See Note 2 below)
Bus Master Write	Can be 1, 2, or 4 bytes. (See Note 2 below)

NOTES:
1. For memory cycles below 16 MB which do not target enabled FWH ranges, the ICH3 will perform standard LPC memory cycles. It will only attempt 8-bit transfers. If the cycle appears on PCI as a 16-bit transfer, it will appear as two consecutive 8-bit transfers on LPC. Likewise, if the cycle appears as a 32-bit transfer on PCI, it will appear as four consecutive 8-bit transfers on LPC. If the cycle is not claimed by any peripheral, it will be subsequently aborted, and the ICH3 will return a value of all 1s to the processor. This is done to maintain compatibility with ISA memory cycles where pull-up resistors would keep the bus high if no device responds.
2. Bus Master Read or Write cycles must be naturally aligned. For example, a 1-byte transfer can be to any address. However, the 2-byte transfer must be word aligned (i.e., with an address where A0=0). A dword transfer must be dword aligned (i.e., with an address where A1and A0 are both 0)

5.3.1.2 Start Field Definition

Table 5-3. Start Field Bit Definitions

Bits[3:0] Encoding	Definition
0000	Start of cycle for a generic target.
0010	Grant for bus master 0.
0011	Grant for bus master 1.
1111	Stop/Abort: End of a cycle for a target.

NOTE: All other encodings are Reserved.

5.3.1.3 Cycle Type / Direction (CYCTYPE + DIR)

The ICH3 will always drive bit 0 of this field to 0. Peripherals running bus master cycles must also drive bit 0 to 0. Table 5-4 shows the valid bit encodings.

Table 5-4. Cycle Type Bit Definitions

Bits[3:2]	Bit[1]	Definition
00	0	I/O Read
00	1	I/O Write
01	0	Memory Read
01	1	Memory Write
10	0	DMA Read
10	1	DMA Write
11	x	Reserved. If a peripheral performing a bus master cycle generates this value, the ICH3 will abort the cycle.

5.3.1.4 SIZE

Bits[3:2] are reserved. The ICH3 will always drive them to 00. Peripherals running bus master cycles are also supposed to drive 00 for bits 3:2; however, the ICH3 will ignore those bits. Table 5-5 shows the encoding for Bits[1:0].

Table 5-5. Transfer Size Bit Definition

Bits[1:0]	Size
00	8-bit transfer (1 byte)
01	16-bit transfer (2 bytes)
10	Reserved. The ICH3 never drives this combination. If a peripheral running a bus master cycle drives this combination, the ICH3 may abort the transfer.
11	32-bit transfer (4 bytes)

5.3.1.5 SYNC

Valid values for the SYNC field are shown in Table 5-6.

Table 5-6. SYNC Bit Definition

Bits[3:0]	Indication
0000	**Ready:** SYNC achieved with no error. For DMA transfers, this also indicates DMA request deassertion and no more transfers desired for that channel.
0101	**Short Wait:** Part indicating wait-states. For bus master cycles, the ICH3 will not use this encoding. It will instead use the Long Wait encoding (see next encoding below).
0110	**Long Wait:** Part indicating wait-states, and many wait-states will be added. This encoding driven by the ICH3 for bus master cycles, rather than the Short Wait (0101).
1001	**Ready More (Used only by peripheral for DMA cycle):** SYNC achieved with no error and more DMA transfers desired to continue after this transfer. This value is valid only on DMA transfers and is not allowed for any other type of cycle.
1010	**Error:** Sync achieved with error. This is generally used to replace the SERR# or IOCHK# signal on the PCI/ISA bus. It indicates that the data is to be transferred, but there is a serious error in this transfer. For DMA transfers, this not only indicates an error, but also indicates DMA request deassertion and no more transfers desired for that channel.

NOTE: All other combinations are Reserved.

5.3.1.6 SYNC Time-out

There are several error cases that can occur on the LPC I/F. Table 5-7 identifies the failing cases and the ICH3 responses.

Table 5-7. Intel® ICH3 Response to Sync Failures

Possible Sync Failure	Intel® ICH3 Response
ICH3 starts a Memory, I/O, or DMA cycle, but no device drives a valid SYNC after four consecutive clocks. This could occur if the processor tries to access an I/O location to which no device is mapped.	ICH3 aborts the cycle after the fourth clock.
ICH3 drives a Memory, I/O, or DMA cycle, and a peripheral drives more than eight consecutive valid SYNC to insert wait-states using the Short (0101b) encoding for SYNC. This could occur if the peripheral is not operating properly.	Continues waiting
ICH3 starts a Memory, I/O, or DMA cycle, and a peripheral drives an invalid SYNC pattern. This could occur if the peripheral is not operating properly or if there is excessive noise on the LPC I/F.	ICH3 aborts the cycle when the invalid Sync is recognized.

There may be other peripheral failure conditions; however, these are not handled by the ICH3.

5.3.1.7 SYNC Error Indication

The SYNC protocol allows the peripheral to report an error via the LAD[3:0] = 1010b encoding. The intent of this encoding is to give peripherals a method of communicating errors to aid higher layers with more robust error recovery.

If the ICH3 was reading data from a peripheral, data will still be transferred in the next two nibbles. This data may be invalid, but it must be transferred by the peripheral. If the ICH3 was writing data to the peripheral, the data had already been transferred.

In the case of multiple byte cycles, such as for memory and DMA cycles, an error SYNC terminates the cycle. Therefore, if the ICH3 is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

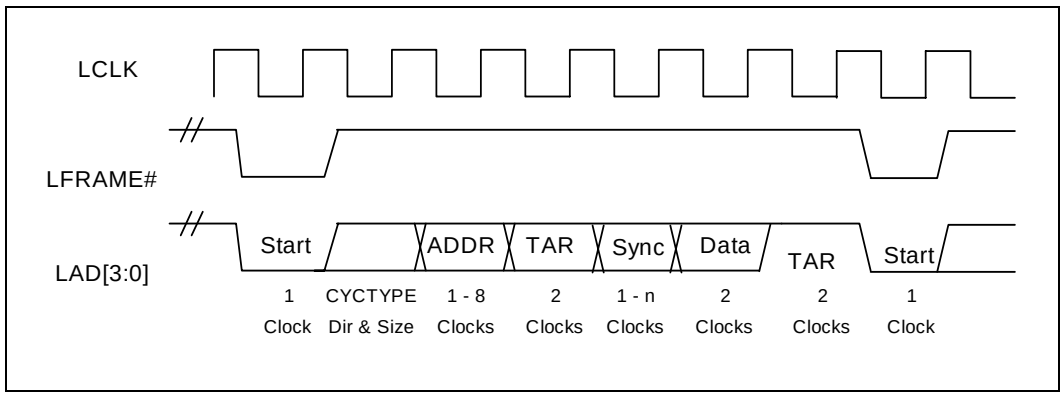
Upon recognizing the SYNC field indicating an error, the ICH3 will treat this the same as IOCHK# going active on the ISA bus.

5.3.1.8 LFRAME# Usage

Start of Cycle

For Memory, I/O, and DMA cycles, the ICH3 asserts LFRAME# for 1 clock at the beginning of the cycle (Figure 5-7). During that clock, the ICH3 drives LAD[3:0] with the proper START field.

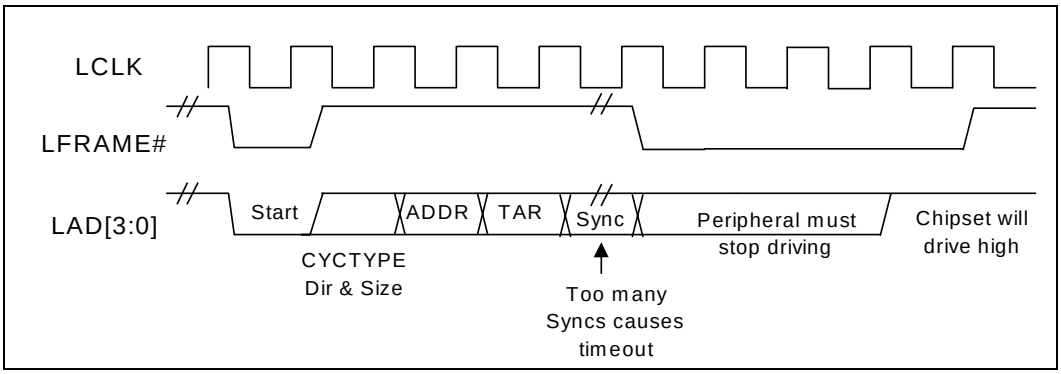
Figure 5-7. Typical Timing for LFRAME#



Abort Mechanism

When performing an Abort, the ICH3 drives LFRAME# active for four consecutive clocks. On the fourth clock, it drives LAD[3:0] to 1111b.

Figure 5-8. Abort Mechanism



The ICH3 performs an abort for the following cases (possible failure cases):

- ICH3 starts a memory, I/O, or DMA cycle, but no device drives a valid SYNC after four consecutive clocks.
- ICH3 starts a memory, I/O, or DMA cycle, and the peripheral drives an invalid SYNC pattern.
- A peripheral drives an illegal address when performing bus master cycles.
- A peripheral drives an invalid value.

5.3.1.9 I/O Cycles

For I/O cycles targeting registers specified in the ICH3's decode ranges, the ICH3 performs I/O cycles as defined in the LPC specification. These will be 8-bit transfers. If the processor attempts a 16-bit or 32-bit transfer, the ICH3 breaks the cycle up into multiple 8-bit transfers to consecutive I/O addresses.

Note: If the cycle is not claimed by any peripheral (and subsequently aborted), the ICH3 returns a value of all 1s (FFh) to the processor. This is to maintain compatibility with ISA I/O cycles where pull-up resistors would keep the bus high if no device responds.

5.3.1.10 Bus Master Cycles

The ICH3 supports Bus Master cycles and requests (using LDRQ#) as defined in the LPC specification. The ICH3 has two LDRQ# inputs, and thus supports two separate bus master devices. It uses the associated START fields for Bus Master 0 (0010b) or Bus Master 1 (0011b).

Note: The ICH3 does not support LPC Bus Masters performing I/O cycles. LPC Bus Masters should only perform memory read or memory write cycles.

5.3.1.11 LPC Power Management

LPCPD# Protocol

Same timings as for SUS_STAT#. Upon driving SUS_STAT# low, LPC peripherals drives LDRQ# low or tri-state it. The ICH3 shuts off the LDRQ# input buffers. After driving SUS_STAT# active, the ICH3 drives LFRAME# low and tri-states (or drive low) LAD[3:0].

5.3.1.12 Configuration and Intel® ICH3 Implications

LPC I/F Decoders

To allow the I/O cycles and memory mapped cycles to go to the LPC I/F, the ICH3 includes several decoders. During configuration, the ICH3 must be programmed with the same decode ranges as the peripheral. The decoders are programmed via the Device 31:Function 0 configuration space.

Note: The ICH3 can not accept PCI write cycles from PCI-to-PCI bridges or devices with similar characteristics (specifically those with a “Retry Read” feature which is enabled) to an LPC device if there is an outstanding LPC read cycle towards the same PCI device or bridge. These cycles are not part of normal system operation, but may be encountered as part of platform validation testing using custom test fixtures.

Bus Master Device Mapping and START Fields

Bus Masters must have a unique START field. In the case of the ICH3 that supports 2 LPC bus masters, it will drive 0010 for the START field for grants to bus master #0 (requested via LDRQ[0]#) and 0011 for grants to bus master #1 (requested via LDRQ[1]#.). Thus, no registers are needed to configure the START fields for a particular bus master.

5.4 DMA Operation (D31:F0)

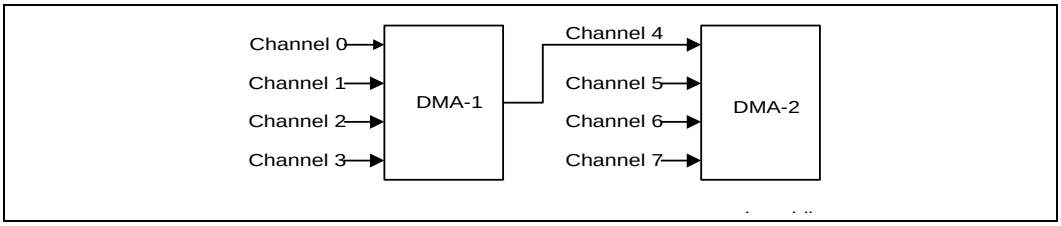
The ICH3 supports two types of DMA: LPC and PC/PCI. DMA via LPC is similar to ISA DMA. LPC DMA and PC/PCI DMA use the ICH3’s DMA controller.

The DMA controller has registers that are fixed in the lower 64 KB of I/O space.

The DMA controller is configured using registers in the PCI configuration space. These registers allow configuration of individual channels for use by LPC or PC/PCI DMA.

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Figure 5-9). DMA Controller 1 (DMA-1) corresponds to DMA Channels 0–3 and DMA Controller 2 (DMA-2) corresponds to Channels 5–7. DMA Channel 4 is used to cascade the two controllers and will default to cascade mode in the DMA Channel Mode (DCM) Register. Channel 4 is not available for any other purpose. In addition to accepting requests from DMA slaves, the DMA controller also responds to requests that software initiates. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1.

Figure 5-9. Intel® ICH3 DMA Controller



Each DMA channel is hardwired to the compatible settings for DMA device size: channels [3:0] are hardwired to 8-bit, count-by-bytes transfers; channels [7:5] are hardwired to 16-bit, count-by-words (address shifted) transfers.

ICH3 provides 24-bit addressing in compliance with the ISA-Compatible specification. Each channel includes a 16-bit ISA-compatible current register which holds the 16 least-significant bits of the 24-bit address, an ISA-compatible page register which contains the eight next most significant bits of address.

The DMA controller also features refresh address generation, and autoinitialization following a DMA termination.

5.4.1 Channel Priority

For priority resolution, the DMA consists of two logical channel groups: channels 0–3 and channels 4–7. Each group may be in either fixed or rotate mode, as determined by the DMA Command Register.

DMA I/O slaves normally assert their DREQ line to arbitrate for DMA service. However, a software request for DMA service can be presented through each channel's DMA request register. A software request is subject to the same prioritization as any hardware request. Please see the detailed register description for request register programming information in the DMA register description section.

5.4.1.1 Fixed Priority

The initial fixed priority structure is as follows:

High priority	Low priority
(0, 1, 2, 3)	(5, 6, 7)

The fixed priority ordering is 0, 1, 2, 3, 5, 6, and 7. In this scheme, Channel 0 has the highest priority, and channel 7 has the lowest priority. Channels [3:0] of DMA-1 assume the priority position of Channel 4 in DMA-2, thus taking priority over channels 5, 6, and 7.

5.4.1.2 Rotating Priority

Rotation allows for “fairness” in priority resolution. The priority chain rotates so that the last channel serviced is assigned the lowest priority in the channel group (0–3, 5–7).

Channels 0–3 rotate as a group of 4. They are always placed between Channel 5 and Channel 7 in the priority list.

Channel 5–7 rotate as part of a group of 4. That is, channels (5–7) form the first three positions in the rotation, while channel group (0–3) comprises the fourth position in the arbitration.

5.4.2 Address Compatibility Mode

Whenever the DMA is operating, the addresses do not increment or decrement through the high- and low-page registers. Therefore, if a 24-bit address is 01FFFFh and increments, the next address will be 010000h, not 020000h. Similarly, if a 24-bit address is 020000h and decrements, the next address will be 02FFFFh, not 01FFFFh. This is compatible with the 82C37 and page register implementation used in the PC-AT. This mode is set after CPURST is valid.

5.4.3 Summary of DMA Transfer Sizes

Table 5-8 lists each of the DMA device transfer sizes. The column labeled “Current Byte/Word Count Register” indicates that the register contents represents either the number of bytes to transfer or the number of 16-bit words to transfer. The column labeled “Current Address Increment/ Decrement” indicates the number added to or taken from the current address register after each DMA transfer cycle. The DMA channel mode register determines if the current address register will be incremented or decremented.

5.4.3.1 Address Shifting When Programmed for 16-Bit I/O Count by Words

Table 5-8. DMA Transfer Size

DMA Device Date Size And Word Count	Current Byte/Word Count Register	Current Address Increment/Decrement
8-Bit I/O, Count By Bytes	Bytes	1
16-Bit I/O, Count By Words (Address Shifted)	Words	1

The ICH3 maintains compatibility with the implementation of the DMA in the PC AT that used the 82C37. The DMA shifts the addresses for transfers to/from a 16-bit device count-by-words. Note that the least significant bit of the low-page register is dropped in 16-bit shifted mode. When programming the current address register (when the DMA channel is in this mode), the Current Address must be programmed to an even address with the address value shifted right by one bit. The address shifting is shown in Table 5-9.

Table 5-9. Address Shifting in 16-Bit I/O DMA Transfers

Output Address	8-Bit I/O Programmed Address (Ch 0–3)	16-Bit I/O Programmed Address (Ch 5–7) (Shifted)
A0 A[16:1] A[23:17]	A0 A[16:1] A[23:17]	0 A[15:0] A[23:17]

NOTE: The least significant bit of the page register is dropped in 16-bit shifted mode.

5.4.4 Autoinitialize

By programming a bit in the DMA channel mode register, a channel may be set up as an autoinitialize channel. When a channel undergoes autoinitialization, the original values of the current page, current address and current byte/word count registers are automatically restored from the base page, address, and byte/word count registers of that channel following TC. The base registers are loaded simultaneously with the current registers by the microprocessor when the DMA channel is programmed and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialize, the channel is ready to perform another DMA service, without processor intervention, as soon as a valid DREQ is detected.

5.4.5 Software Commands

There are three additional special software commands that the DMA controller can execute. The three software commands are:

1. Clear Byte Pointer Flip-Flop
2. Master Clear
3. Clear Mask Register

They do not depend on any specific bit pattern on the data bus.

5.4.5.1 Clear Byte Pointer Flip-Flop

This command is executed prior to writing or reading new address or word count information to/ from the DMA controller. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

When the host processor is reading or writing DMA registers, two byte pointer flip-flops are used; one for channels 0–3 and one for channels 4–7. Both of these act independently. There are separate software commands for clearing each of them (0Ch for channels 0–3, 0D8h for channels 4–7).

5.4.5.2 DMA Master Clear

This software instruction has the same effect as the hardware reset. The command, status, request, and internal first/last flip-flop registers are cleared and the mask register is set. The DMA controller will enter the idle cycle.

There are two independent master clear commands; 0Dh which acts on channels 0–3, and 0DAh which acts on channels 4–7.

5.4.5.3 Clear Mask Register

This command clears the mask bits of all four channels, enabling them to accept DMA requests. I/O port 00Eh is used for channels 0–3 and I/O port 0DCh is used for channels 4–7.

5.5 PCI DMA

The ICH3 provides support for the PC/PCI DMA protocol. PC/PCI DMA uses dedicated REQUEST and GRANT signals to permit PCI devices to request transfers associated with specific DMA channels. Upon receiving a request and getting control of the PCI bus, ICH3 performs a two-cycle transfer. For example, if data is to be moved from the peripheral to main memory, ICH3 will first read data from the peripheral and then write it to main memory. The location in main memory is the current address registers in the Intel® 8237.

ICH3 supports up to 2 PC/PCI REQ/GNT pairs, REQ[A:B]# and GNT[A:B]#. A 16-bit register is included in the ICH3 Function 0 configuration space at offset 90h. It is divided into seven 2-bit fields that are used to configure the 7 DMA channels.

Each DMA channel can be configured to one of two options:

- LPC DMA
- PC/PCI style DMA using the REQ/GNT signals

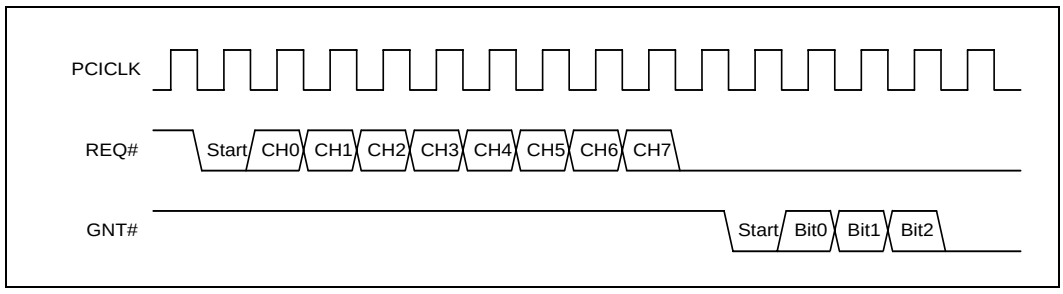
It is not possible for a particular DMA channel to be configured for more than one style of DMA; however, the seven channels can be programmed independently. For example, channel 3 could be set up for PC/PCI and channel 5 set up for LPC DMA.

The ICH3 REQ[A:B]# and GNT[A:B]# can be configured for support of a PC/PCI DMA Expansion agent. The PCI DMA Expansion agent can then provide DMA service or ISA Bus Master service using the ICH3 DMA controller. The REQ#/GNT# pair must follow the PC/PCI serial protocol described below.

5.5.1 PCI DMA Expansion Protocol

The PCI expansion agent must support the PCI expansion Channel Passing Protocol defined in Figure 5-10 for both the REQ# and GNT# pins.

Figure 5-10. DMA Serial Channel Passing Protocol



The requesting device must encode the channel request information as shown above, where CH0–CH7 are one clock active high states representing DMA channel requests 0–7.

ICH3 encodes the granted channel on the GNT# line as shown above, where the bits have the same meaning as shown in Figure 5-10. For example, the sequence [start, bit 0, bit 1, bit 2]=[0,1,0,0] grants DMA channel 1 to the requesting device, and the sequence [start, bit 0, bit 1, bit 2]=[0,0,1,1] grants DMA channel 6 to the requesting device.

All PCI DMA expansion agents must use the channel passing protocol described in Figure 5-10. They must also work as follows:

1. If a PCI DMA expansion agent has more than one request active, it must resend the request serial protocol after one of the requests has been granted the bus and it has completed its transfer. The expansion device should drive its REQ# inactive for two clocks and then transmit the serial channel passing protocol again, even if there are no new requests from the PCI expansion agent to ICH3. For example: If a PCI expansion agent had active requests for DMA Channel 1 and Channel 5, it would pass this information to ICH3 through the expansion channel passing protocol. If after receiving GNT# (assume for CH5) and having the device finish its transfer (device stops driving request to PCI expansion agent) it would then need to re-transmit the expansion channel passing protocol to inform ICH3 that DMA channel 1 was still requesting the bus, even if that was the only request the expansion device had pending.
2. If a PCI DMA expansion agent has a request go inactive before ICH3 asserts GNT#, it must resend the expansion channel passing protocol to update ICH3 with this new request information. For example: If a PCI expansion agent has DMA channel 1 and 2 requests pending it will send them serially to ICH3 using the expansion channel passing protocol. If, however, DMA channel 1 goes inactive into the expansion agent before the expansion agent receives a GNT# from ICH3, the expansion agent MUST pull its REQ# line high for ONE clock and resend the expansion channel passing information with only DMA channel 2 active. Note that ICH3 does not do anything special to catch this case because a DREQ going inactive before a DACK# is received is not allowed in the ISA DMA protocol and, therefore, does not need to work properly in this protocol either. This requirement is needed to be able to support Plug-n-Play ISA devices that toggle DREQ# lines to determine if those lines are free in the system.
3. If a PCI expansion agent has sent its serial request information and receives a new DMA request before receiving GNT#, the agent must resend the serial request with the new request active. For example: If a PCI expansion agent has already passed requests for DMA channel 1 and 2 and sees DREQ 3 active before a GNT is received, the device must pull its REQ# line high for one clock and resend the expansion channel passing information with all three channels active.

The three cases above require the following functionality in the PCI DMA expansion device:

1. Drive REQ# inactive for one clock to signal new request information.
2. Drive REQ# inactive for two clocks to signal that a request that had been granted the bus has gone inactive.
3. The REQ# and GNT# state machines must run independently and concurrently (i.e., a GNT# could be received while in the middle of sending a serial REQ# or a GNT# could be active while REQ# is inactive).

5.5.2 PCI DMA Expansion Cycles

ICH3's support of the PC/PCI DMA Protocol currently consists of four types of cycles: Memory to I/O, I/O to Memory, Verify, and ISA Master cycles. ISA Masters are supported through the use of a DMA channel that has been programmed for cascade mode.

The DMA controller does a two cycle transfer (a load followed by a store) as opposed to the ISA "fly-by" cycle for PC/PCI DMA agents. The memory portion of the cycle generates a PCI memory read or memory write bus cycle, its address representing the selected memory.

The I/O portion of the DMA cycle generates a PCI I/O cycle to one of four I/O addresses (Table 5-10). Note that these cycles must be qualified by an active GNT# signal to the requesting device.

Table 5-10. DMA Cycle vs. I/O Address

DMA Cycle Type	DMA I/O Address	PCI Cycle Type
Normal	00h	I/O Read/Write
Normal TC	04h	I/O Read/Write
Verify	0C0h	I/O Read
Verify TC	0C4h	I/O Read

5.5.3 DMA Addresses

The memory portion of the cycle will generate a PCI memory read or memory write bus cycle, its address representing the selected memory. The I/O portion of the DMA cycle will generate a PCI I/O cycle to one of the four I/O addresses listed in Table 5-10.

5.5.4 DMA Data Generation

The data generated by PC/PCI devices on I/O reads when they have an active GNT# is on the lower two bytes of the PCI AD bus. Table 5-11 lists the PCI pins that the data appears on for 8- and 16-bit channels. Each I/O read results in one memory write and each memory read results in one I/O write. If the I/O device is 8 bit, the ICH3 performs an 8-bit memory write. The ICH3 does not assemble the I/O read into a DWord for writing to memory. Similarly, the ICH3 does not disassemble a DWord read from memory to the I/O device.

Table 5-11. PCI Data Bus vs. DMA I/O port size

PCI DMA I/O Port Size	PCI Data Bus Connection
Byte	AD[7:0]
Word	AD[15:0]

5.5.5 DMA Byte Enable Generation

The byte enables generated by the ICH3 on I/O reads and writes must correspond to the size of the I/O device. Table 5-12 defines the byte enables asserted for 8- and 16-bit DMA cycles.

Table 5-12. DMA I/O Cycle Width vs. BE[3:0]#

BE[3:0]#	Description
1110b	8-bit DMA I/O Cycle: Channels 0–3
1100b	16-bit DMA I/O Cycle: Channels 5–7

NOTE: For verify cycles the value of the Byte Enables (BEs) is a “don’t care”.

5.5.6 DMA Cycle Termination

DMA cycles are terminated when a terminal count is reached in the DMA controller and the channel is not in autoinitialize mode, or when the PC/PCI device deasserts its request. The PC/PCI device must follow explicit rules when deasserting its request, or the ICH3 may not see it in time and run an extra I/O and memory cycle.

The PC/PCI device must deassert its request 7 PCICLKs before it generates TRDY# on the I/O read or write cycle, or the ICH3 is allowed to generate another DMA cycle. For transfers to memory, this means that the memory portion of the cycle will be run without an asserted PC/PCI REQ#.

5.5.7 LPC DMA

DMA on LPC is handled through the use of the LDRQ# lines from peripherals and special encodings on LAD[3:0] from the host. Single, demand, verify, and increment modes are supported on the LPC interface. Channels 0–3 are 8-bit channels. Channels 5–7 are 16-bit channels. Channel 4 is reserved as a generic bus master request.

5.5.8 Asserting DMA Requests

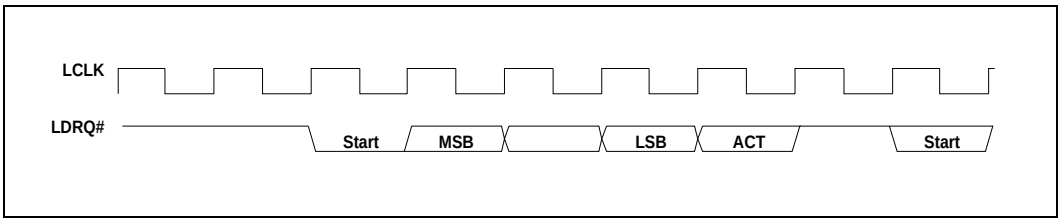
Peripherals that need DMA service encode their requested channel number on the LDRQ# signal. To simplify the protocol, each peripheral on the LPC I/F has its own dedicated LDRQ# signal (they may not be shared between two separate peripherals). The ICH3 has two LDRQ# inputs, allowing at least two devices to support DMA or bus mastering.

LDRQ# is synchronous with LCLK (PCI clock). As shown in Figure 5-11, the peripheral uses the following serial encoding sequence:

- Peripheral starts the sequence by asserting LDRQ# low (start bit). LDRQ# is high during idle conditions.
- The next three bits contain the encoded DMA channel number (MSB first).
- The next bit (ACT) indicates whether the request for the indicated DMA channel is active or inactive. The ACT bit will be a 1 (high) to indicate if it is active and 0 (low) if it is inactive. The case where ACT is low will be rare, and is only used to indicate that a previous request for that channel is being abandoned.
- After the active/inactive indication, the LDRQ# signal must go high for at least 1 clock. After that one clock, the LDRQ# signal can be brought low to the next encoding sequence.

If another DMA channel also needs to request a transfer, another sequence can be sent on LDRQ#. For example, if an encoded request is sent for channel 2 and then channel 3 needs a transfer before the cycle for channel 2 is run on the interface, the peripheral can send the encoded request for channel 3. This allows multiple DMA agents behind an I/O device to request use of the LPC interface, and the I/O device does not need to self-arbitrate before sending the message.

Figure 5-11. DMA Request Assertion Through LDRQ#



5.5.9 Abandoning DMA Requests

DMA Requests can be deasserted in two fashions: on error conditions by sending an LDRQ# message with the “ACT” bit set to “0,” or normally through a SYNC field during the DMA transfer. This section describes boundary conditions where the DMA request needs to be removed prior to a data transfer.

There may be some special cases where the peripheral desires to abandon a DMA transfer. The most likely case of this occurring is due to a floppy disk controller which has overrun or underrun its FIFO, or software stopping a device prematurely.

In these cases, the peripheral wishes to stop further DMA activity. It may do so by sending an LDRQ# message with the ACT bit as “0.” However, since the DMA request was seen by the ICH3, there is no guarantee that the cycle has not been granted and will shortly run on LPC. Therefore, peripherals must take into account that a DMA cycle may still occur. The peripheral can choose not to respond to this cycle, in which case the host will abort it, or it can choose to complete the cycle normally with any random data.

This method of DMA deassertion should be prevented whenever possible, to limit boundary conditions both on the ICH3 and the peripheral.

5.5.10 General Flow of DMA Transfers

Arbitration for DMA channels is performed through the 8237 within the host. Once the host has won arbitration on behalf of a DMA channel assigned to LPC, it asserts LFRAME# on the LPC I/F and begins the DMA transfer. The general flow for a basic DMA transfer is as follows:

1. ICH3 starts transfer by asserting 0000b on LAD[3:0] with LFRAME# asserted.
2. ICH3 asserts 'cycle type' of DMA, direction based on DMA transfer direction.
3. ICH3 asserts channel number and, if applicable, terminal count.
4. ICH3 indicates the size of the transfer: 8 or 16 bits.
5. If a DMA read…
   - The ICH3 drives the first 8 bits of data and turns the bus around.
   - The peripheral acknowledges the data with a valid SYNC.
   - If a 16-bit transfer, the process is repeated for the next 8 bits.
6. If a DMA write…
   - The ICH3 turns the bus around and waits for data.
   - The peripheral indicates data ready through SYNC and transfers the first byte.
   - If a 16-bit transfer, the peripheral indicates data ready and transfers the next byte.
7. The peripheral turns around the bus.

5.5.11 Terminal Count

Terminal count is communicated through LAD[3] on the same clock that DMA channel is communicated on LAD[2:0]. This field is the CHANNEL field. Terminal count indicates the last byte of transfer, based on the size of the transfer.

For example, on an 8-bit transfer size (SIZE field is 00b), if the TC bit is set, then this is the last byte. On a 16-bit transfer (SIZE field is 01b), if the TC bit is set, then the second byte is the last byte. The peripheral, therefore, must internalize the TC bit when the CHANNEL field is communicated, and only signal TC when the last byte of that transfer size has been transferred.

5.5.12 Verify Mode

Verify mode is supported on the LPC interface. A verify transfer to the peripheral is similar to a DMA write, where the peripheral is transferring data to main memory. The indication from the host is the same as a DMA write, so the peripheral will be driving data onto the LPC interface. However, the host will not transfer this data into main memory.

5.5.13 DMA Request Deassertion

An end of transfer is communicated to the ICH3 through a special SYNC field transmitted by the peripheral. An LPC device must not attempt to signal the end of a transfer by deasserting LDREQ#. If a DMA transfer is several bytes, such as a transfer from a demand mode device, the ICH3 needs to know when to deassert the DMA request based on the data currently being transferred.

The DMA agent uses a SYNC encoding on each byte of data being transferred, which indicates to the ICH3 whether this is the last byte of transfer or if more bytes are requested. To indicate the last byte of transfer, the peripheral uses a SYNC value of 0000b (ready with no error), or 1010b (ready with error). These encodings tell the ICH3 that this is the last piece of data transferred on a DMA read (ICH3 to peripheral), or the byte which follows is the last piece of data transferred on a DMA write (peripheral to ICH3).

When the ICH3 sees one of these two encodings, it ends the DMA transfer after this byte and deasserts the DMA request to the 8237. Therefore, if the ICH3 indicated a 16-bit transfer, the peripheral can end the transfer after one byte by indicating a SYNC value of 0000b or 1010b. The ICH3 will not attempt to transfer the second byte, and will deassert the DMA request internally.

If the peripheral indicates a 0000b or 1010b SYNC pattern on the last byte of the indicated size, then the ICH3 will only deassert the DMA request to the 8237 since it does not need to end the transfer.

If the peripheral wishes to keep the DMA request active, then it uses a SYNC value of 1001b (ready plus more data). This tells the 8237 that more data bytes are requested after the current byte has been transferred, so the ICH3 will keep the DMA request active to the 8237. Therefore, on an 8-bit transfer size, if the peripheral indicates a SYNC value of 1001b to the ICH3, the data will be transferred and the DMA request will remain active to the 8237. At a later time, the ICH3 will then come back with another START–CYCTYPE–CHANNEL–SIZE etc. combination to initiate another transfer to the peripheral.

The peripheral must not assume that the next START indication from the ICH3 is another grant to the peripheral if it had indicated a SYNC value of 1001b. On a single mode DMA device, the 8237 will re-arbitrate after every transfer. Only demand mode DMA devices can be guaranteed that they will receive the next START indication from the ICH3.

Note: Indicating a 0000b or 1010b encoding on the SYNC field of an odd byte of a 16-bit channel (first byte of a 16-bit transfer) is an error condition.

Note: The host will stop the transfer on the LPC bus as indicated, fill the upper byte with random data on DMA writes (peripheral to memory), and indicate to the 8237 that the DMA transfer occurred, incrementing the 8237's address and decrementing its byte count.

5.5.14 SYNC field / LDRQ# Rules

Since DMA transfers on LPC are requested through an LDRQ# assertion message, and are ended through a SYNC field during the DMA transfer, the peripheral must obey the following rule when initiating back-to-back transfers from a DMA channel.

The peripheral must not assert another message for eight LCLKs after a deassertion is indicated through the SYNC field. This is needed to allow the 8237, which typically runs off a much slower internal clock, to see a message deasserted before it is re-asserted so that it can arbitrate to the next agent.

Under default operation, the host will only perform 8-bit transfers on 8-bit channels and 16-bit transfers on 16-bit channels.

The method by which this communication between host and peripheral through system BIOS is performed is beyond the scope of this specification. Since the LPC host and LPC peripheral are motherboard devices, no “plug-n-play” registry is required.

The peripheral must not assume that the host will be able to perform transfer sizes that are larger than the size allowed for the DMA channel, and be willing to accept a SIZE field that is smaller than what it may currently have buffered.

To that end, it is recommended that future devices which may appear on the LPC bus, which require higher bandwidth than 8-bit or 16-bit DMA allow, do so with a bus mastering interface and not rely on the 8237.

5.6 Intel® 8254 Timers (D31:F0)

The ICH3 contains three counters which have fixed uses. All registers and functions associated with the 8254 timers are in the core well. The 8254 unit is clocked by a 14.31818 MHz clock.

5.6.1 Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

5.6.2 Counter 1, Refresh Request Signal

This counter provides the refresh request signal and is typically programmed for Mode 2 operation. The counter negates refresh request for one counter period (838 ns) during each count cycle. The initial count value is loaded one counter period after being written to the counter I/O address. The counter initially asserts refresh request, and negates it for 1 counter period when the count value reaches 1. The counter then asserts refresh request and continues counting from the initial count value.

5.6.3 Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to port 061h (see NMI Status and Control ports).

5.6.4 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (as required by Control Word bits 5, 4) of the 16-bit counter.
4. Repeat with other counters

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting will be affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The control word register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command.** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command.** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command.** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 5-13 lists the six operating modes for the interval counters.

Table 5-13. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware retriggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, etc.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

5.6.5 Reading from the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, Counter Latch command, and the Read-Back command. Each is explained below.

With the simple read operation and Counter Latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

5.6.5.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through port 40h (counter 0), 41h (counter 1), or 42h (counter 2).

Note: Performing a direct read from the counter will not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of counter 2, the count can be stopped by writing to the GATE bit in port 61h.

5.6.5.2 Counter Latch Command

The Counter Latch command, written to port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's count register as was programmed by the control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read will be the count at the time the first Counter Latch command was issued.

5.6.5.3 Read Back Command

The Read Back command, written to port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back Commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back Commands. If multiple count and/or status Read Back Commands are issued to the same counters without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter will return the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, return the latched count. Subsequent reads return unlatched count.

5.7 Intel® 8259 Interrupt Controllers (PIC) (D31:F0)

The ICH3 incorporates the functionality of two 8259 interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts are: system timer, keyboard controller, serial ports, parallel ports, floppy disk, IDE, mouse, and DMA channels. In addition, this interrupt controller can support the PCI based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line. Each 8259 core supports 8 interrupts, numbered 0–7. Table 5-14 shows how the cores are connected.

Table 5-14. Interrupt Controller Core Connections

Intel® 8259	Intel® 8259 Input	Typical Interrupt Source	Connected Pin / Function
Master	0	Internal	Internal Timer / Counter 0 output / MMT #0
	1	Keyboard	IRQ1 via SERIRQ
	2	Internal	Slave Controller INTR output
	3	Serial Port A	IRQ3 via SERIRQ
	4	Serial Port B	IRQ4 via SERIRQ
	5	Parallel Port / Generic	IRQ5 via SERIRQ
	6	Floppy Disk	IRQ6 via SERIRQ
	7	Parallel Port / Generic	IRQ7 via SERIRQ
Slave	0	Internal Real Time Clock	Internal RTC / MMT #1
	1	Generic	IRQ9 via SERIRQ
	2	Generic	IRQ10 via SERIRQ
	3	Generic	IRQ11 via SERIRQ
	4	PS/2 Mouse	IRQ12 via SERIRQ
	5	Internal	State Machine output based on processor FERR# assertion.
	6	Primary IDE cable	IRQ14 from input signal (primary IDE in legacy mode only) or via SERIRQ
	7	Secondary IDE Cable	IRQ15 from input signal (secondary IDE in legacy mode only) or via SERIRQ

The ICH3 cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the ICH3 PIC.

Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8#, and IRQ13.

Note that previous PIIXn devices internally latched IRQ12 and IRQ1 and required a port 60h read to clear the latch. The ICH3 can be programmed to latch IRQ12 or IRQ1 (see bit 11 and bit 12 in the General Control Register, D31:F0, offset D0h).

5.7.1 Interrupt Handling

5.7.1.1 Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 5-15 defines the IRR, ISR and IMR.

Table 5-15. Interrupt Status Registers

Bit	Description
IRR	**Interrupt Request Register.** This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode. This bit is set whether or not the interrupt is masked. However, a masked interrupt will not generate INTR.
ISR	**Interrupt Service Register.** This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
IMR	**Interrupt Mask Register.** This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.

5.7.1.2 Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle which is translated by the host bridge into a PCI Interrupt Acknowledge Cycle to the ICH3. The PIC translates this command into two internal INTA# pulses expected by the 8259 cores. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave will sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon bits [7:3] of the corresponding ICW2 Register, combined with three bits representing the interrupt within that controller.

Table 5-16. Content of Interrupt Vector Byte

Master,Slave Interrupt	Bits [7:3]	Bits [2:0]
IRQ7,15	ICW2[7:3]	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

5.7.1.3 Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle. The cycle is translated into a PCI interrupt acknowledge cycle by the host bridge. This command is broadcast over PCI by the ICH3.
4. Upon observing its own interrupt acknowledge cycle on PCI, the ICH3 converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal 3-bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC will return vector 7 from the master controller.
7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

5.7.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the ICH3, this is a four byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.

ICW1

An I/O write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the ICH3 PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
2. The Interrupt Mask Register is cleared.
3. IRQ7 input is assigned priority 7.
4. The slave mode address is set to 7.
5. Special mask mode is cleared and Status Read is set to IRR.

ICW2

The second write in the sequence, ICW2, is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

ICW3

The third write in the sequence, ICW3, has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the ICH3, IRQ2 is used. Therefore, bit 2 of ICW3 on the master controller is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

ICW4

The final write in the sequence, ICW4, must be programmed both controllers. At the very least, bit 0 must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

5.7.3 Operation Command Words (OCW)

These command words reprogram the interrupt controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines.
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 is sets up ISR/IRR reads, enables/disables the special mask mode SMM, and enables/disables polled interrupt mode.

5.7.4 Modes of Operation

5.7.4.1 Fully Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate another interrupt.

Interrupt priorities can be changed in the rotating priority mode.

5.7.4.2 Special Fully Nested Mode

This mode will be used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully nested mode will be programmed to the master controller. This mode is similar to the fully nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave will be recognized by the master and will initiate interrupts to the processor. In the normal nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.

5.7.4.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt will have to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2; the Rotation on Non-Specific EOI command (R=1, SL=0, EOI=1) and the rotate in automatic EOI mode which is set by (R=1, SL=0, EOI=0).

5.7.4.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 will be the highest priority device. The Set Priority command is issued in OCW2 to accomplish this, where: R=1, SL=1, and LO–L2 is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R=1, SL=1, EOI=1 and LO-L2=IRQ level to receive bottom priority.

5.7.4.5 Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read will contain a 1 in bit 7 if there is an interrupt, and the binary code of the highest priority level in bits 2:0.

5.7.4.6 Cascade Mode

The PIC in the ICH3 has one master 8259 and one slave 8259 cascaded onto the master through IRQ2. This configuration can handle up to 15 separate priority levels. The master controls the slaves through a 3-bit internal bus. In the ICH3, when the master drives 010b on this bus, the slave controller takes responsibility for returning the interrupt vector. An EOI command must be issued twice: once for the master and once for the slave.

5.7.4.7 Edge and Level Triggered Mode

In ISA systems this mode is programmed using bit 3 in ICW1, which sets level or edge for the entire controller. In the ICH3, this bit is disabled and a new register for edge and level triggered mode selection, per interrupt input, is included. These are the edge/level control registers (ELCR1 and ELCR2).

If an ELCR bit is 0, an interrupt request will be recognized by a low to high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector will be returned.

5.7.4.8 End of Interrupt Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when AEOI bit in ICW4 is set to 1.

5.7.4.9 Normal End of Interrupt

In Normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the ICH3, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI. An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

5.7.4.10 Automatic End of Interrupt Mode

In this mode, the PIC will automatically perform a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

5.7.5 Masking Interrupts

5.7.5.1 Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller will mask all requests for service from the slave controller.

5.7.5.2 Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The special mask mode enables all interrupts not masked by a bit set in the mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the mask register with the appropriate pattern. The special mask mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

5.7.6 Steering PCI Interrupts

The ICH3 can be programmed to allow PIRQA#–PIRQH# to be internally routed to interrupts 3–7, 9-12, 14 or 15. The assignment is programmable through the PIRQx Route Control Registers, located at 60–63h and 68–6Bh in function 0. One or more PIRQx# lines can be routed to the same IRQx input. If interrupt steering is not required, the route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive to allow multiple interrupts on a PCI Board to share a single line across the connector. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level-sensitive mode. The ICH3 internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an ISA device (through SERIRQ). However, active low non-ISA interrupts can share their interrupt with PCI interrupts.

Internal sources of the PIRQs, including SCI and TCO interrupts, cause the external PIRQ to be asserted. The ICH3 receives the PIRQ input, like all of the other external sources, and routes it accordingly.

5.8 Advanced Interrupt Controller (APIC) (D31:F0)

In addition to the standard ISA compatible interrupt controller (PIC) described in the previous chapter, the ICH3 incorporates the Advanced Programmable Interrupt Controller (APIC). While the standard interrupt controller is intended for use in a uni-processor system, APIC can be used in either a uni-processor or multi-processor system.

5.8.1 Interrupt Handling

The I/O APIC handles interrupts very differently than the 8259. Briefly, these differences are:

- **Method of Interrupt Transmission.** The I/O APIC transmits interrupts through a three wire bus, and interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.
- **Interrupt Priority.** The priority of interrupts in the I/O APIC is independent of the interrupt number. For example, interrupt 10 can be given a higher priority than interrupt 3.
- **More Interrupts.** The I/O APIC in the ICH3 supports a total of 24 interrupts.
- **Multiple Interrupt Controllers.** The I/O APIC interrupt transmission protocol has an arbitration phase, which allows for multiple I/O APICs in the system with their own interrupt vectors. The ICH3 I/O APIC must arbitrate for the APIC bus before transmitting its interrupt message.

5.8.2 Interrupt Mapping

The I/O APIC within the ICH3 supports 24 APIC interrupts. Each interrupt has its own unique vector assigned by software. The interrupt vectors are mapped as follows, and match “Config 6” of the Multi-processor specification.

Table 5-17. APIC Interrupt Mapping

IRQ #	Via SERIRQ	Direct from pin	Via PCI message	Internal Modules
0	No	No	No	Cascade from 8259 #1
1	Yes	No	Yes	
2	No	No	No	8254 Counter 0
3	Yes	No	Yes	
4	Yes	No	Yes	
5	Yes	No	Yes	
6	Yes	No	Yes	
7	Yes	No	Yes	
8	No	No	No	RTC
9	Yes	No	Yes	Option for SCI, TCO
10	Yes	No	Yes	Option for SCI, TCO
11	Yes	No	Yes	Option for SCI, TCO
12	Yes	No	Yes	
13	No	No	No	FERR# logic
14	Yes	Yes	Yes	
15	Yes	Yes[1]	Yes	
16	PIRQ[A]#	PIRQ[A]#	No	USB 1.1 Controller #1
17	PIRQ[B]#	PIRQ[B]#	No	AC ’97 Audio, Modem, option for SMBus
18	PIRQ[C]#	PIRQ[C]#	No	USB 1.1 Controller #3, Native IDE
19	PIRQ[D]#	PIRQ[D]#	No	USB 1.1 Controller #2
20	N/A	PIRQ[E]#	Yes	LAN, option for SCI, TCO
21	N/A	PIRQ[F]#	Yes	Option for SCI, TCO
22	N/A	PIRQ[G]#	Yes	Option for SCI, TCO
23	N/A	PIRQ[H]#	Yes	Option for SCI, TCO

Note: IRQ 14 and 15 can only be driven directly from the pins when in legacy IDE mode.

Note: When programming the polarity of internal interrupt sources on the APIC, interrupts 0 through 15 receive active-high internal interrupt sources, while interrupts 16 through 23 receive active-low internal interrupt sources.

5.8.3 APIC Bus Functional Description

5.8.3.1 Physical Characteristics of APIC

The APIC bus is a 3-wire synchronous bus connecting all I/O and local APICs. Two of these wires are used for data transmission, and one wire is a clock. For bus arbitration, the APIC uses only one of the data wires. The bus is logically a wire-OR and electrically an open-drain connection providing for both bus use arbitration and arbitration for lowest priority. The APIC bus speed can run from 16.67 MHz to 33 MHz.

5.8.3.2 APIC Bus Arbitration

The I/O APIC uses one wire arbitration to win bus ownership. A rotating priority scheme is used for APIC bus arbitration. The winner of the arbitration becomes the lowest priority agent and assumes an arbitration ID of 0. All other agents, except the agent whose arbitration ID is 15, increment their Arbitration IDs by one. The agent whose ID was 15 will take the winner's arbitration ID and will increment it by one. Arbitration IDs are changed only for messages that are transmitted successfully (except for the Low Priority messages). A message is transmitted successfully if no CS error or acceptance error was reported for that message.

An APIC agent can use two different priority schemes: Normal or EOI. EOI has the highest priority. EOI priority is used to send EOI messages for level interrupts from a local APIC to an I/O APIC. When an agent requests the bus with EOI priority, all other agents requesting the bus with normal priorities will back off.

When ICH3 detects a bus idle condition on the APIC Bus, and it has an interrupt to send over the APIC bus, it drives a start cycle to begin arbitration, by driving bit 0 to a 0 on an APICCLK rising edge. It then samples bit 1. If bit 1 was a 0, then a local APIC started arbitration for an EOI message on the same clock edge that the ICH3 started arbitration. The ICH3 has thus lost arbitration and will stop driving the APIC bus.

If the ICH3 did not see an EOI message start, it will start transferring its arbitration ID, located in bits [27:24] of its Arbitration ID Register (ARBID). Starting in Cycle 2, through Cycle 5, it will tri-state bit 0, and drive bit 1 to a 0 if ARBID[27] is a 1. If ARBID[27] is a 0, it will also tri-state bit 1. At the end of each cycle, the ICH3 will sample the state of Bit 1 on the APIC bus. If the ICH3 did not drive bit 1 (ARBID[27] = 0), and it samples a 0, then another APIC agent started arbitration for the APIC bus at the same time as the ICH3, and it has higher priority. The ICH3 will stop driving the APIC bus. Table 5-18 describes the arbitration cycles.

Table 5-18. Arbitration Cycles

Cycle	Bit 1	Bit 0	Comment
1	EOI	0	Bit 1 = 1: Normal, Bit 1 = 0: EOI
2	NOT (**ARBID[27]**)	1	Arbitration ID. If ICH3 samples a different value than it sent, it lost arbitration.
3	NOT (**ARBID[26]**)	1	
4	NOT (**ARBID[25]**)	1	
5	NOT (**ARBID[24]**)	1	

5.8.3.3 Bus Message Formats

After bus arbitration, the winner is granted exclusive use of the bus and will drive its message. APIC messages come in four formats, determined by the delivery mode bits. These four messages are of different length, and are known by all APICs on the bus through the transmission of the delivery mode bits:

Table 5-19. APIC Message Formats

Message	# of Cycles	Delivery Mode Bits	Comments
EOI	14	xxx	End of Interrupt transmission from Local APIC to I/O APIC on Level interrupts. EOI is known by the EOI bit at the start of arbitration
Short	21	001, 010, 100, 101, 111	I/O APIC delivery on Fixed, NMI, SMI, Reset, ExtINT, and Lowest Priority with focus processor messages
Lowest Priority	33	001	Transmission of Lowest Priority interrupts when the status field indicates that the processor does not have focus
Remote Read	39	011	Message from one Local APIC to another to read registers.

EOI Message for Level Triggered Interrupts

EOI messages are used by local APICs to send an EOI cycle occurring for a level triggered interrupt to an I/O APIC. This message is needed so that the I/O APIC can differentiate between a new interrupt on the interrupt line versus the same interrupt on the interrupt line. The target of the EOI is given by the local APIC through the transmission of the priority vector (V7 through V0) of the interrupt. Upon receiving this message, the I/O APIC resets the Remote IRR bit for that interrupt. If the interrupt signal is still active after the IRR bit is reset, the I/O APIC will treat it as a new interrupt.

Table 5-20. EOI Message

Cycle	Bit 1	Bit 0	Comments
1	0	0	EOI message
2–5	ARBID	1	Arbitration ID
6	NOT(V7)	NOT(V6)	Interrupt vector bits V7–V0 from redirection table register
7	NOT(V5)	NOT(V4)	
8	NOT(V3)	NOT(V2)	
9	NOT(V1)	NOT(V0)	
10	NOT(C1)	NOT(C0)	Check Sum from Cycles 6–9
11	1	1	Postamble
12	NOT(A)	NOT(A)	Status Cycle 0
13	NOT(A1)	NOT(A1)	Status Cycle 1
14	1	1	Idle

Short Message

Short messages are used for the delivery of Fixed, NMI, SMI, Reset, ExtINT and Lowest Priority with Focus processor interrupts. The delivery mode bits (M2–M0) specify the message. All short messages take 21 cycles including the idle cycle.

Table 5-21. Short Message

Cycle	Bit 1	Bit 0	Comments
1	1	0	Normal Arbitration
2–5	ARBID	1	Arbitration ID
6	NOT(DM)	NOT(M2)	DM[1] = Destination Mode from bit 11 of the redirection table register
7	NOT(M1)	NOT(M0)	M2-M0 = Delivery Mode from bits 10:8 of the redirection table register
8	NOT(L)	NOT(TM)	L = Level, TM = Trigger Mode
9	NOT(V7)	NOT(V6)	Interrupt vector bits V7–V0 from redirection table register
10	NOT(V5)	NOT(V4)	
11	NOT(V3)	NOT(V2)	
12	NOT(V1)	NOT(V0)	
13	NOT(D7)	NOT(D6)	Destination field from bits 63:56 of redirection table register[1]
14	NOT(D5)	NOT(D4)	
15	NOT(D3)	NOT(D2)	
16	NOT(D1)	NOT(D0)	
17	NOT(C1)	NOT(C0)	Checksum for Cycles 6–16[2]
18	1	1	Postamble[3]
19	NOT(A)	NOT(A)	Status Cycle 0. See Table 5-22.
20	NOT(A1)	NOT(A1)	Status Cycle 1. See Table 5-22.
21	1	1	Idle

NOTES:

1. If DM is 0 (physical mode), then cycles 15 and 16 are the APIC ID and cycles 13 and 14 are sent as 1. If DM is 1 (logical mode), then cycles 13 through 16 are the 8-bit Destination field. The interpretation of the logical mode 8-bit Destination field is performed by the local units using the destination format register. Shorthands of “all-incl-self” and “all-excl-self” both use physical destination mode and a destination field containing APIC ID value of all ones. The sending APIC knows whether it should (incl) or should not (excl) respond to its own message.
2. The checksum field is the cumulative add (mod 4) of all data bits (DM, M0-3, L, TM, V0-7,D0-7). The APIC driving the message provides this checksum. This, in essence, is the lower two bits of an adder at the end of the message.
3. This cycle allows all APICs to perform various internal computations based on the information contained in the received message. One of the computations takes the checksum of the data received in cycles 6 through 16 and compares it with the value in cycle 18. If any APIC computes a different checksum than the one passed in cycle 17, then that APIC will signal an error on the APIC bus (“00”) in cycle 19. If this happens, all APICs assume the message was never sent and the sender must try sending the message again, which includes re-arbitrating for the APIC bus. In lowest priority delivery when the interrupt has a focus processor, the focus processor signals this by driving a “01” during cycle 19. This indicates to all the other APICs that the interrupt has been accepted, the arbitration is preempted, and short message format is used. Cycle 19 and 20 indicates the status of the message (i.e., accepted, check sum error, retry or error). Table 5-22 shows the status signal combinations and their meanings for all delivery modes.

Table 5-22. APIC Bus Status Cycle Definition

Delivery Mode	A	Comments	A1	Comments
Fixed, EOI	11	Checksum OK	1x	Error
			01	Accepted
			00	Retry
	10	Error	xx	
	01	Error	xx	
	00	Checksum Error	xx	
NMI, SMM, Reset, ExtINT	11	Checksum OK	1x	Error
			01	Accepted
			00	Error
	10	Error	xx	
	01	Error	xx	
	00	Checksum Error	xx	
Lowest Priority	11	Checksum OK: No Focus Processor	1x	Error
			01	End and Retry
			00	Go for Low Priority Arbitration
	10	Error	xx	
	01	Checksum OK: Focus Processor	xx	
	00	Checksum Error	xx	
Remote Read	11	Checksum OK	xx	
	10	Error	xx	
	01	Error	xx	
	00	Checksum Error	xx	

Lowest Priority without Focus Processor (FP) Message

This message format is used to deliver an interrupt in the lowest priority mode in which it does not have a Focus Process. Cycles 1 through 21 for this message is same as for the short message discussed above. Status cycle 19 identifies if there is a Focus processor (10) and a status value of 11 in cycle 20 indicates the need for lowest priority arbitration.

Table 5-23. Lowest Priority Message (Without Focus Processor)

Cycle	Bit 1	Bit 0	Comments
1	1	0	Normal Arbitration
2–5	ARBID	1	Arbitration ID
6	NOT(DM)	NOT(M2)	DM = Destination Mode from bit 11 of the redirection table register
7	NOT(M1)	NOT(M0)	M2-M0 = Delivery Mode from bits 10:8 of the redirection table register
8	NOT(L)	NOT(TM)	L = Level, TM = Trigger Mode
9	NOT(V7)	NOT(V6)	Interrupt vector bits V7–V0 from redirection table register
10	NOT(V5)	NOT(V4)	
11	NOT(V3)	NOT(V2)	
12	NOT(V1)	NOT(V0)	
13	NOT(D7)	NOT(D6)	Destination field from bits 63:56 of redirection table register
14	NOT(D5)	NOT(D4)	
15	NOT(D3)	NOT(D2)	
16	NOT(D1)	NOT(D0)	
17	NOT(C1)	NOT(C0)	Checksum for Cycles 6–16
18	1	1	Postamble
19	NOT(A)	NOT(A)	Status Cycle 0.
20	NOT(A1)	NOT(A1)	Status Cycle 1.
21	P7	1	Inverted Processor Priority P7–P0
22	P6	1	
23	P5	1	
24	P4	1	
25	P3	1	
26	P2	1	
27	P1	1	
28	P0	1	
29	ArbID3	1	
30	ArbID2	1	
31	ArbID1	1	
32	ArbID0	1	
33	S	S	Status
34	1	1	Idle

NOTES:
1. Cycle 21 through 28 are used to arbitrate for the lowest priority processor. The processor that takes part in the arbitration drives the processor priority on the bus. Only the local APICs that have “free interrupt slots” will participate in the lowest priority arbitration.
2. Cycles 29 through 32 are used to break tie in case two more processors have lowest priority. The bus arbitration ID's are used to break the tie.

Remote Read Message

Remote read message is used when a local APIC wishes to read the register in another local APIC. The I/O APIC in the ICH3 neither generates or responds to this cycle. The message format is same as short message for the first 21 cycles.

Table 5-24. Remote Read Message

Cycle	Bit 1	Bit 0	Comments
1	1	0	Normal Arbitration
2–5	ARBID	1	Arbitration ID
6	NOT(DM)	NOT(M2)	DM = Destination Mode from bit 11 of the redirection table register
7	NOT(M1)	NOT(M0)	M2–M0 = Delivery Mode from bits 10:8 of the redirection table register
8	NOT(L)	NOT(TM)	L = Level, TM = Trigger Mode
9	NOT(V7)	NOT(V6)	Interrupt vector bits V7–V0 from redirection table register
10	NOT(V5)	NOT(V4)	
11	NOT(V3)	NOT(V2)	
12	NOT(V1)	NOT(V0)	
13	NOT(D7)	NOT(D6)	Destination field from bits 63:56 of redirection table register
14	NOT(D5)	NOT(D4)	
15	NOT(D3)	NOT(D2)	
16	NOT(D1)	NOT(D0)	
17	NOT(C1)	NOT(C0)	Checksum for Cycles 6–16
18	1	1	Postamble
19	NOT(A)	NOT(A)	Status Cycle 0.
20	NOT(A1)	NOT(A1)	Status Cycle 1.
21	d31	d30	Remote register data 31–0
22	d29	d28	
23	d27	d26	
24	d25	d24	
25	d23	d22	
26	d21	d20	
27	d19	d18	
28	d17	d16	
29	d15	d14	
30	d13	d12	
31	d11	d10	
32	d09	d08	
33	d07	d06	
34	d05	d04	
35	d03	d02	
36	d01	d00	
37	S	S	Data Status: 00 = valid, 11 = invalid
38	C	C	Check Sum for data d31–d00
39	1	1	Idle

NOTE: Cycle 21 through 36 contain the remote register data. The status information in cycle 37 specifies if the data is good or not. Remote read cycle is always successful (although the data may be valid or invalid) in that it is never retried. The reason for this is that Remote Read is a debug feature, and a “hung” remote APIC that is unable to respond should not cause the debugger to hang.

5.8.4 PCI Message-Based Interrupts

5.8.4.1 Theory of Operation

The following scheme is only supported when the internal I/O(x) APIC is used (rather than just the 8259). The ICH3 supports the new method for PCI devices to deliver interrupts as write cycles, rather than using the traditional PIRQ[A:D] signals. Essentially, the PCI devices are given a write path directly to a register that will cause the desired interrupt. This mode is only supported when the ICH3's internal I/O APIC is enabled. Upon recognizing the write from the peripheral, the ICH3 will send the interrupt message to the processor using the I/O APIC's serial bus.

The interrupts associated with the PCI Message-based interrupt method must be set up for edge triggered mode, rather than level triggered, since the peripheral only does the write to indicate the edge.

The following sequence is used:

1. During PCI PnP, the PCI peripheral is first programmed with an address (MESSAGE_ADDRESS) and data value (MESSAGE_DATA) that will be used for the interrupt message delivery. For the ICH3, the MESSAGE_ADDRESS is the IRQ Pin assertion register, which is mapped to memory location: FEC0_0020h.
2. To cause the interrupt, the PCI peripheral requests the PCI bus and when granted, writes the MESSAGE_DATA value to the location indicated by the MESSAGE_ADDRESS. The MESSAGE_DATA value indicates which interrupt occurred. This MESSAGE_DATA value is a binary encoded. For example, to indicate that interrupt 7 should go active, the peripheral will write a binary value of 0000111. The MESSAGE_DATA will be a 32-bit value, although only the lower 5 bits are used.
3. If the PRQ bit in the APIC Version Register is set, the ICH3 positively decodes the cycles (as a slave) in Medium time.
4. The ICH3 decodes the binary value written to MESSAGE_ADDRESS and sets the appropriate IRR bit in the internal I/O APIC. The corresponding interrupt must be set up for edge-triggered interrupts. The ICH3 supports interrupts 00h through 23h. Binary values outside this range will not cause any action.
5. After sending the interrupt message to the processor, the ICH3 will automatically clear the interrupt.

Because they are edge triggered, the interrupts that are allocated to the PCI bus for this scheme may not be shared with any other interrupt (e.g., the standard PCI PIRQ[A:D], those received via SERIRQ#, or the internal level-triggered interrupts such as SCI or TCO).

The ICH3 ignores interrupt messages sent by PCI masters that attempt to use IRQ0, 2, 8, or 13.

5.8.4.2 Registers and Bits Associated with PCI Interrupt Delivery

Capabilities Indication

The capability to support PCI interrupt delivery will be indicated via ACPI configuration techniques. This involves the BIOS creating a data structure that gets reported to the ACPI configuration software. The OS reads the PRQ bit in the APIC Version Register to see if the ICH3 is capable of support PCI-based interrupt messages. As a precaution, the PRQ bit will not be set if the XAPIC_EN bit is not set.

Interrupt Message Register

The PCI devices will all write their message into the IRQ pin assertion register, which is a memory-mapped register located at the APIC base memory location + 20h.

5.8.5 Processor System Bus Interrupt Delivery

5.8.5.1 Theory of Operation

For processors that support Processor System Bus interrupt delivery, the ICH3 has an option to let the integrated I/O APIC behave as an I/O (x) APIC. In this case, it will deliver interrupt messages to the processor in a parallel manner, rather than using the I/O APIC serial scheme. The ICH3 is intended to be compatible with the I/O (x) APIC specification, Rev 1.1

This is done by the ICH3 writing (via the Hub Interface) to a memory location that is snooped by the processor(s). The processor(s) snoop the cycle to know which interrupt goes active.

The processor enables the mode by setting the I/O APIC Enable (APIC_EN) bit and by setting the DT bit in the I/O APIC ID Register.

The following sequence is used:

1. When the ICH3 detects an interrupt event (active edge for edge-triggered mode or a change for level-triggered mode), it sets or resets the internal IRR bit associated with that interrupt.
2. Internally, the ICH3 requests to use the bus in a way that automatically flushes upstream buffers. This can be internally implemented similar to a DMA device request.
3. The ICH3 then delivers the message by performing a write cycle to the appropriate address with the appropriate data. The address and data formats are described below in Section 5.8.5.5.

Note: Processor System Bus Interrupt Delivery compatibility with processor clock control depends on the processor, not the ICH3.

5.8.5.2 Edge-Triggered Operation

In this case, the “Assert Message” is sent when there is an inactive-to-active edge on the interrupt.

5.8.5.3 Level-Triggered Operation

In this case, the “Assert Message” is sent when there is an inactive-to-active edge on the interrupt. If after the EOI the interrupt is still active, then another “Assert Message” is sent to indicate that the interrupt is still active.

5.8.5.4 Registers Associated with Processor System Bus Interrupt Delivery

Capabilities Indication

The capability to support Processor System Bus interrupt delivery will be indicated via ACPI configuration techniques. This involves the BIOS creating a data structure that gets reported to the ACPI configuration software.

DT bit in the Boot Configuration Register

This enables the ICH3 to deliver interrupts as memory writes. This bit is ignored if the APIC mode is not enabled.

5.8.5.5 Interrupt Message Format

The ICH3 writes the message to PCI (and to the Host Controller) as a 32-bit memory write cycle. It uses the formats shown in Table 5-25 and Table 5-26 for the Address and Data.

The local APIC (in the processor) has a delivery mode option to interpret Processor System Bus messages as an SMI in which case the processor treats the incoming interrupt as an SMI instead of as an interrupt. This does not mean that the ICH3 has any way to have an SMI source from ICH3 power management logic cause the IOAPIC to send an SMI message (there is no way to do this). The ICH3's IOAPIC can only send interrupts due to interrupts which do not include SMI, NMI or INIT. This means that in IA32/IA64 based platforms, Processor System Bus interrupt message format delivery modes 010 (SMI/PMI), 100 (NMI), and 101 (INIT) as indicated in this section, must not be used and is not supported. Only the hardware pin connection is supported by the ICH3.

Table 5-25. Interrupt Message Address Format

Bit	Description
31:20	Will always be FEEh
19:12	**Destination ID:** This will be the same as bits 63:56 of the I/O Redirection Table entry for the interrupt associated with this message.
11:4	RESERVED (will always be 0)
3	**Redirection Hint:** This bit is used by the processor host bridge to allow the interrupt message to be redirected. 0 = The message will be delivered to the agent (processor) listed in bits 19:12. 1 = The message will be delivered to an agent with a lower interrupt priority This can be derived from bits 10:8 in the Data Field (see below). The redirection hint bit will be a 1 if bits 10:8 in the delivery mode field associated with corresponding interrupt are encoded as 001 (Lowest Priority). Otherwise, the redirection hint bit will be 0
2	**Destination Mode:** This bit is used only the redirection hint bit is set to 1. If the redirection hint bit and the destination mode bit are both set to 1, then the logical destination mode is used, and the redirection is limited only to those processors that are part of the logical group as based on the logical ID.
1:0	Will always be 00.

Table 5-26. Interrupt Message Data Format

Bit	Description
31:16	Will always be 0000h.
15	**Trigger Mode:** 1 = Level, 0 = Edge. Same as the corresponding bit in the I/O Redirection Table for that interrupt.
14	**Delivery Status:** 1 = Assert, 0 = Deassert. If using edge-triggered interrupts, then bit will always be 1, since only the assertion is sent. If using level-triggered interrupts, then this bit indicates the state of the interrupt input.
13:12	Will always be 00
11	**Destination Mode:** 1 = Logical. 0 = Physical. Same as the corresponding bit in the I/O Redirection Table for that interrupt.
10:8	**Delivery Mode:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt. 000 = Fixed 100 = NMI 001 = Lowest Priority 101 = INIT 010 = SMI/PMI 110 = Reserved 011 = Reserved 111 = ExtINT
7:0	**Vector:** This is the same as the corresponding bits in the I/O Redirection Table for that interrupt.

5.9 Serial Interrupt (D31:F0)

The ICH3 supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the host, the ICH3, and all peripherals that support serial interrupts. The signal line, SERIRQ, is synchronous to PCI clock, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S–Sample Phase.** Signal driven low
- **R–Recovery Phase.** Signal driven high
- **T–Turn-around Phase.** Signal released

The ICH3 supports a message for 21 serial interrupts. These represent the ISA interrupts (IRQ[15:0]), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: When the IDE primary and secondary controllers are configured for native IDE mode, the only way to use the internal IRQ14 and IRQ15 connections to the interrupt controllers is through the Serial Interrupt pin.

5.9.1 Start Frame

The serial IRQ protocol has two modes of operation which affect the start frame. These two modes are: Continuous, where the ICH3 is solely responsible for generating the start frame; and Quiet, where a serial IRQ peripheral is responsible for beginning the start frame.

The mode that must first be entered when enabling the serial IRQ protocol is continuous mode. In this mode, the ICH3 will assert the start frame. This start frame is 4, 6, or 8 PCI clocks wide based on the Serial IRQ Control Register, bits 1:0 at 64h in Device 31:Function 0 configuration space. This is a polling mode.

When the serial IRQ stream enters quiet mode (signaled in the Stop Frame), the SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives the SERIRQ signal low. The ICH3 senses the line low and continues to drive it low for the remainder of the Start Frame. Since the first PCI clock of the start frame was driven by the peripheral in this mode, the ICH3 will drive the SERIRQ line low for 1 PCI clock less than in continuous mode. This mode of operation allows for a quiet, and therefore lower power, operation.

5.9.2 Data Frames

Once the Start frame has been initiated, all of the SERIRQ peripherals must start counting frames based on the rising edge of SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase.** During this phase, the SERIRQ device drives SERIRQ low if the corresponding interrupt signal is low. If the corresponding interrupt is high, the SERIRQ devices tri-state the SERIRQ signal. The SERIRQ line remains high due to pull-up resistors (there is no internal pull-up resistor on this signal, an external pull-up resistor is required). A low level during the IRQ[1:0] and IRQ[15:2] frames indicates that an active-high ISA interrupt is not being requested, but a low level during the PCI INT[A:D], SMI#, and IOCHK# frame indicates that an active-low interrupt is being requested.
- **Recovery Phase.** During this phase, the device drives the SERIRQ line high if in the Sample Phase it was driven low. If it was not driven in the sample phase, it is tri-stated in this phase.
- **Turn-around Phase.** The device tri-states the SERIRQ line

5.9.3 Stop Frame

After all data frames, a Stop Frame will be driven by the ICH3. The SERIRQ signal will be driven low by the ICH3 for 2 or 3 PCI clocks. The number of clocks is determined by the SERIRQ configuration register. The number of clocks determines the next mode:

Table 5-27. Stop Frame Explanation

Stop Frame Width	Next Mode
2 PCI clocks	**Quiet Mode.** Any SERIRQ device may initiate a Start Frame
3 PCI clocks	**Continuous Mode.** Only the host (ICH3) may initiate a Start Frame

5.9.4 Specific Interrupts not Supported via SERIRQ

There are three interrupts seen through the serial stream which are not supported by the ICH3. These interrupts are generated internally, and are not sharable with other devices within the system. These interrupts are:

- IRQ0. Heartbeat interrupt generated off of the internal 8254 counter 0.
- IRQ8#. RTC interrupt can only be generated internally.
- IRQ13. Floating point error interrupt generated off of the processor assertion of FERR#.

The ICH3 ignores the state of these interrupts in the serial stream, and does not adjust their level based on the level seen in the serial stream. In addition, the interrupts IRQ14 and IRQ15 from the serial stream are treated differently than their ISA counterparts. These two frames are not passed to the Bus Master IDE logic. The Bus Master IDE logic expects IDE to be behind the ICH3.

5.9.5 Data Frame Format

Table 5-28 shows the format of the data frames. For the PCI interrupts (A–D), the output from the ICH3 is ANDed with the PCI input signal. This way, the interrupt can be signaled via both the PCI interrupt input signal and via the SERIRQ signal (they are shared).

Table 5-28. Data Frame Format

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. IRQ0 can only be generated via the internal 8524
2	IRQ1	5	
3	SMI#	8	Causes SMI# if low. Will set the SERIRQ_SMI_STS bit.
4	IRQ3	11	
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally or on ISA.
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	
14	IRQ13	41	Ignored. IRQ13 can only be generated from FERR#
15	IRQ14	44	Do not include in BM IDE interrupt logic
16	IRQ15	47	Do not include in BM IDE interrupt logic
17	IOCHCK#	50	Same as ISA IOCHCK# going active.
18	PCI INTA#	53	Drive PIRQA#
19	PCI INTB#	56	Drive PIRQB#
20	PCI INTC#	59	Drive PIRQC#
21	PCI INTD#	62	Drive PIRQD#

5.10 Real Time Clock (D31:F0)

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device with two banks of static RAM with 128 bytes each, although the first bank has 114 bytes for general purpose usage. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 µs to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. Daylight savings compensation is optional. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block has very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions.

The time and calendar data should match the data mode (BCD or binary) and hour mode (12 or 24 hour) as selected in register B. It is up to the programmer to make sure that data stored in these locations is within the reasonable values ranges and represents a possible date and time. The exception to these ranges is to store a value of C0–FFh in the Alarm bytes to indicate a don't care situation. All Alarm conditions must match to trigger an Alarm Flag, which could trigger an Alarm Interrupt if enabled. The SET bit must be one while programming these locations to avoid clashes with an update cycle. Access to time and date information is done through the RAM locations. If a RAM read from the ten time and date bytes is attempted during an update cycle, the value read will not necessarily represent the true contents of those locations. Any RAM writes under the same conditions will be ignored.

Note: The ICH3 supports the ability to generate an SMI# based on Year 2000 rollover. See Section 5.10.4 for more information on the century rollover.

The ICH3 does not implement month/year alarms.

5.10.1 Update Cycles

An update cycle occurs once a second, if the SET bit of register B is not asserted and the divide chain is properly configured. During this procedure, the stored time and date will be incremented, overflow will be checked, a matching alarm condition will be checked, and the time and date will be rewritten to the RAM locations. The update cycle will start at least 488 µs after the UIP bit of register A is asserted, and the entire cycle will not take more than 1984 µs to complete. The time and date RAM locations (0–9) will be disconnected from the external bus during this time.

To avoid update and data corruption conditions, external RAM access to these locations can safely occur at two times. When a updated-ended interrupt is detected, almost 999 ms is available to read and write the valid time and date data. If the UIP bit of register A is detected to be low, there is at least 488 µs before the update cycle begins.

Warning: The overflow conditions for leap years and daylight savings adjustments are based on more than one date or time item. To ensure proper operation when adjusting the time, the new time and data values should be set at least two seconds before one of these conditions (leap year, daylight savings time adjustments) occurs.

5.10.2 Interrupts

The real-time clock interrupt is internally routed within the ICH3 both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the ICH3, nor is it shared with any other interrupt. IRQ8# from the SERIRQ stream is ignored.

5.10.3 Lockable RAM Ranges

The RTC's battery-backed RAM supports two 8-byte ranges that can be locked via the configuration space. If the locking bits are set, the corresponding range in the RAM will not be readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (may be all 0s or all 1s).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to relock the RAM range.

5.10.4 Century Rollover

The ICH3 will detect a rollover when the Year byte (RTC I/O space, index offset 09h) transitions form 99 to 00. Upon detecting the rollover, the ICH3 will set the NEWCENTURY_STS bit (TCOBASE + 04h, bit 7). If the system is in an S0 state, this will cause an SMI#. The SMI# handler can update registers in the RTC RAM that are associated with century value. If the system is in a sleep state (S1–S5) when the century rollover occurs, the ICH3 will also set the NEWCENTURY_STS bit, but no SMI# is generated. When the system resumes from the sleep state, BIOS should check the NEWCENTURY_STS bit and update the century value in the RTC RAM.

5.10.5 Clearing Battery-Backed RTC RAM

Clearing CMOS RAM in an ICH3-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.

Using RTCRST# to Clear CMOS

A jumper on RTCRST# can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTCRST# is strapped to ground, the RTC_PWR_STS bit (D31:F0:A4h bit 2) will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTCRST# to be pulled up through a weak pull-up resistor. The following table shows which bits are set to their default state when RTCRST# is asserted.

Table 5-29. Configuration Bits Reset by RTCRST# Assertion

Bit Name	Default State	Register	Location	Bit(s)
FREQ_STRAP[3:0]	GEN_STS	D31:F0:D4h	11:8	1111b
AIE	RTC Reg B	I/O space	5	0
AF	RTC Reg C	I/O space	5	0
PWR_FLR	GEN_PMCON_3	D31:F0:A4h	1	0
AFTERG3_EN	GEN_PMCON_3	D31:F0:A4h	0	0
RTC_PWR_STS	GEN_PMCON_3	D31:F0:A4h	2	1
PRBTNOR_STS	PM1_STS	PMBase + 00h	11	0
PME_EN	GPE0_EN	PMBase + 2Ah	11	0
RI_EN	GPE0_EN	PMBase + 2Ah	8	0
NEW_CENTURY_STS	TCO1_STS	TCOBase + 04h	7	0
INTRD_DET	TCO2_STS	TCOBase + 06h	0	0
TOP_SWAP	GEN_STS	D31:F0:D4h	13	0
RTC_EN	PM1_EN	PMBase + 02h	10	0
BATLOW_EN	GPE0_EN	PMBase + 2Ah	10	0

Using a GPI to Clear CMOS

A jumper on a GPI can also be used to clear CMOS values. BIOS would detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

Using the SAFEMODE Strap to Clear CMOS

A jumper on AC_SDOUT (SAFEMODE strap) can also be used to clear CMOS values. BIOS would detect the setting of the SAFE_MODE status bit (D31:F0: Offset D4h bit 2) on system boot-up, and manually clear the CMOS array.

Note: Both the GPI & SAFEMODE strap techniques to clear CMOS require multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again. The RTCRST# jumper technique allows the jumper to be moved and then replaced, all while the system is powered off. Then, once booted, the RTC_PWR_STS can be detected in the set state.

Note: Clearing CMOS, using a jumper on VCCRTC, **must not** be implemented.

5.11 Processor Interface (D31:F0)

The ICH3 interfaces to the processor with a variety of signals

- Standard Outputs to processor: A20M#, SMI#, NMI, INIT#, INTR, STPCLK#, IGNNE#, CPUSLP#
- Standard Input from processor: FERR#

Most ICH3 outputs to the processor use standard buffers. The ICH3 has a separate Vcc signal which is pulled up at the system level to the processor voltage, and thus determines Voh for the outputs to the processor. Note that this is different than previous generations of chips, that have used open-drain outputs. This new method saves up to 12 external pull-up resistors.

The ICH3 also handles the speed setting for the processor by holding specific signals at certain states just prior to CPURST going inactive. This avoids the glue often required with other chipsets.

The ICH3 does not support the processor's FRC mode.

5.11.1 Processor Interface Signals

This section describes each of the signals that interface between the ICH3 and the processor(s). Note that the behavior of some signals may vary during processor reset, as the signals are used for frequency strapping.

5.11.1.1 A20M#

The A20M# signal will be active (low) when both of the following conditions are true:

- The ALT_A20_GATE bit (Bit 1 of PORT92 Register) is a 0
- The A20GATE input signal is a 0

The A20GATE input signal is expected to be generated by the external microcontroller (KBC).

5.11.1.2 INIT#

The INIT# signal will be active (driven low) based on any one of several events described in Table 5-30. When any of these events occur, INIT# is driven low for 16 PCI clocks, then driven high.

Note: The 16-clock counter for INIT# assertion will halt while STPCLK# is active. Therefore, if INIT# is supposed to go active while STPCLK# is asserted, it will actually go active after STPCLK# goes inactive.

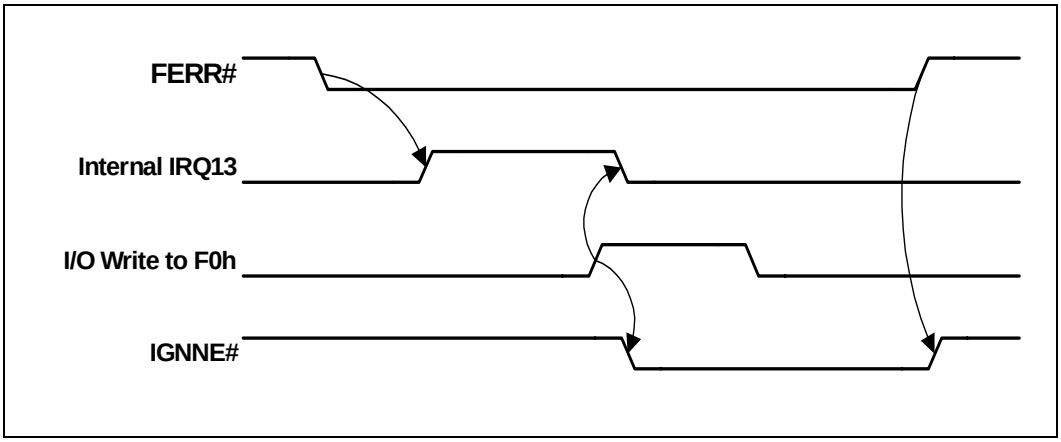
Table 5-30. INIT# Going Active

Cause of INIT# Going Active	Comment
Shutdown special cycle from processor.	
PORT92 write, where INIT_NOW (bit 0) transitions from a 0 to a 1.	
PORTCF9 write, where RST_CPU (bit 2) was a 0 and SYS_RST(bit 1) transitions from 0 to 1.	
RCIN# input signal goes low. RCIN# is expected to be driven by the external microcontroller (KBC).	0 to 1 transition on RCIN# must occur before the ICH3 will arm INIT# to be generated again. **Note:** RCIN# signal is expected to be high during S1 and low during S3, S4, and S5 states. Transition on the RCIN# signal in those states (or the transition to those states) may not necessarily cause the INIT# signal to be generated to the processor.
CPU BIST	To enter BIST, the software sets CPU_BIST_EN bit and then does a full processor reset using the CF9 Register.

5.11.1.3 FERR#/IGNNE# (Coprocessor Error)

The ICH3 supports the coprocessor error function with the FERR#/IGNNE# pins. The function is enabled via the COPROC_ERR_EN bit (Device 31:Function 0, Offset D0, bit 13). FERR# is tied directly to the Coprocessor Error signal of the processor. If FERR# is driven active by the processor, IRQ13 goes active (internally). When it detects a write to the COPROC_ERR Register, the ICH3 negates the internal IRQ13 and drives IGNNE# active. IGNNE# remains active until FERR# is driven inactive. IGNNE# is never driven active unless FERR# is active.

Figure 5-12. Coprocessor Error Timing Diagram



If COPROC_ERR_EN is not set, then the assertion of FERR# will have not generate an internal IRQ13, nor will the write to F0h generate IGNNE#.

5.11.1.4 NMI

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 5-31.

Table 5-31. NMI Sources

Cause of NMI	Comment
SERR# goes active (either internally, externally via SERR# signal, or via message from MCH)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, offset 4Eh, bit 11).
IOCHK# goes active via SERIRQ# stream (ISA system Error)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, offset 4Eh, bit 11).

5.11.1.5 STPCLK# and CPUSLP# Signals

The ICH3 power management logic controls these active-low signals. Refer to Section 5.12 for more information on the functionality of these signals.

5.11.1.6 CPUPWRGD Signal

This signal is connected to the processor's PWRGOOD input. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH3's PWROK and VRMPWRGD signals.

5.11.2 Dual Processor Issues

5.11.2.1 Signal Differences

In dual processor designs, some of the processor signals are unused or used differently than for uniprocessor designs.

Table 5-32. DP Signal Differences

Signal	Difference
A20M# / A20GATE	Generally not used, but still supported by ICH3.
STPCLK#	Used for S1 State as well as preparation for entry to S3–S5 Also allows for THERM# based throttling (not via ACPI control methods). Should be connected to both CPUs.
FERR# / IGNNE#	Generally not used, but still supported by ICH3.

5.11.2.2 Power Management

Attempting clock control with more than one processor is not feasible, because the Host controller does not provide any indication as to which processor is executing a particular Stop-Grant cycle. Without this information, there is no way for the ICH3 to know when it is safe to deassert STPCLK#.

Because the S1 state will have the STPCLK# signal active, the STPCLK# signal can be connected to both processors. However, for ACPI implementations, the ICH3 will not support the C2 state for both processors, since there are not two processor control blocks. The BIOS must indicate that the ICH3 only supports the C1 state for dual processor designs. However, the THRM# signal can be used for overheat conditions to activate thermal throttling.

When entering S1, the ICH3 asserts STPCLK# to both CPUs. In order to meet the processor specifications, the CPUSLP# signal will have to be delayed until the 2nd Stop-Grant cycle occurs. To ensure this, the ICH3 will wait a minimum or 60 PCI clocks after receipt of the first Stop-Grant cycle before asserting CPUSLP# (if the SLP_EN bit is set to 1).

Both processors must immediately respond to the STPCLK# assertion with stop grant acknowledge cycles before the ICH3 asserts CPUSLP# in order to meet the processor setup time for CPUSLP#. Meeting the processor setup time for CPUSLP# is not an issue if both processors are idle when the system is entering S1. If it cannot be guaranteed that both processors will be idle, do not enable the SLP_EN bit. Note that setting SLP_EN to 1 is not required to support S1 in a dual processor configuration.

In going to the S3, S4, or S5 states, the system will appear to pass through the S1 state, and thus STPCLK# and SLP# are also used. During the S3, S4, and S5 states, both processors will lose power. Upon exit from those states, the processors will have their power restored.

5.11.3 Speed Strapping for the Processor

The ICH3 directly sets the speed straps for the processor, saving the external logic that has been needed with prior PCIsets. Refer to processor specification for speed strapping definition.

The ICH3 will perform the following to set the speed straps for the processor:

1. While PCIRST# is active, the ICH3 will drive A20M#, IGNNE#, NMI, and INTR high.
2. As soon as PWROK goes active, the ICH3 reads the FREQ_STRAP field contents.
3. The next step depends on the power state being exited as described in Table 5-33.

Table 5-33. Frequency Strap Behavior Based on Exit State

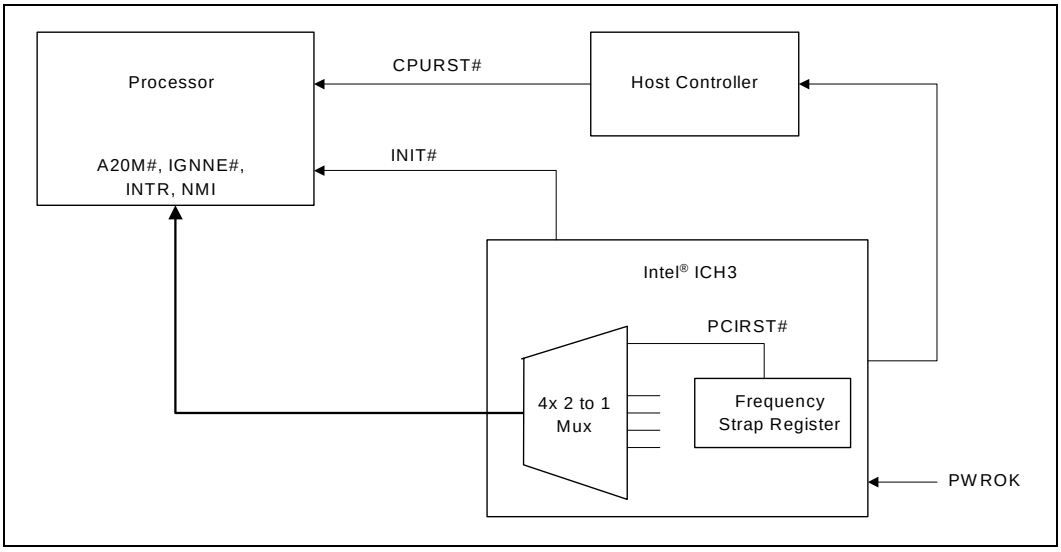
State Exiting	ICH3
S1	There is no processor reset, so no frequency strap logic is used.
S3, S4, S5, or G3	Based on PWROK going active, the ICH3 will deassert PCIRST#, and based on the value of the FREQ_STRAP field (D31:F0,Offset D4), the ICH3 will drive the intended core frequency values on A20M#, IGNNE#, NMI, and INTR. The ICH3 will hold these signals for 120 ns after CPURST# is deasserted by the Host controller.

Table 5-34. Frequency Strap Bit Mapping

FREQ_STRAP Bits [3:0]	Sets High/Low Level for the Corresponding Signal
3	NMI
2	INTR
1	IGNNE#
0	A20M#

NOTE: The FREQ_STRAP Register is in the RTC well. The value in the register can be forced to 1111h via a pinstrap (AC_SDOUT signal), or the ICH3 can automatically force the speed strapping to 1111h if the processor fails to boot.

Figure 5-13. Signal Strapping



5.12 Power Management (D31:F0)

5.12.1 Features

- ACPI Power and Thermal Management Support
  - — ACPI 24-Bit Timer
  - — Software initiated throttling of processor performance for Thermal and Power Reduction
  - — Hardware Override to throttle processor performance if system too hot
  - — SCI and SMI# Generation
- PCI PME# Signal for Wake Up from Low-Power states
- System Clock Control
  - — ACPI C2 state: Stop-Grant state (using STPCLK# signal) halts processor's instruction stream
- System Sleeping State Control
  - — ACPI S1 state: Like C2 state (only STPCLK# active, and SLP# optional)
  - — ACPI S3 state–Suspend to RAM (STR)
  - — ACPI S4 state–Suspend-to-Disk (STD)
  - — ACPI G2/S5 state–Soft Off (SOFF)
  - — Power Failure Detection and Recovery
- Streamlined Legacy Power Management Support for APM-Based Systems

5.12.2 Intel® ICH3 and System Power States

Table 5-35 shows the power states defined for ICH3-based platforms. The state names generally match the corresponding ACPI states.

Table 5-35. General Power States for Systems using Intel® ICH3

State/ Substates	Legacy Name / Description
G0/S0/C0	**Full On:** processor operating. Individual devices may be shut down to save power. The different processor operating levels are defined by Cx states, as shown in Table 5-36. Within the C0 state, the ICH3 can throttle the STPCLK# signal to reduce power consumption. The throttling can be initiated by software or by the THRM# input signal.
G0/S0/C1	**Auto-Halt:** Processor has executed a AutoHalt instruction and is not executing code. The processor snoops the bus and maintains cache coherency.
G0/S0/C2	**Stop-Grant t:** The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle, halts its instruction stream, and remains in that state until the STPCLK# signal goes inactive. In the Stop-Grant state, the processor snoops the bus and maintains cache coherency.
G1/S1	**Stop-Grant:** Similar to G0/S0/C2 state. ICH3 also has the option to assert the CPUSLP# signal to further reduce processor power consumption. Note: The behavior for this state is slightly different when supporting iA64 processors.
G1/S3	**System to RAM (STR).** The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is maintained and refreshes continue. All clocks stop except RTC clock.
G1/S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
G2/S5	**Soft Off (SOFF):** System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
G3	**Mechanical OFF (MOFF):** System context not maintained. All power is shut off except for the RTC. No “Wake” events are possible, because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the “waking” logic. When system power returns, transition depends on the state just prior to the entry to G3 and the AFTERG3 bit in the GEN_PMCON3 Register (D31:F0, offset A4). Refer to Table 5-43 for more details.

Table 5-36 shows the transitions rules among the various states. Note that transitions among the various states may appear to temporarily transition through intermediate states. For example, in going from S0 to S1, it may appear to pass through the G0/S0/C2 states. These intermediate transitions and states are not listed in the table.

Table 5-36. State Transition Rules for Intel® ICH3

Present State	Transition Trigger	Next State
G0/S0/C0	• Processor halt instruction • Level 2 Read • • SLP_EN bit set • Power Button Override • Mechanical Off/Power Failure	• G0/S0/C1 • G0/S0/C2 • G1/Sx or G2/S5state • G2/S5 • G3
G0/S0/C1	• Any Enabled Break Event • STPCLK# goes active • Power Button Override • Power Failure	• G0/S0/C0 • G0/S0/C2 • G2/S5 • G3
G0/S0/C2	• Any Enabled Break Event • STPCLK# goes inactive and previously in C1 • Power Button Override • Power Failure	• G0/S0/C0 • G0/S0/C1 • G2/S5 • G3
G1/S1, G1/S3 or G1/S4	• Any Enabled Wake Event • Power Button Override • Power Failure	• G0/S0/C0 • G2/S5 • G3
G2/S5	• Any Enabled Wake Event • Power Failure	• G0/S0/C0 • G3
G3	• Power Returns	• Optional to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other wake event). (See Note 1)

NOTES:
1. Some wake events can be preserved through power failure.

5.12.3 System Power Planes

The system has several independent power planes, as described in Table 5-37. Note that when a particular power plane is shut off, it should go to a 0 V level.

Table 5-37. System Power Plane

Plane	Controlled By	Description
Processor	SLP_S3# Signal	SLP_S1# puts the clock generator into a low-power state, but does not cut the power to the processor. The SLP_S3# signal can be used to cut the processor's power completely
Main	SLP_S3# Signal	When SLP_S3# goes active, power can be shut off to any circuit not required to wake the system from the S3 state. Since the S3 state requires that the memory context be preserved, power must be retained to the main memory. The processor, devices on the PCI bus, LPC I/F downstream hub interface and AGP will typically be shut off when the Main power plane is shut, although there may be small subsections powered.
Memory	SLP_S5# Signal	When the SLP_S5# goes active, power can be shut off to any circuit not required to wake the system from the S4 or S5 state. Since the memory context does not need to be preserved in the S5 state, the power to the memory can also be shut down.
Device[n]	GPIO	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.

5.12.4 Intel® ICH3 Power Planes

The ICH3 power planes were previously defined in Section 3.1.

Although not specific power planes within the ICH3, there are many interface signals that go to devices that may be powered down. These include:

- IDE: ICH3 can tri-state or drive low all IDE output signals and shut off input buffers.
- USB: ICH3 can tri-state USB output signals and shut off input buffers if USB wakeup is not desired
- AC '97: ICH3 can drive low the outputs and shut off inputs

5.12.5 SMI#/SCI Generation

Upon any SMI# event taking place, ICH3 will assert SMI# to the processor, which will cause it to enter SMM space. SMI# remains active until the EOS bit is set. When the EOS bit is set, SMI# will go inactive for a minimum of 4 PCICLK. If another SMI event occurs, SMI# will be driven active again.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts 9, 10, 11, 20, 21, 22, or 23. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not; (see Section 9.1.11 *ACPI Control Register* for details.) The interrupt will remain asserted until all SCI sources are removed."

Table 5-38 shows which events can cause an SMI# and SCI. Note that some events can be programmed to cause either an SMI# or SCI. The usage of the event for SCI (instead of SMI#) is typically associated with an ACPI-based system. Each SMI# or SCI source has a corresponding enable and status bit.

Table 5-38. Causes of SMI# and SCI

Cause	SCI	SMI	Additional Enables	Where Reported
PME#	Yes	Yes	PME_EN=1	PME_STS
PME_B0 (internal EHCI controller)	Yes	Yes	PME_B0_EN=1	PME_B0_STS
Power Button Press	Yes	Yes	PWRBTN_EN=1	PWRBTN_STS
RTC Alarm	Yes	Yes	RTC_EN=1	RTC_STS
Ring Indicate	Yes	Yes	RI_EN=1	RI_STS
AC '97 wakes	Yes	Yes	AC97_EN=1	AC97_STS
USB#1 wakes	Yes	Yes	USB1_EN=1	USB1_STS
USB#2 wakes	Yes	Yes	USB2_EN=1	USB2_STS
USB#3 wakes	Yes	Yes	USB3_EN=1	USB3_STS
THRM# pin active	Yes	Yes	THRM_EN=1	THRM_STS
ACPI Timer overflow (2.34 sec.)	Yes	Yes	TMROF_EN=1	TMROF_STS
Any GPI	Yes	Yes	GPI[x]_Route=10 (SCI) GPI[x]_Route=01 (SMI) GPE1[x]_EN=1	GPI[x]_STS GPE1_STS
TCO SCI Logic	Yes	No	TCOSCI_EN=1	TCOSCI_STS
TCO SCI message from MCH	Yes	No	none	MCHSCI_STS
TCO SMI Logic	No	Yes	TCO_EN=1	TCO_STS
TCO SMI - Year 2000 Rollover	No	Yes	none	NEWCENTURY_STS
TCO SMI - TCO TIMEROUT	No	Yes	none	TIMEOUT
TCO SMI–OS writes to TCO_DAT_IN Register	No	Yes	none	OS_TCO_SMI
TCO SMI - Message from MCH	No	Yes	none	MCHSMI_STS
TCO SMI–NMI occurred (and NMIs mapped to SMI)	No	Yes	NMI2SMI_EN=1	NMI2SMI_STS
TCO SMI - INTRUDER# signal goes active	No	Yes	INTRD_SEL=10	INTRD_DET
TCO SMI–Change of the BIOSWP bit from 0 to 1	No	Yes	BLD=1	BIOSWR_STS
TCO SMI - Write attempted to BIOS	No	Yes	BIOSWP=1	BIOSWR_STS

Table 5-38. Causes of SMI# and SCI

Cause	SCI	SMI	Additional Enables	Where Reported
BIOS_RLS written to	Yes	No	GBL_EN=1	GBL_STS
GBL_RLS written to	No	Yes	BIOS_EN=1	BIOS_STS
Write to B2h Register	No	Yes	none	APM_STS
Periodic timer expires	No	Yes	PERIODIC_EN=1	PERIODIC_STS
64 ms timer expires	No	Yes	SWSMI_TMR_EN=1	SWSMI_TMR_STS
Legacy USB logic	No	Yes	LEGACY_USB_EN=1	LEGACY_USB_STS
Serial IRQ SMI reported	No	Yes	none	SERIRQ_SMI_STS
Device monitors match address in its range	No	Yes	DEV[n]_TRAP_EN=1	DEVMON_STS, DEV[n]_TRAP_STS
SMBus Host Controller	No	Yes	SMB_SMI_EN Host Controller Enabled	SMBus host status reg.
SMBus Slave SMI message	No	Yes	none	SMBUS_SMI_STS
SMBus SMBALERT# signal active	No	Yes	none	SMBUS_SMI_STS
SMBus Host Notify message received	No	Yes	HOST_NOTIFY_INTREN	SMBUS_SMI_STS HOST_NOTIFY_STS
Access microcontroller 62h/66h	No	Yes	MCSMI_EN	MCSMI_STS
SLP_EN bit written to 1	No	Yes	SMI_ON_SLP_EN=1	SMI_ON_SLP_EN_STS

Notes on causes of SCI and SMI:

1. SCI_EN must be 1 to enable SCI. SCI_EN must be 0 to enable SMI
2. SCI can be routed to cause interrupt 9:11 or 20:23 (20:23 only available in APIC mode)
3. GBL_SMI_EN must be 1 to enable SMI
4. EOS must be written to 1 to re-enable SMI for the next one

5.12.6 Dynamic Processor Clock Control

The ICH3 has extensive control for dynamically starting and stopping system clocks. The clock control is used for transitions among the various S0/Cx states, and processor throttling. Each dynamic clock control method is described in this section. The various Sleep states may also perform types of non-dynamic clock control.

The ICH3 supports the ACPI C0, C1 and C2 states. The Dynamic processor Clock control is handled using the following signals:

- STPCLK#:Used to halt processor instruction stream.

The C1 state is entered based on the processor performing an auto halt instruction.

The C2 state is entered based on the processor reading the Level 2 Register in the ICH3.

A C1, C2 state ends due to a Break event. Based on the break event, the ICH3 returns the system to C0 state. Table 5-39 lists the possible break events from C2. The break events from C1 are indicated in the processor's datasheet

Table 5-39. Break Events

Event	Breaks from	Comment
Any unmasked interrupt goes active	C2	IRQ[0:15] when using the 8259s, IRQ[0:23] for I/O APIC. Since SCI is an interrupt, any SCI will also be a break event.
Any internal event that will cause an NMI or SMI#	C2	Many possible sources
Any internal event that will cause INIT# to go active	C2	Could be indicated by the keyboard controller via the RCIN input signal.
Processor Pending Break Event Indication	C2	Only available if FERR# enabled for break event indication (See FERR# Mux-En in Section 9.1.22)

The ICH3 supports the Pending Break Event (PBE) indication from the processor using the FERR# signal. The following rules apply:

1. When STPCLK# is detected active by the processor, the FERR# signal from the processor is redefined to indicate whether an interrupt is pending. The signal is active low (i.e., FERR# will be low to indicate a pending interrupt).
2. When the ICH3 asserts STPCLK#, it latches the current state of the FERR# signal and continues to present this state to the FERR# state machine (independent of what the FERR# pin does after the latching).
3. When the ICH3 detects the Stop-Grant cycle, it starts looking at the FERR# signal as a break event indication. If FERR# is sampled low, a break event is indicated. This forces a transition to the C0 state.
4. When the processor detects the deassertion of STPCLK#, the processor starts driving the FERR# signal with the natural value (i.e., the value it would do if the pin was not muxed). The time from STPCLK# inactive to the FERR# signal transition back to the native function must be less than 120 ns.
5. The ICH3 waits at least 180 ns after deasserting STPCLK# and then starts using the FERR# signal for an indication of a floating point error. The maximum time that the ICH3 may wait is bounded such that it must have a chance to look at the FERR# signal before reasserting STPCLK#. Based on current implementation, that maximum time would be 240 ns (8 PCI clocks).

The break event associated with this new mechanism does not need to set any particular status bit, since the pending interrupt will be serviced by the processor after returning to the C0 state.

5.12.6.1 Throttling Using STPCLK#

Throttling is used to lower power consumption or reduce heat. The ICH3 asserts STPCLK# to throttle the processor clock and the processor appears to temporarily enter a C2 state. After a programmable time, the ICH3 deasserts STPCLK# and the processor appears to return to the C0 state. This allows the processor to operate at reduced average power, with a corresponding decrease in performance. Two methods are included to start throttling:

1. Software enables a timer with a programmable duty cycle. The duty cycle is set by the THTL_DTY field and the throttling is enabled using the THTL_EN field. This is known as Manual Throttling. The period is fixed to be in the non-audible range, due to the nature of switching power supplies.
2. A Thermal Override condition (THRM# signal active for >2 seconds) occurs that unconditionally forces throttling, independent of the THTL_EN bit. The throttling due to Thermal Override has a separate duty cycle (THRM_DTY) which may vary by field and system. The Thermal Override condition will end when THRM# goes inactive.

Throttling due to the THRM# signal has higher priority than the software initiated throttling.

Throttling does not occur when the system is in a C2 state, even if Thermal override occurs.

5.12.6.2 Transition Rules Among S0/Cx and Throttling States

The following priority rules and assumptions apply among the various S0/Cx and throttling states:

- Entry to any S0/Cx state is mutually exclusive with entry to any S1–S5 state. This is because the processor can only perform one register access at a time and Sleep states have higher priority than thermal throttling.
- When the SLP_EN bit is set (system going to a sleep state (S1–S5), the THTL_EN bit can be internally treated as being disabled (no throttling while going to sleep state). Note that thermal throttling (based on THRM# signal) cannot be disabled in an S0 state. However, once the SLP_EN bit is set, the thermal throttling is shut off (since STPCLK# will be active in S1–S5 states).
- If the THTL_EN bit is set, and a Level 2 read then occurs, the system should immediately go and stay in a C2 state until a break event occurs. A Level 2 read has higher priority than the software initiated throttling or thermal throttling.
- If Thermal Override is causing throttling, and a Level 2read then occurs, the system will stay in a C2 state until a break event occurs. A Level 2 read has higher priority than the Thermal Override.
- After an exit from a C2 state (due to a Break event), and if the THTL_EN bit is still set, or if a Thermal Override is still occurring, the system will continue to throttle STPCLK#. Depending on the time of break event, the first transition on STPCLK# active can be delayed by up to one THRM period (1024 PCI clocks=30.72 microseconds).
- The Host controller must post Stop-Grant cycles in such a way that the processor gets an indication of the end of the special cycle prior to the ICH3 observing the Stop-Grant cycle. This ensures that the STPCLK# signals stays active for a sufficient period after the processor observes the response phase.
- If in the C1 state and the STPCLK# signal goes active, the processor will generate a Stop-Grant cycle, and the system should go to the C2 state. When STPCLK# goes inactive, it should return to the C1 state.

5.12.7 Sleep States

The ICH3 directly supports different sleep states (S1–S5), which are entered by setting the SLP_EN bit, or due to a Power Button press. The entry to the Sleep states are based on several assumptions:

- Entry to a Cx state is mutually exclusive with entry to a Sleep state. This is because the processor can only perform one register access at a time. A request to Sleep always has higher priority than throttling.
- Prior to setting the SLP_EN bit, the software will turn off processor-controlled throttling. Note that thermal throttling cannot be disabled, but setting the SLP_EN bit will disable thermal throttling (since S1–S5 sleep state has higher priority).
- The G3 state cannot be entered via any software mechanism. The G3 state indicates a complete loss of power.

5.12.7.1 Initiating Sleep State

Sleep states (S1–S5) are initiated by:

- Masking interrupts, turning off all bus master enable bits, setting the desired type in the SLP_TYP field and then setting the SLP_EN bit. The hardware will then attempt to gracefully put the system into the corresponding Sleep state by first going to a C2 state. See Section 5.12.6 for details on going to the C2 state.
- Pressing the PWRBTN# Signal for more than 4 seconds to cause a Power Button Override event. In this case the transition to the S5 state will be less graceful, since there will be no dependencies on observing Stop-Grant cycles from the processor or on clocks other than the RTC clock.

Table 5-40. Sleep Types

Sleep Type	Comment
S1	ICH3 asserts the STPCLK# signal. It also has the option to assert CPUSLP# signal. This will lower the processor's power consumption. No snooping is possible in this state.
S3	ICH3 asserts SLP_S3#. The SLP_S3# signal will control the power to non-critical circuits. Power will only be retained to devices needed to wake from this sleeping state, as well as to the memory.
S4	ICH3 asserts SLP_S3# and SLP_S5#. The SLP_S5# signal will shut off the power to the memory subsystem. Only devices needed to wake from this state should be powered.
S5	Same as S4. ICH3 asserts SLP_S3# and SLP_S5#. The SLP_S5# signal will shut off the power to the memory subsystem. Only devices needed to wake from this state should be powered.

5.12.7.2 Exiting Sleep States

Sleep states (S1–S5) are exited based on Wake events. The Wake events will force the system to a full on state (S0), although some non-critical subsystems might still be shut off and have to be brought back manually. For example, the hard disk may be shut off during a sleep state, and have to be enabled via a GPIO pin before it can be used.

Upon exit from the ICH3-controlled Sleep states, the WAK_STS bit is set. The possible causes of Wake Events (and their restrictions) are shown in Table 5-41.

Table 5-41. Causes of Wake Events

Cause	States Can Wake From	How Enabled
RTC Alarm	S1–S5 (Note 1)	Set RTC_EN bit in PM1_EN Register
Power Button	S1–S5	Always enabled as Wake event
GPI[0:n]	S1–S5 (Note 1)	GPE1_EN Register
USB	S1–S4	Set USB1_EN, USB 2_EN or USB3_EN bits in GPE0_EN Register
LAN	S1–S5	Will use PME#. Wake enable set with LAN logic.
RI#	S1–S5 (Note 1)	Set RI_EN bit in GPE0_EN Register
AC '97	S1–S5	Set AC97_EN bit in GPE0_EN Register
Primary PME#	S1–S5	PME_B0_EN bit in GPE0_EN Register
Secondary PME#	S1–S5 (Note 1)	Set PME_EN bit in GPE0_EN Register.
SMBALERT#	S1–S4	SMB_WAK_EN in the GPE0 Register
SMBus Slave Message	S1–S5	Wake/SMI# command always enabled as a Wake Event. **Note:** SMBus Slave Message can wake the system from S1–S5, as well as from S5 due to Power Button Override.
SMBus Host Notify Message Received	S1–S5	HOST_NOTIFY_WKEN bit SMBus Slave Command Register. Reported in the SMB_WAK_STS bit in the GPEO_STS Register.

NOTES:
1. This will be a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software.
2. If in the S5 state due to a powerbutton override, the possible wake events are due to Power Button, Hard Reset Without Cycling (See Command Type 3 in Table 5-93), and Hard Reset System (See Command Type 4 in Table 5-93).

It is important to understand that the various GPIs have different levels of functionality when used as wake events. The GPIs that reside in the core power well can only generate wake events from an S1 state. Also only certain GPIs are "ACPI Compliant," meaning that their Status and Enable bits reside in ACPI I/O space. Table 5-42 summarizes the use of GPIs as wake events.

Table 5-42. GPI Wake Events

GPI	Power Well	Wake From	Notes
GPI[7:0], GPI[23:16]	Core	S1	
GPI[15:8]	Resume	S1–S5	ACPI Compliant

The latency to exit the various Sleep states varies greatly and is heavily dependent on power supply design, so much so that the exit latencies due to the ICH3 are insignificant.

5.12.7.3 Sx–G3–Sx, Handling Power Failures

In server systems, power failures can occur if the AC power is cut (a real power failure) or if the system is unplugged. In either case, PWROK and RSMRST# are assumed to go low.

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system will remain in an S5 state (unless previously in S4). There are only three possible events that will wake the system after a power failure.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the ICH3 exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because Vcc-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.
2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.

The ICH3 monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

Note: Although PME_EN is in the RTC well, this signal cannot wake the system after a power loss. PME_EN is cleared by RTCRST#, and PME_STS is cleared by RSMRST#.

Table 5-43. Transitions Due to Power Failure

State at Power Failure	AFTERG3_EN Bit	Transition When Power Returns
S0, S1	1 0	S5 S0
S4	1 0	S4 S0
S5	1 0	S5 S0

5.12.8 Thermal Management

The ICH3 has mechanisms to assist with managing thermal problems in the system.

5.12.8.1 THRM# Signal

The THRM# signal is used as a status input for a thermal sensor. Based on the THRM# signal going active, the ICH3 generates an SMI# or SCI (depending on SCI_EN).

If the THRM_POL bit is set low, when the THRM# signal goes low, the THRM_STS bit will be set. This is an indicator that the thermal threshold has been exceeded. If the THRM_EN bit is set, then when THRM_STS goes active, either an SMI# or SCI will be generated (depending on the SCI_EN bit being set).

The power management software (BIOS or ACPI) can then take measures to start reducing the temperature. Examples include shutting off unwanted subsystems, or halting the processor.

By setting the THRM_POL bit to high, another SMI# or SCI can optionally be generated when the THRM# signal goes back high. This allows the software (BIOS or ACPI) to turn off the cooling methods.

Note: THRM# assertion will not cause TCO event message in S3 or S4. The level of the signal will not be reported in the heartbeat message.

5.12.8.2 THRM# Initiated Passive Cooling

If the THRM# signal remains active for some time greater than 2 seconds and the ICH3 is in the S0/G0/C0 state, then the ICH3 enters an auto-throttling mode, in which it provides a duty cycle on the STPCLK# signal. This will reduce the overall power consumption by the system, and should cool the system. The intended result of the cooling is that the THRM# signal should go back inactive.

For all programmed values (001–111), THRM# going active will result in STPCLK# active for a minimum time of 12.5% and a maximum of 87.5%. The period is 1024 PCI clocks. Thus, the STPCLK# signal can be active for as little as 128 PCI clocks or as much as 896 PCI clocks. The actual slowdown (and cooling) of the processor will depend on the instruction stream, because the processor is allowed to finish the current instruction. Furthermore, the ICH3 waits for the STOP-GRANT cycle before starting the count of the time the STPCLK# signal is active.

When THRM# goes inactive, the throttling will stop.

In case that the ICH3 is already attempting throttling because the THTL_EN bit is set, the duty cycle associated with the THRM# signal will have higher priority.

If the ICH3 is in the C2 or S1–S5 states, then no throttling will be caused by the THRM# signal being active.

5.12.8.3 THRM# Override Software Bit

The FORCE_THTL bit allows the BIOS to force passive cooling, just as if the THRM# signal had been active for 2 seconds. If this bit is set, the ICH3 will start throttling using the ratio in the THRM_DTY field.

When this bit is cleared the ICH3 will stop throttling, unless the THRM# signal has been active for 2 seconds or if the THTL_EN bit is set (indicating that ACPI software is attempting throttling).

5.12.8.4 Processor Initiated Passive Cooling (Via Programmed Duty Cycle on STPCLK#)

Using the THTL_EN and THTL_DTY bits, the ICH3 can force a programmed duty cycle on the STPCLK# signal. This will reduce the effective instruction rate of the processor and cut its power consumption and heat generation.

5.12.8.5 Active Cooling

Active cooling involves fans. The GPIO signals from the ICH3 can be used to turn on/off a fan.

5.12.9 Event Input Signals and Their Usage

The ICH3 has various input signals that trigger specific events. This section describes those signals and how they should be used.

5.12.9.1 PWRBTN#–Power Button

The ICH3 PWRBTN# signal operates as a “Fixed Power Button” as described in the ACPI specification. PWRBTN# signal has a 16 ms de-bounce on the input. The state transition descriptions are included in the following table. Note that the transitions start as soon as the PWRBTN# is pressed (but after the de-bounce logic), and does not depend on when the Power Button is released.

Table 5-44. Transitions Due to Power Button

Present State	Event	Transition/Action	Comment
S0/Cx	PWRBTN# goes low	SMI# or SCI generated (depending on SCI_EN)	Software will typically initiate a Sleep state.
S1–S5	PWRBTN# goes low	Wake Event. Transitions to S0 state.	Standard wakeup
G3	PWRBTN# pressed	None	No effect since no power. Not latched nor detected.
S0–S4	PWRBTN# held low for at least 4 consecutive seconds	Unconditional transition to S5 state.	No dependence on processor (such as Stop-Grant cycles) or any other subsystem.

Power Button Override Function

If PWRBTN# is observed active for at least 4 consecutive seconds, then the state machine should unconditionally transition to the G2/S5 state, regardless of present state (S0–S4). In this case, the transition to the G2/S5 state should not depend on any particular response from the processor (e.g., a Stop-Grant cycle), nor any similar dependency from any other subsystem.

The PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable via the PWRBTN_LVL bit.

Note: The 4-second PWRBTN# assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the ICH3 is in a S0 state. If the PWRBTN# signal is asserted and held active when the system is in a suspend state (S1–S5), the assertion will cause a wake event. Once the system has resumed to the S0 state, the 4-second timer will start.

Sleep Button

The ACPI specification defines an optional Sleep button. It differs from the power button in that it only is a request to go from S0 to S1–S4 (not S5). Also, in an S5 state, the Power Button can wake the system, but the Sleep Button cannot.

Although the ICH3 does not include a specific signal designated as a Sleep Button, one of the GPIO signals can be used to create a “Control Method” Sleep Button. See the ACPI specification for implementation details.

5.12.9.2 RI#—Ring Indicate

The Ring Indicator can cause a wake event (if enabled) from the S1–S5 states. Table 5-45 shows when the wake event is generated or ignored in different states. If in the G0/S0/Cx states, the ICH3 will generate an interrupt based on RI# active, and the interrupt will be set up as a break event.

Table 5-45. Transitions Due to RI# Signal

Present State	Event	RI_EN	Event
S0	RI# Active	X	Ignored
S1–S5	RI# Active	0 1	Ignored Wake Event

Note: Filtering/Debounce on RI# will not be done in ICH3. This can be in a modem or external.

5.12.9.3 PME#—PCI Power Management Event

The PME# signal comes from a PCI device to request that the system be restarted. The PME# signal can generate an SMI#, SCI, or optionally a Wake event. The event occurs when the PME# signal goes from high to low. No event is caused when it goes from low to high.

In the EHCI controller, there is an internal PME_B0 bit. This is separate from the external PME# signal and can cause the same effect.

5.12.10 ALT Access Mode

Before entering a low-power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the ICH3 implements an ALT access (alternative access) mode.

If the ALT access mode is entered and exited after reading the registers of the ICH3 timer (8254), the timer starts counting faster (13.5 ms). The following steps listed below can cause problems:

- BIOS enters ALT access mode for reading the ICH3 timer related registers.
- BIOS exits ALT access mode.
- BIOS continues through the execution of other needed steps and passes control to the OS.

After getting control in step #3, if the OS does not reprogram the system timer again the timer ticks may be happening faster than expected. For example DOS and its associated software assume that the system timer is running at 54.6 ms and as a result the timeouts in the software may be happening faster than expected.

Operating Systems (e.g., Windows* 98, Windows* 2000 and Windows NT*) reprogram the system timer; hence, will not run into this problem.

For some other OSs (e.g., DOS), the BIOS should restore the timer back to 54.6 ms before passing control to the OS. If the BIOS is entering ALT access mode before entering the suspend state it is not necessary to restore the timer contents after the exit from ALT access mode.

5.12.10.1 Write Only Registers with Read Paths in ALT Access Mode

The registers described in the following table have read paths in ALT access mode. The access number field in the table indicates which register will be returned per access to that port.

Table 5-46. Write Only Registers with Read Paths in ALT Access Mode

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
00h	2	1	DMA Chan 0 base address low byte	40h	7	1	Timer Counter 0 status, bits [5:0]
		2	DMA Chan 0 base address high byte			2	Timer Counter 0 base count low byte
01h	2	1	DMA Chan 0 base count low byte			3	Timer Counter 0 base count high byte
		2	DMA Chan 0 base count high byte			4	Timer Counter 1 base count low byte
02h	2	1	DMA Chan 1 base address low byte			5	Timer Counter 1 base count high byte
		2	DMA Chan 1 base address high byte			6	Timer Counter 2 base count low byte
03h	2	1	DMA Chan 1 base count low byte			7	Timer Counter 2 base count high byte
		2	DMA Chan 1 base count high byte	41h	1		Timer Counter 1 status, bits [5:0]
04h	2	1	DMA Chan 2 base address low byte	42h	1		Timer Counter 2 status, bits [5:0]
		2	DMA Chan 2 base address high byte	70h	1		Bit 7 = NMI Enable, Bits [6:0] = RTC Address
05h	2	1	DMA Chan 2 base count low byte	C4h	2	1	DMA Chan 5 base address low byte
		2	DMA Chan 2 base count high byte			2	DMA Chan 5 base address high byte
06h	2	1	DMA Chan 3 base address low byte	C6h	2	1	DMA Chan 5 base count low byte
		2	DMA Chan 3 base address high byte			2	DMA Chan 5 base count high byte
07h	2	1	DMA Chan 3 base count low byte	C8h	2	1	DMA Chan 6 base address low byte
		2	DMA Chan 3 base count high byte			2	DMA Chan 6 base address high byte

Table 5-46. Write Only Registers with Read Paths in ALT Access Mode (Continued)

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
08h	6	1	DMA Chan 0–3 Command[2]	CAh	2	1	DMA Chan 6 base count low byte
		2	DMA Chan 0–3 Request			2	DMA Chan 6 base count high byte
		3	DMA Chan 0 Mode: Bits(1:0) = “00”	CCh	2	1	DMA Chan 7 base address low byte
		4	DMA Chan 1 Mode: Bits(1:0) = “01”			2	DMA Chan 7 base address high byte
		5	DMA Chan 2 Mode: Bits(1:0) = “10”	CEh	2	1	DMA Chan 7 base count low byte
		6	DMA Chan 3 Mode: Bits(1:0) = “11”.			2	DMA Chan 7 base count high byte
20h	12	1	PIC ICW2 of Master controller	D0h	6	1	DMA Chan 4–7 Command[2]
		2	PIC ICW3 of Master controller			2	DMA Chan 4–7 Request
		3	PIC ICW4 of Master controller			3	DMA Chan 4 Mode: Bits(1:0) = “00”
		4	PIC OCW1 of Master controller[1]			4	DMA Chan 5 Mode: Bits(1:0) = “01”
		5	PIC OCW2 of Master controller			5	DMA Chan 6 Mode: Bits(1:0) = “10”
		6	PIC OCW3 of Master controller			6	DMA Chan 7 Mode: Bits(1:0) = “11”.
		7	PIC ICW2 of Slave controller				
		8	PIC ICW3 of Slave controller				
		9	PIC ICW4 of Slave controller				
		10	PIC OCW1 of Slave controller[1]				
		11	PIC OCW2 of Slave controller				
		12	PIC OCW3 of Slave controller				

NOTE:
1. The OCW1 register must be read before entering ALT access mode.
2. Bits 5, 3, 1, and 0 return 0.

5.12.10.2 PIC Reserved Bits

Many bits within the PIC are reserved, and must have certain values written in order for the PIC to operate properly. Therefore, there is no need to return these values in ALT access mode. When reading PIC registers from 20h and A0h, the reserved bits shall return the values listed in the following table.

Table 5-47. PIC Reserved Bits Return Values

PIC Reserved Bits	Value Returned
ICW2(2:0)	000
ICW4(7:5)	000
ICW4(3:2)	00
ICW4(0)	0
OCW2(4:3)	00
OCW3(7)	0
OCW3(5)	Reflects bit 6
OCW3(4:3)	01

5.12.10.3 Read Only Registers with Write Paths in ALT Access Mode

The registers described in Table 5-48 have write paths to them in ALT access mode. Software will restore these values after returning from a powered down state. These registers must be handled special by software. When in normal mode, writing to the base address/count register also writes to the current address/count register. Therefore, the base address/count must be written first, then the part is put into ALT access mode and the current address/count register is written.

Table 5-48. Register Write Accesses in ALT Access Mode

I/O Address	Register Write Value
08h	DMA Status Register for channels 0–3.
D0h	DMA Status Register for channels 4–7.

5.12.11 System Power Supplies, Planes, and Signals

5.12.11.1 Power Plane Control with SLP_S3# and SLP_S5#

The SLP_S3# output signal can be used to cut power to the system core supply, since it will only go active for the STR state (typically mapped to ACPI S3). Power must be maintained to the ICH3 Resume Well, and to any other circuits that need to generate Wake signals from the STR state.

Cutting power to the core may be done via the power supply, or by external FETs to the motherboard. The SLP_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done via the power supply, or by external FETs to the motherboard.

5.12.11.2 PWROK Signal

The PWROK input should go active based on the core supply voltages becoming valid. PWROK should go active no sooner than 10 ms after Vcc3_3 and Vcc1_8 have reached their nominal values.

Notes:

1. Traditional designs have a reset button logically ANDs with the PWROK signal from the power supply and the processor's voltage regulator module. If this is done with the ICH3, the PWROK_FLR bit will be set. The ICH3 treats this internally as if the RSMRST# signal had gone active. However, it is not treated as a full power failure. If PWROK goes inactive and then active (but RSMRST# stays high), then the ICH3 will reboot (regardless of the state of the AFTERG3 bit). If the RSMRST# signal also goes low before PWROK goes high, then this is a full power failure, and the reboot policy is controlled by the AFTERG3 bit.
2. PWROK and RSMRST# are sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the ICH3

5.12.11.3 VRMPWRGD Signal

This signal is connected to the processor's VRM and is internally ANDed with the PWROK signal that comes from the system power supply. This saves the external AND gate found in server systems that traditionally has been external to the chipset.

5.12.11.4 Controlling Leakage and Power Consumption During Low-Power States

To control leakage in the system, various signals will tri-state or go low during some low-power states.

General principles

- All signals going to powered down planes (either internally or externally) must be either tri-stated or driven low.
- Signals with pull-up resistors should not be low during low-power states. This is to avoid the power consumed in the pull-up resistor.
- Buses should be halted (and held) in a known state to avoid a floating input (perhaps to some other device). Floating inputs can cause extra power consumption.

Based on the above principles, the following measures are taken:

- During S3 (STR), all signals attached to powered down planes will be tri-stated or driven low.

5.12.12 Clock Generators

The clock generator is expected to provide the frequencies shown in Table 5-49.

Table 5-49. Intel® ICH3 Clock Inputs

Clock Domain	Frequency	Source	Usage
CLK66	66 MHz	Main Clock Generator	Should be running in all Cx states. Stopped in S3 ~ S5 based on SLP_S3# assertion.
PCICLK	33 MHz	Main Clock Generator	Free-running PCI Clock to ICH3. Stopped in S3 ~ S5 based on SLP_S3# assertion.
CLK48	48 MHz	Main Clock Generator	Used by USB Controllers. Stopped in S3 ~ S5 based on SLP_S3# assertion.
CLK14	14.318 MHz	Main Clock Generator	Used by ACPI timers. Stopped in S3 ~ S5 based on SLP_S3# assertion.
AC_BIT_CLK	12.288 MHz	AC '97 Codec	AC '97 Link. Control policy is determined by the clock source.
APICCLK	16.67 MHz or 33 MHz	Main Clock Generator	Used for ICH3-processor interrupt messages. Should be running in C0, C1, and C2. Stopped in S3 ~ S5 based on SLP_S3# assertion.
LAN_CLK	0.8 to 50 MHz	LAN Connect	LAN Connect link. Control policy is determined by the clock source.

5.12.13 Legacy Power Management Theory of Operation

Instead of relying on ACPI software, legacy power management uses BIOS and various hardware mechanisms. ICH3 has a greatly simplified method for legacy power management compared with previous generations, such as the PIIX4.

The scheme relies on the concept of detecting when individual subsystems are idle, detecting when the whole system is idle, and detecting when accesses are attempted to idle subsystems.

However, the OS is assumed to be at least APM enabled. Without APM calls, there is no quick way to know when the system is idle between keystrokes. The ICH3 does not support the burst modes found in previous components (e.g., the PIIX4).

5.12.13.1 APM Power Management

The ICH3 has a timer that, when enabled by the 1MIN_EN bit in the SMI Control and Enable Register, will generate an SMI# once per minute. The SMI handler can check for system activity by reading the DEVACT_STS Register. If none of the system bits are set, the SMI handler can increment a software counter. When the counter reaches a sufficient number of consecutive minutes with no activity, the SMI handler can then put the system into a lower power state.

If there is activity, various bits in the DEVACT_STS Register will be set. Software clears the bits by writing a 1 to the bit position.

The DEVACT_STS Register allows for monitoring various internal devices, or Super I/O devices (SP, PP, FDC) on LPC or PCI, keyboard controller accesses, or audio functions on LPC or PCI. Other PCI activity can be monitored by checking the PCI interrupts.

5.13 System Management (D31:F0)

The ICH3 provides various functions to make a system easier to manage and to lower the Total Cost of Ownership (TCO) of the system. Features and functions can be augmented via external A/D converters and GPIO, as well as an external microcontroller.

The following features and functions are supported by the ICH3:

- Processor present detection.
  - — Detects if processor fails to fetch the first instruction after reset.
- Various Error detection (such as ECC Errors) Indicated by Host Controller
  - — Can generate SMI#, SCI, SERR, NMI, or TCO interrupt
- Intruder Detect input
  - — Can generate TCO interrupt or SMI# when the system cover is removed.
  - — INTRUDER# allowed to go active in any power state, including G3.
- Detection of bad FWH programming
  - — Detects if data on first read is FFh (indicates unprogrammed FWH)
- Ability to hide a PCI device
  - — Allows software to hide a PCI device in terms of configuration space through the use of a device hide register (See Section 8.1.26).

Note: Voltage ID from the processor can be read via GPI signals.

5.13.1 Theory of Operation

The System Management functions are designed to allow the system to diagnose failing subsystems. The intent of this logic is that some of the system management functionality be provided without the aid of an external microcontroller.

5.13.1.1 Detecting a System Lockup

When the processor is reset, it is expected to fetch its first instruction. If the processor fails to fetch the first instruction after reset, the TCO timer will timeout twice and the ICH3 will assert PCIRST#.

5.13.1.2 Handling an Intruder

The ICH3 has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a 2 RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCO_STS Register. The INTRD_SEL bits in the TCO_CNT Register can enable the ICH3 to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required.

If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET bit will go to a 0 when the INTRUDER# input signal goes inactive. Note that this is slilghtly different than a classic sticky bit, since most sticky bits would remain acctive indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

Note: The INTRD_DET bit resides in the ICH3's RTC well, and is set and cleared synchronously with the RTC clock. Thus, when software attempts to clear INTRD_DET (by writing a "1" to the bit location) there may be as much as 2 RTC clocks (about 65 µs) delay before the bit is actually cleared. Also, the INTRUDER# signal should be asserted for a minimum of 1 ms in order to guarantee that the INTRD_DET bit will be set.

Note: If the INTRUDER# signal is still active when software attempts to clear the INTRD_DET bit, the bit will remain set and the SMI will be generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signal goes inactive and then active again, there will not be further SMIs, since the INTRD_SEL bits would select that no SMI# be generated.

5.13.1.3 Detecting Improper FWH Programming

The ICH3 can detect the case where the FWH is not programmed. This will result in the first instruction fetched to have a value of FFh. If this occurs, the ICH3 will set the BAD_BIOS bit, which can then be reported via the Heartbeat and Event reporting using an external, Alert on LAN enabled LAN Controller (See Section 5.13.2).

5.13.1.4 Handling an ECC Error or Other Memory Error

The Host Controller provides a message to indicate that it would like to cause an SMI#, SCI, SERR#, or NMI. The software must check the Host Controller as to the exact cause of the error.

5.13.2 Alert on LAN*

The ICH3 integrated LAN controller supports Alert on LAN functionality when used with the 82562EM Platform LAN Connect component. This allows the integrated LAN controller to report messages to a network management console without the aid of the system processor. This is crucial in cases where the processor is malfunctioning or cannot function due to being in a low-power state.

The ICH3 also features an independent, dedicated SMBus interface, referred to as the SMLINK interface that can be used with an external Alert on LAN (or Alert on LAN 2*) enabled LAN Controller. This separate interface is required, since devices on the system SMBus will be powered down during some low power states.

The basic scheme is for the ICH3 integrated LAN Controller to send a prepared Ethernet message to a network management console. The prepared message is stored in the non-volatile EEPROM that is connected to the ICH3.

Messages are sent by the LAN Controller either because a specific event has occurred, or they are sent periodically (also known as a heartbeat). The event and heartbeat messages have the exact same format. The event messages are sent based on events occurring. The heartbeat messages are sent every 30 to 32 seconds. When an event occurs, the ICH3 sends a new message and increment the SEQ[3:0] field. For heartbeat messages the sequence number does not increment.

The following rules/steps apply if the system is in a G0 state and the policy is for the ICH3 **to reboot** the system after a hardware lockup:

1. Upon detecting the lockup the SECOND_TO_STS bit will be set. The ICH3 may send up to 1 Event message to the D110. The ICH3 will then attempt to reboot the processor.
2. If the reboot at step 1 is successful then the BIOS should clear the SECOND_TO_STS bit. This will prevent any further Heartbeats from being sent. The BIOS may then perform addition recovery/boot steps. (See note 2).
3. If the reboot attempt in step 1 is not successful, the timer will timeout a third time. At this point the system has locked up and was unsuccessful in rebooting. The ICH3 will not attempt to automatically reboot again. The ICH3 will start sending a message every heartbeat period (30–32 seconds). The heartbeats will continue until some external intervention occurs (reset, power failure, etc.).
4. After step 3 (unsuccessful reboot after third timeout), if the user does a Power Button Override, the system goes to an S5 state. The ICH3 continues sending the messages every heartbeat period.
5. After step 4 (power button override after unsuccessful reboot) if the user presses the Power Button again, the system should wake to an S0 state and the processor should start executing the BIOS.
6. If step 5 (power button press) is successful in waking the system, the ICH3 will continue sending messages every heartbeat period until the BIOS clears the SECOND_TO_STS bit. (See note 2).
7. If step 5 (power button press) is unsuccessful in waking the system, the ICH3 continues sending a message every heartbeat period. The ICH3 does not attempt to automatically reboot again. The ICH3 starts sending a message every heartbeat period (30–32 seconds). The heartbeats continue until some external intervention occurs (reset, power failure, etc.). (See note 3).
8. After step 3 (unsuccessful reboot after third timeout), if a reset is attempted (using a button that pulses PWROK low or via the message on the SMBus slave I/F), the ICH3 attempts to reset the system.
9. After step 8 (reset attempt) if the reset is successful, BIOS will be run. The ICH3 continues sending a message every heartbeat period until the BIOS clears the SECOND_TO_STS bit. (See note 2)
10. After step 8 (reset attempt), if the reset is unsuccessful, the ICH3 continues sending a message every heartbeat period. The ICH3 does not attempt to reboot the system again without external intervention. (See note 3).

The following rules/steps apply if the system is in a G0 state and the policy is for the ICH3 to **not reboot** the system after a hardware lockup.

1. Upon detecting the lockup, the SECOND_TO_STS bit is set. The ICH3 sends a message with the Watchdog (WD) Event status bit set (and any other bits that must also be set). This message is sent as soon as the lockup is detected and will be sent with the next (incremented) sequence number.
2. After step 1, the ICH3 sends a message every heartbeat period until some external intervention occurs.
3. Rules/steps 4–10 apply if no user intervention (resets, power button presses, SMBus reset messages) occur after a third timeout of the watchdog timer. If the intervention occurs before the third timeout, then jump to rule/step11.

4. After step 3 (third timeout), if the user does a Power Button Override, the system goes to an S5 state. The ICH3 continues sending heartbeats at this point.
5. After step 4 (power button override), if the user presses the power button again, the system should wake to an S0 state and the processor should start executing the BIOS.
6. If step 5 (power button press) is successful in waking the system, the ICH3 continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
7. If step 5 (power button press) is unsuccessful in waking the system, the ICH3 continues sending heartbeats. The ICH3 does not attempt to reboot the system again until some external intervention occurs (reset, power failure, etc.). (See note 3)
8. After step 3 (third timeout), if a reset is attempted (using a button that pulses PWROK low or via the message on the SMBus slave I/F), the ICH3 attempts to reset the system.
9. If step 8 (reset attempt) is successful, BIOS is run. The ICH3 continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
10. If step 8 (reset attempt), is unsuccessful, then the ICH3 continues sending heartbeats. The ICH3 does not attempt to reboot the system again without external intervention.
    Note: A system that has locked up and can not be restarted with power button press is probably very broken (bad power supply, short circuit on some bus, etc.)
11. This and the following rules/steps apply if the user intervention (power button press, reset, SMBus message, etc.) occur prior to the third timeout of the watchdog timer.
12. After step 1 (second timeout), if the user does a Power Button Override, the system goes to an S5 state. The ICH3 continues sending heartbeats at this point.
13. After step 12 (power button override), if the user presses the power button again, the system should wake to an S0 state and the processor should start executing the BIOS.
14. If step 13 (power button press) is successful in waking the system, the ICH3 continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
15. If step 13 (power button press) is unsuccessful in waking the system, the ICH3 continues sending heartbeats. The ICH3 does not attempt to reboot the system again until some external intervention occurs (reset, power failure, etc.). (See note 3)
16. After step 1 (second timeout), if a reset is attempted (using a button that pulses PWROK low or via the message on the SMBus slave I/F), the ICH3 attempts to reset the system.
17. If step 16 (reset attempt) is successful, BIOS is run. The ICH3 continues sending heartbeats until the BIOS clears the SECOND_TO_STS bit. (See note 2)
18. If step 16 (reset attempt), is unsuccessful, the ICH3 continues sending heartbeats. The ICH3 does not attempt to reboot the system again without external intervention. (See note 3).

If the system is in a G1 (S1–S4) state the ICH3 sends a heartbeat message every 30–32 seconds. If an event occurs prior to the system being shutdown, the ICH3 immediately sends an event message with the next incremented sequence number. After the event message the ICH3 resumes sending heartbeat messages.

Note:

1. Normally, the ICH3 does not send heartbeat messages while in the G0 state (except in the case of a lockup). However, if a hardware event (or heartbeat) occurs just as the system is transitioning into a G0 state, the hardware continues to send the message even though the system will be in a G0 state (and the status bits may indicate this).

   When used with an external Alert on LAN enabled LAN controller, the ICH3 sends these messages via the SMLINK signals. When sending messages via these signals, the ICH3 abides

by the SMBus rules associated with collision detection. It delays starting a message until the bus is idle, and detects collisions. If a collision is detected the ICH3 waits until the bus is idle, and tries again.

2. **WARNING:** It is important the BIOS clears the SECOND_TO_STS bit, as the alerts will interfere with the LAN device driver from working properly. The alerts reset part of the D110 and would prevent an OS's device driver from sending or receiving some messages.
3. A system that has locked up and cannot be restarted with power button press is assumed to have broken hardware (bad power supply, short circuit on some bus, etc.), and is beyond ICH3's recovery mechanisms.
4. A spurious alert could occur in the following sequence:
   — The processor has initiated an alert using the SEND_NOW bit
   — During the alert, the THRM#, INTRUDER# or GPI[11] changes state
   — The system then goes to a non-S0 state.

   Once the system transitions to the non-S0 state, it may send a single alert with an incremental SEQUENCE number.
5. An inaccurate alert message can be generated in the following scenario
   — The system successfully boots after a second watchdog Timeout occurs.
   — PWROK goes low (typically due to a reset button press) or a power button override occurs (before the SECOND_TO_STS bit is cleared).
   — An alert message indicating that the processor is missing or locked up is generated with a new sequence number.

Table 5-50 shows the data included in the Alert on LAN messages.

Table 5-50. Alert on LAN* Message Data

Field	Comment
Cover Tamper Status	1 = This bit will be set if the intruder detect bit is set (INTRD_DET).
Temp Event Status	1 = This bit will be set if the ICH3 THERM# input signal is asserted.
CPU Missing Event Status	1 = This bit will be set if the processor failed to fetch the first instruction.
TCO Timer Event Status	1 = This bit is set when the TCO timer expires.
Software Event Status	1 = This bit is set when software writes a 1 to the SEND_NOW bit.
Unprogrammed FWH Event Status	1 = First BIOS fetch returned a value of FFh, indicating that the FWH has not yet been programmed (still erased).
GPIO Status	1 = This bit is set when GPIO[11] signal is high. 0 = This bit is cleared when GPIO[11] signal is low. An event message is triggered on an transition of GPIO[11].
SEQ[3:0]	This is a sequence number. It will initially be 0, and will increment each time the ICH3 sends a new message. Upon reaching 1111, then the sequence number will roll over to 0000. MSB (SEQ3) sent first.
System Power State	00 = G0, 01 = G1, 10 = G2, 11 = Pre-Boot. MSB sent first
MESSAGE1	Will be the same as the MESSAGE1 register. MSB sent first.
MESSAGE2	Will be the same as the MESSAGE2 register. MSB sent first.
WDSTATUS	Will be the same as the WDSTATUS register. MSB sent first.

5.14 General Purpose I/O

5.14.1 GPIO Mapping

Table 5-51. GPIO(s) Mapping

Name/ Muxed Function	Usage	Muxed	I/O	Pwr Plan	Tolerant	Wake Event Support	Wake from State	After RSMRST#	After PCIRST#
GPI[0] / REQ[A]#	REQ[A] for PC/PCI header	Yes	I	Core	5.0 V	Wake / SMI# / SCI	S1		[2]
GPI[1] / REQ[B]#/ REQ[5]#	REQ[5]# for 6th PCI device	Yes	I	Core	5.0 V	Wake / SMI# / SCI	S1		[2]
GPI[2] / PIRQE#	PIRQ[E] will be routed internally when this pin is used as GPIO[x]	Yes	I	Core	5.0 V	Wake / SMI# / SCI	S1		[2]
GPI[3] / PIRQF#	PIRQ[F] will be routed internally when this pin is used as GPIO[x]	Yes	I	Core	5.0 V	Wake / SMI# / SCI	S1		[2]
GPI[4] / PIRQG#	PIRQ[G] will be routed internally when this pin is used as GPIO[x]	Yes	I	Core	5.0 V	Wake / SMI# / SCI	S1		[2]
GPI[5] / PIRQH#	PIRQ[H] will be routed internally when this pin is used as GPIO[x]	Yes	I	Core	5.0 V	Wake / SMI# / SCI	S1		[2]
GPI[7]	If this pin is unused, then it should not matter which level is considered active. An external pull up or down resister is required.	No	I	Core	5.0 V	Wake / SMI# / SCI	S1		—
GPI[8]	If this pin is unused, then it should not matter which level is considered active. An external pull up/down resister is required.	No	I	Resume	3.3 V	Wake / SMI# / SCI	S1–S5	High	—
GPI[11] / SMBALERT#	In heartbeat mode (G1 or hung-G0), this pin will trigger an event (detected via a transition) and send out the alert message, regardless it is programmed as GPIO or not.	Yes	I	Resume	3.3 V	Wake / SMI# / SCI	S1–S5	High	—
GPI[12]		No	I	Resume	3.3 V	Wake / SMI# / SCI	S1–S5	Defined	—
GPI[13]		No	I	Resume	3.3 V	Wake / SMI# / SCI	S1–S5	Defined	—
GPO[16] / GNT[A]#	GNT[A] for PC/PCI header	Yes	O	Core	5.0 V	—	—	High[2]	High[2]
GPO[17] / GNT[B]# / GNT[5]#	GNT[5]# for 6th PCI device	Yes	O	Core	5.0 V	—	—	High[2]	High[2]

Table 5-51. GPIO(s) Mapping (Continued)

Name/ Muxed Function	Usage	Muxed	I/O	Pwr Plan	Tolerant	Wake Event Support	Wake from State	After RSMRST#	After PCIRST#
GPO[21]	(D) uses as NOGO signal to prevent the subtractive decode cycle.	Yes	O	Core	5.0 V	—	—	High	High
GPIO[25]		No	I/[O]	Resume	3.3 V	—	—	High	High
GPIO[27]		No	I/[O]	Resume	3.3 V	—	—	High	High-Z High
GPIO[28]		No	I/[O]	Resume	3.3 V	—	—	High	High-Z High
GPIO[32]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[33]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[34]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[35]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[36]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[37]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[38]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[39]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[40]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[41]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[42]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[43]		Yes	I/[O]	Core	3.3 V	—	—	[2]	High
GPIO[9]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[10]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[14]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[15]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[26]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[29]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[30]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[31]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[44]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[45]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[46]	(not implemented)	—	—	—	—	—	—	—	—
GPIO[47]	(not implemented)	—	—	—	—	—	—	—	—

NOTE:
1. [x] = default
2. After a reset, all multiplexed GPIOs on the core and resume wells are configured as their native function rather than as a GPIO
3. A= Amber color LED, G= Green color LED
   - Both off: USB disconnected, disable or not configured
   - Amber Only: Error condition
   - Green Only: Fully operational
   - Amber Blinking, Green Off: Software attention

5.14.2 Power Wells

Some GPIOs exist in the resume power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes.

Some ICH3 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the ICH3 driving a pin to a logic “1” to another device that is powered down.

5.14.3 SMI# and SCI Routing

The routing bits for GPIO[0:15] allow an input to be routed to SMI# or SCI, or neither. Note that a bit can be routed to either an SMI# or an SCI, but not both.

5.14.4 Power Wells

GPIO[1:15] have “sticky” bits on the input. Refer to the GPE1_STS Register. As long as the signal goes active for at least 2 clocks, the ICH3 will keep the sticky status bit active. The active level can be selected in the GP_LVL Register.

If the system is in an S0 or an S1-D state, the GPI inputs are sampled at 33 MHz, so the signal only needs to be active for about 60 ns to be latched. In the S1-M or S3–S5 states, the GPI inputs are sampled at 32.768 kHz, and thus must be active for at least 61 microseconds to be latched.

If the input signal is still active when the latch is cleared, it will again be set. Another edge trigger is not required. This makes these signals “level” triggered inputs.

5.15 IDE Controller (D31:F1)

The ICH3 IDE controller features two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated or driven low.

The ICH3 IDE controller supports both legacy mode and native mode IDE interface. In native mode, the IDE controller is a fully PCI compliant software interface and does not use any legacy I/O or interrupt resources.

The IDE interfaces of the ICH3 can support several types of data transfers:

- **Programmed I/O (PIO):** Processor is in control of the data transfer.
- **Intel 8237 style DMA:** DMA protocol that resembles the DMA on the ISA bus, although it does not use the 8237 in the ICH3. This protocol off loads the processor from moving data. This allows higher transfer rate of up to 16 MB/s.
- **Ultra ATA/33:** DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 33 MB/s.
- **Ultra ATA/66:** DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 66 MB/s.
- **Ultra ATA/100:** DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s.

5.15.1 PIO Transfers

The ICH3 IDE controller includes both compatible and fast timing modes. The fast timing modes can be enabled only for the IDE data ports. All other transactions to the IDE registers are run in single transaction mode with compatible timings.

Up to 2 IDE devices may be attached per IDE connector (drive 0 and drive 1). The IDETIM and SIDETIM Registers permit different timing modes to be programmed for drive 0 and drive 1 of the same connector.

The Ultra ATA/33/66/100 synchronous DMA timing modes can also be applied to each drive by programming the IDE I/O configuration register and the synchronous DMA control and timing registers. When a drive is enabled for synchronous DMA mode operation, the DMA transfers are executed with the synchronous DMA timings. The PIO transfers are executed using compatible timings or fast timings if also enabled.

5.15.1.1 IDE Port Decode

The command and control block registers are accessed differently depending on the decode mode, which is selected by the programming interface configuration register (Offset 09h).

Note: The primary and secondary channels are controlled by separate bits, allowing one to be in native mode and the other in legacy mode simultaneously.

5.15.1.2 IDE Legacy Mode and Native Mode

The ICH3 IDE controller supports both legacy mode and PCI native mode. In legacy mode, the command and control block registers are accessible at fixed I/O addresses. While in legacy mode, the ICH3 will not decode any of the native mode ranges. Likewise, in native mode the ICH3 will not decode any of the legacy mode ranges

The IDE I/O ports involved in PIO transfers are decoded by the ICH3 to the IDE interface when D31:F1 I/O space is enabled and IDE decode is enabled through the IDE_TIMx Registers. The IDE registers are implemented in the drive itself. An access to the IDE registers results in the assertion of the appropriate IDE chip select for the register, and the IDE command strobes (PDIOR#/ SDIOR#, PDIOW#/SDIOW#).

There are two I/O ranges for each IDE cable: the Command Block, which corresponds to the PCS1#/SCS1# chip select, and the Control Block, which corresponds to the PCS3#/SCS3# chip select. The Command Block is an 8-byte range, while the control block is a 4-byte range.

- **Command Block Offset:** 01F0h for Primary, 0170h for Secondary
- **Control Block Offset:** 03F4h for Primary, 0374h for Secondary

Table 5-52 and Table 5-53 specify the registers as they affect the ICH3 hardware definition.

Note: The data register (I/O Offset 00h) should be accessed using 16-bit or 32-bit I/O instructions. All other registers should be accessed using 8-bit I/O instructions.

Table 5-52. IDE Legacy I/O Ports: Command Block Registers (CS1x# Chip Select)

I/O Offset	Register Function (Read)	Register Function (Write)
00h	Data	Data
01h	Error	Features
02h	Sector Count	Sector Count
03h	Sector Number	Sector Number
04h	Cylinder Low	Cylinder Low
05h	Cylinder High	Cylinder High
06h	Drive	Head
07h	Status	Command

Table 5-53. IDE Legacy I/O Ports: Control Block Registers (CS3x# Chip Select)

I/O Offset	Register Function (Read)	Register Function (Write)
00h	Reserved	Reserved
01h	Reserved	Reserved
02h	Alt Status	Device control
03h	Forward to LPC–Not claimed by IDE	Forward to LPC–Not claimed by IDE

NOTE: For accesses to the alt status register in the Control Block, the ICH3 must always force the upper address bit (PDA[2] or SDA[2]) to 1 in order to guarantee proper native mode decode by the IDE device. Unlike the legacy mode fixed address location, the native mode address for this register may contain a 0 in address bit 2 when it is received by the ICH3

In native mode, the ICH3 does not decode the legacy ranges. The same offsets are used as in Table 5-52 and Table 5-53 above. However, the base addresses are selected using the PCI BARs, rather than fixed I/O locations.

5.15.1.3 PIO IDE Timing Modes

IDE data port transaction latency consists of startup latency, cycle latency, and shutdown latency.

Startup latency is incurred when a PCI master cycle targeting the IDE data port is decoded and the DA[2:0] and CSxx# lines are not set up. Startup latency provides the setup time for the DA[2:0] and CSxx# lines prior to assertion of the read and write strobes (DIOR# and DIOW#).

Cycle latency consists of the I/O command strobe assertion length and recovery time. Recovery time is provided so that transactions may occur back-to-back on the IDE interface (without incurring startup and shutdown latency) without violating minimum cycle periods for the IDE interface. The command strobe assertion width for the enhanced timing mode is selected by the IDE_TIM Register and may be set to 2, 3, 4, or 5 PCI clocks. The recovery time is selected by the IDE_TIM Register and may be set to 1, 2, 3, or 4 PCI clocks.

If IORDY is asserted when the initial sample point is reached, no wait-states are added to the command strobe assertion length. If IORDY is negated when the initial sample point is reached, additional wait-states are added. Since the rising edge of IORDY must be synchronized, at least two additional PCI clocks are added.

Shutdown latency is incurred after outstanding scheduled IDE data port transactions (either a non-empty write post buffer or an outstanding read prefetch cycles) have completed and before other transactions can proceed. It provides hold time on the DA[2:0] and CSxx# lines with respect to the read and write strobes (DIOR# and DIOW#). Shutdown latency is 2 PCI clocks in duration.

The IDE timings for various transaction types are shown in Table 5-54. Note that bit 2 (16-bit I/O recovery enable) of the ISA I/O recovery timer register does not add wait-states to IDE data port read accesses when any of the fast timing modes are enabled.

Table 5-54. IDE Transaction Timings (PCI Clocks)

IDE Transaction Type	Startup Latency	IORDY Sample Point (ISP)	Recovery Time (RCT)	Shutdown Latency
Non-Data Port Compatible	4	11	22	2
Data Port Compatible	3	6	14	2
Fast Timing Mode	2	2–5	1–4	2

5.15.1.4 IORDY Masking

The IORDY signal can be ignored and assumed asserted at the first IORDY Sample Point (ISP) on a drive by drive basis via the IDETIM Register.

5.15.1.5 PIO 32-Bit IDE Data Port Accesses

A 32-bit PCI transaction run to the IDE data address (01F0h primary, 0170h secondary) results in two back-to-back 16-bit transactions to the IDE data port. The 32-bit data port feature is enabled for all timings, not just enhanced timing. For compatible timings, a shutdown and startup latency is incurred between the two 16-bit halves of the IDE transaction. This guarantees that the chip selects will be deasserted for at least 2 PCI clocks between the two cycles.

5.15.1.6 PIO IDE Data Port Prefetching and Posting

The ICH3 can be programmed via the IDETIM registers to allow data to be posted to and prefetched from the IDE data ports.

Data pre fetching is initiated when a data port read occurs. The read prefetch eliminates latency to the IDE data ports and allows them to be performed back to back for the highest possible PIO data transfer rates. The first data port read of a sector is called the demand read. Subsequent data port reads from the sector are called prefetch reads. The demand read and all prefetch reads much be of the same size (16 or 32 bits).

Data posting is performed for writes to the IDE data ports. The transaction is completed on the PCI bus after the data is received by the ICH3. The ICH3 will then run the IDE cycle to transfer the data to the drive. If the ICH3 write buffer is non-empty and an unrelated (non-data or opposite channel) IDE transaction occurs, that transaction will be stalled until all current data in the write buffer is transferred to the drive.

5.15.2 Bus Master Function

The ICH3 can act as a PCI Bus master on behalf of an IDE slave device. Two PCI Bus master channels are provided, one channel for each IDE connector (primary and secondary). By performing the IDE data transfer as a PCI Bus master, the ICH3 off-loads the processor and improves system performance in multitasking environments. Both devices attached to a connector can be programmed for bus master transfers, but only one device per connector can be active at a time.

5.15.2.1 Physical Region Descriptor Format

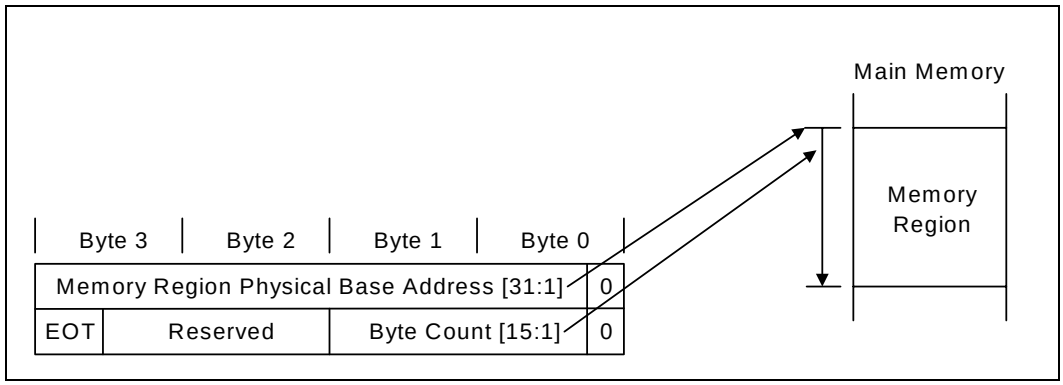
The physical memory region to be transferred is described by a Physical Region Descriptor (PRD). The PRDs are stored sequentially in a Descriptor Table in memory. The data transfer proceeds until all regions described by the PRDs in the table have been transferred. Note that the ICH3 bus master IDE function does not support memory regions or Descriptor tables located on ISA.

Descriptor Tables must not cross a 64-KB boundary. Each PRD entry in the table is 8 bytes in length. The first 4 bytes specify the byte address of a physical memory region. This memory region must be dword-aligned and must not cross a 64-KB boundary. The next two bytes specify the size or transfer count of the region in bytes (64-KB limit per region). A value of zero in these two bytes indicates 64 KB (thus the minimum transfer count is 1). If bit 7 (EOT) of the last byte is a 1, it indicates that this is the final PRD in the Descriptor table. Bus master operation terminates when the last descriptor has been retired.

When the Bus Master IDE controller is reading data from the memory regions, bit 1 of the Base Address is masked and byte enables are asserted for all read transfers. When writing data, bit 1 of the Base Address is not masked and if set, will cause the lower WORD byte enables to be deasserted for the first dword transfer. The write to PCI will typically consist of a 32-byte cache line. If valid data ends prior to end of the cache line, the byte enables will be deasserted for invalid data.

The total sum of the byte counts in every PRD of the descriptor table must be equal to or greater than the size of the disk transfer request. If greater than the disk transfer request, the driver must terminate the bus master transaction (by setting bit 0 in the Bus Master IDE Command Register to 0) when the drive issues an interrupt to signal transfer completion.

Figure 5-14. Physical Region Descriptor Table Entry



A single line buffer exists for the ICH3 Bus master IDE interface. This buffer is not shared with any other function. The buffer is maintained in either the read state or the write state. Memory writes are typically 4-dword bursts and invalid dwords have C/BE[3:0]#=0Fh. The line buffer allows burst data transfers to proceed at peak transfer rates.

The bus master IDE active bit in Bus Master IDE Status Register is reset automatically when the controller has transferred all data associated with a Descriptor Table (as determined by EOT bit in last PRD). The IDE interrupt status bit is set when the IDE device generates an interrupt. These events may occur prior to line buffer emptying for memory writes. If either of these conditions exist, all PCI Master non-Memory read accesses to ICH3 are retried until all data in the line buffers has been transferred to memory.

5.15.2.2 Bus Master IDE Timings

The timing modes used for Bus Master IDE transfers are identical to those for PIO transfers. The DMA Timing Enable Only bits in the IDE Timing Register can be used to program fast timing mode for DMA transactions only. This is useful for IDE devices whose DMA transfer timings are faster that its PIO transfer timings. The IDE device DMA request signal is sampled on the same PCI clock that DIOR# or DIOW# is deasserted. If inactive, the DMA Acknowledge signal is deasserted on the next PCI clock and no more transfers take place until DMA request is asserted again.

5.15.2.3 Interrupts

Legacy Mode

The ICH3 is connected to IRQ14 for the primary interrupt and IRQ15 for the secondary interrupt. This connection is done from the ISA pin, before any mask registers. This implies the following:

- Bus Master IDE devices are connected directly off of ICH3. IDE interrupts cannot be communicated through PCI devices or the serial stream.

Warning: In this mode, the ICH3 will not drive the PCI Interrupt associated with this function. That is only used in native mode.

Native Mode

In this case both the Primary and Secondary channels share an interrupt. It will be internally connected to PIRQ[C]# (IRQ18 in APIC mode).
The interrupt will be active-low and shared.

Behavioral notes in native mode:

- The IRQ14 and IRQ15 pins do not affect the internal IRQ14 and IRQ15 inputs to the interrupt controllers. The IDE logic forces these signals inactive in such a way that the Serial IRQ source may be used.
- The IRQ14 and IRQ15 inputs (not external IRQ[14:15] pins) to the interrupt controller can come from other sources (Serial IRQ, PIRQx).
- The IRQ14 and IRQ15 pins are inverted from active-high to the active-low PIRQ.
- When switching the IDE controller to native mode, the IDE Interrupt Pin Register (see Section 11.1.16) will be masked. If an interrupt occurs while the masking is in place and the interrupt is still active when the masking ends, the interrupt will be allowed to be asserted.*

5.15.2.4 Bus Master IDE Operation

To initiate a bus master transfer between memory and an IDE device, the following steps are required:

1. Software prepares a PRD Table in system memory. The PRD Table must be dword aligned and must not cross a 64-Kbyte boundary.
2. Software provides the starting address of the PRD Table by loading the PRD table pointer register. The direction of the data transfer is specified by setting the read/write control bit. The interrupt bit and error bit in the status register are cleared.
3. Software issues the appropriate DMA transfer command to the disk device.
4. The bus master function is engaged by software writing a '1' to the start bit in the command register. The first entry in the PRD table is fetched and loaded into two registers which are not visible by software, the current base and current count registers. These registers hold the current value of the address and byte count loaded from the PRD table. The value in these registers is only valid when there is an active command to an IDE device.
5. Once the PRD is loaded internally, the IDE device will receive a DMA acknowledge.
6. The controller transfers data to/from memory responding to DMA requests from the IDE device. The IDE device and the host controller may or may not throttle the transfer several times. When the last data transfer for a region has been completed on the IDE interface, the next descriptor is fetched from the table. The descriptor contents are loaded into the current base and current count registers.
7. At the end of the transfer the IDE device signals an interrupt.
8. In response to the interrupt, software resets the start/stop bit in the command register. It then reads the controller status followed by the drive status to determine if the transfer completed successfully.

The last PRD in a table has the End of List (EOL) bit set. The PCI bus master data transfers terminate when the physical region described by the last PRD in the table has been completely transferred. The active bit in the status register will be reset and the DDRQ signal will be masked.

The buffer is flushed (when in the write state) or invalidated (when in the read state) when a terminal count condition exists; that is, the current region descriptor has the EOL bit set and that region has been exhausted. The buffer is also flushed (write state) or invalidated (read state) when the interrupt bit in the Bus Master IDE Status Register is set. Software that reads the status register and finds the error bit reset, and either the active bit reset or the interrupt bit set, can be assured that all data destined for system memory has been transferred and that data is valid in system memory. Table 5-55 describes how to interpret the interrupt and active bits in the status register after a DMA transfer has started.

During concurrent DMA or Ultra ATA transfers, the ICH3 IDE interface will arbitrate between the primary and secondary IDE cables when a PRD expires.

Table 5-55. Interrupt/Active Bit Interaction Definition

Interrupt	Active	Description
0	1	DMA transfer is in progress. No interrupt has been generated by the IDE device.
1	0	The IDE device generated an interrupt. The controller exhausted the Physical Region Descriptors. This is the normal completion case where the size of the physical memory regions was equal to the IDE device transfer size.
1	1	The IDE device generated an interrupt. The controller has not reached the end of the physical memory regions. This is a valid completion case where the size of the physical memory regions was larger than the IDE device transfer size.
0	0	This bit combination signals an error condition. If the error bit in the status register is set, then the controller has some problem transferring data to/from memory. Specifics of the error have to be determined using bus-specific information. If the error bit is not set, then the PRD's specified a smaller size than the IDE transfer size.

5.15.2.5 Error Conditions

IDE devices are sector based mass storage devices. The drivers handle errors on a sector basis; either a sector is transferred successfully or it is not. A sector is 512 bytes.

If the IDE device does not complete the transfer due to a hardware or software error, the command will eventually be stopped by the driver setting command start bit to zero when the driver times out the disk transaction. Information in the IDE device registers help isolate the cause of the problem.

If the controller encounters an error while doing the bus master transfers, it will stop the transfer (i.e., reset the active bit in the command register) and set the error bit in the Bus Master IDE Status Register. The controller does not generate an interrupt when this happens. The device driver can use device specific information (PCI configuration space status register and IDE drive register) to determine what caused the error.

When a requested transfer does not complete properly, information in the IDE device registers (Sector Count) can be used to determine how much of the transfer was completed and to construct a new PRD table to complete the requested operation. In most cases the existing PRD table can be used to complete the operation.

5.15.2.6 Intel® 8237-Like Protocol

Intel 8237 mode DMA is similar in form to DMA used on the ISA bus. This mode uses pins familiar to the ISA bus, namely a DMA Request, a DMA Acknowledge, and I/O read/write strobes. These pins have similar characteristics to their ISA counterparts in terms of when data is valid relative to strobe edges, and the polarity of the strobes, however the ICH3 does not use the 8237 for this mode.

5.15.3 Ultra ATA/33 Protocol

Ultra ATA/33 is enabled through configuration register 48h in Device 31:Function 1 for each IDE device. The IDE signal protocols are significantly different under this mode than for the 8237 mode.

Ultra ATA/33 is a physical protocol used to transfer data between a Ultra ATA/33 capable IDE controller such as the ICH3 and one or more Ultra ATA/33 capable IDE devices. It utilizes the standard Bus Master IDE functionality and interface to initiate and control the transfer. Ultra ATA/33 utilizes a “source synchronous” signaling protocol to transfer data at rates up to 33 MB/s. The Ultra ATA/33 definition also incorporates a Cyclic Redundancy Checking (CRC-16) error checking protocol.

5.15.3.1 Signal Descriptions

The Ultra ATA/33 protocol requires no extra signal pins on the IDE connector. It does redefine a number of the standard IDE control signals when in Ultra ATA/33 mode. These redefinitions are shown in the following table. Read cycles are defined as transferring data from the IDE device to the ICH3. Write cycles are defined as transferring data from ICH3 to IDE device.

Table 5-56. UltraATA/33 Control Signal Redefinitions

Standard IDE Signal Definition	Ultra ATA/33 Read Cycle Definition	Ultra ATA/33 Write Cycle Definition	ICH3 Primary Channel Signal	ICH3 Secondary Channel Signal
DIOW#	STOP	STOP	PDIOW#	SDIOW#
DIOR#	DMARDY#	STROBE	PDIOR#	SDIOR#
IORDY	STROBE	DMARDY#	PIORDY	SIORDY

The DIOW# signal is redefined as STOP for both read and write transfers. This is always driven by the ICH3 and is used to request that a transfer be stopped or as an acknowledgment to stop a request from the IDE device.

The DIOR# signal is redefined as DMARDY# for transferring data from the IDE device to the ICH3 (read). It is used by the ICH3 to signal when it is ready to transfer data and to add wait-states to the current transaction. The DIOR# signal is redefined as STROBE for transferring data from the ICH3 to the IDE device (write). It is the data strobe signal driven by the ICH3 on which data is transferred during each rising and falling edge transition.

The IORDY signal is redefined as STROBE for transferring data from the IDE device to the ICH3 (read). It is the data strobe signal driven by the IDE device on which data is transferred during each rising and falling edge transition. The IORDY signal is redefined as DMARDY# for transferring data from the ICH3 to the IDE device (write). It is used by the IDE device to signal when it is ready to transfer data and to add wait-states to the current transaction.

All other signals on the IDE connector retain their functional definitions during Ultra ATA/33 operation.

5.15.3.2 Operation

Initial setup programming consists of enabling and performing the proper configuration of ICH3 and the IDE device for Ultra ATA/33 operation. For ICH3, this consists of enabling Synchronous DMA mode and setting up appropriate Synchronous DMA timings.

When ready to transfer data to or from an IDE device, the Bus Master IDE programming model is followed. Once programmed, the drive and ICH3 control the transfer of data via the Ultra ATA/33 protocol. The actual data transfer consists of three phases, a start-up phase, a data transfer phase, and a burst termination phase.

The IDE device begins the start-up phase by asserting DMARQ signal. When ready to begin the transfer, the ICH3 will assert DMACK# signal. When DMACK# signal is asserted, the host controller will drive CS0# and CS1# inactive, DA0-DA2 low. For write cycles, the ICH3 will deassert STOP, wait for the IDE device to assert DMARDY#, and then drive the first data word and STROBE signal. For read cycles, the ICH3 will tri-state the DD lines, deassert STOP, and assert DMARDY#. The IDE device will then send the first data word and STROBE.

The data transfer phase continues the burst transfers with the data transmitter (ICH3–writes, IDE device - reads) providing data and toggling STROBE. Data is transferred (latched by receiver) on each rising and falling edge of STROBE. The transmitter can pause the burst by holding STROBE high or low, resuming the burst by again toggling STROBE. The receiver can pause the burst by deasserting DMARDY# and resumes the transfers by asserting DMARDY#. The ICH3 will pause a burst transaction in order to prevent an internal line buffer over or under flow condition, resuming once the condition has cleared. It may also pause a transaction if the current PRD byte count has expired, resuming once it has fetched the next PRD.

The current burst can be terminated by either the transmitter or receiver. A burst termination consists of a Stop Request, Stop Acknowledge and transfer of CRC data. The ICH3 can stop a burst by asserting STOP, with the IDE device acknowledging by deasserting DMARQ. The IDE device stops a burst by deasserting DMARQ and the ICH3 acknowledges by asserting STOP. The transmitter then drives the STROBE signal to a high level. The ICH3 will then drive the CRC value onto the DD lines and deassert DMACK#. The IDE device will latch the CRC value on rising edge of DMACK#. The ICH3 will terminate a burst transfer if it needs to service the opposite IDE channel, if a Programmed I/O (PIO) cycle is executed to the IDE channel currently running the burst, or upon transferring the last data from the final PRD.

5.15.3.3 CRC Calculation

Cyclic Redundancy Checking (CRC-16) is used for error checking on Ultra ATA/33 transfers. The CRC value is calculated for all data by both the ICH3 and the IDE device over the duration of the Ultra ATA/33 burst transfer segment. This segment is defined as all data transferred with a valid STROBE edge from DDACK# assertion to DDACK# deassertion. At the end of the transfer burst segment, the ICH3 will drive the CRC value onto the DD[15:0] signals. It is then latched by the IDE device on deassertion of DDACK#. The IDE device compares the ICH3 CRC value to its own and reports an error if there is a mismatch.

5.15.4 Ultra ATA/66 Protocol

In addition to Ultra ATA/33, the ICH3 supports the Ultra ATA/66 protocol. The Ultra ATA/66 protocol is enabled via configuration bits 3:0 at offset 54h. The two protocols are similar, and are intended to be device driver compatible. The Ultra ATA/66 logic can achieve transfer rates of up to 66 MB/s.

In order to achieve the higher data rate, the timings are shortened and the quality of the cable is improved to reduce reflections, noise, and inductive coupling. Note that the improved cable is required and will still plug into the standard IDE connector.

The Ultra ATA/66 protocol also supports a 44 MB/s mode.

5.15.5 Ultra ATA/100 Protocol

When the ATA_FAST bit is set for any of the 4 IDE devices, then the timings for the transfers to and from the corresponding device run at a higher rate. The ICH3 Ultra ATA/100 logic can achieve read transfer rates up to 100 MB/s, and write transfer rates up to 88.9 MB/s.

The cable improvements required for Ultra ATA/66 are sufficient for Ultra ATA/100, so no further cable improvements are required when implementing Ultra ATA/100.

5.15.6 Ultra ATA/33/66/100 Timing

The timings for Ultra ATA/33/66/100 modes are programmed via the synchronous DMA Timing Register and the IDE configuration register. Different timings can be programmed for each drive in the system. The Base Clock frequency for each drive is selected in the IDE configuration register. The Cycle Time (CT) and Ready to Pause (RP) time (defined as multiples of the Base Clock) are programmed in the synchronous DMA timing register. The Cycle Time represents the minimum pulse width of the data strobe (STROBE) signal. The Ready to Pause time represents the number of Base Clock periods that the ICH3 will wait from deassertion of DMARDY# to the assertion of STOP when it desires to stop a burst read transaction.

Note: The internal Base Clock for Ultra ATA/100 (Mode 5) runs at 133 MHz, and the Cycle Time (CT) must be set for 3 Base Clocks. The ICH3 will thus toggle the write strobe signal every 22.5 ns, transferring two bytes of data on each strobe edge. This means that the ICH3 will perform Mode 5 write transfers at a maximum rate of 88.9 MB/s. For read transfers, the read strobe will be driven by the ATA/100 device, and the ICH3 supports reads at the maximum rate of 100 MB/s.

5.16 USB 1.1 Controllers (D29:F0, F1 and F2)

The ICH3 contains three USB 1.1 Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of six USB ports. The ICH3 Host Controllers support the standard *Universal Host Controller Interface (UHCI) Design Guide*, Revision 1.1 (http://developer.intel.com/design/USB/UHCI11D.htm).

Overcurrent detection on all six USB ports is supported. The overcurrent inputs are 5 V-tolerant, and can be used as GPIs if not needed.

The ICH3's USB 1.1 controllers are arbitrated as differently than standard PCI devices to improve arbitration latency.

The USB 1.1 controllers use the Analog Front End (AFE) embedded cell instead of USB I/O buffers.

5.16.1 Data Structures in Main Memory

This section describes the details of the data structures used to communicate control, status, and data between software and the ICH3: Frame Lists, Transfer Descriptors, and Queue Heads. Frame Lists are aligned on 4-KB boundaries. Transfer Descriptors and Queue Heads are aligned on 16-byte boundaries.

5.16.1.1 Frame List Pointer

The frame list pointer contains a link pointer to the first data object to be processed in the frame, as well as the control bits defined in Table 5-57.

Table 5-57. Frame List Pointer Bit Description

Bit	Description
31:4	**Frame List Pointer (FLP).** This field contains the address of the first data object to be processed in the frame and corresponds to memory address signals [31:4], respectively.
3:2	Reserved. These bits must be written as 0.
1	**QH/TD Select (Q).** This bit indicates to the hardware whether the item referenced by the link pointer is a TD (Transfer Descriptor) or a QH (Queue Head). This allows the ICH3 to perform the proper type of processing on the item after it is fetched. 0 = TD 1 = QH
0	**Terminate (T).** This bit indicates to the ICH3 whether the schedule for this frame has valid entries in it. 0 = Pointer is valid (points to a QH or TD). 1 = Empty Frame (pointer is invalid).

5.16.1.2 Transfer Descriptor (TD)

Transfer Descriptors (TDs) express the characteristics of the transaction requested on USB by a client. TDs are always aligned on 16-byte boundaries, and the elements of the TD are shown in Figure 5-15. The four different USB transfer types are supported by a small number of control bits in the descriptor that the ICH3 interprets during operation. All Transfer Descriptors have the same basic, 32-byte structure. During operation, the ICH3 hardware performs consistency checks on some fields of the TD. If a consistency check fails, the ICH3 halts immediately and issues an interrupt to the system. This interrupt cannot be masked within the ICH3.

Figure 5-15. Transfer Descriptor

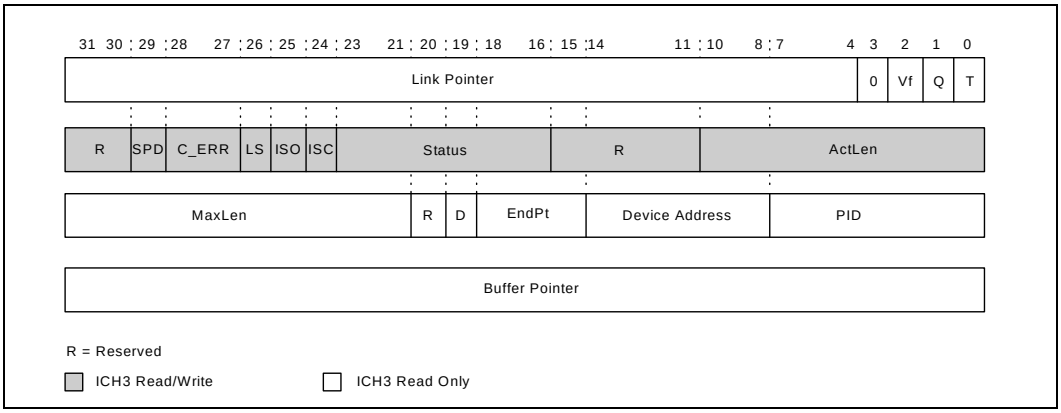


Table 5-58. TD Link Pointer

Bit	Description
31:4	**Link Pointer (LP).** Bits [31:4] Correspond to memory address signals [31:4], respectively. This field points to another TD or QH.
3	Reserved. Must be 0 when writing this field.
2	**Depth/Breadth Select (VF).** This bit is only valid for queued TDs and indicates to the hardware whether it should process in a depth first or breadth first fashion. When set to depth first, it informs the ICH3 to process the next transaction in the queue rather than starting a new queue. 0 = Breadth first. 1 = Depth first.
1	**QH/TD Select (Q).** This bit informs the ICH3 whether the item referenced by the link pointer is another TD or a QH. This allows the ICH3 to perform the proper type of processing on the item after it is fetched 0 = TD. 1 = QH.
0	**Terminate (T).** This bit informs the ICH3 that the link pointer in this TD does not point to another valid entry. When encountered in a queue context, this bit indicates to the ICH3 that there are no more valid entries in the queue. A TD encountered outside of a queue context with the T bit set informs the ICH3 that this is the last TD in the frame. 0 = Link Pointer field is valid. 1 = Link Pointer field not valid.

Table 5-59. TD Control and Status

Bit	Description
31:30	Reserved.
29	**Short Packet Detect (SPD).** When a packet has this bit set to 1 and the packet is an input packet, is in a queue; and successfully completes with an actual length less than the maximum length, then the TD is marked inactive, the Queue Header is not updated and the USBINT status bit (status register) is set at the end of the frame. In addition, if the interrupt is enabled, the interrupt will be sent at the end of the frame. Note that any error (e.g., babble or FIFO error) prevents the short packet from being reported. The behavior is undefined when this bit is set with output packets or packets outside of queues. 0 = Disable. 1 = Enable.
28:27	**Error Counter (C_ERR).** This field is a 2-bit down counter that keeps track of the number of Errors detected while executing this TD. If this field is programmed with a non zero value during setup, the ICH3 decrements the count and writes it back to the TD if the transaction fails. If the counter counts from one to zero, the ICH3 marks the TD inactive, sets the “STALLED” and error status bit for the error that caused the transition to zero in the TD. An interrupt will be generated to Host Controller Driver (HCD) if the decrement to zero was caused by Data Buffer error, Bit stuff error, or if enabled, a CRC or Timeout error. If HCD programs this field to zero during setup, the ICH3 will not count errors for this TD and there will be no limit on the retries of this TD. **Bits[28:27] — Interrupt After** 00 — No Error Limit 01 — Error 10 — 2 Errors 11 — 3 Errors **Error — Decrement Counter** CRC Error — Yes Timeout Error — Yes NAK Received — No Babble Detected — No* **Error — Decrement Counter** Data Buffer Error — Yes Stalled — No* Bit stuff Error — Yes *Detection of Babble or Stall automatically deactivates the TD. Thus, count is not decremented.
26	**Low Speed Device (LS).** This bit indicates that the target device (USB data source or sink) is a low speed device, running at 1.5 Mb/s, instead of at full speed (12 Mb/sec). There are special restrictions on schedule placement for low speed TDs. If an ICH3 root hub port is connected to a full speed device and this bit is set to a 1 for a low speed transaction, the ICH3 sends out a low speed preamble on that port before sending the PID. No preamble is sent if a ICH3 root hub port is connected to a low speed device. 0 = Full Speed Device 1 = Low Speed Device
25	**Isochronous Select (IOS).** The field specifies the type of the data structure. If this bit is set to a 1, then the TD is an isochronous transfer. Isochronous TDs are always marked inactive by the hardware after execution, regardless of the results of the transaction. 0 = Non-isochronous Transfer Descriptor 1 = Isochronous Transfer Descriptor
24	**Interrupt on Complete (IOC).** This specifies that the ICH3 should issue an interrupt on completion of the frame in which this Transfer Descriptor is executed. Even if the active bit in the TD is already cleared when the TD is fetched (no transaction will occur on USB), an IOC interrupt is generated at the end of the frame. 1 = Issue IOC
23	**Active.** For ICH3 schedule execution operations, see the Data Transfers To/From Main Memory section. 0 = When the transaction associated with this descriptor is completed, the ICH3 sets this bit to 0 indicating that the descriptor should not be executed when it is next encountered in the schedule. The active bit is also set to 0 if a stall handshake is received from the endpoint. 1 = Set to 1 by software to enable the execution of a message transaction by the ICH3.

Table 5-59. TD Control and Status (Continued)

Bit	Description
22	**Stalled.** 1 = Set to a 1 by the ICH3 during status updates to indicate that a serious error has occurred at the device/endpoint addressed by this TD. This can be caused by babble, the error counter counting down to zero, or reception of the STALL handshake from the device during the transaction. Any time that a transaction results in the stalled bit being set, the active bit is also cleared (set to 0). If a STALL handshake is received from a SETUP transaction, a Time Out Error will also be reported.
21	**Data Buffer Error (DBE).** 1 = Set to a 1 by the ICH3 during status update to indicate that the ICH3 is unable to keep up with the reception of incoming data (overrun) or is unable to supply data fast enough during transmission (underrun). When this occurs, the actual length and Max Length field of the TD will not match. In the case of an underrun, the ICH3 will transmit an incorrect CRC (thus invalidating the data at the endpoint) and leave the TD active (unless error count reached zero). If a overrun condition occurs, the ICH3 will force a timeout condition on the USB, invalidating the transaction at the source.
20	**Babble Detected (BABD).** 1 = Set to a 1 by the ICH3 during status update when “babble” is detected during the transaction generated by this descriptor. Babble is unexpected bus activity for more than a preset amount of time. In addition to setting this bit, the ICH3 also sets the” STALLED” bit (bit 22) to a 1. Since ”babble” is considered a fatal error for that transfer, setting the ”STALLED bit to a 1 insures that no more transactions occur as a result of this descriptor. Detection of babble causes immediate termination of the current frame. No further TDs in the frame are executed. Execution resumes with the next frame list index.
19	**Negative Acknowledgment (NAK) Received (NAKR).** 1 = Set to a 1 by the ICH3 during status update when the ICH3 receives a “NAK” packet during the transaction generated by this descriptor. If a NAK handshake is received from a SETUP transaction, a Time Out Error will also be reported.
18	**CRC/Time Out Error (CRC_TOUT).** 1 = Set to a 1 by the ICH3 as follows: During a status update in the case that no response is received from the target device/endpoint within the time specified by the protocol chapter of the USB specification. During a status update when a Cycli Redundancy Check (CRC) error is detected during the transaction associated with this transfer descriptor. In the transmit case (OUT or SETUP command), this is in response to the ICH3 detecting a timeout from the target device/endpoint. In the receive case (IN command), this is in response to the ICH3’s CRC checker circuitry detecting an error on the data received from the device/endpoint or a NAK or STALL handshake being received in response to a SETUP transaction.
17	**Bit Stuff Error (BSE).** 1 = This bit is set to a 1 by the ICH3 during status update to indicate that the receive data stream contained a sequence of more than 6 ones in a row.
16	**Bus Turn Around Time-out (BTTO).** 1 = This bit is set to a 1 by the ICH3 during status updates to indicate that a bus time-out condition was detected for this USB transaction. This time-out is specially defined as not detecting an IDLE-to ‘K’ state Start of Packet (SOP) transition from 16 to 18 bit times after the SE0-to IDE transition of previous End of Packet (EOP).
15:11	Reserved
10:0	**Actual Length (ACTLEN).** The Actual Length field is written by the ICH3 at the conclusion of a USB transaction to indicate the actual number of bytes that were transferred. It can be used by the software to maintain data integrity. The value programmed in this register is encoded as n-1 (see Maximum Length field description in the TD Token).

Table 5-60. TD Token

Bit	Description
31:21	**Maximum Length (MAXLEN).** The Maximum Length field specifies the maximum number of data bytes allowed for the transfer. The Maximum Length value does not include protocol bytes, such as Packet ID (PID) and CRC. The maximum data packet is 1280 bytes. The 1280 packet length is the longest packet theoretically guaranteed to fit into a frame. Actual packet maximum lengths are set by HCD according to the type and speed of the transfer. Note that the maximum length allowed by the USB specification is 1023 bytes. The valid encodings for this field are: 0x000 = 1 byte 0x001 = 2 bytes .... 0x3FE = 1023 bytes 0x3FF = 1024 bytes .... 0x4FF = 1280 bytes 0x7FF = 0 bytes (null data packet) Note that values from 500h to 7FEh are illegal and cause a consistency check failure. In the transmit case, the ICH3 uses this value as a terminal count for the number of bytes it fetches from host memory. In most cases, this is the number of bytes it will actually transmit. In rare cases, the ICH3 may be unable to access memory (e.g., due to excessive latency) in time to avoid underrunning the transmitter. In this instance the ICH3 would transmit fewer bytes than specified in the Maximum Length field.
20	Reserved.
19	**Data Toggle (D).** This bit is used to synchronize data transfers between a USB endpoint and the host. This bit determines which data PID is sent or expected (0=DATA0 and 1=DATA1). The data toggle bit provides a 1-bit sequence number to check whether the previous packet completed. This bit must always be 0 for Isochronous TDs.
18:15	**Endpoint (ENDPT).** This 4-bit field extends the addressing internal to a particular device by providing 16 endpoints. This permits more flexible addressing of devices in which more than one sub-channel is required.
14:8	**Device Address.** This field identifies the specific device serving as the data source or sink.
7:0	**Packet Identification (PID).** This field contains the Packet ID to be used for this transaction. Only the IN (69h), OUT (E1h), and SETUP (2Dh) tokens are allowed. Any other value in this field causes a consistency check failure resulting in an immediate halt of the ICH3. Bits [3:0] are complements of bits [7:4].

Table 5-61. TD Buffer Pointer

Bit	Description
31:0	**Buffer Pointer (BUFF_PNT).** Bits [31:0] corresponds to memory address [31:0], respectively. It points to the beginning of the buffer that will be used during this transaction. This buffer must be at least as long as the value in the Maximum Length field described int the TD Token. The data buffer may be byte-aligned.

5.16.1.3 Queue Head (QH)

Queue heads are special structures used to support the requirements of Control, Bulk, and Interrupt transfers. Since these TDs are not automatically retired after each use, their maintenance requirements can be reduced by putting them into a queue. Queue Heads must be aligned on a 16-byte boundary and the elements are shown in Table 5-62.

Table 5-62. Queue Head Block

Bytes	Description	Attributes
00–03	Queue Head Link Pointer	RO
04–07	Queue Element Link Pointer	R/W

Table 5-63. Queue Head Link Pointer

Bit	Description
31:4	**Queue Head Link Pointer (QHLP).** This field contains the address of the next data object to be processed in the horizontal list and corresponds to memory address signals [31:4], respectively.
3:2	Reserved. These bits must be written as 0s.
1	**QH/TD Select (Q).** This bit indicates to the hardware whether the item referenced by the link pointer is another TD or a QH. 0 = TD 1 = QH
0	**Terminate (T).** This bit indicates to the ICH3 that this is the last QH in the schedule. If there are active TDs in this queue, they are the last to be executed in this frame. 0 = Pointer is valid (points to a QH or TD). 1 = Last QH (pointer is invalid).

Table 5-64. Queue Element Link Pointer

Bit	Description
31:4	**Queue Element Link Pointer (QELP).** This field contains the address of the next TD or QH to be processed in this queue and corresponds to memory address signals [31:4], respectively.
3:2	Reserved.
1	**QH/TD Select (Q).** This bit indicates to the hardware whether the item referenced by the link pointer is another TD or a QH. For entries in a queue, this bit is typically set to 0. 0 = TD 1 = QH
0	**Terminate (T).** This bit indicates to the ICH3 that there are no valid TDs in this queue. When HCD has new queue entries it overwrites this value with a new TD pointer to the queue entry. 0 = Pointer is valid. 1 = Terminate (No valid queue entries).

5.16.2 Data Transfers to/from Main Memory

The following sections describe the details on how HCD and the ICH3 communicate via the Schedule data structures. The discussion is organized in a top-down manner, beginning with the basics of walking the Frame List, followed by a description of generic processing steps common to all transfer descriptors, and finally a discussion on Transfer Queuing.

5.16.2.1 Executing the Schedule

Software programs the ICH3 with the starting address of the Frame List and the Frame List index, then causes the ICH3 to execute the schedule by setting the run/stop bit in the control register to Run. The ICH3 processes the schedule one entry at a time: the next element in the frame list is not fetched until the current element in the frame list is retired.

Schedule execution proceeds in the following fashion:

- The ICH3 first fetches an entry from the Frame List. This entry has three fields. Bit 0 indicates whether the address pointer field is valid. Bit 1 indicates whether the address points to a Transfer Descriptor or to a queue head. The third field is the pointer itself.
- If isochronous traffic is to be moved in a given frame, the Frame List entry points to a Transfer Descriptor. If no isochronous data is to be moved in that frame, the entry points to a queue head or the entry is marked invalid and no transfers are initiated in that frame.
- If the Frame List entry indicates that it points to a Transfer Descriptor, the ICH3 fetches the entry and begins the operations necessary to initiate a transaction on USB. Each TD contains a link field that points to the next entry, as well as indicating whether it is a TD or a QH.
- If the Frame List entry contains a pointer to a QH, the ICH3 processes the information from the QH to determine the address of the next data object that it should process.
- The TD/QH process continues until the millisecond allotted to the current frame expires. At this point, the ICH3 fetches the next entry from the Frame List. If the ICH3 is not able to process all of the transfer descriptors during a given frame, those descriptors are retired by software without having been executed.

5.16.2.2 Processing Transfer Descriptors

The ICH3 executes a TD using the following generalized algorithm. These basic steps are common across all modes of TDs. Subsequent sections present processing steps unique to each TD mode.

1. ICH3 Fetches TD or QH from the current Link Pointer.
2. If a QH, go to 1 to fetch from the Queue Element Link Pointer. If inactive, go to 12
3. Build Token, actual bits are in TD Token.
4. If (Host-to-Function) then
   [*PCI Access*] issue request for data, (referenced through TD.BufferPointer)
   wait for first chunk data arrival
   end if
5. [*Begin USB Transaction*] Issue Token (from token built in 2, above) and begin data transfer.
   if (Host-to-Function) then Go to 6
   else Go to 7
   end if
6. Fetch data from memory (via TD BufferPointer) and transfer over USB until TD Max-Length bytes have been read and transferred. [*Concurrent system memory and USB Accesses*]. Go to 8.
7. Wait for data to arrive (from USB). Write incoming bytes into memory beginning at TD BufferPointer. Internal HC buffer should signal end of data packet. Number of bytes received must be (TD Max-Length; The length of the memory area referenced by TD BufferPointer must be (TD Max-Length. [*Concurrent system memory and USB Accesses*].
8. Issue handshake based on status of data received (Ack or Time-out). Go to 10.
9. Wait for handshake, if required [*End of USB Transaction*].
10. Update Status [*PCI Access*] (TD.Status and TD.ActualLength).
    If the TD was an isochronous TD, mark the TD inactive. Go to 12.
    If not an isochronous TD, and the TD completed successfully, mark the TD inactive. Go to 11.
    If not successful, and the error count has not been reached, leave the TD active. If the error count has been reached, mark the TD inactive. Go to 12.
11. Write the link pointer from the current TD into the element pointer field of the QH structure. If the Vf bit is set in the TD link pointer, go to 2.
12. Proceed to next entry.

5.16.2.3 Command Register, Status Register, and TD Status Bit Interaction

Table 5-65. Command Register, Status Register and TD Status Bit Interaction

Condition	ICH3 USB Status Register Actions	TD Status Register Actions
CRC/Time Out Error	Set USB Error Int bit[1], Clear HC Halted bit	Clear Active bit[1] and set Stall bit[1]
Illegal PID, PID Error, Max Length (illegal)	Clear Run/Stop bit in command register Set HC Process Error and HC Halted bits	
PCI Master/Target Abort	Clear Run/Stop bit in command register Set Host System Error and HC Halted bits	
Suspend Mode	Clear Run/Stop bit in command register[2] Set HC Halted bit	
Resume Received and Suspend Mode = 1	Set Resume received bit	
Run/Stop = 0	Clear Run/Stop bit in command register Set HC Halted bit	
Configuration Flag Set	Set Configuration Flag in command register	
HC Reset/Global Reset	Clear Run/Stop and Configuration Flag in command register Clear USB Int, USB Error Int, Resume received, Host System Error, HC Process Error, and HC Halted bits	
IOC = 1 in TD Status	Set USB Int bit	
Stall	Set USB Error Int bit	Clear Active bit[1] and set Stall bit
Bit Stuff/Data Buffer Error	Set USB Error Int bit[1]	Clear Active bit[1] and set Stall bit[1]
Short Packet Detect	Set USB Int bit	Clear Active bit

NOTES:
1. Only If error counter counted down from 1 to 0
2. Suspend mode can be entered only when Run/Stop bit is 0

Note that if a NAK or STALL response is received from a SETUP transaction, a Time Out Error will be reported. This will cause the Error counter to decrement and the CRC/Time-out Error status bit to be set within the TD Control and Status dword during write back. If the Error counter changes from 1 to 0, the Active bit will be reset to 0 and Stalled bit to 1 as normal.

5.16.2.4 Transfer Queuing

Transfer Queues are used to implement a guaranteed data delivery stream to a USB Endpoint. Transfer Queues are composed of two parts: a Queue Header (QH) and a linked list. The linked list of TDs and QHs has an indeterminate length (0 to n).

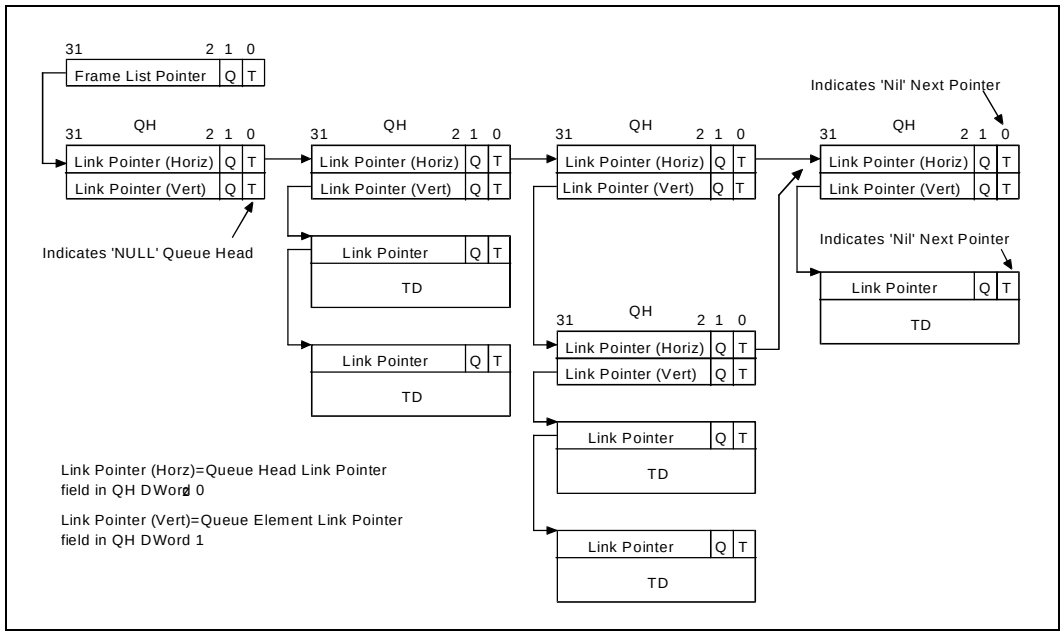
The QH contains two link pointers and is organized as two contiguous dwords. The first dword is a horizontal pointer (Queue Head Link Pointer), used to link a single transfer queue with either another transfer queue, or a TD (target data structure depends on Q bit). If the T bit is set, this QH represents the last data structure in the current Frame. The T bit informs the ICH3 that no further processing is required until the beginning of the next frame. The second dword is a vertical pointer (Queue Element Link Pointer) to the first data structure (TD or QH) being managed by this QH. If the T bit is set, the queue is empty. This pointer may reference a TD or another QH.

Figure 5-16 illustrates four example queue conditions. The first QH (on far left) is an example of an “empty” queue; the termination bit (T Bit), in the vertical link pointer field, is set to 1. The horizontal link pointer references another QH. The next queue is the expected typical configuration. The horizontal link pointer references another QH, and the vertical link pointer references a valid TD.

Typically, the vertical pointer in a QH points to a TD. However, as shown in Figure 5-16 (third example from left side of figure) the vertical pointer could point to another QH. When this occurs, a new Q Context is entered and the Q Context just exited is NULL (ICH3 will not update the vertical pointer field).

The far right QH is an example of a frame “termination” node. Since its horizontal link pointer has its termination bit set, the ICH3 assumes there is no more work to complete for the current Frame.

Figure 5-16. Example Queue Conditions



Transfer Queues are based on the following characteristics:

- A QH's vertical link pointer (Queue Element Link Pointer) references the 'Top' queue member. A QH's horizontal link pointer (Queue Head Link Pointer) references the "next" work element in the Frame.
- Each queue member's link pointer references the next element within the queue.

In the simplest model, the ICH3 follows vertical link point to a queue element, then executes the element. If the completion status of the TD satisfies the advance criteria as shown in Table 5-66, the ICH3 advances the queue by writing the just-executed TD's link pointer back into the QH's Queue Element link pointer. The next time the queue head is traversed, the next queue element will be the Top element.

The traversal has two options: Breadth first, or Depth first. A flag bit in each TD (Vf–Vertical Traversal Flag) controls whether traversal is Breadth or Depth first. The default mode of traversal is Breadth-First. For Breadth-First, the ICH3 only executes the top element from each queue. The execution path is shown below:

1. QH (Queue Element Link Pointer)
2. TD
3. Write-Back to QH (Queue Element Link Pointer)
4. QH (Queue Head Link pointer).

Breadth-First is also performed for every transaction execution that fails the advance criteria. This means that if a queued TD fails, the queue does not advance, and the ICH3 traverses the QH's Queue Head Link Pointer.

In a Depth-first traversal, the top queue element must complete successfully to satisfy the *advance criteria* for the queue. If the ICH3 is currently processing a queue, and the advance criteria are met, and the Vf bit is set, the ICH3 follows the TD's link pointer to the next schedule work item.

Note that regardless of traversal model, when the advance criteria are met, the successful TD's link pointer is written back to the QH's Queue Element link pointer.

When the ICH3 encounters a QH, it caches the QH internally, and sets internal state to indicate it is in a Q-context. It needs this state to update the correct QH (for auto advancement) and also to make the correct decisions on how to traverse the Frame List.

Restricting the advancement of queues to advancement criteria implements a guaranteed data delivery stream.

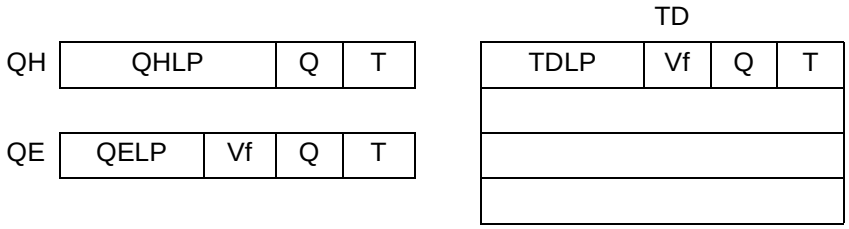
A queue is **never** advanced on an error completion status (even in the event the error count was exhausted).

Table 5-66 lists the general queue advance criteria, which are based on the execution status of the TD at the "top" of a currently "active" queue.

Table 5-66. Queue Advance Criteria

Function-to-Host (IN)			Host-to-Function (OUT)		
Non-NULL	**NULL**	**Error/NAK**	**Non-NULL**	**NULL**	**Error/NAK**
Advance Q	Advance Q	Retry Q Element	Advance Q	Advance Q	Retry Q Element

Table 5-67 is a decision table illustrating the valid combinations of link pointer bits and the valid actions taken when advancement criteria for a queued transfer descriptor are met. The column headings for the link pointer fields are encoded, based on the following list:



Legend:

QH.LP = Queue Head Link Pointer (or Horizontal Link Pointer)
QE.LP = Queue Element Link Pointer (or Vertical Link Pointer)
TD.LP = TD Link Pointer
QH.Q = Q bit in QH
QH.T = T bit in QH
QE.Q = Q bit in QE
QE.T = T bit in QE
TD. Vf = Vf bit in TD
TD.Q = Q bit in TD
TD. T = T bit in TD

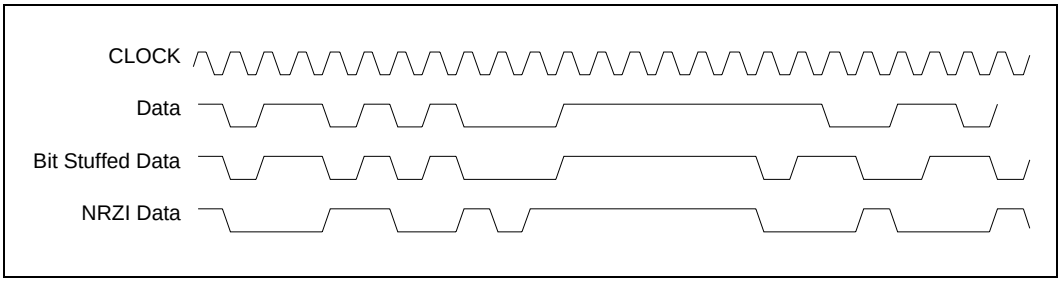
Table 5-67. USB Schedule List Traversal Decision Table

Q Context	QH.Q	QH.T	QE.Q	QE.T	TD.Vf	TD.Q	TD.T	Description
0	-	-	-	-	x	0	0	Not in Queue–execute TD. Use TD.LP to get next TD
0	-	-	-	-	x	x	1	Not in Queue–execute TD. End of Frame
0	-	-	-	-	x	1	0	Not in Queue –execute TD. Use TD.LP to get next (QH+QE). Set Q Context to 1.
1	0	0	0	0	0	x	x	In Queue. Use QE.LP to get TD. Execute TD. Update QE.LP with TD.LP. Use QH.LP to get next TD.
1	x	x	0	0	1	0	0	In Queue. Use QE.LP to get TD. Execute TD. Update QE.LP with TD.LP. Use TD.LP to get next TD.
1	x	x	0	0	1	1	0	In Queue. Use QE.LP to get TD. Execute TD. Update QE.LP with TD.LP. Use TD.LP to get next (QH+QE).
1	0	0	x	1	x	x	x	In Queue. Empty queue. Use QH.LP to get next TD
1	x	x	1	0	-	-	-	In Queue. Use QE.LP to get (QH+QE)
1	x	1	0	0	0	x	x	In Queue. Use QE.LP to get TD. Execute TD. Update QE.LP with TD.LP. End of Frame
1	x	1	x	1	x	x	x	In Queue. Empty queue. End of Frame
1	1	0	0	0	0	x	x	In Queue. Use QE.LP to get TD. Execute TD. Update QE.LP with TD.LP. Use QH.LP to get next (QH+QE).
1	1	0	x	1	x	x	x	In Queue. Empty queue. Use QH.LP to get next (QH+QE)

5.16.3 Data Encoding and Bit Stuffing

The USB employs NRZI data encoding (Non-Return to Zero Inverted) when transmitting packets. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. A string of zeros causes the NRZI data to toggle each bit time. A string of ones causes long periods with no transitions in the data. In order to ensure adequate signal transitions, bit stuffing is employed by the transmitting device when sending a packet on the USB. A 0 is inserted after every six consecutive 1s in the data stream before the data is NRZI encoded to force a transition in the NRZI data stream. This gives the receiver logic a data transition at least once every seven bit times to guarantee the data and clock lock. A waveform of the data encoding is shown in Figure 5-17.

Figure 5-17. USB Data Encoding



Bit stuffing is enabled beginning with the Sync Pattern and throughout the entire transmission. The data “one” that ends the Sync Pattern is counted as the first one in a sequence. Bit stuffing is always enforced, without exception. If required by the bit stuffing rules, a zero bit will be inserted even if it is the last bit before the end-of-packet (EOP) signal.

5.16.4 Bus Protocol

5.16.4.1 Bit Ordering

Bits are sent out onto the bus least significant bit (LSb) first, followed by next LSb, through to the most significant bit (MSb) last.

5.16.4.2 SYNC Field

All packets begin with a synchronization (SYNC) field, which is a coded sequence that generates a maximum edge transition density. The SYNC field appears on the bus as IDLE followed by the binary string “KJKJKJKK,” in its NRZI encoding. It is used by the input circuitry to align incoming data with the local clock and is defined to be eight bits in length. SYNC serves only as a synchronization mechanism and is not shown in the following packet diagrams. The last two bits in the SYNC field are a marker that is used to identify the first bit of the PID. All subsequent bits in the packet must be indexed from this point.

5.16.4.3 Packet Field Formats

Field formats for the token, data, and handshake packets are described in the following section. The effects of NRZI coding and bit stuffing have been removed for the sake of clarity. All packets have distinct start and end of packet delimiters.

Table 5-68. PID Format

Bit	Data Sent	Bit	Data Sent
0	PID 0	4	NOT(PID 0)
1	PID 1	5	NOT(PID 1)
2	PID 2	6	NOT(PID 2)
3	PID 3	7	NOT(PID 3)

Packet Identifier Field

A packet identifier (PID) immediately follows the SYNC field of every USB packet. A PID consists of a four-bit packet type field followed by a four-bit check field as shown in Table 5-68. The PID indicates the type of packet and, by inference, the format of the packet and the type of error detection applied to the packet. The four-bit check field of the PID insures reliable decoding of the PID so that the remainder of the packet is interpreted correctly. The PID check field is generated by performing a ones complement of the packet type field.

Any PID received with a failed check field or which decodes to a non-defined value is assumed to be corrupted and the remainder of the packet is assumed to be corrupted and is ignored by the receiver. PID types, codes, and descriptions are listed in Table 5-69.

Table 5-69. PID Types

PID Type	PID Name	PID[3:0]	Description
Token	OUT	b0001	Address + endpoint number in host -> function transaction
	IN	b1001	Address + endpoint number in function -> host transaction
	SOF	b0101	Start of frame marker and frame number
	SETUP	b1101	Address + endpoint number in host -> function transaction for setup to a control endpoint
Data	DATA0	b0011	Data packet PID even
	DATA1	b1011	Data packet PID odd
Handshake	ACK	b0010	Receiver accepts error free data packet
	NAK	b1010	Rx device cannot accept data or Tx device cannot send data
	STALL	b1110	Endpoint is stalled
Special	PRE	b1100	Host-issued preamble. Enables downstream bus traffic to low speed devices.

PIDs are divided into four coding groups: token, data, handshake, and special, with the first two transmitted PID bits (PID[1:0]) indicating which group. This accounts for the distribution of PID codes.

5.16.4.4 Address Fields

Function endpoints are addressed using two fields: function address field and endpoint field.

Table 5-70. Address Field

Bit	Data Sent	Bit	Data Sent
0	ADDR 0	4	ADDR 4
1	ADDR 1	5	ADDR 5
2	ADDR 2	6	ADDR 6
3	ADDR 3		

Address Field

The function address (ADDR) field specifies the function, via its address, that is either the source or destination of a data packet, depending on the value of the token PID. As shown in Table 5-70, a total of 128 addresses are specified as ADDR[6:0]. The ADDR field is specified for IN, SETUP, and OUT tokens.

Endpoint Field

An additional four-bit endpoint (ENDP) field, shown in Table 5-71, permits more flexible addressing of functions in which more than one sub-channel is required. Endpoint numbers are function specific. The endpoint field is defined for IN, SETUP, and OUT token PIDs only.

Table 5-71. Endpoint Field

Bit	Data Sent
0	ENDP 0
1	ENDP 1
2	ENDP 2
3	ENDP 3

5.16.4.5 Frame Number Field

The frame number field is an 11-bit field that is incremented by the host on a per-frame basis. The frame number field rolls over upon reaching its maximum value of x7FFh, and is sent only for SOF tokens at the start of each frame.

5.16.4.6 Data Field

The data field may range from 0 to 1023 bytes and must be an integral numbers of bytes. Data bits within each byte are shifted out LSB first.

5.16.4.7 Cyclic Redundancy Check (CRC)

CRC is used to protect the all non-PID fields in token and data packets. In this context, these fields are considered to be protected fields. The PID is not included in the CRC check of a packet containing CRC. All CRCs are generated over their respective fields in the transmitter before bit stuffing is performed. Similarly, CRCs are decoded in the receiver after stuffed bits have been removed. Token and data packet CRCs provide 100% coverage for all single- and double-bit errors. A failed CRC is considered to indicate that one or more of the protected fields is corrupted and causes the receiver to ignore those fields, and, in most cases, the entire packet.

5.16.5 Packet Formats

5.16.5.1 Token Packets

Table 5-72 shows the field formats for a token packet. A token consists of a PID, specifying either IN, OUT, or SETUP packet type, and ADDR and ENDP fields. For OUT and SETUP transactions, the address and endpoint fields uniquely identify the endpoint that will receive the subsequent data packet. For IN transactions, these fields uniquely identify which endpoint should transmit a data packet. Only the ICH3 can issue token packets. IN PIDs define a data transaction from a function to the ICH3. OUT and SETUP PIDs define data transactions from the ICH3 to a function.

Token packets have a five-bit CRC which covers the address and endpoint fields as shown above. The CRC does not cover the PID, which has its own check field. Token and SOF packets are delimited by an EOP after three bytes of packet field data. If a packet decodes as an otherwise valid token or SOF but does not terminate with an EOP after three bytes, it must be considered invalid and ignored by the receiver.

Table 5-72. Token Format

Packet	Width
PID	8 bits
ADDR	7 bits
ENDP	4 bits
CRC5	5 bits

5.16.5.2 Start of Frame Packets

Table 5-73 shows a start of frame (SOF) packet. SOF packets are issued by the host at a nominal rate of once every 1.00 ms 0.05. SOF packets consist of a PID indicating packet type followed by an 11-bit frame number field.

The SOF token comprises the token-only transaction that distributes a start of frame marker and accompanying frame number at precisely timed intervals corresponding to the start of each frame. All full speed functions, including hubs, must receive and decode the SOF packet. The SOF token does not cause any receiving function to generate a return packet; therefore, SOF delivery to any given function cannot be guaranteed. The SOF packet delivers two pieces of timing information. A function is informed that a start of frame has occurred when it detects the SOF PID. Frame timing sensitive functions, which do not need to keep track of frame number, need only decode the SOF PID; they can ignore the frame number and its CRC. If a function needs to track frame number, it must comprehend both the PID and the time stamp.

Table 5-73. SOF Packet

Packet	Width
PID	8 bits
Frame Number	11 bits
CRC5	5 bits

5.16.5.3 Data Packets

A data packet consists of a PID, a data field, and a CRC as shown in Table 5-74. There are two types of data packets, identified by differing PIDs: DATA0 and DATA1. Two data packet PIDs are defined to support data toggle synchronization.

Data must always be sent in integral numbers of bytes. The data CRC is computed over only the data field in the packet and does not include the PID, which has its own check field.

Table 5-74. Data Packet Format

Packet	Width
PID	8 bits
DATA	0-1023 bytes
CRC16	16 bits

5.16.5.4 Handshake Packets

Handshake packets consist of only a PID. Handshake packets are used to report the status of a data transaction and can return values indicating successful reception of data, flow control, and stall conditions. Only transaction types that support flow control can return handshakes. Handshakes are always returned in the handshake phase of a transaction and may be returned, instead of data, in the data phase. Handshake packets are delimited by an EOP after one byte of packet field. If a packet is decoded as an otherwise valid handshake but does not terminate with an EOP after one byte, it must be considered invalid and ignored by the receiver.

There are three types of handshake packets:

- **ACK** indicates that the data packet was received without bit stuff or CRC errors over the data field and that the data PID was received correctly. An ACK handshake is applicable only in transactions in which data has been transmitted and where a handshake is expected. ACK can be returned by the host for IN transactions and by a function for OUT transactions.
- **NAK** indicates that a function was unable to accept data from the host (OUT) or that a function has no data to transmit to the host (IN). NAK can only be returned by functions in the data phase of IN transactions or the handshake phase of OUT transactions. The host can never issue a NAK. NAK is used for flow control purposes to indicate that a function is temporarily unable to transmit or receive data, but will eventually be able to do so without need of host intervention. NAK is also used by interrupt endpoints to indicate that no interrupt is pending.
- **STALL** is returned by a function in response to an IN token or after the data phase of an OUT. STALL indicates that a function is unable to transmit or receive data, and that the condition requires host intervention to remove the stall. Once a function's endpoint is stalled, the function must continue returning STALL until the condition causing the stall has been cleared through host intervention. The host is not permitted to return a STALL under any condition.

5.16.5.5 Handshake Responses

IN Transaction

A function may respond to an IN transaction with a STALL or NAK. If the token received was corrupted, the function will issue no response. If the function can transmit data, it will issue the data packet. The ICH3, as the USB host, can return only one type of handshake on an IN transaction, an ACK. If it receives a corrupted data, or cannot accept data due to a condition such as an internal buffer overrun, it discards the data and issues no response.

OUT Transaction

A function may respond to an OUT transaction with a STALL, ACK, or NAK. If the transaction contained corrupted data, it will issue no response.

SETUP Transaction

Setup defines a special type of host to function data transaction which permits the host to initialize an endpoint's synchronization bits to those of the host. Upon receiving a Setup transaction, a function must accept the data. Setup transactions cannot be STALLed or NAKed and the receiving function must accept the Setup transfer's data. If a non-control endpoint receives a SETUP PID, it must ignore the transaction and return no response.

5.16.6 USB Interrupts

There are two general groups of USB interrupt sources, those resulting from execution of transactions in the schedule, and those resulting from an ICH3 operation error. All transaction-based sources can be masked by software through the ICH3's Interrupt Enable Register. Additionally, individual transfer descriptors can be marked to generate an interrupt on completion.

When the ICH3 drives an interrupt for USB, it internally drives the PIRQ[A]# pin for USB function #0, PIRQ[D]# pin for USB function #1, and the PIRQ[C]# pin for USB function #2, until all sources of the interrupt are cleared. In order to accommodate some operating systems, the Interrupt Pin Register must contain a different value for each function of this new multi-function device.

5.16.6.1 Transaction Based Interrupts

These interrupts are not signaled until after the status for the last complete transaction in the frame has been written back to host memory. This guarantees that software can safely process through (Frame List Current Index -1) when it is servicing an interrupt.

CRC Error / Time-Out

A CRC/Time-out error occurs when a packet transmitted from the ICH3 to a USB device or a packet transmitted from a USB device to the ICH3 generates a CRC error. The ICH3 is informed of this event by a time-out from the USB device or by the ICH3's CRC checker generating an error on reception of the packet. Additionally, a USB bus time-out occurs when USB devices do not respond to a transaction phase within 19 bit times of an EOP. Either of these conditions will cause the C_ERR field of the TD to decrement.

When the C_ERR field decrements to zero, the following occurs:

- The active bit in the TD is cleared
- The stalled bit in the TD is set
- The CRC/Time-out bit in the TD is set.
- At the end of the frame, the USB error interrupt bit is set in the HC status register.

If the CRC/Time-out interrupt is enabled in the Interrupt Enable Register, a hardware interrupt will be signaled to the system.

Interrupt on Completion

Transfer Descriptors contain a bit that can be set to cause an interrupt on their completion. The completion of the transaction associated with that block causes the USB interrupt bit in the HC Status Register to be set at the end of the frame in which the transfer completed. When a TD is encountered with the IOC bit set to 1, the IOC bit in the HC status register is set to 1 at the end of the frame if the active bit in the TD is set to 0 (even if it was set to zero when initially read).

If the IOC enable bit of Interrupt Enable Register (bit 2 of I/O offset 04h) is set, a hardware interrupt is signaled to the system. The USB interrupt bit in the HC status register is set either when the TD completes successfully or because of errors. If the completion is because of errors, the USB error bit in the HC status register is also set.

Short Packet Detect

A transfer set is a collection of data which requires more than 1 USB transaction to completely move the data across the USB. An example might be a large print file which requires numerous TDs in multiple frames to completely transfer the data. Reception of a data packet that is less than the endpoint's Max Packet size during Control, Bulk or Interrupt transfers signals the completion of the transfer set, even if there are active TDs remaining for this transfer set. Setting the SPD bit in a TD indicates to the HC to set the USB interrupt bit in the HC Status Register at the end of the frame in which this event occurs. This feature streamlines the processing of input on these transfer types. If the short packet interrupt enable bit in the Interrupt Enable Register is set, a hardware interrupt is signaled to the system at the end of the frame where the event occurred.

Serial Bus Babble

When a device transmits on the USB for a time greater than its assigned Max Length, it is said to be babbling. Since isochrony can be destroyed by a babbling device, this error results in the active bit in the TD being cleared to 0 and the Stalled and Babble bits being set to one. The C_ERR field is not decremented for a babble. The USB error interrupt bit in the HC status register is set to 1 at the end of the frame. A hardware interrupt is signaled to the system.

If an EOF babble was caused by the ICH3 (due to incorrect schedule for instance), the ICH3 will force a bit stuff error followed by an EOP and the start of the next frame.

Stalled

This event indicates that a device/endpoint returned a STALL handshake during a transaction or that the transaction ended in an error condition. The TDs stalled bit is set and the active bit is cleared. Reception of a STALL does not decrement the error counter. A hardware interrupt is signaled to the system.

Data Buffer Error

This event indicates that an overrun of incoming data or a under-run of outgoing data has occurred for this transaction. This would generally be caused by the ICH3 not being able to access required data buffers in memory within necessary latency requirements. Either of these conditions will cause the C_ERR field of the TD to be decremented.

When C_ERR decrements to zero, the active bit in the TD is cleared, the stalled bit is set, the USB error interrupt bit in the HC status register is set to 1 at the end of the frame and a hardware interrupt is signaled to the system.

Bit Stuff Error

A bit stuff error results from the detection of a sequence of more that 6 ones in a row within the incoming data stream. This will cause the C_ERR field of the TD to be decremented. When the C_ERR field decrements to zero, the active bit in the TD is cleared to 0, the stalled bit is set to one, the USB error interrupt bit in the HC status register is set to 1 at the end of the frame and a hardware interrupt is signaled to the system.

5.16.6.2 Non-Transaction Based Interrupts

If an ICH3 process error or system error occur, the ICH3 halts and immediately issues a hardware interrupt to the system.

Resume Received

This event indicates that the ICH3 received a RESUME signal from a device on the USB bus during a global suspend. If this interrupt is enabled in the Interrupt Enable Register, a hardware interrupt will be signaled to the system allowing the USB to be brought out of the suspend state and returned to normal operation.

ICH3 Process Error

The HC monitors certain critical fields during operation to ensure that it does not process corrupted data structures. These include checking for a valid PID and verifying that the MaxLength field is less than 1280. If it detects a condition that would indicate that it is processing corrupted data structures, it immediately halts processing, sets the HC process error bit in the HC Status Register and signals a hardware interrupt to the system.

This interrupt cannot be disabled through the Interrupt Enable Register.

Host System Error

The ICH3 sets this bit to 1 when a PCI Parity error, PCI Master Abort, or PCI Target Abort occur. When this error occurs, the ICH3 clears the run/stop bit in the USB Command Register to prevent further execution of the scheduled TDs. This interrupt cannot be disabled through the Interrupt Enable Register.

5.16.7 USB Power Management

The Host Controller can be put into a suspended state and its power can be removed. This requires that certain bits of information are retained in the resume power plane of the ICH3 so that a device on a port may wake the system. Such a device may be a fax-modem, which will wake up the machine to receive a fax or take a voice message. The settings of the following bits in I/O space will be maintained when the ICH3 enters the S3, S4, or S5 states.

Table 5-75. Bits Maintained in Low Power States

Register	Offset	Bit	Description
Command	00h	3	Enter Global Suspend Mode (EGSM)
Status	02h	2	Resume Detect
Port Status and Control	10h & 12h	2	Port Enabled/Disabled
		6	Resume Detect
		8	Low Speed Device Attached
		12	Suspend

When the ICH3 detects a resume event on any of its ports, it will set the corresponding USB_STS bit in ACPI space. If USB is enabled as a wake/break event, the system will wake up and an SCI will be generated.

5.16.8 USB Legacy Keyboard Operation

When a USB keyboard is plugged into the system, and a standard keyboard is not, the system may not boot, and DOS legacy software will not run, because the keyboard will not be identified. The ICH3 implements a series of trapping operations which will snoop accesses that go to the keyboard controller, and put the expected data from the USB keyboard into the keyboard controller.

Note: The scheme described below assumes that the keyboard controller (8042 or equivalent) is on the LPC bus.

This legacy operation is performed through SMM space.

Figure 5-18 shows the Enable and Status path. The latched SMI source (60R, 60W, 64R, 64W) is available in the status register. Because the enable is after the latch, it is possible to check for other events that didn't necessarily cause an SMI. It is the software's responsibility to logically AND the value with the appropriate enable bits.

Note also that the SMI is generated before the PCI cycle completes (e.g., before TRDY# goes active) to ensure that the processor doesn't complete the cycle before the SMI is observed. This method is used on MPIIX and has been validated.

The logic will also need to block the accesses to the 8042. If there is an external 8042, then this is simply accomplished by not activating the 8042 CS. This is simply done by logically ANDing the 4 enables (60R, 60W, 64R, 64W) with the 4 types of accesses to determine if 8042CS should go active. An additional term is required for the “Pass-through” case.

The state table for the diagram is shown in Table 5-76.

Figure 5-18. USB Legacy Keyboard Flow Diagram

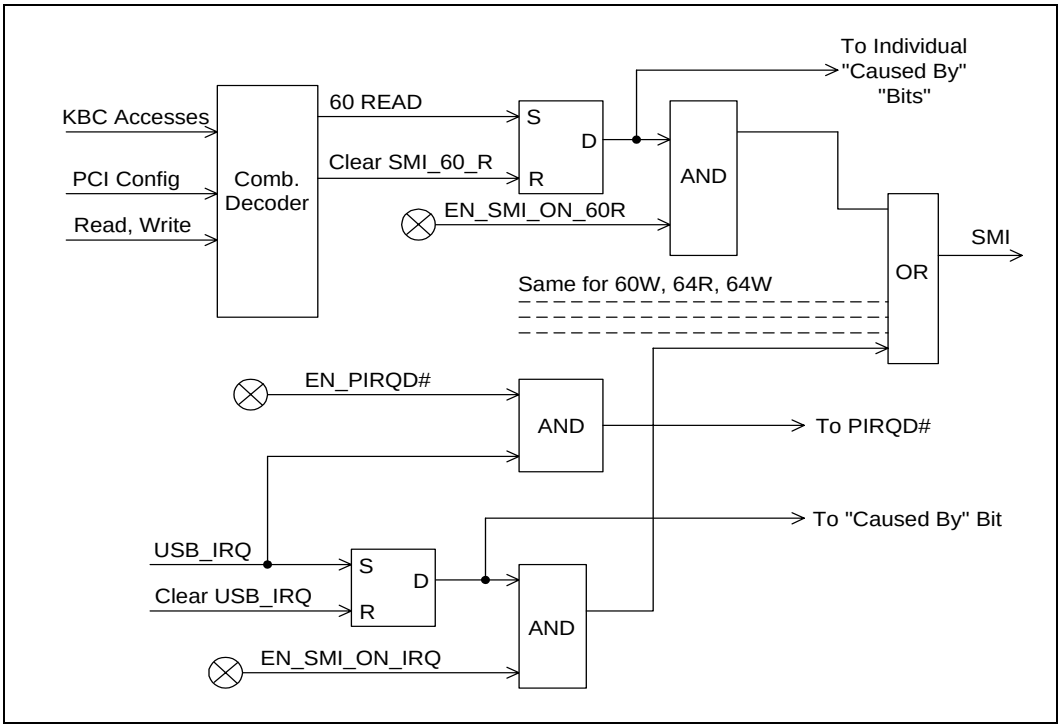


Table 5-76. USB Legacy Keyboard State Transitions

Current State	Action	Data Value	Next State	Comment
IDLE	64h / Write	D1h	GateState1	Standard D1 command. Cycle passed through to 8042. SMI# doesn't go active. PSTATE (offset C0, bit 6) goes to 1.
IDLE	64h / Write	Not D1h	IDLE	Bit 3 in the configuration register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	64h / Read	N/A	IDLE	Bit 2 in the configuration register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h / Write	Don't Care	IDLE	Bit 1 in the configuration register determines if cycle passed through to 8042 and if SMI# generated.
IDLE	60h / Read	N/A	IDLE	Bit 0 in the configuration register determines if cycle passed through to 8042 and if SMI# generated.
GateState1	60h / Write	XXh	GateState2	Cycle passed through to 8042, even if trap enabled in Bit 1 in the configuration register. No SMI# generated. PSTATE remains 1. If data value is not DFh or DDh then the 8042 may chose to ignore it.
GateState1	64h / Write	D1h	GateState1	Cycle passed through to 8042, even if trap enabled via Bit 3 in the configuration register. No SMI# generated. PSTATE remains 1. Stay in GateState1 because this is part of the double-trigger sequence.
GateState1	64h / Write	Not D1h	ILDE	Bit 3 in the configuration register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in the configuration register is set, then SMI# should be generated.
GateState1	60h / Read	N/A	IDLE	This is an invalid sequence. Bit 0 in the configuration register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in the configuration register is set, then SMI# should be generated.
GateState1	64h / Read	N/A	GateState1	Just stay in same state. Generate an SMI# if enabled in Bit 2 of the configuration register. PSTATE remains 1.
GateState2	64 / Write	FFh	IDLE	Standard end of sequence. Cycle passed through to 8042. PSTATE goes to 0. Bit 7 in the Configuration Space determines if SMI# should be generated.
GateState2	64h / Write	Not FFh	IDLE	Improper end of sequence. Bit 3 in the configuration register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in the configuration register is set, then SMI# should be generated.
GateState2	64h / Read	N/A	GateState2	Just stay in same state. Generate an SMI# if enabled in Bit 2 of the configuration register. PSTATE remains 1.
GateState2	60h / Write	XXh	IDLE	Improper end of sequence. Bit 1 in the configuration register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in the configuration register is set, then SMI# should be generated.
GateState2	60h / Read	N/A	IDLE	Improper end of sequence. Bit 0 in the configuration register determines if cycle passed through to 8042 and if SMI# generated. PSTATE goes to 0. If Bit 7 in the configuration register is set, then SMI# should be generated.

5.17 SMBus 2.0 Controller Functional Description (D31:F3)

The ICH3 provides a *System Management Bus (SMBus) Specification*, Version 2.0-compliant Host Controller as well as an SMBus Slave Interface. The Host Controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). The ICH3 is also capable of operating in a mode in which it can communicate with I^2C* compatible devices.

The ICH3 can perform SMBus messages with either packet error checking (PEC) enabled or disabled. The actual PEC calculation and checking is performed in software.

The Slave Interface allows an external master to read from or write to the ICH3. Write cycles can be used to cause certain events or pass messages, and the read cycles can be used to determine the state of various status bits. The ICH3's internal Host Controller cannot access the ICH3's internal Slave Interface.

The ICH3 SMBus logic exists in Device 31:Function 3 configuration space, and consists of a transmit data path, and host controller. The transmit data path provides the data flow logic needed to implement the seven different SMBus command protocols and is controlled by the host controller. The ICH3 SMBus controller logic is clocked by RTC clock.

The SMBus Address Resolution Protocol (ARP) is supported by using the existing host controller commands through software, except for the new Host Notify command (which is actually a received message).

The programming model of the host controller is combined into two portions: a PCI configuration portion, and a system I/O mapped portion. All static configuration, such as the I/O base address, is done via the PCI configuration space. Real-time programming of the Host interface is done in system I/O space.

5.17.1 Host Controller

The SMBus Host Controller is used to send commands to other SMBus slave devices. Software sets up the host controller with an address, command, and, for writes, data and optional PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it will generate an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMBus interface (see System Management Bus Specifications): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

The SMBus Host Controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMBus Host Controller will perform the requested transaction, and interrupt the processor (or generate an SMI#) when the transaction is completed. Once a START command has been issued, the values of the "active registers" (i.e., host control, host command, transmit slave address, data 0, data 1) should not be changed or read until the interrupt status bit (INTR) has been set (indicating the completion of the command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMBus Host Controller will update all registers while completing the new command.

Using the SMB Host Controller to send commands to the ICH3's SMB slave port is supported.

The ICH3 supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, in order to be fully compliant with the *System Management Bus (SMBus) Specification*, Version 2.0 (which requires the Host Notify protocol), the SMLink and SMBus signals should be tied together externally.

5.17.1.1 Command Protocols

In all of the following commands, the Host Status Register (offset 00h) is used to determine the progress of the command. While the command is in operation, the HOST_BUSY bit is set. If the command completes successfully, the INTR bit will be set in the Host Status Register. If the device does not respond with an acknowledge, and the transaction times out, the DEV_ERR bit is set. If software sets the KILL bit in the Host Control Register while the command is running, the transaction will stop and the FAILED bit will be set.

Quick Command

When programmed for a Quick command, the Transmit Slave Address Register is sent. The PEC byte is never appended to the Quick protocol. Software should force the PEC_EN bit to 0 when performing the Quick command. The Quick command with I2C_EN set produces undefined results. Software should force the I2C_EN bit to 0 when performing the Quick command. The format of the protocol is shown in Table 5-77.

Table 5-77. Quick Protocol

Bit	Description
1	Start Condition
2–8	Slave Address–7 bits
9	Read / Write Direction
10	Acknowledge from slave
11	Stop

Send Byte / Receive Byte

For the Send Byte command, the Transmit Slave Address and Device Command Registers are sent For the Receive Byte command, the Transmit Slave Address Register is sent. The data received is stored in the Data 0 Register.

The Receive Byte is similar to a Send Byte, the only difference is the direction of data transfer. The format of the protocol is shown in Table 5-78. and Table 5-79. The Send Byte / Receive Byte command with I2C_EN set produces undefined results. Software should force the I2C_EN bit to 0 when running this command.

Table 5-78. Send / Receive Byte Protocol without PEC

Send Byte Protocol		Receive Byte Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Read
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Data byte from slave
19	Acknowledge from slave	19	NOT Acknowledge
20	Stop	20	Stop

Table 5-79. Send/Receive byte Protocol with PEC

Send Byte Protocol		Receive Byte Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Read
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Data byte from slave
19	Acknowledge from slave	19	Acknowledge
20–27-	PEC	20–27	PEC from slave
28	Acknowledge from slave	28	Not Acknowledge
29	Stop	29	Stop

Write Byte/Word

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a Write Byte/Word command, the transmit slave address, device command, and Data 0 Registers are sent. In addition, the Data 1 Register is sent on a Write Word command. The Write Byte / Word command with I2C_EN set produces undefined results. Software should force the I2C_EN bit to 0 when running this command. The format of the protocol is shown in Table 5-80 and Table 5-81.

Table 5-80. Write Byte/Word Protocol without PEC

Write Byte Protocol		Write Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Command code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20–27	Data Byte–8 bits	20–27	Data Byte Low–8 bits
28	Acknowledge from Slave	28	Acknowledge from Slave
29	Stop	29–36	Data Byte High–8 bits
		37	Acknowledge from slave
		38	Stop

Table 5-81. Write Byte/Word Protocol with PEC

Write Byte Protocol		Write Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Command code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20–27	Data Byte–8 bits	20–27	Data Byte Low–8 bits
28	Acknowledge from Slave	28	Acknowledge from Slave
29–36	PEC	29–36	Data Byte High–8 bits
37	Acknowledge from Slave	37	Acknowledge from slave
38	Stop	38–45	PEC
		46	Acknowledge from slave
		47	Stop

Read Byte/Word

Reading data is slightly more complicated than writing data. First the ICH3 must write a command to the slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The slave then returns 1 or 2 bytes of data.

When programmed for the Read Byte/Word command, the Transmit Slave Address and Device Command Registers are sent. Data is received into the data 0 on the read byte, and the Data 0 and Data 1 Registers on the Read Word command. The Read Byte / Word command with I2C_EN set produces undefined results. Software should force the I2C_EN bit to 0 when running this command. The format of the protocol is shown in Table 5-82 and Table 5-83.

Table 5-82. Read Byte/Word Protocol without PEC

Read Byte Protocol		Read Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Command code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20	Repeated Start	20	Repeated Start
21–27	Slave Address–7 bits	21–27	Slave Address–7 bits
28	Read	28	Read
29	Acknowledge from slave	29	Acknowledge from slave
30–37	Data from slave–8 bits	30–37	Data Byte Low from slave–8 bits
38	NOT acknowledge	38	Acknowledge
39	Stop	39–46	Data Byte High from slave–8 bits
		47	NOT acknowledge
		48	Stop

Table 5-83. Read Byte/Word Protocol with PEC

Read Byte Protocol		Read Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Command code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20	Repeated Start	20	Repeated Start
21–27	Slave Address–7 bits	21–27	Slave Address–7 bits
28	Read	28	Read
29	Acknowledge from slave	29	Acknowledge from slave
30–37	Data from slave–8 bits	30–37	Data Byte Low from slave–8 bits
38	Acknowledge	38	Acknowledge
39–46	PEC from slave	39–46	Data Byte High from slave–8 bits
47	NOT Acknowledge	47	Acknowledge
48	Stop	48–55	PEC from slave
		56	NOT acknowledge
		57	Stop

Process Call

The process call is so named because a command sends data and waits for the slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition.

When programmed for the Process Call command, the ICH3 transmits the Transmit Slave Address, Host Command, Data 0, and Data 1 Registers. Data received from the device is stored in the Data 0 and Data 1 Registers. The Process Call command with I2C_EN set and the PEC_EN bit set produces undefined results. Software must force either I2C_EN or PEC_EN to 0 when running this command. The format of the protocol is shown in Table 5-84 and Table 5-85.

Note: For Process Call command, the value written into bit 0 of the Transmit Slave Address Register (SMB I/O Register, offset 04h) needs to be 0.

Table 5-84. Process Call Protocol without PEC

Bit	Description
1	Start
2–8	Slave Address–7 bits
9	Write
10	Acknowledge from Slave
11–18	Command code–8 bits (skip this step if I2C_EN bit is set)
19	Acknowledge from slave (skip this step if I2C_EN bit is set)
20–27	Data byte Low–8 bits
28	Acknowledge from slave
29–36	Data Byte High–8 bits
37	Acknowledge from slave
38	Repeated Start
39–45	Slave Address–7 bits
46	Read
47	Acknowledge from slave
48–55	Data Byte Low from slave–8 bits
56	Acknowledge
57–64	Data Byte High from slave–8 bits
65	NOT acknowledge
66	Stop

Table 5-85. Process Call Protocol with PEC

Bit	Description
1	Start
2–8	Slave Address–7 bits
9	Write
10	Acknowledge from Slave
11–18	Command code–8 bits
19	Acknowledge from slave
20–27	Data byte Low–8 bits
28	Acknowledge from slave
29–36	Data Byte High–8 bits
37	Acknowledge from slave
38	Repeated Start
39–45	Slave Address–7 bits
46	Read
47	Acknowledge from slave
48–55	Data Byte Low from slave–8 bits
56	Acknowledge
57–64	Data Byte High from slave–8 bits
65	Acknowledge
66–73	PEC from slave
74	NOT acknowledge
75	Stop

Block Read/Write

The Block Write begins with a slave address and a write condition. After the command code, the ICH3 issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0.

Note that, unlike the PIIX4, which implements 32-byte buffer for Block Read/Write command, the ICH3 implements the block data byte register (D31:F3, I/O offset 07h) for Block Read/Write command.

When programmed for a Block Write command, the Transmit Slave Address, Host Command, and Data 0 (count) Registers are sent. Data is then sent from the block data byte register. After the byte has been sent, the ICH3 will set the BYTE_DONE_STS bit in the Host Status Register. If there are more bytes to send, the software will write the next byte to the block data byte register and will also clear the BYTE_DONE_STS bit. The ICH3 will then send the next byte. When doing a block write, first poll the BYTE_DONE_STS Register until it is set, then write the next byte, then clear the BYTE_DONE_STS Register.

On block read commands, after the byte count is stored in the Data 0 Register, the first data byte goes in the block data byte register; the ICH3 will then set the BYTE_DONE_STS bit and generate an SMI# or interrupt. The SMI# or interrupt handler will read the byte and then clear the BYTE_DONE_STS bit to allow the next byte to be read into the block data byte register. Note that

after receiving data byte N–1 of the block, the software needs to set the LAST_BYTE bit in the Host Control Register; this allows the ICH3 to send a NOT ACK (instead of an ACK) after receiving the last data byte (byte N) of the block.

After each byte of a block message the ICH3 sets the BYTE_DONE_STS bit and generates an interrupt or SMI#. Software clears the BYTE_DONE_STS bit before the next transfer occurs. When the interrupt handler clears the BYTE_DONE_STS bit after the last byte has been transferred, the ICH3 will set the INTR bit and generate another interrupt to signal the end of the block transfer. Thus, for a block message of n bytes, the ICH3 will generate n+1 interrupts. The interrupt handler needs to be implemented to handle all of these interrupts.

The format of the Block Read/Write protocol is shown in Table 5-86 and Table 5-87.

Note: For Block Write, if the I^2C_EN bit is set, the format of the command changes slightly. The ICH3 will still send the number of bytes indicated in the Data 0 Register. However, it will not send the contents of the Data 0 Register as part of the message. The Block Write command with I2C_EN set and the PEC_EN bit set produces undefined results. Software must force the PEC_EN bit to 0 when running this command.

Table 5-86. Block Read/Write Protocol without PEC

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Command code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20–27	Byte Count–8 bits (Skip this step if I2C_EN bit set)	20	Repeated Start
28	Acknowledge from Slave (Skip this step if I2C_EN bit set)	21–27	Slave Address–7 bits
29–36	Data Byte 1–8 bits	28	Read
37	Acknowledge from Slave	29	Acknowledge from slave
38–45	Data Byte 2–8 bits	30–37	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
...	Data Bytes / Slave Acknowledges...	39–46	Data Byte 1 from slave–8 bits
...	Data Byte N–8 bits	47	Acknowledge
...	Acknowledge from Slave	48–55	Data Byte 2 from slave–8 bits
...	Stop	56	Acknowledge
		...	Data Bytes from slave/Acknowledge
		...	Data Byte N from slave–8 bits
		...	NOT Acknowledge
		...	Stop

Table 5-87. Block Read/Write Protocol with PEC

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2–8	Slave Address–7 bits	2–8	Slave Address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11–18	Command code–8 bits	11–18	Command code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20–27	Byte Count–8 bits (Skip this step if I2C_EN bit set)	20	Repeated Start
28	Acknowledge from Slave (Skip this step if I2C_EN bit set)	21–27	Slave Address–7 bits
29–36	Data Byte 1–8 bits	28	Read
37	Acknowledge from Slave	29	Acknowledge from slave
38–45	Data Byte 2–8 bits	30–37	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
...	Data Bytes / Slave Acknowledges...	39–46	Data Byte 1 from slave–8 bits
...	Data Byte N–8 bits	47	Acknowledge
...	Acknowledge from Slave	48–55	Data Byte 2 from slave–8 bits
...	PEC–8 bits	56	Acknowledge
...	Acknowledge from Slave	...	Data Bytes from slave/Acknowledge
...	Stop	...	Data Byte N from slave–8 bits
		...	Acknowledge
		...	PEC from slave–8 bits
		...	NOT Acknowledge
		...	Stop

5.17.1.2 I²C Behavior

When the I2C _EN bit is set, the ICH3 SMBus logic is instead set to communicate with I²C devices. This forces the following changes:

1. The Process Call command skips the Command code (and its associated acknowledge)
2. The Block Write command skips sending the Byte Count (data 0)

5.17.1.3 Heartbeat for Use with the External LAN Controller

This method allows the ICH3 to send messages to an *external* LAN Controller when the processor is otherwise unable to do so. It uses the SMLINK I/F between the ICH3 and the external LAN Controller. The actual Heartbeat message is a Block Write. Only 8 bytes are sent.

5.17.2 Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving the SMBDATA line low to signal a start condition. The ICH3 must continuously monitor the SMBDATA line. When the ICH3 is attempting to drive the bus to a 1 by letting go of the SMBDATA line, and it samples SMBDATA low, then some other master is driving the bus and the ICH3 must stop transferring data.

If the ICH3 sees that it has lost arbitration, the condition is called a collision. The ICH3 sets the BUS_ERR bit in the Host Status Register, and if enabled, generates an interrupt or SMI#. The processor is responsible for restarting the transaction.

When the ICH3 is a SMBus master, it drives the clock. When the ICH3 is sending address or command as an SMBus master, or data bytes as a master on writes, it drives data relative to the clock it is also driving. It does not start toggling the clock until the start or stop condition meets proper setup and hold time. The ICH3 also guarantees minimum time between SMBus transactions as a master.

The ICH3 supports the same arbitration protocol for both the SMBus and the System Management (SMLINK) interfaces.

5.17.3 Bus Timing

5.17.3.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that the ICH3 as an SMBus master would like. They have the capability of stretching the low time of the clock. When the ICH3 attempts to release the clock (allowing the clock to go high), the clock remains low for an extended period of time.

The ICH3 must monitor the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

5.17.3.2 Bus Time Out (Intel® ICH3 as SMBus Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. The ICH3 will discard the cycle, and set the DEV_ERR bit. The time out minimum is 25 ms. The time-out counter inside the ICH3 starts after the last bit of data is transferred by the ICH3 and it is waiting for a response. The 25 ms is a count of 800 RTC clocks.

5.17.4 Interrupts / SMI#

The ICH3 SMBus controller uses PIRQB# as its interrupt pin. However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMBUS_SMI_EN bit.

Table 5-89 and Table 5-90 specify how the various enable bits in the SMBus function control the generation of the interrupt, Host and Slave SMI, and Wake internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario then the Results for all of the activated rows will occur.

Table 5-88. Enable for SMBALERT#

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit 1)	SMBALERT_DIS (Slave Command I/O Register, Offset 11h, Bit 2)	Result
SMBALERT# asserted low (always reported in Host Status Register, Bit 5)	X	X	X	Wake generated
	X	1	0	Slave SMI# generated (SMBUS_SMI_STS)
	1	0	0	Interrupt generated

Table 5-89. Enables for SMBus Slave Write and SMBus Host Events

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit1)	Result
Slave Write to Wake/ SMI# Command	X	X	Wake generated when asleep. Slave SMI# generated when awake (SMBUS_SMI_STS).
Slave Write to SMLINK_SLAVE_SMI Command	X	X	Slave SMI# generated when in the S0 state (SMBUS_SMI_STS)
Any combination of Host Status Register [4:1] asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

Table 5-90. Enables for the Host Notify Command

HOST_NOTIFY_INTREN (Slave Control I/O Register, Offset 11h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Off40h, Bit 1)	HOST_NOTIFY_WKEN (Slave Control I/O Register, Offset 11h, Bit 1)	Result
0	X	0	None
X	X	1	Wake generated
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

5.17.5 SMBALERT#

SMBALERT# is multiplexed with GPIO[11]. When enable and the signal is asserted, The ICH3 can generate an interrupt, an SMI# or a wake event from S1–S4.

Note: Any event on SMBALERT# (regardless whether it is programmed as a GPIO or not), causes the event message to be sent in “heartbeat mode.”

5.17.6 SMBus Slave Interface

The ICH3’s SMBus Slave interface is accessed via the SMLINK[1:0] signals. The SMBus slave logic will not generate or handle receiving the PEC byte and will only act as a Legacy Alerting Protocol (Alert on LAN) device. The slave interface allows the ICH3 to decode cycles, and allows an external microcontroller to perform specific actions. Key features and capabilities include:

- Supports decode of three types of messages: Byte Write, Byte Read, and Host Notify
- Receive Slave Address Register: This is the address that the ICH3 decodes. A default value is provided so that the slave interface can be used without the processor having to program this register.
- Receive Slave Data Register in the SMBus I/O space that includes the data written by the external microcontroller
- Registers that the external microcontroller can read to get the state of the ICH3. See Table 5-95
- Status bits to indicate that the SMLink/SMBus slave logic caused an interrupt or SMI# due to the reception of a message that matched the slave address.
  - — Bit 0 of the Slave Status Register for the Host Notify command
  - — Bit 16 of the SMI Status Register (Section 9.8.3.12) for all others

If a master leaves the clock and data bits of the SMLink interface at '1' for 50 µs or more in the middle of a cycle, the ICH3 slave logic's behavior is undefined. This is interpreted as an unexpected idle and should be avoided when performing management activities to the slave logic.

When an external microcontroller accesses the SMBus Slave Interface over the SMLink, a translation in the address is needed to accommodate the least significant bit used for read/write control. For example, if the ICH3 slave address (RCV_SLVA) is left at 44h (default), the external microcontroller would use an address of 88h/89h (write/read).

5.17.6.1 Format of Slave Write Cycle

The external master performs Byte Write commands to the ICH3 SMBus Slave I/F. The "command" field (bits 11–18) indicate which register is being accessed. The Data field (bits 20–27) indicate the value that should be written to that register.

The Write Cycle format is shown below in Table 5-91. Table 5-92 has the values associated with the registers.

Table 5-91. Slave Write Cycle Format

Bits	Description	Driven by	Comment
1	Start Condition	External Microcontroller	
2–8	Slave Address–7 bits	External Microcontroller	Must match value in Receive Slave Address Register
9	Write	External Microcontroller	Always 0
10	ACK	ICH3	
11–18	Command	External Microcontroller	This field indicates which register will be accessed. See Table 5-92 below for the register definitions
19	ACK	ICH3	
20–27	Register Data	External Microcontroller	See Table 5-92 below for the register definitions
28	ACK	ICH3	
29	Stop	External Microcontroller	

Table 5-92. Slave Write Registers

Register	Function
0	Command Register. See Table 5-93 for legal values written to this register.
1–3	Reserved
4	Data Message Byte 0
5	Data Message Byte 1
6–7	Reserved
8	Frequency Straps will be written on bits 3:0. Bits 7:4 should be 0, but will be ignored.
9–FFh	Reserved

NOTE: The external microcontroller is responsible to make sure that it does not update the contents of the data byte registers until they have been read by the system processor. The ICH3 will overwrite the old value with any new value received. A race condition is possible where the new value is being written to the register just at the time it is being read. ICH3 will not attempt to cover this race condition (i.e., unpredictable results in this case).

Table 5-93. Command Types

Command Type	Description
0	Reserved
1	**WAKE/SMI#:** Wake system if it is not already awake. If system is already awake, then an SMI# will be generated. **Note:** The SMB_WAK_STS bit will be set by this command, even if the system is already awake. The SMI handler should then clear this bit.
2	**Unconditional Powerdown:** This command sets the PWRBTNOR_STS bit, and has the same effect as the Powerbutton Override occurring.
3	**HARD RESET WITHOUT CYCLING:** The will cause a hard reset of the system (does not include cycling of the power supply). This is equivalent to a write to the CF9h register with bits 2:1 set to 1, but bit 3 set to 0.
4	**HARD RESET SYSTEM:** The will cause a hard reset of the system (including cycling of the power supply). This is equivalent to a write to the CF9h register with bits 3:1 set to 1.
5	**Disable the TCO Messages.** This command will disable the ICH3 from sending Heartbeat and Event messages (as described in Section 5.13.2). Once this command has been executed, Heartbeat and Event message reporting can only be re-enabled by assertion and deassertion of the RSMRST# signal.
6	**WD RELOAD:** Reload watchdog timer.
7	Reserved
8	SMLINK_SLV_SMI. When ICH3 detects this command type while in the S0 state, it sets the SMLINK_SLV_SMI_STS bit (see Section 9.9.8). This command should only be used if the system is in an S0 state. If the message is received during S1–S5 states, the ICH3 acknowledges it, but the SMLINK_SLV_SMI_STS bit does not get set. **Note:** It is possible that the system transitions out of the S0 state at the same time that the SMLINK_SLV_SMI command is received. In this case, the SMLINK_SLV_SMI_STS bit may get set but not serviced before the system goes to sleep. Once the system returns to S0, the SMI associated with this bit would then be generated. Software must be able to handle this scenario.
9–FFh	Reserved

5.17.6.2 Format of Read Command

The external master performs Byte Read commands to the ICH3 SMBus Slave I/F. The "Command" field (bits 11–18) indicate which register is being accessed. The Data field (bits 30–37) contain the value that should be read from that register.

Table 5-94 shows the Read Cycle format. Table 5-95 shows the register mapping for the data byte.

Table 5-94. Read Cycle Format

Bit	Description	Driven By	Comment
1	Start	External Microcontroller	
2–8	Slave Address–7 bits	External Microcontroller	Must match value in Receive Slave Address Register
9	Write	External Microcontroller	Always 0
10	ACK	ICH3	
11–18	Command code – 8 bits	External Microcontroller	Indicates which register is being accessed. See Table 5-95.
19	ACK	ICH3	
20	Repeated Start	External Microcontroller	
21–27	Slave Address–7 bits	External Microcontroller	Must match value in Receive Slave Address Register
28	Read	External Microcontroller	Always 1
29	ACK	ICH3	
30–37	Data Byte	ICH3	Value depends on register being accessed. See Table 5-95.
38	NOT ACK	External Microcontroller	
39	Stop	External Microcontroller	

Table 5-95. Data Values for Slave Read Registers

Register	Bits	Description
0	7:0	Reserved.
1	2:0	System Power State 000 = S0 001 = S1 010 = Reserved 011 = S3 100 = S4 101 = S5 110 = Reserved 111 = Reserved
1	7:3	Reserved
2	3:0	Frequency Strap Register
2	7:4	Reserved
3	5:0	Watchdog Timer current value
3	7:6	Reserved
4	0	1 = The Intruder Detect (INTRD_DET) bit is set. This indicates that the system cover has probably been opened.
4	1	1 = BTI Temperature Event occurred. This bit will be set if the ICH3's THRM# input signal is active. Need to take after polarity control.
4	2	Boot-Status. This bit will be 1 when boot failed
4	3	This bit will be set after the TCO timer times out a second time (Both TIMEOUT and SECOND_TO_STS bits set).
4	6:4	Reserved.
4	7	The bit will reflect the state of the GPI[11]/SMBALERT# signal, and will depend on the GP_INV[11] bit. It does not matter if the pin is configured as GPI[11] or SMBALERT#. • If the GP_INV[11] bit is 1 then the value of register 4, bit 7 will equal the level of the GPI[11]/SMBALERT# pin (high = 1, low = 0). • If the GP_INV[11] bit is 0 then the value of register 4, bit 7 will equal the inverse of the level of the GPI[11]/SMBALERT# pin (high = 1, low = 0).
5	0	Unprogrammed FWH bit. This bit will be 1 to indicate that the first BIOS fetch returned FFh, which indicates that the FWH is probably blank.
5	7:1	Reserved
6	7:0	Contents of the Message 1 register. See Section 9.9.10.
7	7:0	Contents of the Message 2 register. See Section 9.9.10.
8	7:0	Contents of the WDSTATUS register. See Section 9.9.11.
9–FFh	7:0	Reserved

5.17.6.2.1 Behavioral Notes

According to SMBus protocol, Read and Write messages always begin with a start bit–address–write bit sequence. When the ICH3 detects that the address matches the value in the Receive Slave Address Register, it will assume that the protocol is always followed and ignore the write bit (bit 9) and signal an Acknowledge during bit 10 (See Table 5-91 and Table 5-94). In other words, if a Start–Address–Read occurs (which is illegal for SMBus Read or Write protocol), and the address matches the ICH3's Slave Address, the ICH3 will still grab the cycle.

Also according to SMBus protocol, a Read cycle contains a Repeated Start–Address–Read sequence beginning at bit 20 (See Table 5-94). Once again, if the Address matches the ICH3's Receive Slave Address, it will assume that the protocol is followed, ignore bit 28, and proceed with the Slave Read cycle.

Note: An external microcontroller must not attempt to access the ICH3's SMBus Slave logic until at least 1 second after both RTCRST# and RSMRST# are deasserted (high).

5.17.6.3 Format of Host Notify Command

The ICH3 tracks and responds to the standard Host Notify command as specified in the SMBus 2.0 specification. The host address for this command is fixed to 0001000b. If the ICH3 already has data for a previously-received host notify command which has not been serviced yet by the host software (as indicated by the HOST_NOTIFY_STS bit), then it will NACK following the host address byte of the protocol. This allows the host to communicate non-acceptance to the master and retain the host notify address and data values for the previous cycle until host software completely services the interrupt.

Note: Host software must always clear the HOST_NOTIFY_STS bit after completing any necessary reads of the address and data registers.

Table 5-96 shows the Host Notify format.

Table 5-96. Host Notify Format

Bit	Description	Driven by	Comment
1	Start	External Master	
2–8	SMB Host Address–7 bits	External Master	Always 0001_000
9	Write	External Master	Always 0
10	ACK (or NACK)	ICH3	ICH3 NACKs if HOST_NOTIFY_STS is 1
11–17	Device Address – 7 bits	External Master	Indicates the address of the master; loaded into the notify device address register
18	Unused–Always 0	External Master	7-bit-only address; this bit is inserted to complete the byte
19	ACK	ICH3	
20–27	Data Byte Low–8 bits	External Master	Loaded into the notify Data Low Byte Register
28	ACK	ICH3	
29–36	Data Byte High–8 bits	External Master	Loaded into the notify Data High Byte Register
37	ACK	ICH3	
38	Stop	External Master	

5.18 AC ’97 Controller Functional Description (Audio D31:F5, Modem D31:F6)

Note: All references to AC ’97 in this document refer to the *Audio Codec ’97*, Revision 2.2 specification. For further information on the operation of the AC-link protocol, please see the *Audio Codec ’97*, Revision 2.2 specification.

The ICH3 AC ’97 Controller features include:

- Independent PCI functions for audio and modem.
- Independent bus master logic for Mic input, PCM Audio input (2-channel stereo), PCM audio output (2, 4 or 6-channel stereo), Modem input and Modem output.
- 16-bit sample resolution
- Multiple sample rates up to 48 kHz
- 16 GPIOs
- Single modem line
- Dual codec configuration with two SDIN pins

Table 5-97 shows a detailed list of features supported by the ICH3 AC ’97 digital controller.

Table 5-97. Features Supported by Intel® ICH3

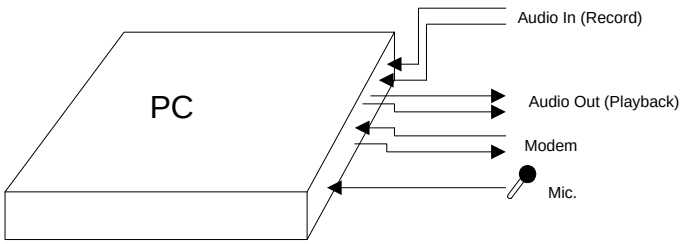
Feature	Description
System Interface	• Isochronous low latency bus master memory interface • Scatter/gather support for word-aligned buffers in memory (all mono or stereo 16-bit data types are supported, no 8-bit data types are supported) • Data buffer size in system memory from 3 to 65535 samples per input • Data buffer size in system memory from 0 to 65535 samples per output • Independent PCI audio and modem functions with configuration and I/O spaces • AC ’97 codec registers are shadowed in system memory via driver (not PCI I/O space) • AC ’97 codec register accesses are serialized via semaphore bit in PCI I/O space (new accesses are not allowed while a prior access is still in progress)
Power Management	• Power management via ACPI control methods Support for audio states: *D0, D2, D3hot, D3cold* Support for modem states: *D0, D3hot, D3cold* • SCI event generation for PCI modem function with wake-up from *D3cold* • Independent codec D3 w/ Link down event, synchronized via two-bit semaphore (in PCI I/O Space)
PCI Audio Function	• Read/write access to audio codec registers 00h–3Ah and vendor registers 5Ah–7Eh • 16-bit stereo PCM output, up to 48 kHz (L,R, Center, Sub-woofer, L-rear and R-rear channels on slots 3,4,6,7,8.9) • 16-bit stereo PCM input, up to 48 kHz (L,R channels on slots 3,4) • 16-bit mono mic in w/ or w/o mono mix, up to 48 kHz (L,R channel, slots 3,4) (mono mix supports mono hardware AEC reference for speakerphone) • 16-bit mono PCM input, up to 48 kHz from dedicated mic ADC (slot 6) (supports speech recognition or stereo hardware AEC ref for speakerphone) • During cold reset AC_RST# is held low until after POST and software deassertion of AC_RST# (supports passive PC_BEEP to speaker connection during POST)

Table 5-97. Features Supported by Intel® ICH3 (Continued)

Feature	Description
PCI Modem Function	• Read/write access to modem codec registers 3Ch–58h and vendor registers 5Ah–7Eh • 16-bit mono modem line1 output and input, up to 48 kHz (slot 5) • Low latency GPIO[15:0] via hardwired update between slot 12 and PCI I/O register • Programmable PCI interrupt on modem GPIO input changes via slot 12 GPIO_INT • SCI event generation on primary or secondary SDIN wake-up signal
AC-Link	• *Audio Codec '97*, Revision 2.2 compliant AC-link interface • Variable sample rate output support via AC '97 SLOTREQ protocol (slots 3,4,5,6,7,8,9) • Variable sample rate input support via monitoring of slot valid tag bits (slots 3,4,5,6) • 3.3 V digital operation meets *Audio Codec '97*, Revision 2.2 DC switching levels • AC-Link I/O driver capability meets *Audio Codec '97*, Revision 2.2 dual codec specifications • Codec register status reads must be returned with data in the next AC-link frame, per *Audio Codec '97*, Revision 2.2.
Multiple Codec	• Dual codec addressing: All AC '97 codec register accesses are addressable to codec ID 00 (primary) or codec ID 01 (secondary) • Dual codec receive capability via primary and secondary SDIN pins (primary, secondary SDIN frames are internally validated, synch'd, and OR'd)

Note: Throughout this document, references to D31:F5 indicate that the audio function exists in PCI Device 31, Function 5. References to D31:F6 indicate that the modem function exists in PCI Device 31, Function 6.

Figure 5-19. Intel® ICH3 Based Audio Codec '97, Revision 2.2

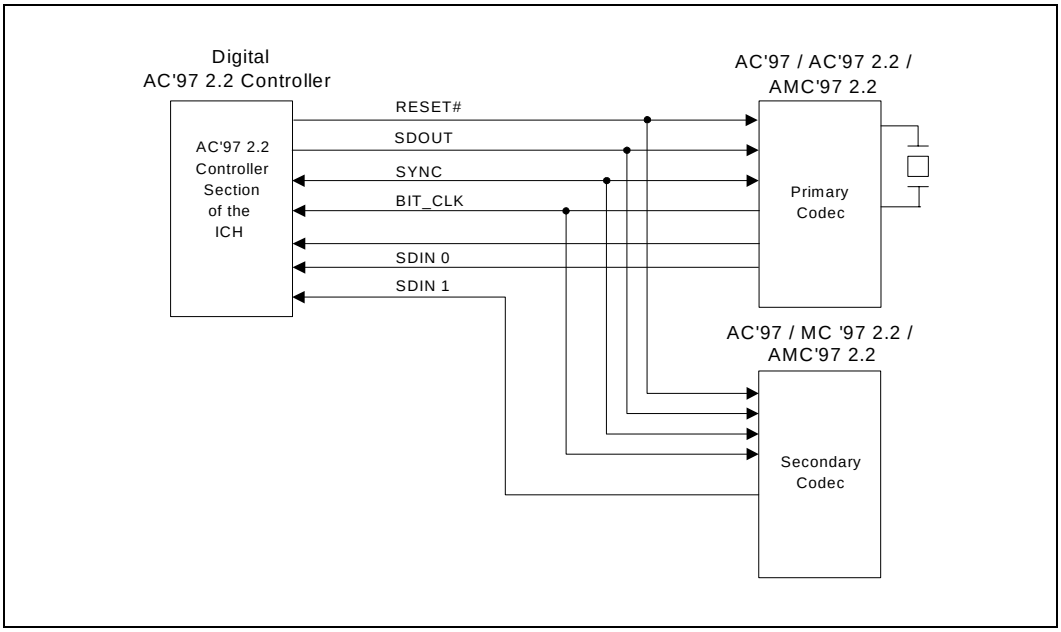


5.18.1 AC-Link

The ICH3 is an *Audio Codec '97*, Revision 2.2 controller that communicates with companion codecs via a digital serial link called the AC-link. All digital audio/modem streams and command/status information is communicated over the AC-link.

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH3 AC-link allows a maximum of two codecs to be connected. Figure 5-20 shows a two codec topology of the AC-link for the ICH3.

Figure 5-20. Audio Codec '97, Revision 2.2 Controller-Codec Connection



The AC-link consists of a five signal interface between the controller and codec. Table 5-98 indicates the AC-link signal pins on the ICH3 and their associated power wells.

Table 5-98. AC '97 Signals

Signal Name	Type	Power Well[1]	Description
AC_RESET#	Output	Resume	Master hardware reset
AC_SYNC	Output	Core	48 kHz fixed rate sample sync
AC_BIT_CLK	Input	Core	12.288 MHz Serial data clock
AC_SDOUT	Output	Core	Serial output data
AC_SDIN 0	Input	Resume	Serial input data
AC_SDIN 1	Input	Resume	Serial input data

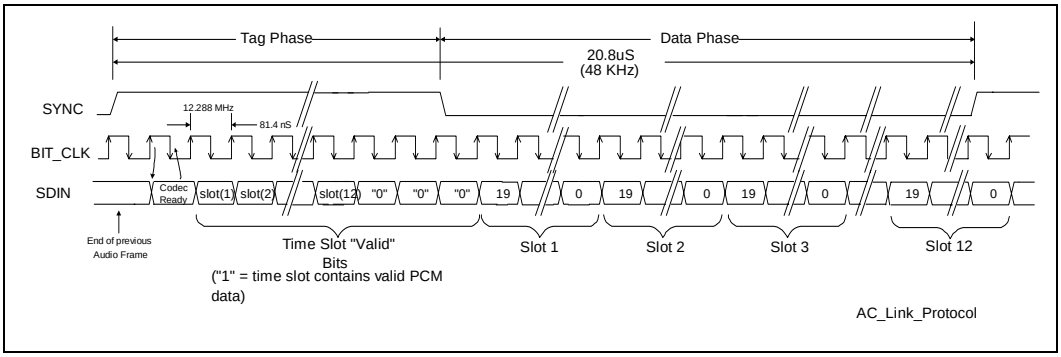
NOTES:
1. Power well voltage levels are 3.3 V

ICH3 core well outputs may be used as strapping options for the ICH3, sampled during system reset. These signals may have weak pullups/pulldowns on them, however this will not interfere with link operation. ICH3 inputs integrate weak pulldowns to prevent floating traces when a secondary codec is not attached. When the shut off bit in the control register is set, all buffers will be turned off and the pins will be held in a steady state, based on these pullups/pulldowns.

BIT_CLK is fixed at 12.288 MHz and is sourced by the primary codec. It provides the necessary clocking to support the twelve, 20-bit time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data samples each serial bit on the falling edge of BIT_CLK.

Synchronization of all AC-link data transactions is signaled by the AC ’97 controller via the AC_SYNC signal, as shown in Figure 5-21. The primary codec drives the serial bit clock onto the AC-link, which the AC ’97 controller then qualifies with the AC_SYNC signal to construct data frames. AC_SYNC, fixed at 48 kHz, is derived by dividing down BIT_CLK. AC_SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each frame. The portion of the frame where AC_SYNC is high is defined as the tag phase. The remainder of the frame where AC_SYNC is low is defined as the data phase. Each data bit is sampled on the falling edge of BIT_CLK.

Figure 5-21. AC-Link Protocol



The ICH3 has two SDIN pins allowing a single or dual codec configuration. When two codecs are connected, the primary and secondary codecs can be connected to either SDIN line, however it is recommended that the primary codec be attached to SDIN [0]. The ICH3 does not distinguish between primary and secondary codecs on its SDIN[1:0] pins, however the registers do distinguish between SDIN[0] and SDIN[1] for wake events, etc. The primary codec can be an AC (audio codec), MC (modem codec), or AMC (audio/modem codec) device. The secondary codec can be an AC, MC, or AMC device.

The MC can be either on the primary or the secondary codec, while the AC can be either on the primary or the secondary codec, or BOTH the primary or the secondary codec.

The ICH3 does not support optional test modes as outlined in the *Audio Codec ’97*, Revision 2.2 specification.

5.18.1.1 AC-Link Output Frame (SDOUT)

A new audio output frame begins with a low to high transition of AC_SYNC. AC_SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the codec samples the assertion of AC_SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new frame. On the next rising edge of BIT_CLK, the ICH3 transitions SDOUT into the first bit position of slot 0, or the valid frame bit. Each new bit position is presented to the AC-link on a rising edge of BIT_CLK, and subsequently sampled by the codec on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

The output frame data phase corresponds to the multiplexed bundles of all digital output data targeting codec DAC inputs and control registers. Each output frame supports up to twelve outgoing data time slots. The ICH3 generates 16-bit samples and, in compliance with the *Audio Codec '97*, Revision 2.2 specification, pads the four least significant bits of valid slots with zeros.

The output data stream is sent with the most significant bit first, and all invalid slots are stuffed with zeros. When mono audio sample streams are output from the ICH3, software must ensure both left and right sample stream time slots are filled with the same data.

5.18.1.2 Output Slot 0: Tag Phase

Slot 0 is considered the tag phase. The tag phase is a special 16-bit time slot wherein each bit conveys a valid tag for its corresponding time slot within the current frame. A one in a given bit position of slot 0 indicates that the corresponding time slot within the current frame has been assigned to a data stream and contains valid data. If a slot is tagged invalid with a zero in the corresponding bit position of slot 0, the ICH3 stuffs the corresponding slot with zeros during that slot's active time.

Within slot 0, the first bit is a valid frame bit (slot 0, bit 15) which flags the validity of the entire frame. If the valid frame bit is set to one, this indicates that the current frame contains at least one slot with valid data. When there is no transaction in progress, the ICH3 will deassert the frame valid bit. Note that after a write to slot 12, that slot will always stay valid, and therefore the frame valid bit will remain set.

The next 12 bit positions of slot 0 (bits [14:3]) indicate which of the corresponding twelve time slots contain valid data. Bits [1:0] of slot 0 are used as codec ID bits to distinguish between separate codecs on the link.

Using the valid bits in the tag phase allows data streams of differing sample rates to be transmitted across the link at its fixed 48 kHz frame rate. The codec can control the output sample rate of the ICH3 using the SLOTREQ bits as described in the *Audio Codec '97*, Revision 2.2 specification.

5.18.1.3 Output Slot 1: Command Address Port

The command port is used to control features and monitor status of AC ’97 functions including, but not limited to, mixer settings and power management.

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid.

Output frame slot 1 communicates control register address, and Write/Read command information.

In the case of the split codec implementation, accesses to the codecs are differentiated by the driver using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec. The differentiation on the link, however, is done via the codec ID bits. See Section 5.18.1.23 for further details.

5.18.1.4 Output Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle as indicated in slot 1, bit 19. If the current command port operation is a read then the entire slot time stuffed with 0s by the ICH3. Bits [19:4] contain the write data. Bits [3:0] are reserved and are stuffed with zeros.

5.18.1.5 Output Slot 3: PCM Playback Left Channel

Output frame slot 3 is the composite digital audio left playback stream. Typically this slot is composed of standard PCM (.wav) output samples digitally mixed by the host processor. The ICH3 transmits sample streams of 16 bits and stuffs the remaining bits with zeros.

Data in output slots 3 and 4 from the ICH3 should be duplicated by software if there is only a single channel out.

5.18.1.6 Output Slot 4: PCM Playback Right Channel

Output frame slot 4 is the composite digital audio right playback stream. Typically this slot is composed of standard PCM (.wav) output samples digitally mixed by the host processor. The ICH3 transmits sample streams of 16 bits and stuffs the remaining bits with zeros.

Data in output slots 3 and 4 from the ICH3 should be duplicated by software if there is only a single channel out.

5.18.1.7 Output Slot 5: Modem Codec

Output frame slot 5 contains modem DAC data. The modem DAC output supports 16-bit resolution. At boot time, if the modem codec is supported, the AC ’97 controller driver determines the DAC resolution. During normal runtime operation the ICH3 stuffs trailing bit positions within this time slot with zeros.

5.18.1.8 Output Slot 6: PCM Playback Center Front Channel

When set up for 6 channel mode, this slot is used for the front center channel. The format is the same as Slots 3. If not set up for 6 channel mode, this channel will always be stuffed with 0s by ICH3.

5.18.1.9 Output Slots 7–8: PCM Playback Left and Right Rear Channels

When set up for 4 or 6 channel modes, slots 7 and 8 are used for the rear Left and Right channels. The format for these two channels are the same as Slots 3 and 4.

5.18.1.10 Output Slot 9: Playback SubWoofer Channel

When set for 6 channel mode, this slot is used for the SubWoofer. The format is the same as Slots 3. If not set up for 6 channel mode, this channel will always be stuffed with 0s by ICH3.

5.18.1.11 Output Slots 10–11: Reserved

Output frame slots 10–11 are reserved and are always stuffed with 0s by the ICH3 AC ’97 controller.

5.18.1.12 Output Slot 12: I/O Control

Sixteen bits of DAA and GPIO control (output) and status (input) have been directly assigned to bits on slot 12 in order to minimize latency of access to changing conditions.

The value of the bits in this slot are the values written to the GPIO control register at offset 54h and D4h (in the case of a secondary codec) in the modem codec I/O space. The following rules govern the usage of slot 12.

1. Slot 12 is marked invalid by default on coming out of AC-link reset, and will remain invalid until a register write to 54h/D4h.
2. A write to offset 54h/D4h in codec I/O space will cause the write data to be transmitted on slot 12 in the next frame, with slot 12 marked valid, and the address/data information to also be transmitted on slots 1 and 2.
3. After the first write to offset 54h/D4h, slot 12 remains valid for all following frames. The data transmitted on slot 12 is the data last written to offset 54h/D4h. Any subsequent write to the register will cause the new data to be sent out on the next frame.
4. Slot 12 will get invalidated after the following events: PCI reset, AC ’97 cold reset, warm reset, and hence a wake from S3, S4, or S5. Slot 12 will remain invalid until the next write to offset 54h/D4h.

5.18.1.13 AC-Link Input Frame (SDIN)

There are two SDIN lines on the ICH3 for use with a primary and secondary codec. Each SDIN pin can have a codec attached. Depending upon which codec (AC, MC, or AMC) is attached, various slots will be valid or invalid. The data slots on the two inputs must be completely orthogonal (except for the tag slot 0); that is, no two data slots at the same location will be valid on both lines. This precludes the use of two similar codecs, such as two ACs or MCs, which use the same time slots.

The input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC ’97 controller. As in the case for the output frame, each AC-link input frame consists of twelve time slots.

A new audio input frame begins with a low to high transition of AC_SYNC. AC_SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the receiver samples the assertion of AC_SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the codec transitions SDIN into the first bit position of slot 0 (codec ready bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the ICH3 on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDIN data stream must follow the *Audio Codec ’97*, Revision 2.2 specification and be MSB-justified with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with zeros. SDIN data is sampled by the ICH3 on the falling edge of BIT_CLK.

5.18.1.14 Input Slot 0: Tag Phase

Input slot 0 consists of a codec ready bit (bit 15), and slot valid bits for each subsequent slot in the frame (bits [14:3]).

The codec ready bit within slot 0 (bit 15) indicates whether the codec on the AC-link is ready for operation. If the codec ready bit in slot 0 is a zero, the codec is not ready for normal operation. When the AC-link codec ready bit is a 1, it indicates that the AC-link and codec control and status registers are in a fully operational state. The codec ready bits are visible through the global status register of the ICH3. Software must further probe the powerdown control/status register in the codec to determine exactly which subsections, if any, are ready.

Bits [14:3] in slot 0 indicate which slots of the input stream to the ICH3 contain valid data, just as in the output frame. The remaining bits in this slot are stuffed with zeros.

5.18.1.15 Input Slot 1: Status Address Port / Slot Request Bits

The status port is used to monitor status of codec functions including, but not limited to, mixer settings and power management.

Slot 1 must echo the control register index, for historical reference, for the data to be returned in slot 2, assuming that slots 1 and 2 had been tagged valid by the codec in slot 0.

For multiple sample rate output, the codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDOUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current audio input frame signal which output slots require data from the controller in the next audio output frame. For fixed 48 kHz operation the SLOTREQ bits are always set active (low) and a sample is transferred each frame.

For multiple sample rate input, the tag bit for each input slot indicates whether valid data is present or not.

Table 5-99. Input Slot 1 Bit Definitions

Bit	Description
19	Reserved (Set to zero)
18:12	Control Register Index (Stuffed with zeros if tagged invalid)
11	Slot 3 Request: PCM Left Channel (see note 1)
10	Slot 4 Request: PCM Right Channel (see note 1)
9	Slot 5 Request: Modem Line 1
8	Slot 6 Request: PCM Center Channel (see note 1)
7	Slot 7 Request: PCM Left Surround (see note 1)
6	Slot 8 Request: PCM Right Surround (see note 1)
5	Slot 9 Request: PCM LFE Channel (see note 1)
4:2	Slot Request 10–12: Not Implemented
1:0	Reserved (Stuffed with zeros)

NOTES:
1. Slot 3 Request and Slot 4 Request bits must be the same value, i.e., set or cleared in tandem. This is also true for the Slot 7 and Slot 8 Request bits, as well as the Slot 6 and Slot 9 Request bits.

As shown in Table 5-99, slot 1 delivers codec control register read address and multiple sample rate slot request flags for all output slots of the controller. When a slot request bit is set by the codec, the controller will return data in that slot in the next output frame. Slot request bits for slots 3 and 4 are always set or cleared in tandem, i.e., both are set or cleared.

When set, the input slot 1 tag bit only pertains to Status Address Port data from a previous read. SLOTREQ bits are always valid independent of the slot 1 tag bit.

5.18.1.16 Input Slot 2: Status Data Port

The status data port receives 16-bit control register read data.

- Bit [19:4]: Control Register Read Data
- Bit [3:0]: Reserved.

5.18.1.17 Input Slot 3: PCM Record Left Channel

Input slot 3 is the left channel input of the codec. The ICH3 supports 16-bit sample resolution. Samples transmitted to the ICH3 must be in left/right channel order.

5.18.1.18 Input Slot 4: PCM Record Right Channel

Input slot 4 is the right channel input of the codec. The ICH3 supports 16-bit sample resolution. Samples transmitted to the ICH3 must be in left/right channel order.

5.18.1.19 Input Slot 5: Modem Line

Input slot 5 contains MSB justified modem data. The ICH3 supports 16-bit sample resolution.

5.18.1.20 Input Slot 6: Optional Dedicated Microphone Record Data

Input slot 6 is a third PCM system input channel available for dedicated use by a microphone. This input channel supplements a true stereo output which enables more precise echo cancellation algorithm for speakerphone applications. The ICH3 supports 16-bit resolution for slot 6 input.

5.18.1.21 Input Slots 7–11: Reserved

Input frame slots 7–11 are reserved for future use and should be stuffed with zeros by the codec, per the *Audio Codec '97*, Revision 2.2 specification.

5.18.1.22 Input Slot 12: I/O status

The status of the GPIOs configured as inputs are to be returned on this slot in every frame. The data returned on the latest frame is accessible to software by reading the register at offset 54h/D4h in the codec I/O space. Only the 16 MSBs are used to return GPI status. Bit 0 of this slot indicates the GPI status. Whenever a GPI changes state, this bit gets set for one frame by the codec. This bit can cause an interrupt to the processor if enabled via the global control register.

Reads from 54h/D4h will not be transmitted across the link in slot 1 and 2. The data from the most recent slot 12 is returned on reads from offset 54h/D4h.

5.18.1.23 Register Access

In the ICH3 implementation of the AC-link, up to two codecs can be connected to the SDOUT pin. The following mechanism is used to address the primary and secondary codecs individually.

The primary device uses bit 19 of slot 1 as the direction bit to specify read or write. Bits [18:12] of slot 1 are used for the register index. For I/O writes to the primary codec, the valid bits [14:13] for slots 1 and 2 must be set in slot 0, as shown in Table 5-100. Slot 1 is used to transmit the register address, and slot 2 is used to transmit data. For I/O reads to the primary codec, only slot 1 should be valid since only an address is transmitted. For I/O reads only slot 1 valid bit is set, while for I/O writes both slots 1 and 2 valid bits are set.

The secondary codec registers are accessed using slots 1 and 2 as described above, however the slot valid bits for slots 1 and 2 are marked invalid in slot 0 and the codec ID bit 0 (bit 0 of slot 0) is set to 1. This allows the secondary codec to monitor the slot valid bits of slots 1and 2, and bit 0 of slot 0 to determine if the access is directed to the secondary codec. If the register access is targeted to the secondary codec, slot 1 and 2 will contain the address and data for the register access. Since slots 1 and 2 are marked invalid, the primary codec will ignore these accesses.

Table 5-100. Output Tag Slot 0

Bit	Primary Access Example	Secondary Access Example	Description
15	1	1	Frame Valid
14	1	0	Slot 1 Valid, Command Address bit (Primary codec only)
13	1	0	Slot 2 Valid, Command Data bit (Primary codec only)
12:3	X	X	Slot 3–12 Valid
2	0	0	Reserved
1:0	00	01	Codec ID (00 reserved for primary; 01 indicate secondary)

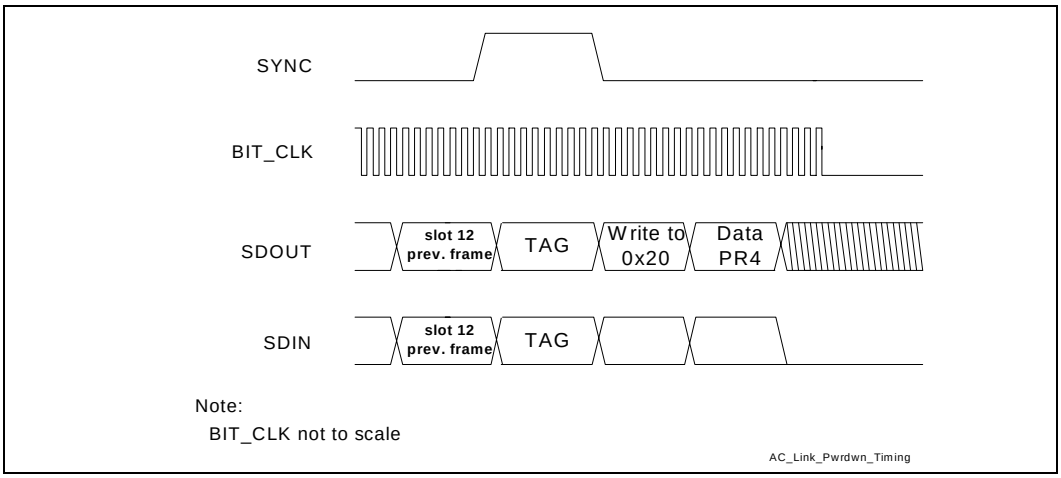
When accessing the codec registers, only one I/O cycle can be pending across the AC-link at any time. The ICH3 implements write posting on I/O writes across the AC-link (i.e., writes across the link are indicated as complete before they are actually sent across the link). In order to prevent a second I/O write from occurring before the first one is complete, software must monitor the CAS bit in the codec access semaphore register which indicates that a codec access is pending. Once the CAS bit is cleared, then another codec access (read or write) can go through. The exception to this being reads to offset 54h/D4h (slot 12) which are returned immediately with the most recently received slot 12 data. Writes to offset 54h and D4h (primary and secondary codecs), get transmitted across the AC-link in slots 1 and 2 as a normal register access. Slot 12 is also updated immediately to reflect the data being written.

The controller will not issue back to back reads. It must get a response to the first read before issuing a second. In addition, codec reads and writes are only executed once across the link, and are not repeated.

5.18.2 AC-Link Low Power Mode

The AC-link signals can be placed in a low-power mode. When the AC ’97 power-down register (26h), is programmed to the appropriate value, both BIT_CLK and SDIN will be brought to, and held at a logic low voltage level.

Figure 5-22. AC-Link Powerdown Timing



BIT_CLK and SDIN transition low immediately following a write to the power-down register (26h) with PR4. When the AC ’97 controller driver is at the point where it is ready to program the AC-link into its low-power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame.

The AC ’97 controller also drives AC_SYNC, and SDOUT low after programming AC ’97 to this low-power, halted mode

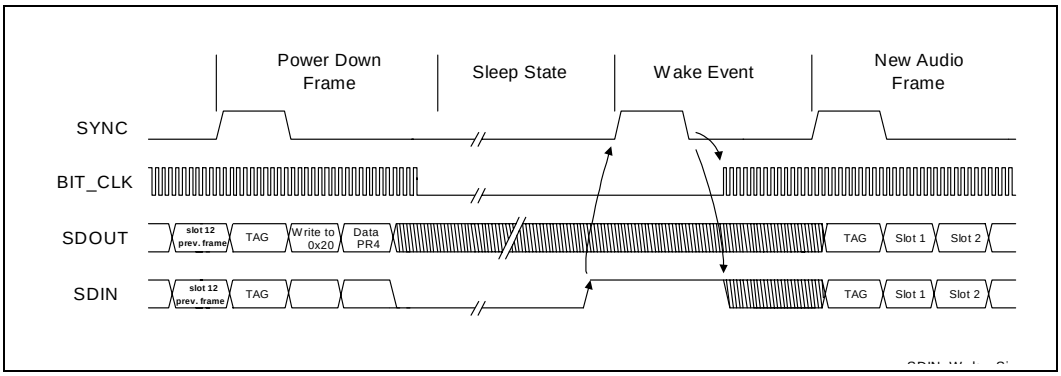
Once the codec has been instructed to halt BIT_CLK, a special wake up protocol must be used to bring the AC-link to the active mode since normal output and input frames can not be communicated in the absence of BIT_CLK. Once in a low-power mode, the ICH3 provides three methods for waking up the AC-link; external wake event, cold reset and warm reset.

Note: Before entering any low-power mode where the link interface to the codec is expected to be powered down while the rest of the system is awake, the software must set the “shut off” bit in the control register.

5.18.2.1 External Wake Event

Codecs can signal the controller to wake the AC-link, and wake the system using SDIN.

Figure 5-23. SDIN Wake Signaling



The minimum SDIN wake up pulse width is 1 µs. The rising edge of SDIN[0] or SDIN[1] causes the ICH3 to sequence through an AC-link warm reset and set the AC97_STS bit in the GPE0_STS Register to wake the system. The primary codec must wait to sample AC_SYNC high and low before restarting BIT_CLK as diagrammed in Figure 5-23. The codec that signaled the wake event must keep its SDIN high until it has sampled AC_SYNC having gone high, and then low.

The AC-link protocol provides for a cold reset and a warm reset. The type of reset used depends on the system's current power down state. Unless a cold or register reset (a write to the reset register in the codec) is performed, wherein the AC '97 codec registers are initialized to their default values, registers are required to keep state during all power down modes.

Once powered down, activation of the AC-link via re-assertion of the AC_SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-link powers up, it indicates readiness via the codec ready bit.

5.18.3 AC '97 Cold Reset

A cold reset is achieved by asserting AC_RST# for 1 µs. By driving AC_RST# low, BIT_CLK, and SDOUT will be activated and all codec registers will be initialized to their default power on reset values. AC_RST# is an asynchronous AC '97 input to the codec.

5.18.4 AC '97 Warm Reset

A warm reset will re-activate the AC-link without altering the current codec register values. A warm reset is signaled by driving AC_SYNC high for a minimum of 1us in the absence of BIT_CLK.

Within normal frames, AC_SYNC is a synchronous AC '97 input to the codec. However, in the absence of BIT_CLK, AC_SYNC is treated as an asynchronous input to the codec used in the generation of a warm reset.

The codec must not respond with the activation of BIT_CLK until AC_SYNC has been sampled low again by the codec. This will prevent the false detection of a new frame.

Note: On receipt of wake up signalling from the codec, the digital controller will issue an interrupt if enabled. Software will then have to issue a warm or cold reset to the codec by setting the appropriate bit in the global control register.

5.18.5 System Reset

Table 5-101 indicates the states of the link during various system reset and sleep conditions.

Table 5-101. AC-Link State during PCIRST#

Signal	Power Plane	I/O	During PCIRST#/	After PCIRST#/	S1	S3	S4/S5
AC_RST#	Resume[3]	Output	Low	Low	Cold Reset bit (Hi)	Low	Low
AC_SDOUT	Core[1]	Output	Low	Running	Low	Low	Low
AC_SYNC	Core	Output	Low	Running	Low	Low	Low
BIT_CLK	Core	Input	Driven by codec	Running	Low[2,4]	Low[2,4]	Low[2,4]
SDIN[1:0]	Resume	Input	Driven by codec	Running	Low[2,4]	Low[2,4]	Low[2,4]

NOTE:
1. ICH3 core well outputs are used as strapping options for the ICH3, sampled during system reset. These signals may have weak pullups/pulldowns on them. The ICH3 outputs will be driven to the appropriate level prior to AC_RST# being deasserted, preventing a codec from entering test mode. Straps are tied to the core well to prevent leakage during a suspend state.
2. The pull-down resistors on these signals are only enabled when the AC-link shut off bit in the AC ’97 global control register is set to 1. All other times, the pull-down resistor is disabled.
3. AC_RST# will be held low during S3–S5. It cannot be programmed high during a suspend state.
4. BIT_CLK and SDIN[1:0] are driven low by the codecs during normal states. If the codec is powered during suspend states it will hold these signals low. However, if the codec is not present, or not powered in suspend, external pull-down resistors are required.

The transition of AC_RST# to the deasserted state will only occur under driver control. In the S1sleep state, the state of the AC_RST# signal is controlled by the AC ’97 Cold Reset# bit (bit 1) in the global control register. AC_RST# will be asserted (low) by the ICH3 under the following conditions:

- RSMRST# (system reset, including the a reset of the resume well and PCIRST#)
- Mechanical power up (causes PCIRST#)
- Write to CF9h hard reset (causes PCIRST#)
- Transition to S3/S4/S5 sleep states (causes PCIRST#)
- Write to AC ’97 Cold Reset# bit in the global control register.

Hardware will never deassert AC_RST# (i.e., never deasserts the Cold Reset# bit) automatically. Only software can deassert the Cold Reset# bit, and hence the AC_RST# signal. This bit, while it resides in the core well, will remain cleared upon return from S3/S4/S5 sleep states. The AC_RST# pin will remain actively driven from the resume well, as indicated.

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Register and Memory Mapping 6

The ICH3 contains registers that are located in the processor's I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes the ICH3 I/O and memory maps at the register-set level. Register access is also described. Register-level address maps and individual register bit descriptions are provided in the following chapters. The following notations and definitions are used in the register/instruction description chapters.

RO	Read Only. In some cases, If a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
WO	Write Only. In some cases, If a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
R/W	Read/Write. A register with this attribute can be read and written.
R/WC	Read/Write Clear. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.
Default	When ICH3 is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the ICH3 registers accordingly.
Bold	In the register bit description tables, register bit names that are highlighted in bold text indicate that the bit is implemented in the ICH3. Register bit names that are not bolded are not implemented or are hardwired.

6.1 PCI Devices and Functions

The ICH3 incorporates a variety of PCI functions as shown in Table 6-1. These functions are divided into four logical devices (B0:D30, B0:D31, B0:D29 and B1:D8). D30 is the hub interface-to-PCI bridge, D31 contains the PCI-to-LPC Bridge, IDE Controller, SMBus Controller and the AC '97 Audio and Modem Controller functions and D29 contains the three USB 1.1 Controllers. B1:D8 is the integrated LAN Controller.

Note: From a software perspective, the integrated LAN Controller resides on the ICH3's external PCI bus (See Section 5.1.2). This is typically Bus 1, but may be assigned a different number depending upon system configuration.

If for some reason, the particular system platform does not want to support any one of Device 31's Functions 1-6, Device 29's functions, or Device 8, they can individually be disabled. The integrated LAN Controller will be disabled if no Platform LAN Connect component is detected (See Section 5.2.2.3). When a function is disabled, it does not appear at all to the software. A disabled function will not respond to any register reads or writes. This is intended to prevent software from thinking that a function is present (and reporting it to the end-user).

Table 6-1. PCI Devices and Functions

Bus:Device:Function	Function Description
Bus 0:Device 30:Function 0	Hub Interface to PCI Bridge
Bus 0:Device 31:Function 0	PCI to LPC Bridge[1]
Bus 0:Device 31:Function 1	IDE Controller
Bus 0:Device 31:Function 3	SMBus Controller
Bus 0:Device 31:Function 5	AC '97 Audio Controller
Bus 0:Device 31:Function 6	AC '97 Modem Controller
Bus 0:Device 29:Function 0	USB UHCI Controller #1
Bus 0:Device 29:Function 1	USB UHCI Controller #2
Bus 0:Device 29:Function 2	New: USB UHCI Controller #3
Bus n:Device 8:Function 0	LAN Controller

NOTES:
1. The PCI to LPC bridge contains registers that control LPC, Power Management, System Management, GPIO, Processor Interface, RTC, Interrupts, Timers, DMA.

Table 6-2 lists the Intel ICH3 Device IDs. Refer to the Specification Update for the Revision IDs.

Table 6-2. Intel® ICH3 Device IDs

Device Function	Description	ICH3 Dev ID	Comments
D30, F0	P2P Bridge	244Eh	
D31, F0	P2L Bridge	2480h	
D31, F1	IDE	248Bh	
D31, F3	SMBus	2483h	
D31, F5	AC97 Audio	2485h	
D31, F6	AC97 Modem	2486h	
D8, F0	LAN	Note 1	
D29, F0	USBC #1	2482h	
D29, F1	USBC #2	2484h	
D29, F2	USBC #3	2487h	

6.2 PCI Configuration Map

Each PCI function on the ICH3 has a set of PCI configuration registers. The register address map tables for these register sets are included at the beginning of the chapter for the particular function. Refer to Table A-1 for a complete list of all PCI Configuration Registers.

Configuration Space registers are accessed through configuration cycles on the PCI bus by the Host bridge using configuration mechanism #1 detailed in the *PCI Local Bus Specification*, Revision 2.2.

Some of the PCI registers contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the configuration space contains reserved locations. Software should not write to reserved PCI configuration locations in the device-specific region (above address offset 3Fh).

6.3 I/O Map

The I/O map is divided into Fixed and Variable address ranges. Fixed ranges cannot be moved, but in some cases can be disabled. Variable ranges can be moved and can also be disabled.

6.3.1 Fixed I/O Address Ranges

Table 6-3 shows the Fixed I/O decode ranges from the processor perspective. Note that for each I/O range, there may be separate behavior for reads and writes. The hub interface cycles that go to target ranges that are marked as "Reserved" will not be decoded by the ICH3, and will be passed to PCI. If a PCI master targets one of the fixed I/O target ranges, it will be positively decoded by the ICH3 in medium speed.

Refer to Table A-2 for a complete list of all fixed I/O registers.

Address ranges that are not listed or marked "Reserved" are **not** decoded by the ICH3 (unless assigned to one of the variable ranges).

Table 6-3. Fixed I/O Ranges Decoded by Intel® ICH3

I/O Address	Read Target	Write Target	Internal Unit
00h–08h	DMA Controller	DMA Controller	DMA
09h–0Eh	RESERVED	DMA Controller	DMA
0Fh	DMA Controller	DMA Controller	DMA
10h–18h	DMA Controller	DMA Controller	DMA
19h–1Eh	RESERVED	DMA Controller	DMA
1Fh	DMA Controller	DMA Controller	DMA
20h–21h	Interrupt Controller	Interrupt Controller	Interrupt
24h–25h	Interrupt Controller	Interrupt Controller	Interrupt
28h–29h	Interrupt Controller	Interrupt Controller	Interrupt
2Ch–2Dh	Interrupt Controller	Interrupt Controller	Interrupt
2E–2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h–31h	Interrupt Controller	Interrupt Controller	Interrupt
34h–35h	Interrupt Controller	Interrupt Controller	Interrupt
38h–39h	Interrupt Controller	Interrupt Controller	Interrupt
3Ch–3Dh	Interrupt Controller	Interrupt Controller	Interrupt
40h–42h	Timer/Counter	Timer/Counter	PIT (8254)
43h	RESERVED	Timer/Counter	PIT
4E–4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h–52h	Timer/Counter	Timer/Counter	PIT
53h	RESERVED	Timer/Counter	PIT
60h	Microcontroller	Microcontroller	Forwarded to LPC
61h	NMI Controller	NMI Controller	Processor I/F
62h	Microcontroller	Microcontroller	Forwarded to LPC
63h	NMI Controller	NMI Controller	Processor I/F
64h	Microcontroller	Microcontroller	Forwarded to LPC
65h	NMI Controller	NMI Controller	Processor I/F
66h	Microcontroller	Microcontroller	Forwarded to LPC
67h	NMI Controller	NMI Controller	Processor I/F

Table 6-3. Fixed I/O Ranges Decoded by Intel® ICH3 (Continued)

I/O Address	Read Target	Write Target	Internal Unit
70h	RESERVED	NMI and RTC Controller	RTC
71h	RTC Controller	RTC Controller	RTC
72h	RTC Controller	NMI and RTC Controller	RTC
73h	RTC Controller	RTC Controller	RTC
74h	RTC Controller	NMI and RTC Controller	RTC
75h	RTC Controller	RTC Controller	RTC
76h	RTC Controller	NMI and RTC Controller	RTC
77h	RTC Controller	RTC Controller	RTC
80h	DMA Controller	DMA Controller and LPC or PCI	DMA
81h–83h	DMA Controller	DMA Controller	DMA
84h–86h	DMA Controller	DMA Controller and LPC or PCI	DMA
87h	DMA Controller	DMA Controller	DMA
88h	DMA Controller	DMA Controller and LPC or PCI	DMA
89h–8Bh	DMA Controller	DMA Controller	DMA
8Ch–8Eh	DMA Controller	DMA Controller and LPC or PCI	DMA
08Fh	DMA Controller	DMA Controller	DMA
90h–91h	DMA Controller	DMA Controller	DMA
92h	Reset Generator	Reset Generator	Processor I/F
93h–9Fh	DMA Controller	DMA Controller	DMA
A0h–A1h	Interrupt Controller	Interrupt Controller	Interrupt
A4h–A5h	Interrupt Controller	Interrupt Controller	Interrupt
A8h–A9h	Interrupt Controller	Interrupt Controller	Interrupt
ACh–ADh	Interrupt Controller	Interrupt Controller	Interrupt
B0h–B1h	Interrupt Controller	Interrupt Controller	Interrupt
B2h–B3h	Power Management	Power Management	Power Management
B4h–B5h	Interrupt Controller	Interrupt Controller	Interrupt
B8h–B9h	Interrupt Controller	Interrupt Controller	Interrupt
BCh–BDh	Interrupt Controller	Interrupt Controller	Interrupt
C0h–D1h	DMA Controller	DMA Controller	DMA
D2h–DDh	RESERVED	DMA Controller	DMA
DEh–DFh	DMA Controller	DMA Controller	DMA
F0h	See Note 3	FERR#/IGNNE# / Interrupt Controller	Processor I/F
170h–177h	IDE Controller[2]	IDE Controller[2]	Forwarded to IDE
1F0h–1F7h	IDE Controller[1]	IDE Controller[1]	Forwarded to IDE
376h	IDE Controller[2]	IDE Controller[2]	Forwarded to IDE
3F6h	IDE Controller[1]	IDE Controller[1]	Forwarded IDE
4D0h–4D1h	Interrupt Controller	Interrupt Controller	Interrupt
CF9h	Reset Generator	Reset Generator	Processor I/F

NOTES:
1. Only if IDE Standard I/O space is enabled for Primary Channel and the IDE Controller is in legacy mode. Otherwise, the target is PCI.
2. Only if IDE Standard I/O space is enabled for Secondary Channel and the IDE Controller is in legacy mode. Otherwise, the target is PCI.
3. If POS_DEC_EN bit is enabled, reads from F0h will not be decoded by the ICH3. If POS_DEC_EN is not enabled, reads from F0h will forward to LPC.

6.3.2 Variable I/O Decode Ranges

Table 6-4 shows the Variable I/O Decode Ranges. They are set using Base Address Registers (BARs) or other configuration bits in the various PCI configuration spaces. The PNP software (PCI or ACPI) can use their configuration mechanisms to set and adjust these values.

When a cycle is detected on the hub interface, the ICH3 positively decodes the cycle. If the response is on the behalf of an LPC device, the ICH3 forwards the cycle to the LPC I/F.

Refer to Table A-3 for a complete list of all variable I/O registers.

Warning: The Variable I/O Ranges should not be set to conflict with the Fixed I/O Ranges. Unpredictable results if the configuration software allows conflicts to occur. The ICH3 does not perform any checks for conflicts.

Table 6-4. Variable I/O Decode Ranges

Range Name	Mappable	Size (Bytes)	Target
ACPI	Anywhere in 64 KB I/O Space	64	Power Management
IDE Bus Master	Anywhere in 64 KB I/O Space	16	IDE Unit
USB 1.1 Controller #1	Anywhere in 64 KB I/O Space	32	USB Unit 1
SMBus	Anywhere in 64 KB I/O Space	32	SMB Unit
AC ’97 Audio Mixer	Anywhere in 64 KB I/O Space	256	AC ’97 Unit
AC ’97 Bus Master	Anywhere in 64 KB I/O Space	64	AC ’97 Unit
AC ’97 Modem Mixer	Anywhere in 64 KB I/O Space	256	AC ’97 Unit
TCO	96 Bytes above ACPI Base	32	TCO Unit
GPIO	Anywhere in 64 KB I/O Space	64	GPIO Unit
Parallel Port	3 ranges in 64 KB I/O Space	8	LPC Peripheral
Serial Port 1	8 Ranges in 64 KB I/O Space	8	LPC Peripheral
Serial Port 2	8 Ranges in 64 KB I/O Space	8	LPC Peripheral
Floppy Disk Controller	2 Ranges in 64 KB I/O Space	8	LPC Peripheral
MIDI	4 Ranges in 64 KB I/O Space	2	LPC Peripheral
MSS	4 Ranges in 64 KB I/O Space	8	LPC Peripheral
SoundBlaster	2 Ranges in 64 KB I/O Space	32	LPC Peripheral
LAN	Anywhere in 64 KB I/O Space	64	LAN Unit
USB 1.1 Controller #2	Anywhere in 64 KB I/O Space	32	USB Unit 2
USB 1.1 Controller #3	Anywhere in 64 KB I/O Space	32	USB Unit 3
LPC Generic 1	Anywhere in 64 KB I/O Space	128	LPC Peripheral
LPC Generic 2	Anywhere in 64 KB I/O Space	16	LPC Peripheral
Monitors 4:7	Anywhere in 64 KB I/O Space	16	LPC Peripheral or Trap on PCI
Native IDE Primary Command	Anywhere in 64 KB I/O Space	8	IDE Unit
Native IDE Primary Control	Anywhere in 64 KB I/O Space	4	IDE Unit
Native IDE Secondary Command	Anywhere in 64 KB I/O Space	8	IDE Unit
Native IDE Secondary Control	Anywhere in 64 KB I/O Space	4	IDE Unit

6.4 Memory Map

Table 6-5 shows (from the processor perspective) the memory ranges that the ICH3 will decode. Cycles that arrive from the Hub Interface that are not directed to any of the internal memory targets that decode directly from Hub Interface will be driven out on PCI. The ICH3 may then claim the cycle for it to be forwarded to LPC or claimed by the internal APIC. If subtractive decode is enabled, the cycle can be forwarded to LPC.

PCI cycles generated by an external PCI master will be positively decoded unless it falls in the PCI-PCI bridge forwarding range (those addresses are reserved for PCI peer-to-peer traffic). If the cycle is not in the I/O APIC or LPC ranges, it will be forwarded up the hub interface to the Host Controller. PCI masters can not access the memory ranges for functions that decode directly from Hub Interface

Table 6-5. Memory Decode Ranges from Processor Perspective

Memory Range	Target	Dependency/Comments
0000 0000–000D FFFFh 0010 0000–TOM (Top of Memory)	Main Memory	TOM registers in Host Controller
000E 0000–000F FFFFh	FWH	Bit 7 in FWH Decode Enable Register is set
FEC0 0000–FEC0 0100h	I/O APIC inside ICH3	
FFC0 0000–FFC7 FFFFh FF80 0000–FF87 FFFFh	FWH	Bit 0 in FWH Decode Enable Register
FFC8 0000–FFCF FFFFh FF88 0000–FF8F FFFFh	FWH	Bit 1 in FWH Decode Enable Register
FFD0 0000–FFD7 FFFFh FF90 0000—FF97 FFFFh	FWH	Bit 2 in FWH Decode Enable Register is set
FFD8 0000–FFDF FFFFh FF98 0000—FF9F FFFFh	FWH	Bit 3 in FWH Decode Enable Register is set
FFE0 000–FFE7 FFFFh FFA0 0000–FFA7 FFFFh	FWH	Bit 4 in FWH Decode Enable Register is set
FFE8 0000–FFEF FFFFh FFA8 0000–FFAF FFFFh	FWH	Bit 5 in FWH Decode Enable Register is set
FFF0 0000–FFF7 FFFFh FFB0 0000–FFB7 FFFFh	FWH	Bit 6 in FWH Decode Enable Register is set.
FFF8 0000–FFFF FFFFh FFB8 0000–FFBF FFFFh	FWH	Always enabled. The top two 64K-byte blocks of this range can be swapped, as described in Section 6.4.1.
FF70 0000–FF7F FFFFh FF30 0000–FF3F FFFFh	FWH	Bit 3 in FWH Decode Enable 2 Register is set
FF60 0000–FF6F FFFFh FF20 0000–FF2F FFFFh	FWH	Bit 2 in FWH Decode Enable 2 Register is set
FF50 0000–FF5F FFFFh FF10 0000–FF1F FFFFh	FWH	Bit 1 in FWH Decode Enable 2 Register is set
FF40 0000–FF4F FFFFh FF00 0000–FF0F FFFFh	FWH	Bit 0 in FWH Decode Enable 2 Register is set

Table 6-5. Memory Decode Ranges from Processor Perspective (Continued)

Memory Range	Target	Dependency/Comments
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable via BAR in Device 29:Function 0 (Integrated LAN Controller)
1 KB anywhere in 4 GB range	IDE Expansion[2]	Enable via standard PCI mechanism and bits in IDE I/O Configuration Register (Device 31, Function 1)
All other	PCI	None

NOTES:
1. These ranges are decoded directly from Hub Interface. The memory cycles will not be seen on PCI.
2. Software must not attempt locks to memory mapped I/O ranges for IDE Expansion. If attempted, the lock is not honored, which means potential deadlock conditions may occur.

6.4.1 Boot-Block Update Scheme

The ICH3 supports a “top-block swap” mode that has the ICH3 swap the top block in the FWH (the boot block) with another location. This allows for safe update of the Boot Block (even if a power failure occurs). When the “top-swap” enable bit is set, the ICH3 will invert A16 for cycles targeting FWH BIOS space. When this bit is 0, the ICH3 will not invert A16. This bit is automatically set to 0 by RTCRST#, but not by PCIRST#.

The scheme is based on the concept that the top block is reserved as the “boot” block, and the block immediately below the top block is reserved for doing boot-block updates.

The algorithm is:

1. Software copies the top block to the block immediately below the top.
2. Software checks that the copied block is correct. This could be done by performing a checksum calculation.
3. Software sets the “top-block swap” bit. This will invert A16 for cycles going to the FWH. Processor access to FFFF_0000 through FFFF_FFFF will be directed to FFFE_0000 through FFFE_FFFF in the FWH, and processor accesses to FFFE_0000 through FFFE_FFFF will be directed to FFFF_0000 through FFFF_FFFF.
4. Software erases the top block.
5. Software writes the new top block.
6. Software checks the new top block.
7. Software clears the top-block swap bit.

If a power failure occurs at any point after step 3, the system will be able to boot from the copy of the boot block that is stored in the block below the top. This is because the top-swap bit is backed in the RTC well.

Note: The top-block swap mode may be forced by an external strapping option (See Section 2.20.1). When top-block swap mode is forced in this manner, the top-swap bit cannot be cleared by software. A re-boot with the strap removed will be required to exit a forced top-block swap mode.

Note: The top-block swap mode only affects accesses to the FWH BIOS space, not feature space.

Note: The top-block swap mode has no effect on accesses below FFFE_0000h.

LAN Controller Registers (B1:D8:F0) 7

The ICH3 integrated LAN Controller appears to reside at PCI Device 8, Function 0 on the secondary side of the ICH3's virtual PCI-to-PCI Bridge (See Section 5.1.2). This is typically Bus 1, but may be assigned a different number depending upon system configuration. The LAN Controller acts as both a master and a slave on the PCI bus. As a master, the LAN Controller interacts with the system main memory to access data for transmission or deposit received data. As a slave, some of the LAN Controller's control structures are accessed by the host processor to read or write information to the on-chip registers. The processor also provides the LAN Controller with the necessary commands and pointers that allow it to process receive and transmit data.

7.1 PCI Configuration Registers (B1:D8:F0)

Note: Registers that are not shown should be treated as Reserved (See Section 6.2 for details).

Table 7-1. PCI Configuration Map (LAN Controller—B1:D8:F0)

Offset	Mnemonic	Register Name/Function	Default	Type
00–01h	VID	Vendor ID	8086h	RO
02–03h	DID	Device ID	2449h	RO
04–05h	PCICMD	PCI Device Command	0000h	R/W
06–07h	PCISTS	PCI Device Status	0290h	R/W
08h	REVID	Revision ID	See Note	RO
0Ah	SCC	Sub Class Code	00h	RO
0Bh	BCC	Base Class Code	02h	RO
0Dh	PMLT	PCI Master Latency Timer	00h	R/W
0Eh	HEADTYP	Header Type	00h	RO
10–13h	CSR_MEM_BASE	CSR Memory-Mapped Base Address	0008h	R/W
14–17h	CSR_IO_BASE	CSR I/O-Mapped Base Address	0001h	R/W
2C–2Dh	SVID	Subsystem Vendor ID	0000h	RO
2E–2Fh	SID	Subsystem ID	0000h	RO
34h	CAP_PTR	Capabilities Pointer	DCh	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	01h	RO
3Eh	MIN_GNT	Minimum Grant	08h	RO
3Fh	MAX_LAT	Maximum Latency	38h	RO
DCh	CAP_ID	Capability ID	01h	RO
DDh	NXT_PTR	Next Item Pointer	00h	RO
DE–DFh	PM_CAP	Power Management Capabilities	FE21h	RO
E0–E1h	PMCSR	Power Management Control/Status	0000h	R/W
E3h	PCIDATA	PCI Power Management Data	00h	RO

NOTE: Refer to the Specification Update for the Revision ID.

7.1.1 VID—Vendor ID Register (LAN Controller—B1:D8:F0)

Offset Address: 00–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Vendor Identification Value.** This is a 16-bit value assigned to Intel.

7.1.2 DID—Device ID Register (LAN Controller—B1:D8:F0)

Offset Address: 02–03h Attribute: RO
Default Value: 2449h Size: 16 bits

Bit	Description
15:0	Device Identification Value. This is a 16-bit value assigned to the ICH3 integrated LAN Controller. 1. If the EEPROM is not present (or not properly programmed), reads to the Device ID return the default value of 2449h. 2. If the EEPROM is present (or properly programmed) and if the value of Word 23h is not 0000f or FFFFh, the Device ID is loaded from the EEPROM, Word 23h after the hardware reset. (See Section 7.1.14–SID, Subsystem ID of LAN controller for detail).

7.1.3 PCICMD—PCI Command Register (LAN Controller—B1:D8:F0)

Offset Address: 04–05h Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:10	Reserved.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0. The integrated LAN Controller will not run fast back-to-back PCI cycles.
8	**SERR# Enable (SERR_EN)**—R/W. 0 = Disable. 1 = Enable. Allow SERR# to be asserted.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0. Not implemented.
6	**Parity Error Response (PER)**—R/W. 0 = The LAN Controller will ignore PCI parity errors. 1 = The integrated LAN Controller will take normal action when a PCI parity error is detected and will enable generation of parity on the hub interface.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0'. Not Implemented.
4	**Memory Write and Invalidate Enable (MWIE)**—R/W. 0 = Disable. The LAN Controller will not use the Memory Write and Invalidate command. 1 = Enable.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0. The LAN Controller ignores special cycles.
2	**Bus Master Enable (BME)**—R/W. 0 = Disable. 1 = Enable. The ICH3's integrated may function as a PCI bus master.
1	**Memory Space Enable (MSE)**—R/W. 0 = Disable. 1 = Enable. The ICH3's integrated LAN Controller will respond to the memory space accesses.
0	**I/O Space Enable (IOE)**—R/W. 0 = Disable. 1 = Enable. The ICH3's integrated LAN Controller will respond to the I/O space accesses.

7.1.4 PCISTS—PCI Status Register (LAN Controller—B1:D8:F0)

Offset Address: 06–07h
Default Value: 0290h
Attribute: RO, R/WC
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = This bit is cleared by writing a 1 to the bit location. 1 = The ICH3's integrated LAN Controller has detected a parity error on the PCI bus (will be set even if Parity Error Response is disabled in the PCI Command register).
14	**Signaled System Error (SSE)**—R/WC. 0 = This bit is cleared by writing a 1 to the bit location. 1 = The ICH3's integrated LAN Controller has asserted SERR#. (SERR# can be routed to cause NMI, SMI# or interrupt.
13	**Master Abort Status (MAS)**—R/C. 0 = This bit is cleared by writing a 1 to the bit location. 1 = The ICH3's integrated LAN Controller (as a PCI master) has generated a master abort.
12	**Received Target Abort (RTA)**—R/WC. 0 = This bit is cleared by writing a 1 to the bit location. 1 = The ICH3's integrated LAN Controller (as a PCI master) has received a target abort.
11	Signaled Target Abort (STA)—RO. Hardwired to 0. The device will never signal Target Abort.
10:9	DEVSEL# Timing Status (DEV_STS)—RO. 01h = Medium timing.
8	**Data Parity Error Detected (DPED)**—R/WC. 0 = This bit is cleared by writing a 1 to the bit location. 1 = All of the following three conditions have been met: 1. The LAN Controller is acting as bus master. 2. The LAN Controller has asserted PERR# (for reads) or detected PERR# asserted (for writes). 3. The Parity Error Response bit in the LAN Controller's PCI Command Register is set.
7	Fast Back to Back (FB2B)—RO. Hardwired to 1. The device can accept fast back-to-back transactions.
6	User Definable Features (UDF)—RO. Hardwired to 0. Not implemented.
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0. The device does not support 66 MHz PCI.
4	**Capabilities List (CAP_LIST)**—RO. 0 = The EEPROM indicates that the integrated LAN controller does not support PCI Power Management. 1 = The EEPROM indicates that the integrated LAN controller supports PCI Power Management.
3:0	Reserved.

7.1.5 REVID—Revision ID Register (LAN Controller—B1:D8:F0)

Offset Address: 08h
Default Value: See Note 1
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision Identification Value.** 8-bit value that indicates the revision number for the integrated LAN Controller. The three least significant bits in this register may be overridden by the ID and REV ID fields in the EEPROM.

NOTE 1: Refer to the Specification Update for the Revision ID.

7.1.6 SCC—Sub Class Code Register (LAN Controller—B1:D8:F0)

Offset Address: 0Ah Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Sub Class Code.** 8-bit value that specifies the sub-class of the device as an Ethernet controller.

7.1.7 BCC—Base Class Code Register (LAN Controller—B1:D8:F0)

Offset Address: 0Bh Attribute: RO
Default Value: 02h Size: 8 bits

Bit	Description
7:0	**Base Class Code.** 8-bit value that specifies the base class of the device as a network controller.

7.1.8 CLS—Cache Line Size Register (LAN Controller—B1:D8:F0)

Offset Address: 0Ch Attribute: RW
Default Value: 00h Size: 8 bits

Bit	Description
7:5	Reserved.
4:3	**Cache Line Size (CLS)**—RW. 00 = Memory Write and Invalidate (MWI) command will not be used by the integrated LAN Controller. 01 = MWI command will be used with Cache Line Size set to 8 DWords (only set if a value of 08h is written to this register). 10 = MWI command will be used with Cache Line Size set to 16 DWords (only set if a value of 10h is written to this register). 11 = Invalid. MWI command will not be used.
2:0	Reserved.

7.1.9 PMLT—PCI Master Latency Timer Register (LAN Controller—B1:D8:F0)

Offset Address: 0Dh Attribute: RW
Default Value: 00h Size: 8 bits

Bit	Description
7:3	**Master Latency Timer Count (MLTC)**—RW. Defines the number of PCI clock cycles that the integrated LAN Controller may own the bus while acting as bus master.
2:0	Reserved.

7.1.10 HEADTYP—Header Type Register (LAN Controller—B1:D8:F0)

Offset Address: 0Eh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7	**Multi-Function Device**—RO. Hardwired to 0 to indicate a single function device.
6:0	**Header Type**—RO. 7-bit field identifies the header layout of the configuration space as an Ethernet controller.

7.1.11 CSR_MEM_BASE CSR—Memory-Mapped Base Address Register (LAN Controller—B1:D8:F0)

Offset Address: 10–13h Attribute: R/W, RO
Default Value: 0000 0008h Size: 32 bits

Note: The ICH3's integrated LAN Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the Lan Controller's CSR registers.

Bit	Description
31:12	**Base Address**—R/W. Upper 20 bits of the base address provides 4 KB of memory-Mapped space for the LAN Controller's Control/Status Registers.
11:4	Reserved.
3	Prefetchable—RO. Hardwired to 0 to indicate that this is not a pre-fetchable memory-Mapped address range.
2:1	Type—RO. Hardwired to 00b to indicate the memory-Mapped address range may be located anywhere in 32-bit address space.
0	Memory Space Indicator—RO. Hardwired to 0 to indicate that this base address maps to memory space.

7.1.12 CSR_IO_BASE—CSR I/O-Mapped Base Address Register (LAN Controller—B1:D8:F0)

Offset Address: 14–17h Attribute: R/W
Default Value: 0000 0001h Size: 32 bits

Note: The ICH3's integrated LAN Controller requires one BAR for memory mapping. Software determines which BAR (memory or I/O) is used to access the Lan Controller's CSR registers.

Bit	Description
31:16	Reserved.
15:6	**Base Address**—R/W. Provides 64 bytes of I/O-Mapped address space for the LAN Controller's Control/Status Registers.
5:1	Reserved.
0	I/O Space Indicator—RO. Hardwired to 1 to indicate that this base address maps to I/O space.

7.1.13 SVID—Subsystem Vendor ID Register (LAN Controller—B1:D8:F0)

Offset Address: 2C–2D Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:0	Subsystem Vendor ID—RO.(see Section 7.1.14 for detail).

7.1.14 SID—Subsystem ID Register (LAN Controller—B1:D8:F0)

Offset Address: 2E–2Fh Attribute: RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:0	Subsystem ID—RO.

Note: The ICH3's integrated LAN Controller provides support for configurable Subsystem ID and Subsystem Vendor ID fields. After reset, the LAN Controller automatically reads addresses Ah through Ch, and 23h of the EEPROM. The LAN Controller checks bits 15:13 in the EEPROM word Ah, and functions according to Table 7-2.

Table 7-2. Configuration of Subsystem ID and Subsystem Vendor ID via EEPROM

Bits 15:14	Bit 13	Device ID	Vendor ID	Revision ID	Subsystem ID	Subsystem Vendor ID
11b, 10b, 00b	X	2449h	8086h	See Note 1	0000h	0000h
01b	0b	Word 23h	8086h	See Note 1	Word Bh	Word Ch
01b	1b	Word 23h	Word Ch	See Note 1	Word Bh	Word Ch

NOTE:
1. Refer to the Specification Update for the Revision ID, which is subject to change according to the silicon stepping.
2. The Device ID is loaded from Word 23h only if the value of Word 23h is not 0000h or FFFFh

7.1.15 CAP_PTR—Capabilities Pointer Register (LAN Controller—B1:D8:F0)

Offset Address: 34h Attribute: RO
Default Value: DCh Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)**—RO. Hardwired to DCh to indicate the offset within configuration space for the location of the Power Management registers.

7.1.16 INT_LN—Interrupt Line Register (LAN Controller—B1:D8:F0)

Offset Address: 3Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)**—R/W. Identifies the system interrupt line to which the LAN Controller's PCI interrupt request pin (as defined in the Interrupt Pin Register) is routed.

7.1.17 INT_PN—Interrupt Pin Register (LAN Controller—B1:D8:F0)

Offset Address: 3Dh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)**—RO. Hardwired to 01h to indicate that the LAN Controller's interrupt request is connected to PIRQA#. However, in the ICH3 implementation, when the LAN Controller interrupt is generated PIRQ[E]# will go active, not PIRQ[A]#. Note that if the PIRQ[E]# signal is used as a GPIO, the external visibility will be lost (though PIRQ[E]# will still go active internally).

7.1.18 MIN_GNT—Minimum Grant Register (LAN Controller—B1:D8:F0)

Offset Address: 3Eh
Default Value: 08h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Minimum Grant (MIN_GNT)—RO. Indicates the amount of time (in increments of 0.25µs) that the LAN Controller needs to retain ownership of the PCI bus when it initiates a transaction.

7.1.19 MAX_LAT—Maximum Latency Register (LAN Controller—B1:D8:F0)

Offset Address: 3Fh
Default Value: 38h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Maximum Latency (MAX_LAT)—RO. Defines how often (in increments of 0.25µs) the LAN Controller needs to access the PCI bus.

7.1.20 CAP_ID—Capability ID Register (LAN Controller—B1:D8:F0)

Offset Address: DCh Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Capability ID (CAP_ID)**—RO. Hardwired to 01h to indicate that the ICH3's integrated LAN Controller supports PCI Power Management.

7.1.21 NXT_PTR—Next Item Pointer Register (LAN Controller—B1:D8:F0)

Offset Address: DDh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Next Item Pointer (NXT_PTR)**—RW. Hardwired to 00b to indicate that power management is the last item in the Capabilities list.

7.1.22 PM_CAP—Power Management Capabilities Register (LAN Controller—B1:D8:F0)

Offset Address: DE–DFh Attribute: RO
Default Value: FE21h Size: 16 bits

Bit	Description
15:11	**PME Support.** Hardwired to 11111b. This 5-bit field indicates the power states in which the LAN Controller may assert PME#. The LAN Controller supports wake-up in all power states.
10	**D2 Support.** Hardwired to 1 to indicate that the LAN Controller supports the D2 power state.
9	**D1 Support.** Hardwired to 1 to indicate that the LAN Controller supports the D1 power state.
8:6	**Auxiliary Current.** Hardwired to 000b to indicate that the LAN Controller implements the Data registers. The auxiliary power consumption is the same as the current consumption reported in the D3 state in the Data register.
5	**Device Specific Initialization (DSI).** Hardwired to 1 to indicate that special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. DSI is required for the LAN Controller after D3-to-D0 reset.
4	Reserved.
3	**PME Clock.** Hardwired to 0 to indicate that the LAN Controller does not require a clock to generate a power management event.
2:0	**Version.** Hardwired to 010b to indicate that the LAN Controller complies with of the PCI Power Management Specification, Revision 1.1.

7.1.23 PMCSR—Power Management Control/Status Register (LAN Controller—B1:D8:F0)

Offset Address:	E0–E1h	Attribute:	RO, R/W, R/WC
Default Value:	0000h	Size:	16 bits

Bit	Description
15	**PME Status**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. This also de-asserts the PME# signal and clears the PME status bit in the Power Management Driver Register. When the PME# signal is enabled, the PME# signal reflects the state of the PME status bit. 1 = Set upon occurrence of a wake-up event, independent of the state of the PME enable bit.
14:13	**Data Scale**—RO. This field indicates the data register scaling factor. It equals 10b for registers zero through eight and 00b for registers nine through fifteen, as selected by the “Data Select” field.
12:9	**Data Select**—R/W. This field is used to select which data is reported through the Data register and Data Scale field.
8	**PME Enable**—R/W. This bit enables the ICH3’s integrated LAN controller to assert PME#. 0 = The device will not assert PME#. 1 = Enable PME# assertion when PME Status is set.
7:5	Reserved.
4	**Dynamic Data**—RO. Hardwired to 0 to indicate that the device does not support the ability to monitor the power consumption dynamically.
3:2	Reserved.
1:0	**Power State**—R/W. This 2-bit field is used to determine the current power state of the integrated LAN Controller, and to put it into a new power state. The definition of the field values is as follows: 00 = D0 01 = D1 10 = D2 11 = D3

7.1.24 PCIDATA—PCI Power Management Data Register (LAN Controller—B1:D8:F0)

Offset Address:	E3h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	State dependent power consumption and heat dissipation data.

Note: The data register is an 8-bit read only register that provides a mechanism for the ICH3's integrated LAN Controller to report state dependent maximum power consumption and heat dissipation. The value reported in this register depends on the value written to the Data Select field in the PMCSR register. The power measurements defined in this register have a dynamic range of 0 to 2.55 W with 0.01 W resolution, scaled according to the Data Scale field in the PMCSR. The structure of the Data Register is given in Table 7-3 below.

Table 7-3. Data Register Structure

Data Select	Data Scale	Data Reported
0	2	D0 Power Consumption
1	2	D1 Power Consumption
2	2	D2 Power Consumption
3	2	D3 Power Consumption
4	2	D0 Power Dissipated
5	2	D1 Power Dissipated
6	2	D2 Power Dissipated
7	2	D3 Power Dissipated
8	2	Common Function Power Dissipated
9–15	0	Reserved

7.2 LAN Control / Status Registers (CSR)

Table 7-4. Intel® ICH3 Integrated LAN Controller CSR Space

Offset	Register Name/Function	Default	Type
01h–00h	SCB Status Word	0000h	R/WC
03h–02h	SCB Command Word	0000h	R/W
07h–04h	SCB General Pointer	0000 0000h	R/W
0Bh–08h	PORT	0000 0000h	R/W (special)
0Dh–0Ch	Reserved		
0Eh	EEPROM Control Register	00	R/W
0Fh	Reserved		
13h–10h	MDI Control Register	0000 0000h	R/W (special)
17h–14h	Receive DMA Byte Count	0000 0000h	RO
18h	Early Receive Interrupt	00h	R/W
1A–19h	Flow Control Register	0000h	R/W
1Bh	PMDR	00h	R/WC
1Ch	General Control	00	R/W
1Dh	General Status	N/A	RO
1Eh–3Ch	Reserved		

7.2.1 System Control Block Status Word Register

Offset Address: 00–01h
Default Value: 0000h
Attribute: R/WC, RO
Size: 16 bits

The ICH3's integrated LAN Controller places the status of its Command and Receive units and interrupt indications in this register for the processor to read.

Bit	Description
15	**Command Unit (CU) Executed (CX)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = Interrupt signaled because the CU has completed executing a command with its interrupt bit set.
14	**Frame Received (FR)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = Interrupt signaled because the Receive Unit (RU) has finished receiving a frame.
13	**CU Not Active (CNA)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = The Command Unit left the Active state or entered the Idle state. There are 2 distinct states of the CU. When configured to generate CNA interrupt, the interrupt will be activated when the CU leaves the Active state and enters either the Idle or the Suspended state. When configured to generate CI interrupt, an interrupt will be generated only when the CU enters the Idle state.
12	**Receive Not Ready (RNR)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = Interrupt signaled because the Receive Unit left the Ready state. This may be caused by an RU Abort command, a no resources situation, or set suspend bit due to a filled Receive Frame Descriptor.
11	**Management Data Interrupt (MDI)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = Set when a Management Data Interface read or write cycle has completed. The management data interrupt is enabled through the interrupt enable bit (bit 29 in the management data interface control register in the CSR).
10	**Software Interrupt (SWI)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = Set when software generates an interrupt.
9	**Early Receive (ER)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = Indicates the occurrence of an Early Receive Interrupt.
8	**Flow Control Pause (FCP)**—R/WC. 0 = Software acknowledges the interrupt and clears this bit by writing a 1 to the bit position. 1 = Indicates Flow Control Pause interrupt.
7:6	**Command Unit Status (CUS)**—RO. 00 = Idle 01 = Suspended 10 = LPQ (Low Priority Queue) active 11 = HPQ (High Priority Queue) active
5:2	**Receive Unit Status (RUS)**—RO. 0000 = Idle 0001 = Suspended 0010 = No Resources 0011 = Reserved 0100 = Ready 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Reserved 1001 = Suspended with no more RBDs 1010 = No resources due to no more RBDs 1011 = Reserved 1100 = Ready with no RBDs present 1101 = Reserved 1110 = Reserved 1111 = Reserved
1:0	Reserved.

7.2.2 System Control Block Command Word Register

Offset Address:	02–03h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

The processor places commands for the Command and Receive units in this register. Interrupts are also acknowledged in this register.

Bit	Description
15	**CX Mask** —R/W. 0 = Interrupt not masked. 1 = Disable the generation of a CX interrupt.
14	**FR Mask** —R/W. 0 = Interrupt not masked. 1 = Disable the generation of an FR interrupt.
13	**CNA Mask** —R/W. 0 = Interrupt not masked. 1 = Disable the generation of a CNA interrupt.
12	**RNR Mask** —R/W. 0 = Interrupt not masked. 1 = Disable the generation of an RNR interrupt.
11	**ER Mask** —R/W. 0 = Interrupt not masked. 1 = Disable the generation of an ER interrupt.
10	**FCP Mask** —R/W. 0 = Interrupt not masked. 1 = Disable the generation of an FCP interrupt.
9	**Software Generated Interrupt (SI)**—WO. 0 = No Effect. 1 = Setting this bit causes the LAN Controller to generate an interrupt.
8	**Interrupt Mask (M)**—R/W. This bit enables or disables the LAN Controllers assertion of the INTA# signal. This bit has higher precedence that the specific interrupt mask bits and the SI bit. 0 = Enable the assertion of INTA#. 1 = Disable the assertion of INTA#.

Bit	Description
7:4	**Command Unit Command (CUC)**—R/W. Valid values are listed below. All other values are Reserved. 0000 = **NOP:** Does not affect the current state of the unit. 0001 = **CU Start**: Start execution of the first command on the CBL. A pointer to the first CB of the CBL should be placed in the SCB General Pointer before issuing this command. The CU Start command should only be issued when the CU is in the Idle or Suspended states (never when the CU is in the active state), and all of the previously issued Command Blocks have been processed and completed by the CU. Sometimes it is only possible to determine that all Command Blocks are completed by checking that the complete bit is set in all previously issued Command Blocks. 0010 = **CU Resume:** Resume operation of the Command unit by executing the next command. This command will be ignored if the CU is idle. 0011 = **CU HPQ Start:** Start execution of the first command on the high priority CBL. A pointer to the first CB of the HPQ CBL should be placed in the SCB General POinter before issuing this command. 0100 = **Load Dump Counters Address:** Tells the device where to write dump data when using the Dump Statistical Counters or Dump and Reset Statistical Counters commands. This command must be executed at least once before any usage of the Dump Statistical Counters or Dump and Reset Statistical Counters commands. The address of the dump area must be placed in the General Pointer register. 0101 = **Dump Statistical Counters:** Tells the device to dump its statistical counters to the area designated by the Load Dump Counters Address command. 0110 = **Load CU Base:** The device's internal CU Base Register is loaded with the value in the CSB General Pointer. 0111 = **Dump and Reset Statistical Counters:** Tells the device to dump its statistical counters to the area designated by the Load Dump Counters Address command, and then to clear these counters. 1010 = **CU Static Resume:** Resume operation of the Command unit by executing the next command. This command will be ignored if the CU is idle. This command should be used only when the CU is in the Suspended state and has no pending CU Resume commands. 1011 = **CU HPQ Resume:** Resume execution of the first command on the HPQ CBL. this command will be ignored if the HPQ was never started.
3	Reserved.
2:0	**Receive Unit Command (RUC)**—R/W. Valid values are: 000 = **NOP:** Does not affect the current state of the unit. 001 = **RU Start:** Enables the receive unit. The pointer to the RFA must be placed in the SCB General POinter before using this command. The device pre-fetches the first RFD and the first RBD (if in flexible mode) in preparation to receive incoming frames that pass its address filtering. 010 = **RU Resume:** Resume frame reception (only when in suspended state). 011 = **RCV DMA Redirect:** Resume the RCV DMA when configured to "Direct DMA Mode." The buffers are indicated by an RBD chain which is pointed to by an offset stored in the General Pointer Register (this offset will be added to the RU Base). 100 = **RU Abort:** Abort RU receive operation immediately. 101 = **Load Header Data Size (HDS):** This value defines the size of the Header portion of the RFDs or Receive buffers. The HDS value is defined by the lower 14 bits of the SCB General Pointer, so bits 31:15 should always be set to zeros when using this command. Once a Load HDS command is issued, the device expects only to find Header RFDs, or be used in "RCV Direct DMA mode" until it is reset. Note that the value of HDS should be an even, non-zero number. 110 = **Load RU Base:** The device's internal RU Base Register is loaded with the value in the SCB General Pointer. 111 = **RBD Resume:** Resume frame reception into the RFA. This command should only be used when the RU is already in the "No Resources due to no RBDs" state or the "Suspended with no more RBDs" state.

7.2.3 System Control Block General Pointer Register

Offset Address: 04–07h
Default Value: 0000 0000h
Attribute: R/W
Size: 32 bits

Bit	Description
15:0	**SCB General Pointer.** The SCB General Pointer register is programmed by software to point to various data structures in main memory depending on the current SCB Command word.

7.2.4 PORT

Offset Address: 08–0Bh
Default Value: 0000 0000h
Attribute: R/W (special)
Size: 32 bits

The PORT interface allows the processor to reset the ICH3's internal LAN Controller, or perform an internal self test. The PORT DWord may be written as a 32-bit entity, two 16-bit entities, or four 8-bit entities. The LAN Controller will only accept the command after the high byte (offset 0Bh) is written, therefore the high byte must be written last.

Bit	Description
31:4	**Pointer Field.** A 16-byte aligned address must be written to this field when issuing a Self-Test command to the PORT interface.The results of the Self Test will be written to the address specified by this field.
3:0	**PORT Function Selection.** Valid values are listed below. All other values are Reserved. 0000 = **PORT Software Reset:** Completely resets the LAN Controller (all CSR and PCI registers). This command should not be used when the device is active. If a PORT Software Reset is desired, software should do a Selective Reset (described below), wait for the PORT register to be cleared (completion of the Selective Reset), and then issue the PORT Software Reset command. Software should wait approximately 10µs after issuing this command before attempting to access the LAN Controller's registers again. 0001 = **Self Test:** The Self-Test begins by issuing an internal Selective Reset followed by a general internal self-test of the LAN Controller. The results of the self-test are written to memory at the address specified in the Pointer field of this register. The format of the self-test result is shown in Table 7-5. After completing the self-test and writing the results to memory, the LAN Controller will execute a full internal reset and will re-initialize to the default configuration. Self-Test does not generate an interrupt of similar indicator to the host processor upon completion. 0010 = **Selective Reset:** Sets the CU and RU to the Idle state, but otherwise maintains the current configuration parameters (RU and CU Base, HDSSize, Error Counters, Configure information and Individual/Multicast Addresses are preserved). Software should wait approximately 10µs after issuing this command before attempting to access the LAN Controller's registers again.

Table 7-5. Self-Test Results Format

Bit	Description
31:13	Reserved.
12	**General Self-Test Result.** 0 = Pass 1 = Fail
11:6	Reserved.
5	**Diagnose Result.** This bit provides the result of an internal diagnostic test of the Serial Subsystem. 0 = Pass 1 = Fail
4	Reserved.
3	**Register Result.** This bit provides the result of a test of the internal Parallel Subsystem registers. 0 = Pass 1 = Fail
2	**ROM Content Result.** This bit provides the result of a test of the internal microcode ROM. 0 = Pass 1 = Fail
1:0	Reserved.

7.2.5 EEPROM Control Register

Offset Address: 0Eh Attribute: RO/R/W
Default Value: 00h Size: 8 bits

The EEPROM Control Register is a 16-bit field that enables a read from and a write to the external EEPROM.

Bit	Description
7:4	Reserved.
3	**EEPROM Serial Data Out (EEDO)**—RO. Note that this bit represents “Data Out” from the perspective of the EEPROM device. This bit contains the value read from the EEPROM when performing read operations.
2	**EEPROM Serial Data In (EEDI)**—WO. Note that this bit represents “Data In” from the perspective of the EEPROM device. The value of this bit is written to the EEPROM when performing write operations.
1	**EEPROM Chip Select (EECS)**—R/W. 0 = Drives the ICH3’s EE_CS signal low, to disable the EEPROM. this bit must be set to 0 for a minimum of 1µs between consecutive instruction cycles. 1 = Drives the ICH3’s EE_CS signal high, to enable the EEPROM.
0	**EEPROM Serial Clock (EESK)**—R/W. Toggling this bit, clocks data into or out of the EEPROM. Software must ensure that this bit is toggled at a rate that meets the EEPROM component’s minimum clock frequency specification. 0 = Drives the ICH3’s EE_SHCLK signal low. 1 = Drives the ICH3’s EE_SHCLK signal high.

7.2.6 Management Data Interface (MDI) Control Register

Offset Address:	10–13h	Attribute:	R/W (special)
Default Value:	0000 0000h	Size:	32 bits

The Management Data Interface (MDI) Control register is a 32-bit field and is used to read and write bits from the LAN Connect component. This register may be written as a 32-bit entity, two 16-bit entities, or four 8-bit entities. The LAN Controller will only accept the command after the high byte (offset 13h) is written, therefore the high byte must be written last.

Bit	Description
31:30	These bits are reserved and should be set to 00b.
29	**Interrupt Enable.** 0 = Disable. 1 = Enables the LAN Controller to assert an interrupt to indicate the end of an MDI cycle.
28	**Ready.** 0 = Expected to be reset by software at the same time the command is written. 1 = Set by the LAN Controller at the end of an MDI transaction.
27:26	**Opcode.** These bits define the opcode: 00 = Reserved 01 = MDI write 10 = MDI read 11 = Reserved
25:21	**LAN Connect Address.** This field of bits contains the LAN Connect address.
20:16	**LAN Connect Register Address.** This field of bits contains the LAN Connect Register Address.
15:0	**Data.** In a write command, software places the data bits in this field, and the LAN Controller transfers the data to the external LAN Connect component. During a read command, the LAN Controller reads these bits serially from the LAN Connect, and software reads the data from this location.

7.2.7 Receive DMA Byte Count Register

Offset Address:	14–17h	Attribute:	RO
Default Value:	0000 0000h	Size:	32 bits

Bit	Description
31:0	**Receive DMA Byte Count**—RO. Keeps track of how many bytes of receive data have been passed into host memory via DMA.

7.2.8 Early Receive Interrupt Register

Offset Address:	18h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

The Early Receive Interrupt register allows the internal LAN Controller to generate an early interrupt depending on the length of the frame. The LAN Controller will generate an interrupt at the end of the frame regardless of whether or not Early Receive Interrupts are enabled.

Note: It is recommended that software NOT utilize this register unless receive interrupt latency is a critical performance issue in that particular software environment. Using this feature may reduce receive interrupt latency, but will also result in the generation of more interrupts, which can degrade system efficiency and performance in some environments.

Bit	Description
7:0	**Early Receive Count**—R/W. When some non-zero value ***x*** is programmed into this register, the LAN Controller will set the ER bit in the SCB Status Word Register and assert INTA# when the byte count indicates that there are ***x*** quad-words remaining to be received in the current frame (based on the Type/Length field of the received frame). No Early Receive interrupt will be generated if a value of 00h (the default value) is programmed into this register.

7.2.9 Flow Control Register

Offset Address: 19–1Ah
Default Value: 0000h
Attribute: RO, R/W (special)
Size: 16 bits

Bit	Description
15:13	Reserved.
12	**FC Paused Low**—RO. 0 = Cleared when the FC timer reaches zero, or a Pause frame is received. 1 = Set when the LAN Controller receives a Pause Low command with a value greater than zero.
11	**FC Paused**—RO. 0 = Cleared when the FC timer reaches zero. 1 = Set when the LAN Controller receives a Pause command regardless of its cause (FIFO reaching Flow Control Threshold, fetching a Receive Frame Descriptor with its flow control pause bit set, or software writing a 1 to the Xoff bit).
10	**FC Full**—RO. 0 = Cleared when the FC timer reaches zero. 1 = Set when the LAN Controller sends a Pause command with a value greater than zero.
9	**Xoff**—R/W (special). This bit should only be used if the LAN Controller is configured to operate with IEEE frame-based flow control. 0 = This bit can only be cleared by writing a 1 to the Xon bit (bit 8 in this register). 1 = Writing a 1 to this bit forces the Xoff request to 1 and causes the LAN Controller to behave as if the FIFO extender is full. This bit will also be set to 1 when an Xoff request due to an “RFD Xoff” bit.
8	**Xon**—WO. This bit should only be used if the LAN Controller is configured to operate with IEEE frame-based flow control. 0 = This bit always returns 0 on reads. 1 = Writing a 1 to this bit resets the Xoff request to the LAN Controller, clearing bit 9 in this register.
7:3	Reserved.
2:0	**Flow Control Threshold**—R/W. The LAN Controller can generate a Flow Control Pause frame when its Receive FIFO is almost full. The value programmed into this field determines the number of bytes still available in the Receive FIFO when the Pause frame is generated. **Bits 2:0** / **Free Bytes in Receive FIFO** / **Comment** 000 — 0.50 KB — Fast system (recommended default) 001 — 1.00 KB 010 — 1.25 KB 011 — 1.50 KB 100 — 1.75 KB 101 — 2.00 KB 110 — 2.25 KB 111 — 2.50 KB — Slow system

7.2.10 Power Management Driver (PMDR) Register

Offset Address:	1Bh	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

The ICH3's internal LAN Controller provides an indication in the PMDR that a wake-up event has occurred.

Bit	Description
7	**Link Status Change Indication**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = The link status change bit is set following a change in link status.
6	**Magic Packet***—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = This bit is set when a Magic Packet is received regardless of the Magic Packet wake-up disable bit in the configuration command and the PME Enable bit in the power management control/ status register.
5	**Interesting Packet**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = This bit is set when an "interesting" packet is received. Interesting packets are defined by the LAN Controller packet filters.
4:1	Reserved.
0	**PME Status**—R/WC. This bit is a reflection of the PME status bit in the Power Management Control/ Status Register (PMCSR). 0 = Software clears this bit by writing a 1 to the bit location. This also clears the PME status bit in the PMCSR and de-asserts the PME signal. 1 = Set upon a wake-up event, independent of the PME enable bit.

7.2.11 General Control Register

Offset Address:	1Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:4	Reserved. These bits should be set to 0000b.
3	**LAN Connect Software Reset**—R/W. 0 = Cleared by software to begin normal LAN Connect operating mode. Software must not attempt to access the LAN Connect interface for at least 1 ms after clearing this bit. 1 = Software can set this bit to force a reset condition on the LAN Connect interface.
2	Reserved. This bit should be set to 0.
1	**Deep Power-Down on Link Down Enable.** 0 = Disable. 1 = The ICH3's internal LAN Controller may enter a deep power-down state (sub-3 mA) in the D2 and D3 power states while the link is down. In this state, the LAN Controller does not keep link integrity. This state is not supported for point-to-point connection of two end stations.
0	Reserved.

7.2.12 General Status Register

Offset Address: 1Dh Attribute: RO
Default Value: N/A Size: 8 bits

Bit	Description
7:3	Reserved.
2	**Duplex Mode.** This bit indicates the wire duplex mode. 0 = Half duplex 1 = Full duplex
1	**Speed.** This bit indicates the wire speed: 0 = 10 Mbps 1 = 100 Mbps
0	**Link Status Indication.** This bit indicates the status of the link: 0 = Invalid 1 = Valid

7.2.13 Statistical Counters

The ICH3's integrated LAN Controller provides information for network management statistics by providing on-chip statistical counters that count a variety of events associated with both transmit and receive. The counters are updated by the LAN Controller when it completes the processing of a frame (that is, when it has completed transmitting a frame on the link or when it has completed receiving a frame). The Statistical Counters are reported to the software on demand by issuing the Dump Statistical Counters command or Dump and Reset Statistical Counters command in the SCB Command Unit Command (CUC) field.

Table 7-6. Statistical Counters

ID	Counter	Description
0	Transmit Good Frames	This counter contains the number of frames that were transmitted properly on the link. It is updated only after the actual transmission on the link is completed, not when the frame was read from memory as is done for the Transmit Command Block status.
4	Transmit Maximum Collisions (MAXCOL) Errors	This counter contains the number of frames that were not transmitted because they encountered the configured maximum number of collisions.
8	Transmit Late Collisions (LATECOL) Errors	This counter contains the number of frames that were not transmitted since they encountered a collision later than the configured slot time.
12	Transmit Underrun Errors	A transmit underrun occurs because the processor system bus cannot keep up with the transmission. This counter contains the number of frames that were either not transmitted or retransmitted due to a transmit DMA underrun. If the LAN Controller is configured to retransmit on underrun, this counter may be updated multiple times for a single frame.
16	Transmit Lost Carrier Sense (CRS)	This counter contains the number of frames that were transmitted by the LAN Controller despite the fact that it detected the de-assertion of CRS during the transmission.
20	Transmit Deferred	This counter contains the number of frames that were deferred before transmission due to activity on the link.
24	Transmit Single Collisions	This counter contains the number of transmitted frames that encountered one collision.

Table 7-6. Statistical Counters (Continued)

ID	Counter	Description
28	Transmit Multiple Collisions	This counter contains the number of transmitted frames that encountered more than one collision.
32	Transmit Total Collisions	This counter contains the total number of collisions that were encountered while attempting to transmit. This count includes late collisions and frames that encountered MAXCOL.
36	Receive Good Frames	This counter contains the number of frames that were received properly from the link. It is updated only after the actual reception from the link is completed and all the data bytes are stored in memory.
40	Receive CRC Errors	This counter contains the number of aligned frames discarded because of a CRC error. This counter is updated, if needed, regardless of the Receive Unit state. The Receive CRC Errors counter is mutually exclusive of the Receive Alignment Errors and Receive Short Frame Errors counters.
44	Receive Alignment Errors	This counter contains the number of frames that are both misaligned (for example, CRS de-asserts on a non-octal boundary) and contain a CRC error. The counter is updated, if needed, regardless of the Receive Unit state. The Receive Alignment Errors counter is mutually exclusive of the Receive CRC Errors and Receive Short Frame Errors counters.
48	Receive Resource Errors	This counter contains the number of good frames discarded due to unavailability of resources. Frames intended for a host whose Receive Unit is in the No Resources state fall into this category. If the LAN Controller is configured to Save Bad Frames and the status of the received frame indicates that it is a bad frame, the Receive Resource Errors counter is not updated.
52	Receive Overrun Errors	This counter contains the number of frames known to be lost because the local system bus was not available. If the traffic problem persists for more than one frame, the frames that follow the first are also lost; however, because there is no lost frame indicator, they are not counted.
56	Receive Collision Detect (CDT)	This counter contains the number of frames that encountered collisions during frame reception.
60	Receive Short Frame Errors	This counter contains the number of received frames that are shorter than the minimum frame length. The Receive Short Frame Errors counter is mutually exclusive to the Receive Alignment Errors and Receive CRC Errors counters. A short frame will always increment only the Receive Short Frame Errors counter.
64	Flow Control Transmit Pause	This counter contains the number of Flow Control frames transmitted by the LAN Controller. This count includes both the Xoff frames transmitted and Xon (PAUSE(0)) frames transmitted.
68	Flow Control Receive Pause	This counter contains the number of Flow Control frames received by the LAN Controller. This count includes both the Xoff frames received and Xon (PAUSE(0)) frames received.
72	Flow Control Receive Unsupported	This counter contains the number of MAC Control frames received by the LAN Controller that are not Flow Control Pause frames. These frames are valid MAC control frames that have the predefined MAC control Type value and a valid address but has an unsupported opcode.
76	Receive TCO Frames	This counter contains the number of TCO packets received by the LAN Controller.
78	Transmit TCO Frames	This counter contains the number of TCO packets transmitted.

The Statistical Counters are initially set to zero by the ICH3's integrated LAN Controller after reset. They cannot be preset to anything other than zero. The LAN Controller increments the counters by internally reading them, incrementing them and writing them back. This process is invisible to the processor and PCI bus. In addition, the counters adhere to the following rules:

- The counters are wrap-around counters. After reaching FFFFFFFFH the counters wrap around to 0.
- The LAN Controller updates the required counters for each frame. It is possible for more than one counter to be updated as multiple errors can occur in a single frame.
- The counters are 32 bits wide and their behavior is fully compatible with the IEEE 802.1 standard. The LAN Controller supports all mandatory and recommend statistics functions through the status of the receive header and directly through these Statistical Counters.

The processor can access the counters by issuing a Dump Statistical Counters SCB command. This provides a "snapshot", in main memory, of the internal LAN Controller statistical counters. The LAN Controller supports 21 counters. The dump could consist of the either 16, 19, or all 21 counters, depending on the status of the Extended Statistics Counters and TCO Statistics configuration bits in the Configuration command.

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Hub Interface to PCI Bridge Registers (D30:F0) 8

The hub interface to PCI Bridge resides in PCI Device 30, Function 0 on bus #0. This portion of the ICH3 implements the buffering and control logic between PCI and the hub interface. The arbitration for the PCI bus is handled by this PCI device. The PCI decoder in this device must decode the ranges for the hub interface. All register contents will be lost when core well power is removed.

8.1 PCI Configuration Registers (D30:F0)

Note: Registers that are not shown should be treated as Reserved (See Section 6.2 for details).

Table 8-1. PCI Configuration Map (HUB-PCI—D30:F0)

Offset	Mnemonic	Register Name/Function	Default	Type
00–01h	VID	Vendor ID	8086h	RO
02–03h	DID	Device ID	244Eh	RO
04–05h	CMD	PCI Device Command	0001h	R/W
06–07h	PD_STS	PCI Device Status	0080h	R/W
08h	REVID	Revision ID	See Note	RO
0Ah	SCC	Sub Class Code	04h	RO
0Bh	BCC	Base Class Code	06h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	01h	RO
18h	PBUS_NUM	Primary Bus Number	00h	RO
19h	SBUS_NUM	Secondary Bus Number	00h	R/W
1Ah	SUB_BUS_NUM	Subordinate Bus Number	00h	R/W
1Bh	SMLT	Secondary Master Latency Timer	00h	R/W
1Ch	IOBASE	I/O Base Register	F0h	R/W
1Dh	IOLIM	I/O Limit Register	00h	R/W
1E–1Fh	SECSTS	Secondary Status	0280h	R/W
20–21h	MEMBASE	Memory Base	FFF0h	R/W
22–23h	MEMLIM	Memory Limit	0000h	R/W
24–25h	PREF_MEM_BASE	Prefetchable Memory Base	0000h	RO
26–27h	PREF_MEM_MLT	Prefetchable Memory Limit	0000h	RO
30–31h	IOBASE_HI	I/O Base Upper 16 Bits	0000h	RO
32–33h	IOLIMIT_HI	I/O Limit Upper 16 Bits	0000h	RO
3Ch	INT_LINE	Interrupt Line	00h	RO
3E–3Fh	BRIDGE_CNT	Bridge Control	0000h	R/W

Table 8-1. PCI Configuration Map (HUB-PCI—D30:F0) (Continued)

Offset	Mnemonic	Register Name/Function	Default	Type
40h	BRIDGE_CNT2	Bridge Control 2	00	R/W
44–45h	DEVICE_HIDE	Secondary PCI Device Hiding	00	R/W
50–51h	CNF	ICH3 Configuration	1400h	R/W
70h	MTT	Multi-Transaction Timer	20h	R/W
82h	PCI_MAST_STS	PCI Master Status	00h	R/W
90h	ERR_CMD	Error Command Register	00h	R/W
92h	ERR_STS	Error Status Register	00h	R/W

NOTE: Refer to the Specification Update for the Revision ID.

8.1.1 VID—Vendor ID Register (HUB-PCI—D30:F0)

Offset Address: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor Identification Value**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h.

8.1.2 DID—Device ID Register (HUB-PCI—D30:F0)

Offset Address: 02–03h
Default Value: 244Eh
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device Identification Value**—RO. This is a 16 bit value assigned to the ICH3 hub interface to PCI bridge (i.e., Device #2). DID = 244Eh

8.1.3 CMD—Command Register (HUB-PCI—D30:F0)

Offset Address: 04–05h
Default Value: 0001h
Attribute: R/W
Size: 16 bits

Bit	Description
15:10	Reserved.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0. The ICH3 does not support this capability.
8	**SERR# Enable (SERR_EN)**—R/W. 0 = Disable 1 = Enable the ICH3 to generate an NMI (or SMI# if NMI routed to SMI#) when the D30:F0 SSE bit (offset 06h, bit 14) is set.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	**Parity Error Response (PER)**—R/W. 0 = The ICH3 will ignore parity errors on the hub interface. 1 = The ICH3 is allowed to report parity errors detected on the hub interface.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0 by P2P Bridge spec.
2	**Bus Master Enable (BME)**—R/W. 0 = Disable 1 = Allows the Hub interface-to-PCI bridge to accept cycles from PCI to run on the hub interface. Note: This bit does not affect the CF8h and CFCh I/O accesses. **NOTE:** Cycles that generated from the ICH3's Device 31 functionality are not blocked by clearing this bit. (PC/PCI Cascade Mode cycles may be blocked).
1	**Memory Space Enable (MSE)**—R/W. The ICH3 provides this bit as read/writable for software only. However, the ICH3 ignores the programming of this bit, and runs hub interface memory cycles to PCI.
0	**I/O Space Enable (IOE)**—R/W. The ICH3 provides this bit as read/writable for software only. However, the ICH3 ignores the programming of this bit and runs hub interface I/O cycles to PCI that are not intended for USB, IDE, or AC '97.

8.1.4 PD_STS—Primary Device Status Register (HUB-PCI—D30:F0)

Offset Address:	06–07h	Attribute:	R/WC
Default Value:	0080h	Size:	16 bits

For the writable bits in this register, writing a 1 will clear the bit. Writing a 0 to the bit will have no effect.

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = Indicates that the ICH3 detected a parity error on the hub interface. This bit gets set even if the Parity Error Response bit (offset 04, bit 6) is not set.
14	**Signaled System Error (SSE)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = An address, or command parity error, or special cycles data parity error has been detected on the PCI bus, and the Parity Error Response bit (D30:F0, Offset 04h, bit 6) is set. If this bit is set because of parity error and the D30:F0 SERR_EN bit (Offset 04h, bit 8) is also set, the ICH3 will generate an NMI (or SMI# if NMI routed to SMI#).
13	**Received Master Abort (RMA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = ICH3 received a master abort from the hub interface device.
12	**Received Target Abort (RTA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = ICH3 received a target abort from the hub interface device. The TCO logic can cause an SMI#, NMI, or interrupt based on this bit getting set.
11	**Signaled Target Abort (STA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = ICH3 signals a target abort condition on the hub interface.
10:9	DEVSEL# Timing Status (DEV_STS)—RO. 00h = Fast timing. This register applies to the hub interface; therefore, this field does not matter.
8	**Master Data Parity Error Detected (MDPD)—**R/WC. Since this register applies to the hub interface, the ICH3 must interpret this bit differently than it is in the PCI spec. 0 = Software clears this bit by writing a 1 to the bit location. 1 = ICH3 detects a parity error on the hub interface and the Parity Error Response bit in the Command Register (offset 04h, bit 6) is set.
7	Fast Back to Back (FB2B)—RO. Hardwired to 1.
6	User Definable Features (UDF)—RO. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0.
4:0	Reserved.

8.1.5 REVID—Revision ID Register (HUB-PCI—D30:F0)

Offset Address: 08h
Default Value: See Note
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision Identification Value**—RO. 8-bit value that indicates the revision number for the ICH3 hub interface to PCI bridge.

NOTE: Refer to the Specification Update for the Revision ID.

8.1.6 SCC—Sub Class Code Register (HUB-PCI—D30:F0)

Offset Address: 0Ah
Default Value: 04h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code**—RO. 8-bit value that indicates the category of bridge for the ICH3 hub interface to PCI bridge. The code is 04h indicating a PCI-to-PCI bridge.

8.1.7 BCC—Base-Class Code Register (HUB-PCI—D30:F0)

Offset Address: 0Bh
Default Value: 06h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code**—RO. 8-bit value that indicates the type of device for the ICH3 hub interface to PCI bridge. The code is 06h indicating a bridge device.

8.1.8 PMLT—Primary Master Latency Timer Register (HUB-PCI—D30:F0)

Offset Address: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

This register does not apply to hub interface.

Bit	Description
7:3	Master Latency Timer Count (MLTC). Not implemented.
2:0	Reserved.

8.1.9 HEADTYP—Header Type Register (HUB-PCI—D30:F0)

Offset Address: 0Eh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7	Multi-Function Device—RO. This bit is 0 to indicate a single function device.
6:0	Header Type—RO. 8-bit field identifies the header layout of the configuration space, which is a PCI-to-PCI bridge in this case.

8.1.10 PBUS_NUM—Primary Bus Number Register (HUB-PCI—D30:F0)

Offset Address: 18h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Primary Bus Number**—RO. This field indicates the bus number of the hub interface and is hardwired to 00h.

8.1.11 SBUS_NUM—Secondary Bus Number Register (HUB-PCI—D30:F0)

Offset Address: 19h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Secondary Bus Number**—R/W. This field indicates the bus number of PCI. **NOTE:** When this number is equal to the primary bus number (i.e., bus #0), the ICH3 will run hub interface configuration cycles to this bus number as Type 1 configuration cycles on PCI.

8.1.12 SUB_BUS_NUM—Subordinate Bus Number Register (HUB-PCI—D30:F0)

Offset Address: 1A
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Subordinate Bus Number**—R/W. This field specifies the highest PCI bus number below the hub interface to PCI bridge. If a Type 1 configuration cycle from the hub interface does not fall in the Secondary-to-Subordinate Bus ranges of Device 30, the ICH3 will indicate a master abort back to the hub interface.

8.1.13 SMLT—Secondary Master Latency Timer Register (HUB-PCI—D30:F0)

Offset Address: 1Bh Attribute: R/W
Default Value: 00h Size: 8 bits

This Master Latency Timer (MLT) controls the amount of time that the ICH3 will continue to burst data as a master on the PCI bus. When the ICH3 starts the cycle after being granted the bus, the counter is loaded and starts counting down from the assertion of FRAME#. If the internal grant to this device is removed, then the expiration of the MLT counter will result in the de-assertion of FRAME#. If the internal grant has not been removed, then the ICH3 can continue to own the bus.

Bit	Description
7:3	**Master Latency Timer Count (MLTC)**—R/W. 5-bit value that indicates the number of PCI clocks, in 8-clock increments, that the ICH3 will remain as master of the bus.
2:0	Reserved.

8.1.14 IOBASE—I/O Base Register (HUB-PCI—D30:F0)

Offset Address: 1Ch Attribute: R/W
Default Value: F0h Size: 8 bits

Bit	Description
7:4	**I/O Address Base Bits [15:12]**—R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	**I/O Addressing Capability**—RO. This is hardwired to 0h, indicating that the hub interface to PCI bridge does not support 32-bit I/O addressing. This means that the I/O Base & Limit Upper Address registers must be read only.

8.1.15 IOLIM—I/O Limit Register (HUB-PCI—D30:F0)

Offset Address: 1Dh Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:4	**I/O Address Limit Bits [15:12]**—R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
3:0	**I/O Addressing Capability**—RO. This is hardwired to 0h, indicating that the hub interface-to-PCI bridge does not support 32-bit I/O addressing. This means that the I/O Base & Limit Upper Address registers must be read only.

8.1.16 SECSTS—Secondary Status Register (HUB-PCI—D30:F0)

Offset Address:	1E–1Fh	Attribute:	R/W
Default Value:	0280h	Size:	16 bits

For the writable bits in this register, writing a 1 will clear the bit. Writing a 0 to the bit will have no effect.

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = This bit is cleared by software writing a 1. 1 = ICH3 detected a parity error on the PCI bus.
14	**Received System Error (SSE)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = SERR# assertion is received on PCI.
13	**Received Master Abort (RMA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Hub interface to PCI cycle is master-aborted on PCI.
12	**Received Target Abort (RTA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Hub interface to PCI cycle is target-aborted on PCI. For “completion required” cycles from the hub interface, this event should also set the Signaled Target Abort in the primary status register in this device, and the ICH3 must send the “target abort” status back to the hub interface.
11	Signaled Target Abort (STA)—RO. The ICH3 does not generate target aborts.
10:9	DEVSEL# Timing Status (DEV_STS)—RO. 01h = Medium timing.
8	**Master Data Parity Error Detected (MDPD)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = The ICH3 sets this bit when all of the following three conditions are met: - The parity error response enable bit in the bridge control register (bit 0, offset 3Eh) is set - USB, AC ’97 or IDE is a Master - PERR# asserts during a write cycle ***OR*** a parity error is detected internally during a read cycle
7	Fast Back to Back (FB2B)—RO. Hardwired to 1 to indicate that the PCI to hub interface target logic is capable of receiving fast back-to-back cycles.
6	User Definable Features (UDF)—RO. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0.
4:0	Reserved.

8.1.17 MEMBASE—Memory Base Register (HUB-PCI—D30:F0)

Offset Address: 20–21h
Default Value: FFF0h
Attribute: R/W
Size: 16 bits

This register defines the base of the hub interface to PCI non-prefetchable memory range. Since the ICH3 will forward all hub interface memory accesses to PCI, the ICH3 will only use this information for determining when not to accept cycles as a target.

This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Memory Address Base**—R/W. Defines the base of the memory range for PCI. These 12 bits correspond to address bits 31:20.
3:0	Reserved.

8.1.18 MEMLIM—Memory Limit Register (HUB-PCI—D30:F0)

Offset Address: 22–23h
Default Value: 0000h
Attribute: R/W
Size: 16 bits

This register defines the upper limit of the hub interface to PCI non-prefetchable memory range. Since the ICH3 will forward all hub interface memory accesses to PCI, the ICH3 will only use this information for determining when not to accept cycles as a target.

This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Memory Address Limit**—R/W. Defines the top of the memory range for PCI. These 12 bits correspond to address bits 31:20.
3:0	Reserved.

8.1.19 PREF_MEM_BASE—Prefetchable Memory Base Register (HUB-PCI—D30:F0)

Offset Address: 24h–25h
Default Value: 0000FFF0h
Attribute: R/W
Size: 16-bit

Bit	Description
15:4	**Prefetchable Memory Address Base**—R/W. Defines the base address of the prefetchable memory address range for PCI. These 12 bits correspond to address bits 31:20.
3:0	Reserved. RO.

8.1.20 PREF_MEM_MLT—Prefetchable Memory Limit Register (HUB-PCI—D30:F0)

Offset Address: 26h–27h
Default Value: 00000000h
Attribute: R/W
Size: 16-bit

Bit	Description
15:4	**Prefetchable Memory Address Limit**—RW. Defines the limit address of the prefetchable memory address range for PCI. These 12 bits correspond to address bits 31:20.
3:0	Reserved. RO

8.1.21 IOBASE_HI—I/O Base Upper 16 Bits Register (HUB-PCI—D30:F0)

Offset Address: 30–31h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	I/O Address Base Upper 16 Bits [31:16]—RO. Not supported; hardwired to 0.

8.1.22 IOLIM_HI—I/O Limit Upper 16 Bits Register (HUB-PCI—D30:F0)

Offset Address: 32–33h
Default Value: 0000h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	I/O Address Limit Upper 16 Bits [31:16]—RO. Not supported; hardwired to 0.

8.1.23 INT_LINE—Interrupt Line Register (HUB-PCI—D30:F0)

Offset Address: 3Ch
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Interrupt Line (INT_LN)—RO. Hardwired to 00h. The bridge does not generate interrupts, and interrupts from downstream devices are routed around the bridge.

8.1.24 BRIDGE_CNT—Bridge Control Register (HUB-PCI—D30:F0)

Offset Address: 3E–3Fh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:8	Reserved.
7	Fast Back to Back Enable—RO. Hardwired to 0. The PCI logic will not generate fast back-to-back cycles on the PCI bus.
6	Secondary Bus Reset—RO. hardwired to 0. The ICH3 does not follow the P2P bridge reset scheme; Software-controlled resets are implemented in the PCI-LPC device.
5	**Master Abort Mode**—R/W. This bit controls the behavior of the ICH3 when a master abort occurs on a transaction that crosses the hub interface-PCI bridge in either direction. The default is 0. When set to 0, the ICH3 behaves in the following manner: • **Hub Interface Completion-Required requests to PCI:** When these master abort on PCI, the ICH3 returns a master abort status. For reads, FFFFh is returned for each DWord. • **Hub Interface Posted Writes to PCI:** When these master abort on PCI, the ICH3 discards the data. • **PCI Reads to Hub Interface:** When these master abort on Hub Interface, the ICH3 returns the data provided with the Hub Interface master abort packet to the PCI requestor. • **PCI writes to Hub Interface:** The ICH3 has no idea when these "master-abort." When set to 1, the ICH3 treats the master abort as an error: • **Hub Interface Completion-Required requests to PCI:** When these master abort on PCI, the ICH3 returns a target abort status. For reads, FFFFh is returned for each DWord. • **Hub Interface Posted Writes to PCI:** When these master abort on PCI, the ICH3 discards the data and sets the Primary Signaled SERR# bit (if the corresponding SERR_EN bit is set). • **PCI Reads to Hub Interface:** When these master abort on Hub Interface, the ICH3 terminates the cycle with a target abort and flushes the remainder of the prefetched data. • **PCI writes to Hub Interface:** the ICH3 has no idea when these "master-abort."
4	**VGA 16-Bit Decode.** This bit does not have any functionality relative to address decodes because the ICH3 will forward the cycles to PCI, independent of the decode. Writes of 1 have no impact other than to force the bit to 1. Writes of 0 have no impact other than to force the bit to 0. Reads to this bit will return the previously written value (or 0 if no writes since reset).
3	**VGA Enable**—R/W. 0 = No VGA device on PCI. 1 = Indicates that the VGA device is on PCI. Therefore, the PCI to hub interface decoder will not accept memory cycles in the range A0000h–BFFFFh. Note that the ICH3 will never take I/O cycles in the VGA range from PCI.
2	**ISA Enable**—R/W. The ICH3 ignores this bit. However, this bit is read/write for software compatibility. Since the ICH3 forwards all I/O cycles that are not in the USB, AC '97, or IDE ranges to PCI, this bit would have no effect.
1	**SERR# Enable**—R/W. 0 = Disable 1 = If this bit is set AND bit 8 in CMD register (D30:F0 Offset 04h) is also set, the ICH3 will set the SSE bit in PD_STS register (D30:F0, offset 06h, bit 14) AND also generate an NMI (or SMI# if NMI routed to SMI) when the SERR# signal is asserted.
0	**Parity Error Response Enable**—R/W. 0 = Disable 1 = Enable the hub interface to PCI bridge for parity error detection and reporting on the PCI bus.0 =

8.1.25 BRIDGE_CNT2—Bridge Control Register 2 (HUB-PCI—D30:F0)

Offset Address:	40h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:1	Reserved.
0	**PCI_DAC_EN**—R/W. Allows ICH3 to recognize external PCI masters performing DAC on PCI. 0 = Disable 1 = Enable

8.1.26 DEVICE_HIDE—Secondary PCI Device Hiding Register (HUB-PCI—D30:F0)

Offset Address:	44–45h	Attribute:	R/W
Default Value:	00h	Size:	16 bits
Power Well:	00h		

This register allows software to “hide” PCI devices (0 through 5) in terms of configuration space. Specifically, when PCI devices (0–5) are hidden, the configuration space is not accessible because the PCI IDSEL pin does not assert. The ICH3 supports the hiding of 6 external devices (0 through 5), which matches the number of PCI request/grant pairs, and the ability to hide the integrated LAN device by masking out the configuration space decode of LAN controller. Writing a 1 to this bit will not restrict the configuration cycle to the PCI bus. This differs from bits 0 through 5 in which the configuration cycle is restricted.

Hiding a PCI device can be useful for debugging, bug work-arounds, and system management support. Devices should only be hidden during initialization before any configuration cycles are run. This guarantees that the device is not in a semi-enable state.

Bit	Description
15:9	Reserved.
8	**HIDE_DEV8.** Same as bit 0 of this register, except for device 8 (AD[24]), which is hardwired to the integrated LAN device. This bit will not change the way the configuration cycle appears on PCI bus
7:6	Reserved.
5	**HIDE_DEV5.** Same as bit 0 of this register, except for device 5 (AD[21]).
4	**HIDE_DEV4.** Same as bit 0 of this register, except for device 4 (AD[20]).
3	**HIDE_DEV3.** Same as bit 0 of this register, except for device 3 (AD[19]).
2	**HIDE_DEV2.** Same as bit 0 of this register, except for device 2 (AD[18]).
1	**HIDE_DEV1.** Same as bit 0 of this register, except for device 1 (AD[17]).
0	**HIDE_DEV0.** 0 = The PCI configuration cycles for this slot are not affected. 1 = Device 0 hidden on the PCI bus. This is done by masking the IDSEL (keeping it low) for configuration cycles to that device. Since the device does not see its IDSEL go active, it does not respond to PCI configuration cycles and the processor thinks the device is not present. AD[16] is used as IDSEL for device 0.

8.1.27 CNF—ICH3 Configuration Register (HUB-PCI—D30:F0)

Offset Address: 50–51h
Default Value: 1400h
Attribute: R/W
Size: 16 bits

Bit	Description
15:10	Reserved.
9	**HP_PCI_EN**—R/W. High Priority PCI Enable. 0 = All PCI REQ#/GNT pairs have the same arbitration priority. 1 = Enables a mode where the REQ[0]#/GNT[0]# signal pair has a higher arbitration priority.
8	**Hole Enable (15 MB–16 MB)—**R/W. 0 = Disable 1 = Enables the 15-MB to 16-MB hole in the DRAM.
7:2	Reserved.
1	**12-Clock Retry Enable**—R/W. System BIOS must set this bit for PCI compliance. 0 = If this bit is not set, under the same circumstance, the bus will not be released since all other masters see the lock in use. 1 = When a PCI Master is running a locked memory read or write cycle, while all other bus masters are waiting to run locked cycles, this bit, when set allows the ICH3 to retry the cycle after 12 PCI clocks.
0	Reserved.

8.1.28 MTT—Multi-Transaction Timer Register (HUB-PCI—D30:F0)

Offset Address: 70h
Default Value: 20h
Attribute: R/W
Size: 8 bits

MTT is an 8-bit register that controls the amount of time that the ICH3's arbiter allows a PCI initiator to perform multiple back-to-back transactions on the PCI bus. The ICH3's MTT mechanism is used to guarantee a fair share of the Primary PCI bandwidth to an initiator that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers).

The number of clocks programmed in the MTT represents the guaranteed time slice (measured in PCI clocks) allotted to the current agent, after which the arbiter will grant another agent that is requesting the bus. The MTT value must be programmed with 8 clock granularity in the same manner as MLT. For example, if the MTT is programmed to 18h, then the selected value corresponds to the time period of 24 PCI clocks.The default value of MTT is 20h (32 PCI clocks).

Note: Programming the MTT to a value of 00h disables this function, which could cause starvation problems for some PCI master devices. Programming of the MTT to anything less than 16 clocks will not allow the Grant-to-FRAME# latency to be 16 clocks. The MTT timer will timeout before the Grant-to-FRAME# trigger causing a re-arbitration.

Bit	Description
7:3	**Multi-Transaction Timer Count Value**—R/W. This field specifies the amount of time that grant will remain asserted to a master continuously asserting its request for multiple transfers. This field specifies the count in an 8-clock (PCI clock) granularity.
2:0	Reserved.

8.1.29 PCI_MAST_STS—PCI Master Status Register (HUB-PCI—D30:F0)

Offset Address:	82h	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Bit	Description
7	**Internal PCI Master Request Status (INT_MREQ_STS)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = The ICH3's internal DMA controller or LPC has requested use of the PCI bus.
6	**Internal LAN Master Request Status (LAN_MREQ_STS)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = The ICH3's internal LAN controller has requested use of the PCI bus.
5:0	**PCI Master Request Status (PCI_MREQ_STS)**—R/WC. Allows software to see if a particular bus master has requested use of the PCI bus. For example, bit 0 will be set if ICH3 has detected REQ[0]# asserted and bit 5 will be set if ICH3 detected REQ[5]# asserted. 0 = Software clears these bits by writing a 1 to the bit position. 1 = The associated PCI master has requested use of the PCI bus.

8.1.30 ERR_CMD—Error Command Register (HUB-PCI—D30:F0)

Offset Address:	90h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

This register configures the ICH3's Device 30 responses to various system errors. The actual assertion of the internal SERR# (routed to cause NMI# or SMI#) is enabled via the PCI Command register.

Bit	Description
7:3	Reserved.
2	**SERR# Enable on Receiving Target Abort (SERR_RTA_EN)**—R/W. 0 = Disable 1 = Enable. When SERR_EN is set, the ICH3 will report SERR# when SERR_RTA is set.
1	**SERR# Enable on Delayed Transaction Timeout (SERR_DTT_EN)**—R/W. 0 = Disable 1 = Enable. When SERR_EN is set, the ICH3 will report SERR# when SERR_DTT is set.
0	Reserved.

8.1.31 ERR_STS—Error Status Register (HUB-PCI—D30:F0)

Offset Address:	92h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

This register records the cause of system errors in Device 30. The actual assertion of SERR# is enabled via the PCI Command register.

Bit	Description
7:3	Reserved.
2	**SERR# Due to Received Target Abort (SERR_RTA)**—R/W. 0 = This bit is cleared by writing a 1. 1 = The ICH3 sets this bit when the ICH3 receives a target abort. If SERR_EN, the ICH3 will also generate an SERR# when SERR_RTA is set.
1	**SERR# Due to Delayed Transaction Timeout (SERR_DTT)**—R/W. 0 = This bit is cleared by writing a 1 1 = When a PCI master does not return for the data within 1024 clocks of the cycle's completion, the ICH3 clears the delayed transaction, and sets this bit. If both SERR_DTT_EN and SERR_EN are set, then ICH3 will also generate an SERR# when SERR_DTT is set..
0	Reserved.

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LPC I/F Bridge Registers (D31:F0) 9

The LPC Bridge function of the ICH3 resides in PCI Device 31:Function 0. This function contains many other functional units, such as DMA and Interrupt Controllers, Timers, Power Management, System Management, GPIO, RTC, and LPC Configuration Registers.

Registers and functions associated with other functional units (USB 1.1, IDE, etc.) are described in their respective Sections.

9.1 PCI Configuration Registers (D31:F0)

Note: Registers that are not shown should be treated as Reserved (See Section 6.2 for details).

Table 9-1. PCI Configuration Map (LPC I/F—D31:F0)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor ID	8086h	RO
02–03h	DID	Device ID	2480h	RO
04–05h	PCICMD	PCI Command	000Fh	R/W
06–07h	PCISTA	PCI Device Status	0280h	R/W
08h	RID	Revision ID	See Note 1	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	06h	RO
0Eh	HEADT	Header Type	80h	RO
40–43h	PMBASE	ACPI Base Address	00000001h	R/W
44h	ACPI_CNTL	ACPI Control	00h	R/W
4E–4Fh	BIOS_CNTL	BIOS Control	0000h	R/W
54h	TCO_CNTL	TCO Control	00h	R/W
58–5Bh	GPIO_BASE	GPIO Base Address	00000001h	R/W
5Ch	GPIO_CNTL	GPIO Control	00h	R/W
60–63h	PIRQ[*n*]_ROUT	PIRQ[A–D] Routing Control	80808080h	R/W
64h	SIRQ_CNTL	Serial IRQ Control	10h	R/W
68–6Bh	PIRQ[*n*]_ROUT	PIRQ[E–H] Routing Control	80808080h	R/W
88h	D31_ERR_CFG	Device 31 Error Configuration	00h	R/W
8Ah	D31_ERR_STS	Device 31 Error Status	00h	R/W
90–91h	PCI_DMA_C	PCI DMA Configuration	0000h	R/W
A0–CFh		Power Management (See Section 9.8.1)		
D0–D3h	GEN_CNTL	General Control	00000000h	R/W
D4–D7h	GEN_STA	General Status	00000F00h	R/W
D8h	RTC_CONF	Real Time Clock Configuration	00h	R/W

Table 9-1. PCI Configuration Map (LPC I/F—D31:F0) (Continued)

Offset	Mnemonic	Register Name	Default	Type
E0h	COM_DEC	LPC I/F COM Port Decode Ranges	00h	R/W
E1h	LPCFDD_DEC	LPC I/F FDD & LPT Decode Ranges	00h	R/W
E2h	SND_DEC	LPC I/F Sound Decode Ranges	00h	R/W
E3h	FWH_DEC_EN1	FWH Decode Enable 1	FFh	R/W
E4–E5h	GEN1_DEC	LPC I/F General 1 Decode Range	0000h	R/W
E6–E7h	LPC_EN	LPC I/F Enables	00h	R/W
E8–EBh	FWH_SEL1	FWH Select 1	00112233h	R/W
EC–EDh	GEN2_DEC	LPC I/F General 2 Decode Range	0000h	R/W
EE–EFh	FWH_SEL2	FWH Select 2	5678h	R/W
F0h	FWH_DEC_EN2	FWH Decode Enable 2	0Fh	R/W
F2h	FUNC_DIS	Function Disable	00h	R/W

NOTE 1: Refer to the Specification Update for the Revision ID.

9.1.1 VID—Vendor ID Register (LPC I/F—D31:F0)

Offset Address: 00–01h
Default Value: 8086h
Lockable: No
Attribute: RO
Size: 16-bit
Power Well: Core

Bit	Description
15:0	**Vendor Identification Value.** This is a 16 bit value assigned to Intel. Intel VID = 8086h.

9.1.2 DID—Device ID Register (LPC I/F—D31:F0)

Offset Address: 02–03h
Default Value: 2480h
Lockable: No
Attribute: RO
Size: 16-bit
Power Well: Core

Bit	Description
15:0	**Device Identification Value.** This is a 16 bit value assigned to the ICH3 LPC Bridge.

9.1.3 PCICMD—PCI COMMAND Register (LPC I/F—D31:F0)

Offset Address:	04–05h	Attribute:	R/W
Default Value:	000Fh	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN)**—R/W. 0 = Disable. 1 **=** Enable. Allow SERR# to be generated.0 =
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	**Parity Error Response (PER)**—R/W. 0 = No action is taken when detecting a parity error 1 = The ICH will take normal action when a parity error is detected. .
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—Hardwired to 1.
2	Bus Master Enable (BME)—RO. Hardwired to 1 to indicate that bus mastering can not be disabled for function 0 (DMA/ISA Master).
1	Memory Space Enable (MSE)—RO. Hardwired to 1 to indicate that memory space can not be disabled for Function 0 (LPC I/F).
0	I/O Space Enable (IOE)—RO. Hardwired to 1 to indicate that the I/O space cannot be disabled for function 0 (LPC I/F).

9.1.4 PCISTA—PCI Device Status Register (LPC I/F—D31:F0)

Offset Address:	06–07h	Attribute:	R/WC
Default Value:	0280h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15	**Detected Parity Error (DPE)**— R/W. 0 = This bit is cleared by software writing a 1 to the bit position. 1 = PERR# signal goes active. Set even if the PER bit is 0.
14	**Signaled System Error (SSE)**—R/W. 0 = This bit is cleared by software writing a 1 to the bit position. 1 = Set by the ICH3 if the SERR_EN bit is set and the ICH3 generates an SERR# on function 0. The ERR_STS register can be read to determine the cause of the SERR#. The SERR# can be routed to cause SMI#, NMI, or interrupt.
13	**Master Abort Status (MAS)**—R/W. 0 = This bit is cleared by software writing a 1 to the bit position. 1 = ICH3 generated a master abort on PCI due to LPC I/F master or DMA cycles.
12	**Received Target Abort (RTA)**—R/W. 0 = This bit is cleared by software writing a 1 to the bit position. 1 = ICH3 received a target abort during LPC I/F master or DMA cycles to PCI.
11	**Signaled Target Abort (STA)**—R/W. This bit is cleared by software writing a 1 to the bit position. 1 = ICH3 generated a target abort condition on PCI cycles claimed by the ICH3 for ICH3 internal registers or for going to LPC I/F.
10:9	**DEVSEL# Timing Status (DEV_STS)**—RO. 01 = Medium Timing.
8	**Data Parity Error Detected (DPED)**—R/WC. 0 = This bit is cleared by software writing a 1 to the bit position. 1 = Set when all three of the following conditions are true: - The ICH3 is the initiator of the cycle, - The ICH3 asserted PERR# (for reads) or observed PERR# (for writes), and - The PER bit is set.
7	Fast Back to Back (FB2B)—RO. Always 1. Indicates ICH3 as a target can accept fast back-to-back transactions.
6	User Definable Features (UDF). Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0.
4:0	Reserved.

9.1.5 REVID—Revision ID Register (LPC I/F—D31:F0)

Offset Address:	08h	Attribute:	RO
Default Value:	See Note	Size:	8 bits

Bit	Description
7:0	Revision Identification Value—RO. 8-bit value that indicates the revision number for the LPC bridge.

NOTE: Refer to the Specification Update for the Revision ID.

9.1.6 PI—Programming Interface Register (LPC I/F—D31:F0)

Offset Address: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Programming Interface Value—RO.

9.1.7 SCC—Sub Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Ah Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	Sub Class Code. 8-bit value that indicates the category of bridge for the LPC PCI bridge.

9.1.8 BCC—Base Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Bh Attribute: RO
Default Value: 06h Size: 8 bits

Bit	Description
7:0	Base Class Code—RO. 8-bit value that indicates the type of device for the LPC bridge. The code is 06h indicating a bridge device.

9.1.9 HEADTYP—Header Type Register (LPC I/F—D31:F0)

Offset Address: 0Eh Attribute: RO
Default Value: 80h Size: 8 bits

Bit	Description
7	Multi-Function Device—RO. This bit is 1 to indicate a multi-function device.
6:0	Header Type—RO. 8-bit field identifies the header layout of the configuration space.

9.1.10 PMBASE—ACPI Base Address Register (LPC I/F—D31:F0)

Offset Address:	40–43h	Attribute:	R/W
Default Value:	00000001h	Size:	32-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Sets base address for ACPI I/O registers, GPIO registers and TCO I/O registers. Can be mapped anywhere in the 64 KB I/O space on 128-byte boundaries.

Bit	Description
31:16	Reserved.
15:7	**Base Address**—R/W. Provides 128 bytes of I/O space for ACPI, GPIO, and TCO logic. This is placed on a 128-byte boundary.
6:1	Reserved.
0	**Resource Indicator**—RO. Tied to 1 to indicate I/O space.

9.1.11 ACPI_CNTL—ACPI Control Register (LPC I/F—D31:F0)

Offset Address:	44h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Bit	Description
7:5	Reserved.
4	**ACPI Enable (ACPI_EN)**—R/W. 0 = Disable. 1 = Decode of the I/O range pointed to by the ACPI base register is enabled, and the ACPI power management function is enabled. Note that the APM power management ranges (B2/B3h) are always enabled and are not affected by this bit.
3	Reserved.
2:0	**SCI IRQ Select (SCI_IRQ_SEL)**—R/W. Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ9–11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. **Bits SCI Map** 000 IRQ9 001 IRQ10 010 IRQ11 011 Reserved 100 IRQ20 (Only available if APIC enabled) 101 IRQ21 (Only available if APIC enabled) 110 IRQ22 (Only available if APIC enabled) 111 IRQ23 (Only available if APIC enabled) **NOTE:** When the TCO interrupt is mapped to APIC interrupts 9, 10 or 11, the signal is in fact active high. When the TCO interrupt is mapped to IRQ 20, 21, 22, or 23, the signal is active low and can be shared with PCI interrupts that may be mapped to those same signals (IRQs).

9.1.12 BIOS_CNTL Register (LPC I/F—D31:F0)

Offset Address:	4E–4Fh	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:2	Reserved.
1	**BIOS Lock Enable (BLE)**—R/W. 0 = Setting the BIOSWE will not cause SMIs. Once set, this bit can only be cleared by a PCIRST#. 1 = Enables setting the BIOSWE bit to cause SMIs.
0	**BIOS Write Enable (BIOSWE)**—R/W. 0 = Only read cycles result in FWH I/F cycles. 1 = Access to the BIOS space is enabled for both read and write cycles. When this bit is written from a 0 to a 1 and BIOS lock Enable (BLE) is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

9.1.13 TCO_CNTL—TCO Control Register (LPC I/F—D31:F0)

Offset Address:	54h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved.
3	**TCO Interrupt Enable (TCO_INT_EN)**—R/W. This bit enables/disables the TCO interrupt. 0 = Disables TCO interrupt. 1 = Enables TCO Interrupt, as selected by the TCO_INT_SEL field.
2:0	**TCO Interrupt Select (TCO_INT_SEL)**—R/W. Specifies on which IRQ the TCO will internally appear. If not using the APIC, the TCO interrupt must be routed to IRQ9-11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the TCO interrupt can also be mapped to IRQ20–23, and can be shared with other interrupt. Note that if the TCOSCI_EN bit is set (bit 6 of the GPEO_EN register), then the TCO interrupt will be sent to the same interrupt as the SCI, and the TCO_INT_SEL bits will have no meaning. When the TCO interrupt is mapped to APIC interrupts 9, 10 or 11, the signal is in fact active high. When the TCO interrupt is mapped to IRQ 20, 21, 22, or 23, the signal is active low and can be shared with PCI interrupts that may be mapped to those same signals (IRQs). **Bits** — **SCI Map** 000 — IRQ9 001 — IRQ10 010 — IRQ11 011 — Reserved 100 — IRQ20 (Only available if APIC enabled) 101 — IRQ21 (Only available if APIC enabled) 110 — IRQ22 (Only available if APIC enabled) 111 — IRQ23 (Only available if APIC enabled)

9.1.14 GPIOBASE—GPIO Base Address Register (LPC I/F—D31:F0)

Offset Address:	58h–5Bh	Attribute:	R/W
Default Value:	00000001h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:16	Reserved.
15:6	**Base Address**—R/W. Provides the 64 bytes of I/O space for GPIO.
5:1	Reserved.
0	**Resource Indicator**—RO. Tied to 1 to indicate I/O space.

9.1.15 GPIO_CNTL—GPIO Control Register (LPC I/F—D31:F0)

Offset Address:	5Ch	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Reserved.
4	**GPIO Enable (GPIO_EN)**—R/W. This bit enables/disables decode of the I/O range pointed to by the GPIO base register and enables/disables the GPIO function. 0 = Disable. 1 = Enable.
3:0	Reserved.

9.1.16 PIRQ[n]_ROUT—PIRQ[A,B,C,D] Routing Control Register (LPC I/F—D31:F0)

Offset Address:	PIRQA–60h, PIRQB–61h, PIRQC–62h, PIRQD–63h	Attribute:	R/W
Default Value:	80h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN)**—R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. **NOTE:** BIOS must program this bit to “0” during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved.
3:0	**IRQ Routing**—R/W. (ISA compatible) 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = IRQ3 0100 = IRQ4 0101 = IRQ5 0110 = IRQ6 0111 = IRQ7 1000 = Reserved 1001 = IRQ9 1010 = IRQ10 1011 = IRQ11 1100 = IRQ12 1101 = Reserved 1110 = IRQ14 1111 = IRQ15

9.1.17 SERIRQ_CNTL—Serial IRQ Control Register (LPC I/F—D31:F0)

Offset Address:	64h	Attribute:	R/W
Default Value:	10h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Serial IRQ Enable (SIRQEN)**—R/W. 0 = The buffer is input only and internally SERIRQ will be a 1. 1 = Serial IRQs will be recognized. The SERIRQ pin will be configured as SERIRQ.
6	Serial IRQ Mode Select (SIRQMD)—R/W. For systems using Quiet Mode, this bit should be set to 1 (Continuous Mode) for at least one frame after coming out of reset before switching back to Quiet Mode. Failure to do so will result in the ICH3 not recognizing SERIRQ interrupts. 0 = The serial IRQ machine will be in quiet mode. 1 = The serial IRQ machine will be in continuous mode.
5:2	**Serial IRQ Frame Size (SIRQSZ)**—R/W. Fixed field that indicates the size of the SERIRQ frame. In the ICH3, this field needs to be programmed to 21 frames (0100). This is an offset from a base of 17 which is the smallest data frame size.
1:0	**Start Frame Pulse Width (SFPW)**—R/W. This is the number of PCI clocks that the SERIRQ pin will be driven low by the serial IRQ machine to signal a start frame. In continuous mode, the ICH3 will drive the start frame for the number of clocks specified. In quiet mode, the ICH3 will drive the start frame for the number of clocks specified minus one, as the first clock was driven by the peripheral. 00 = 4 clocks 01 = 6 clocks 10 = 8 clocks 11 = Reserved

9.1.18 PIRQ[n]_ROUT—PIRQ[E,F,G,H] Routing Control Register (LPC I/F—D31:F0)

Offset Address:	PIRQE–68h, PIRQF–69h, PIRQG–6Ah, PIRQH–6Bh	Attribute:	R/W
Default Value:	80h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN)**—R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. **NOTE:** BIOS must program this bit to “0” during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved.
3:0	**IRQ Routing**—R/W (ISA compatible). 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = IRQ3 0100 = IRQ4 0101 = IRQ5 0110 = IRQ6 0111 = IRQ7 1000 = Reserved 1001 = IRQ9 1010 = IRQ10 1011 = IRQ11 1100 = IRQ12 1101 = Reserved 1110 = IRQ14 1111 = IRQ15

9.1.19 D31_ERR_CFG—Device 31 Error Configuration Register (LPC I/F—D31:F0)

Offset Address:	88h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

This register configures the ICH3’s Device 31 responses to various system errors. The actual assertion of SERR# is enabled via the PCI Command register

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Bit	Description
7:3	Reserved.
2	**SERR# on Received Target Abort Enable (SERR_RTA_EN)**—R/W. 0 = Disable. No SERR# assertion on Received Target Abort. 1 = The ICH3 will generate SERR# when SERR_RTA is set if SERR_EN is set.
1	**SERR# on Delayed Transaction Timeout Enable (SERR_DTT_EN)**—R/W. 0 = Disable. No SERR# assertion on Delayed Transaction Timeout. 1 = The ICH3 will generate SERR# when SERR_DTT bit is set if SERR_EN is set.
0	Reserved.

9.1.20 D31_ERR_STS—Device 31 Error Status Register (LPC I/F—D31:F0)

Offset Address:	8Ah	Attribute:	R/WC
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

This register configures the ICH3's Device 31 responses to various system errors. The actual assertion of SERR# is enabled via the PCI Command register.

Bit	Description
7:3	Reserved.
2	**SERR# Due to Received Target Abort (SERR_RTA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = The ICH3 sets this bit when it receives a target abort. If SERR_EN, the ICH3 will also generate an SERR# when SERR_RTA is set.
1	**SERR# Due to Delayed Transaction Timeout (SERR_DTT)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = When a PCI master does not return for the data within 1 ms of the cycle's completion, the ICH3 clears the delayed transaction and sets this bit. If both SERR_DTT_EN and SERR_EN are set, then ICH3 will also generate an SERR# when SERR_DTT is set.
0	Reserved.

9.1.21 PCI_DMA_CFG—PCI DMA Configuration Register (LPC I/F—D31:F0)

Offset Address:	90h–91h	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:14	**Channel 7 Select**—R/W. 00 = Reserved 01 = PC/PCI DMA 10 = Reserved 11 = LPC I/F DMA
13:12	**Channel 6 Select**—R/W. Same bit decode as for Channel 7.
11:10	**Channel 5 Select**—R/W. Same bit decode as for Channel 7.
9:8	Reserved.
7:6	**Channel 3 Select**—R/W. Same bit decode as for Channel 7.
5:4	**Channel 2 Select**—R/W. Same bit decode as for Channel 7.
3:2	**Channel 1 Select**—R/W. Same bit decode as for Channel 7.
1:0	**Channel 0 Select**—R/W. Same bit decode as for Channel 7.

9.1.22 GEN_CNTL—General Control Register (LPC I/F—D31:F0)

Offset Address:	D0h–D3h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:26	Reserved.
25	**REQ[5]#/GNT[5]# PC/PCI Protocol Select (PCPCIB_SEL)**—R/W. 0 = The REQ[5]#/GNT[5]# pins will function as a standard PCI REQ/GNT signal pair. 1 = When this bit is set to a 1, the PCI REQ[5]#/GNT[5]# signal pair will use the PC/PCI protocol as REQ[B]#/GNT[B]. The corresponding bits in the GPIO_USE_SEL register must also be set to a 0. If the corresponding bits in the GPIO_USE_SEL register are set to a 1, then the signals will be used as a GPI and GPO.
24	**Hide ISA Bridge (HIDE_ISA)**—R/W. The ICH3 will not prevent AD22 from asserting during configuration cycles to the PCI-to-ISA bridge. 1 = Software sets this bit to 1 to disable configuration cycle from being claimed by a PCI-to-ISA bridge. This will prevent the OS PCI PnP from getting confused by seeing two ISA bridges. It is required for the ICH3 PCI address line AD22 to connect to the PCI-to-ISA bridge's IDSEL input. When this bit is set, the ICH3 will not assert AD22 during configuration cycles to the PCI-to-ISA bridge.
23: 22	Reserved.
21	**Processor Break Event Indication Enable (FERR#-MUX-EN)**—R/W. 0 = (Default) The ICH3 will not examine the FERR# signal during C2. 1 = Software sets this bit to 1 to enable the ICH3 to examine the FERR# signal during a C2 state as a break event. (see Section 6.12.6 for details).
20:14	Reserved.
13	**Coprocessor Error Enable (COPR_ERR_EN)**—R/W. 0 = FERR# will not generate IRQ13 nor IGNNE#. 1 = When FERR# is low, ICH3 generates IRQ13 internally and holds it until an I/O write to port F0h. It will also drive IGNNE# active.
12	**Keyboard IRQ1 Latch Enable (IRQ1LEN)**—R/W. 0 = IRQ1 will bypass the latch. 1 = The active edge of IRQ1 will be latched and held until a port 60h read.
11	**Mouse IRQ12 Latch Enable (IRQ12LEN)**—R/W. 0 = IRQ12 will bypass the latch. 1 = The active edge of IRQ12 will be latched and held until a port 60h read.
10:9	Reserved.
8	**APIC Enable (APIC_EN)**—R/W. 0 = Disables internal I/O (x) APIC. 1 = Enables the internal I/O (x) APIC and its address decode. The following behavioral rules apply for bits 8 and 7 in this register: **Rule 1:** If bit 8 is 0, then the ICH3 will not decode any of the registers associated with the I/O APIC or I/O (x) APIC. The state of bit 7 is "Don't Care" in this case. **Rule 2:** If bit 8 is 1 and bit 7 is 0, then the ICH3 will decode the memory space associated with the I/O APIC, but not the extra registers associated I/O (x) APIC. **Rule 3:** If bit 8 is 1 and bit 7 is 1, then the ICH3 will decode the memory space associated with both the I/O APIC and the I/O (x) APIC. This also enables PCI masters to write directly to the register to cause interrupts (PCI Message Interrupt). **NOTE:** There is no separate way to disable PCI Message Interrupts if the I/O (x) APIC is enabled. This is not considered necessary.

Bit	Description
7	**Enables I/O (x) Extension Enable (XAPIC_EN)**—R/W. 0 = The I/O (x) APIC extensions are not supported. 1 = Enables the extra features (beyond standard I/O APIC) associated with the I/O (x) APIC. **NOTE:** This bit is only valid if the APIC_EN bit is also set to 1.
6	**Alternate Access Mode Enable (ALTACC_EN)**—R/W. 0 = ALT Access Mode Disabled (default). Alt Access Mode allows reads to otherwise unreadable registers and writes otherwise unwritable registers. 1 = ALT Access Mode Enable.
5:3	Reserved.
2	**DMA Collection Buffer Enable (DCB_EN)**— R/W. 0 = DCB disabled. 1 = Enables DMA Collection Buffer (DCB) for LPC I/F and PC/PCI DMA.
1	**Delayed Transaction Enable (DTE)**—R/W. 0 = Delayed transactions disabled. 1 = ICH3 enables delayed transactions for internal register, FWH and LPC I/F accesses.
0	**Positive Decode Enable (POS_DEC_EN)**—R/W. 0 = The ICH3 will perform subtractive decode on the PCI bus and forward the cycles to LPC I/F if not to an internal register or other known target on LPC I/F. Accesses to internal registers and to known LPC I/F devices will still be positively decoded. 1 = Enables ICH3 to only perform positive decode on the PCI bus.

9.1.23 GEN_STA—General Status Register (LPC I/F—D31:F0)

Offset Address:	D4h– D7h	Attribute:	R/W
Default Value:	00000F0Xh (upon RTCRST# assertion low) 00002F0Xh (if Safe Mode Strap is active)	Size:	32-bit
Lockable:	No	Power Well:	Core(0:7), RTC (8:15)

Bit	Description
31:14	Reserved.
13	**TOP_SWAP**—R/W. 0 = ICH3 will not invert A16. This bit is cleared by RTCRST# assertion, but not by any other type of reset. 1 = ICH3 will invert A16 for cycles targeting FWH BIOS space (Does not affect accesses to FWH feature space).
12	**Enables Processor BIST (CPU_BIST_EN)**—R/W. 0 = Disable. 1 = The INIT# signal will be driven active when CPURST# is active. INIT# will go inactive with the same timings as the other Processor I/F signals (Hold Time after CPURST# inactive). Note that CPURST# is generated by the memory controller hub, but the ICH3 has a hub interface special cycle that allows the ICH3 to control the assertion/deassertion of CPURST#.
11:8	**Processor Frequency Strap (FREQ_STRAP[3:0])**—R/W. These bits determine the internal frequency multiplier of the processor. These bits can be reset to 1111 based on an external pin strap or via the RTCRST# input signal. Software must program this field based on the processor's specified frequency. Note that this field is only writable when the SAFE_MODE bit is cleared to zero, and SAFE_MODE is only cleared by PWROK rising edge. These bits are in the RTC well.
7:3	Reserved.
2	**SAFE_MODE**—RO. 0 = ICH3 sampled AC_SDOUT low on the rising edge of PWROK. 1 = ICH3 sampled AC_SDOUT high on the rising edge of PWROK. ICH3 will force FREQ_STRAP[3:0] bits to all 1s (safe mode multiplier).
1	**NO_REBOOT**—R/W (special). 0 = Normal TCO Timer reboot functionality (reboot after 2nd TCO timeout). This bit can not be set to 0 by software if the strap is set to No Reboot. 1 = ICH3 will disable the TCO Timer system reboot feature. This bit is set either by hardware when SPKR is sampled high on the rising edge of PWROK, or by software writing a 1 to the bit.
0	Reserved.

9.1.24 RTC_CONF—RTC Configuration Register (LPC I/F—D31:F0)

Offset Address:	D8h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	Yes	Power Well:	Core

Bit	Description
7:5	Reserved.
4	**Upper 128-byte Lock (U128LOCK)**—R/W (special). 0 = Access to these bytes in the upper CMOS RAM range have not been locked. 1 = Locks reads and writes to bytes 38h–3Fh in the upper 128-byte bank of the RTC CMOS RAM. Write cycles to this range will have no effect and read cycles will not return any particular guaranteed value. This is a write once register that can only be reset by a hardware reset.
3	**Lower 128-byte Lock (L128LOCK)**—R/W (special). 0 = Access to these bytes in the lower CMOS RAM range have not been locked. 1 = Locks reads and writes to bytes 38h–3Fh in the lower 128-byte bank of the RTC CMOS RAM. Write cycles to this range will have no effect and read cycles will not return any particular guaranteed value. This is a write once register that can only be reset by a hardware reset.
2	**Upper 128-byte Enable (U128E)**—R/W. 0 = Disable. 1 = Enables access to the upper 128-byte bank of RTC CMOS RAM.
1:0	Reserved.

9.1.25 COM_DEC—LPC I/F Communication Port Decode Ranges Register (LPC I/F—D31:F0)

Offset Address:	E0h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7	Reserved.
6:4	**COMB Decode Range**—R/W. This field determines which range to decode for the COMB Port. **Bits** — **Decode Range** 000 — 3F8h–3FFh (COM1) 001 — 2F8h–2FFh (COM2) 010 — 220h–227h 011 — 228h–22Fh 100 — 238h–23Fh 101 — 2E8h–2EFh (COM4) 110 — 338h–33Fh 111 — 3E8h–3EFh (COM3)
3	Reserved.
2:0	**COMA Decode Range**—R/W. This field determines which range to decode for the COMA Port. **Bits** — **Decode Range** 000 — 3F8h–3FFh (COM1) 001 — 2F8h–2FFh (COM2) 010 — 220h–227h 011 — 228h–22Fh 100 — 238h–23Fh 101 — 2E8h–2EFh (COM4) 110 — 338h–33Fh 111 — 3E8h–3EFh (COM3)

9.1.26 FDD/LPT_DEC—LPC I/F FDD & LPT Decode Ranges Register (LPC I/F—D31:F0)

Offset Address:	E1h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Reserved.
4	**FDD Decode Range**—R/W. Determines which range to decode for the FDD Port 0 = 3F0h–3F5h, 3F7h (Primary) 1 = 370h–2FFh (Secondary)
3:2	Reserved.
1:0	**LPT Decode Range**—R/W. This field determines which range to decode for the LPTPort. 00 = 378h–37Fh and 778h–77Fh 01 = 278h–27Fh (port 279h is read only) and 678h–67Fh 10 = 3BCh–3BEh and 7BCh–7BEh 11 = Reserved

9.1.27 SND_DEC—LPC I/F Sound Decode Ranges Register (LPC I/F—D31:F0)

Offset Address:	E2h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:6	Reserved.
5:4	**MSS Decode Range**—R/W. This field determines which range to decode for the Microsoft Sound System (MSS) 00 = 530h–537h 01 = 604h–60Bh 10 = E80h–E87h 11 = F40h–F47h
3	**MIDI Decode Range**—R/W. This bit determines which range to decode for the Midi Port 0 = 330h–331h 1 = 300h–301h
2	Reserved.
1:0	**SB16 Decode Range**—R/W. This field determines which range to decode for the Sound Blaster 16 (SB16) Port 00 = 220h–233h 01 = 240h–253h 10 = 260h–273h 11 = 280h–293h

9.1.28 FWH_DEC_EN1—FWH Decode Enable 1 Register (LPC I/F—D31:F0)

Offset Address:	E3h	Attribute:	R/W
Default Value:	FFh	Size:	8 bits

This register determines which memory ranges will be decoded on the PCI bus and forwarded to the FWH. The ICH3 will subtractively decode cycles on PCI unless POS_DEC_EN is set to 1.

Bit	Description
7	**FWH_F8_EN**—RO. Enables decoding two 512 KB FWH memory ranges, and one 128 KB memory range. 1 = Enable the following ranges for the FWH FFF80000h–FFFFFFFFh FFB80000h–FFBFFFFFh 000E0000h–000FFFFFh
6	**FWH_F0_EN**—R/W. Enables decoding two 512 KB FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH: FFF00000h–FFF7FFFFh FFB00000h–FFB7FFFFh
5	**FWH_E8_EN**—R/W. Enables decoding two 512 KB FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH: FFE80000h–FFEFFFFFh FFA80000h–FFAFFFFFh
4	**FWH_E0_EN**—R/W. Enables decoding two 512 KB FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH: FFE00000h–FFE7FFFFh FFA00000h–FFA7FFFFh
3	**FWH_D8_EN**—R/W. Enables decoding two 512 KB FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FFD80000h–FFDFFFFFh FF980000h–FF9FFFFFh
2	**FWH_D0_EN**—R/W. Enables decoding two 512 KB FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FFD00000h–FFD7FFFFh FF900000h–FF97FFFFh
1	**FWH_C8_EN**—R/W. Enables decoding two 512 KB FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FFC80000h–FFCFFFFFh FF880000h–FF8FFFFFh
0	**FWH_C0_EN**—R/W. Enables decoding two 512 KB FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FFC00000h–FFC7FFFFh FF800000h–FF87FFFFh

9.1.29 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0)

Offset Address:	E4h–E5h	Attribute:	R/W
Default Value:	00h	Size:	16-bit
Lockable:	Yes	Power Well:	Core

Bit	Description
15:7	**Generic I/O Decode Range 1 Base Address (GEN1_BASE)**—R/W. This address is aligned on a 128-byte boundary, and must have address lines 31:16 as 0. Note that this generic decode is for I/O addresses only, not memory addresses. The size of this range is 128 bytes.
6:1	Reserved.
0	**Generic Decode Range 1 Enable (GEN1_EN)**—R/W. 0 = Disable. 1 = Enable the GEN1 I/O range to be forwarded to the LPC I/F.

9.1.30 LPC_EN—LPC I/F Enables Register (LPC I/F—D31:F0)

Offset Address:	E6h–E7h	Attribute:	R/W
Default Value:	00h	Size:	16-bit
Lockable:	Yes	Power Well:	Core

Bit	Description
15:14	Reserved.
13	**CNF2_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the I/O locations 4Eh and 4Fh to the LPC interface. This range is used for a microcontroller.
12	**CNF1_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the I/O locations 2Eh and 2Fh to the LPC interface. This range is used for Super I/O devices.
11	**MC_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the I/O locations 62h and 66h to the LPC interface. This range is used for a microcontroller.
10	**KBC_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the I/O locations 60h and 64h to the LPC interface. This range is used for a microcontroller.
9	**GAMEH_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the I/O locations 208h to 20Fh to the LPC interface. This range is used for a gameport.
8	**GAMEL_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the I/O locations 200h to 207h to the LPC interface. This range is used for a gameport.

Bit	Description
7	**ADLIB_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the I/O locations 388h–38Bh to the LPC interface.
6	**MSS_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the MSS range to the LPC interface. This range is selected in the LPC_Sound Decode Range Register.
5	**MIDI_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the MIDI range to the LPC interface. This range is selected in the LPC_Sound Decode Range Register.
4	**SB16_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the SB16 range to the LPC interface. This range is selected in the LPC_Sound Decode Range Register.
3	**FDD_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the FDD range to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register.
2	**LPT_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the LPTrange to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register.
1	**COMB_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the COMB range to the LPC interface. This range is selected in the LPC_COM Decode Range Register.
0	**COMA_LPC_EN**—R/W. 0 = Disable. 1 = Enables the decoding of the COMA range to the LPC interface. This range is selected in the LPC_COM Decode Range Register.

9.1.31 FWH_SEL1—FWH Select 1 Register (LPC I/F—D31:F0)

Offset Address: E8h Attribute: R/W
Default Value: 00112233h Size: 32 bits

Bit	Description
31:28	**FWH_F8_IDSEL**—RO. IDSEL for two 512 KB FWH memory ranges and one 128 KB memory range. This field is fixed at 0000. The IDSEL programmed in this field addresses the following memory ranges: FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh 000E 0000h–000F FFFFh
27:24	**FWH_F0_IDSEL**—R/W. IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFF0 0000h–FFF7 FFFFh FFB0 0000h–FFB7 FFFFh
23:20	**FWH_E8_IDSEL**—R/W. IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE8 0000h–FFEF FFFFh FFA8 0000h–FFAF FFFFh
19:16	**FWH_E0_IDSEL**—R/W. IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE0 0000h–FFE7 FFFFh FFA0 0000h–FFA7 FFFFh
15:12	**FWH_D8_IDSEL**—R/W. IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD8 0000h–FFDF FFFFh FF98 0000h–FF9F FFFFh
11:8	**FWH_D0_IDSEL**—R/W. IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD0 0000h–FFD7 FFFFh FF90 0000h–FF97 FFFFh
7:4	**FWH_C8_IDSEL**—R/W. IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC8 0000h–FFCF FFFFh FF88 0000h–FF8F FFFFh
3:0	**FWH_C0_IDSEL**—R/W. IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC0 0000h–FFC7 FFFFh FF80 0000h–FF87 FFFFh

9.1.32 GEN2_DEC—LPC I/F Generic Decode Range 2 Register (LPC I/F—D31:F0)

Offset Address:	ECh–EDh	Attribute:	R/W
Default Value:	00h	Size:	16-bit
Lockable:	Yes	Power Well:	Core

Bit	Description
15:4	**Generic I/O Decode Range 2 Base Address (GEN2_BASE)**—R/W. This address is aligned on a 64-byte boundary, and must have address lines 31:16 as 0. Note that this generic decode is for I/O addresses only, not memory addresses. The size of this range is 16 bytes.
3:1	Reserved. Read as 0.
0	**Generic I/O Decode Range 2 Enable (GEN2_EN)**—R/W. 0 = Disable. 1 = Accesses to the GEN2 I/O range will be forwarded to the LPC I/F.

9.1.33 FWH_SEL2—FWH Select 2 Register (LPC I/F—D31:F0)

Offset Address:	EEh–EFh	Attribute:	R/W
Default Value:	4567h	Size:	32 bits

Bit	Description
15:12	**FWH_70_IDSEL**—R/W. IDSEL for two 1M FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF70 0000h—FF7F FFFFh FF30 0000h—FF3F FFFFh
11:8	**FWH_60_IDSEL**—R/W. IDSEL for two 1M FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF60 0000h—FF6F FFFFh FF20 0000h—FF2F FFFFh
7:4	**FWH_50_IDSEL**—R/W. IDSEL for two 1M FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF50 0000h—FF5F FFFFh FF10 0000h—FF1F FFFFh
3:0	**FWH_40_IDSEL**—R/W. IDSEL for two 1M FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF40 0000h—FF4F FFFFh FF00 0000h—FF0F FFFFh

9.1.34 FWH_DEC_EN2—FWH Decode Enable 2 Register (LPC I/F—D31:F0)

Offset Address:	F0h	Attribute:	R/W
Default Value:	0Fh	Size:	8 bits

This register determines which memory ranges will be decoded on the PCI bus and forwarded to the FWH. The ICH3 will subtractively decode cycles on PCI unless POS_DEC_EN is set to 1.

Bit	Description
7:4	Reserved.
3	**FWH_70_EN**—R/W. Enables decoding two 1M FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FF70 0000h—FF7F FFFFh FF30 0000h—FF3F FFFFh
2	**FWH_60_EN**—R/W. Enables decoding two 1M FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FF60 0000h—FF6F FFFFh FF20 0000h—FF2F FFFFh
1	**FWH_50_EN**—R/W. Enables decoding two 1M FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FF50 0000h—FF5F FFFFh FF10 0000h—FF1F FFFFh
0	**FWH_40_EN**—R/W. Enables decoding two 1M FWH memory ranges. 0 = Disable. 1 = Enable the following ranges for the FWH FF40 0000h—FF4F FFFFh FF00 0000h—FF0F FFFFh

9.1.35 FUNC_DIS—Function Disable Register (LPC I/F—D31:F0)

Offset Address:	F2h	Attribute:	R/W
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:11	Reserved.
10	**D29_F2_Disable**—R/W. Software sets this bit to disable the USB 1.1 Controller #3 function. BIOS must not enable I/O or memory address space decode, interrupt generation, or any other functionality of functions that are to be disabled. 0 = USB 1.1 Controller #3 is enabled. 1 = USB 1.1 Controller #3 is disabled.
9	**D29_F1_Disable**—R/W. Software sets this bit to disable the USB 1.1 Controller #2 function. BIOS must not enable I/O or memory address space decode, interrupt generation, or any other functionality of functions that are to be disabled. 0 = USB 1.1 Controller #2 is enabled. 1 = USB 1.1 Controller #2 is disabled.
8	**D29_F0_Disable**—R/W. Software sets this bit to disable the USB 1.1 Controller #1 function.BIOS must not enable I/O or memory address space decode, interrupt generation, or any other functionality of functions that are to be disabled. 0 = USB 1.1 Controller #1 is enabled. 1 = USB 1.1 Controller #1 is disabled.
7	Reserved.
6	**D31_F6_Disable**—R/W. Software sets this bit to disable the AC'97 modem controller function. BIOS must not enable I/O or memory address space decode, interrupt generation, or any other functionality of functions that are to be disabled. 0 = AC'97 Modem is enabled. 1 = AC'97 Modem is disabled.
5	**D31_F5_Disable**—R/W. Software sets this bit to disable the AC'97 audio controller function. BIOS must not enable I/O or memory address space decode, interrupt generation, or any other functionality of functions that are to be disabled. 0 = AC'97 audio controller is enabled. 1 = AC'97 audio controller is disabled.
4	Reserved.
3	**D31_F3_Disable**—R/W. Software sets this bit to disable the SMBus Host Controller function. BIOS must not enable I/O or memory address space decode, interrupt generation, or any other functionality of functions that are to be disabled. 0 = SMBus controller is enabled. 1 = SMBus controller is disabled.
2	Reserved.
1	**D31_F1_Disable**—R/W. Software sets this bit to disable the IDE controller function. BIOS must not enable I/O or memory address space decode, interrupt generation, or any other functionality of functions that are to be disabled. 0 = IDE controller is enabled. 1 = IDE controller is disabled.
0	**SMB_FOR_BIOS**—R/W. This bit is used in conjunction with bit 3 in this register. 0 = No effect. 1 = Allows the SMBus I/O space to be accessible by software when bit 3 in this register is set. The PCI configuration space is hidden in this case. Note that if bit 3 is set alone, the decode of both SMBus PCI configuration and I/O space will be disabled.

NOTE: Software must always disable all functionality within the function before disabling the configuration space

9.2 DMA I/O Registers

Table 9-2. DMA Registers

Port	Alias	Register Name	Default	Type
00h	10h	Channel 0 DMA Base & Current Address	Undefined	R/W
01h	11h	Channel 0 DMA Base & Current Count	Undefined	R/W
02h	12h	Channel 1 DMA Base & Current Address	Undefined	R/W
03h	13h	Channel 1 DMA Base & Current Count	Undefined	R/W
04h	14h	Channel 2 DMA Base & Current Address	Undefined	R/W
05h	15h	Channel 2 DMA Base & Current Count	Undefined	R/W
06h	16h	Channel 3 DMA Base & Current Address	Undefined	R/W
07h	17h	Channel 3 DMA Base & Current Count	Undefined	R/W
08h	18h	Channel 0–3 DMA Command	Undefined	WO
		Channel 0–3 DMA Status	Undefined	RO
0Ah	1Ah	Channel 0–3 DMA Write Single Mask	000001XXb	WO
0Bh	1Bh	Channel 0–3 DMA Channel Mode	000000XXb	WO
0Ch	1Ch	Channel 0–3 DMA Clear Byte Pointer	Undefined	WO
0Dh	1Dh	Channel 0–3 DMA Master Clear	Undefined	WO
0Eh	1Eh	Channel 0–3 DMA Clear Mask	Undefined	WO
0Fh	1Fh	Channel 0–3 DMA Write All Mask	0Fh	R/W
80h	90h	Reserved Page	Undefined	R/W
81h	91h	Channel 2 DMA Memory Low Page	Undefined	R/W
82h	–	Channel 3 DMA Memory Low Page	Undefined	R/W
83h	93h	Channel 1 DMA Memory Low Page	Undefined	R/W
84h–86h	94h–96h	Reserved Page s	Undefined	R/W
87h	97h	Channel 0 DMA Memory Low Page	Undefined	R/W
88h	98h	Reserved Page	Undefined	R/W
89h	99h	Channel 6 DMA Memory Low Page	Undefined	R/W
8Ah	9Ah	Channel 7 DMA Memory Low Page	Undefined	R/W
8Bh	9Bh	Channel 5 DMA Memory Low Page	Undefined	R/W
8Ch–8Eh	9Ch–9Eh	Reserved Page s	Undefined	R/W
8Fh	9Fh	Refresh Low Page	Undefined	R/W
C0h	C1h	Channel 4 DMA Base & Current Address	Undefined	R/W
C2h	C3h	Channel 4 DMA Base & Current Count	Undefined	R/W
C4h	C5h	Channel 5 DMA Base & Current Address	Undefined	R/W
C6h	C7h	Channel 5 DMA Base & Current Count	Undefined	R/W
C8h	C9h	Channel 6 DMA Base & Current Address	Undefined	R/W
CAh	CBh	Channel 6 DMA Base & Current Count	Undefined	R/W
CCh	CDh	Channel 7 DMA Base & Current Address	Undefined	R/W
CEh	CFh	Channel 7 DMA Base & Current Count	Undefined	R/W

Table 9-2. DMA Registers (Continued)

Port	Alias	Register Name	Default	Type
D0h	D1h	Channel 4–7 DMA Command	Undefined	WO
		Channel 4–7 DMA Status	Undefined	RO
D4h	D5h	Channel 4–7 DMA Write Single Mask	000001XXb	WO
D6h	D7h	Channel 4–7 DMA Channel Mode	000000XXb	WO
D8h	D9h	Channel 4–7 DMA Clear Byte Pointer	Undefined	WO
DAh	DBh	Channel 4–7 DMA Master Clear	Undefined	WO
DCh	DDh	Channel 4–7 DMA Clear Mask	Undefined	WO
DEh	DFh	Channel 4–7 DMA Write All Mask	0Fh	R/W

9.2.1 DMABASE_CA—DMA Base and Current Address Registers

I/O Address:	Ch. #0 = 00h; Ch. #1 = 02h Ch. #2 = 04h; Ch. #3 = 06h Ch. #5 = C4h Ch. #6 = C8h Ch. #7 = CCh;	Attribute:	RO
Default Value:	Undef	Size:	16-bit (per channel), but accessed in two 8-bit quantities
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Base and Current Address**—R/W. This register determines the address for the transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the *Base Address* register and copied to the *Current Address* register. On reads, the value is returned from the *Current Address* register. The address increments/decrements in the Current Address register after each transfer, depending on the mode of the transfer. If the channel is in auto-initialize mode, the Current Address register will be reloaded from the Base Address register after a terminal count is generated. For transfers to/from a 16-bit slave (channels 5–7), the address is shifted left one bit location. Bit 15 will be shifted out. Therefore, if bit 15 was a 1, it will be lost. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing an address register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first.

9.2.2 DMABASE_CC—DMA Base and Current Count Registers

I/O Address:	Ch. 0: = 01h; Ch. #1 = 03h Ch. 2: = 05h; Ch. #3 = 07h Ch. 5 = C6h; Ch. #6 = CAh Ch. 7 = CEh;	Attribute:	R/W
Default Value:	Undefined	Size:	16-bit (per channel), but accessed in two 8-bit quantities
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Base and Current Count**—R/W. This register determines the number of transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the Base Count register and copied to the Current Count register. On reads, the value is returned from the Current Count register. The actual number of transfers is one more than the number programmed in the Base Count Register (i.e., programming a count of 4h results in 5 transfers). The count is decrements in the Current Count register after each transfer. When the value in the register rolls from zero to FFFFh, a terminal count is generated. If the channel is in auto-initialize mode, the Current Count register will be reloaded from the Base Count register after a terminal count is generated. For transfers to/from an 8-bit slave (channels 0-3), the count register indicates the number of bytes to be transferred. For transfers to/from a 16-bit slave (channels 5–7), the count register indicates the number of words to be transferred. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing a count register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first.

9.2.3 DMAMEM_LP—DMA Memory Low Page Registers

I/O Address:	Ch. 0 = 87h; Ch. #1 = 83h Ch. 2 = 81h; Ch. #3 = 82h Ch. 5 = 8Bh; Ch. #6 = 89h Ch. 7 = 8Ah;	Attribute:	R/W
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**DMA Low Page (ISA Address Bits [23:16])**—R/W. This register works in conjunction with the DMA controller's Current Address Register to define the complete 24-bit address for the DMA channel. This register remains static throughout the DMA transfer.

9.2.4 DMACMD—DMA Command Register

I/O Address:	Ch. #0–3 = 08h; Ch. #4–7 = D0h	Attribute:	WO
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Reserved. Must be 0.
4	**DMA Group Arbitration Priority**—WO. Each channel group is individually assigned either fixed or rotating arbitration priority. At part reset, each group is initialized in fixed priority. 0 = Fixed priority to the channel group. 1 = Rotating priority to the group.
3	Reserved. Must be 0.
2	**DMA Channel Group Enable**—WO. Both channel groups are enabled following part reset. 0 = Enable the DMA channel group. 1 = Disable. Disabling channel group 4–7 also disables channel group 0–3, which is cascaded through channel 4.
1:0	Reserved. Must be 0.

9.2.5 DMASTA—DMA Status Register

I/O Address:	Ch. #0–3 = 08h; Ch. #4–7 = D0h	Attribute:	RO
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	**Channel Request Status**—RO. When a valid DMA request is pending for a channel, the corresponding bit is set to 1. When a DMA request is not pending for a particular channel, the corresponding bit is set to 0. The source of the DREQ may be hardware or a software request. Note that channel 4 is the cascade channel, so the request status of channel 4 is a logical OR of the request status for channels 0 through 3. 4 = Channel 0 5 = Channel 1 (5) 6 = Channel 2 (6) 7 = Channel 3 (7)
3:0	**Channel Terminal Count Status**—RO. When a channel reaches terminal count (TC), its status bit is set to 1. If TC has not been reached, the status bit is set to 0. Channel 4 is programmed for cascade, so the TC bit response for channel 4 is irrelevant: 0 = Channel 0 1 = Channel 1 (5) 2 = Channel 2 (6) 3 = Channel 3 (7)

9.2.6 DMA_WRSMSK—DMA Write Single Mask Register

I/O Address:	Ch. #0–3 = 0Ah; Ch. #4–7 = D4h	Attribute:	WO
Default Value:	0000 01xx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:3	Reserved. Must be 0.
2	**Channel Mask Select**—WO. 0 = Enable DREQ for the selected channel. The channel is selected through bits [1:0]. Therefore, only one channel can be masked / unmasked at a time. 1 = Disable DREQ for the selected channel.
1:0	**DMA Channel Select**—WO. These bits select the DMA Channel Mode Register to program. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

9.2.7 DMACH_MODE—DMA Channel Mode Register

I/O Address:	Ch. #0–3 = 0Bh; Ch. #4–7 = D6h	Attribute:	WO
Default Value:	0000 00xx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:6	**DMA Transfer Mode**—WO. Each DMA channel can be programmed in one of four different modes: 00 = Demand mode 01 = Single mode 10 = Reserved 11 = Cascade mode
5	**Address Increment/Decrement Select**—WO. This bit controls address increment/decrement during DMA transfers. 0 = Address increment. (default after part reset or Master Clear) 1 = Address decrement.
4	**Autoinitialize Enable**—WO. 0 = Autoinitialize feature is disabled and DMA transfers terminate on a terminal count. A part reset or Master Clear disables autoinitialization. 1 = DMA restores the Base Address and Count registers to the current registers following a terminal count (TC).
3:2	**DMA Transfer Type**—WO. These bits represent the direction of the DMA transfer. When the channel is programmed for cascade mode, (bits[7:6] = “11”) the transfer type is irrelevant. 00 = Verify–No I/O or memory strobes generated 01 = Write–Data transferred from the I/O devices to memory 10 = Read–Data transferred from memory to the I/O device 11 = Illegal
1:0	**DMA Channel Select**—WO. These bits select the DMA Channel Mode Register that will be written by bits [7:2]. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

9.2.8 DMA Clear Byte Pointer Register

I/O Address:	Ch. #0–3 = 0Ch; Ch. #4–7 = D8h	Attribute:	WO
Default Value:	xxxx xxxx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Clear Byte Pointer**—WO. No specific pattern. Command enabled with a write to the I/O port address. Writing to this register initializes the byte pointer flip/flop to a known state. It clears the internal latch used to address the upper or lower byte of the 16-bit Address and Word Count Registers. The latch is also cleared by part reset and by the Master Clear command. This command precedes the first access to a 16 bit DMA controller register. The first access to a 16 bit register will then access the significant byte, and the second access automatically accesses the most significant byte.

9.2.9 DMA Master Clear Register

I/O Address:	Ch. #0–3 = 0Dh; Ch. #4–7 = DAh	Attribute:	WO
Default Value:	xxxx xxxx	Size:	8-bit

Bit	Description
7:0	**Master Clear**—WO. No specific pattern. Enabled with a write to the port. This has the same effect as the hardware Reset. The Command, Status, Request, and Byte Pointer flip/flop registers are cleared and the Mask Register is set.

9.2.10 DMA_CLMSK—DMA Clear Mask Register

I/O Address:	Ch. #0–3 = 0Eh; Ch. #4–7 = DCh	Attribute:	WO
Default Value:	xxxx xxxx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Clear Mask Register**—WO. No specific pattern. Command enabled with a write to the port.

9.2.11 DMA_WRMSK—DMA Write All Mask Register

I/O Address:	Ch. #0–3 = 0Fh; Ch. #4–7 = DEh	Attribute:	R/W
Default Value:	0000 1111	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved. Must be 0.
3:0	**Channel Mask Bits**—R/W. This register permits all four channels to be simultaneously enabled/disabled instead of enabling/disabling each channel individually, as is the case with the Mask Register - Write Single Mask Bit. In addition, this register has a read path to allow the status of the channel mask bits to be read. A channel's mask bit is automatically set to 1 when the Current Byte/Word Count Register reaches terminal count (unless the channel is in auto-initialization mode). Setting the bit(s) to a 1 disables the corresponding DREQ(s). Setting the bit(s) to a 0 enables the corresponding DREQ(s). Bits [3:0] are set to 1 upon part reset or Master Clear. When read, bits [3:0] indicate the DMA channel [3:0] ([7:4]) mask status. Bit 0 = Channel 0 (4) 1 = Masked, 0 = Not Masked Bit 1 = Channel 1 (5) 1 = Masked, 0 = Not Masked Bit 2 = Channel 2 (6) 1 = Masked, 0 = Not Masked Bit 3 = Channel 3 (7) 1 = Masked, 0 = Not Masked **NOTE:** Disabling channel 4 also disables channels 0–3 due to the cascade of channels 0–3 through channel 4.

9.3 Timer I/O Registers

Port	Aliases	Register Name	Default Value	Type
40h	50h	Counter 0 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 0 Counter Access Port	Undefined	R/W
41h	51h	Counter 1 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 1 Counter Access Port	Undefined	R/W
42h	52h	Counter 2 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 2 Counter Access Port	Undefined	R/W
43h	53h	Timer Control Word	Undefined	WO
		Timer Control Word Register Read Back	XXXXXXX0b	WO
		Counter Latch Command	X0h	WO

9.3.1 TCW—Timer Control Word Register

I/O Address: 43h Attribute: WO
Default Value: All bits undefined Size: 8 bits

This register is programmed prior to any counter being accessed to specify counter modes. Following part reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Bit	Description
7:6	**Counter Select**—WO. The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1. 00 = Counter 0 select 01 = Counter 1 select 10 = Counter 2 select 11 = Read Back Command
5:4	**Read/Write Select**—WO. These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2). 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Counter Mode Selection**—WO. These bits select one of six possible modes of operation for the selected counter. 000 = Mode 0Out signal on end of count (=0) 001 = Mode 1Hardware retriggerable one-shot x10 = Mode 2Rate generator (divide by n counter) x11 = Mode 3Square wave output 100 = Mode 4Software triggered strobe 101 = Mode 5Hardware triggered strobe
0	**Binary/BCD Countdown Select**—WO. 0 = Binary countdown is used. The largest possible binary count is 2^{16}. 1 = Binary coded decimal (BCD) count is used. The largest possible BCD count is 10^4.

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined. These register formats are described below.

9.3.1.1 RDBK_CMD—Read Back Command

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read. Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Bit	Description
7:6	**Read Back Command.** Must be “11” to select the Read Back Command.
5	**Latch Count of Selected Counters.** 0 = Current count value of the selected counters will be latched. 1 = Current count will not be latched.
4	**Latch Status of Selected Counters.** 0 = Status of the selected counters will be latched. 1 = Status will not be latched.
3	**Counter 2 Select.** 1 = Counter 2 count and/or status will be latched.
2	**Counter 1 Select.** 1 = Counter 1 count and/or status will be latched.
1	**Counter 0 Select.** 1 = Counter 0 count and/or status will be latched.
0	Reserved. Must be 0.

9.3.1.2 LTCH_CMD—Counter Latch Command

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2). The count must be read according to the programmed format, i.e., if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Bit	Description
7:6	**Counter Selection.** These bits select the counter for latching. If “11” is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Counter 1 10 = Counter 2
5:4	**Counter Latch Command.** 00 = Selects the Counter Latch Command.
3:0	Reserved. Must be 0.

9.3.2 SBYTE_FMT—Interval Timer Status Byte Format Register

I/O Address:	Counter 0 = 40h, Counter 1 = 41h, Counter 2 = 42h	Attribute:	RO
Default Value:	Bits[6:0] undefined, Bit 7=0	Size:	8 bits per counter

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2) returns the status byte. The status byte returns the following:

Bit	Description
7	**Counter OUT Pin State**—RO. 0 = OUT pin of the counter is also a 0. 1 = OUT pin of the counter is also a 1.
6	**Count Register Status**—RO. This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 = Count has been transferred from CR to CE and is available for reading. 1 = Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	**Read/Write Selection Status**—RO. These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Mode Selection Status**—RO. These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 = Mode 0Out signal on end of count (=0) 001 = Mode 1Hardware retriggerable one-shot x10 = Mode 2Rate generator (divide by n counter) x11 = Mode 3Square wave output 100 = Mode 4Software triggered strobe 101 = Mode 5Hardware triggered strobe
0	**Countdown Type Status**—RO. This bit reflects the current countdown type. 0 = Binary countdown. 1 = Binary Coded Decimal (BCD) countdown.

9.3.3 Counter Access Ports Register

I/O Address:	Counter 0–40h, Counter 1–41h, Counter 2–42h	Attribute:	R/W
Default Value:	All bits undefined	Size:	8 bit

Bit	Description
7:0	**Counter Port**—R/W. Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

9.4 Intel® 8259 Interrupt Controller (PIC) Registers

9.4.1 Interrupt Controller I/O MAP

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ0–7), and at A0h and A1h for the slave controller (IRQ8–13). These registers have multiple functions, depending upon the data written to them. Below is a description of the different register possibilities for each address.

Table 9-3. PIC Registers

Port	Aliases	Register Name	Default	Type
20h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	Master PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Master PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Master PIC OCW3 Op Ctrl Word 3	X01XXX10b	R/W
21h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	Master PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Master PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Master PIC ICW4 Init. Cmd Word 4	01h	WO
		Master PIC OCW1 Op Ctrl Word 1	00h	R/W
A0h	A4h, A8h, ACh, B0h, B4h, B8h, BCh	Slave PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Slave PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Slave PIC OCW3 Op Ctrl Word 3	X01XXX10b	R/W
A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	Slave PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Slave PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Slave PIC ICW4 Init. Cmd Word 4	01h	WO
		Slave PIC OCW1 Op Ctrl Word 1	00h	R/W
4D0h	–	Master PIC Edge/Level Triggered	00h	R/W
4D1h	–	Slave PIC Edge/Level Triggered	00h	R/W

9.4.2 ICW1—Initialization Command Word 1 Register

Offset Address:	Master Controller–020h Slave Controller–0A0h	Attribute:	WO
Default Value:	All bits undefined	Size:	8 bit /controller

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit	Description
7:5	**ICW/OCW Select**—WO. These bits are MCS-85 specific, and not needed. 000 = Should be programmed to “000”
4	**ICW/OCW Select**—WO. 1 = This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	**Edge/Level Bank Select (LTIM)**—WO. Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	ADI—WO. 0 = Ignored for the ICH3. Should be programmed to 0.
1	**Single or Cascade (SNGL)**—WO. 0 = Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	**ICW4 Write Required (IC4)**—WO. 1 = This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

9.4.3 ICW2—Initialization Command Word 2 Register

Offset Address:	Master Controller—021h Slave Controller—0A1h	Attribute:	WO
Default Value:	All bits undefined	Size:	8 bit /controller

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the processor to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Bit	Description
7:3	**Interrupt Vector Base Address**—WO. Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	**Interrupt Request Level**—WO. When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: **Code** / **Master Interrupt** / **Slave Interrupt** 000 / IRQ0 / IRQ8 001 / IRQ1 / IRQ9 010 / IRQ2 / IRQ10 011 / IRQ3 / IRQ11 100 / IRQ4 / IRQ12 101 / IRQ5 / IRQ13 110 / IRQ6 / IRQ14 111 / IRQ7 / IRQ15

9.4.4 ICW3—Master Controller Initialization Command Word 3 Register

Offset Address:	21h	Attribute:	WO
Default Value:	All bits undefined	Size:	8 bits

Bit	Description
7:3	0 = These bits must be programmed to zero.
2	**Cascaded Interrupt Controller IRQ Connection**—WO. This bit indicates that the slave controller is cascaded on IRQ2. When IRQ8#–IRQ15 is asserted, it goes through the slave controller's priority resolver. The slave controller's INTR output onto IRQ2. IRQ2 then goes through the master controller's priority solver. If it wins, the INTR signal is asserted to the processor, and the returning interrupt acknowledge returns the interrupt vector for the slave controller. 1 = This bit must always be programmed to a 1.
1:0	0 = These bits must be programmed to zero.

9.4.5 ICW3—Slave Controller Initialization Command Word 3 Register

Offset Address:	A1h	Attribute:	WO
Default Value:	All bits undefined	Size:	8 bits

Bit	Description
7:3	0 = These bits must be programmed to zero.
2:0	**Slave Identification Code**—WO. These bits are compared against the slave identification code broadcast by the master controller from the trailing edge of the first internal INTA# pulse to the trailing edge of the second internal INTA# pulse. These bits must be programmed to 02h to match the code broadcast by the master controller. When 02h is broadcast by the master controller during the INTA# sequence, the slave controller assumes responsibility for broadcasting the interrupt vector.

9.4.6 ICW4—Initialization Command Word 4 Register

Offset Address:	Master Controller–021h Slave Controller–0A1h	Attribute:	WO
Default Value:		Size:	8 bits

Bit	Description
7:5	0 = These bits must be programmed to zero.
4	**Special Fully Nested Mode (SFNM)**—WO. 0 = Should normally be disabled by writing a 0 to this bit. 1 = Special fully nested mode is programmed.
3	**Buffered Mode (BUF)**—WO. 0 = Must be programmed to 0 for the ICH3. This is non-buffered mode.
2	**Master/Slave in Buffered Mode**—WO. Not used. 0 = Should always be programmed to 0.
1	**Automatic End of Interrupt (AEOI)**—WO. 0 = This bit should normally be programmed to 0. This is the normal end of interrupt. 1 = Automatic End of Interrupt (AEOI) mode is programmed. AEOI is discussed in Section 5.7.4.10.
0	**Microprocessor Mode**—WO. 1 = Must be programmed to 1 to indicate that the controller is operating in an Intel Architecture-based system.

9.4.7 OCW1—Operational Control Word 1 (Interrupt Mask) Register

Offset Address:	Master Controller–021h Slave Controller–0A1h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Request Mask**—R/W. When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

9.4.8 OCW2—Operational Control Word 2 Register

Offset Address:	Master Controller–020h Slave Controller–0A0h	Attribute:	WO
Default Value:	Bit[4:0]=undefined, Bit[7:5]=001	Size:	8 bits

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes (R, SL, EOI)**—WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = Rotate in Auto EOI Mode (Clear) 001 = Non-specific EOI command 010 = No Operation 011 = Specific EOI Command 100 = Rotate in Auto EOI Mode (Set) 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	**OCW2 Select**—WO. When selecting OCW2, bits 4:3 = “00”
2:0	**Interrupt Level Select (L2, L1, L0)**—WO. L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined below, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. **Bits** **Interrupt Level** **Bits** **Interrupt Level** 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

9.4.9 OCW3—Operational Control Word 3 Register

Offset Address:	Master Controller—020h Slave Controller—0A0h	Attribute:	WO
Default Value:	Bit[6,0]=0, Bit[7,4:2]=undef, Bit[5,1]=1	Size:	8 bits

Bit	Description
7	Reserved. Must be 0.
6	**Special Mask Mode (SMM)**—WO. 1 = The Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/disabling of the other channel's mask bits. Bit 5, the ESMM bit, must be set for this bit to have any meaning.
5	**Enable Special Mask Mode (ESMM)**—WO. 0 = Disable. The SMM bit becomes a “don't care”. 1 = Enable the SMM bit to set or reset the Special Mask Mode.
4:3	**OCW3 Select**—WO. When selecting OCW3, bits 4:3 = “01”.
2	**Poll Mode Command**—WO. 0 = Disable. Poll Command is not issued. 1 = Enable. The next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	**Register Read Command**—WO. These bits provide control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1=0, bit 0 will not affect the register read selection. When bit 1=1, bit 0 selects the register status returned following an OCW3 read. If bit 0=0, the IRR will be read. If bit 0=1, the ISR will be read. Following ICW initialization, the default OCW3 port address read will be “read IRR”. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 = No Action 01 = No Action 10 = Read IRQ Register 11 = Read IS Register

9.4.10 ELCR1—Master Controller Edge/Level Triggered Register

Offset Address:	4D0h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The cascade channel, IRQ2, the heart beat timer (IRQ0), and the keyboard controller (IRQ1), cannot be put into level mode.

Bit	Description
7	**IRQ7 ECL**—R/W. 0 = Edge. 1 = Level.
6	**IRQ6 ECL**—R/W. 0 = Edge. 1 = Level.
5	**IRQ5 ECL**—R/W. 0 = Edge. 1 = Level.
4	**IRQ4 ECL**—R/W. 0 = Edge. 1 = Level.
3	**IRQ3 ECL**—R/W. 0 = Edge. 1 = Level.
2:0	Reserved. Must be 0.

9.4.11 ELCR2—Slave Controller Edge/Level Triggered Register

Offset Address:	4D1h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The real time clock interrupt (IRQ8#) and the floating point error interrupt (IRQ13) cannot be programmed for level mode.

Bit	Description
7	**IRQ15 ECL**—R/W. 0 = Edge. 1 = Level.
6	**IRQ14 ECL**—R/W. 0 = Edge. 1 = Level.
5	Reserved. Must be 0.
4	**IRQ12 ECL**—R/W. 0 = Edge. 1 = Level.
3	**IRQ11 ECL**—R/W. 0 = Edge. 1 = Level.
2	**IRQ10 ECL**—R/W. 0 = Edge. 1 = Level.
1	**IRQ9 ECL**—R/W. 0 = Edge. 1 = Level.
0	Reserved. Must be 0.

9.5 Advanced Interrupt Controller (APIC)

9.5.1 APIC Register Map

The APIC is accessed via an indirect addressing scheme. Two registers are visible by software for manipulation of most of the APIC registers. These registers are mapped into memory space. The registers are shown in Table 9-4.

Table 9-4. APIC Direct Registers

Address	Register Name	Size	Type
FEC0_0000h	Index Register	8 bits	R/W
FEC0_0010h	Data Register	32 bits	R/W
FECO_0020h	IRQ Pin Assertion Register	8 bits	WO
FECO_0040h	EOI Register	8 bits	WO

Table 9-5 lists the registers which can be accessed within the APIC via the Index Register. When accessing these registers, accesses must be done a DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Table 9-5. APIC Indirect Registers

Index	Register Name	Size	Type
00h	ID	32 bits	R/W
01h	Version	32 bits	RO
02h	Arbitration ID	32 bits	RO
03h	Boot Configuration	32 bits	R/W
03–0Fh	Reserved		RO
10–11h	Redirection Table 0	64 bits	R/W
12–13h	Redirection Table 1	64 bits	R/W
...	...	...	...
3E–3Fh	Redirection Table 23	64 bits	R/W
40–FFh	Reserved		RO

9.5.2 IND—Index Register

Memory Address	FEC0_0000h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

The Index Register will select which APIC indirect register to be manipulated by software. The selector values for the indirect registers are listed in Table 9-5. Software will program this register to select the desired APIC internal register

Bit	Description
7:0	**APIC Index**—R/W. This is an 8 bit pointer into the I/O APIC register table.

9.5.3 DAT—Data Register

Memory Address	FEC0_0010h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This is a 32 bit register specifying the data to be read or written to the register pointed to by the Index register. This register can only be accessed in DWord quantities.

Bit	Description
7:0	**APIC Data**—R/W. This is a 32 bit register for the data to be read or written to the APIC indirect register pointed to by the Index register.

9.5.4 IRQPA—IRQ Pin Assertion Register

Memory Address	FEC0_0020h	Attribute:	WO
Default Value:	N/A	Size:	32 bits

The IRQ Pin Assertion Register is present to provide a mechanism to scale the number of interrupt inputs into the I/O APIC without increasing the number of dedicated input pins. When a device that supports this interrupt assertion protocol requires interrupt service, that device will issue a write to this register. Bits 4:0 written to this register contain the IRQ number for this interrupt. The only valid values are 0–23. Bits 31:5 are ignored. To provide for future expansion, peripherals should always write a value of 0 for Bits 31:5.

See Section 5.8.4 for more details on how PCI devices will use this field.

Note: Writes to this register are only allowed by the processor and by masters on the ICH3's PCI bus. Writes by devices on PCI buses above the ICH3 (e.g., a PCI segment on a P64H) are not supported.

Bit	Description
31:5	Reserved. To provide for future expansion, the processor should always write a value of 0 to Bits 31:5.
4:0	**IRQ Number**—WO. Bits 4:0 written to this register contain the IRQ number for this interrupt. The only valid values are 0–23.

9.5.5 EOIR—EOI Register

Memory Address	FEC0_0040h	Attribute:	WO
Default Value:	N/A	Size:	32 bits

The EOI register is present to provide a mechanism to maintain the level triggered semantics for level-triggered interrupts issued on the parallel bus.

When a write is issued to this register, the I/O APIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

Note: This is similar to what already occurs when the APIC sees the EIO message on the serial bus. Note that if multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to 0. The interrupt which was prematurely reset will not be lost because if its input remained active when the Remote_IRR bit is cleared, the interrupt will be reissued and serviced at a later time.

Note: Only bits 7:0 are actually used. Bits 31:8 are ignored by the ICH3.

Note: To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.

Bit	Description
31:8	Reserved. To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.
7:0	**Redirection Entry Clear**—WO. When a write is issued to this register, the I/O APIC will check this field, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

9.5.6 ID—Identification Register

Index Offset:	00h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

The APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to zero on power up reset

Bit	Description
31:28	Reserved.
27:24	**APIC ID**—R/W. Software must program this value before using the APIC.
23:16	Reserved.
15	Scratchpad bit.
14:0	Reserved.

9.5.7 VER—Version Register

Index Offset: 01h
Default Value: 00170002h
Attribute: RO
Size: 32 bits

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information also is in this register, to let software know how many interrupt are supported by this APIC.

Bit	Description
31:24	Reserved.
23:16	**Maximum Redirection Entries**—RO. This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range 0 through 239. In the ICH3 this field is hardwired to 17h to indicate 24 interrupts.
15	**PRQ**—RO. This bit is set to 1 to indicate that this version of the I/O APIC implements the IRQ Assertion register and allows PCI devices to write to it to cause interrupts.
14:8	Reserved.
7:0	**Version**—RO. This is a version number that identifies the implementation version.

9.5.8 ARBID—Arbitration ID Register

Index Offset: 02h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

This register contains the bus arbitration priority for the APIC. If APIC Clock is running, this register is loaded whenever the APIC ID register is loaded. A rotating priority scheme is used for APIC bus arbitration. The winner of the arbitration becomes the lowest priority agent and assumes an arbitration ID of 0.

Bit	Description
31:28	Reserved.
27:24	**I/O APIC Identification**—RO. This 4 bit field contains the I/O APIC Arbitration ID.
23:0	Reserved.

9.5.9 BOOT_CONFIG—Boot Configuration Register

Index Offset: 03h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

This register is used to control the interrupt delivery mechanism for the APIC.

Bit	Description
31:1	Reserved.
0	Delivery Type (DT)—R/W. 0 = Interrupt delivery mechanism is via the APIC serial bus (default). 1 = Interrupt delivery mechanism is a Processor System Bus message.

9.5.10 Redirection Table

Index Offset:	10h–11h (vector 0) through 3E–3Fh (vector 23)	Attribute:	R/W
Default Value:	Bit 16–1, Bits[15:12]=0. All other bits undefined	Size:	64 bits each, (accessed as two 32 bit quantities)

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.

The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an acknowledgment from the APIC bus unit that the interrupt message was sent over the APIC bus. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request Register bit to go from 0 to 1. (In other words, if the interrupt was not already pending at the destination.)

Bit	Description
63:56	Destination—R/W. If bit 11 of this entry is 0 [Physical], then bits [59:56] specifies an APIC ID. In this case, bits 63:59 should be programmed by software to 0. If bit 11 of this entry is 1 [Logical], then bits [63:56] specify the logical destination address of a set of processors.
55:17	Reserved. Software should program bits 55:48 to 0.
16	**Mask**—R/W. 0 = Not masked: An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Masked: Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt. This behavior is identical to the device withdrawing the interrupt before it is posted to the processor. It is software's responsibility to deal with the case where the mask bit is set after the interrupt message has been accepted by a local APIC unit but before the interrupt is dispensed to the processor.
15	**Trigger Mode**—R/W. This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = Edge triggered. 1 = Level triggered.
14	**Remote IRR**—R/W. This bit is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received from a local APIC. 1 = Set when Local APIC/s accept the level interrupt sent by the I/O APIC.
13	**Interrupt Input Pin Polarity**—R/W. This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Active high. 1 = Active low.
12	**Delivery Status**—RO. This field contains the current status of the delivery of this interrupt. Writes to this bit have no effect. 0 = Idle. No activity for this interrupt. 1 = Pending. Interrupt has been injected, but delivery is held up due to the APIC bus being busy or the inability of the receiving APIC unit to accept the interrupt at this time.

Bit	Description
11	**Destination Mode**—R/W. This field determines the interpretation of the Destination field. 0 = Physical. Destination APIC ID is identified by bits [59:56]. 1 = Logical. Destinations are identified by matching bit [63:56] with the Logical Destination in the Destination Format Register and Logical Destination Register in each Local APIC.
10:8	**Delivery Mode**—R/W. This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are listed in the note below.
7:0	**Vector**—R/W. This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

NOTE: Delivery Mode encoding:

000 = Fixed. Deliver the signal on the INTR signal of all processor cores listed in the destination. Trigger Mode can be edge or level.

001 = Lowest Priority. Deliver the signal on the INTR signal of the processor core that is executing at the lowest priority among all the processors listed in the specified destination. Trigger Mode can be edge or level.

010 = SMI (System Management Interrupt). Requires the interrupt to be programmed as edge triggered. The vector information is ignored but must be programmed to all zeroes for future compatibility.

011 = Reserved

100 = NMI. Deliver the signal on the NMI signal of all processor cores listed in the destination. Vector information is ignored. NMI is treated as an edge triggered interrupt even if it is programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The NMI delivery mode does not set the RIRR bit. Once the interrupt is detected, it will be sent over the APIC bus. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the NMI pin is reached again, the interrupt will be sent over the APIC bus again.

101 = INIT. Deliver the signal to all processor cores listed in the destination by asserting the INIT signal. All addressed local APICs will assume their INIT state. INIT is always treated as an edge triggered interrupt even if programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The INIT delivery mode does not set the RIRR bit. Once the interrupt is detected, it will be sent over the APIC bus. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the INIT pin is reached again, the interrupt will be sent over the APIC bus again.

110 = Reserved

111 = ExtINT. Deliver the signal to the INTR signal of all processor cores listed in the destination as an interrupt that originated in an externally connected 8259A compatible interrupt controller. The INTA cycle that corresponds to this ExtINT delivery will be routed to the external controller that is expected to supply the vector. Requires the interrupt to be programmed as edge triggered.

9.6 Real Time Clock Registers

9.6.1 I/O Register Address Map

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A–D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM, and will be accessible even when the RTC module is disabled (via the RTC configuration register). Registers A–D do not physically exist in the RAM.

All data movement between the host processor and the real-time clock is done through registers mapped to the standard I/O space. The register map appears in Table 9-6.

Table 9-6. RTC I/O Registers

I/O Locations	If U128E bit = 0	Function
70h and 74h	Also alias to 72h and 76h	Real-Time Clock (Standard RAM) Index Register
71h and 75h	Also alias to 73h and 77h	Real-Time Clock (Standard RAM) Target Register
72h and 76h		Extended RAM Index Register (if enabled)
73h and 77h		Extended RAM Target Register (if enabled)

NOTES:

1. I/O locations 70h and 71h are the standard ISA location for the real-time clock. The map for this bank is shown in Table 9-7. Locations 72h and 73h are for accessing the extended RAM. The extended RAM bank is also accessed using an indexed scheme. I/O address 72h is used as the address pointer and I/O address 73h is used as the data register. Index addresses above 127h are not valid. If the extended RAM is not needed, it may be disabled.
2. Software must preserve the value of bit 7 at I/O addresses 70h and 74h. When writing to these addresses, software must first read the value, and then write the same value for bit 7 during the sequential address write.

9.6.2 Indexed Registers

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70/71h or 72/73h), as shown in Table 9-7.

Table 9-7. RTC (Standard) RAM Bank

Index	Name
00h	Seconds
01h	Seconds Alarm.
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0E–7Fh	114 Bytes of User RAM

9.6.2.1 RTC_REGA—Register A

RTC Index:	0Ah	Attribute:	R/W
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	RTC

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other ICH3 reset signal.

Bit	Description
7	**Update In Progress (UIP)**—R/W. This bit may be monitored as a status flag. 0 = The update cycle will not start for at least 492us. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:4	**Division Chain Select (DV[2:0])**— R/W. These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal. DV[2] corresponds to bit 6. 010 = Normal Operation 11X = Divider Reset 101 = Bypass 15 stages (test mode only) 100 = Bypass 10 stages (test mode only) 011 = Bypass 5 stages (test mode only) 001 = Invalid 000 = Invalid
3:0	**Rate Select (RS[3:0])**—R/W. Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to zero. RS3 corresponds to bit 3. 0000 = Interrupt never toggles 0001 = 3.90625 ms 0010 = 7.8125 ms 0011 = 122.070 µs 0100 = 244.141 µs 0101 = 488.281 µs 0110 = 976.5625 µs 0111 = 1.953125 ms 1000 = 3.90625 ms 1001 = 7.8125 ms 1010 = 15.625 ms 1011 = 31.25 ms 1100 = 62.5 ms 1101 = 125 ms 1110 = 250 ms 1111= 500 ms

9.6.2.2 RTC_REGB—Register B (General Configuration)

RTC Index:	0Bh	Attribute:	R/W
Default Value:	U0U00UUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Update Cycle Inhibit (SET)**—R/W. Enables/Inhibits the update cycles. This bit is not affected by RSMRST# nor any other reset signal. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to zero. When set is one, the BIOS may initialize time and calendar bytes safely.
6	**Periodic Interrupt Enable (PIE)**—R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Allows an interrupt to occur with a time base set with the RS bits of register A.
5	**Alarm Interrupt Enable (AIE)**—R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Allows an interrupt to occur when the AF is set by an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or one a month.
4	**Update-Ended Interrupt Enable (UIE)**—R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Allows an interrupt to occur when the update cycle ends.
3	**Square Wave Enable (SQWE)**—R/W. This bit serves no function in the ICH3. It is left in this register bank to provide compatibility with the Motorola* 146818B. The ICH3 has no SQW pin. This bit is cleared by RSMRST#, but not on any other reset.
2	**Data Mode (DM)**—R/W. Specifies either binary or BCD data representation. This bit is not affected by RSMRST# nor any other reset signal. 0 = BCD. 1 = Binary.
1	**Hour Format (HOURFORM)**—R/W. Indicates the hour byte format. This bit is not affected by RSMRST# nor any other reset signal. 0 = Twelve-hour mode. In twelve hour mode, the seventh bit represents AM as zero and PM as one. 1 = Twenty-four hour mode.
0	**Daylight Savings Enable (DSE)**—R/W. Triggers two special hour updates per year. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. This bit is not affected by RSMRST# nor any other reset signal. 0 = Daylight Savings Time updates do not occur. 1 = a) Update on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. b) Update on the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time must increment normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly.

9.6.2.3 RTC_REGC—Register C (Flag Register)

RTC Index:	0Ch	Attribute:	RO
Default Value:	00U00000 (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Writes to Register C have no effect.

Bit	Description
7	**Interrupt Request Flag (IRQF)**—RO. IRQF = (PF * PIE) + (AF * AIE) + (UF *UFE). This also causes the CH_IRQ_B signal to be asserted. This bit is cleared upon RSMRST# or a read of Register C.
6	**Periodic Interrupt Flag (PF)**—RO. This bit is cleared upon RSMRST# or a read of Register C. 0 = If no taps are specified via the RS bits in Register A, this flag will not be set. 1 = Periodic interrupt Flag will be 1 whenever the tap specified by the RS bits of register A is 1.
5	**Alarm Flag (AF)**—RO. 0 = This bit is cleared upon RTCRST# or a read of Register C. 1 = Alarm Flag will be set after all Alarm values match the current time.
4	**Update-Ended Flag (UF)**—RO. 0 = The bit is cleared upon RSMRST# or a read of Register C. 1 = Set immediately following an update cycle for each second.
3:0	Reserved. Will always report 0.

9.6.2.4 RTC_REGD—Register D (Flag Register)

RTC Index:	0Dh	Attribute:	R/W
Default Value:	10UUUUUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Valid RAM and Time Bit (VRT)**—R/W. 0 = This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles. 1 = This bit is hardwired to 1 in the RTC power well.
6	Reserved. This bit always returns a 0 and should be set to 0 for write cycles.
5:0	**Date Alarm**—R/W. These bits store the date of month alarm value. If set to 000000b, then a don't care state is assumed. The host must configure the date alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by RESET.

9.7 Processor Interface Registers

9.7.1 NMI_SC—NMI Status and Control Register

I/O Address:	61h	Attribute:	R/W (some bits RO)
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**SERR# NMI Source Status (SERR#_NMI_STS)**—RO. 1 = PCI agent detected a system error and pulses the PCI SERR# line. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. When writing to port 61h, this bit must be 0.
6	**IOCHK# NMI Source Status (IOCHK_NMI_STS)**—RO. 1 = An ISA agent (via SERIRQ) asserted IOCHK# on the ISA bus. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 0 and then set it to 1. When writing to port 61h, this bit must be a 0.
5	**Timer Counter 2 OUT Status (TMR2_OUT_STS)**—RO. This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	**Refresh Cycle Toggle (REF_TOGGLE)**—RO. This signal toggles from either 0 to 1 or 1 to 0 at a rate that is equivalent to when refresh cycles would occur. When writing to port 61h, this bit must be a 0.
3	I**OCHK# NMI Enable (IOCHK_NMI_EN)**—R/W. 0 = Enabled. 1 = Disabled and cleared.
2	**PCI SERR# Enable (PCI_SERR_EN)**—R/W. 0 = SERR# NMIs are enabled. 1 = SERR# NMIs are disabled and cleared.
1	**Speaker Data Enable (SPKR_DAT_EN)**—R/W. 0 = SPKR output is a 0. 1 = SPKR output is equivalent to the Counter 2 OUT signal value.
0	**Timer Counter 2 Enable (TIM_CNT2_EN)**—R/W. 0 = Disable. 1 = Enable.

9.7.2 NMI_EN—NMI Enable (and Real Time Clock Index) Register

I/O Address:	70h	Attribute:	R/W (Special)
Default Value:	80h	Size:	8-bit
Lockable:	No	Power Well:	Core

Note: The RTC Index field is write-only for normal operation. This field can only be read in Alt-Access Mode. Note, however that this register is aliased to Port 74h (documented in Table 9-6), and all bits are readable at that address.

Bits	Description
7	**NMI Enable (NMI_EN)**—R/W. 0 = Enable NMI sources. 1 = Disable All NMI sources.
6:0	**Real Time Clock Index Address (RTC_INDX)**—R/W. This data goes to the RTC to select which register or CMOS RAM address is being accessed.

9.7.3 PORT92—Fast A20 and Init Register

I/O Address:	92h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:2	Reserved.
1	**Alternate A20 Gate (ALT_A20_GATE)**—R/W. This bit is Or'd with the A20GATE input signal to generate A20M# to the processor. 0 = A20M# signal can potentially go active. 1 = This bit is set when INIT# goes active.
0	**INIT_NOW**—R/W. When this bit transitions from a 0 to a 1, the ICH3 will force INIT# active for 16 PCI clocks.

9.7.4 COPROC_ERR—Coprocessor Error Register

I/O Address:	F0h	Attribute:	WO
Default Value:	00h	Size:	8-bits
Lockable:	No	Power Well:	Core

Bits	Description
7:0	**COPROC_ERR**—WO. Any value written to this register will cause IGNNE# to go active, if FERR# had generated an internal IRQ13. For FERR# to generate an internal IRQ13, the COPROC_ERR_EN bit (Device 31:Function 0, Offset D0, Bit 13) must be 1.

9.7.5 RST_CNT—Reset Control Register

I/O Address:	CF9h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved.
3	**Full Reset (FULL_RST)**—R/W. This bit is used to determine the states of SLP_S3# and SLP_S5# after a CF9 hard reset (SYS_RST =1 and RST_CPU is set to 1), after PWROK going low (with RSMRST# high), or after two TCO timeouts. 0 = ICH3 will keep SLP_S3# and SLP_S5# high. 1 = ICH3 will drive SLP_S3# and SLP_S5# low for 3–5 seconds.
2	**Reset CPU (RST_CPU)**—R/W. When this bit transitions from a 0 to a 1, it initiates a hard or soft reset, as determined by the SYS_RST bit (bit 1 of this register).
1	**System Reset (SYS_RST)**—R/W. This bit is used to determine a hard or soft reset to the processor. 0 = When RST_CPU bit goes from 0 to 1, the ICH3 performs a soft reset by activating INIT# for 16 PCI clocks. 1 = When RST_CPU bit goes from 0 to 1, the ICH3 performs a hard reset by activating PCIRST# for 1 millisecond. It also resets the resume well bits (except for those noted throughout the EDS).
0	Reserved.

9.8 Power Management Registers (D31:F0)

The power management registers are distributed within the PCI Device 31: Function 0 space, as well as a separate I/O range. Each register is described below. Unless otherwise indicate, bits are in the main (core) power well.

Bits not explicitly defined in each register are assumed to be reserved. When writing to a reserved bit, the value should always be 0. Software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

9.8.1 Power Management PCI Configuration Registers (D31:F0)

Table 9-8 shows a small part of the configuration space for PCI Device 31: Function 0. It includes only those registers dedicated for power management.

Some of the registers are only used for Legacy Power management schemes.

Table 9-8. PCI Configuration Map (PM—D31:F0)

Offset	Mnemonic	Register Name/Function	Default	Type
40–43h	ACPI_BASE	ACPI Base Address	00000001h	R/W
44h	ACPI_CNTL	ACPI Control	00h	R/W
A0h	GEN_PMCON_1	General Power Management Configuration 1	0000h	R/W
A2h	GEN_PMCON_2	General Power Management Configuration 2	0000h	R/W
A4h	GEN_PMCON_3	General Power Management Configuration 3	00h	R/W
A8h	STPCLK_DEL	Stop Clock Delay Register	0Dh	R/W
B8–BBh	GPI_ROUT	GPI Route Control	00000000h	R/W
C0h	TRP_FWD_EN	I/O Monitor Trap Forwarding Enable	00h	
C4–CAh	MON[*n*]_TRP_RNG	I/O Monitor[4:7] Trap Range	0000h	R/W
CCh	MON_TRP_MSK	I/O Monitor Trap Range Mask	0000h	R/W

9.8.1.1 GEN_PMCON_1—General PM Configuration 1 Register (PM—D31:F0)

Offset Address:	A0h	Attribute:	R/W
Default Value:	00h	Size:	16-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Bit	Description
15:11	Reserved.
10	**Software SMI Rate Select (SWSMI_RATE_SEL)**—R/W. 0 = SWSMI Timer will time out in 64 ms ± 4 ms (default). 1 = SWSMI Timer will time out in 1.5 ms ± 0.5 ms.
9	**PWRBTN_LVL**—RO. This read-only bit indicates the current state of the PWRBTN# signal. 0 = Low. 1 = High.
8:6	Reserved.
5	**CPU SLP# Enable (CPUSLP_EN)**—R/W. 0 = Disable. 1 = Enables the CPUSLP# signal to go active in the S1. This reduces the processor power. Note that CPUSLP# will go active during Intel® SpeedStep™ technology transitions and on entry to S1, S3, S4 and S5 even if this bit is not set.
4:2	Reserved.
1:0	**Periodic SMI# Rate Select (PER_SMI_SEL)**—R/W. Set by software to control the rate at which periodic SMI# is generated. 00 = 1 minute 01 = 32 seconds 10 = 16 seconds 11 = 8 seconds

9.8.1.2 GEN_PMCON_2—General PM Configuration 2 Register (PM—D31:F0)

Offset Address:	A2h	Attribute:	R/WC
Default Value:	00h	Size:	16-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Resume		

Bit	Description
7:2	Reserved.
1	**CPU Power Failure (CPUPWR_FLR)**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Indicates that the VRMPWRGD signal, from the processor's VRM, went low.
0	**PWROK Failure (PWROK_FLR)**—R/WC. 0 = Software clears this bit by writing a 1 to it, or when the system goes into a G3 state. 1 = This bit will be set any time PWROK goes low, when the system was in S0, or S1 state. The bit will be cleared only by software by writing a 1 to this bit or when the system goes to a G3 state. **NOTE:** Traditional designs have a reset button logically AND'd with the PWROK signal from the power supply and the processor's voltage regulator module. If this is done with the ICH3, the PWROK_FLR bit will be set. The ICH3 treats this internally as if the RSMRST# signal had gone active. However, it is not treated as a full power failure. If PWROK goes inactive and then active (but RSMRST# stays high), then the ICH3 will reboot (regardless of the state of the AFTERG3 bit). If the RSMRST# signal also goes low before PWROK goes high, then this is a full power failure, and the reboot policy is controlled by the AFTERG3 bit.

NOTE: VGATE is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the ICH3.

9.8.1.3 GEN_PMCON_3—General PM Configuration 3 Register (PM—D31:F0)

Offset Address:	A4h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	RTC		

Bit	Description
7:3	Reserved.
2	**RTC Power Status (RTC_PWR_STS)**—R/WC. 0 = Software clears this bit by writing a 0 to the bit position. 1 = Indicates that the RTC battery was removed or has 0 volts. This bit is set when the RTCRST# signal is low. **NOTE:** Clearing CMOS in an Intel ICH3-based platform can be done by using a jumper on RTCRST# or GPI, or using a SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.
1	**Power Failure (PWR_FLR)**—R/WC. This bit is in the RTC well, and is not cleared by any type of reset except RTCRST#. 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software clears this bit by writing a 1 to the bit position. 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. **NOTE:** Clearing CMOS in an ICH3-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.
0	**AFTERG3_EN**—R/W. Determines what state to go to when power is re-applied after a power failure (G3 state). This bit is in the RTC well and is not cleared by any type of reset except writes to CF9h or RTCRST#. 0 = System will return to S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4). In the S5 state, the only enabled wake event is the Power Button or any enabled wake event that was preserved through the power failure.

NOTE: RSMRST# is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the ICH3.

9.8.1.4 STPCLK_DEL—Stop Clock Delay Register (PM—D31:F0)

Offset Address:	A8h	Attribute:	R/W
Default Value:	0Dh	Size:	8-bit
Power Well:	Core	Usage:	ACPI, Legacy

Bit	Description
7:6	Reserved.
5:0	**STPCLK_DEL.** Selects the value for t190 (CPUSLP# inactive to STPCLK# inactive). The default value of 0Dh yields a default of approximately 50.045 microseconds. The maximum value of 3Fh will result in a time of 245 microseconds. **NOTE:** Software must program the value to a range that can be tolerated by the associated processor and chipset. The ICH3 requires that software does not program a value of 00h or 01h; a minimum programming of 02h yields the minimum possible delay of 3.87 microseconds.

9.8.1.5 GPI_ROUT—GPI Routing Control Register (PM—D31:F0)

Offset Address:	B8h–BBh	Attribute:	R/W
Default Value:	0000h	Size:	32-bit
Lockable:	No	Power Well:	Resume

Bit	Description
31:30	**GPI[15] Route**—R/W. See bits 1:0 for description.
Same pattern for GPI[14] through GPI[3]	
5:4	**GPI[2] Route**—R/W. See bits 1:0 for description.
3:2	**GPI[1] Route**—R/W. See bits 1:0 for description.
1:0	**GPI[0] Route**—R/W. GPIO[15:0] can be routed to cause an SMI or SCI when the GPI[n]_STS bit is set. If the GPIO is not set to an input, this field has no effect. If the system is in an S1–S5 state and if the GPE1_EN bit is also set, then the GPI can cause a Wake event, even if the GPI is NOT routed to cause an SMI# or SCI. 00 = No effect. 01 = SMI# (if corresponding GPE1_EN bit is also set). 10 = SCI (if corresponding GPE1_EN bit is also set). 11 = Reserved.

Note: GPIOs that are not implemented will not have the corresponding bits implemented in this register.

9.8.1.6 TRP_FWD_EN—I/O Monitor Trap Forwarding Enable Register (PM—D31:F0)

Offset Address:	C0h	Attribute:	R/W (Special)
Default Value:	00h	Size:	8 bits
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

The ICH3 uses this register to enable the monitors to forward cycles to LPC, independent of the POS_DEC_EN bit and the bits that enable the monitor to generate an SMI#. The only criteria is that the address passes the decoding logic as determined by the MON[*n*]_TRP_RNG and MON_TRP_MSK register settings.

Bit	Description
7	**MON7_FWD_EN**—R/W. 0 = Disable. Cycles trapped by I/O Monitor 7 will not be forwarded to LPC. 1 = Enable. Cycles trapped by I/O Monitor 7 will be forwarded to LPC.
6	**MON6_FWD_EN**—R/W. 0 = Disable. Cycles trapped by I/O Monitor 6 will not be forwarded to LPC. 1 = Enable. Cycles trapped by I/O Monitor 6 will be forwarded to LPC.
5	**MON5_FWD_EN**—R/W. 0 = Disable. Cycles trapped by I/O Monitor 5 will not be forwarded to LPC. 1 = Enable. Cycles trapped by I/O Monitor 5 will be forwarded to LPC.
4	**MON4_FWD_EN**—R/W. 0 = Disable. Cycles trapped by I/O Monitor 4 will not be forwarded to LPC. 1 = Enable. Cycles trapped by I/O Monitor 4 will be forwarded to LPC.
3:0	Reserved.

9.8.1.7 MON[*n*]_TRP_RNG—I/O Monitor [4:7] Trap Range Register for Devices 4–7 (PM—D31:F0)

Offset Address:	C4h, C6h, C8h, CAh	Attribute:	R/W
Default Value:	00h	Size:	16 bits
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

These registers set the ranges that Device Monitors 4–7 should trap. Offset 4Ch corresponds to Monitor 4. Offset C6h corresponds to Monitor 5, etc.

If the trap is enabled in the MON_SMI register and the address is in the trap range (and passes the mask set in the MON_TRP_MSK register) the ICH3 will generate an SMI#. This SMI# occurs if the address is positively decoded by another device on PCI or by the ICH3 (because it would be forwarded to LPC or some other ICH3 internal registers). The trap ranges should not point to registers in the ICH3's internal IDE, USB, AC'97 or LAN I/O space. If the cycle is to be claimed by the ICH3 and targets one of the permitted ICH3 internal registers (interrupt controller, RTC, etc.), the cycle will complete to the intended target and an SMI# will be generated (this is the same functionality as the ICH component). If the cycle is to be claimed by the ICH3 and the intended target is on LPC, an SMI# will be generated but the cycle will only be forwarded to the intended target if forwarding to LPC is enabled via the TRP_FWD_EN register settings.

Bit	Description
15:0	**MON[*n*]_TRAP_BASE**—R/W. Base I/O locations that MON[*n*] traps (where *n* = 4, 5, 6 or 7). The range can be mapped anywhere in the processor I/O space (0–64K). Any access to the range will generate an SMI# if enabled by the associated DEV[*n*]_TRAP_EN bit in the MON_SMI register (PMBASE +40h).

9.8.1.8 MON_TRP_MSK—I/O Monitor Trap Range Mask Register for Devices 4-7 (PM—D31:F0)

Offset Address:	CCh	Attribute:	R/W
Default Value:	00h	Size:	16 bits
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Bit	Description
15:12	**MON7_MASK**—R/W. Selects low 4-bit mask for the I/O locations that MON7 will trap. Similar to MON4_MASK.
11:8	**MON6_MASK**—R/W. Selects low 4-bit mask for the I/O locations that MON6 will trap. Similar to MON4_MASK.
7:4	**MON5_MASK**—R/W. Selects low 4-bit mask for the I/O locations that MON5 will trap. Similar to MON4_MASK.
3:0	**MON4_MASK**—R/W. Selects low 4-bit mask for the I/O locations that MON7 will trap. When a mask bit is set to a 1, the corresponding bit in the base I/O selection will not be decoded. For example, if MON4_TRAP_BASE = 1230h, and MON4_MSK = 0011b, the ICH3 will decode 1230h, 1231h, 1232h, and 1233h for Monitor 4.

9.8.2 APM I/O Decode

Table 9-9 shows the I/O registers associated with APM support. This register space is enabled in the PCI Device 31: Function 0 space (APMDEC_EN), and cannot be moved (fixed I/O location).

Table 9-9. APM Register Map

Address	Mnemonic	Register Name	Default	Type
B2h	APM_CNT	Advanced Power Management Control Port	00h	R/W
B3h	APM_STS	Advanced Power Management Status Port	00h	R/W

9.8.2.1 APM_CNT—Advanced Power Management Control Port Register

I/O Address: B2h
Default Value: 00h
Lockable: No
Power Well: Core
Attribute: R/W
Size: 8-bit
Usage: Legacy Only

Bit	Description
7:0	Used to pass an APM command between the OS and the SMI handler. Writes to this port not only store data in the APMC register, but also generates an SMI# when the APMC_EN bit is set.

9.8.2.2 APM_STS—Advanced Power Management Status Port Register

I/O Address: B3h
Default Value: 00h
Lockable: No
Power Well: Core
Attribute: R/W
Size: 8-bit
Usage: Legacy Only

Bit	Description
7:0	Used to pass data between the OS and the SMI handler. Basically, this is a scratchpad register and is not effected by any other register or function (other than a PCI reset).

9.8.3 Power Management I/O Registers

Table 9-10 shows the registers associated with ACPI and Legacy power management support. These registers are enabled in the PCI Device 31: Function 0 space (PM_IO_EN), and can be moved to any I/O location (128-byte aligned). The registers are defined to be compliant with the ACPI 1.0 specification, and use the same bit names.

Note: All reserved bits and registers will always return 0 when read, and will have no effect when written.

Table 9-10. ACPI and Legacy I/O Register Map

PMBASE+ Offset	Register Name	ACPI Pointer	Default	Attributes
00–01h	PM1 Status	PM1a_EVT_BLK	0000h	R/W
02–03h	PM1 Enable	PM1a_EVT_BLK+2	0000h	R/W
04–07h	PM1 Control	PM1a_CNT_BLK	00000000h	R/W
08–0Bh	PM1 Timer	PMTMR_BLK	00000000h	RO
0C–0Fh	Reserved	—	—	—
10h–13h	Processor Control	P_BLK	00000000h	R/W
14h	Level 2 Register	P_BLK+4	00h	RO
15–27h	Reserved	—	—	—
28–29h	General Purpose Event 0 Status	GPE0_BLK	0000h	R/W
2A–2Bh	General Purpose Event 0 Enables	GPE0_BLK+2	0000h	R/W
2C–2D	General Purpose Event 1 Status	GPE1_BLK	0000h	R/W
2E–2F	General Purpose Event 1 Enables	GPE1_BLK+2	0000h	R/W
30–31h	SMI# Control and Enable	—	0000h	R/W
34–35h	SMI Status Register	—	0000h	R/W
36–3Fh	Reserved	—	0000h	RO
40–41h	Monitor SMI Status	—	0000h	R/W
41–43h	Reserved	—	—	—
44–45h	Device Trap Status	—	0000h	R/W
48–49h	Trap Enable register	—	0000h	R/W
4Ch–4Dh	Bus Address Tracker	—	Last Cycle	RO
4Eh	Bus Cycle Tracker	—	Last Cycle	RO
4Fh–5Fh	Reserved	—	—	—
60h–7Fh	Reserved for TCO Registers	—	—	—

9.8.3.1 PM1_STS—Power Management 1 Status Register

I/O Address:	PMBASE + 00h ***(ACPI PM1a_EVT_BLK)***	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–15: Resume, except Bit 11 in RTC		

If bit 10 or 8 in this register is set, and the corresponding _EN bit is set in the PM1_EN register, then the ICH3 generates a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the ICH3 also generates an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set.

Note: Bit 5 does not cause an SMI# or a wake event. Bit 0 does not cause a wake event but can cause an SMI# or SCI.

Bit	Description
15	**Wake Status (WAK_STS)**—R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when the system is in one of the sleep states (via the SLP_EN bit) and an enabled wake event occurs. Upon setting this bit, the ICH3 will transition the system to the ON state. If the AFTERG3_EN bit is not set and a power failure (such as removed batteries) occurs without the SLP_EN bit set, the system will return to an S0 state when power returns, and the WAK_STS bit will not be set. If the AFTERG3_EN bit is set and a power failure occurs without the SLP_EN bit having been set, the system will go into an S5 state when power returns, and a subsequent wake event will cause the WAK_STS bit to be set. Note that any subsequent wake event would have to be caused by either a Power Button press, or an enabled wake event that was preserved through the power failure (enable bit in the RTC well).
14:12	Reserved.
11	**Power Button Override Status (PRBTNOR_STS)**—R/WC. This bit is not affected by hard resets caused by a CF9 write, and is not reset by RSMRST#. Thus, this bit will be preserved through a power failure. 0 = The BIOS or SCI handler can clear this bit by writing a 1 to it. 1 = Set by hardware anytime PWROK is high and a Power Button Override Event occurs, which occurs when the power button is pressed for at least 4 consecutive seconds. The power button override causes an unconditional transition to the S5 state, and sets the AFTERG3 bit. This bit can also be set by the SMBus Slave logic.
10	**RTC Status (RTC_STS)**—R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when the RTC generates an alarm (assertion of the IRQ8# signal). Additionally if the RTC_EN bit is set, the setting of the RTC_STS bit will generate a wake event.
9	Reserved.

Bit	Description
8	**Power Button Status (PWRBTN__STS)**—R/WC. This bit is not affected by hard resets caused by a CF9 write. 0 = If the PWRBTN# signal is held low for more than 4 seconds, the hardware clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, and the system transitions to the S5 state with only PWRBTN# enabled as a wake event. This bit can be cleared by software by writing a one to the bit position. 1 = 1 = This bit is set by hardware when the PWRBTN# signal is asserted Low, independent of any other enable bit. In the S0 state, while PWRBTN_EN and PWRBTN_STS are both set, an SCI (or SMI# if SCI_EN is not set) will be generated. In any sleeping state S1–S5, while PWRBTN_EN and PWRBTN_STS are both set, a wake event is generated.
7:6	Reserved.
5	**Global Status (GBL _STS)**—R/WC. 0 = The SCI handler should then clear this bit by writing a 1 to the bit location. 1 = Set when an SCI is generated due to BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit.
4:1	Reserved.
0	**Timer Overflow Status (TMROF_STS)**—R/WC. 0 = The SCI or SMI# handler clears this bit by writing a 1 to the bit location. 1 = This bit gets set any time bit 22 of the 24-bit timer goes high (bits are numbered from 0 to 23). This will occur every 2.3435 seconds. When the TMROF_EN bit is set, then the setting of the TMROF_STS bit will additionally generate an SCI or SMI# (depending on the SCI_EN).

9.8.3.2 PM1_EN—Power Management 1 Enable Register

I/O Address:	PMBASE + 02h ***(ACPI PM1a_EVT_BLK + 2)***	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0:7: Core, Bits 8, 9: Resume Bit 10: RTC Bits 11:15: Resume		

Bit	Description
15:11	Reserved.
10	**RTC Event Enable (RTC_EN)**—R/W. This bit is in the RTC well to allow an RTC event to wake after a power failure. This bit is not cleared by any reset other than RTCRST# or a Power Button Override event. 0 = No SCI (or SMI#) or wake event is generated then RTC_STS goes active. 1 = An SCI (or SMI#) or wake event will occur when this bit is set and the RTC_STS bit goes active.
9	Reserved.
8	**Power Button Enable (PWRBTN_EN)**—R/W. This bit is used to enable the setting of the PWRBTN_STS bit to generate a power management event (SMI#, SCI). PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event. 0 = Disable. 1 = Enable.
7:6	Reserved.
5	**Global Enable (GBL_EN)**—R/W. When both the GBL_EN and the GBL_STS are set, an SCI is raised. 0 = Disable. 1 = Enable SCI on GBL_STS going active.
4:1	Reserved.
0	**Timer Overflow Interrupt Enable (TMROF_EN)**—R/W. Works in conjunction with the SCI_EN bit as described below: **TMROF_EN** / **SCI_EN** / **Effect when TMROF_STS is set** 0 / x / No SMI# or SCI 1 / 0 / SMI# 1 / 1 / SCI

9.8.3.3 PM1_CNT—Power Management 1 Control Register

I/O Address:	PMBASE + 04h (***ACPI PM1a_CNT_BLK)***	Attribute:	R/W
Default Value:	0000h	Size:	32-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–15: Resume		

Bit	Description
15:14	Reserved.
13	**Sleep Enable (SLP_EN)**—WO. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	**Sleep Type (SLP_TYP)**—R/W. This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. 000 = ON: Typically maps to S0 state. 001 = Asserts STPCLK#. Puts processor in Stop-Grant state. Optional to assert CPUSLP# to put the processor in sleep state: Typically maps to S1 state. 010 = Reserved. 011 = Reserved. 100 = Reserved. 101 = Suspend-To-RAM. Assert SLP_S1# and SLP_S3#: Typically maps to S3 state. 110 = Suspend-To-Disk. Assert SLP_S1#, SLP_S3#, and SLP_S5# SLP_S3# and SLP_S5#: Typically maps to S4 state. 111 = Soft Off. Assert SLP_S1#, SLP_S3#, and SLP_S5# SLP_S3#, and SLP_S5#: Typically maps to S5 state.
9:3	Reserved.
2	**Global Release (GBL_RLS)**—WO. 0 = This bit always reads as 0. 1 = ACPI software writes a 1 to this bit to raise an event to the BIOS. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events.
1	Reserved.
0	**SCI Enable (SCI_EN)**—R/W. Selects the SCI interrupt or the SMI# interrupt for various events including the bits in the PM1_STS register (bit 10, 8, 0), and bits in GPE0_STS. 0 = These events will generate an SMI#. 1 = These events will generate an SCI.

9.8.3.4 PM1_TMR—Power Management 1 Timer Register

I/O Address:	PMBASE + 08h (***ACPI PMTMR_BLK)***	Attribute:	RO
Default Value:	xx000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI
Power Well:	Core		

Bit	Description
31:24	Reserved.
23:0	**Timer Value (TMR_VAL)**—RO. Returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (14.31818 MHz divided by 4). It is reset to zero during a PCI reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. If the TMROF_EN bit is set, an SCI interrupt is also generated.

9.8.3.5 PROC_CNT—Processor Control Register

I/O Address:	PMBASE + 10h ***(ACPI P_BLK)***	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No (bits 7:5 are write once)	Usage:	ACPI or Legacy
Power Well:	Core		

Bit	Description
31:18	Reserved.
17	**Throttle Status (THTL_STS)**—RO. 0 = No clock throttling is occurring (maximum processor performance). 1 = Indicates that the clock state machine is in some type of low power state (where the processor is not running at its maximum performance): thermal throttling or hardware throttling.
16:9	Reserved.
8	**Force Thermal Throttling (FORCE_THTL)**—R/W. Software can set this bit to force the thermal throttling function. This has the same effect as the THRM# signal being active for 2 seconds. 0 = No forced throttling. 1 = Throttling at the duty cycle specified in THRM_DTY starts immediately (no 2 second delay), and no SMI# is generated.
7:5	**THRM_DTY.** This write-once 3-bit field determines the duty cycle of the throttling when the thermal override condition occurs. The duty cycle indicates the approximate percentage of time the STPCLK# signal is asserted while in the throttle mode. The STPCLK# throttle period is 1024 PCICLKs. Note that the throttling only occurs if the system is in the C0 state. If in the C2 state, no throttling occurs. There is no enable bit for thermal throttling, because it should not be disabled. Once the THRM_DTY field is written, any subsequent writes will have no effect until PCIRST# goes active. **THRM_DTY** / **Throttle Mode** / **PCI Clocks** 000 / RESERVED (Default) (Will be 50%) / 512 001 / 87.5% / 896 010 / 75.0% / 768 011 / 62.5% / 640 100 / 50% / 512 101 / 37.5% / 384 110 / 25% / 256 111 / 12.5% / 128
4	**THTL_EN.** When set and the system is in a C0 state, it enables a processor-controlled STPCLK# throttling. The duty cycle is selected in the THTL_DTY field. 0 = Disable. 1 = Enable.
3:1	**THTL_DTY.** This 3-bit field determines the duty cycle of the throttling when the THTL_EN bit is set. The duty cycle indicates the approximate percentage of time the STPCLK# signal is asserted (low) while in the throttle mode. The STPCLK# throttle period is 1024 PCICLKs. **THTL_DTY** / **Throttle Mode** / **PCI Clocks** 000 / RESERVED (Default) (Will be 50%) / 512 001 / 87.5% / 896 010 / 75.0% / 768 011 / 62.5% / 640 100 / 50% / 512 101 / 37.5% / 384 110 / 25% / 256 111 / 12.5% / 128
0	Reserved.

9.8.3.6 LV2—Level 2 Register

I/O Address:	PMBASE + 14h ***(ACPI P_BLK+4)***	Attribute:	RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Bit	Description
7:0	Reads to this register return all zeros, writes to this register have no effect. Reads to this register generate a “enter a level 2 power state” (C2) to the clock control logic. This will cause the STPCLK# signal to go active, and stay active until a break event occurs. Throttling (due either to THTL_EN or THRM# override) will be ignored.

9.8.3.7 GPE0_STS—General Purpose Event 0 Status Register

I/O Address:	PMBASE + 28h (ACPI GPE0_BLK)	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI
Power Well:	Resume		

Note: This register is symmetrical to the General Purpose Event 0 Enable Register. If the corresponding _EN bit is set, then when the _STS bit get set, the ICH3 generates a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the ICH3 also generates an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set. There will be no SCI/SMI# or wake event on THRMOR_STS since there is no corresponding _EN bit. None of these bits are reset by CF9h write. All are reset by RSMRST#.

Bit	Description
15:14	Reserved.
13	**PME_B0_STS**—R/W. 0 = The default for this bit is 0. Writing a 1 to this bit clears this bit. 1 = Set to 1 by the ICH3 when any internal device on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN bit is set and the system is in an S0 state, the setting of the PME_B0_STS bit generates an SCI (or SMI# if SCI_EN is not set). If the PME_B0_STS bit is set and the system is in an S1–S4 state (or S5 state due to SLP_TYP and SLP_EN), the setting of the PME_B0_STS bit generates a wake event, and an SCI (or SMI# if SCI_EN is not set) is generated. If the system is in an S5 state due to power button override, the PME_B0_STS bit does not cause a wake event or SCI.
12	**USB3_STS**—R/W 0 = Disable. 1 = Set by hardware and can be reset by writing a one to this bit position or a resume-well reset. This bit is set when USB 1.1 Controller #3 needs to cause a wake. Additionally if the USB3_EN bit is set, the setting of the USB3_STS bit will generate a wake event.
11	**PME_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when the PME# signal goes active. Additionally, if the PME_EN bit is set, and the system is in an S0 state, then the setting of the PME_STS bit will generate an SCI or SMI# (if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S1-S4 state (or S5 state due to setting SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event, and an SCI will be generated. If the system is in an S5 state due to power button override or a power failure, then PME_STS will not cause a wake event or SCI.
10:9	Reserved.

Bit	Description
8	**RI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when the RI# input signal goes active.
7	**SMBus Wake Status (SMB_WAK_STS)**—R/WC. The SMBus controller can independently cause an SMI# or SCI, so this bit does not need to do so (unlike the other bits in this register). 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware to indicate that the wake event was caused by the ICH3's SMBus logic.This bit will be set by the WAKE/SMI# command type, even if the system is already awake. The SMI handler should then clear this bit. **NOTE:** This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state.
6	**TCOSCI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when the TCO logic causes an SCI.
5	**AC97_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when the codecs are attempting to wake the system. The AC97_STS bit gets set only from the following two cases: 1. ACSDIN[1] or ACSDIN[0] is high and BITCLK is not oscillating, or 2. The GSCI bit is set (section 13.2.9, NAMBAR +30h, bit 0).
4	**USB2_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when USB Controller 2 needs to cause a wake. Wake event will be generated if the corresponding USB2_EN bit is set.
3	**USB1_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware when USB Controller 1 needs to cause a wake. Wake event will be generated if the corresponding USB1_EN bit is set.
2	Reserved.
1	**Thermal Interrupt Override Status (THRMOR_STS)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = This bit is set by hardware anytime a thermal over-ride condition occurs and starts throttling the processor's clock at the THRM_DTY ratio. This will not cause an SMI#, SCI, or wake event.
0	**Thermal Interrupt Status (THRM_STS)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by hardware anytime the THRM# signal is driven active as defined by the THRM_POL bit. Additionally, if the THRM_EN bit is set, then the setting of the THRM_STS bit will also generate a power management event (SCI or SMI#).

9.8.3.8 GPE0_EN—General Purpose Event 0 Enables Register

I/O Address:	PMBASE + 2Ah ***(ACPI GPE0_BLK + 2)***	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI
Power Well:	Bits 0–7 Resume, Bits 8–15 RTC		

Note: This register is symmetrical to the General Purpose Event 0 Status Register. All the bits in this register should be cleared to 0 based on a Power Button Override. The resume well bits are all cleared by RSMRST#. The RTC sell bits are cleared by RTCRST#.

Bit	Description
15:14	Reserved.
13	**PME_B0_EN**—R/W. Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. PME_B0_STS can be a wake event from the S1–S4 states, or from S5 (if entered via SLP_TYP and SLP_EN) or power failure, but not Power Button Override. This bit defaults to 0. It is only cleared by Software or RTCRST#. It is not cleared by CF9h writes.
12	**USB3_EN**—R/W. 0 = Disable. 1 = Enable the setting of the USB3_STS bit to generate a wake event. The USB3_STS bit is set when USB 1.1 Controller #3 signals a wake event. Break events are handled via the USB interrupt.
11	**PME_EN**—R/W. 0 = Disable. 1 = Enables the setting of the PME_STS to generate a wake event and/or an SCI. PME# can be a wake event from the S1–S4 state or from S5 (if entered via SLP_EN, but not power button override).
10:9	Reserved.
8	**RI_EN**—R/W. The value of this bit will be maintained through a G3 state and is not affected by a hard reset caused by a CF9h write. 0 = Disable. 1 = Enables the setting of the RI_STS to generate a wake event.
7	Reserved.
6	**TCOSCI_EN**—R/W. 0 = Disable. 1 = Enables the setting of the TCOSCI_STS to generate an SCI.
5	**AC97_EN**—R/W. 0 = Disable. 1 = Enables the setting of the AC97_STS to generate a wake event.
4	**USB2_EN**—R/W. 0 = Disable. 1 = Enables the setting of the USB2_STS to generate a wake event.
3	**USB1_EN**—R/W. 0 = Disable. 1 = Enables the setting of the USB1_STS to generate a wake event.
2	**THRM#_POL**—R/W. This bit controls the polarity of the THRM# pin needed to set the THRM_STS bit. 0 = Low value on the THRM# signal will set the THRM_STS bit. 1 = HIGH value on the THRM# signal will set the THRM_STS bit.
1	Reserved.
0	**THRM_EN**—R/W. 0 = Disable. 1 = Active assertion of the THRM# signal (as defined by the THRM_POL bit) will set the THRM_STS bit and generate a power management event (SCI or SMI).

9.8.3.9 GPE1_STS—General Purpose Event 1 Status Register

I/O Address:	PMBASE + 2Ch ***(ACPI GPE1_BLK)***	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI
Power Well:	Resume		

Note: This register is symmetrical to the General Purpose Event 1 Enable Register. GPIOs that are not implemented will not have the corresponding bits implemented in this register.

Bit	Description
15:0	**GPI[n]_STS**—R/WC. 0 = Software clears each bit by writing a 1 to the bit position when the corresponding GPIO signal is not active. (The status bit cannot be cleared while the corresponding signal is still active). 1 = These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is low (or high if the corresponding GP_INV bit is set). If the corresponding GPI[n]_EN bit is set in the GPE1_EN register, and the GPI[n]_STS bit is set, then: - If the system is in an S1_S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SMI# or SCI will be generated, depending on the GPI_ROUT bits for the corresponding GPI.

9.8.3.10 GPE1_EN—General Purpose Event 1 Enable Register

I/O Address:	PMBASE + 2Eh *(ACPI GPE1_BLK + 2)*	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI
Power Well:	Resume		

Note: This register is symmetrical to the General Purpose Event 1 Status Register. GPIOs that are not implemented will not have the corresponding bits implemented in this register. All of the bits in this register will be cleared by RSMRST#. The ICH3 uses the same GPE1_EN register (I/O address: PMBase+2Eh) to enable/disable both SMI and ACPI SCI general purpose input events. APCI OS assumes that it owns the entire GPE1_EN register per ACPI spec. Problems arise when some of the general-purpose inputs are enabled as SMI by BIOS, and some of the general purpose inputs are enabled for SCI. In this case ACPI OS turns off the enabled bit for any GPIx input signals that are not indicated as SCI general-purpose events at boot, and exit from sleeping states. BIOS should define a dummy control method which prevents the ACPI OS from clearing the SMI GPE1_EN bits.

Bit	Description
15:0	**GPI[n]_EN**—R/W. 0 = Disable. 1 = Enable the corresponding GPI[n]_STS bit being set to cause an SMI#, SCI, and/or wake event.

9.8.3.11 SMI_EN—SMI Control and Enable Register

I/O Address:	PMBASE + 30h	Attribute:	R/W
Default Value:	0000h	Size:	32 bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Bit	Description
31:15	Reserved.
14	**PERIODIC_EN**—R/W. 0 = Disable. 1 = Enables the ICH3 to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register.
13	**TCO_EN**—R/W. 0 = Disables TCO logic generating an SMI#. Note that if the NMI2SMI_EN bit is set, SMIs that are caused by re-routed NMIs will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, NMIs will still be routed to cause SMIs. 1 = Enables the TCO logic to generate SMI#.
12	Reserved.
11	**Microcontroller SMI Enable (MCSMI_EN)**—R/W. 0 = Disable. 1 = Enables ICH3 to trap accesses to the microcontroller range (62h or 66h) and generate an SMI#. Note that 'trapped' cycles will be claimed by the ICH3 on PCI, but not forwarded to LPC.
10:8	Reserved.
7	**BIOS Release (BIOS_RLS)**—WO. 0 = This bit will always return 0 on reads. Writes of 0 to this bit have no effect. 1 = Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software.
6	**Software SMI# Timer Enable (SWSMI_TMR_EN)**—R/W. 0 = Disable. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. 1 = Starts Software SMI# Timer. When the SWSMI timer expires (the timeout period depends upon the SWSMI_RATE_SEL bit setting), SWSMI_TMR_STS is set and an SMI# is generated. SWSMI_TMR_EN stays set until cleared by software.
5	**APMC_EN**—R/W. 0 = Disable. Writes to the APM_CNT register will not cause an SMI#. 1 = Enables writes to the APM_CNT register to cause an SMI#.
4	**SLP_SMI_EN**—R/W. 0 = Disables the generation of SMI# on SLP_EN. Note that this bit must be 0 before the software attempts to transition the system into a sleep state by writing a 1 to the SLP_EN bit. 1 = A write of 1 to the SLP_EN bit (bit 13 in PM1_CNT register) will generate an SMI#, and the system will not transition to the sleep state based on that write to the SLP_EN bit.
3	**LEGACY_USB_EN**—R/W. 0 = Disable. 1 = Enables legacy USB circuit to cause SMI#.
2	**BIOS_EN**—R/W. 0 = Disable. 1 = Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit.
1	**End of SMI (EOS)**—R/W (special). This bit controls the arbitration of the SMI signal to the processor. This bit must be set for the ICH3 to assert SMI# low to the processor. 0 = Once the ICH3 asserts SMI# low, the EOS bit is automatically cleared. 1 = When this bit is set, SMI# signal will be deasserted for 4 PCI clocks before its assertion. In the SMI handler, the processor should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to re-assert SMI upon detection of an SMI event and the setting of a SMI status bit.
0	**GBL_SMI_EN**—R/W. 0 = No SMI# will be generated by ICH3. This bit is reset by a PCI reset event. 1 = Enables the generation of SMI# in the system upon any enabled SMI event.

9.8.3.12 SMI_STS—SMI Status Register

I/O Address:	PMBASE + 34h	Attribute:	R/W
Default Value:	0000h	Size:	32-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Note: If the corresponding _EN bit is set when the _STS bit is set, the ICH3 will cause an SMI# (except bits 8–10 and 12, which do not need enable bits since they are logic ORs of other registers that have enable bits).

Bit	Description
31:17	Reserved.
16	**SMBus SMI Status (SMBUS_SMI_STS)**—R/WC. 0 = This bit is cleared by writing a 1 to its bit position. This bit is set from the 64 kHz clock domain used by the SMBus. Software must wait at least 15.63 µs after the initial assertion of this bit before clearing it. 1 = Indicates that the SMI# was caused by: • The SMBus Slave receiving a message, or • The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or • The SMBus Slave receiving a Host Notify message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or • The ICH3 detecting the SMLINK_SLAVE_SMI command while in the S0 state.
15	**SERIRQ_SMI_STS**—RO. 0 = SMI# was not caused by SERIRQ decoder. This is not a sticky bit. 1 = Indicates that the SMI# was caused by the SERIRQ decoder.
14	**PERIODIC_STS**—R/WC. 0 = This bit is cleared by writing a 1 to its bit position. 1 = This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the ICH3 will generate an SMI#.
13	**TCO_STS**—RO. 0 = SMI# not caused by TCO logic. 1 = Indicates the SMI# was caused by the TCO logic. Note that this is not a wake event.
12	**Device Monitor Status (DEVMON_STS)**—RO. 0 = SMI# not caused by Device Monitor. 1 = Set under any of the following conditions: - Any of the DEV[7:4]_TRAP_STS bits are set and the corresponding DEV[7:4]_TRAP_EN bits are also set. - Any of the DEVTRAP_STS bits are set and the corresponding DEVTRAP_EN bits are also set.
11	**Microcontroller SMI# Status (MCSMI_STS)**—R/WC. 0 = Indicates that there has been no access to the power management microcontroller range (62h or 66h). This bit is cleared by software writing a 1 to the bit position. 1 = Set if there has been an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the ICH3 will generate an SMI#.
10	**GPE1_STS**—RO. This bit is a logical OR of the bits in the GPE1_STS register that are also set up to cause an SMI# (as indicated by the GPI_ROUT registers) and have the corresponding bit set in the GPE1_EN register. Bits that are not routed to cause an SMI# will have no effect on the GPE1_STS bit. 0 = SMI# was not generated by a GPI assertion. 1 = SMI# was generated by a GPI assertion.
9	**GPE0_STS**—RO. This bit is a logical OR of the bits in the GPE0_STS register that also have the corresponding bit set in the GPE0_EN register. 0 = SMI# was not generated by a GPE0 event. 1 = SMI# was generated by a GPE0 event.

Bit	Description
8	**PM1_STS_REG**—RO. This is an ORs of the bits in the ACPI PM1 Status Register (offset PMBASE+00h) that can cause an SMI#. 0 = SMI# was not generated by a PM1_STS event. 1 = SMI# was generated by a PM1_STS event.
7	Reserved.
6	**SWSMI_TMR_STS**—R/WC. 1 = Set by the hardware when the Software SMI# Timer expires. 0 = Software clears this bit by writing a 1 to the bit location.
5	**APM_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = SMI# was generated by a write access to the APM control register with the APMC_EN bit set.
4	**SLP_SMI_STS**—R/WC. 1 = Indicates an SMI# was caused by a write of 1 to SLP_EN bit when SLP_SMI_EN bit is also set. 0 = Software clears this bit by writing a 1 to the bit location.
3	**LEGACY_USB_STS**—RO. This bit is a logical OR of each of the SMI status bits in the USB Legacy Keyboard/Mouse Control Registers ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. 0 = SMI# was not generated by USB Legacy event. 1 = SMI# was generated by USB Legacy event.
2	**BIOS_STS**—R/WC. 0 = This bit cleared by software writing a 1 to its bit position. 1 = SMI# was generated due to ACPI software requesting attention (writing a 1 to the GBL_RLS bit with the BIOS_EN bit set).
1:0	Reserved.

9.8.3.13 MON_SMI—Device Monitor SMI Status and Enable Register

I/O Address:	PMBASE +40h	Attribute:	R/W, R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Bit	Description
15:12	**DEV[7:4]_TRAP_STS**—R/WC. Bit 12 corresponds to Monitor 4, bit 13 corresponds to Monitor 5 etc. 0 = SMI# was not caused by the associated device monitor. 1 = SMI# was caused by an access to the corresponding device monitor's I/O range.
11:8	**DEV[7:4]_TRAP_EN**—R/W. Bit 8 corresponds to Monitor 4, bit 9 corresponds to Monitor 5 etc. 0 = Disable. 1 = Enables SMI# due to an access to the corresponding device monitor's I/O range.
7:0	Reserved.

9.8.3.14 DEVACT_STS—Device Activity Status Register

I/O Address:	PMBASE +44h	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

This register is used in conjunction with the Periodic SMI# timer to detect any system activity for legacy power management.

Bit	Description
15:14	Reserved.
13	**ADLIB_ACT_STS**—R/WC. Ad-Lib. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
12	**KBC_ACT_STS**—R/WC. KBC (60/64h). 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
11	**MIDI_ACT_STS**—R/WC. MIDI. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
10	**AUDIO_ACT_STS**—R/WC. Audio (Sound Blaster "OR'd" with MSS). 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
9	**PIRQDH_ACT_STS**—R/WC. PIRQ[D or H]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
8	**PIRQCG_ACT_STS**—R/WC. PIRQ[C or G]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
7	**PIRQBF_ACT_STS**—R/WC. PIRQ[B or F]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
6	**PIRQAE_ACT_STS**—R/WC. PIRQ[A or E]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
5	**LEG_ACT_STS**—R/WC. Parallel Port, Serial Port 1, Serial Port 2, Floppy Disk Controller. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
4	Reserved.
3	**IDES1_ACT_STS**—R/WC. IDE Secondary Drive 1. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
2	**IDES0_ACT_STS**—R/WC. IDE Secondary Drive 0. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
1	**IDEP1_ACT_STS**—R/WC. IDE Primary Drive 1. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
0	**IDEP0_ACT_STS**—R/WC. IDE Primary Drive 0. 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.

9.8.3.15 DEVTRAP_EN— Device Trap Enable Register

I/O Address:	PMBASE +48h	Attribute:	R/W
Default Value	0000h	Size:	16-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

This register enables the individual trap ranges to generate an SMI# when the corresponding status bit in the DEVACT_STS register is set. When a range is enabled, I/O cycles associated with that range will not be forwarded to LPC or IDE.

Bit	Description
15:14	Reserved.
13	**ADLIB_TRP_EN**—R/W. Ad-Lib. 0 = Disable. 1 = Enable.
12	**KBC_TRP_EN**—R/W. KBC (60/64h). 0 = Disable. 1 = Enable.
11	**MIDI_TRP_EN**—R/W. MIDI. 0 = Disable. 1 = Enable.
10	**AUDIO_TRP_EN**—R/W. Audio (Sound Blaster “OR’d” with MSS). 0 = Disable. 1 = Enable.
9:6	Reserved.
5	**LEG_IO_TRP_EN**—R/W. Parallel Port, Serial Port 1, Serial Port 2, Floppy Disk Controller. 0 = Disable. 1 = Enable.
4	Reserved.
3	**IDES1_TRP_EN**—R/W. IDE Secondary Drive 1. 0 = Disable. 1 = Enable.
2	**IDES0_TRP_EN**—R/W. IDE Secondary Drive 0. 0 = Disable. 1 = Enable.
1	**IDEP1_TRP_EN**—R/W. IDE Primary Drive 1. 0 = Disable. 1 = Enable.
0	**IDEP0_TRP_EN**—R/W. IDE Primary Drive 0. 0 = Disable. 1 = Enable.

9.8.3.16 BUS_ADDR_TRACK— Bus Address Tracker Register

I/O Address:	PMBASE +4Ch	Attribute:	RO
Lockable:	No	Size:	16-bit
Power Well:	Core	Usage:	Legacy Only

This register could be used by the SMI# handler to assist in determining what was the last cycle from the processor. BUS_ADDR_TRACK may not contain “expected” last I/O cycle data if Asynchronous SMIs and Synchronous SMIs are occurring simultaneously. This register only reports “expected” last I/O cycle data if Asynchronous SMIs are disabled.

Bit	Description
15:0	Corresponds to the low 16 bits of the last I/O cycle, as would be defined by the PCI AD[15:0] signals on the PCI bus (even though it may not be a real PCI cycle). The value is latched based on SMI# active. This functionality is useful for figuring out which I/O was last being accessed.

9.8.3.17 BUS_CYC_TRACK— Bus Cycle Tracker Register

I/O Address:	PMBASE +4Eh	Attribute:	RO
Lockable:	No	Size:	8-bit
Power Well:	Core	Usage:	Legacy Only

This register could be used by the SMM handler to assist in determining what was the last cycle from the processor. BUS_CYC_TRACK may not contain “expected” last I/O cycle data if Asynchronous SMIs and Synchronous SMIs are occurring simultaneously. This register only reports “expected” last I/O cycle data if Asynchronous SMIs are disabled.

Bit	Description
7:4	Corresponds to the byte enables, as would be defined by the PCI C/BE# signals on the PCI bus (even though it may not be a real PCI cycle). The value is latched based on SMI# going active.
3:0	Corresponds to the cycle type, as would be defined by the PCI C/BE# signals on the PCI bus (even though it may not be a real PCI cycle). The value is latched based on SMI# going active.

9.9 System Management TCO Registers (D31:F0)

The TCO logic is accessed via registers mapped to the PCI configuration space (Device 31:Function 0) and the system I/O space. For TCO PCI Configuration registers, see LPC Device 31:Function 0 PCI Configuration registers.

9.9.1 TCO Register I/O Map

The TCO I/O registers reside in a 32-byte range pointed to by a TCOBASE value, which is, ACPIBASE + 60h in the PCI configuration space. Table 9-11 shows the mapping of the registers within that 32-byte range.

Table 9-11. TCO I/O Register Map

Offset	Register Name: Function	Type
00h	TCO_RLD: TCO Timer Reload and Current Value	R/W
01h	TCO_TMR: TCO Timer Initial Value	R/W
02h	TCO_DAT_IN: TCO Data In	R/W
03h	TCO_DAT_OUT: TCO Data Out	R/W
04h–05h	TCO1_STS: TCO Status	R/W
06h–07h	TCO2_STS: TCO Status	R/W
08h–09h	TCO1_CNT: TCO Control	R/W
0Ah–0Bh	TCO2_CNT: TCO Control	R/W
0Ch–0Dh	TCO_MESSAGE1, TCO_MESSAGE2: Used by BIOS to indicate POST/Boot progress	R/W
0Eh	TCO_WDSTATUS: Watchdog Status Register	R/W
0Fh	Reserved	RO
10h	SW_IRQ_GEN: Software IRQ Generation Register	R/W
11h–1Fh	Reserved	RO

9.9.2 TCO1_RLD—TCO Timer Reload and Current Value Register

I/O Address:	TCOBASE +00h	Attribute:	R/W
Default Value:	0000h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout. Bits 7:6 will always be 0.

9.9.3 TCO1_TMR—TCO Timer Initial Value Register

I/O Address:	TCOBASE +01h	Attribute:	R/W
Default Value:	0004h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:6	Reserved.
5:0	Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0h–3h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and this allows timeouts ranging from 2.4 seconds to 38 seconds.

9.9.4 TCO1_DAT_IN—TCO Data In Register

I/O Address:	TCOBASE +02h	Attribute:	R/W
Default Value:	0000h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Data Register for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the OS_TCO_SMI bit in the TCO_STS register.

9.9.5 TCO1_DAT_OUT—TCO Data Out Register

I/O Address:	TCOBASE +03h	Attribute:	R/W
Default Value:	0000h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Data Register for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It will also cause an interrupt, as selected by the TCO_INT_SEL bits.

9.9.6 TCO1_STS—TCO1 Status Register

I/O Address:	TCOBASE +04h	Attribute:	R/WC, RO
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core (Except bit 7 in RTC)

Bit	Description
15:13	Reserved.
12	**HUBSERR_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = ICH3 received an SERR# message via the hub interface. The software must read the memory controller hub (or its equivalent) to determine the reason for the SERR#. **NOTE:** If this bit is set AND the SERR_EN bit in CMD Register (D30:F0, Offset 04h, bit 8) is also set, the ICH3 will set the SSE bit in SECSTS Register (D30:F0, offset 1Eh, bit 14) AND will also generate an NMI (or SMI# if NMI routed to SMI#).
11	**HUBNMI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = ICH3 received an NMI message via the hub interface. The software must read the memory controller hub (or its equivalent) to determine the reason for the NMI. .
10	**HUBSMI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = ICH3 received an SMI message via the hub interface. The software must read the memory controller hub (or its equivalent) to determine the reason for the SMI#.
9	**HUBSCI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = ICH3 received an SCI message via the hub interface. The software must read the memory controller hub (or its equivalent) to determine the reason for the SCI.
8	**BIOSWR_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = ICH3 sets this bit and generates and SMI# to indicate an illegal attempt to write to the BIOS. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the BLD bit is also set, or b) any write is attempted to the BIOS and the BIOSWP bit is also set. **NOTE:** On write cycles attempted to the 4MB lower alias to the BIOS space, the BIOSWR_STS will not be set.
7	**NEWCENTURY_STS**—R/WC. This bit is in the RTC well. 0 = Cleared by writing a 1 to the bit position or by RTCRST# going active. 1 = This bit is set when the Year byte (RTC I/O space, index offset 09h) rolls over from 99 to 00. Setting this bit will cause an SMI# (but not a wake event). Note that the NEWCENTURY_STS bit is not valid when the RTC battery is first installed (or when RTC power has not been maintained). Software can determine if RTC power has not been maintained by checking the RTC_PWR_STS bit, or by other means (such as a checksum on RTC RAM). If RTC power is determined to have not been maintained, BIOS should set the time to a legal value and then clear the NEWCENTURY_STS bit. The NEWCENTURY_STS bit may take up to 3 RTC clocks for the bit to be cleared after a “1” is written to the bit to clear it. After writing a “1” to this bit, software should not exit the SMI handler until verifying that the bit has actually been cleared. This will ensure that the SMI is not re-entered.
6:4	Reserved.
3	**TIMEOUT**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Set by ICH3 to indicate that the SMI was caused by the TCO timer reaching 0.
2	**TCO_INT_STS**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = SMI handler caused the interrupt by writing to the TCO_DAT_OUT register.

Bit	Description
1	**SW_TCO_SMI**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Software caused an SMI# by writing to the TCO_DAT_IN register.
0	**NMI2SMI_STS**—RO. 0 = Cleared by clearing the associated NMI status bit. 1 = Set by the ICH3 when an SMI# occurs because an event occurred that would otherwise have caused an NMI (because NMI2SMI_EN is set).

9.9.7 TCO2_STS—TCO2 Status Register

I/O Address:	TCOBASE +06h	Attribute:	R/WC, RO
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Resume (Except Bit 0, in RTC)

Bit	Description
15:5	Reserved.
4	**SMLink Slave SMI Status (SMLINK_SLV_SMI_STS)**—R/W. (Allow the software to go directly into pre-determined sleep state. This avoids race conditions. 0 = The bit is reset by RSMRST#, but not due to the PCI Reset associated with exit from S3–S5 states. 1 = ICH3 sets this bit to 1 when it receives the SMI message on the SMLink's Slave Interface. Software clears the bit by writing a 1 to this bit position.
3	Reserved.
2	**BOOT_STS.** 0 = Cleared by ICH3 based on RSMRST# or by software writing a 1 to this bit. Note that software should first clear the SECOND_TO_STS bit before writing a 1 to clear the BOOT_STS bit. 1 = Set to 1 when the SECOND_TO_STS bit goes from 0 to 1 and the processor has not fetched the first instruction. **NOTE:** If rebooting due to a second TCO timer timeout, and if the BOOT_STS bit is set, the ICH3 will reboot using the 'safe' multiplier (1111). This allows the system to recover from a processor frequency multiplier that is too high, and allows the BIOS to check the BOOT_STS bit at boot. If the bit is set and the frequency multiplier is 1111, then the BIOS knows that the processor has been programmed to an illegal multiplier.
1	**SECOND_TO_STS**—R/WC. 0 = This bit is cleared by writing a 1 to the bit position or by a RSMRST#. 1 = The ICH3 sets this bit to a 1 to indicate that the TCO timer timed out a second time (probably due to system lock). If this bit is set and the NO_REBOOT configuration bit is 0, then the ICH3 will reboot the system after the second timeout. The reboot is done by asserting PCIRST#. 0 =
0	**Intruder Detect (INTRD_DET)**—R/WC. 0 = This bit is only cleared by writing a 1 to the bit position, or by RTCRST# assertion. 1 = Set by ICH3 to indicate that an intrusion was detected. This bit is set even if the system is in G3 state.

9.9.8 TCO1_CNT—TCO1 Control Register

I/O Address:	TCOBASE +08h	Attribute:	R/W, R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:12	Reserved.
11	**TCO Timer Halt (TCO_TMR_HLT)**—R/W. 0 = The TCO Timer is enabled to count. 1 = The TCO Timer will halt. It will not count, and thus cannot reach a value that will cause an SMI# or set the SECOND_TO_STS bit. When set, this bit will prevent rebooting and prevent Alert On LAN event messages from being transmitted on the SMLINK (but not Alert On LAN* heartbeat messages).
10	**SEND_NOW**—R/W (special). 0 = The ICH will clear this bit when it has completed sending the message. Software must not set this bit to 1 again until the ICH has set it back to 0. 1 = Writing a 1 to this bit will cause the ICH to send an Alert On LAN Event message over the SMLINK interface, with the Softwware Event bit set. Setting the SEND_NOW bit causes the ICH3 integrated LAN Controller to reset, which can have unpredictable side-effects. Unless software protects against these side effects, software should not attempt to set this bit.
9	**NMI2SMI_EN**—R/W. 0 = Normal NMI functionality. 1 = Forces all NMIs to instead cause SMIs. The functionality of this bit is dependent upon the settings of the NMI_EN bit and the GBL_SMI_EN bit as detailed in the following table: **NMI_EN / GBL_SMI_EN / Description** 0 / 0 / No SMI# at all because GBL_SMI_EN = 0 0 / 1 / SMI# will be caused due to NMI events 1 / 0 / No SMI# at all because GBL_SMI_EN = 0 1 / 1 / No SMI# due to NMI because NMI_EN = 1
8	**NMI_NOW**—R/WC. 0 = This bit is cleared by writing a 1 to the bit position. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared. 1 = Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force an entry to the NMI handler.
7:0	Reserved.

9.9.9 TCO2_CNT—TCO2 Control Register

I/O Address:	TCOBASE +0Ah	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Resume

Bit	Description
15:4	Reserved.
3	**GPIO11_ALERT_DISABLE**—R/W. Disable GPIO11/SMBALERT# as an alert source for the heartbeats and the SMBus slave. At reset (via RSMRST# asserted) this bit is set and GPIO[11] alerts are disabled.
2:1	**INTRD_SEL**—R/W. Selects the action to take if the INTRUDER# signal goes active. 00 = No interrupt or SMI#. 01 = Interrupt (as selected by TCO_INT_SEL). 10 = SMI. 11 = Reserved.
0	Reserved.

9.9.10 TCO_MESSAGE1 and TCO_MESSAGE2 Registers

I/O Address:	TCOBASE +0Ch (Message 1) TCOBASE +0Dh (Message 2)	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Resume

Bit	Description
7:0	**TCO_MESSAGE[*n*]**—R/W.The value written into this register will be sent out via the SMLINK interface in the MESSAGE field of the Alert On LAN message. BIOS can write to this register to indicate its boot progress which can be monitored externally.

9.9.11 TCO_WDSTATUS—TCO2 Control Register

Offset Address:	TCOBASE + 0Eh	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Power Well:	Resume		

Bit	Description
7:0	**Watchdog Status (WDSTATUS)**—R/W. The value written to this register will be sent in the Alert On LAN message on the SMLINK interface. It can be used by the BIOS or system management software to indicate more details on the boot progress. This register will be reset to the default of 00h based on RSMRST# (but not PCI reset).

9.9.12 SW_IRQ_GEN—Software IRQ Generation Register

Offset Address:	TCOBASE + 10h	Attribute:	R/W
Default Value:	03h	Size:	8 bits
Power Well:	Resume		

Bit	Description
7:2	Reserved.
1	**IRQ12_CAUSE**—R/W. The state of this bit is logically ANDed with the IRQ12 signal as received by the ICH3's SERIRQ logic. This bit must be a "1" (default) if the ICH3 is expected to receive IRQ12 assertions from a SERIRQ device.
0	**IRQ1_CAUSE**—R/W. The state of this bit is logically ANDed with the IRQ1 signal as received by the ICH3's SERIRQ logic. This bit must be a "1" (default) if the ICH3 is expected to receive IRQ1 assertions from a SERIRQ device.

9.10 General Purpose I/O Registers (D31:F0)

The control for the general purpose I/O signals is handled through a separate 64-byte I/O space. The base offset for this space is selected by the GPIO_BAR register. Table 9-12 summarizes the ICH3 GPIO implementation.

Table 9-12. Summary of GPIO Implementation

GPIO	Type	Alternate Function (Note 1)	Power Well	Notes
GPIO[0]	Input Only	REQ[A]#	Core	GPIO_USE_SEL bit 0 enables REQ/GNT[A]# pair. Input active status read from GPE1_STS register bit 0. Input active high/low set through GPI_INV register bit 0.
GPIO[1]	Input Only	REQ[B]# or REQ[5]#	Core	GPIO_USE_SEL bit 1 enables REQ/GNT[B]# pair (See note 4). Input active status read from GPE1_STS register bit 1. Input active high/low set through GPI_INV register bit 1.
GPIO[2:5]	Input Only	PIRQ[E:H]#	Core	GPIO_USE_SEL bits [2:5] enable PIRQ[E:H]#. Input active status read from GPE1_STS reg. bits [2:5]. Input active high/low set through GPI_INV reg. bit [2:5].
GPIO[6]	Input Only	Unmuxed	Core	Input active status read from GPE1_STS register bit 6. Input active high/low set through GPI_INV register bit 6.
GPIO[7]	Input Only	Unmuxed	Core	Input active status read from GPE1_STS register bit 7. Input active high/low set through GPI_INV register bit 7
GPIO[8]	Input Only	Unmuxed	Resume	Input active status read from GPE1_STS register bit 8. Input active high/low set through GPI_INV register bit 8.
GPIO[9:10]	N/A	N/A	N/A	Not implemented
GPIO[11]	Input Only	SMBALERT#	Resume	GPIO_USE_SEL bit 11 enables SMBALERT# Input active status read from GPE1_STS register bit 11. Input active high/low set through GPI_INV register bit 11.
GPIO[12]	Input Only	Unmuxed	Resume	Input active status read from GPE1_STS register bit 12. Input active high/low set through GPI_INV register bit 12.
GPIO[13]	Input Only	Unmuxed	Resume	Input active status read from GPE1_STS register bit 13. Input active high/low set through GPI_INV register bit 13.
GPIO[14:15]	N/A	N/A	N/A	Not Implemented
GPIO[16]	Output Only	GNT[A]#	Core	Output controlled via GP_LVL register bit 16. TTL driver output
GPIO[17]	Output Only	GNT[B]# or GNT[5]#	Core	Output controlled via GP_LVL register bit 17. TTL driver output
GPIO[18:19]	Output Only	Unmuxed	Core	Output controlled via GP_LVL register bits [18:19]. TTL driver output
GPIO[20]	Output Only	Unmuxed	Core	Output controlled via GP_LVL register bit 20. TTL driver output
GPIO[21]	Output Only	Unmuxed	Core	This GPO defaults high. Output controlled via GP_LVL register bit 21. TTL driver output
GPIO[22]	Output Only	Unmuxed	Core	Output controlled via GP_LVL register bit [22]. Open-drain output
GPIO[23	Output Only	Unmuxed	Core	Output controlled via GP_LVL register bit [23]. TTL driver output

Table 9-12. Summary of GPIO Implementation (Continued)

GPIO	Type	Alternate Function (Note 1)	Power Well	Notes
GPIO[24]	Input / Output	Unmuxed	Resume	Input active status read from GP_LVL register bit 24. Output controlled via GP_LVL register bit 24. TTL driver output
GPIO[25]	Input / Output	Unmuxed	Resume	Blink enabled via GPO_BLINK register bit 25. Input active status read from GP_LVL register bit 25 Output controlled via GP_LVL register bit 25. TTL driver output
GPIO[26]	N/A	N/A	N/A	Not implemented
GPIO[27:28]	Input / Output	Unmuxed	Resume	Input active status read from GP_LVL register bits [27:28] Output controlled via GP_LVL register bits [27:28] TTL driver output
GPIO[29:31]	N/A	N/A	N/A	Not implemented
GPIO[32:43]	I/O	Unmuxed	Core	Input active status read from GP_LVL2 register bits [32:43]. Output controlled via GP_LVL2 register bits [32:43]
GPIO[44:48]	I/O	Unmuxed		Not implemented

NOTES:
1. All GPIOs default to their alternate function.
2. All inputs are sticky. The status bit will remain set as long as the input was asserted for 2 clocks. GPIs are sampled on PCI clocks in S0/S1. GPIs are sampled on RTC clocks in S3/S4/S5.
3. GPIO[0:7] are 5V tolerant, and all GPIs can be routed to cause an SCI or SMI#
4. If GPIO_USE_SEL bit 1 is set to 1 and GEN_CNT bit 25 is also set to 1 then REQ/GNT[5]# is enabled. See Section 9.1.22.

9.10.1 GPIO Register I/O Address Map

Table 9-13. Registers to Control GPIO

Offset	Mnemonic	Register Name	Default	Type
General Registers				
00–03h	GPIO_USE_SEL	GPIO Use Select	1A003180h	R/W
04–07h	GP_IO_SEL	GPIO Input/Output Select	0000 FFFFh	R/W
08–0Bh	—	Reserved	00h	RO
0C–0Fh	GP_LVL	GPIO Level for Input or Output	1F1F 0000h	R/W
10–13h	—	Reserved	00h	RO
Output Control Registers				
14–17h	GPO_TTL	GPIO TTL Select	06630000h	RO
18–1Bh	GPO_BLINK	GPIO Blink Enable	00000000h	R/W
1C–1Fh		Reserved	0	RO
Input Control Registers				
20–2Bh	—	Reserved	00000000h	RO
2C–2Fh	GPI_INV	GPIO Signal Invert	00000000h	R/W
30–33h	GPIO_USE_SEL2	GPIO Use Select	00000000h	R/W
34–37h	GP_IO_SEL2	GPIO Input/Output Select 2	00000000h	R/W
38–3Bh	GP_LVL2	GPIO Level for Input or Output 2	00000FFFh	R/W

9.10.2 GPIO_USE_SEL—GPIO Use Select Register

Offset Address: GPIOBASE + 00h
Default Value: 1A003180h
Lockable: Yes
Attribute: R/W
Size: 32-bit
Power Well: Resume

Bit	Description
21,11, 5:0	**GPIO_USE_SEL**—R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. **NOTE:** Bits 31:29, 26, 15:14, and 10:9 are not implemented because there is no corresponding GPIO. **NOTE:** Bits 28:27, 25:22, 20:18, 13:12, and 8:6 are not implemented because the corresponding GPIOs are not mutiplexed. **NOTE:** Bits 16:17 are not implemented because the GPIO selection is controlled by bits 0:1. The REQ/GNT# pairs are enabled/disabled together. For example, if bit 0 is set to 1 then the REQ/GNT[A]# pair will function as GPIO[0] and GPIO[16].

9.10.3 GP_IO_SEL—GPIO Input/Output Select Register

Offset Address:	GPIOBASE +04h	Attribute:	R/W
Default Value:	0000FFFFh	Size:	32-bit
Lockable:	No	Power Well:	Resume

Bit	Description
31:29, 26	Reserved.
28:27 25:24	**GPIO[n]_SEL**—R/W. 0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.
23:16	Always 0. The GPIOs are fixed as outputs.
15:0	Always 1. These GPIOs are fixed as inputs.

9.10.4 GP_LVL—GPIO Level for Input or Output Register

Offset Address:	GPIOBASE +0Ch	Attribute:	R/W, RO
Default Value:	1B3F 0000h	Size:	32-bit
Lockable:	No	Power Well:	See bit descriptions

Bit	Description
31:29, 26	Reserved.
28:27, 25:24	**GP_LVL[n]**—R/W. If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL register) then the bit can be updated by software to drive a high or low value on the output pin. If GPIO[n] is programmed as an input, then software can read the bit to determine the level on the corresponding input pin. These bits correspond to GPIO that are in the Resume well, and will be reset to their default values by RSMRST# but not by PCIRST#. 0 = Low 1 = High
23:16	**GP_LVL[n]**—R/W. These bits can be updated by software to drive a high or low value on the output pin. These bits correspond to GPIO that are in the Core well, and will be reset to their default values by PCIRST#. 0 = Low 1 = High
15:0	Reserved. GPI[13:11] and [8:0] the active status of a GPI is read from the corresponding bit in GPE1_STS register.

9.10.5 GPO_BLINK—GPO Blink Enable Register

Offset Address:	GPIOBASE +18h	Attribute:	R/W
Default Value:	0004 0000h	Size:	32-bit
Lockable:	No	Power Well:	See bit description

Bit	Description
31:29, 26, 24:20, 17:0	Reserved.
28:27, 25	**GP_BLINK[n]**—R/W. The setting of these bits will have no effect if the corresponding GPIO is programmed as an input. These bits correspond to GPIO that are in the Resume well, and will be reset to their default values by RSMRST# but not by PCIRST#. 0 = The corresponding GPIO will function normally. 1 = If the corresponding GPIO is programmed as an output, the output signal will blink at a rate of approximately once per second. The high and low times have approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set.
19:18	**GP_BLINK[n]**—R/W. The setting of these bits will have no effect if the corresponding GPIO is programmed as an input. These bits correspond to GPIO that are in the Core well, and will be reset to their default values by PCIRST#. 0 = The corresponding GPIO will function normally. 1 = If the corresponding GPIO is programmed as an output, the output signal will blink at a rate of approximately once per second. The high and low times are approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set.

Note: GPIO[18] blinks by default immediately after reset. This signal could be connected to an LED to indicate a failed boot (by programming BIOS to clear GP_BLINK[18] after successful POST).

9.10.6 GPI_INV—GPIO Signal Invert Register

Offset Address:	GPIOBASE +2Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	See bit description

Bit	Description
31:14, 10:9	Reserved.
13:11, 8	**GP_INV[n]**—R/W. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least 2 PCI clocks to ensure detection by the ICH3. In the S3, S4 or S5 states the input signal must be active for at least 2 RTC clocks to ensure detection. The setting of these bits will have no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPIO that are in the Resume well, and will be reset to their default values by RSMRST# but not by PCIRST#. 0 = The corresponding GPI_STS bit will be set when the ICH3 detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit will be set when the ICH3 detects the state of the input pin to be low.
7:0	**GP_INV[n]**—R/W. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least 2 PCI clocks to ensure detection by the ICH3. The setting of these bits will have no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPIO that are in the Core well, and will be reset to their default values by PCIRST#. 0 = The corresponding GPI_STS bit will be set when the ICH3 detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit will be set when the ICH3 detects the state of the input pin to be low.

9.10.7 GPIO_USE_SEL2—GPIO Use Select 2 Register

Offset Address:	GPIOBASE +30h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:0	**GPIO_USE_SEL2[43:32]**—R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. **NOTES:** 1. Bits 31:12 are not implemented because they have no corresponding GPIOs. 2. If GPIO[n] does not exist, the bit in this register always reads as 0 and writes have no effect. After a full reset (RSMRST#) all multiplexed signals in the resume and core wells are configured as their native function rather than as a GPIO. After just a PCIRST#, the GPIO in the core well are configured as their native function.

9.10.8 GP_IO_SEL2—GPIO Input/Output Select 2 Register

Offset Address:	GPIOBASE +34h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:12	Always 0. No corresponding GPIO.
11:0	**GP_IO_SEL2[43:32].** When set to a 1, the corresponding GPIO signal (if enabled in the GPIO_USE_SEL2 register) is programmed as an input. When set to 0, the GPIO signal is programmed as an output.

9.10.9 GP_LVL2—GPIO Level for Input or Output 2 Register

Offset Address:	GPIOBASE +38h	Attribute:	R/W
Default Value:	00000FFFh	Size:	32-bit
Lockable:	No	Power Well:	See below

Bit	Description
31:12	Reserved. Read-only 0.
11:0	**GP_LVL2[43:32].** If GPIO[n] is programmed to be an output (via the corresponding bit in the GP_IO_SEL2 register), then the corresponding GP_LVL2[n] bit can be updated by software to drive a high or low value on the output pin. 1 = high, 0 = low. If GPIO[n] is programmed as an input, then the corresponding GP_LVL2 bit reflects the state of the input signal (1 = high, 0 = low). Writes will have no effect. Since these bits correspond to GPIO that are in the core well, these bits will be reset by PCIRST#.

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IDE Controller Registers (D31:F1) 10

10.1 PCI Configuration Registers (IDE—D31:F1)

Note: Registers that are not shown should be treated as Reserved (See Section 6.2 for details).

All of the IDE registers are in the core well. None can be locked.

Table 10-1. PCI Configuration Map (IDE-D31:F1)

Offset	Mnemonic	Register Name	Default	Type
00–01h	VID	Vendor ID	8086h	RO
02–03h	DID	Device ID	248Bh	RO
04–05h	CMD	Command	00h	R/W
06–07h	STS	Device Status	0280h	R/W
08h	RID	Revision ID	See Note 2	RO
09h	PI	Programming Interface	8Ah	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	01h	RO
0Dh	MLT	Master Latency Timer	00	RO
0Eh	HTYPE	Header Type	00h	RO
10–13h	PCMD_BAR	Primary Command Block Base Address	00000001h	R/W
14–17h	PCNL_BAR	Primary Control Block Base Address	00000001h	R/W
18–1Bh	SCMD_BAR	Secondary Command Block Base Address	00000001h	R/W
1C–1Fh	SCNL_BAR	Primary Command Block Base Address	00000001h	R/W
20–23h	BAR	Base Address Register	00000001h	R/W
24–27h	EXBAR	Expansion BAR	00h	R/W
2C–2Dh	SVID	Subsystem Vendor ID	00	R/Write-Once
2E–2Fh	SID	Subsystem ID	00	R/Write-Once
3C	INTR_LN	Interrupt Line	00	R/W
3D	INTR_PN	Interrupt Pin	01	R/W
40–41h	IDE_TIMP	Primary IDE Timing	0000h	R/W
42–43h	ID_TIMS	Secondary IDE Timing	0000h	R/W
44h	SIDETIM	Slave IDE Timing	00h	R/W
48h	SDMAC	Synchronous DMA Control Register	00h	R/W
4A–4Bh	SDMATIM	Synchronous DMA Timing Register	0000h	R/W
54h	IDE_CONFIG	IDE I/O Configuration Register	00h	R/W

NOTES:
1. The ICH3 IDE controller is not arbitrated as a PCI device, therefore it doe s not need a master latency timer.
2. Refer to the Specification Update for the Revision ID.

10.1.1 VID—Vendor ID Register (IDE—D31:F1)

Offset Address: 00–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Vendor Identification Value**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h.

10.1.2 DID—Device ID Register (IDE—D31:F1)

Offset Address: 02–03h Attribute: RO
Default Value: 248Bh Size: 16 bits

Bit	Description
15:0	**Device Identification Value**—RO. DID = 248Bh

10.1.3 CMD—Command Register (IDE—D31:F1)

Address Offset: 04h–05h Attribute: RO, R/W
Default Value: 00h Size: 16 bits

Bit	Description
15:10	Reserved.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	SERR# Enable (SERR_EN)—RO. Hardwired to 0.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	Parity Error Response (PER)—RO. Hardwired to 0.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0.
2	**Bus Master Enable (BME)**—R/W. Controls the ICH3's ability to act as a PCI master for IDE Bus Master transfers. 0 = Disable 1 = Enable.
1	**Memory Space Enable (MSE)**—R/W. 0 = Disables access. 1 = Enables access to the IDE Expansion memory range. The EXBAR register (Offset 24h) must be programmed before this bit is set. **NOTE:** BIOS should set this bit to a 1.
0	**I/O Space Enable (IOE)**—R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master I/O registers. 1 = Enable. Note that the Base Address register for the Bus Master registers should be programmed before this bit is set. **NOTES:** 1. Separate bits are provided (IDE Decode Enable, in the IDE Timing register) to independently disable the Primary or Secondary I/O spaces. 2. When this bit is 0 and the IDE controller is in Native Mode, the Interrupt Pin Register (see Section 11.1.14) will be masked (the interrupt will not be asserted). If an interrupt occurs while the masking is in place and the interrupt is still active when the masking ends, the interrupt will be allowed to be asserted.

10.1.4 STS—Device Status Register (IDE—D31:F1)

Address Offset: 06–07h
Default Value: 0280h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15	Detected Parity Error (DPE)—RO. Hardwired to 0.
14	Signaled System Error (SSE)—RO. Hardwired to 0.
13	**Received Master Abort (RMA)**—R/WC. 0 = Cleared by writing a 1 to it. 1 = Bus Master IDE interface function, as a master, generated a master-abort.
12	Reserved as 0—RO.
11	**Signaled Target Abort (STA)**—R/WC. 0 = Cleared by writing a 1 to it. 1 = ICH3 IDE interface function is targeted with a transaction that the ICH3 terminates with a target abort.
10:9	**DEVSEL# Timing Status (DEV_STS)**—RO. 01 = Hardwired; however, the ICH3 does not have a real DEVSEL# signal associated with the IDE unit, so these bits have no effect.
8	Data Parity Error Detected (DPED)—RO. Hardwired to 0.
7	Fast Back to Back (FB2B)—RO. Hardwired to 1.
6	User Definable Features (UDF)—RO. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0.
4:0	Reserved.

10.1.5 RID—Revision Identification Register (IDE—D31:F1)

Address Offset: 08h
Default Value: See Note
Attribute: RO
Size: 8 Bits

Bit	Description
7:0	**Revision Identification Value**—RO.

NOTE: Refer to the Specification Update for the Revision ID.

10.1.6 PI—Programming Interface Register (IDE—D31:F1)

Address Offset: 09h Attribute: R/W
Default Value: 8Ah Size: 8 bits

Bit	Description
7	This read-only bit is a 1 to indicate that the ICH3 supports bus master operation.
6:4	Reserved. Will always return 0.
3	SOP_MODE_CAP**.** This read-only bit is a 1 to indicate that the secondary controller supports both legacy and native modes.
2	**SOP_MODE_SEL.** This read-write bits determines the mode that the secondary IDE channel is operating in. 0 = Legacy-PCI mode (default). 1 = Native-PCI mode.
1	POP_MODE_CAP**.** This read-only bit is a 1 to indicate that the primary controller supports both legacy and native modes.
0	**POP_MODE_SEL.** This read-write bits determines the mode that the primary IDE channel is operating in. 0 = Legacy-PCI mode (default). 1 = Native-PCI mode.

10.1.7 SCC—Sub Class Code Register (IDE—D31:F1)

Address Offset: 0Ah Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Sub Class Code**—RO. 01h = IDE device, in the context of a mass storage device.

10.1.8 BCC—Base Class Code Register (IDE—D31:F1)

Address Offset: 0Bh Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Base Class Code**—RO. 01 = Mass storage device.

10.1.9 MLT—Master Latency Timer Register (IDE—D31:F1)

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Master Latency Timer Count (MLTC)—RO. Hardwired to 00h. The IDE controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

10.1.10 PCMD_BAR—Primary Command Block Base Address Register (IDE—D31:F1)

Address Offset: 10h–13h Attribute: R/W
Default Value: 00000001h Size: 32 bits

Bit	Description
31:16	Reserved.
15:3	**Base Address**—R/W. Base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved.
0	**Resource Type Indicator (RTE)**—This bit is set to one, indicating a request for I/O space.Read-Only.

Note: This 8-byte I/O space is used in native mode for the Primary Controller's Command Block.

10.1.11 PCNL_BAR—Primary Control Block Base Address Register (IDE—D31:F1)

Address Offset: 14h–17h Attribute: R/W
Default Value: 00000001h Size: 32 bits

Bit	Description
31:16	Reserved.
15:2	**Base Address**—R/W. Base address of the I/O space (4 consecutive I/O locations).
1	Reserved.
0	**Resource Type Indicator (RTE)**—This bit is set to one, indicating a request for I/O space.Read-Only.

Note: This 4-byte I/O space is used in native mode for the Primary Controller's Command Block.

10.1.12 SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1)

Address Offset: 18h–1Bh Attribute: R/W
Default Value: 00000001h Size: 32 bits

Bit	Description
31:16	Reserved.
15:3	**Base Address**—R/W. Base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved.
0	**Resource Type Indicator (RTE)**—This bit is set to one, indicating a request for I/O space.Read-Only.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

10.1.13 SCNL_BAR—Secondary Control Block Base Address Register (IDE D31:F1)

Address Offset:	14h–17h	Attribute:	R/W
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved.
15:2	**Base Address**—R/W. Base address of the I/O space (4 consecutive I/O locations).
1	Reserved.
0	**Resource Type Indicator (RTE)**—This bit is set to one, indicating a request for I/O space.Read-Only.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

10.1.14 BM_BASE—Bus Master Base Address Register (IDE—D31:F1)

Address Offset:	20h–23h	Attribute:	R/W
Default Value:	00000001h	Size:	32 bits

The Bus Master IDE interface function uses Base Address register 5 to request a 16-byte I/O space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary, 6 bytes for secondary). Only bits [15:4] are used to decode the address.

Bit	Description
31:16	Reserved.
15:4	**Base Address—**R/W. Base address of the I/O space (16 consecutive I/O locations).
3:1	Reserved.
0	**Resource Type Indicator (RTE)—**RO. Hardwired to 1, indicating a request for I/O space.

10.1.15 EXBAR—Expansion Base Address Register (IDE—D31:F1)

Address Offset:	24h–27h	Attribute:	R/W
Default Value:	00h	Size:	32 bits

Note: This is a memory mapped BAR that requires 1 KB of dword aligned memory that is Intel reserved for future functionality. BIOS needs to program the base address for a 1-K memory space.

Bit	Description
31:0	Intel Reserved for Future Functionality.

10.1.16 IDE_SVID—Subsystem Vendor ID Register (IDE—D31:F1)

Address Offset:	2Ch–2Dh	Attribute:	R/Write-Once
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem Vendor ID**—R/WO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. Software (BIOS) sets the value in this register. After that, the value can be read, but subsequent writes to this register have no effect. The value written to this register will also be readable via the corresponding SVID registers for the USB#1, USB#2 and SMBus functions.

10.1.17 IDE_SID—Subsystem ID Register (IDE—D31:F1)

Address Offset:	2Eh–2Fh	Attribute:	R/Write-Once
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem ID**—R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. Software (BIOS) sets the value in this register. After that, the value can be read, but subsequent writes to this register have no effect. The value written to this register will also be readable via the corresponding SID registers for the USB#1, USB#2 and SMBus functions.

10.1.18 INTR_LN—Interrupt Line Register (IDE—D31:F1)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN).** It is to communicate to software the interrupt line that the interrupt pin is connected to.

10.1.19 INTR_PN—Interrupt Pin Register (IDE—D31:F1)

Address Offset:	3Dh	Attribute:	RO
Default Value:	01h	Size:	8 bits

Bit	Description
7:3	Reserved.
2:0	**Interrupt Pin (INT_PN).** The value of 01h indicates to “software” that the ICH3 will drive PIRQ[A]#. Note that this is only used in native mode. Also note that the routing to the internal interrupt controller does not necessarily relate to the value in this register. The IDE interrupt is in fact routed to PIRQ[C]# (IRQ18 in APIC mode). Read-Only.

10.1.20 IDE_TIM—IDE Timing Register (IDE—D31:F1)

Address Offset:	Primary: 40–41h Secondary: 42–43h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

This register controls the timings driven on the IDE cable for PIO and Intel® 8237 style DMA transfers. It also controls operation of the buffer for PIO transfers.

Bit	Description
15	**IDE Decode Enable (IDE)**—R/W. Individually enable/disable the Primary or Secondary decode. The IDE I/O Space Enable bit in the Command register must be set in order for this bit to have any effect. Additionally, separate configuration bits are provided (in the IDE I/O Configuration register) to individually disable the primary or secondary IDE interface signals, even if the IDE Decode Enable bit is set. 0 = Disable. 1 = Enables the ICH3 to decode the associated Command Blocks (1F0–1F7h for primary, 170–177h for secondary) and Control Block (3F6h for primary and 376h for secondary). This bit effects the IDE decode ranges for both legacy and native-Mode decoding. It also effects the corresponding primary or secondary memory decode range for IDE Expansion.
14	**Drive 1 Timing Register Enable (SITRE)**—R/W. 0 = Use bits 13:12, 9:8 for both drive 0 and drive 1. 1 = Use bits 13:12, 9:8 for drive 0, and use the Slave IDE Timing register for drive 1.
13:12	**IORDY Sample Point (ISP)**—R/W**.** The setting of these bits determine the number of PCI clocks between IDE IOR#/IOW# assertion and the first IORDY sample point. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved.
11:10	Reserved.
9:8	**Recovery Time (RCT)**—R/W. The setting of these bits determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clock
7	**Drive 1 DMA Timing Enable (DTE1)**—R/W. 0 = Disable. 1 = Enable the fast timing mode for DMA transfers only for this drive. PIO transfers to the IDE data port will run in compatible timing.
6	**Drive 1 Prefetch/Posting Enable (PPE1)**—R/W. 0 = Disable. 1 = Enable Prefetch and posting to the IDE data port for this drive.
5	**Drive 1 IORDY Sample Point Enable (IE1)**—R/W. 0 = Disable IORDY sampling for this drive. 1 = Enable IORDY sampling for this drive.
4	**Drive 1 Fast Timing Bank (TIME1)**— /W. 0 = Accesses to the data port will use compatible timings for this drive. 1 = When this bit = 1 and bit 14 = 0, accesses to the data port will use bits 13:12 for the IORDY sample point, and bits 9:8 for the recovery time. When this bit = 1 and bit 14 = 1, accesses to the data port will use the IORDY sample point and recover time specified in the slave IDE timing register.

Bit	Description
3	**Drive 0 DMA Timing Enable (DTE0)**—R/W. 0 = Disable. 1 = Enable fast timing mode for DMA transfers only for this drive. PIO transfers to the IDE data port will run in compatible timing.
2	**Drive 0 Prefetch/Posting Enable (PPE0)**—R/W. 0 = Disable prefetch and posting to the IDE data port for this drive. 1 = Enable prefetch and posting to the IDE data port for this drive.
1	**Drive 0 IORDY Sample Point Enable (IE0)**—R/W. 0 = Disable IORDY sampling is disabled for this drive. 1 = Enable IORDY sampling for this drive.
0	**Drive 0 Fast Timing Bank (TIME0)**—R/W. 0 = Accesses to the data port will use compatible timings for this drive. 1 = Accesses to the data port will use bits 13:12 for the IORDY sample point, and bits 9:8 for the recovery time.

10.1.21 SLV_IDETIM—Slave (Drive 1) IDE Timing Register (IDE—D31:F1)

Address Offset: 44h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:6	**Secondary Drive 1 IORDY Sample Point (SISP1)**—R/W. Determines the number of PCI clocks between IDE IOR#/IOW# assertion and the first IORDY sample point, if the access is to drive 1 data port and bit 14 of the IDE timing register for secondary is set. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved
5:4	**Secondary Drive 1 Recovery Time (SRCT1)**—R/W. Determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle, if the access is to drive 1 data port and bit 14 of the IDE timing register for secondary is set. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clocks
3:2	**Primary Drive 1 IORDY Sample Point (PISP1)**—R/W. Determines the number of PCI clocks between IOR#/IOW# assertion and the first IORDY sample point, if the access is to drive 1 data port and bit 14 of the IDE timing register for primary is set. 00 = 5 clocks 01 = 4 clocks 10 = 3 clocks 11 = Reserved
1:0	**Primary Drive 1 Recovery Time (PRCT1)**—R/W. Determines the minimum number of PCI clocks between the last IORDY sample point and the IOR#/IOW# strobe of the next cycle, if the access is to drive 1 data port and bit 14 of the IDE timing register for primary is set. 00 = 4 clocks 01 = 3 clocks 10 = 2 clocks 11 = 1 clocks

10.1.22 SDMA_CNT—Synchronous DMA Control Register (IDE—D31:F1)

Address Offset: 48h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:4	Reserved.
3	**Secondary Drive 1 Synchronous DMA Mode Enable (SSDE1)**—R/W. 0 = Disable (default). 1 = Enable Synchronous DMA mode for secondary channel drive 1.
2	**Secondary Drive 0 Synchronous DMA Mode Enable (SSDE0)**—R/W. 0 = Disable (default). 1 = Enable Synchronous DMA mode for secondary drive 0.
1	**Primary Drive 1 Synchronous DMA Mode Enable (PSDE1)**—R/W. 0 = Disable (default). 1 = Enable Synchronous DMA mode for primary channel drive 1.
0	**Primary Drive 0 Synchronous DMA Mode Enable (PSDE0)**—R/W. 0 = Disable (default). 1 = Enable Synchronous DMA mode for primary channel drive 0.

10.1.23 SDMA_TIM—Synchronous DMA Timing Register (IDE—D31:F1)

Address Offset:	4A–4Bh	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:14	Reserved.
13:12	**Secondary Drive 1 Cycle Time (SCT1)**—R/W. For Ultra ATA mode. The setting of these bits determines the minimum write strobe cycle time (CT). The DMARDY#-to-STOP (RP) time is also determined by the setting of these bits. **SCB1 = 0 (33 MHz clk)** 00 = CT 4 clocks, RP 6 clocks 01 = CT 3 clocks, RP 5 clocks 10 = CT 2 clocks, RP 4 clocks 11 = Reserved **SCB1 = 1 (66 MHz clk)** 00 = Reserved 01 = CT 3 clocks, RP 8 clocks 10 = CT 2 clocks, RP 8 clocks 11 = Reserved **FAST_SCB1 = 1 (133 MHz clk)** 00 = Reserved 01 = CT 3 clks, RP 16 clks 10 = Reserved 11 = Reserved
11:10	Reserved.
9:8	**Secondary Drive 0 Cycle Time (SCT0)**—R/W. For Ultra ATA mode. The setting of these bits determines the minimum write strobe cycle time (CT). The DMARDY#-to-STOP (RP) time is also determined by the setting of these bits. **SCB1 = 0 (33 MHz clk)** 00 = CT 4 clocks, RP 6 clocks 01 = CT 3 clocks, RP 5 clocks 10 = CT 2 clocks, RP 4 clocks 11 = Reserved **SCB1 = 1 (66 MHz clk)** 00 = Reserved 01 = CT 3 clocks, RP 8 clocks 10 = CT 2 clocks, RP 8 clocks 11 = Reserved **FAST_SCB1 = 1 (133 MHz clk)** 00 = Reserved 01 = CT 3 clks, RP 16 clks 10 = Reserved 11 = Reserved
7:6	Reserved.
5:4	**Primary Drive 1 Cycle Time (PCT1)**—R/W. For Ultra ATA mode, the setting of these bits determines the minimum write strobe cycle time(CT). The DMARDY#-to-STOP (RP) time is also determined by the setting of these bits. **PCB1 = 0 (33 MHz clk)** 00 = CT 4 clocks, RP 6 clocks 01 = CT 3 clocks, RP 5 clocks 10 = CT 2 clocks, RP 4 clocks 11 = Reserved **PCB1 = 1 (66 MHz clk)** 00 = Reserved 01 = CT 3 clocks, RP 8 clocks 10 = CT 2 clocks, RP 8 clocks 11 = Reserved **FAST_PCB1 = 1 (133 MHz clk)** 00 = Reserved 01 = CT 3 clks, RP 16 clks 10 = Reserved 11 = Reserved
3:2	Reserved.
1:0	**Primary Drive 0 Cycle Time (PCT0)**—R/W. For Ultra ATA mode, the setting of these bits determines the minimum write strobe cycle time (CT). The DMARDY#-to-STOP (RP) time is also determined by the setting of these bits. **PCB1 = 0 (33 MHz clk)** 00 = CT 4 clocks, RP 6 clocks 01 = CT 3 clocks, RP 5 clocks 10 = CT 2 clocks, RP 4 clocks 11 = Reserved **PCB1 = 1 (66 MHz clk)** 00 = Reserved 01 = CT 3 clocks, RP 8 clocks 10 = CT 2 clocks, RP 8 clocks 11 = Reserved **FAST_PCB1 = 1 (133 MHz clk)** 00 = Reserved 01 = CT 3 clks, RP 16 clks 10 = Reserved 11 = Reserved

10.1.24 IDE_CONFIG—IDE I/O Configuration Register

Address Offset: 54h
Default Value: 00h
Attribute: R/W
Size: 32 bits

Bit	Description
31:20	Reserved.
19:18	**SEC_SIG_MODE**—R/W. These bits should always be set to 00b. 00 = Normal (Enabled) 01 = Reserved 10 = Reserved 11 = Reserved
17:16	**PRIM_SIG_MODE**—R/W. These bits should always be set to 00b. 00 = Normal (Enabled) 01 = Reserved 10 = Reserved 11 = Reserved
15	**Fast Secondary Drive 1 Base Clock (FAST_SCB1)**—R/W. This bit is used in conjunction with the SCT1 bits to enable/disable Ultra ATA/100 timings for the Secondary Slave drive. 0 = Disable Ultra ATA/100 timing for the Secondary Slave drive. 1 = Enable Ultra ATA/100 timing for the Secondary Slave drive (overrides bit 3 in this register).
14	**Fast Secondary Drive 0 Base Clock (FAST_SCB0)**—R/W. This bit is used in conjunction with the SCT0 bits to enable/disable Ultra ATA/100 timings for the Secondary Master drive. 0 = Disable Ultra ATA/100 timing for the Secondary Master drive. 1 = Enable Ultra ATA/100 timing for the Secondary Master drive (overrides bit 2 in this register).
13	**Fast Primary Drive 1 Base Clock (FAST_PCB1)**—R/W. This bit is used in conjunction with the PCT1 bits to enable/disable Ultra ATA/100 timings for the Primary Slave drive. 0 = Disable Ultra ATA/100 timing for the Primary Slave drive. 1 = Enable Ultra ATA/100 timing for the Primary Slave drive (overrides bit 1 in this register).
12	**Fast Primary Drive 0 Base Clock (FAST_PCB0)**—R/W. This bit is used in conjunction with the PCT0 bits to enable/disable Ultra ATA/100 timings for the Primary Master drive. 0 = Disable Ultra ATA/100 timing for the Primary Master drive. 1 = Enable Ultra ATA/100 timing for the Primary Master drive (overrides bit 0 in this register).
11	Reserved.
10	**WR_PingPong_EN**—R/W. 0 = Disabled. The buffer will behave similar to PIIX4. 1 = Enables the write buffer to be used in a split (ping/pong) manner.
9:8	Reserved.
7	**Secondary Slave Channel Cable Reporting**—R/W. BIOS should program this bit to tell the IDE driver which cable is plugged into the channel. 0 = 40 conductor cable is present. 1 = 80 conductor cable is present.
6	**Secondary Master Channel Cable Reporting**—R/W. Same description as bit 7.
5	**Primary Slave Channel Cable Reporting**—R/W. Same description as bit 7.
4	**Primary Master Channel Cable Reporting**—R/W. Same description as bit 7.
3	**Secondary Drive 1 Base Clock (SCB1)**—R/W. 0 = 33 MHz base clock for Ultra ATA timings. 1 = 66 MHz base clock for Ultra ATA timings.
2	**Secondary Drive 0 Base Clock (SCBO)**—R/W. 0 = 33 MHz base clock for Ultra ATA timings. 1 = 66 MHz base clock for Ultra ATA timings.

Bit	Description
1	**Primary Drive 1 Base Clock (PCB1)**—R/W. 0 = 33 MHz base clock for Ultra ATA timings. 1 = 66 MHz base clock for Ultra ATA timings.
0	**Primary Drive 0 Base Clock (PCB0)**—R/W. 0 = 33 MHz base clock for Ultra ATA timings. 1 = 66 MHz base clock for Ultra ATA timings.

10.2 Bus Master IDE I/O Registers (D31:F1)

The bus master IDE function uses 16 bytes of I/O space, allocated via the BMIBA register, located in Device 31:Function 1 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or dword quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). The description of the I/O registers is shown below in Table 10-2.

Table 10-2. Bus Master IDE I/O Registers

Offset	Mnemonic	Register	Default	Type
00h	BMICP	Command Register Primary	00h	R/W
01h	—	Reserved	00h	RO
02h	BMISP	Status Register Primary	00h	R/WC
03h	—	Reserved	00h	RO
04–07h	BMIDP	Descriptor Table Pointer Primary	xxxxxxxxh	R/W
08h	BMICS	Command Register Secondary	00h	R/W
09h	—	Reserved	00h	RO
0Ah	BMISS	Status Register Secondary	00h	R/WC
0Bh	—	Reserved	00h	RO
0C–0Fh	BMIDS	Descriptor Table Pointer Secondary	xxxxxxxxh	R/W

10.2.1 BMIC[P,S]—Bus Master IDE Command Register

Address Offset:	Primary: 00h Secondary: 08h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:4	Reserved. Returns 0s.
3	**Read / Write Control (RWC)**—R/W. This bit sets the direction of the bus master transfer. This bit must NOT be changed when the bus master function is active. 0 = Memory reads. 1 = Memory writes.
2:1	Reserved. Returns 0.
0	**Start/Stop Bus Master (START)**—R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (i.e., the Bus Master IDE Active bit of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from a zero to a one. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a '0' to this bit. This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically.

10.2.2 BMIS[P,S]—Bus Master IDE Status Register

Address Offset:	Primary: 02h Secondary: 0Ah	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Bit	Description
7	Reserved. Returns 0.
6	**Drive 1 DMA Capable**—R/W. 0 = Not Capable. 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The ICH3 does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
5	**Drive 0 DMA Capable**—R/W. 0 = Not Capable. 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The ICH3 does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved. Returns 0s.
2	**Interrupt**—R/WC. Software can use this bit to determine if an IDE device has asserted its interrupt line (IRQ 14 for the Primary channel, and IRQ 15 for Secondary). 0 = This bit is cleared by software writing a '1' to the bit position. If this bit is cleared while the interrupt is still active, this bit will remain clear until another assertion edge is detected on the interrupt line. 1 = Set by the rising edge of the IDE interrupt line, regardless of whether or not the interrupt is masked in the 8259 or the internal I/O APIC. When this bit is read as a one, all data transferred from the drive is visible in system memory.
1	**Error**—R/WC. 0 = This bit is cleared by software writing a '1' to the bit position. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	**Bus Master IDE Active (ACT)**—RO. 0 = This bit is cleared by the ICH3 when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the ICH3 when the Start bit is cleared in the Command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the ICH3 when the Start bit is written to the Command register.

10.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register

Address Offset:	Primary: 04h Secondary: 0Ch	Attribute:	R/W
Default Value:	All bits undefined	Size:	32 bits

Bit	Description
31:2	**Address of Descriptor Table (ADDR)**—R/W. Corresponds to A[31:2]. The Descriptor Table must be dword aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved.

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USB 1.1 Controllers Registers 11

11.1 PCI Configuration Registers (D29:F0/F1/F2)

Note: Registers that are not shown should be treated as Reserved (See Section 6.2 for details).

Table 11-1. PCI Configuration Map (USB—D29:F0/F1/F2)

Offset	Mnemonic	Register Name	Function 0 Default	Function 1 Default	Function 2 Default	Type
00–01h	VID	Vendor ID	8086h	8086h	8086h	RO
02–03h	DID	Device ID	2482h	2484h	2487h	RO
04–05h	CMD	Command	0000h	0000h	0000h	R/W
06–07h	STA	Device Status	0280h	0280h	0280h	R/W
08h	RID	Revision ID	See Note	See Note	See Note	RO
09h	PI	Programming Interface	00h	00h	00h	RO
0Ah	SCC	Sub Class Code	03h	03h	03h	RO
0Bh	BCC	Base Class Code	0Ch	0Ch	0Ch	RO
0Eh	HTYPE	Header Type	80h	00h	00h	RO
20–23h	Base	Base Address	00000001h	00000001h	00000001h	R/W
2C–2Dh	SVID	Subsystem Vendor ID	00	00	00	RO
2E–2Fh	SID	Subsystem ID	00	00	00	RO
3Ch	INTR_LN	Interrupt Line	00h	00h	00h	R/W
3Dh	INTR_PN	Interrupt Pin	01h	02h	03h	RO
60h	SB_RELNUM	Serial Bus Release Number	10h	10	10	RO
C0–C1h	USB_LEGKEY	USB Legacy Keyboard/Mouse Control	2000h	2000h	2000h	R/W
C4h	USB_RES	USB Resume Enable	00h	00h	00h	R/W

NOTE: Refer to the Specification Update for the Revision ID.

11.1.1 VID—Vendor Identification Register (USB—D29:F0/F1/F2)

Address Offset:	00–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Vendor Identification Value**—RO. This is a 16-bit value assigned to Intel.

11.1.2 DID—Device Identification Register (USB—D29:F0/F1/F2)

Address Offset:	02–03h	Attribute:	RO
Default Value:	Function 0: 2482h Function 1: 2484h Function 2: 2487h	Size:	16 bits

Bit	Description
15:0	**Device Identification Value**—RO. This is a 16-bit value assigned to the ICH3 USB Host Controllers.

11.1.3 CMD—Command Register (USB—D29:F0/F1/F2)

Address Offset:	04–05h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:10	Reserved.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	SERR# Enable (SERR_EN)—RO. Hardwired to 0.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	Parity Error Response (PER)—RO. Hardwired to 0.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0.
2	**Bus Master Enable (BME)**—RW. 0 = Disable. 1 = Enable. The ICH3 can act as a master on the PCI bus for USB transfers.
1	Memory Space Enable (MSE)—RO. Hardwired to 0.
0	**I/O Space Enable (IOE)**—RW. This bit controls access to the I/O space registers. 0 = Disable. 1 = Enable accesses to the USB I/O registers. The Base Address register for USB should be programmed before this bit is set.

11.1.4 STA—Device Status Register (USB—D29:F0/F1/F2)

Address Offset:	06–07h	Attribute:	R/WC
Default Value:	0280h	Size:	16 bits

Bit	Description
15:14	Reserved as 00b. Read Only.
13	**Received Master Abort (RMA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = USB, as a master, generated a master-abort.
12	Reserved. Always read as 0.
11	**Signaled Target Abort (STA)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit location. 1 = USB function is targeted with a transaction that the ICH3 terminates with a target abort.
10:9	**DEVSEL# Timing Status (DEV_STS)**—RO. This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the ICH3's DEVSEL# timing when performing a positive decode. ICH3 generates DEVSEL# with medium timing for USB.
8	Data Parity Error Detected (DPED). Reserved as 0. Read Only.
7	Fast Back to Back (FB2B). Reserved as 1 Read Only.
6	User Definable Features (UDF). Reserved as 0. Read Only.
5	66 MHz Capable (66MHZ_CAP). Reserved as 0. Read Only.
4:0	Reserved.

11.1.5 RID—Revision Identification Register (USB—D29:F0/F1/F2)

Address Offset:	08h	Attribute:	RO
Default Value:	See Note	Size:	8 bits

Bit	Description
7:0	These bits contain device stepping information and are hardwired to the default value.

NOTE: Refer to the Specification Update for the Revision ID.

11.1.6 PI—Programming Interface Register (USB—D29:F0/F1/F2)

Address Offset:	09h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	Programming Interface Value—RO: 00h = No specific register level programming interface defined.

11.1.7 SCC—Sub Class Code Register (USB—D29:F0/F1/F2)

Address Offset: 0Ah Attribute: RO
Default Value: 03h Size: 8 bits

Bit	Description
7:0	**Sub Class Code**—RO. 03h = Universal Serial Bus Host Controller.

11.1.8 BCC—Base Class Code Register (USB—D29:F0/F1/F2)

Address Offset: 0Bh Attribute: RO
Default Value: 0Ch Size: 8 bits

Bit	Description
7:0	**Base Class Code**—RO. 0Ch = Serial Bus controller.

11.1.9 HTYPE—Header Type Register (USB—D29:F0/F1/F2)

Address Offset: 0Eh Attribute: RO
Default Value: FN 0: 80h Size: 8 bits
FN 1: 00h
FN 2: 00h

For functions 1 and 2, this register is hardwired to 00h. For function 0, bit 7 is determined by the values in bits 15, 10, and 9 of the function disable register (D31:F0:F2h).

Bit	Description
7	**Multi-Function Device.** When set to 1, this bit indicates to software that this is a multi-function device. 0 indicates a single-function device. Since the upper functions in this device can be individually hidden, this bit must be based on the function-disable bits in Device 31, Function 0, Offset F2h as follows: **D29:F7_Disable (bit 15)** / **D29:F2_Disable (bit 10)** / **D29:F2_Disable (bit 9)** / **Multi-Function Bit** 0 / X / X / 1 X / 0 / X / 1 X / X / 0 / 1 1 / 1 / 1 / 0
6:0	Configuration Layout. Hardwired to 00h, which indicates the standard PCI configuration layout.

11.1.10 BASE—Base Address Register (USB—D29:F0/F1/F2)

Address Offset:	20–23h	Attribute:	R/W
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved.
15:5	**Base Address**—R/W. Bits [15:5] correspond to I/O address signals AD [15:5], respectively. This gives 32 bytes of relocatable I/O space.
4:1	Reserved.
0	**Resource Type Indicator (RTE)**—RO. This bit is hardwired to 1 indicating that the base address field in this register maps to I/O space.

11.1.11 SVID—Subsystem Vendor ID Register (USB—D29:F0/F1/F2)

Address Offset:	2Ch–2Dh	Attribute:	RO
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem Vendor ID**—RO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE_SVID register.

11.1.12 SID—Subsystem ID Register (USB—D29:F0/F1/F2)

Address Offset:	2Eh–2Fh	Attribute:	RO
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem ID**—R/Write-Once. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE_SID register.

11.1.13 INTR_LN—Interrupt Line Register (USB—D29:F0/F1/F2)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)**—R/W. This data is not used by the ICH3. It is to communicate to software the interrupt line that the interrupt pin is connected to.

11.1.14 INTR_PN—Interrupt Pin Register (USB—D29:F0/F1/F2)

Address Offset:	3Dh	Attribute:	RO
Default Value:	Function 0: 01h Function 1: 02h Function 2: 03h	Size:	8 bits

Bit	Description
7:3	Reserved.
2:0	**Interrupt Pin (INT_PN).** The values of 01h, 02h, and 03h in function 0, 1, and 2, respectively, indicate to software that the corresponding ICH3 USB controllers drive the INTA#, INTB#, and INTC# PCI signals. Read-Only. Note that this does not determine the mapping to the ICH3 PIRQ inputs. Function 0 drives PIRQA; Function 1 drives PIRQD; Function 2 drives PIRQC. Function 1 does not use the corresponding mapping in order to spread the interrupts with AC '97, which has historically been mapped to PIRQB.

11.1.15 SB_RELNUM—Serial Bus Release Number Register (USB—D29:F0/F1/F2)

Address Offset:	60h	Attribute:	RO
Default Value:	10h	Size:	8 bits

Bit	Description
7:0	**Serial Bus Release Number**—RO. 10h = Indicates that the USB controller is compliant with the USB specification release 1.0.

11.1.16 USB_LEGKEY—USB Legacy Keyboard/Mouse Control Register (USB—D29:F0/F1/F2)

Address Offset:	C0–C1h	Attribute:	R/W
Default Value:	2000h	Size:	16 bits

This register is implemented separately in each of the USB 1.1 functions. However, the enable and status bits for the trapping logic are OR'ed and shared, respectively, since their functionality is not specific to any one host controller.

Bit	Description
15	**SMI Caused by End of Pass-through (SMIBYENDPS)**—R/WC. Indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
14	Reserved.
13	**PCI Interrupt Enable (USBPIRQEN)**—R/W. Used to prevent the USB controller from generating an interrupt due to transactions on its ports. Note, when disabled, that it will probably be configured to generate an SMI using bit 4 of this register. Default to 1 for compatibility with older USB software. 0 = Disable. 1 = Enable.

Bit	Description
12	**SMI Caused by USB Interrupt (SMIBYUSB)**—RO. Indicates if an interrupt event occurred from this controller. The interrupt from the controller is taken before the enable in bit 13 has any effect to create this read-only bit. Note that even if the corresponding enable bit is not set in the Bit 4, then this bit may still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software should clear the interrupts via the USB controllers. Writing a 1 to this bit will have no effect. 1 = Event Occurred.
11	**SMI Caused by Port 64 Write (TRAPBY64W)**—R/WC. Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
10	**SMI Caused by Port 64 Read (TRAPBY64R)**—R/WC. Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
9	**SMI Caused by Port 60 Write (TRAPBY60W)**—R/WC. Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
8	**SMI Caused by Port 60 Read (TRAPBY60R)**—R/WC. Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
7	**SMI at End of Pass-through Enable (SMIATENDPS)**—R/W. May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later. 0 = Disable. 1 = Enable.
6	**Pass Through State (PSTATE)**—RO. 0 = If software needs to reset this bit, it should set bit 5 in all of the host controllers to 0. 1 = Indicates that the state machine is in the middle of an A20GATE pass-through sequence.
5	**A20Gate Pass-Through Enable (A20PASSEN)**—R/W. 0 = Disable. 1 = Allows A20GATE sequence Pass-Through function. A specific cycle sequence involving writes to port 60h and 64h does not result in the setting of the SMI status bits.
4	**SMI on USB IRQ Enable (USBSMIEN)**—R/W. 0 = Disable 1 = USB interrupt will cause an SMI event..
3	**SMI on Port 64 Writes Enable (64WEN)**—R/W. 0 = Disable. 1 = A 1 in bit 11 will cause an SMI event.
2	**SMI on Port 64 Reads Enable (64REN)**—R/W. 0 = Disable. 1 = A 1 in bit 10 will cause an SMI event.
1	**SMI on Port 60 Writes Enable (60WEN)**—R/W. 0 = Disable. 1 = A 1 in bit 9 will cause an SMI event.
0	**SMI on Port 60 Reads Enable (60REN)**—R/W. 0 = Disable. 1 = A 1 in bit 8 will cause an SMI event.

11.1.17 USB_RES—USB Resume Enable Register (USB—D29:F0/F1/F2)

Address Offset:	C4h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:2	Reserved.
1	**PORT1EN**—R/W. Enable the USB controller to respond to wakeup events on this port. For Function 2 this applies to port 1, for Function 4 this applies to port 3. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/disconnect events.
0	**PORT0EN**—R/W. Enable the USB controller to respond to wakeup events on this port. For Function 2 this applies to port 0, for Function 4 this applies to port 2. 0 = The USB controller will not look at this port for a wakeup event. 1 = The USB controller will monitor this port for remote wakeup and connect/disconnect events.

11.2 USB I/O Registers

Some of the read/write register bits which deal with changing the state of the USB hub ports function such that on read back they reflect the current state of the port, and not necessarily the state of the last write to the register. This allows the software to poll the state of the port and wait until it is in the proper state before proceeding. A Host Controller Reset, Global Reset, or Port Reset will immediately terminate a transfer on the affected ports and disable the port. This affects the USBCMD register, bit [4] and the PORTSC registers, bits [12,6,2]. See individual bit descriptions for more detail.

Table 11-2. USB I/O Registers

Offset	Mnemonic	Register	Default	Type
00–01h	USBCMD	USB Command	0000h	R/W*
02–03h	USBSTS	USB Status	0020h	R/WC
04–05h	USBINTR	USB Interrupt Enable	0000h	R/W
06–07h	FRNUM	USB Frame Number	0000h	R/W (see Note 1)
08–0Bh	FRBASEADD	USB Frame List Base Address	Undefined	R/W
0Ch	SOFMOD	USB Start of Frame Modify	40h	R/W
0D–0Fh	—	Reserved	0	RO
10–11h	PORTSC0	Port 0 Status/Control	0080h	R/WC (see Note 1)
12–13h	PORTSC1	Port 1 Status/Control	0080h	R/WC (see Note 1)
14–17h	—	Reserved	0	RO
18h	LOOPDATA	Loop Back Test Data	00h	RO

NOTES:
1. These registers are WORD writable only. Byte writes to these registers have unpredictable effects.

11.2.1 USBCMD—USB Command Register

I/O Offset:	Base + (00–01h)	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed. The table following the bit description provides additional information on the operation of the Run/Stop and Debug bits.

Bit	Description
15:7	Reserved.
8	**Loop Back Test Mode**—R/W. 0 = Disable loop back test mode. 1 = ICH3 is in loop back test mode. When both ports are connected together, a write to one port will be seen on the other port and the data will be stored in I/O offset 18h.
7	**Max Packet (MAXP)**—R/W. This bit selects the maximum packet size that can be used for full speed bandwidth reclamation at the end of a frame. This value is used by the Host Controller to determine whether it should initiate another transaction based on the time remaining in the SOF counter. Use of reclamation packets larger than the programmed size will cause a Babble error if executed during the critical window at frame end. The Babble error results in the offending endpoint being stalled. Software is responsible for ensuring that any packet which could be executed under bandwidth reclamation be within this size limit. 0 = 32 bytes. 1 = 64 bytes.
6	**Configure Flag (CF)**—R/W. This bit has no effect on the hardware. It is provided only as a semaphore service for software. 0 = Indicates that software has not completed host controller configuration. 1 = HCD software sets this bit as the last action in its process of configuring the Host Controller.
5	**Software Debug (SWDBG)**—R/W. The SWDBG bit must only be manipulated when the controller is in the stopped state. This can be determined by checking the HCHalted bit in the USBSTS register. 0 = Normal Mode 1 = Debug mode. In SW Debug mode, the Host Controller clears the Run/Stop bit after the completion of each USB transaction. The next transaction is executed when software sets the Run/Stop bit back to 1.
4	**Force Global Resume (FGR)**—R/W: 0 = Software resets this bit to 0 after 20 ms has elapsed to stop sending the Global Resume signal. At that time all USB devices should be ready for bus activity. The 1 to 0 transition causes the port to send a low speed EOP signal. This bit will remain a 1 until the EOP has completed. 1 = Host Controller sends the Global Resume signal on the USB, and sets this bit to 1 when a resume event (connect, disconnect, or K-state) is detected while in global suspend mode.
3	**Enter Global Suspend Mode (EGSM)**—R/W: 0 = Software resets this bit to 0 to come out of Global Suspend mode. Software writes this bit to 0 at the same time that Force Global Resume (bit 4) is written to 0 or after writing bit 4 to 0. 1 = Host Controller enters the Global Suspend mode. No USB transactions occur during this time. The Host Controller is able to receive resume signals from USB and interrupt the system. Software must ensure that the Run/Stop bit (bit 0) is cleared prior to setting this bit.
2	**Global Reset (GRESET)**—R/W: 0 = This bit is reset by the software after a minimum of 10 ms has elapsed as specified in Chapter 7 of the USB Specification. 1 = Global Reset. The Host Controller sends the global reset signal on the USB and then resets all its logic, including the internal hub registers. The hub registers are reset to their power on state. Chip Hardware Reset has the same effect as Global Reset (bit 2), except that the Host Controller does not send the Global Reset on USB.

Bit	Description
1	**Host Controller Reset (HCRESET)**—R/W. The effects of HCRESET on Hub registers are slightly different from Chip Hardware Reset and Global USB Reset. The HCRESET affects bits [8,3:0] of the Port Status and Control Register (PORTSC) of each port. HCRESET resets the state machines of the Host Controller including the Connect/Disconnect state machine (one for each port). When the Connect/Disconnect state machine is reset, the output that signals connect/disconnect are negated to 0, effectively signaling a disconnect, even if a device is attached to the port. This virtual disconnect causes the port to be disabled. This disconnect and disabling of the port causes bit 1 (connect status change) and bit 3 (port enable/disable change) of the PORTSC to get set. The disconnect also causes bit 8 of PORTSC to reset. About 64 bit times after HCRESET goes to 0, the connect and low-speed detect will take place, and bits 0 and 8 of the PORTSC will change accordingly. 0 = Reset by the Host Controller when the reset process is complete. 1 = Reset. When this bit is set, the Host Controller module resets its internal timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated.
0	**Run/Stop (RS)**—R/W. When set to 1, the ICH3 proceeds with execution of the schedule. The ICH3 continues execution as long as this bit is set. When this bit is cleared, the ICH3 completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the Host Controller has finished the transaction and has entered the stopped state. The Host Controller clears this bit when the following fatal errors occur: consistency check failure, PCI Bus errors. 0 = Stop. 1 = Run. **Note:** The USB run stop bit should be cleared only under one of the following conditions: 1. There are no active Transaction Descriptors in the schedule. 2. A reset of the USB host controller is guaranteed prior to a subsequent run/stop bit assertion.

Table 11-3. Run/Stop, Debug Bit Interaction SWDBG (Bit 5), Run/Stop (Bit 0) Operation

SWDBG (Bit 5)	Run/Stop (Bit 0)	Description
0	0	If executing a command, the Host Controller completes the command and then stops. The 1.0 ms frame counter is reset and command list execution resumes from start of frame using the frame list pointer selected by the current value in the FRNUM register. (While Run/Stop=0, the FRNUM register can be reprogrammed).
0	1	Execution of the command list resumes from Start Of Frame using the frame list pointer selected by the current value in the FRNUM register. The Host Controller remains running until the Run/Stop bit is cleared (by software or hardware).
1	0	If executing a command, the Host Controller completes the command and then stops and the 1.0 ms frame counter is frozen at its current value. All status are preserved. The Host Controller begins execution of the command list from where it left off when the Run/Stop bit is set.
1	1	Execution of the command list resumes from where the previous execution stopped. The Run/Stop bit is set to 0 by the Host Controller when a TD is being fetched. This causes the Host Controller to stop again after the execution of the TD (single step). When the Host Controller has completed execution, the HC Halted bit in the Status Register is set.

When the USB Host Controller is in Software Debug Mode (USBCMD Register bit 5=1), the single stepping software debug operation is as follows:

To Enter Software Debug Mode:

1. HCD puts Host Controller in Stop state by setting the Run/Stop bit to 0.
2. HCD puts Host Controller in Debug Mode by setting the SWDBG bit to 1.
3. HCD sets up the correct command list and Start Of Frame value for starting point in the Frame List Single Step Loop.
4. HCD sets Run/Stop bit to 1.
5. Host Controller executes next active TD, sets Run/Stop bit to 0, and stops.
6. HCD reads the USBCMD register to check if the single step execution is completed (HCHalted=1).
7. HCD checks results of TD execution. Go to step 4 to execute next TD or step 8 to end Software Debug mode.
8. HCD ends Software Debug mode by setting SWDBG bit to 0.
9. HCD sets up normal command list and Frame List table.
10. HCD sets Run/Stop bit to 1 to resume normal schedule execution.

In Software Debug mode, when the Run/Stop bit is set, the Host Controller starts. When a valid TD is found, the Run/Stop bit is reset. When the TD is finished, the HCHalted bit in the USBSTS register (bit 5) is set.

The SW Debug mode skips over inactive TDs and only halts after an active TD has been executed. When the last active TD in a frame has been executed, the Host Controller waits until the next SOF is sent and then fetches the first TD of the next frame before halting.

This HCHalted bit can also be used outside of Software Debug mode to indicate when the Host Controller has detected the Run/Stop bit and has completed the current transaction. Outside of the Software Debug mode, setting the Run/Stop bit to 0 always resets the SOF counter so that when the Run/Stop bit is set the Host Controller starts over again from the frame list location pointed to by the Frame List Index (see FRNUM Register description) rather than continuing where it stopped.

11.2.2 USBSTA—USB Status Register

I/O Offset:	Base + (02–03h)	Attribute:	R/WC
Default Value:	0020h	Size:	16 bits

This register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to 0 in this register by writing a 1 to it.

Bit	Description
15:6	Reserved.
5	**HCHalted**—R/WC: 0 = Software resets this bit to 0 by writing a 1 to the bit position. 1 = The Host Controller has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware (debug mode or an internal error). Default.
4	**Host Controller Process Error**—R/WC. 0 = Software resets this bit to 0 by writing a 1 to the bit position. 1 = The Host Controller has detected a fatal error. This indicates that the Host Controller suffered a consistency check failure while processing a Transfer Descriptor. An example of a consistency check failure would be finding an illegal PID field while processing the packet header portion of the TD. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further schedule execution. A hardware interrupt is generated to the system.
3	**Host System Error**—R/WC. 0 = Software resets this bit to 0 by writing a 1 to the bit position. 1 = A serious error occurred during a host system access involving the Host Controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system.
2	**Resume Detect (RSM_DET)**—R/WC: 0 = Software resets this bit to 0 by writing a 1 to the bit position. 1 = The Host Controller received a “RESUME” signal from a USB device. This is only valid if the Host Controller is in a global suspend state (bit 3 of Command register = 1).
1	**USB Error Interrupt**—R/WC: 0 = Software resets this bit to 0 by writing a 1 to the bit position. 1 = Completion of a USB transaction resulted in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set.
0	**USB Interrupt (USBINT)**—R/WC: 0 = Software resets this bit to 0 by writing a 1 to the bit position. 1 = The Host Controller sets this bit when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. Also set when a short packet is detected (actual length field in TD is less than maximum length field in TD), and short packet detection is enabled in that TD.

11.2.3 USBINTR—Interrupt Enable Register

I/O Offset:	Base + (04–05h)	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Fatal errors (Host Controller Processor Error-bit 4, USBSTS Register) cannot be disabled by the host controller. Interrupt sources that are disabled in this register still appear in the Status Register to allow the software to poll for events.

Bit	Description
15:4	Reserved.
3	**Short Packet Interrupt Enable**—R/W: 0 = Disabled. 1 = Enabled.
2	**Interrupt On Complete (IOC) Enable**—R/W: 0 = Disabled. 1 = Enabled.
1	**Resume Interrupt Enable**—R/W: 0 = Disabled. 1 = Enabled.
0	**Timeout/CRC Interrupt Enable**—R/W: 0 = Disabled. 1 = Enabled.

11.2.4 FRNUM—Frame Number Register

I/O Offset:	Base + (06–07h)	Attribute:	R/W (Word Writes Only)
Default Value:	0000h	Size:	16 bits

Bits [10:0] of this register contain the current frame number which is included in the frame SOF packet. This register reflects the count value of the internal frame number counter. Bits [9:0] are used to select a particular entry in the Frame List during scheduled execution. This register is updated at the end of each frame time.

This register must be written as a word. Byte writes are not supported. This register cannot be written unless the Host Controller is in the STOPPED state as indicated by the HCHalted bit (USBSTS register). A write to this register while the Run/Stop bit is set (USBCMD register) is ignored.

Bit	Description
15:11	Reserved.
10:0	**Frame List Current Index/Frame Number**—R/W. Provides the frame number in the SOF Frame. The value in this register increments at the end of each time frame (approximately every 1 ms). In addition, bits [9:0] are used for the Frame List current index and correspond to memory address signals [11:2].

11.2.5 FRBASEADD—Frame List Base Address Register

I/O Offset:	Base + (08–0Bh)	Attribute:	R/W
Default Value:	Undefined	Size:	32 bits

This 32-bit register contains the beginning address of the Frame List in the system memory. HCD loads this register prior to starting the schedule execution by the Host Controller. When written, only the upper 20 bits are used. The lower 12 bits are written as zero (4-KB alignment). The contents of this register are combined with the frame number counter to enable the Host Controller to step through the Frame List in sequence. The two least significant bits are always 00. This requires DWord alignment for all list entries. This configuration supports 1024 Frame List entries.

Bit	Description
31:12	**Base Address**—R/W. These bits correspond to memory address signals [31:12], respectively.
11:0	Reserved.

11.2.6 SOFMOD—Start of Frame Modify Register

I/O Offset:	Base + (0Ch)	Attribute:	R/W
Default Value:	40h	Size:	8 bits

This 1-byte register is used to modify the value used in the generation of SOF timing on the USB. Only the 7 least significant bits are used. When a new value is written into these 7 bits, the SOF timing of the next frame will be adjusted. This feature can be used to adjust out any offset from the clock source that generates the clock that drives the SOF counter. This register can also be used to maintain real time synchronization with the rest of the system so that all devices have the same sense of real time. Using this register, the frame length can be adjusted across the full range required by the USB specification. It's initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. It may be reprogrammed by USB system software at any time. Its value will take effect from the beginning of the next frame. This register is reset upon a Host Controller Reset or Global Reset. Software must maintain a copy of its value for reprogramming if necessary.

Bit	Description
7	Reserved.
6:0	**SOF Timing Value**—R/W. Guidelines for the modification of frame time are contained in Chapter 7 of the USB Specification. The SOF cycle time (number of SOF counter clock periods to generate a SOF frame length) is equal to 11936 + value in this field. The default value is decimal 64 which gives a SOF cycle time of 12000. For a 12 MHz SOF counter clock input, this produces a 1 ms Frame period. The following table indicates what SOF Timing Value to program into this field for a certain frame period. **Frame Length (# 12 MHz Clocks) (decimal)** / **SOF Reg. Value (decimal)** 11936 / 0 11937 / 1 . / . . / . 11999 / 63 12000 / 64 12001 / 65 . / . . / . 12062 / 126 12063 / 127

11.2.7 PORTSC[0,1]—Port Status and Control Register

I/O Offset:	Port 0/2/4: Base + (10–11h) Port 1/3/5: Base + (12–13h)	Attribute:	R/W (Word Writes Only)
Default Value:	0080h	Size:	16 bits

Note: For Function 0 this applies to ICH3 USB ports 0 and 1, for Function 1 this applies to ICH3 USB ports 2 and 3, and for Function 2 this applies to ICH3 USB ports 4 and 5.

After a Power-up reset, Global reset, or Host Controller reset, the initial conditions of a port are no device connected, Port disabled, and the bus line status is 00 (single-ended zero).

Bit	Description
15:13	Reserved—RO.
12	**Suspend**—R/W. This bit should not be written to a 1 if global suspend is active (bit 3=1 in the USBCMD register). Bit 2 and bit 12 of this register define the hub states as follows: **Bits [12,2] Hub State** X,0 Disable 0,1 Enable 1,1 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for single-ended 0 resets (global reset and port reset). The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. 0 = Port not in suspend state. 1 = Port in suspend state. **NOTE:** Normally, if a transaction is in progress when this bit is set, the port will be suspended when the current transaction completes. However, in the case of a specific error condition (out transaction with babble), the ICH3 may issue a start-of-frame, and then suspend the port.
11	**Overcurrent Indicator**—R/WC. Set by hardware 0 = Software clears this bit by writing a 1 to the bit position. 1 = Overcurrent pin has gone from inactive to active on this port.
10	**Overcurrent Active**—RO. This bit is set and cleared by hardware. 0 = Indicates that the overcurrent pin is inactive (high). 1 = Indicates that the overcurrent pin is active (low).
9	**Port Reset**—RO. 0 = Port is not in Reset. 1 = Port is in Reset. When set, the port is disabled and sends the USB Reset signaling.
8	**Low Speed Device Attached (LS)** —RO. Writes have no effect. 0 = Full speed device is attached. 1 = Low speed device is attached to this port.
7	Reserved—RO. Always read as 1.
6	**Resume Detect (RSM_DET)—**R/W. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected for at least 32 microseconds while the port is in the Suspend state. The ICH3 will then reflect the K-state back onto the bus as long as the bit remains a 1, and the port is still in the suspend state (bit 12,2 are 11). Writing a 0 (from 1) causes the port to send a low speed EOP. This bit will remain a 1 until the EOP has completed. 0 = No resume (K-state) detected/driven on port. 1 = Resume detected/driven on port.

Bit	Description
5:4	**Line Status**—RO. These bits reflect the D+ (bit 4) and D- (bit 5) signals lines' logical levels. These bits are used for fault detect and recovery as well as for USB diagnostics. This field is updated at EOF2 time (See Chapter 11 of the USB Specification).
3	**Port Enable/Disable Change**—R/WC. For the root hub, this bit gets set only when a port is disabled due to disconnect on that port or due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification). 0 = No change. Software clears this bit by writing a 1 to the bit location. 1 = Port enabled/disabled status has changed.
2	**Port Enabled/Disabled (PORT_EN)** —R/W. Ports can be enabled by host software only. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes and that there may be a delay in disabling or enabling a port if there is a transaction currently in progress on the USB. 0 = Disable. 1 = Enable.
1	**Connect Status Change**—R/WC. Indicates that a change has occurred in the port's Current Connect Status (see bit 0). The hub device sets this bit for any changes to the port device connect status, even if system software has not cleared a connect status change. If, for example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be setting" an already-set bit (i.e., the bit will remain set). However, the hub transfers the change bit only once when the Host Controller requests a data transfer to the Status Change endpoint. System software is responsible for determining state change history in such a case. 0 = No change. Software clears this bit by writing a 1 to the bit location. 1 = Change in Current Connect Status.
0	**Current Connect Status**—RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. 1 = Device is present on port.

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SMBus Controller Registers (D31:F3) 12

12.1 PCI Configuration Registers (SMBus—D31:F3)

Table 12-1. PCI Configuration Registers (SMBUS—D31:F3)

Offset	Mnemonic	Register Name/Function	Default	Type
00–01h	VID	Vendor ID	8086	RO
02–03h	DID	Device ID	2483h	RO
04–05h	CMD	Command Register	0000h	R/W
06–07h	STA	Device Status	0280h	R/W
08h	RID	Revision ID	See Note 2	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	05h	RO
0Bh	BCC	Base Class Code	0Ch	RO
20–23h	SMB_BASE	SMBus Base Address Register	00000001h	R/W
2C–2Dh	SVID	Subsystem Vendor ID	00h	RO
2E–2Fh	SID	Subsystem ID	00h	RO
3Ch	INTR_LN	Interrupt Line	00h	R/W
3Dh	INTR_PN	Interrupt Pin	02h	RO
40h	HOSTC	Host Configuration	00h	R/W

NOTES:
1. Registers that are not shown should be treated as Reserved (See Section 6.2 for details).
2. Refer to the Specification Update for the Revision ID.

12.1.1 VID—Vendor Identification Register (SMBUS—D31:F3)

Address: 00–01h Attributes: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Vendor Identification Value**—RO. This is a 16-bit value assigned to Intel.

12.1.2 DID—Device Identification Register (SMBUS—D31:F3)

Address: 02–03h Attributes: RO
Default Value: 2483h Size: 16 bits

Bit	Description
15:0	**Device Identification Value**—RO.

12.1.3 CMD—Command Register (SMBUS—D31:F3)

Address: 04–05h Attributes: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:10	Reserved.
9	Fast Back to Back Enable (FBE)—RO. Reserved as 0.
8	SERR# Enable (SERR_EN)—RO. Reserved as 0.
7	Wait Cycle Control (WCC)—RO. Reserved as 0.
6	Parity Error Response (PER)—RO. Reserved as 0.
5	VGA Palette Snoop (VPS)—RO. Reserved as 0.
4	Postable Memory Write Enable (PMWE) —RO. Reserved as 0.
3	Special Cycle Enable (SCE)—RO. Reserved as 0.
2	Bus Master Enable (BME)—RO. Reserved as 0.
1	Memory Space Enable (MSE) —RO. Reserved as 0.
0	**I/O Space Enable (IOE)**—R/W. 0 = Disable. 1 = Enables access to the SM Bus I/O space registers as defined by the Base Address Register.

12.1.4 STA—Device Status Register (SMBUS—D31:F3)

Address: 06–07h Attributes: RO, R/WC
Default Value: 0280h Size: 16 bits

Bit	Description
15	Detected Parity Error (DPE)—RO. Reserved as 0.
14	Signaled System Error (SSE)—RO. Reserved as 0.
13	Received Master Abort (RMA)—RO. Reserved as 0.
12	Received Target Abort (RTA)—RO. Reserved as 0.
11	**Signaled Target Abort (STA)**—R/WC**.** 0 = Software resets STA to 0 by writing a 1 to this bit location. 1 = Set when the function is targeted with a transaction that the ICH3 terminates with a target abort.
10:9	**DEVSEL# Timing Status (DEV_STS)**—RO**.** This 2-bit field defines the timing for DEVSEL# assertion for positive decode. 01 = Medium timing.
8	Data Parity Error Detected (DPED)—RO. Reserved as 0.
7	Fast Back to Back (FB2B)—RO. Reserved as 1.
6	User Definable Features (UDF)—RO. Reserved as 0.
5	66 MHz Capable (66MHZ_CAP)—RO. Reserved as 0.
4:0	Reserved.

12.1.5 RID—Revision Identification Register (SMBUS—D31:F3)

Address Offset: 08h
Default Value: See Note
Attribute: RO
Size: 8 Bits

Bit	Description
7:0	**Revision Identification Value**—RO.

NOTE: Refer to the Specification Update for the Revision ID.

12.1.6 SCC—Sub Class Code Register (SMBUS—D31:F3)

Address Offset: 0Ah
Default Value: 05h
Attributes: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code**—RO. 05h = SM Bus serial controller.

12.1.7 BCC—Base Class Code Register (SMBUS—D31:F3)

Address Offset: 0Bh
Default Value: 0Ch
Attributes: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code**—RO. 0Ch = Serial controller.

12.1.8 SMB_BASE—SMBus Base Address Register (SMBUS—D31:F3)

Address Offset: 20–23h
Default Value: 00000001h
Attribute: R/W
Size: 32-bits

Bit	Description
31:16	Reserved—RO.
15:5	**Base Address**—R/W. Provides the 32 byte system I/O base address for the ICH3 SMB logic.
4:1	Reserved—RO.
0	**I/O Space Indicator**—RO. This read-only bit is always 1, indicating that the SMB logic is I/O mapped.

12.1.9 SVID—Subsystem Vendor ID Register (SMBUS—D31:F2/F4)

Address Offset:	2Ch–2Dh	Attribute:	RO
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem Vendor ID**—RO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE_SVID register.

12.1.10 SID—Subsystem ID Register (SMBUS—D31:F2/F4)

Address Offset:	2Eh–2Fh	Attribute:	RO
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem ID**—R/Write-Once. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE_SID register.

12.1.11 INTR_LN—Interrupt Line Register (SMBUS—D31:F3)

Address Offset:	3Ch	Attributes:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)**—R/W. This data is not used by the ICH3. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

12.1.12 INTR_PN—Interrupt Pin Register (SMBUS—D31:F3)

Address Offset:	3Dh	Attributes:	RO
Default Value:	02h	Size:	8 bits

Bit	Description
7:0	**Interrupt Pin (INT_PN)**—RO. 02h = Indicates that the ICH3 SMBus Controller will drive PIRQB# as its interrupt line.

12.1.13 HOSTC—Host Configuration Register (SMBUS—D31:F3)

Address Offset:	40h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:3	Reserved.
2	**I²C_EN**—R/W. 0 = SMBus behavior. 1 = The ICH3 is enabled to communicate with I²C devices. This will change the formatting of some commands.
1	**SMB_SMI_EN**—R/W. 0 = SMBus interrupts will not generate an SMI#. 1 = Any source of an SMB interrupt will instead be routed to generate an SMI#. Refer to Section 5.17.4, “Interrupts / SMI#” on page 5-205. This bit needs to be set for SMBALERT# to be enabled.
0	**SMBus Host Enable (HST_EN)**—R/W. 0 = Disable the SMBus Host Controller. 1 = Enable. The SMB Host Controller interface is enabled to execute commands. The INTREN bit needs to be enabled for the SMB Host Controller to interrupt or SMI#. Note that the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared.

12.2 SMBus I/O Registers

Table 12-2. SMB I/O Registers

Offset	Mnemonic	Register Name	Default	Access
00h	HST_STS	Host Status	00h	R/W
02h	HST_CNT	Host Control	00h	R/W
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W
07h	BLOCK_DB	Block Data Byte	00h	R/W
08h	PEC	Packet Error Check	00h	R/W
09h	RCV_SLVA	Receive Slave Address	44h	R/W
0Ah	SLV_DATA	Slave Data	0000h	R/W
0Eh	SMLINK_PIN_CTL	SMLink Pin Control	04h	R/W
0Fh	SMBUS_PIN_CTL	SMBus Pin Control	04h	R/W
10h	SLV_STS	Slave Status	00h	R/WC
11h	SLV_CMD	Slave Command	00h	R/W
14h	NOTIFY_DADDR	Notify Device Address	00h	RO
16h	NOTIFY_DLOW	Notify Data Low Byte	00h	RO
17h	NOTIFY_DHIGH	Notify Data High Byte	00h	RO

12.2.1 HST_STS—Host Status Register

Register Offset:	00h	Attribute:	R/WC
Default Value:	00h	Size:	8-bits

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no effect.

Bit	Description
7	**BYTE_DONE_STS**—R/WC. 0 = Cleared by writing a 1 to the bit position. 1 = The ICH3 has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands). This bit will be set even on the last byte of the transfer. It will not be set when transmission is due to the Alert On LAN* heartbeat.
6	**INUSE_STS**—R/WC (special). This bit is used as semaphore among various independent software threads that may need to use the ICH3's SMBus logic, and has no other effect on hardware. 0 = After a full PCI reset, a read to this bit returns a 0. 1 = After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller.
5	**SMBALERT_STS**—R/WC. 0 = Interrupt or SMI# was not generated by SMBALERT#. 1 = The source of the interrupt or SMI# was the SMBALERT# signal. This bit is only cleared by software writing a 1 to the bit position or by RSMRST# going low. If the signal is programmed as a GPIO, then this bit will never be set.
4	**FAILED**—R/WC. 0 = Cleared by writing a 1 to the bit position. 1 = The source of the interrupt or SMI# was a failed bus transaction. This bit is set in response to the KILL bit being set to terminate the host transaction.
3	**BUS_ERR**—R/WC. 0 = Cleared by writing a 1 to the bit position. 1 = The source of the interrupt of SMI# was a transaction collision.
2	**DEV_ERR**—R/WC. The source of the interrupt or SMI# was due to one of the following: • Illegal Command Field, • Unclaimed Cycle (host initiated), • Host Device Time-out Error.] 0 = Software resets this bit by writing a 1 to this location. The ICH3 will then deassert the interrupt or SMI#.
1	**INTR**—R/WC (special). This bit can only be set by termination of a command. INTR is not dependent on the INTREN bit of the Host Controller Register (offset 02h). It is only dependent on the termination of the command. If the INTREN bit is not set, then the INTR bit will be set, although the interrupt will not be generated. Software can poll the INTR bit in this non-interrupt case. 0 = Software resets this bit by writing 1 to this location. The ICH3 will then deassert the interrupt or SMI#. 1 = The source of the interrupt or SMI# was the successful completion of its last command.
0	**HOST_BUSY**—RO. 0 = Cleared by the ICH3 when the current transaction is completed. 1 = Indicates that the ICH3 is running a command from the host interface. No SMB registers should be accessed while this bit is set, except the BLOCK DATA BYTE Register. The BLOCK DATA BYTE Register can be accessed when this bit is set only when the SMB_CMD bits in the Host Control Register are programmed for Block command or I^2C Read command. This is necessary in order to check the BYTE_DONE_STS bit.

12.2.2 HST_CNT—Host Control Register

Register Offset: 02h
Default Value: 00h
Attribute: R/W
Size: 8-bits

Bit	Description
7	**PEC_EN**—R/W 0 = SMBus host controller does not perform the transaction with the PEC phase appended. 1 = Causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. This bit must be written prior to the write in which the **START** bit is set.
6	**START**—WO. 0 = This bit will always return 0 on reads. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the ICH3 has finished the command. 1 = Writing a 1 to this bit initiates the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position.
5	**LAST_BYTE**—WO. This bit is used for Block Read commands. 1 = Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the ICH3 to send a NACK (instead of an ACK) after receiving the last byte. **NOTE:** Once the SECOND_TO_STS bit in TCO2_STS register (D31:F0, TCOBASE+6h, bit 1) is set, the LAST_BYTE bit also gets set. While the SECOND_TO_STS bit is set, the LAST_BYTE bit cannot be cleared. This prevents the ICH3 from running some of the SMBus commands (Block Read/Write, I^2C Read, Block I^2C Write).
4:2	**SMB_CMD**—R/W. The bit encoding below indicates which command the ICH3 is to perform. If enabled, the ICH3 will generate an interrupt or SMI# when the command has completed If the value is for a non-supported or reserved command, the ICH3 will set the device error (DEV_ERR) status bit and generate an interrupt when the START bit is set. The ICH3 will perform no command, and will not operate until DEV_ERR is cleared. **000 = Quick**: The slave address and read/write value (bit 0) are stored in the transmit slave address register. **001 = Byte**: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. **010 = Byte Data**: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. **011 = Word Data**: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes, DATA0 and DATA1 registers contain the read data. 100 = Process Call: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. **101 = Block**: This command uses the transmit slave address, command, DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. **110 = I^2C Read**: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The ICH3 will continue reading data until the NAK is received. **111** = Reserved.
1	**KILL**—R/W. 0 = Normal SMBus Host Controller functionality. 1 = When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#). This bit, once set, must be cleared by software to allow the SMBus Host Controller to function normally.
0	**INTREN**—R/W. 0 = Disable. 1 = Enable the generation of an interrupt or SMI# upon the completion of the command.

12.2.3 HST_CMD—Host Command Register

Register Offset: 03h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	This eight bit field is transmitted by the host controller in the command field of the SMBus protocol during the execution of any command.

12.2.4 XMIT_SLVA—Transmit Slave Address Register

Register Offset: 04h
Default Value: 00h
Attribute: R/W
Size: 8 bits

This register is transmitted by the host controller in the slave address field of the SMBus protocol.

Bit	Description
7:1	**Address**—R/W. 7-bit address of the targeted slave.
0	**Read/Write Control (RW)**—R/W. Direction of the host transfer. 0 = Write. 1 = Read.

12.2.5 HST_D0—Data 0 Register

Register Offset: 05h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**DATA0/COUNT**—R/W. This field contains the eight bit data sent in the DATA0 field of the SMBus protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

12.2.6 HST_D1—Data 1 Register

Register Offset: 06h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**DATA1**—R/W. This eight bit register is transmitted in the DATA1 field of the SMBus protocol during the execution of any command.

12.2.7 BLOCK_DB—Block Data Byte Register

Register Offset:	07h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Block Data Byte**—R/W. For Block Writes, the software will write the first byte to this register as part of the setup for this command. After the ICH3 has sent the Address, Command, and Byte Count fields, it will send the byte in the Block Data Byte register. After the byte has been sent, the ICH3 will set the BYTE_DONE_STS bit in the Host Status register. If there are more bytes to send, the software then writes the next byte to the Block Data Byte register and subsequently clears the BYTE_DONE_STS bit. The ICH3 will then send the next byte. During the time from when a byte has been transmitted to when the next byte has been loaded, the ICH3 will insert wait-states on the SMBus/I^2C. A similar process will be used for Block Reads. After receiving the byte count (which goes in the DATA 0 register), the first “data byte” goes in the Block Data Byte register and the ICH3 will generate an SMI# or interrupt (depending on configuration). The interrupt or SMI# handler will then read the byte and clear the BYTE_DONE_STS bit. This will free room for the next byte. During the time from when a byte is read to when the BYTE_DONE_STS bit is cleared, the ICH3 will insert wait-states on the SMBus/I^2C.

12.2.8 PEC—Packet Error Check (PEC) Register

Register Offset:	08h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**PEC_DATA**—R/W. This 8-bit register is written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

12.2.9 RCV_SLVA—Receive Slave Address Register

Register Offset:	09h	Attribute:	R/W
Default Value:	44h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7	Reserved.
6:0	**SLAVE_ADDR**—R/W. This field is the slave address that the ICH3 decodes for read and write cycles. the default is not 0, so the SMBus Slave Interface can respond even before the processor comes up (or if the processor is dead). This register is cleared by RSMRST#, but not by PCIRST#.

12.2.10 SLV_DATA—Receive Slave Data Register

Register Offset:	0Ah	Attribute:	RO
Default Value:	00h	Size:	16 bits
Lockable:	No	Power Well:	Resume

This register contains the 16-bit data value written by the external SMBus master. The processor can then read the value from this register. This register is reset by RSMRST#, but not PCIRST#

Bit	Description
15:8	**Data Message Byte 1 (DATA_MSG1)**—RO. See Section 5.17.6 for a discussion of this field.
7:0	**Data Message Byte 0 (DATA_MSG0)**—RO. See Section 5.17.6 for a discussion of this field.

12.2.11 SMLINK_PIN_CTL—SMLink Pin Control Register

Register Offset:	0Eh	Attribute:	R/W
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#

Bit	Description
7:3	Reserved.
2	**SMLINK_CLK_CTL**—R/W. This Read/Write bit has a default of 1. 0 = ICH3 will drive the SMLINK[0] pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK[0] pin. 1 = The SMLINK[0] pin is *Not* overdriven low. The other SMLINK logic controls the state of the pin.
1	**SMLINK[1]_CUR_STS**—R/W. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLINK[1] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	**SMLINK[0]_CUR_STS**—R/W. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLINK[0] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

12.2.12 SMBUS_PIN_CTL—SMBus Pin Control Register

Register Offset:	0Fh	Attribute:	R/W
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:3	Reserved.
2	**SMBCLK_CTL**—R/W. This Read/Write bit has a default of 1. 0 = ICH3 will drive the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. 1 = The SMBCLK pin is *Not* overdriven low. The other SMBus logic controls the state of the pin.
1	**SMBDATA_CUR_STS**—R/W. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBDATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	**SMBCLK_CUR_STS**—R/W. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBCLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

12.2.13 SLV_STS—Slave Status Register

Register Offset:	10h	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll this register until a write takes effect before assuming that a write has completed internally.

Bit	Description
7:1	Reserved.
0	**HOST_NOTIFY_STS**—R/WC. The ICH3 sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMLink pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the ICH3 will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the ICH3 will NACK the first byte (host address) of any new “Host Notify” commands on the SMLink. Writing a 0 to this bit has no effect.

12.2.14 SLV_CMD—Slave Command Register

Register Offset:	11h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#

Bit	Description
7:2	Reserved.
2	**SMBALERT_DIS**—R/W. 0 = Allows the generation of the interrupt or SMI#. 1 = Software sets this bit to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit. The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	**HOST_NOTIFY_WKEN**—R/W. Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is “OR”ed in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register.
0	**HOST_NOTIFY_INTREN**—R/W. Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQ[B]# or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by ANDing the STS and INTREN bits.

12.2.15 NOTIFY_DADDR—Notify Device Address

Register Offset:	14h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:1	**DEVICE_ADDRESS**—RO. This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	Reserved.

12.2.16 NOTIFY_DLOW—Notify Data Low Byte Register

Register Offset:	16h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_LOW_BYTE**—RO. This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

12.2.17 NOTIFY_DHIGH—Notify Data High Byte Register

Register Offset:	17h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_HIGH_BYTE**—RO. This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

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AC '97 Audio Controller Registers (D31:F5) 13

13.1 AC '97 Audio PCI Configuration Space (D31:F5)

Note: Registers that are not shown should be treated as Reserved (See Section 6.2 for details).

Table 13-1. PCI Configuration Map (Audio—D31:F5)

Offset	Mnemonic	Register	Default	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2485h	RO
04–05h	PCICMD	PCI Command	0000	R/W
06–07h	PCISTS	PCI Device Status	0280h	R/WC
08h	RID	Revision Identification	See Note	RO
09h	PI	Programming Interface	00	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	04h	RO
0Eh	HEDT	Header Type	00	RO
10–13h	NAMBAR	Native Audio Mixer Base Address	00000001h	R/W
14–17h	NABMBAR	Native Audio Bus Mastering Base Address	00000001h	R/W
2C–2Dh	SVID	Subsystem Vendor ID	0000h	Write-Once
2E–2Fh	SID	Subsystem ID	0000h	Write-Once
3Ch	INTR_LN	Interrupt Line	00h	R/W
3Dh	INTR_PN	Interrupt Pin	02h	RO
40h	PCID	Programmable Codec ID	01h	R/W

NOTE: Refer to the Specification Update for the Revision ID.

13.1.1 VID—Vendor Identification Register (Audio—D31:F5)

Offset:	00–01h	Attribute:	RO
Default Value:	8086h	Size:	16 Bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Vendor Identification Value.** This is a 16-bit value assigned to Intel.

13.1.2 DID—Device Identification Register (Audio—D31:F5)

Offset:	02–03h	Attribute:	RO
Default Value:	2485h	Size:	16 Bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Device Identification Value.**

13.1.3 PCICMD—PCI Command Register (Audio—D31:F5)

Address Offset:	04–05h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCICMD is a 16-bit control register. Refer to the PCI 2.2 specification for complete details on each bit.

Bit	Description
15:10	Reserved. Read 0.
9	Fast Back to Back Enable (FBE). Not implemented. Hardwired to 0.
8	SERR# Enable (SERR_EN). Not implemented. Hardwired to 0.
7	Wait Cycle Control (WCC). Not implemented. Hardwired to 0.
6	Parity Error Response (PER). Not implemented. Hardwired to 0.
5	VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE). Not implemented. Hardwired to 0.
3	Special Cycle Enable (SCE). Not implemented. Hardwired to 0.
2	**Bus Master Enable (BME)**—R/W. Controls standard PCI bus mastering capabilities. 0 = Disable. 1 = Enable.
1	Memory Space Enable (MSE). Hardwired to 0, AC '97 does not respond to memory accesses
0	**I/O Space Enable (IOE)**—R/W. This bit controls access to the AC '97 Audio Controller I/O space registers. 0 = Disable (Default). 1 = Enable access to I/O space. The Native PCI Mode Base Address register should be programmed prior to setting this bit.

13.1.4 PCISTS—PCI Device Status Register (Audio—D31:F5)

Offset:	06–07h	Attribute:	R/WC
Default Value	0280h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCISTA is a 16-bit status register. Refer to the PCI 2.2 specification for complete details on each bit.

Bit	Description
15	Detected Parity Error (DPE). Not implemented. Hardwired to 0.
14	Signaled System Error (SSE). Not implemented. Hardwired to 0.
13	**Master Abort Status (MAS)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Bus Master AC '97 2.2 interface function, as a master, generates a master abort.
12	Reserved. Will always read as 0.
11	Signaled Target Abort (STA). Not implemented. Hardwired to 0.
10:9	**DEVSEL# Timing Status (DEV_STS)**—RO. This 2-bit field reflects the ICH3's DEVSEL# timing when performing a positive decode. 01b = Medium timing.
8	Data Parity Error Detected (DPED). Not implemented. Hardwired to 0.
7	Fast Back to Back (FB2B). Hardwired to 1. This bit indicates that the ICH3 as a target is capable of fast back-to-back transactions.
6	User Definable Features (UDF). Not implemented. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP). Hardwired to 0.
4:0	Reserved. Read as 0s.

13.1.5 RID—Revision Identification Register (Audio—D31:F5)

Offset:	08h	Attribute:	RO
Default Value:	See Note	Size:	8 Bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Revision Identification Value**—RO.

NOTE: Refer to the Specification Update for the Revision ID.

13.1.6 PI—Programming Interface Register (Audio—D31:F5)

Offset:	09h	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	Programming Interface Value—RO.

13.1.7 SCC—Sub Class Code Register (Audio—D31:F5)

Address Offset:	0Ah	Attribute:	RO
Default Value:	01h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Sub Class Code**—RO. 01h = Audio Device.

13.1.8 BCC—Base Class Code Register (Audio—D31:F5)

Address Offset:	0Bh	Attribute:	RO
Default Value:	04h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Base Class Code**—RO. 04h = Multimedia device.

13.1.9 HEDT—Header Type Register (Audio—D31:F5)

Address Offset:	0Eh	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Header Type.** Hardwired to 00h.

13.1.10 NAMBAR—Native Audio Mixer Base Address Register (Audio—D31:F5)

Address Offset:	10–13h	Attribute:	R/W
Default Value:	00000001h	Size:	32 bits
Lockable:	No	Power Well:	Core

The Native PCI Mode Audio function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Native Audio Mixer software interface. The mixer requires 256 bytes of I/O space. Native Audio Mixer and Modem codec I/O registers are located from 00h to 7Fh and reside in the codec. Access to these registers will be decoded by the AC '97 controller and forwarded over the AC-link to the codec. The codec will then respond with the register value.

In the case of the split codec implementation, accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec.

For description of these I/O registers, refer to the *Audio Codec '97*, Revision 2.2 specification.

Bit	Description
31:16	Hardwired to 0s.
15:8	**Base Address**—R/W. These bits are used in the I/O space decode of the Native Audio Mixer interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 mixer, the upper 16 bits are hardwired to 0, while bits 15:8 are programmable. This configuration yields a maximum I/O block size of 256 bytes for this base address.
7:1	Reserved. Read as 0s.
0	**Resource Type Indicator (RTE)**—RO. Hardwired to 1, indicating a request for I/O space.

13.1.11 NABMBAR—Native Audio Bus Mastering Base Address Register (Audio—D31:F5)

Address Offset:	14–17h	Attribute:	R/W
Default Value:	00000001h	Size:	32 bits
Lockable:	No	Power Well:	Core

The Native PCI Mode Audio function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Native Mode Audio software interface.

Bit	Description
31:16	Hardwired to 0s.
15:6	**Base Address**—R/W. These bits are used in the I/O space decode of the Native Audio Bus Mastering interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For AC '97 bus mastering, the upper 16 bits are hardwired to 0, while bits 15:6 are programmable. This configuration yields a maximum I/O block size of 64 bytes for this base address.
5:1	Reserved. Read as 0s.
0	**Resource Type Indicator (RTE)**—RO. This bit is set to one, indicating a request for I/O space.

13.1.12 SVID—Subsystem Vendor ID Register (Audio—D31:F5)

Address Offset:	2D–2Ch	Attribute:	Read/Write-Once
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SVID register, in combination with the Subsystem ID register, enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

Bit	Description
15:0	**Subsystem Vendor ID**—R/WO.

13.1.13 SID—Subsystem ID Register (Audio—D31:F5)

Address Offset:	2E–2Fh	Attribute:	Read/Write-Once
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

Bit	Description
15:0	**Subsystem ID**—R/WO.

13.1.14 INTR_LN—Interrupt Line Register (Audio—D31:F5)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt line is used for the AC '97 module interrupt.

Bit	Description
7:0	**Interrupt Line (INT_LN)**—R/W. This data is not used by the ICH3. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

13.1.15 INTR_PN—Interrupt Pin Register (Audio—D31:F5)

Address Offset:	3Dh	Attribute:	RO
Default Value:	02h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt pin is used for the AC ’97 module interrupt. The AC ’97 interrupt is internally OR’ed to the interrupt controller with the PIRQB# signal.

Bit	Description
7:3	Reserved.
2:0	**Interrupt Pin (INT_PN)**—RO. Hardwired to 010b to select PIRQB#.

13.1.16 PCID—Programmable Codec ID Register (Audio—D31:F5)

Address Offset:	40h	Attribute:	R/W
Default Value:	01h	Size:	8 bits
Lockable:	No	Power Well:	Core

Note: The value in this register must only be modified prior to any AC ’97 codec accesses.

Bit	Description
7:2	Reserved.
1:0	**Secondary Codec ID (SCID)**—R/W. These two bits define the encoded ID that is used to address the secondary codec I/O space. The two bits are the ID that will be placed on slot-0, bits 0 and 1, upon an I/O access to the secondary codec. Bit 1 is the first bit sent and bit 0 is the second bit sent on AC_SDATA_OUT during slot 0.

13.2 AC ’97 Audio I/O Space (D31:F5)

The AC ’97 I/O space includes Native Audio Bus Master Registers and Native Mixer Registers. Table 13-2 shows the register addresses for the audio mixer registers.

Table 13-2. Intel® ICH3 Audio Mixer Register Configuration

Primary offset	Secondary Offset	NAMBAR Exposed Registers (D31:F5)
00h	80h	Reset
02h	82h	Master Volume Mute
04h	84h	Headphone Volume Mute
06h	86h	Master Volume Mono Mute
08h	88h	Master Tone (R & L)
0Ah	8Ah	PC_BEEP Volume Mute
0Ch	8Ch	Phone Volume Mute
0Eh	8Eh	Mic Volume Mute
10h	90h	Line In Volume Mute
12h	92h	CD Volume Mute
14h	94h	Video Volume Mute
16h	96h	Aux Volume Mute
18h	98h	PCM Out Volume Mute
1Ah	9Ah	Record Select
1Ch	9Ch	Record Gain Mute
1Eh	9Eh	Record Gain Mic Mute
20h	A0h	General Purpose
22h	A2h	3D Control
24h	A4h	AC ’97 RESERVED
26h	A6h	Powerdown Ctrl/Stat
28h	A8h	Extended Audio
2Ah	AAh	Extended Audio Ctrl/Stat
2Ch	ACh	PCM Front DAC Rate
2Eh	AEh	PCM Surround DAC Rate
30h	B0h	PCM LFE DAC Rate
32h	B2h	PCM LR ADC Rate
34h	B4h	MIC ADC Rate
36h	B6h	6Ch Vol: C, LFE Mute
38h	B8h	6Ch Vol: L, R Surround Mute
3A–56h	BA–F6h	Intel RESERVED
58h		**Vendor Reserved**
7Ah		**Vendor Reserved**
7Ch		**Vendor ID1**
7Eh		**Vendor ID2**

NOTE:
1. Registers in bold are multiplexed between audio and modem functions
2. Software should not try to access reserved registers

The Bus Master registers are located from offset + 00h to offset + 51h and reside in the AC ’97 controller. Accesses to these registers do **not** cause the cycle to be forwarded over the AC-link to the codec.

In the case of the split codec implementation accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec.

The Global Control (GLOB_CNT) and Global Status (GLOB_STA) registers are aliased to the same global registers in the audio and modem I/O space. Therefore a read/write to these registers in either audio or modem I/O space affects the same physical register.

Bus Mastering registers exist in I/O space and reside in the AC ’97 controller. The three channels, PCM in, PCM out, and Mic in, each have their own set of Bus Mastering registers. The following register descriptions apply to all three channels. The register definition section titles use a generic “x_” in front of the register to indicate that the register applies to all three channels. The naming prefix convention used in Table 13-3 and in the register description I/O address is as follows:

PI = PCM in channel
PO = PCM out channel
MC = Mic in channel.

Table 13-3. Native Audio Bus Master Control Registers

Offset	Mnemonic	Name	Default	Access
00h	PI_BDBAR	PCM In Buffer Descriptor list Base Address Register	00000000h	R/W
04h	PI_CIV	PCM In Current Index Value	00h	RO
05h	PI_LVI	PCM In Last Valid Index	00h	R/W
06h	PI_SR	PCM In Status Register	0001h	R/W
08h	PI_PICB	PCM In Position In Current Buffer	0000h	RO
0Ah	PI_PIV	PCM In Prefetched Index Value	00h	RO
0Bh	PI_CR	PCM In Control Register	00h	R/W
10h	PO_BDBAR	PCM Out Buffer Descriptor list Base Address Register	00000000h	R/W
14h	PO_CIV	PCM Out Current Index Value	00h	RO
15h	PO_LVI	PCM Out Last Valid Index	00h	R/W
16h	PO_SR	PCM Out Status Register	0001h	R/W
18h	PO_PICB	PCM Out Position In Current Buffer	0000h	RO
1Ah	PO_PIV	PCM Out Prefetched Index Value	00h	RO
1Bh	PO_CR	PCM Out Control Register	00h	R/W
20h	MC_BDBAR	Mic. In Buffer Descriptor list Base Address Register	00000000h	R/W
24h	PM_CIV	Mic. In Current Index Value	00h	RO
25h	MC_LVI	Mic. In Last Valid Index	00h	R/W
26h	MC_SR	Mic. In Status Register	0001h	R/W
28h	MC_PICB	Mic In Position In Current Buffer	0000h	RO
2Ah	MC_PIV	Mic. In Prefetched Index Value	00h	RO
2Bh	MC_CR	Mic. In Control Register	00h	R/W
2Ch	GLOB_CNT	Global Control	00000000h	R/W
30h	GLOB_STA	Global Status	00000000h	RO
34h	ACC_SEMA	Codec Write Semaphore Register	00h	R/W

13.2.1 *x*_BDBAR—Buffer Descriptor Base Address Register

I/O Address:	NABMBAR + 00h (PIBDBAR), NABMBAR + 10h (POBDBAR), NABMBAR + 20h (MCBDBAR)	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:3	**Buffer Descriptor Base Address[31:3]**—R/W. These bits represent address bits 31:3. The data should be aligned on 8-byte boundaries. Each buffer descriptor is 8 bytes long and the list can contain a maximum of 32 entries.
2:0	Hardwired to 0.

13.2.2 *x*_CIV—Current Index Value Register

I/O Address:	NABMBAR + 04h (PICIV), NABMBAR + 14h (POCIV), NABMBAR + 24h (MCCIV)	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single 32-bit read from address offset 04h. Software can also read this register individually by doing a single 8-bit read to offset 04h.

Bit	Description
7:5	Hardwired to 0.
4:0	**Current Index Value[4:0]**—RO. These bits represent which buffer descriptor within the list of 32 descriptors is currently being processed. As each descriptor is processed, this value is incremented. The value rolls over after it reaches 31.

13.2.3 *x*_LVI—Last Valid Index Register

I/O Address:	NABMBAR + 05h (PILVI), NABMBAR + 15h (POLVI), NABMBAR + 25h (MCLVI)	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single 32 bit read from address offset 04h. Software can also read this register individually by doing a single 8 bit read to offset 05h.

Bit	Description
7:5	Hardwired to 0.
4:0	**Last Valid Index[4:0]**—R/W. This value represents the last valid descriptor in the list. This value is updated by the software each time it prepares a new buffer and adds it to the list.

13.2.4 *x*_SR—Status Register

I/O Address:	NABMBAR + 06h (PISR), NABMBAR + 16h (POSR), NABMBAR + 26h (MCSR)	Attribute:	R/WC, RO
Default Value:	0001h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:5	Reserved.
4	**FIFO Error (FIFOE)**—R/WC. 0 = Cleared by writing a 1 to this bit position. 1 = FIFO error occurs. **PISR Register:** FIFO error indicates a FIFO overrun. The FIFO pointers don't increment, the incoming data is not written into the FIFO, thus is lost. **POSR Register:** FIFO error indicates a FIFO underrun. The sample transmitted in this case should be the last valid sample. The ICH3 will set the FIFOE bit if the under-run or overrun occurs when there are more valid buffers to process.
3	**Buffer Completion Interrupt Status (BCIS)**—R/WC. 0 = Cleared by writing a 1 to this bit position. 1 = Set by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until cleared by software.
2	**Last Valid Buffer Completion Interrupt (LVBCI)**—R/WC. 0 = Cleared by writing a 1 to this bit position. 1 = Last valid buffer has been processed. It remains active until cleared by software. This bit indicates the occurrence of the event signified by the last valid buffer being processed. Thus this is an event status bit that can be cleared by software once this event has been recognized. This event will cause an interrupt if the enable bit in the Control Register is set. The interrupt is cleared when the software clears this bit. In the case of *Transmits* (PCM out, Modem out) this bit is set, after the last valid buffer has been fetched (not after transmitting it). While in the case of *Receives*, this bit is set after the data for the last buffer has been written to memory.
1	**Current Equals Last Valid (CELV)**—RO. 0 = Cleared by hardware when controller exists state (i.e., until a new value is written to the LVI register.) 1 = Current Index is equal to the value in the Last Valid Index Register, and the buffer pointed to by the CIV has been processed (i.e., after the last valid buffer has been processed). This bit is very similar to bit 2, except this bit reflects the state rather than the event. This bit reflects the state of the controller, and remains set until the controller exits this state.
0	**DMA Controller Halted (DCH)**—RO. 1 = Halted. This could happen because of the Start/Stop bit being cleared, or it could happen once the controller has processed the last valid buffer (in which case it will set bit 1 and halt).

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single 32-bit read from address offset 04h. Software can also read this register individually by doing a single 16-bit read to offset 06h.

13.2.5 *x*_PICB—Position In Current Buffer Register

I/O Address:	NABMBAR + 08h (PIPICB), NABMBAR + 18h (POPICB), NABMBAR + 28h (MCPICB)	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Position In Current Buffer[15:0]**—RO. These bits represent the number of DWords left to be processed in the current buffer. Once again, this means, the number of samples not yet read from memory (in the case of reads from memory) or not yet written to memory (in the case of writes to memory), irrespective of the number of samples that have been transmitted/received across AC-link.

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single 16-bit read to offset 08h.

13.2.6 *x*_PIV—Prefetched Index Value Register

I/O Address:	NABMBAR + 0Ah (PIPIV), NABMBAR + 1Ah (POPIV), NABMBAR + 2Ah (MCPIV)	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Hardwired to 0.
4:0	**Prefetched Index Value[4:0]**—RO. These bits represent which buffer descriptor in the list has been prefetched. The bits in this register are also modulo 32 and roll over after they reach 31.

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single 8-bit read to offset 0Ah.

13.2.7 *x*_CR—Control Register

I/O Address:	NABMBAR + 0Bh (PICR), NABMBAR + 1Bh (POCR), NABMBAR + 2Bh (MCCR)	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Reserved.
4	**Interrupt On Completion Enable (IOCE)**—R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. 0 = Disable. Interrupt will not occur. 1 = Enable.
3	**FIFO Error Interrupt Enable (FEIE)**—R/W. This bit controls whether the occurrence of a FIFO error will cause an interrupt or not. 0 = Disable. Bit 4 in the Status Register will be set, but the interrupt will not occur. 1 = Enable. Interrupt will occur.
2	**Last Valid Buffer Interrupt Enable (LVBIE)**—R/W. This bit controls whether the completion of the last valid buffer will cause an interrupt or not. 0 = Disable. Bit 2 in the Status register will still be set, but the interrupt will not occur. 1 = Enable.
1	**Reset Registers (RR)**—R/W (special). 0 = Removes reset condition. 1 = Contents of all Bus master related registers to be reset, except the interrupt enable bits (bit 4,3,2 of this register). Software needs to set this bit but need not clear it since the bit is self clearing. This bit must be set only when the Run/Pause bit is cleared. Setting it when the Run bit is set will cause undefined consequences.
0	**Run/Pause Bus Master (RPBM)**—R/W. 0 = Pause bus master operation. This results in all state information being retained (i.e., master mode operation can be stopped and then resumed). 1 = Run. Bus master operation starts.

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single 8-bit read to offset 0Bh.

13.2.8 GLOB_CNT—Global Control Register

I/O Address:	NABMBAR + 2Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:22	Reserved.
21:20	**PCM 4/6 Enable**—R/W. Configures PCM Output for 2, 4 or 6 channel mode. 00 = 2-channel mode (default) 01 = 4-channel mode 10 = 6-channel mode 11 = Reserved
19:6	Reserved.
5	**Secondary Resume Interrupt Enable**—R/W. 0 = Disable. 1 = Enable an interrupt to occur when the secondary codec causes a resume event on the AC-link.
4	**Primary Resume Interrupt Enable**—R/W. 0 = Disable. 1 = Enable an interrupt to occur when the primary codec causes a resume event on the AC-link.
3	**ACLINK Shut Off**—R/W. 0 = Normal operation. 1 = Drive all AC '97 outputs low and turn off all AC '97 input buffer enables
2	**AC '97 Warm Reset**—R/W (special). 0 = Normal operation. 1 = Writing a 1 to this bit causes a warm reset to occur on the AC-link. The warm reset will awaken a suspended codec without clearing its internal registers. If software attempts to perform a warm reset while bit_clk is running, the write will be ignored and the bit will not change. This bit is self-clearing (it remains set until the reset completes and bit_clk is seen on the ACLink, after which it clears itself).
1	**AC '97 Cold Reset#**—R/W. 0 = Writing a 0 to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed. 1 = This bit defaults to 0; hence, after reset, the driver needs to set this bit to a 1.
0	**GPI Interrupt Enable (GIE)**—R/W. This bit controls whether the change in status of any GPI causes an interrupt. 0 = Bit 0 of the Global Status Register is set, but no interrupt is generated. 1 = The change on value of a GPI causes an interrupt and sets bit 0 of the Global Status Register.

13.2.9 GLOB_STA—Global Status Register

I/O Address:	NABMBAR + 30h	Attribute:	RO, R/W, R/WC
Default Value:	00300000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:22	Reserved.
21	**6 Channel Capability (6CH_CAP)**—RO. Hardwired to 1 in the ICH3. 0 = The AC '97 Controller does not support 6-channel PCM Audio output. 1 = The AC '97 Controller supports 6-channel PCM Audio output.
20	**4 Channel Capability (4CH_CAP)**—RO. Hardwired to '1' in the ICH3. 0 = The AC '97 Controller does not support 4-channel PCM Audio output. 1 = The AC '97 Controller supports 4-channel PCM Audio output.
19:18	Reserved.
17	**MD3**—R/W. Power down semaphore for Modem. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the AD3 bit to coordinate the entry of the two codecs into D3 state.
16	**AD3**—R/W. Power down semaphore for Audio. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the MD3 bit to coordinate the entry of the two codecs into D3 state.
15	**Read Completion Status (RCS)**—R/WC. This bit indicates the status of codec read completions. 0 = A codec read completes normally. 1 = A codec read results in a time-out. The bit remains set until being cleared by software writing a 1 to the bit location.
14	**Bit 3 of slot 12**—RO. Display bit 3 of the most recent slot 12.
13	**Bit 2 of slot 12**—RO. Display bit 2 of the most recent slot 12.
12	**Bit 1 of slot 12**—RO. Display bit 1 of the most recent slot 12.
11	**Secondary Resume Interrupt (SRI)**—R/WC. This bit indicates that a resume event occurred on AC_SDIN[1]. 0 = Cleared by writing a 1 to this bit position. 1 = Resume event occurred.
10	**Primary Resume Interrupt (PRI)**—R/WC. This bit indicates that a resume event occurred on AC_SDIN[0]. 0 = Cleared by writing a 1 to this bit position. 1 = Resume event occurred.
9	**Secondary Codec Ready (SCR)**—RO. Reflects the state of the codec ready bit in AC_SDIN[1]. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
8	**Primary Codec Ready (PCR)**—RO. Reflects the state of the codec ready bit in AC_SDIN [0]. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
7	**Mic In Interrupt (MINT)**—RO. This bit indicates that one of the Mic in channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.

Bit	Description
6	**PCM Out Interrupt (POINT)**—RO. This bit indicates that one of the PCM out channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred. 0 =
5	**PCM In Interrupt (PIINT)**—RO. This bit indicates that one of the PCM in channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.
4:3	Reserved.
2	**Modem Out Interrupt (MOINT)**—RO. This bit indicates that one of the modem out channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.
1	**Modem In Interrupt (MIINT)**—RO. This bit indicates that one of the modem in channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.
0	**GPI Status Change Interrupt (GSCI)**—RWC. This bit reflects the state of bit 0 in slot 12, and is set whenever bit 0 of slot 12 is set. This happens when the value of any of the GPIOs currently defined as inputs changes. 0 = Cleared by writing a 1 to this bit position. 1 = Input changed.

13.2.10 CAS—Codec Access Semaphore Register

I/O Address:	NABMBAR + 34h	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:1	Reserved.
0	**Codec Access Semaphore (CAS)**—R/W (special). This bit is read by software to check whether a codec access is currently in progress. 0 = No access in progress. 1 = The act of reading this register sets this bit to 1. The driver that read this bit can then perform an I/O access. Once the access is completed, hardware automatically clears this bit.

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AC ’97 Modem Controller Registers (D31:F6) 14

14.1 AC ’97 Modem PCI Configuration Space (D31:F6)

Note: Registers that are not shown should be treated as Reserved (See Section 6.2 for details).

Table 14-1. PCI Configuration Map (Modem—D31:F6)

Offset	Mnemonic	Register	Default	Access
00–01h	VID	Vendor Identification	8086	RO
02–03h	DID	Device Identification	2486h	RO
04–05h	PCICMD	PCI Command	0000	R/W
06–07h	PCISTA	PCI Device Status	0280h	R/WC
08h	RID	Revision Identification	See Note	RO
09h	PI	Programming Interface	00	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	07h	RO
0Eh	HEDT	Header Type	00	RO
10–13h	MMBAR	Modem Mixer Base Address	00000001h	R/W
14–17h	MBAR	Modem Base Address	00000001h	R/W
2C–2Dh	SVID	Subsystem Vendor ID	0000h	Write-Once
2E–2Fh	SID	Subsystem ID	0000h	Write-Once
3Ch	INTR_LN	Interrupt Line	00h	RO
3Dh	INT_PN	Interrupt Pin	02h	RO

NOTE: Refer to the Specification Update for the Revision ID.

14.1.1 VID—Vendor Identification Register (Modem—D31:F6)

Address Offset: 00–01h
Default Value: 8086
Lockable: No
Attribute: RO
Size: 16 Bits
Power Well: Core

Bit	Description
15:0	**Vendor Identification Value.**

14.1.2 DID—Device Identification Register (Modem—D31:F6)

Address Offset:	02–03h	Attribute:	RO
Default Value:	2486h	Size:	16 Bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Device Identification Value.**

14.1.3 PCICMD—PCI Command Register (Modem—D31:F6)

Address Offset:	04–05h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCICMD is a 16-bit control register. Refer to the *PCI Local Bus Specification*, Revision 2.2 for complete details on each bit.

Bit	Description
15:10	Reserved. Read 0.
9	Fast Back to Back Enable (FBE). Not implemented. Hardwired to 0.
8	SERR# Enable (SERR_EN). Not implemented. Hardwired to 0.
7	Wait Cycle Control (WCC). Not implemented. Hardwired to 0.
6	Parity Error Response (PER). Not implemented. Hardwired to 0.
5	VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE). Not implemented. Hardwired to 0.
3	Special Cycle Enable (SCE). Not implemented. Hardwired to 0.
2	**Bus Master Enable (BME)**—R/W. Controls standard PCI bus mastering capabilities. 0 = Disable. 1 = Enable.
1	Memory Space Enable (MSE). Hardwired to 0, AC '97 does not respond to memory accesses.
0	**I/O Space Enable (IOE)**—R/W. This bit controls access to the I/O space registers. 0 = Disable access. (default = 0). 1 = Enable access to I/O space. The Native PCI Mode Base Address register should be programmed prior to setting this bit.

14.1.4 PCISTA—Device Status Register (Modem—D31:F6)

Address Offset:	06–07h	Attribute:	R/WC
Default Value:	0280h	Size:	16 bits
Lockable:	No	Power Well:	Core

PCISTA is a 16-bit status register. Refer to the PCI 2.2 specification for complete details on each bit.

Bit	Description
15	Detected Parity Error (DPE)—RO. Not implemented. Hardwired to 0.
14	Signaled System Error (SSE)—RO. Not implemented. Hardwired to 0.
13	**Master Abort Status (MAS)**—R/WC. 0 = Software clears this bit by writing a 1 to the bit position. 1 = Bus Master AC '97 interface function, as a master, generates a master abort.
12	Reserved. Read as 0.
11	Signaled Target Abort (STA)—RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEV_STS)—RO. This 2-bit field reflects the ICH3's DEVSEL# timing parameter. These read only bits indicate the ICH3's DEVSEL# timing when performing a positive decode.
8	Data Parity Error Detected (DPED)—RO. Not implemented. Hardwired to 0.
7	Fast Back to Back (FB2B)—RO. Hardwired to 1. This bit indicates that the ICH3 as a target is capable of fast back-to-back transactions.
6	User Definable Features (UDF)—RO. Not implemented. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0.
4:0	Reserved. Read as 0's.

14.1.5 RID—Revision Identification Register (Modem—D31:F6)

Address Offset:	08h	Attribute:	RO
Default Value:	See Note	Size:	8 Bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Revision Identification Value**—RO.

NOTE: Refer to the Specification Update for the Revision ID.

14.1.6 PI—Programming Interface Register (Modem—D31:F6)

Address Offset:	09h	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Programming Interface Value**—RO.

14.1.7 SCC—Sub Class Code Register (Modem—D31:F6)

Address Offset:	0Ah	Attribute:	RO
Default Value:	03h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Sub Class Code**—RO. 03h = Generic Modem.

14.1.8 BCC—Base Class Code Register (Modem—D31:F6)

Address Offset:	0Bh	Attribute:	RO
Default Value:	07h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Base Class Code**—RO. 07h = Simple Communications Controller.

14.1.9 HEDT—Header Type Register (Modem—D31:F6)

Address Offset:	0Eh	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Header Type**—RO.

14.1.10 MMBAR—Modem Mixer Base Address Register (Modem—D31:F6)

Address Offset:	10–13h	Attribute:	R/W
Default Value:	00000001h	Size:	32 bits

The Native PCI Mode Modem uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Modem Mixer software interface. The mixer requires 256 bytes of I/O space. All accesses to the mixer registers are forwarded over the AC-link to the codec where the registers reside.

In the case of the split codec implementation accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec.

Bit	Description
31:16	Hardwired to 0s.
15:8	**Base Address**—R/W. These bits are used in the I/O space decode of the Modem interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 Modem, the upper 16 bits are hardwired to 0, while bits 15:8 are programmable. This configuration yields a maximum I/O block size of 256 bytes for this base address.
7:1	Reserved. Read as 0.
0	**Resource Type Indicator (RTE)**—RO. This bit is set to one, indicating a request for I/O space.

14.1.11 MBAR—Modem Base Address Register (Modem—D31:F6)

Address Offset:	14–17h	Attribute:	R/W
Default Value:	00000001h	Size:	32 bits

The Modem function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Modem software interface. The Modem Bus Mastering register space requires 128 bytes of I/O space. All Modem registers reside in the controller, therefore cycles are NOT forwarded over the AC-link to the codec.

Bit	Description
31:16	Hardwired to 0s.
15:7	**Base Address**—R/W. These bits are used in the I/O space decode of the Modem interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 Modem, the upper 16 bits are hardwired to 0, while bits 15:7 are programmable. This configuration yields a maximum I/O block size of 128 bytes for this base address.
6:1	Reserved. Read as 0.
0	**Resource Type Indicator (RTE)**—RO. This bit is set to one, indicating a request for I/O space.

14.1.12 SVID—Subsystem Vendor ID (Modem—D31:F6)

Address Offset:	2C–2Dh	Attribute:	Read/Write-Once
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SVID register, in combination with the Subsystem ID register, enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

Bit	Description
15:0	**Subsystem Vendor ID**—R/WO.

14.1.13 SID—Subsystem ID (Modem—D31:F6)

Address Offset:	2E–2Fh	Attribute:	Read/Write-Once
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from another.

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

Bit	Description
15:0	**Subsystem ID**—R/WO.

14.1.14 INTR_LN—Interrupt Line Register (Modem—D31:F6)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt line is used for the AC '97 module interrupt.

Bit	Description
7:0	**Interrupt Line (INT_LN)**—R/W. This data is not used by the ICH3. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

14.1.15 INT_PIN—Interrupt Pin (Modem—D31:F6)

Address Offset:	3Dh	Attribute:	RO
Default Value:	02h	Size:	8 bits
Lockable:	No	Power Well:	Core

This register indicates which PCI interrupt pin is used for the AC '97 modem interrupt. The AC '97 interrupt is internally ORed to the interrupt controller with the PIRQB# signal.

Bit	Description
7:3	Reserved.
2:0	**Interrupt Pin (INT_PN)**—RO. Hardwired to 010b to select PIRQB#.

14.2 AC ’97 Modem I/O Space (D31:F6)

In the case of the split codec implementation accesses to the modem mixer registers in different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec. Table 14-2 shows the register addresses for the modem mixer registers.

Table 14-2. Intel® ICH3 Modem Mixer Register Configuration

Register		MMBAR Exposed Registers (D31:F6)
Pri.	**Sec.**	**Name**
00h:38h	80h:B8h	Intel RESERVED
3Ch	BCh	Extended Modem ID
3Eh	BEh	Extended Modem Stat/Ctrl
40h	C0h	Line 1 DAC/ADC Rate
42h	*C2h*	*Line 2 DAC/ADC Rate*
44h	*C4h*	*Handset DAC/ADC Rate*
46h	C6h	Line 1 DAC/ADC Level Mute
48h	*C8h*	*Line 2 DAC/ADC Level Mute*
4Ah	*CAh*	*Handset DAC/ADC Level Mute*
4Ch	CCh	GPIO Pin Configuration
4Eh	CEh	GPIO Polarity/Type
50h	D0h	GPIO Pin Sticky
52h	D2h	GPIO Pin Wake Up
54h	D4h	GPIO Pin Status
56h	D6h	Misc. Modem AFE Stat/Ctrl
58h	**D8h**	**Vendor Reserved**
7Ah	**FAh**	**Vendor Reserved**
7Ch	**FCh**	**Vendor ID1**
7Eh	**FEh**	**Vendor ID2**

NOTE:
1. Registers in bold are multiplexed between audio and modem functions.
2. Registers in italics are for functions not supported by the ICH3.
3. Software should not try to access reserved registers.
4. The ICH3 supports a modem codec as either primary or secondary, but does not support two modem codecs.

The Global Control (GLOB_CNT) and Global Status (GLOB_STA) registers are aliased to the same global registers in the audio and modem I/O space. Therefore a read/write to these registers in either audio or modem I/O space affects the same physical register.

These registers exist in I/O space and reside in the AC ’97 controller. The two channels, Modem in and Modem out, each have their own set of Bus Mastering registers. The following register descriptions apply to both channels. The naming prefix convention used is as follows:
MI = Modem in channel
MO = Modem out channel

Table 14-3. Modem Registers

Offset	Mnemonic	Name	Default	Access
00h	MI_BDBAR	Modem In Buffer Descriptor List Base Address Register	00000000h	R/W
04h	MI_CIV	Modem In Current Index Value Register	00h	R
05h	MI_LVI	Modem In Last Valid Index Register	00h	R/W
06h	MI_SR	Modem In Status Register	0001h	R/W
08h	MI_PICB	Modem In Position In Current Buffer Register	00h	R
0Ah	MI_PIV	Modem In Prefetch Index Value Register	00h	RO
0Bh	MI_CR	Modem In Control Register	00h	R/W
10h	MO_BDBAR	Modem Out Buffer Descriptor List Base Address Register	00000000h	R/W
14h	MO_CIV	Modem Out Current Index Value Register	00h	RO
15h	MO_LVI	Modem Out Last Valid Register	00h	R/W
16h	MO_SR	Modem Out Status Register	0001h	R/W
18h	MI_PICB	Modem In Position In Current Buffer Register	00h	RO
1Ah	MO_PIV	Modem Out Prefetched Index Register	00h	RO
1Bh	MO_CR	Modem Out Control Register	00h	R/W
3Ch	GLOB_CNT	Global Control	00000000h	R/W
40h	GLOB_STA	Global Status	00000000h	RO
44h	ACC_SEMA	Codec Write Semaphore Register	00h	R/W

NOTE:
1. MI = Modem in channel; MO = Modem out channel

14.2.1 *x*_BDBAR—Buffer Descriptor List Base Address Register

I/O Address:	MBAR + 00h (MIBDBAR), MBAR + 10h (MOBDBAR)	Attribute:	R/W
Default Value:	00000000h	Size:	32bits
Lockable:	No	Power Well:	Core

Bit	Description
31:3	**Buffer Descriptor List Base Address[31:3]**—R/W. These bits represent address bits 31:3. The entries should be aligned on 8 byte boundaries.
2:0	Hardwired to 0.

14.2.2 *x*_CIV—Current Index Value Register

I/O Address:	MBAR + 04h (MICIV), MBAR + 14h (MOCIV),	Attribute:	RO
Default Value:	00h	Size:	8bits
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Hardwired to 0.
4:0	**Current Index Value [4:0]**—RO. These bits represent which buffer descriptor within the list of 16 descriptors is being processed currently. As each descriptor is processed, this value is incremented.

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single 32-bit read from address offset 04h. Software can also read this register individually by doing a single 8-bit read to offset 04h.

14.2.3 *x*_LVI—Last Valid Index Register

I/O Address:	MBAR + 05h (MILVI), MBAR + 15h (MOLVI)	Attribute:	R/W
Default Value:	00h	Size:	8bits
Power Well:	Core		

Bit	Description
7:5	Hardwired to 0.
4:0	**Last Valid Index [4:0]**—R/W. These bits indicate the last valid descriptor in the list. This value is updated by the software as it prepares new buffers and adds to the list.

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single 32-bit read from address offset 04h. Software can also read this register individually by doing a single 8-bit read to offset 05h.

14.2.4 x_SR—Status Register

I/O Address:	MBAR + 06h (MISR), MBAR + 16h (MOSR)	Attribute:	R/WC
Default Value:	0001h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:5	Reserved.
4	**FIFO Error (FIFOE)**—R/WC. 0 = Cleared by writing a 1 to this bit position. 1 = FIFO error occurs. **Modem in:** FIFO error indicates a FIFO overrun. The FIFO pointers don't increment, the incoming data is not written into the FIFO, thereby being lost. **Modem out:** FIFO error indicates a FIFO underrun. The sample transmitted in this case should be the last valid sample. The ICH3 will set the FIFOE bit if the under-run or overrun occurs when there are more valid buffers to process.
3	**Buffer Completion Interrupt Status (BCIS)**—R/WC. 0 = Cleared by writing a 1 to this bit position. 1 = Set by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. Remains active until software clears bit.
2	**Last Valid Buffer Completion Interrupt (LVBCI)**—R/WC. 0 = Cleared by writing a 1 to this bit position. 1 = Set by hardware when last valid buffer has been processed. It remains active until cleared by software. This bit indicates the occurrence of the event signified by the last valid buffer being processed. Thus, this is an event status bit that can be cleared by software once this event has been recognized. This event will cause an interrupt if the enable bit in the Control Register is set. The interrupt is cleared when the software clears this bit. In the case of transmits (PCM out, Modem out) this bit is set, after the last valid buffer has been fetched (not after transmitting it) While in the case of Receives, this bit is set after the data for the last buffer has been written to memory.
1	**Current Equals Last Valid (CELV)**—RO. 0 = Hardware clears when controller exists state (i.e., until a new value is written to the LVI register). 1 = Current Index is equal to the value in the Last Valid Index Register, AND the buffer pointed to by the CIV has been processed (i.e., after the last valid buffer has been processed). This bit is very similar to bit 2, except, this bit reflects the state rather than the event. This bit reflects the state of the controller, and remains set until the controller exits this state.
0	**DMA Controller Halted (DCH)**—RO. 1 = DMA controller is halted. This could happen because of the Start/Stop bit being cleared, or it could happen once the controller has processed the last valid buffer (in which case it will set bit 1 and halt).

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single 32-bit read from address offset 04h. Software can also read this register individually by doing a single 16-bit read to offset 06h.

14.2.5 *x*_PICB—Position In Current Buffer Register

I/O Address:	MBAR + 08h (MIPICB), MBAR + 18h (MOPICB),	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Position In Current Buffer[15:0]**—RO. These bits represent the number of DWords left to be processed in the current buffer.

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single 16-bit read to offset 08h.

14.2.6 *x*_PIV—Prefetch Index Value Register

I/O Address:	MBAR + 0Ah (MIPIV), MBAR + 1Ah (MOPIV)	Attribute:	RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Hardwired to 0
4:0	**Prefetched Index Value [4:0]**—RO. These bits represent which buffer descriptor in the list has been prefetched.

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single 8-bit read to offset 0Ah.

14.2.7 *x*_CR—Control Register

I/O Address:	MBAR + 0Bh (MICR), MBAR + 1Bh (MOCR)	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Reserved.
4	**Interrupt On Completion Enable (IOCE)**—R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. 0 = Disable. 1 = Enable.
3	**FIFO Error Interrupt Enable (FEIE)**—R/W. This bit controls whether the occurrence of a FIFO error will cause an interrupt or not. 0 = Disable. Bit 4 in the Status Register will be set, but the interrupt will not occur. 1 = Enable. Interrupt will occur.
2	**Last Valid Buffer Interrupt Enable (LVBIE)**—R/W. This bit controls whether the completion of the last valid buffer will cause an interrupt or not. 0 = Disable. Bit 2 in the Status register will still be set, but the interrupt will not occur. 1 = Enable.
1	**Reset Registers (RR)**—R/W (special). 0 = Removes reset condition. 1 = Contents of all registers to be reset, except the interrupt enable bits (bit 4,3,2 of this register). Software needs to set this bit. It must be set only when the Run/Pause bit is cleared. Setting it when the Run bit is set will cause undefined consequences. This bit is self-clearing (software needs not clear it).
0	**Run/Pause Bus Master (RPBM)**—R/W. 0 = Pause bus master operation. This results in all state information being retained (i.e., master mode operation can be stopped and then resumed). 1 = Run. Bus master operation starts.

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single 8-bit read to offset 0Bh.

14.2.8 GLOB_CNT—Global Control Register

I/O Address:	MBAR + 3Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:6	Reserved. **NOTE:** Software must preserve the value of these bits when writing to this register. This can be achieved by either not writing to the upper two bytes at all (with byte-writes to this register enabled) or by performing a read-modify-write to the entire 4-byte register.
5	**Secondary Resume Interrupt Enable**—R/W. 0 = Disable. 1 = Enable an interrupt to occur when the secondary codec causes a resume event on the AC-link.
4	**Primary Resume Interrupt Enable**—R/W. 0 = Disable. 1 = Enable an interrupt to occur when the primary codec causes a resume event on the AC-link.
3	**ACLINK Shut Off**—R/W. 0 = Normal operation. 1 = Disable the AC-link signals (drive all AC '97 outputs low and turn off all AC '97 input buffer enables).
2	**AC '97 Warm Reset**—R/W (special). 0 = This bit is self-clearing (it clears itself after the reset has occurred and BIT_CLK has started). 1 = Writing a 1 to this bit causes a warm reset to occur on the AC-link. The warm reset will awaken a suspended codec without clearing its internal registers. If software attempts to perform a warm reset while BIT_CLK is running, the write will be ignored and the bit will not be changed. A warm reset can only occur in the absence of BIT_CLK.
1	**AC '97 Cold Reset#**—R/W. 0 = Writing a 0 to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed. 1 = This bit defaults to 0; hence, after reset, the driver needs to set this bit to a 1.
0	**GPI Interrupt Enable (GIE)**—R/W. This bit controls whether the change in status of any GPI causes an interrupt. 0 = Bit 0 of the Global Status Register is set, but an interrupt is not generated. 1 = The change on value of a GPI causes an interrupt and sets bit 0 of the Global Status Register.

14.2.9 GLOB_STA—Global Status Register

I/O Address:	MBAR + 40h	Attribute:	RO, R/W, R/WC
Default Value:	00300000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:22	Reserved.
21	**6 Channel Capability (6CH_CAP)**—RO. Hardwired to 1 in the ICH3. 0 = The AC '97 Controller does not support 6-channel PCM Audio output. 1 = The AC '97 Controller supports 6-channel PCM Audio output.
20	**4 Channel Capability (4CH_CAP)**—RO. Hardwired to 1 in the ICH3. 0 = The AC '97 Controller does not support 4-channel PCM Audio output. 1 = The AC '97 Controller supports 4-channel PCM Audio output.
19:18	Reserved.
17	**MD3**—R/W. Power down semaphore for Modem. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the AD3 bit to coordinate the entry of the two codecs into D3 state.
16	**AD3**—R/W. Power down semaphore for Audio. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the MD3 bit to coordinate the entry of the two codecs into D3 state.
15	**Read Completion Status (RCS)**—R/W. This bit indicates the status of codec read completions. 0 = A codec read completes normally. 1 = A codec read results in a time-out. The bit remains set until being cleared by software.
14	**Bit 3 of slot 12**—RO. Display bit 3 of the most recent slot 12.
13	**Bit 2 of slot 12**—RO. Display bit 2 of the most recent slot 12.
12	**Bit 1 of slot 12**—RO. Display bit 1 of the most recent slot 12.
11	**Secondary Resume Interrupt (SRI)**—R/WC. This bit indicates that a resume event occurred on AC_SDIN[1]. 0 = Cleared by writing a 1 to this bit position. 1 = Resume event occurred.
10	**Primary Resume Interrupt (PRI)**—R/WC. This bit indicates that a resume event occurred on AC_SDIN[0]. 0 = Cleared by writing a 1 to this bit position. 1 = Resume event occurred.
9	**Secondary Codec Ready (SCR)**—RO. Reflects the state of the codec ready bit in AC_SDIN[1]. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
8	**Primary Codec Ready (PCR)**—RO. Reflects the state of the codec ready bit in AC_SDIN [0]. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is "ready", it must never go "not ready" spontaneously. 0 = Not Ready. 1 = Ready.
7	**Mic In Interrupt (MINT)**—RO. This bit indicates that one of the Mic in channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.
6	**PCM Out Interrupt (POINT)**—RO. This bit indicates that one of the PCM out channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.

Bit	Description
5	**PCM In Interrupt (PIINT)**—RO. This bit indicates that one of the PCM in channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.
4:3	Reserved.
2	**Modem Out Interrupt (MOINT)**—RO. This bit indicates that one of the modem out channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.
1	**Modem In Interrupt (MIINT)**—RO. This bit indicates that one of the modem in channel interrupts occurred. 0 = When the specific interrupt is cleared, this bit will be cleared. 1 = Interrupt occurred.
0	**GPI Status Change Interrupt (GSCI)**—RWC. This bit reflects the state of bit 0 in slot 12, and is set whenever bit 0 of slot 12 is set. This happens when the value of any of the GPIOs currently defined as inputs changes. 0 = Cleared by writing a 1 to this bit position. 1 = Input changed.

Note: On reads from a codec, the controller will give the codec a maximum of 4 frames to respond, after which if no response is received, it will return a dummy read completion to the processor (with all If's on the data) and also set the read completion status bit in the global status register.

14.2.10 CAS—Codec Access Semaphore Register

I/O Address:	NABMBAR + 44h	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:1	Reserved.
0	**Codec Access Semaphore (CAS)** —R/W (special). This bit is read by software to check whether a codec access is currently in progress. 0 = No access in progress. 1 = The act of reading this register sets this bit to 1. The driver that read this bit can then perform an I/O access. Once the access is completed, hardware automatically clears this bit.

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Ballout Definition 15

This section contains the ICH3 ballout information. Figure 15-1 and Figure 15-2 provide graphical illustrations of how the ballout maps to the 421-ball BGA package, and Table 15-1 provides the BGA ball list sorted alphabetically by signal name.

Figure 15-1. Intel® ICH3 Ballout (Topview—Left Side)

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	PIRQD#	REQ2#	GNT0#	PIRQH# / GPIO5	PIRQE# / GPIO2	AC_SYNC	LAN_RXD1	LAN_RXD2	LAN_TXD2	OC5#
B	PIRQA#	PIRQC#	GNTB# / GNT5# / GPIO17	GNT4#	PIRQF# / GPIO3	GNTA# / GPIO16	AC_BIT_CLK	VSS	LAN_TXD0	VSS	AC_SDIN0
C	PIRQB#	NC	VSS	REQA# / GPIO0	PIRQG# / GPIO4	VSS	AC_SDOUT	LAN_RXD0	LAN_CLK	LAN_TXD1	AC_SDIN1
D	AD28	GNT2#	REQ0#	REQB# / REQ5# / GPIO1	GNT3#	NC	LAN_RSTSYNC	EE_DIN	VSS	EE_SHCLK	AC_RST#
E	AD30	AD26	GNT1#	REQ4#	VSS	V5REF1	NC	EE_DOUT	EE_CS	VccSus3_3	Vcc1_8
F	FRAME#	AD22	AD24	REQ1#	AD16	Vcc3_3	VccLAN1_8	VccLAN1_8	VccLAN3_3	VccLAN3_3	
G	AD20	AD9	VSS	AD18	PAR	Vcc3_3					
H	TRDY#	STOP#	AD6	AD11	AD4	Vcc3_3					
J	AD15	AD0	AD13	AD2	VSS	Vcc3_3					
K	AD1	C/BE0#	AD3	AD5	C/BE1#	Vcc1_8				VccLAN1_8	VSS
L	AD7	AD8	VSS	AD10	SERR#					VSS	VSS
M	PLOCK#	PERR#	DEVSEL#	AD12	AD14					Vcc3_3	VSS
N	C/BE2#	AD17	IRDY#	AD27	VSS					VSS	VSS
P	AD21	AD19	AD23	AD29	AD31	Vcc1_8				VccSus1_8	VSS
R	AD25	C/BE3#	VSS	REQ3#	VSS	Vcc3_3					
T	NC	LDRQ0#	LAD2 / FWH2	VSS	PCICLK	Vcc3_3					
U	LFRAME#	LAD3 / FWH3	LAD1 / FWH1	LDRQ1#	THRM#	Vcc3_3					
V	LAD0 / FHW0	GPIO7	VSS	GPIO6	GPIO21	VccSus1_8	VccSus1_8	VccSus3_3	VccSus3_3	Vcc1_8	
W	PME#	GPIO8	GPIO25	GPIO27	V5REF_Sus2	VSS	VSS	V5REF2	PDD10	VSS	PDD4
Y	PCIRST#	GPIO13	GPIO28	GPIO12	LAN_RST#	INTRUDER#	RTCRST#	VSS	PDD5	PDD9	PDD11
AA	RI#	SLP_S5#	VSS	SUSCLK	SLP_S3#	PWROK	RSMRST#	VSS	PDD7	PDD2	PDD14
AB	PWRBTN#	SMLINK1	TP[0]	SUSSTAT#	SMBDATA	VCCRTC	VBIAS	VSS	PDD6	PDD12	PDD1
AC	VSS	GPIO24	SMLINK0	SMBCLK	SMBALERT# / GPIO11	RTCX2	RTCX1	VSS	PDD8	PDD3	PDD13
	1	2	3	4	5	6	7	8	9	10	11

Figure 15-2. Intel® ICH3 Ballout (Topview—Right Side)

12	13	14	15	16	17	18	19	20	21	22	23	
OC4#	VSS	USBP5N	USBP5P	VSS	VSS	USBP1N	USBP1P	VSS	VSS	VSS	VSS	A
OC3#	VSS	VSS	VSS	USBP3N	USBP3P	VSS	VSS	VSS	USBRBIAS	VSS	VccSus1_8	B
OC2#	V5REF_Sus1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VccSus1_8	C
OC1#	VSS	USBP4N	USBP4P	VSS	VSS	USBP0N	USBP0P	VSS	VSS	VSS	GPIO42	D
OC0#	VccSus1_8	VSS	VSS	USBP2N	USBP2P	VSS	VSS	VSS	GPIO37	GPIO36	GPIO43	E
		VccSus1_8	VccSus1_8	VccSus1_8	VccSus3_3	VccSus3_3	VSS	CLK48	GPIO34	VSS	GPIO40	F
						Vcc3_3	GPIO35	VSS	GPIO41	GPIO33	GPIO39	G
						Vcc3_3	VSS	GPIO32	GPIO38	SERIRQ	SPKR	H
						Vcc1_8	APICCLK	APICD0	APICD1	FERR#	CLK14	J
VccSus1_8	VSS	VccSus3_3				Vcc1_8	HICOMP	VSS	VSS	VSS	VSS	K
VSS	VSS	VSS					HITERM	HIREF	VSS	HI0	VSS	L
VSS	VSS	Vcc1_8					HI8	VSS	HI1	VSS	HI2	M
VSS	VSS	VSS					HI10	HI3	VSS	HI_STBS	VSS	N
Vcc3_3	VSS	V_CPU_IO				Vcc1_8	HI9	VSS	HI4	VSS	HI_STBF	P
						Vcc1_8	HI11	HI6	VSS	HI5	VSS	R
						Vcc1_8	CLK66	VSS	NC	VSS	HI7	T
						V_CPU_IO	Vcc1_8	GPIO23	GPIO18	RCIN#	STPCLK#	U
		Vcc1_8	Vcc3_3	Vcc3_3	Vcc3_3	Vcc3_3	VRMPWRGD	VSS	GPIO20	V_CPU_IO	A20M#	V
PDD0	SDD8	VSS	SDD7	SDD4	SDD1	VSS	IRQ15	GPIO19	CPUSLP#	VSS	CPUPWRGD	W
PDIOW#	PDDACK#	SDD5	SDD10	SDD9	SDD0	SDD14	SDDACK#	GPIO22	NMI	A20GATE	SMI#	Y
VSS	SDD6	PDA0	PDA2	VSS	SDD13	SDIOW#	SDA1	VSS	IGNNE#	VSS	INTR	AA
PDDREQ	PIORDY	IRQ14	PDCS3#	SDD3	SDD12	SDDREQ	SIORDY	SDA2	NC	NC	INIT#	AB
PDD15	PDIOR#	PDA1	PDCS1#	SDD11	SDD2	SDD15	SDIOR#	SDA0	SDCS1#	SDCS3#	VSS	AC
12	13	14	15	16	17	18	19	20	21	22	23	

Table 15-1. Intel® ICH3-S Ball List by Signal Name

Signal Name	Ball Number
A20GATE	Y22
A20M#	V23
AC_BIT_CLK	B7
AC_RST#	D11
AC_SDIN0	B11
AC_SDIN1	C11
AC_SDOUT	C7
AC_SYNC	A7
AD0	J2
AD1	K1
AD2	J4
AD3	K3
AD4	H5
AD5	K4
AD6	H3
AD7	L1
AD8	L2
AD9	G2
AD10	L4
AD11	H4
AD12	M4
AD13	J3
AD14	M5
AD15	J1
AD16	F5
AD17	N2
AD18	G4
AD19	P2
AD20	G1
AD21	P1
AD22	F2
AD23	P3
AD24	F3
AD25	R1
AD26	E2
AD27	N4
AD28	D1

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
AD29	P4
AD30	E1
AD31	P5
GPIO6	V4
APICCLK	J19
APICD0	J20
APICD1	J21
TP[0]	AB3
C/BE0#	K2
C/BE1#	K5
C/BE2#	N1
C/BE3#	R2
GPIO21	V5
CLK14	J23
CLK48	F20
CLK66	T19
GPIO24	AC2
CPUSLP#	W21
GPIO22	Y20
CPUPWRGD	W23
DEVSEL#	M3
EE_CS	E9
EE_DIN	D8
EE_DOUT	E8
EE_SHCLK	D10
FERR#	J22
FRAME#	F1
GNT0#	A4
GNT1#	E3
GNT2#	D2
GNT3#	D5
GNT4#	B4
GNTA# / GPIO16	B6
GNTB# / GNT5# / GPIO17	B3
GPIO7	V2
GPIO8	W2
GPIO12	Y4
GPIO13	Y2

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
GPIO25	W3
GPIO27	W4
GPIO28	Y3
GPIO32	H20
GPIO33	G22
GPIO34	F21
GPIO35	G19
GPIO36	E22
GPIO37	E21
GPIO38	H21
GPIO39	G23
GPIO40	F23
GPIO41	G21
GPIO42	D23
GPIO43	E23
HI_STBS	N22
HI_STBF	P23
HI0	L22
HI1	M21
HI2	M23
HI3	N20
HI4	P21
HI5	R22
HI6	R20
HI7	T23
HI8	M19
HI9	P19
HI10	N19
HI11	R19
HICOMP	K19
HIREF	L20
HITERM	L19
IGNNE#	AA21
INIT#	AB23
INTR	AA23
INTRUDER#	Y6
IRDY#	N3
IRQ14	AB14

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
IRQ15	W19
LAD0 / FHW0	V1
LAD1 / FWH1	U3
LAD2 / FWH2	T3
LAD3 / FWH3	U2
LAN_CLK	C9
LAN_RST#	Y5
LAN_RSTSYNC	D7
LAN_RXD0	C8
LAN_RXD1	A8
LAN_RXD2	A9
LAN_TXD0	B9
LAN_TXD1	C10
LAN_TXD2	A10
LDRQ0#	T2
LDRQ1#	U4
LFRAME#	U1
NC	AB21
NC	AB22
NC	C2
NC	D6
NC	E7
NC	T1
NC	T21
NMI	Y21
OC0#	E12
OC1#	D12
OC2#	C12
OC3#	B12
OC4#	A12
OC5#	A11
PAR	G5
PCICLK	T5
PCIRST#	Y1
PDA0	AA14
PDA1	AC14
PDA2	AA15
PDCS1#	AC15

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
PDCS3#	AB15
PDD0	W12
PDD1	AB11
PDD2	AA10
PDD3	AC10
PDD4	W11
PDD5	Y9
PDD6	AB9
PDD7	AA9
PDD8	AC9
PDD9	Y10
PDD10	W9
PDD11	Y11
PDD12	AB10
PDD13	AC11
PDD14	AA11
PDD15	AC12
PDDACK#	Y13
PDDREQ	AB12
PDIOR#	AC13
PDIOW#	Y12
PERR#	M2
PIORDY	AB13
PIRQA#	B1
PIRQB#	C1
PIRQC#	B2
PIRQD#	A2
PIRQE# / GPIO2	A6
PIRQF# / GPIO3	B5
PIRQG# / GPIO4	C5
PIRQH# / GPIO5	A5
PLOCK#	M1
PME#	W1
PWRBTN#	AB1
PWROK	AA6
RCIN#	U22
REQ0#	D3
REQ1#	F4

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
REQ2#	A3
REQ3#	R4
REQ4#	E4
REQA# / GPIO0	C4
REQB# / REQ5# / GPIO1	D4
RI#	AA1
RSMRST#	AA7
RTCRST#	Y7
RTCX1	AC7
RTCX2	AC6
SDA0	AC20
SDA1	AA19
SDA2	AB20
SDCS1#	AC21
SDCS3#	AC22
SDD0	Y17
SDD1	W17
SDD2	AC17
SDD3	AB16
SDD4	W16
SDD5	Y14
SDD6	AA13
SDD7	W15
SDD8	W13
SDD9	Y16
SDD10	Y15
SDD11	AC16
SDD12	AB17
SDD13	AA17
SDD14	Y18
SDD15	AC18
SDDACK#	Y19
SDDREQ	AB18
SDIOR#	AC19
SDIOW#	AA18
SERIRQ	H22
SERR#	L5
SIORDY	AB19

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
GPIO19	W20
SLP_S3#	AA5
SLP_S5#	AA2
SMBALERT# / GPIO11	AC5
SMBCLK	AC4
SMBDATA	AB5
SMI#	Y23
SMLINK0	AC3
SMLINK1	AB2
SPKR	H23
GPIO23	U20
STOP#	H2
GPIO20	V21
GPIO18	U21
STPCLK#	U23
SUS_STAT#	AB4
SUSCLK	AA4
THRM#	U5
TRDY#	H1
USBP0N	D18
USBP0P	D19
USBP1N	A18
USBP1P	A19
USBP2N	E16
USBP2P	E17
USBP3N	B16
USBP3P	B17
USBP4N	D14
USBP4P	D15
USBP5N	A14
USBP5P	A15
USBRBIAS	B21
V_CPU_IO	P14
V_CPU_IO	U18
V_CPU_IO	V22
V5REF_Sus1	C13
V5REF_Sus2	W5
V5REF1	E6

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
V5REF2	W8
VBIAS	AB7
Vcc1_8	E11
Vcc1_8	J18
Vcc1_8	K18
Vcc1_8	K6
Vcc1_8	M14
Vcc1_8	P18
Vcc1_8	P6
Vcc1_8	R18
Vcc1_8	T18
Vcc1_8	U19
Vcc1_8	V10
Vcc1_8	V14
Vcc3_3	F6
Vcc3_3	G18
Vcc3_3	G6
Vcc3_3	H18
Vcc3_3	H6
Vcc3_3	J6
Vcc3_3	M10
Vcc3_3	P12
Vcc3_3	R6
Vcc3_3	T6
Vcc3_3	U6
Vcc3_3	V15
Vcc3_3	V16
Vcc3_3	V17
Vcc3_3	V18
VccLAN1_8	F7
VccLAN1_8	F8
VccLAN1_8	K10
VccLAN3_3	F10
VccLAN3_3	F9
VCCRTC	AB6
VccSus1_8	B23
VccSus1_8	C23
VccSus1_8	E13

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
VccSus1_8	F14
VccSus1_8	F15
VccSus1_8	F16
VccSus1_8	K12
VccSus1_8	P10
VccSus1_8	V6
VccSus1_8	V7
VccSus3_3	E10
VccSus3_3	F17
VccSus3_3	F18
VccSus3_3	K14
VccSus3_3	V8
VccSus3_3	V9
VRMPWRGD	V19
VSS	D9
VSS	A1
VSS	A13
VSS	A16
VSS	A17
VSS	A20
VSS	A21
VSS	A22
VSS	A23
VSS	AA12
VSS	AA16
VSS	AA20
VSS	AA22
VSS	AA3
VSS	AA8
VSS	AB8
VSS	AC1
VSS	AC23
VSS	AC8
VSS	B10
VSS	B13
VSS	B14
VSS	B15
VSS	B18

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
VSS	B19
VSS	B20
VSS	B22
VSS	B8
VSS	C14
VSS	C15
VSS	C16
VSS	C17
VSS	C18
VSS	C19
VSS	C20
VSS	C21
VSS	C22
VSS	C3
VSS	C6
VSS	D13
VSS	D16
VSS	D17
VSS	D20
VSS	D21
VSS	D22
VSS	E14
VSS	E15
VSS	E18
VSS	E19
VSS	E20
VSS	E5
VSS	F19
VSS	F22
VSS	G20
VSS	G3
VSS	H19
VSS	J5
VSS	K11
VSS	K13
VSS	K20
VSS	K21
VSS	K22

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
VSS	K23
VSS	L10
VSS	L11
VSS	L12
VSS	L13
VSS	L14
VSS	L21
VSS	L23
VSS	L3
VSS	M11
VSS	M12
VSS	M13
VSS	M20
VSS	M22
VSS	N10
VSS	N11
VSS	N12
VSS	N13
VSS	N14
VSS	N21
VSS	N23

Table 15-1. Intel® ICH3-S Ball List by Signal Name (Continued)

Signal Name	Ball Number
VSS	N5
VSS	P11
VSS	P13
VSS	P20
VSS	P22
VSS	R21
VSS	R23
VSS	R3
VSS	R5
VSS	T20
VSS	T22
VSS	T4
VSS	V20
VSS	V3
VSS	W10
VSS	W14
VSS	W18
VSS	W22
VSS	W6
VSS	W7
VSS	Y8

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Electrical Characteristics 16

This chapter provides the DC and AC electrical charateristics of the ICH3-S.

16.1 Absolute Maximum Ratings

Case Temperature under Bias	= 0 °C to +108 °C
Storage Temperature	= -55 °C to +150 °C
Voltage on Any 3.3 V Pin with Respect to Ground	= -0.5 to Vcc + 0.3 V
Voltage on Any 5 V Tolerant Pin with Respect to Ground (VREF=5V)	= -0.5 to VREF + 0.3 V
1.8 V Supply Voltage with Respect to Vss	= -0.5 to +2.7 V
3.3 V Supply Voltage with Respect to Vss	= -0.5 to +4.6 V
5.0 V Supply Voltage (Vref) with Respect to Vss	= -0.5 to +5.5 V

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. See Section 16.2 for the Functional Operating Range of the ICH3.

Note: A non-condensing environment is required to maintain RTC accuracy.

16.2 Functional Operating Range

All of the AC and DC Characteristics specified in this document assume that the ICH3 component is operating within the Functional Operating Range given in this section. Operation outside of the Functional Operating Range is not recommended, and extended exposure outside of the Functional Operating Range may affect component reliability.

- Case Temperature under Bias = 0 °C to +108 °C
- 1.8 V Supply Voltage (VCC1_8, VccSus1_8) with respect to Vss = 1.71 V to 1.89 V
- 3.3 V Supply Voltage (VCC3_3, VccSus3_3) with respect to Vss = 3.135 V to 3.465 V
- 5 V Supply Voltage (V5REF, V5REF_Sus) with respect to Vss = 4.75 V to 5.25 V
- V_CPU_IO Voltage with respect to Vss =0.950 V to 2.625 V

16.3 DC Characteristics

Table 16-1. Intel® ICH3-S Power Consumption Estimates

Power Plane		Maximum Power Consumption				
		S0	S1	S3	S4/S5	G3
Vcc1_8		550 mA	152 mA	N/A	N/A	N/A
Vcc3_3		420 mA	1 mA	N/A	N/A	N/A
VccSus1_8	External PHY connected, but PHY power not included	94 mA	63 mA	8.5 mA	8.5 mA	N/A
	External PHY not connected to ICH3-S	64 mA	54 mA	7.5 mA	7.5 mA	N/A
VccSus3_3	External PHY connected, but PHY power not included	26 mA	5 mA	4.05 mA	4.05 mA	N/A
	External PHY not connected to ICH3-S	14.01 mA	1.01 mA	0.06 mA	0.06 mA	N/A
Vcc RTC		N/A	N/A	N/A	N/A	4 uA

NOTES:
1. 3.3V SUS S0 was measured with USB traffic (6 ports populated at full speed).
2. Both VccSUS1_8 and VccSUS3_3 S0 max were measured with LAN 100 Mbs full duplex test.
3. VccSUS estimates represent ICH3-S power only; they do not include PHY.

Table 16-2. DC Characteristics Input Signal Association

Symbol	Associated Signals[2]
V_{IH1}/V_{IL1} (5V Tolerant)	**PCI Signals:** AD[31:0], C/BE[3:0]#, DEVSEL#, FRAME#, IRDY#, TRDY#, STOP#, PAR, PERR#, PLOCK#, SERR#, REQ[4:0]# **PC/PCI Signals:** REQ[A]#/GPIO[0], REQB[#]/REQ[5]#/GPIO[1] **Interrupt Signals:** IRQ[15:14], PIRQ[D:A]#, PIRQ[H:E]#/GPIO[5:2] **Legacy Signals:** RCIN#, A20GATE **GPIO Signals:** GPIO[7:6]
V_{IH2}/V_{IL2}	**Clock Signals:** CLK66, CLK48, CLK14
V_{IH3}/V_{IL3}	**Interrupt Signals:** SERIRQ **LPC/FWH Signals:** LDRQ[1:0]#, LAD[3:0]/FWH[3:0]; LFRAME#/FWH[4] **Power Management Signals:** PME#, PWRBTN#, RI#, LAN_RST#, RTCRST#, THRM#, VRMPWRGD **System Management Signals:** SMBALERT#/GPIO[11] **EEPROM Signals:** EE_DIN **GPIO Signals:** GPIO[25:24, 13:12, 8]
V_{IH4}/V_{IL4}	**Clock Signals:** APICCLK
V_{IH5}/V_{IL5}	**SMBus Signals:** SMBCLK, SMBDATA **System Management Signals:** INTRUDER#, SMLINK[1:0] **Power Management Signals:** RSMRST#, PWROK **GPIO Signals:** GPIO[28:27]
V_{IL6}/V_{IH6}	**LAN Signals:** LAN_RXD[2:0]
V_{IL7}/V_{IH7}	**Processor Signals:** FERR#, APICD[1:0]
V_{IL8}/V_{IH8}	**Hub Interface Signals:** HI[11:0], HI_STBF, HI_STBS
V_{IL9}/V_{IH9}	**Real Time Clock Signals:** RTCX1
VIL10/VIH10 (5 V Tolerant)	**USB Signals:** OC[5:0]#
VIL11/VIH11	**AC'97 Signals:** AC_BITCLK, AC_SDIN[1:0], AC_SYNC **GPIO Signals:** GPIO[43:32]
VIL12/VIH12	**Clock Signals:** LAN_CLK
VIL13/VIH13	**Clock Signals:** PCICLK
VIL14/VIH14	**IDE Signals:** PDD[15:0], SDD[15:0], PDDREQ, PIORDY, SDDREQ, SIORDY
V_{DI} / V_{CM} / V_{SE}	**USB Signals:** USBP[5:0][P,N]

NOTE: To determine the signals's power plane, refer to Table 3-5.

Table 16-3. DC Input Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.5	0.8	V	
V_{IH1}	Input High Voltage	2.0	V5REF + 0.5	V	
V_{IL2}	Input Low Voltage	-0.5	0.8	V	
V_{IH2}	Input High Voltage	2.0	Vcc3_3 + 0.5	V	
V_{IL3}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH3}	Input High Voltage	0.5Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL4}	Input Low Voltage	-0.5	0.7	V	
V_{IH4}	Input High Voltage	1.7	2.625	V	
V_{IL5}	Input Low Voltage	-0.5	0.6	V	
V_{IH5}	Input High Voltage	2.1	VccSus3_3 + 0.5	V	
V_{IL6}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH6}	Input High Voltage	0.6Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL7}	Input Low Voltage	-0.5	0.6	V	
V_{IH7}	Input High Voltage	1.2	Vcc3_3 + 0.5	V	
V_{IL8}	Input Low Voltage	-0.3	HIREF – 0.10	V	
V_{IH8}	Input High Voltage	HIREF + 0.10	Vcc1_8 + 0.5	V	
V_{IL9}	Input Low Voltage	-0.5	0.10	V	
V_{IH9}	Input High Voltage	0.40	2.0	V	
V_{IL10}	Input Low Voltage	-0.5	0.8	V	
V_{IH10}	Input High Voltage	2.0	V5REF_SUS + 0.5	V	
V_{IL11}	Input Low Voltage	-0.5	0.35Vcc3_3	V	
V_{IH11}	Input High Voltage	0.65Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL12}	Input Low Voltage	-0.5	0.3Vcc3_3	V	
V_{IH12}	Input High Voltage	0.6Vcc3_3	Vcc3_3 + 0.5	V	
V_{IL13}	Input Low Voltage	-0.5	0.8	V	
V_{IH13}	Input High Voltage	2.0	Vcc3_3 + 0.5	V	
V_{IL14}	Input Low Voltage		0.8	V	Note 3
V_{IH14}	Input High Voltage	2.0	V5REF + 0.5	V	
V_{DI}	Differential Input Sensitivity	0.2		V	Note 1
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Note 2
V_{SE}	Single-Ended Receiver Threshold	0.8	2.0	V	

NOTES:
1. V_{DI} = | USBPx[P]–USBPx[N] |
2. Includes V_{DI} range.
3. These voltages represent steady state values. For transient values, consult V_{RING} in Table 16-6.

Table 16-4. DC Characteristic Output Signal Association

Symbol	Associated Signals
V_{OH1}/V_{OL1}	**IDE Signals:** PDD[15:0], SDD[15:0], PDIOW#/PDSTOP, SDIOW#/SDSTOP, PDIOR#/ PDWSTB/PRDMARDY, SDIOR#/STWSTB/SRDMARDY, PDDACK#, SDDACK#, PDA[2:0], SDA[2:0], PDCS[3,1]#, SDCS[3,1]#
V_{OH2}/V_{OL2}	**Processor Signals:** A20M#, CPUPWRGD (1), CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#
V_{OH3}/V_{OL3}	**PCI Signals:** AD[31:0], C/BE[3:0]#, PCIRST#, GNT[4:0]#, PAR, DEVSEL#, PERR#, PLOCK#, STOP#, TRDY#, IRDY#, FRAME#, SERR# (1) **Interrupt Signals:** SERIRQ, PIRQ[D:A]# (1), PIRQ[H:E]#/GPIO[5:2](1)
V_{OH4}/V_{OL4}	**PCI Signals:** GNT5#/GNTB#/GPIO17, GNTA#/GPIO16 **LPC/FWH Signals:** LAD[3:0]/FWH[3:0], LFRAME#/FWH[4] **AC '97 Signals:** AC_RST#, AC_SDOUT, AC_SYNC **LAN Signals:** LAN_RSTSYNC, LAN_TXD[2:0] **GPIO Signals:** GPIO[21], GPIO[43:32]
V_{OL5}/V_{OH5}	**SMBus Signals:** SMBCLK (1), SMBDATA (1) **System Management Signals:** SMLINK[1:0] (1) **Interrupt Signals:** APICD[1:0] (1)
V_{OL6}/V_{OH6}	**Power Management Signals:** SLP_S3#, SLP_S5#, SUS_STAT#, SUSCLK **EEPROM Signals:** EE_CS, EE_DOUT, EE_SHCLK **GPIO Signals:** GPIO[28:27, 25:22, 20:18] **Other Signals:** SPKR
V_{OL7}/V_{OH7}	**USB Signals:** USBP[5:0][P,N]
V_{OL8}/V_{OH8}	**Hub Signals:** HI[11:0], HI_STBF, HI_STBS

NOTE 1: These signal are open drain.

Table 16-5. DC Output Characteristics

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL1}	Output Low Voltage		0.5	V	4 mA	Note 1
V_{OH1}	Output High Voltage	2.4		V	-0.4 mA	Note 1
V_{OL2}	Output Low Voltage		0.4	V	4.0 mA	
V_{OH2}	Output High Voltage	V_CPU_IO – 26 mV		V	-0.1 mA	Note 2
V_{OL3}	Output Low Voltage		0.55	V	6 mA	
V_{OH3}	Output High Voltage	2.4		V	-2 mA	Note 2
V_{OL4}	Output Low Voltage		0.1Vcc3_3	V	1.5 mA	
V_{OH4}	Output High Voltage	0.9Vcc3_3		V	-0.5 mA	Note 2
V_{OL5}	Output Low Voltage		0.4	V	4 mA	
V_{OH5}	Output High Voltage	N/A		V		Note 2
V_{OL6}	Output Low Voltage		0.4	V	4.0 mA	
V_{OH6}	Output High Voltage	Vcc3_3 - 0.5		V	-2.0 mA	Note 2
V_{OL7}	Output Low Voltage		0.4	V	5 mA	
V_{OH7}	Output High Voltage	Vcc3_3 - 0.5		V	-2 mA	
V_{OL8}	Output Low Voltage		0.05	V	20 mA	
V_{OH8}	Output High Voltage	1.6		V	-1.5 mA	

NOTES:
1. IDE signal DC voltage levels shall be measured at the host connector.
2. The CPUPWRGD, SERR#, PIRQ[A:H], GPIO[22]/CPUPERF#, APIC[1:0], SMBDATA, SMBCLK and SMLINK[1:0] signal has an open drain driver, and the V_{OH} spec does not apply. This signal must have external pull-up resistor.

Table 16-6. Other DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V5REF	ICH3 Core Well Reference Voltage	4.75	5.25	V	
VCC3_3	I/O Buffer Voltage	3.135	3.465	V	
VCC1_8	Internal Logic Voltage	1.71	1.89	V	
HIREF	Hub Interface Reference Voltage	0.343	0.357	V	
V5REF_Sus	Suspend Well Reference Voltage	4.75	5.25	V	
VccSus3_3	Suspend Well I/O Buffer Voltage	3.135	3.465	V	
VccSus1_8	Suspend Well Logic Voltage	1.71	1.89	V	
Vcc(RTC)	Battery Voltage	2.0	3.6	V	
V+	Low to High Input Threshold	1.5	2.0	V	Applies to Ultra DMA modes greater than mode 4.
V-	High to Low Input Threshold	1.0	1.5	V	Applies to Ultra DMA modes greater than mode 4
V_{HYS}	Difference between Input Thresholds: $(V+_{current\ value}) - (V-_{current\ value})$	320		mV	Applies to Ultra DMA modes greater than mode 4
V_{THRAVG}	Average of thresholds: $((V+_{current\ value}) + (V-_{current\ value}))/2$	1.3	1.7	V	Applies to Ultra DMA modes greater than mode 4
V_{RING}	Voltage at Recipient Connector	-1.0	6.0	V	
V_{IT+}	Hysteresis Input Rising Threshold	1.9		V	Applied to USBP[5:0][P,N]
V_{IT-}	Hysteresis Input Falling Threshold		1.3	V	Applied to USBP[5:0]P,N]
V_{DI}	Differential Input Sensitivity	0.2		V	|(USBPx+,USBPx-)|
V_{CM}	Differential Common Mode Range	0.8	2.5	V	Includes V_{DI}
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V	
V_{SE}	Single Ended Rcvr Threshold	0.8	2.0	V	
I_{LI1}	Input Leakage Current	-1.0	+1.0	uA	
I_{LI2}	Hi-Z State Data Line Leakage	-10	+10	uA	(0 V< V_{IN}< 3.3V)
I_{LI3}	Input Leakage Current–Clock signals	-100	+100	uA	See Note
C_{IN}	Input Capacitance–Hub interface Input Capacitance–All Other		8 12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz
Crystal Load Capacitance		**Typical Value**			
C_L	XTAL1	6		pF	
C_L	XTAL2	6		pF	

NOTE: Includes APICCLK, CLK14, CLK48, CLK66, LAN_CLK, and PCICLK.

16.4 AC Characteristics

Table 16-7. Clock Timings

Sym	Parameter	Min	Max	Unit	Notes	Figure
	PCI Clock (PCICLK)					
t1	Period	30	33.3	ns		16-1
t2	High Time	12		ns		16-1
t3	Low Time	12		ns		16-1
t4	Rise Time		3	ns		16-1
t5	Fall Time		3	ns		16-1
	Oscillator Clock (OSC)					
t6	Period	67	70	ns		16-1
t7	High Time	20				16-1
t8	Low Time	20		ns		16-1
	USB Clock (USBCLK)					
f_{clk48}	Operating Frequency	48		MHz	1	
t9	Frequency Tolerance		500	ppm	2	
t10	High Time	8		ns		16-1
t11	Low Time	8		ns		16-1
t12	Rise Time		1.2	ns		16-1
t13	Fall Time		1.2	ns		16-1
	SMBus Clock (SMBCLK)					
f_{smb}	Operating Frequency	10	16	kHz		
t18	High Time	4.0	50	µs	3	16-16
t19	Low Time	4.7		µs		16-16
t20	Rise Time		1000	ns		16-16
t21	Fall Time		300	ns		16-16
	I/O APIC Clock (APICCLK)					
f_{ioap}	Operating Frequency	14.32	33.33	MHz		
t22	High Time	12	36	ns		16-1
t23	Low Time	12	36	ns		16-1
t24	Rise Time	1.0	5.0	ns		16-1
t25	Fall Time	1.0	5.0	ns		16-1
	AC '97 Clock (BITCLK)					
f_{ac97}	Operating Frequency	12.288		MHz		
t26	Output Jitter		750	ps		
t27	High Time	32.56	48.84	ns		16-1
t28	Low Time	32.56	48.84	ns		16-1

Table 16-7. Clock Timings (Continued)

Sym	Parameter	Min	Max	Unit	Notes	Figure
t29	Rise Time	2.0	6.0	ns	4	16-1
t30	Fall Time	2.0	6.0	ns	4	16-1
	Hub Interface Clock					
f_{hi}	Operating Frequency	66		MHz		
t31	High Time	6.0		ns		16-1
t32	Low Time	6.0		ns		16-1
t33	Rise Time	0.25	1.2	ns		16-1
t34	Fall Time	0.25	1.2	ns		16-1
t35	CLK66 leads PCICLK	1.0	4.5	ns	5	

NOTES:
1. The USBCLK is a 48 MHz that expects a 40/60% duty cycle.
2. USBCLK is a pass-thru clock that is not altered by the ICH3. This frequency tolerance specification is required for USB 1.1 compliance and is affected by external elements such as the clock generator and the system board.
3. The maximum high time (t18 Max) provide a simple guaranteed method for devices to detect bus idle conditions.
4. BITCLK rise and fall times are measured from 10%VDD and 90%VDD.
5. This specification includes pin-to-pin skew from the clock generator as well as board skew.
6. SUSCLK duty cycle can range from 30% minimum to 70% maximum.

Table 16-8. PCI Interface Timing

Sym	Parameter	Min	Max	Units	Notes	Figure
t40	AD[31:0] Valid Delay	2	11	ns	Min: 0pF Max: 50pF	16-2
t41	AD[31:0] Setup Time to PCICLK Rising	7		ns		16-3
t42	AD[31:0] Hold Time from PCICLK Rising	0		ns		16-3
t43	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, PERR#, PLOCK#, DEVSEL# Valid Delay from PCICLK Rising	2	11	ns	Min: 0pF Max: 50pF	16-2
t44	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, PERR#, PLOCK#, IDSEL, DEVSEL# Output Enable Delay from PCICLK Rising	2		ns		16-6
t45	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PERR#, PLOCK#, DEVSEL#, GNT[A:B]# Float Delay from PCICLK Rising	2	28	ns		16-4
t46	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR#, DEVSEL#, Setup Time to PCICLK Rising	7		ns		16-3
t47	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR#, DEVSEL#, REQ[A:B]# Hold Time from PCLKIN Rising	0		ns		16-3
t48	PCIRST# Low Pulse Width	1		ms		16-5
t49	GNT[A:B}#, GNT[5:0]# Valid Delay from PCICLK Rising	2	12	ns		
t50	REQ[A:B]#, REQ[5:0]# Setup Timer to PCICLK Rising	12		ns		

Table 16-9. IDE PIO and Multiword DMA ModeTiming

Sym	Parameter	Min	Max	Units	Notes	Figure
t60	PDIOR#/PDIOW#/SDIOR#/SDIOW# Active From CLK66 Rising	2	20	ns		16-7,16-8
t61	PDIOR#/PDIOW#/SDIOR#/SDIOW# Inactive From CLK66 Rising	2	20	ns		16-7,16-8
t62	PDA[2:0]/SDA[2:0] Valid Delay From CLK66 Rising	2	30	ns		16-7
t63	PDCS1#/SDCS1#, PDCS3#/SDCS3# Active From CLK66 Rising	2	30	ns		16-7
t64	PDCS1#/SDCS1#, PDCS3#/SDCS3# Inactive From CLK66 Rising	2	30	ns		16-7
t65	PDDACK#/SDDACK# Active From CLK66 Rising	2	20	ns		16-8
t66	PDDACK#/SDDACK# Inactive From CLK66 Rising	2	20	ns		
t67	PDDREQ/SDDREQ Setup Time to CLK66 Rising	7		ns		16-8
t68	PDDREQ/SDDREQ Hold From CLK66 Rising	7		ns		16-8
t69	PDD[15:0]/SDD[15:0] Valid Delay From CLK66 Rising	2	30	ns		16-7,16-8
t70	PDD[15:0]/SDD[15:0] Setup Time to CLK66 Rising	10		ns		16-7,16-8
t71	PDD[15:0]/SDD[15:0] Hold From CLK66 Rising	7		ns		16-7,16-8
t72	PIORDY/SIORDY Setup Time to CLK66 Rising	7		ns	1	16-7
t73	PIORDY/SIORDY Hold From CLK66 Rising	7		ns	1	16-7
t74	PIORDY/SIORDY Inactive Pulse Width	48		ns		16-7
t75	PDIOR#/PDIOW#/SDIOR#/SDIOW# Pulse Width Low				2,3	16-7,16-8
t76	PDIOR#/PDIOW#/SDIOR#/SDIOW# Pulse Width High				3,4	16-7,16-8

NOTES:
1. IORDY is internally synchronized. This timing is to guarantee recognition on the next clock.
2. PIORDY sample point from DIOx# assertion and PDIOx# active pulse width is programmable from 2-5 PCI clocks when the drive mode is Mode 2 or greater. Refer to the ISP field in the IDE Timing Register
3. PIORDY sample point from DIOx# assertion, PDIOx# active pulse width and PDIOx# inactive pulse width cycle time is the compatible timing when the drive mode is Mode 0/1. Refer to the TIM0/1 field in the IDE timing register.
4. PDIOx# inactive pulse width is programmable from 1-4 PCI clocks when the drive mode is Mode 2 or greater. Refer to the RCT field in the IDE Timing Register.

Table 16-10. Ultra ATA Timing (Mode 0, Mode 1, Mode 2)

Sym	Parameter[1]	Mode 0 (ns)		Mode 1 (ns)		Mode 2 (ns)		Measuring Location	Figure
		Min	Max	Min	Max	Min	Max		
t80	Sustained Cycle Time (T2cyctyp)	240		160		120		Sender Connector	
t81	Cycle Time (Tcyc)	112		73		54		End Recipient Connector	16-10
t82	Two Cycle Time (T2cyc)	230		153		115		Sender Connector	16-10
t83a	Data Setup Time (Tds)	15		10		7		Recipient Connector	16-10
t84a	Data Hold Time (Tdh)	5		5		5		Recipient Connector	16-10
t85a	Data Valid Setup Time (Tdvs)	70		48		31		Sender Connector	16-10
t86a	Data Valid Hold Time (Tdvh)	6.2		6.2		6.2		Sender Connector	16-10
t87	Limited Interlock Time (Tli)	0	150	0	150	0	150	See Note 2	16-12
t88	Interlock Time w/ Minimum (Tmli)	20		20		20		Host Connector	16-12
t89	Envelope Time (Tenv)	20	70	20	70	20	70	Host Connector	16-9
t90	Ready to Pause Time (Trp)	160		125		100		Recipient Connector	16-11
t91	DMACK setup/hold Time (Tack)	20		20		20		Host Connector	16-9, 16-12
t92a	CRC Word Setup Time at Host (Tcvs)	70		48		31		Host Connector	
t92b	CRC word valid hold time at sender (from DMACK# negation until CRC may become invalid)[2] (Tcvh)	6.2		6.2		6.2		Host Connector	
t93	STROBE output released-to-driving to the first transition of critical timing (Tzfs)	0		0		0		Device Connector	
t94	Data Output Released-to-Driving Until the First Tunisian of Critical Timing (Tdzfs)	70		48		31		Sender Connector	
t95	Unlimited Interlock Time (Tui)	0		0		0		Host Connector	
t96a	Maximum time allowed for output drivers to release (from asserted or negated) (Taz)		10		10		10	See Note 2	
t96b	Minimum time for drivers to assert or negate (from released) (Tzad)	0		0		0		Device Connector	
t97	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY#) (Trfs)		75		70		60	Sender Connector	

Table 16-10. Ultra ATA Timing (Mode 0, Mode 1, Mode 2) (Continued)

Sym	Parameter[1]	Mode 0 (ns)		Mode 1 (ns)		Mode 2 (ns)		Measuring Location	Figure
		Min	Max	Min	Max	Min	Max		
t98a	Maximum time before releasing IORDY (Tiordyz)		20		20		20	Device Connector	
t98b	Minimum time before driving IORDY[2] (Tziordy)	0		0		0		Device Connector	
t99	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst) (Tss)	50		50		50		Sender Connector	
t83b	Recipient IC data setup time (from data valid until STROBE edge)[2] (Tdsic)	14.7		9.7		6.8		ICH3 ball	
t84b	Recipient IC data hold time (from STROBE edge until data may become invalid)[2] (Tdhic)	4.8		4.8		4.8		ICH3 ball	
t85b	Sender IC data valid setup time (from data valid until STROBE edge)[2] (Tdvsic)	72.9		50.9		33.9		ICH3 ball	
t86b	Sender IC data valid hold time (from STROBE edge until data may become invalid)[2] (Tdvhic)	9		9		9		ICH3 ball	

NOTES:
1. The specification symbols in parentheses correspond to the AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6) specification name.
2. See the AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6) specification for further details on measuring these timing parameters.

Table 16-11. Ultra ATA Timing (Mode 3, Mode 4, Mode 5)

Sym	Parameter[1]	Mode 3 (ns)		Mode 4 (ns)		Mode 5 (ns)		Measuring Location	Figure
		Min	Max	Min	Max	Min	Max		
t80	Sustained Cycle Time (T2cyctyp)	90		60		40		Sender Connector	
t81	Cycle Time (Tcyc)	39		25		16.8		End Recipient Connector	16-10
t82	Two Cycle Time (T2cyc)	86		57		38		Sender Connector	16-10
t83	Data Setup Time (Tds)	7		5		4.0		Recipient Connector	16-10
t84	Data Hold Time (Tdh)	5		5		4.6		Recipient Connector	16-10
t85	Data Valid Setup Time (Tdvs)	20		6.7		4.8		Sender Connector	16-10
t86	Data Valid Hold Time (Tdvh)	6.2		6.2		4.8		Sender Connector	16-10
t87	Limited Interlock Time (Tli)	0	100	0	100	0	75	See Note 2	16-12
t88	Interlock Time w/ Minimum (Tmli)	20		20		20		Host Connector	16-12
t89	Envelope Time (Tenv)	20	55	20	55	20	50	Host Connector	16-9
t90	Ready to Pause Time (Trp)	100		100		85		Recipient Connector	16-11
t91	DMACK setup/hold Time (Tack)	20		20		20		Host Connector	16-9, 16-12
t92a	CRC Word Setup Time at Host (Tcvs)	20		6.7		10		Host Connector	
t92b	CRC Word Hold Time at Sender CRC word valid hold time at sender (from DMACK# negation until CRC may become invalid)[2] (Tcvh)	6.2		6.2		10.0		Host Connector	
t93	STROBE output released-to-driving to the first transition of critical timing (Tzfs)	0		0		35		Device Connector	
t94	Data Output Released-to-Driving Until the First Transition of Critical Timing (Tdzfs)	20.0		6.7		25		Sender Connector	
t95	Unlimited Interlock Time (Tui)	0		0		0		Host Connector	
t96a	Maximum time allowed for output drivers to release (from asserted or negated) (Taz)		10		10		10	See Note 2	
t96b	Drivers to assert or negate (from released) (Tzad)	0		0		0		Device Connector	
t97	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY#) (Trfs)		60		60		50	Sender Connector	

Table 16-11. Ultra ATA Timing (Mode 3, Mode 4, Mode 5) (Continued)

Sym	Parameter[1]	Mode 3 (ns)		Mode 4 (ns)		Mode 5 (ns)		Measuring Location	Figure
		Min	Max	Min	Max	Min	Max		
t98a	Maximum time before releasing IORDY (Tiordyz)		20		20		20	Device Connector	
t98b	Minimum time before driving IORDY [2] (Tziordy)	0		0		0		Device Connector	
t99	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst) (Tss)	50		50		50		Sender Connector	
t83b	Recipient IC data setup time (from data valid until STROBE edge)[2] (Tdsic)	6.8		4.8		2.3		ICH3 Balls	
t84b	Recipient IC data hold time (from STROBE edge until data may become invalid)[2] (Tdhic)	4.8		4.8		2.8		ICH3 Balls	
t85b	Sender IC data valid setup time (from data valid until STROBE edge)[2] (Tdvsic)	22.6		9.5		6.0		ICH3 Balls	
t86b	Sender IC data valid hold time (from STROBE edge until data may become invalid)[2] (Tdvhic)	9.0		9.0		6.0		ICH3 Balls	

NOTES:
1. The specification symbols in parentheses correspond to the AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6) specification name.
2. See the AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6) specification for further details on measuring these timing parameters.

Table 16-12. Universal Serial Bus Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
Full Speed Source (Note 7)						
t100	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, C_L = 50 pF	16-13
t101	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, C_L = 50 pF	16-13
t102	Source Differential Driver Jitter To Next Transition For Paired Transitions	 -3.5 -4	 3.5 1	 ns ns	2, 3	16-14
t103	Source SE0 interval of EOP	160	175	ns	4	16-15
t104	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns	5	
t105	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 -18.5 -9	 18.5 9	 ns ns	3	16-14
t106	EOP Width: Must accept as EOP	82		ns	4	16-15
t107	Width of SE0 interval during differential transition		14	ns		
Low Speed Source (Note 8)						
t108	USBPx+, USBPx- Driver Rise Time	75	300	ns ns	1, 6 C_L = 50 pF C_L = 350 pF	16-13
t109	USBPx+, USBPx- Driver Fall Time	75	300	ns ns	1,6 C_L = 50 pF C_L = 350 pF	16-13
t110	Source Differential Driver Jitter To Next Transition For Paired Transitions	 -25 -14	 25 14	 ns ns	2, 3	16-14
t111	Source SE0 interval of EOP	1.25	1.50	µs	4	16-15
t112	Source Jitter for Differential Transition to SE0 Transition	-40	100	ns	5	
t113	Receiver Data Jitter Tolerance To Next Transition For Paired Transitions	 -152 -200	 152 200	 ns ns	3	16-14
t114	EOP Width: Must accept as EOP	670		ns	4	16-15
t115	Width of SE0 interval during differential transition		210	ns		

1. Driver output resistance under steady state drive is specified at 28 ohms at minimum and 43 ohms at maximum
2. Timing difference between the differential data signals
3. Measured at crossover point of differential data signals
4. Measured at 50% swing point of data signals
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP
6. Measured from 10% to 90% of the data signal
7. Full Speed Data Rate has minimum of 11.97 Mbps and maximum of 12.03 Mbps
8. Low Speed Data Rate has a minimum of 1.48 Mbps and a maximum of 1.52 Mbps

Table 16-13. IOAPIC Bus Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t120	APICCD[1:0]# Valid Delay from APICCLK Rising	3.0	12.0	ns		16-2
t121	APICCD[1:0]# Setup Time to APICCLK Rising	8.5		ns		16-3
t122	APICCD[1:0]# Hold Time from APICCLK Rising	3.0		ns		16-3

NOTE: The Min AC column indicates the minimum times required by the SMBus and/or I^2C specifications. The ICH3 tolerates these timings on both its SMBus and SMLink interfaces.

Table 16-14. SMBus Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t130	Bus Tree Time Between Stop and Start Condition	4.7		µs		16-16
t131	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0		µs		16-16
t132	Repeated Start Condition Setup Time	4.7		µs		16-16
t133	Stop Condition Setup Time	4.0		µs		16-16
t134	Data Hold Time	0		ns	4	16-16
t135	Data Setup Time	250		ns		16-16
t136	Device Time Out	25	35	ms	1	
t137	Cumulative Clock Low Extend Time (slave device)		25	ms	2	16-17
t138	Cumulative Clock Low Extend Time (master device)		10	ms	3	16-17

NOTES:
1. A device will timeout when any clock low exceeds this value.
2. t137 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
3. t138 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack or ack-to-stop.
4. t134 has a minimum timing for I^2C of 0 ns, while the minimum timing for SMBus is 300 ns.

Table 16-15. AC '97 Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t140	ACSDIN[0:1] Setup to Falling Edge of BITCLK	15		ns		
t141	ACSDIN[0:1] Hold from Falling Edge of BITCLK	5		ns		
t142	ACSYNC, ACSDOUTvalid delay from rising edge of BITCLK		15	ns		16-2

Table 16-16. LPC Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t150	LAD[3:0] Valid Delay from PCICLK Rising	2	11	ns		16-2
t151	LAD[3:0] Output Enable Delay from PCICLK Rising	2		ns		16-6
t152	LAD[3:0] Float Delay from PCICLK Rising		28	ns		16-4
t153	LAD[3:0] Setup Time to PCICLK Rising	7		ns		16-3
t154	LAD[3:0] Hold Time from PCICLK Rising	0		ns		16-3
t155	LDRQ[1:0]# Setup Time to PCICLK Rising	12		ns		16-3
t156	LDRQ[1:0]# Hold Time from PCICLK Rising	0		ns		16-3
t157	LFRAME# Valid Delay from PCICLK Rising	2	12	ns		16-2

Table 16-17. Miscellaneous Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t160	SERIRQ Setup Time to PCICLK Rising	7		ns		16-3
t161	SERIRQ Hold Time from PCICLK Rising	0		ns		16-3
t162	RI#, EXTSMI#, GPI, USB Resume Pulse Width	2		RTCCLK		16-5
t163	SPKR Valid Delay from OSC Rising		200	ns		16-2
t164	SERR# Active to NMI Active		200	ns		
t165	IGNNE# Inactive from FERR# Inactive		230	ns		

Table 16-18. Power Sequencing and Reset Signal Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t170	VccRTC active to RTCRST# inactive	5	-	ms		16-18
t171	V5RefSus active to VccSus3_3, VccSus1_8 active	0	-	ms	1, 2	16-18
t172	VccRTC supply active to VccSus supplies active	0	-	ms	3	16-18
t173	VccSus supplies active to LAN_RST# active, RSMRST# inactive	10	-	ms		16-18 16-21
t174	V5Ref active to Vcc3_3, Vcc1_8 active	0	-	ms	1, 2	16-18
t175	VccSus supplies active to Vcc supplies active	0	-	ms	3	16-18
t176	Vcc supplies active to PWROK, VRMPWRGD active	10	-	ms		16-18 16-21
t177	PWROK and VRMPWRGD both active to SUS_STAT# inactive.	32	34	RTCCLK		16-21
t178	SUS_STAT# inactive to PCIRST# inactive	1	3	RTCCLK		16-21
t179	AC_RST# active low pulse width	1		µs		
t180	AC_RST# inactive to BIT_CLK startup delay	162.8		ns		

NOTES:
1. The V5Ref supply must power up before or simultaneous with its associated 3.3 V supply, and must power down simultaneous with or after the 3.3 V supply. See Section 2.20.3 for details.
2. The associated 3.3 V and 1.8 V supplies are assumed to power up or down ‘together. The difference between the levels of the 3.3 V and 1.8 V supplies must never be greater than 2.0 V.
3. The VccSus supplies must **never** be active while the VccRTC supply is inactive. Likewise, the Vcc or VccLAN, in mobile configurations, supplies must **never** be active while the VccSus supplies are inactive, and the Vcc supplies must **never** be active while the VccLAN supplies are inactive in mobile configurations.

Table 16-19. Power Management Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t181	VccSus active to SLP_S3#, SLP_S5#, SUS_STAT# and PCIRST# active		50	ns		16-20
t182 t183	RSMRST# inactive to SUSCLK running, SLP_S3#, SLP_S5# inactive		110	ms	7	16-20
t184	Vcc active to STPCLK# and CPUSLP# inactive, and CPU Frequency Strap signals high		50	ns		16-20 16-21
t185	PWROK and VRMPWRGD active to SUS_STAT# inactive and processor Frequency Straps latched to Strap Values	32	34	RTCCLK	1	16-20
t186	CPU Reset Complete to Frequency Strap signals unlatched from Strap Values	7	9	CLK66	2	16-20
t187	STPCLK# active to Stop Grant cycle	N/A	N/A		3	16-21
t188	Stop Grant cycle to CPUSLP# active	60	63	PCICLK	4	16-21
t192	CPUSLP# active to SUS_STAT# active	2	4	RTCCLK	1	16-21
t193	SUS_STAT# active to PCIRST# active	9	21	RTCCLK	1	16-21
t194	PCIRST# active to SLP_S3# active	1	2	RTCCLK	1	16-21
t195	SLP_S3# active to SLP_S5# active	1	2	RTCCLK	1, 6	16-21
t196	SLP_S3# active to PWROK, VRMPWRGD inactive	0		ms	5	16-21
t197	PWROK, VRMPWRGD inactive to Vcc supplies inactive	20		ns		16-21
t198	Wake Event to SLP_S3#, SLP_S5# inactive	1	10	RTCCLK	1	16-21
t204	Processor I/F signals latched prior to STPCLK# active	0	4	CLK66	2	16-22
t205	Break Event to STPCLK# inactive	30	3120	ns		16-22
t206	STPCLK# inactive to Processor I/F signals unlatched	240	1880	ns		16-22

NOTES:
1. These transitions are clocked off the internal RTC. 1 RTC clock is approximately 32 us.
2. This transition is clocked off the 66 MHz CLK66. 1 CLK66 is approximately 15 ns.
3. The ICH3 STPCLK# assertion will trigger the processor to send a stop grant acknowledge cycle. The timing for this cycle getting to the ICH3 is dependant on the processor and the memory controller.
4. These transitions are clocked off the 33 MHz PCICLK. 1 PCICLK is approximately 30ns.
5. The ICH3 has no maximum timing requirement for this transition. It is up to the system designer to determine if the SLP_S3# and SLP_S5# signals are used to control the power planes.
6. If the transition to S5 is due to Power Button Override, SLP_S3# and SLP_S5# are asserted together following timing t194 (PCIRST# active to SLP_S3# and SLP_S5# active).
7. If there is no RTC battery in the system, so VccRTC and the VccSus supplies come up together, the delay from RTCRST# and RSMRST# inactive to SUSCLK toggling may be as much as 1000 ms.

16.5 Timing Diagrams

Figure 16-1. Clock Timing

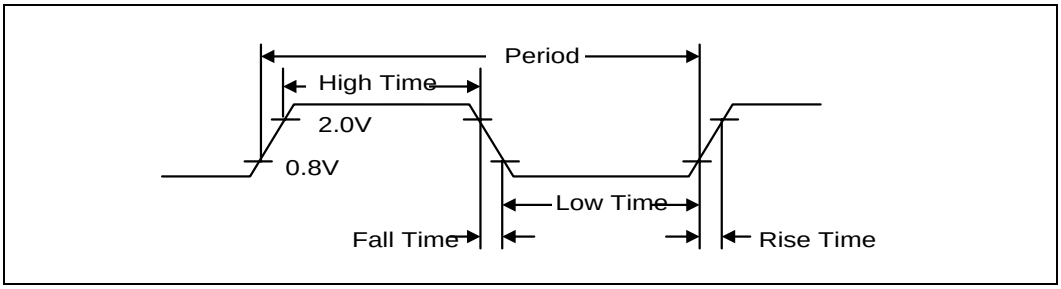


Figure 16-2. Valid Delay From Rising Clock Edge

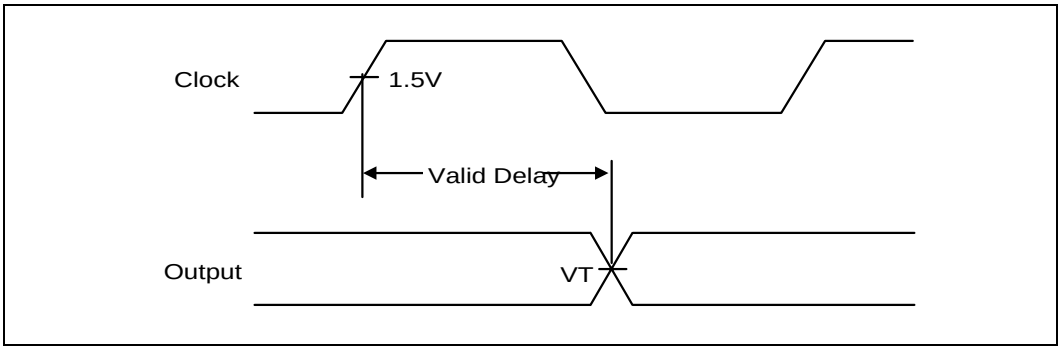


Figure 16-3. Setup and Hold Times

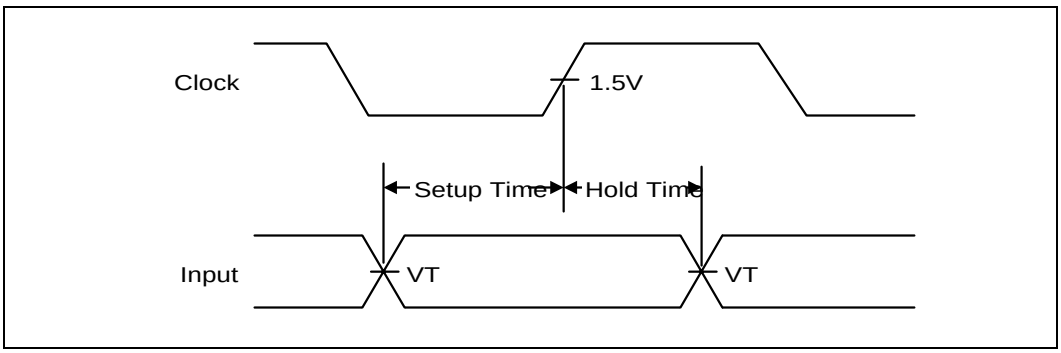


Figure 16-4. Float Delay

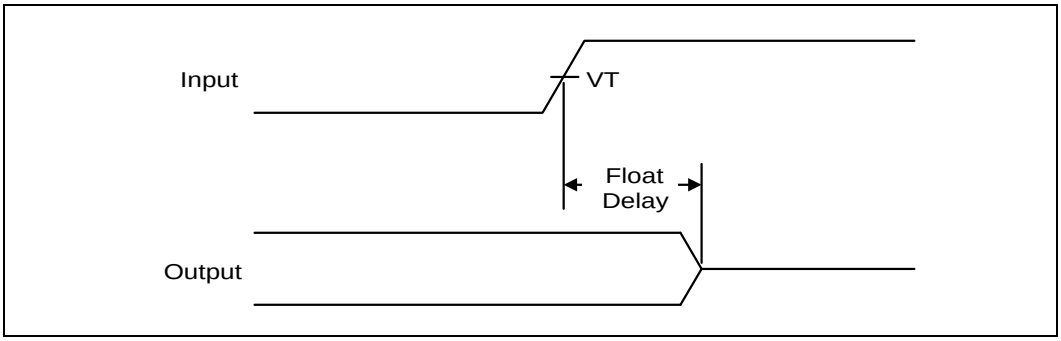


Figure 16-5. Pulse Width

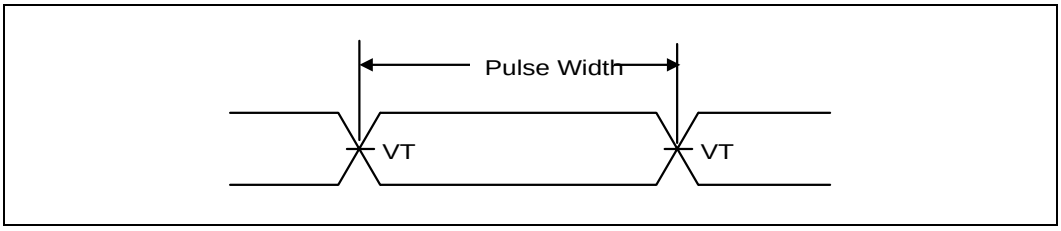


Figure 16-6. Output Enable Delay

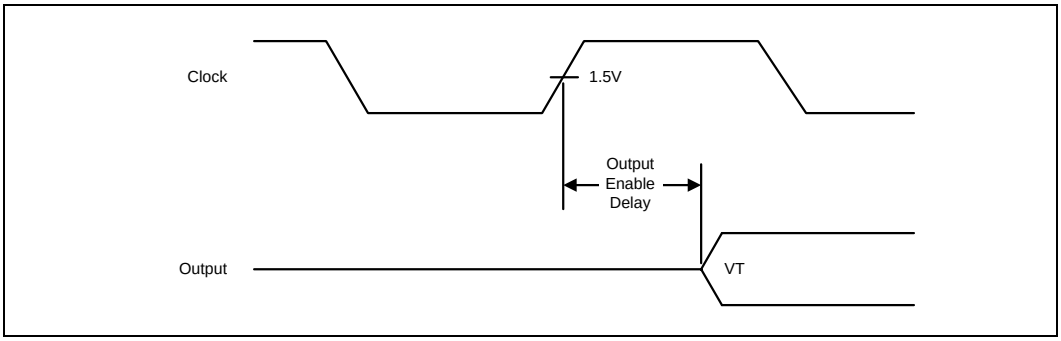


Figure 16-7. IDE PIO Mode

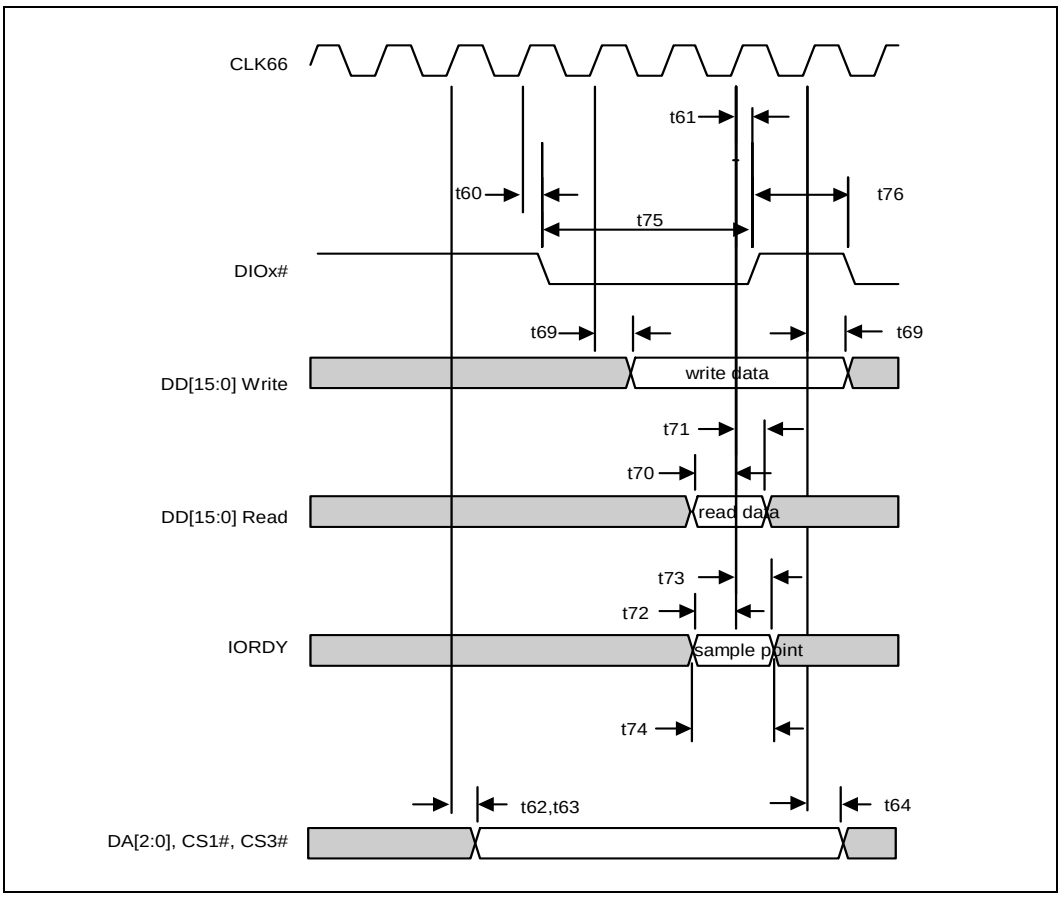


Figure 16-8. IDE Multiword DMA

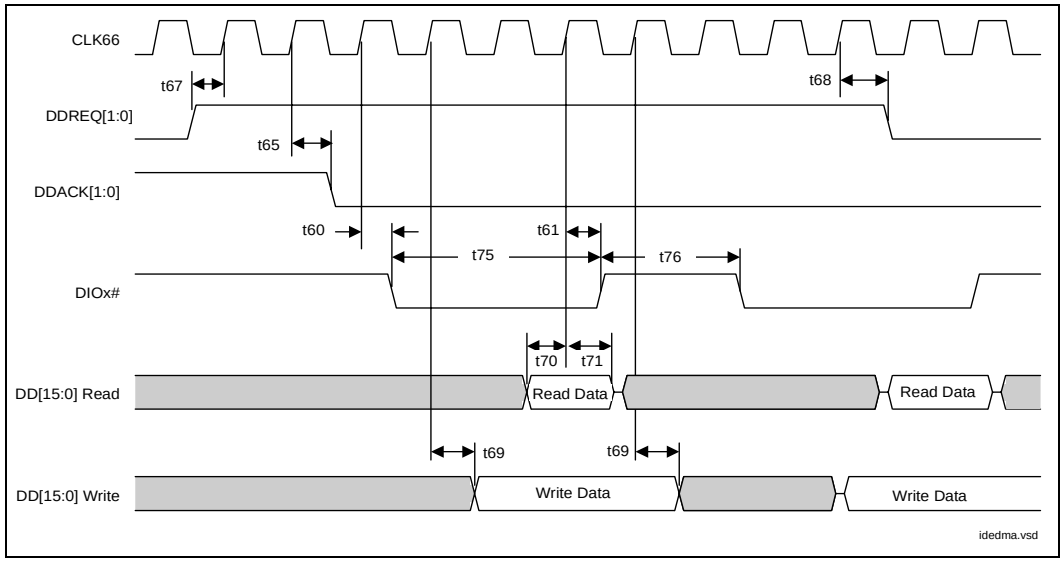


Figure 16-9. Ultra ATA Mode (Drive Initiating a Burst Read)

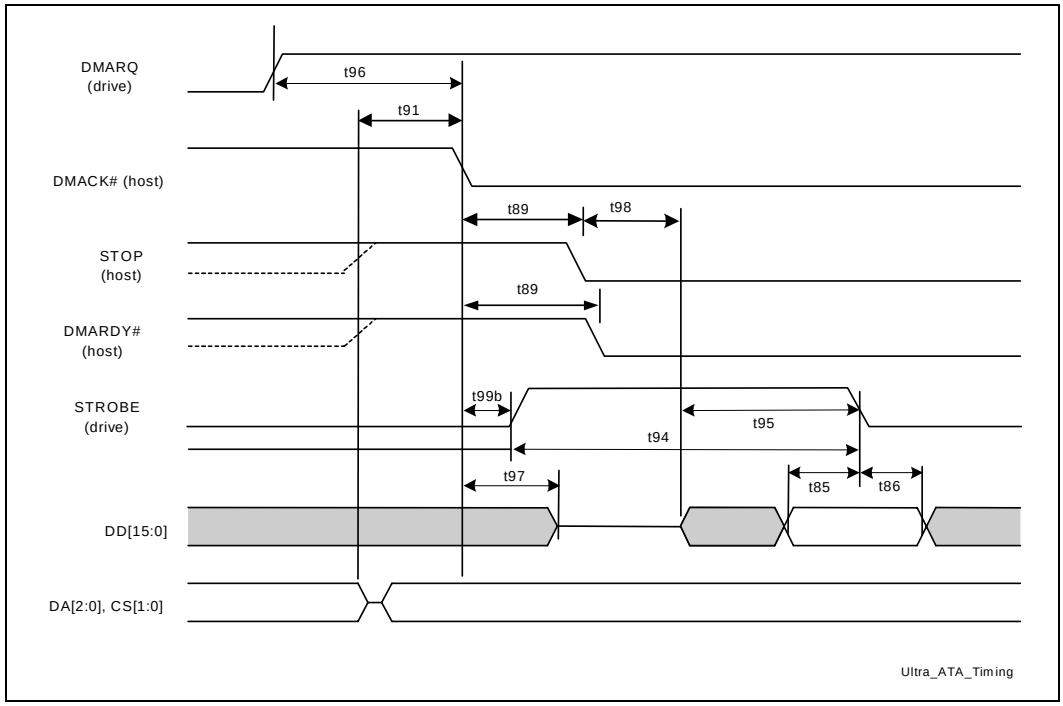


Figure 16-10. Ultra ATA Mode (Sustained Burst)

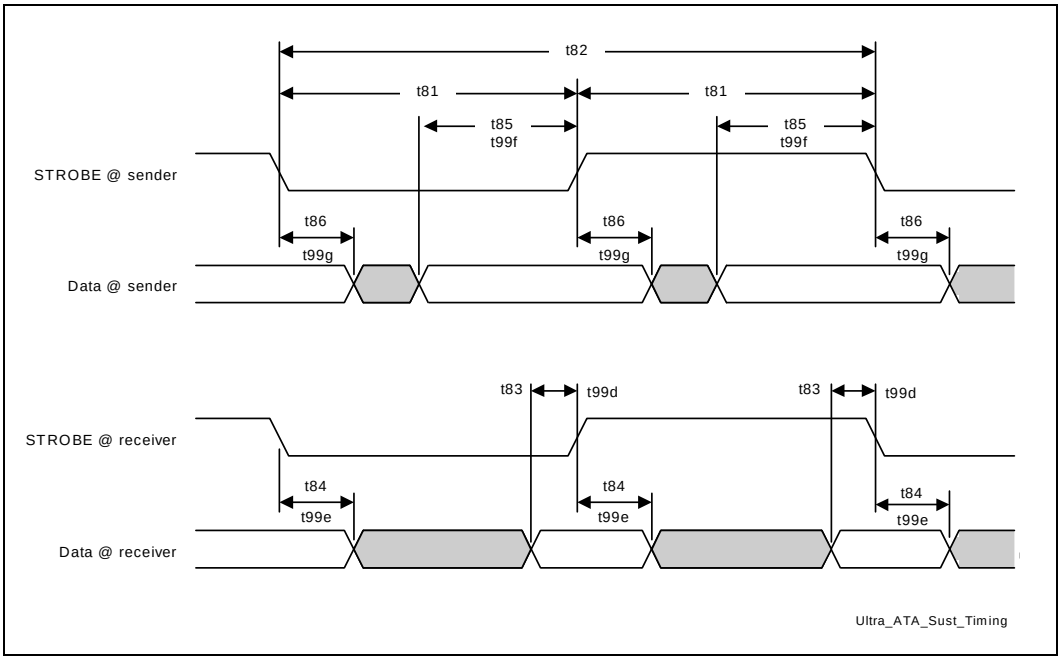


Figure 16-11. Ultra ATA Mode (Pausing a DMA Burst)

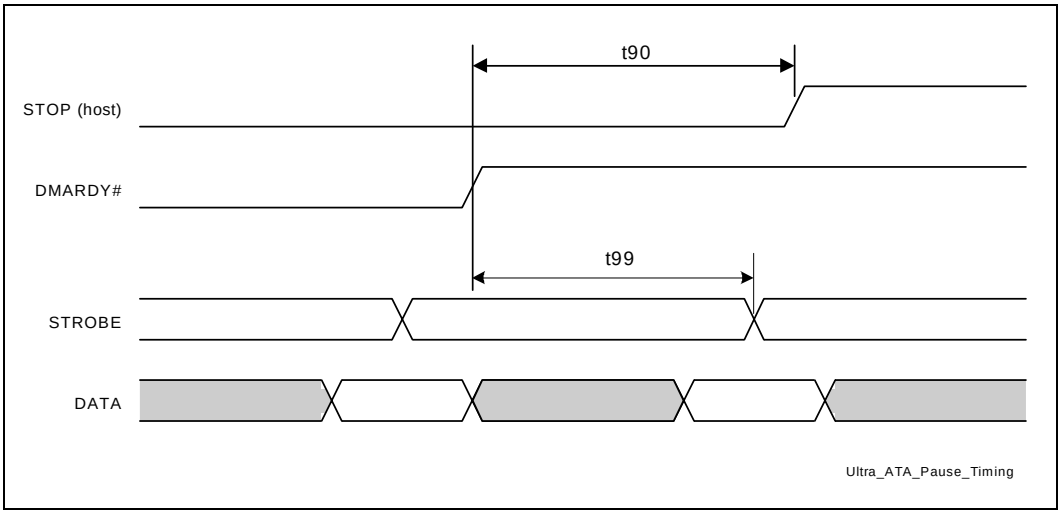


Figure 16-12. Ultra ATA Mode (Terminating a DMA Burst)

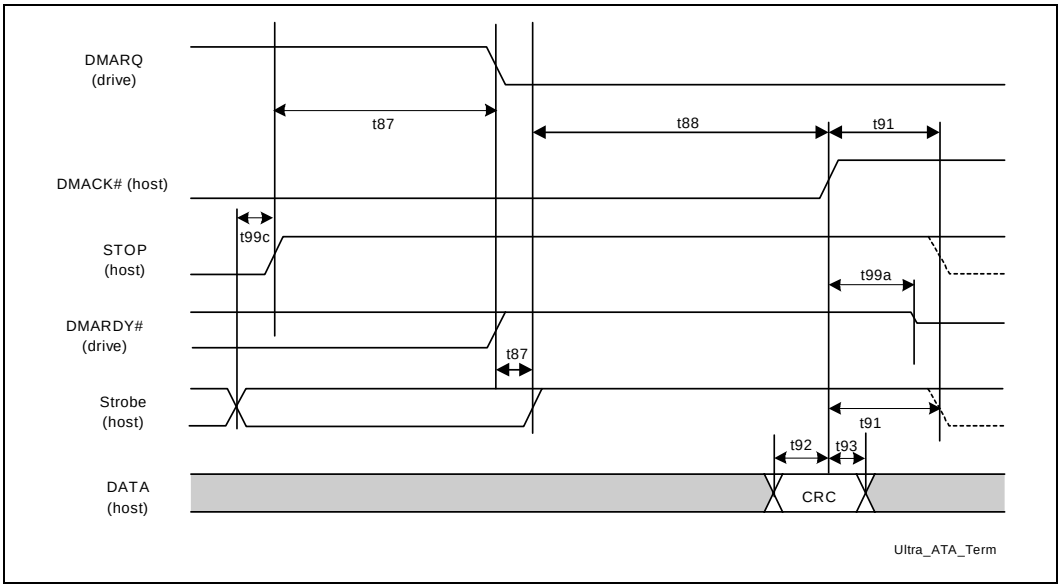


Figure 16-13. USB Rise and Fall Times

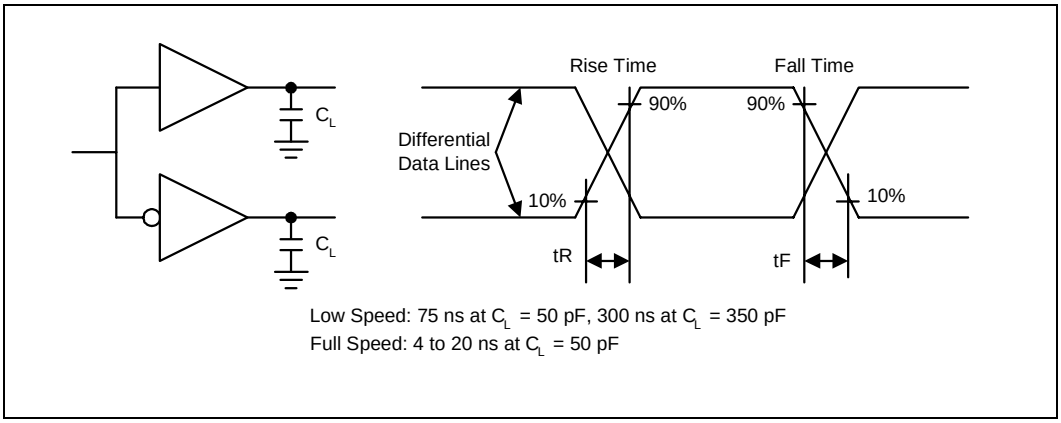


Figure 16-14. USB Jitter

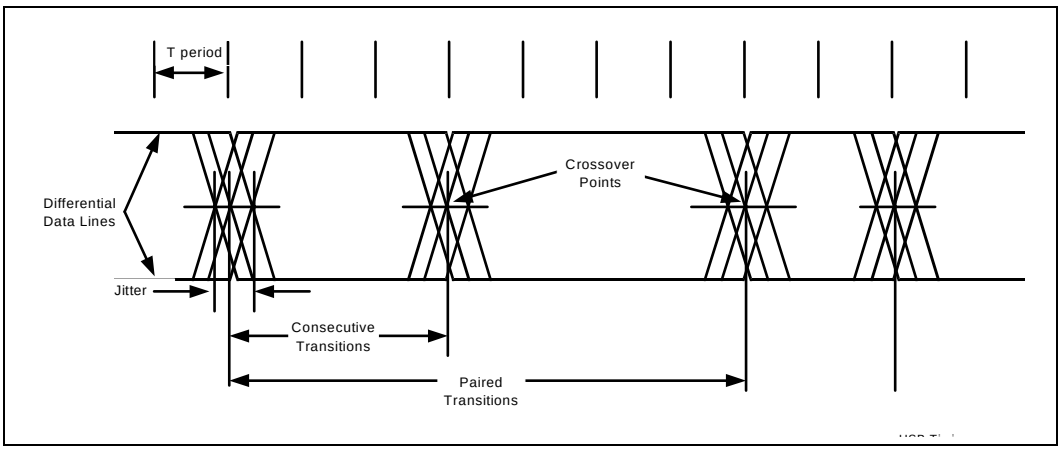


Figure 16-15. USB EOP Width

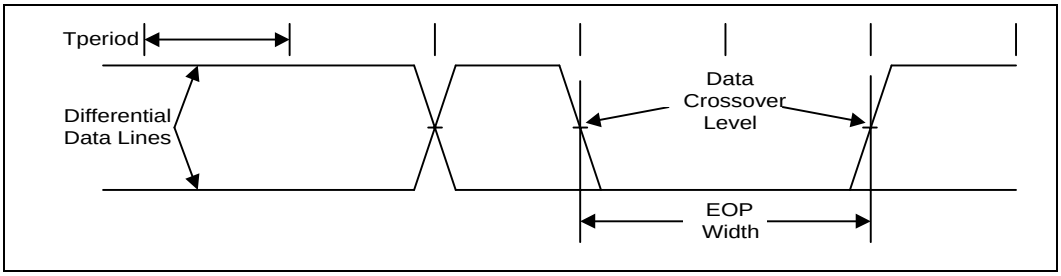


Figure 16-16. SMBus Transaction

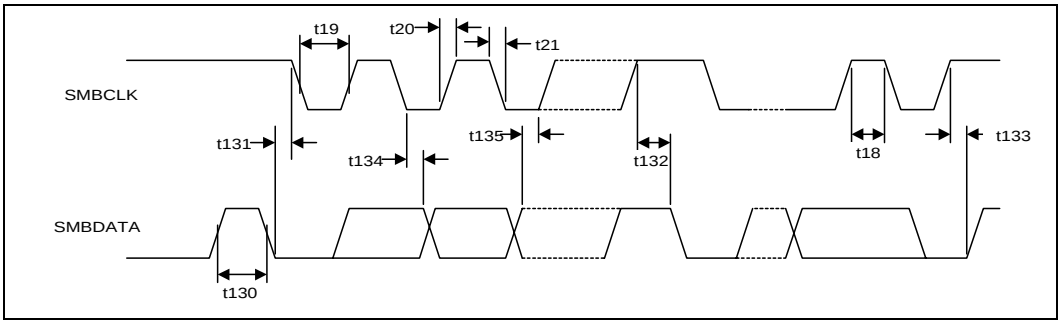


Figure 16-17. SMBus Timeout

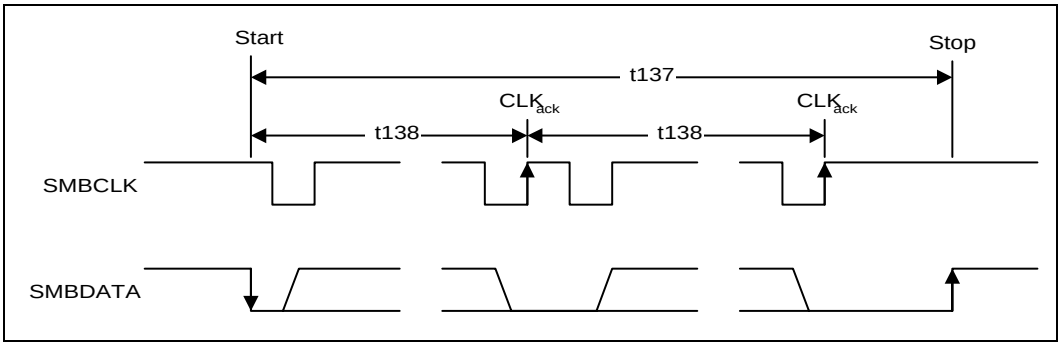


Figure 16-18. Power Sequencing and Reset Signal Timings

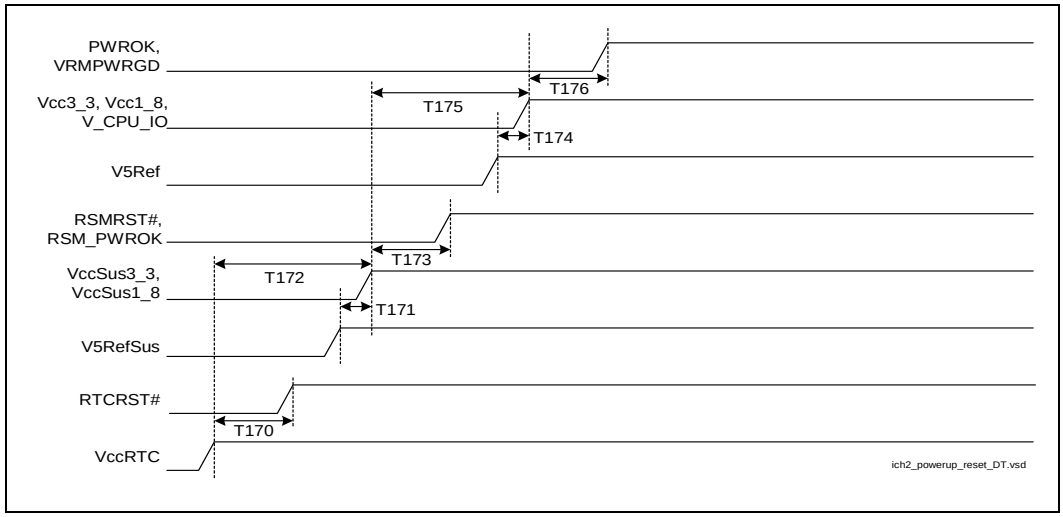


Figure 16-19. 1.8 V/3.3 V Power Sequencing

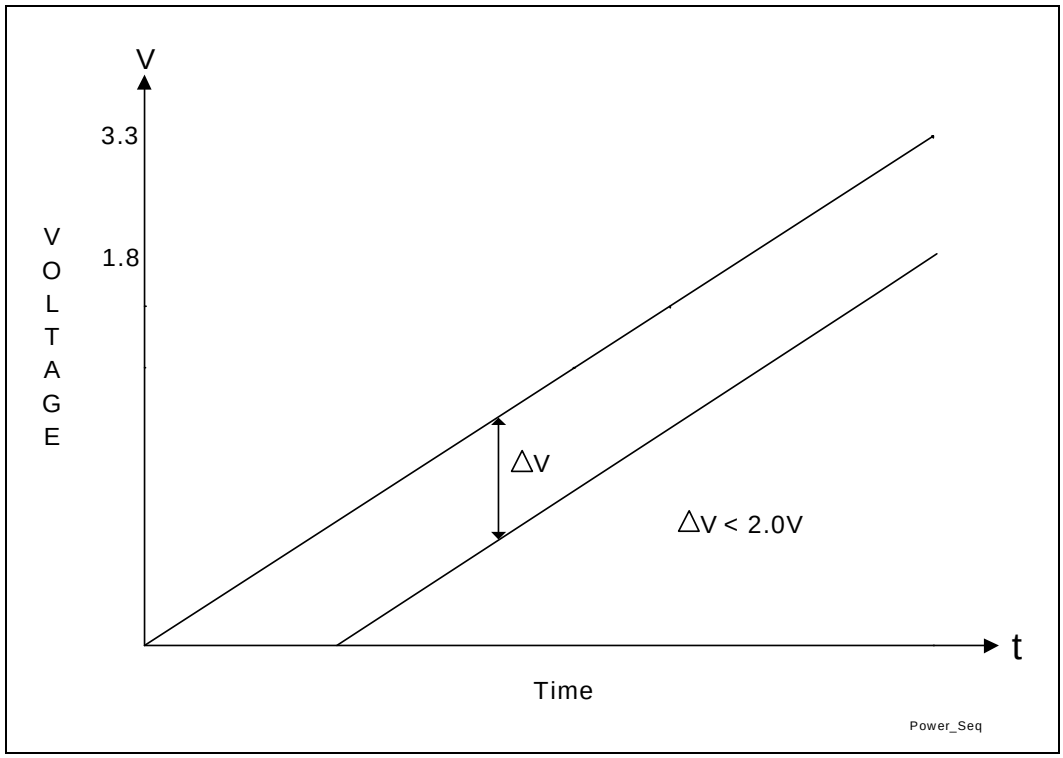


Figure 16-20. G3 (Mechanical Off) to S0 Timings

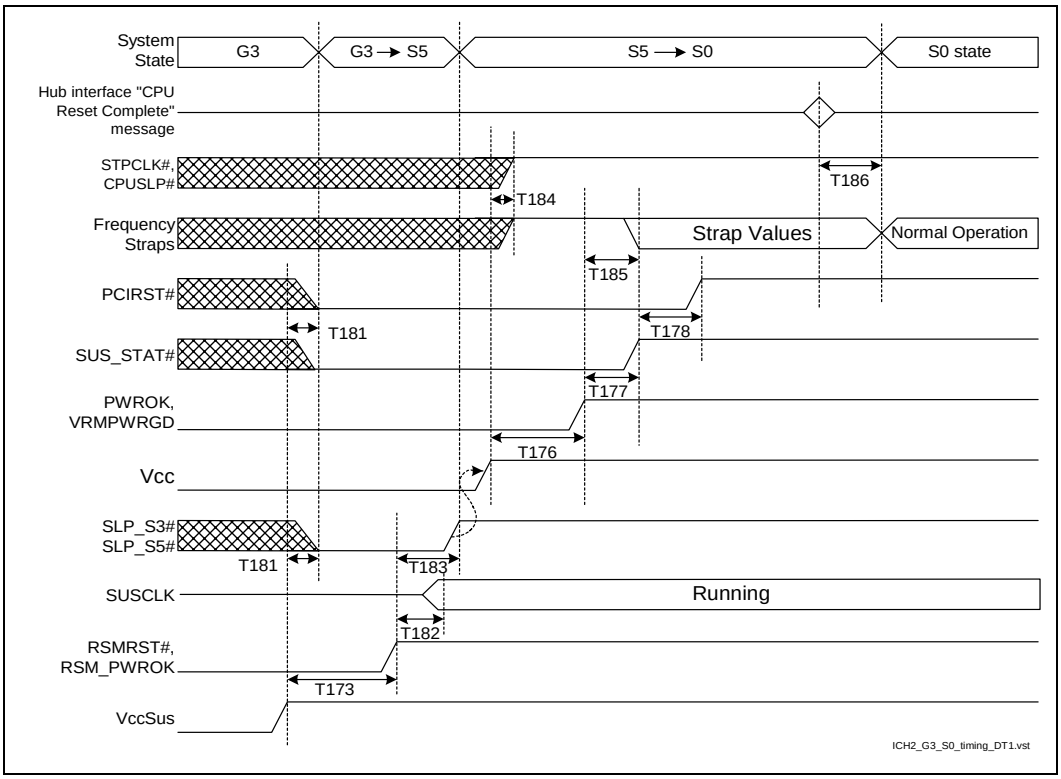


Figure 16-21. S0 to S5 to S0 Timings

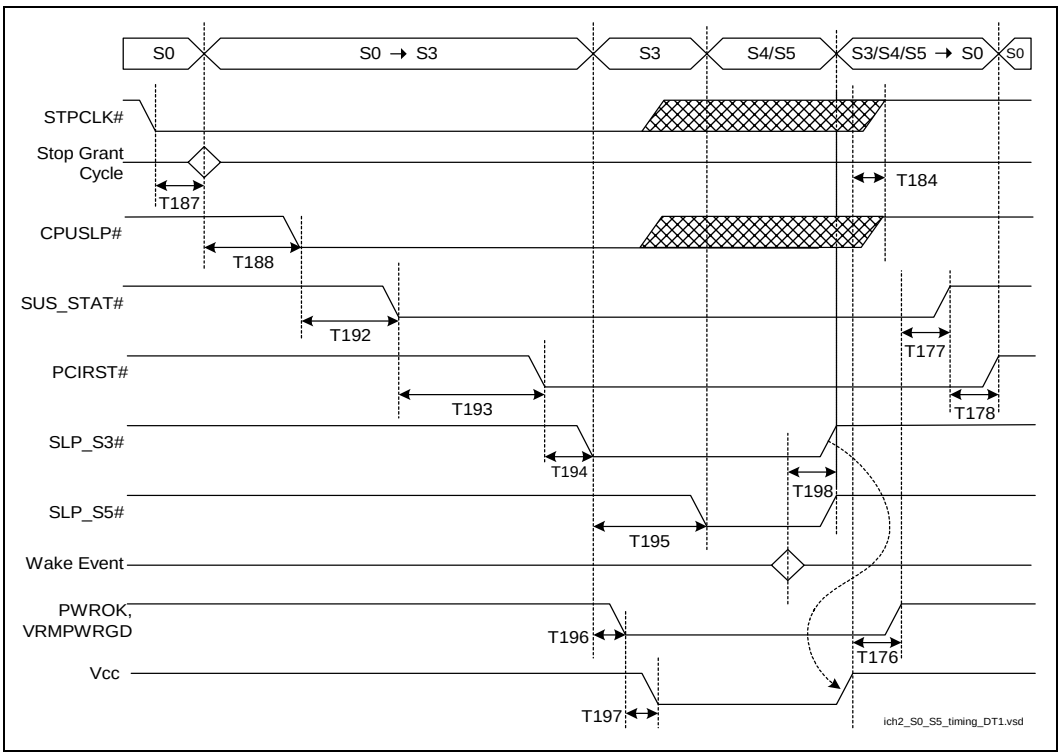
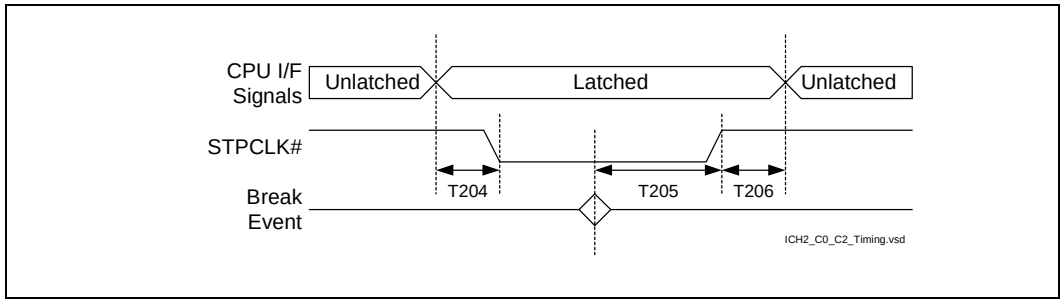


Figure 16-22. C0 to C2 to C0 Timings



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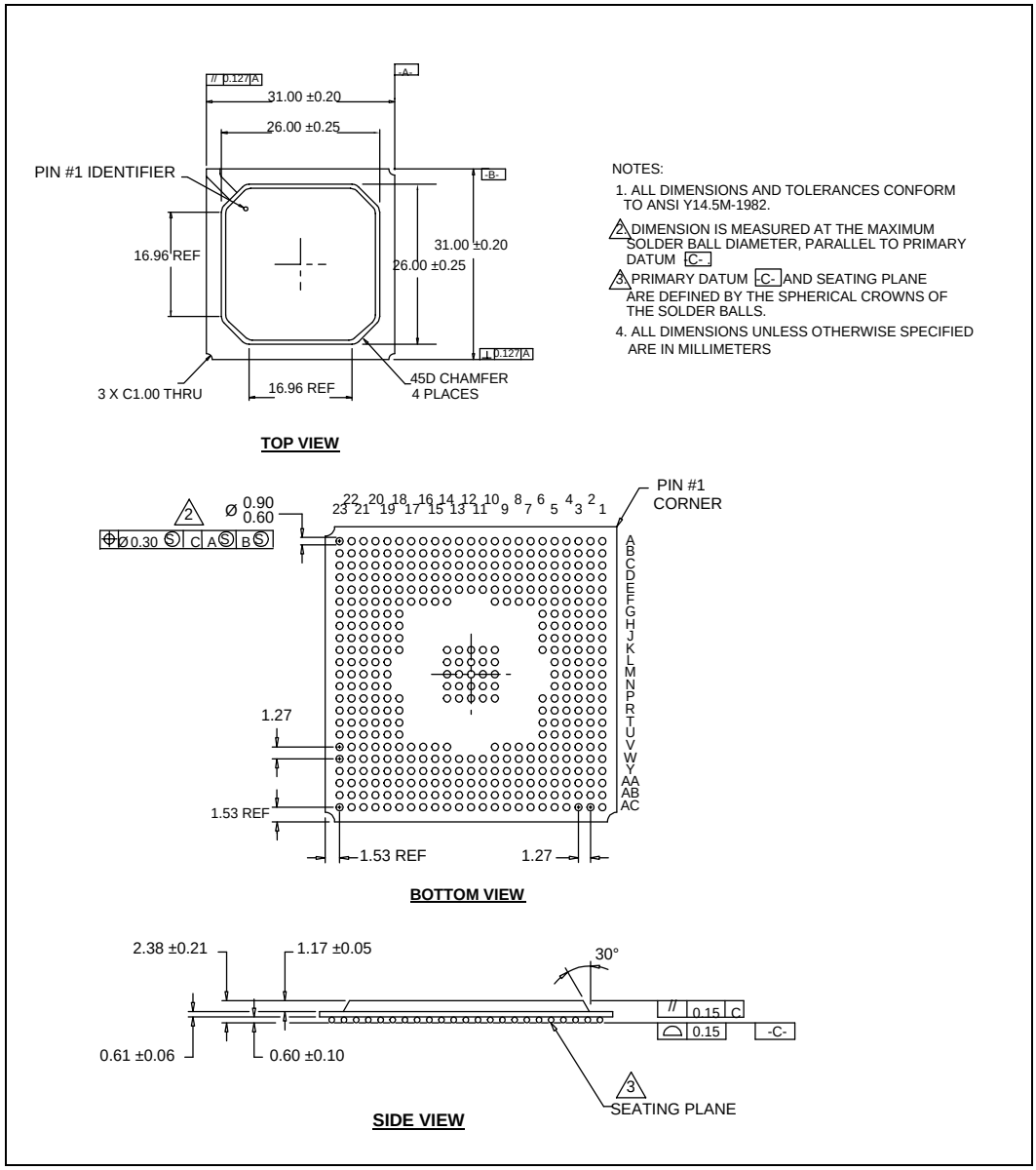
Package Information 17

Figure 17-1 illustrates the ICH3 421 BGA package. All dimensions are in millimeters.

Figure 17-1. Intel® ICH3 Package



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Testability 18

18.1 Test Mode Description

The ICH3 supports two types of test modes, a tri-state test mode and a XOR Chain test mode. Driving RTCRST# low for a specific number of PCI clocks while PWROK is high will activate a particular test mode as described in Table 18-1.

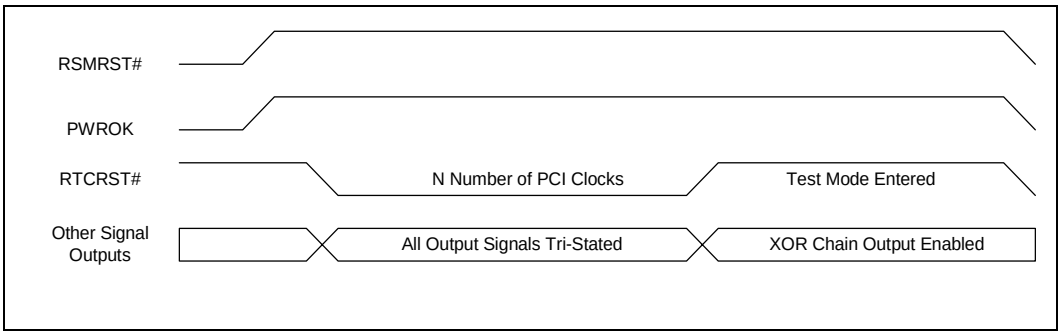
Note: RTCRST# can be driven low any time after PCIRST# is inactive.

Table 18-1. Test Mode Selection

Number of PCI Clocks RTCRST# driven low after PWROK active	Test Mode
<4	No Test Mode Selected
4	XOR Chain 1
5	XOR Chain 2
6	XOR Chain 3
7	XOR Chain 4
8	All Z
9–42	Reserved. DO NOT ATTEMPT
>42	No Test Mode Selected

Figure 18-1 illustrates the entry into a test mode. A particular test mode is entered upon the rising edge of the RTCRST# after being asserted for a specific number of PCI clocks while PWROK is active. To change test modes, the same sequence should be followed again. To restore the ICH3 to normal operation, execute the sequence with RTCRST# being asserted so that no test mode is selected as specified in Table 18-1.

Figure 18-1. Test Mode Entry (XOR Chain Example)



18.2 Tri-state Mode

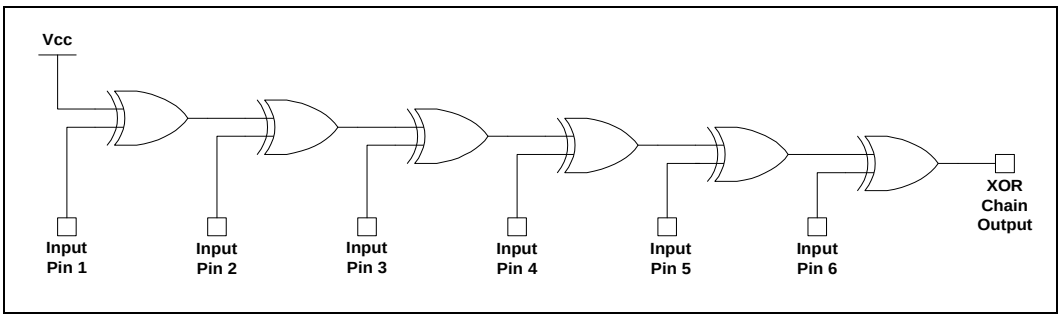
When in the tri-state mode, all outputs and bi-directional pin are tri-stated, including the XOR Chain outputs.

18.3 XOR Chain Mode

In the ICH3, provisions for Automated Test Equipment (ATE) board level testing are implemented with XOR Chains. The ICH3 signals are grouped into four independent XOR chains which are enabled individually. When an XOR chain is enabled, all output and bi-directional buffers within that chain are tri-stated, except for the XOR chain output. Every signal in the enabled XOR chain (except for the XOR chain's output) functions as an input. All output and bi-directional buffers for pins not in the selected XOR chain are tri-stated. Figure 18-2 is a schematic example of XOR chain circuitry.

Table 18-3–Table 18-6 list each XOR chain pin ordering, with the first value being the first input and the last value being the XOR chain output. Table 18-7 lists the signal pins not included in any XOR chain.

Figure 18-2. Example XOR Chain Circuitry



18.3.1 XOR Chain Testability Algorithm Example

XOR chain testing allows motherboard manufacturers to check component connectivity (e.g., opens and shorts to VCC or GND). An example algorithm to do this is shown in Table 18-2.

Table 18-2. XOR Test Pattern Example

Vector	Input Pin 1	Input Pin 2	Input Pin 3	Input Pin 4	Input Pin 5	Input Pin 6	XOR Output
1	0	0	0	0	0	0	1
2	1	0	0	0	0	0	0
3	1	1	0	0	0	0	1
4	1	1	1	0	0	0	0
5	1	1	1	1	0	0	1
6	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1

In this example, Vector 1 applies all 0s to the chain inputs. The outputs being non-inverting, will consistently produce a 1 at the XOR output on a good board. One short to Vcc (or open floating to Vcc) will result in a 0 at the chain output, signaling a defect.

Likewise, applying Vector 7 (all 1s) to the chain inputs (given that there are an even number of input signals in the chain), will consistently produce a 1 at the XOR chain output on a good board. One short to Vss (or open floating to Vss) will result in a 0 at the chain output, signaling a defect. It is important to note that the number of inputs pulled to 1 will affect the expected chain output value. If the number of chain inputs pulled to 1 is even, then expect 1 at the output. If the number of chain inputs pulled to 1 is odd, expect 0 at the output.

Continuing with the example in Table 18-2, as the input pins are driven to 1 across the chain in sequence, the XOR Output will toggle between 0 and 1. Any break in the toggling sequence (e.g., 1011) will identify the location of the short or open.

Table 18-3. XOR Chain #1 (RTCRST# Asserted for 4 PCI Clocks While PWROK Active)

Pin Name	Ball #	Notes
AC_SYNC	A7	Top of XOR Chain
AC_SDOUT	C7	2nd signal in XOR
PIRQE#/GPIO2	A6	
GNTA#/GPIO16	B6	
PIRQH#/GPIO5	A5	
PIRQF#/GPIO3	B5	
PIRQG#/GPIO4	C5	
GNT3#	D5	
GNT0#	A4	
GNT4#	B4	
REQA#/GPIO0	C4	
REQB#/REQ5#/ GPIO1	D4	
REQ2#	A3	
GNTB#/GNT5#/ GPIO17	B3	
PIRQD#	A2	
PIRQC#	B2	
PIRQA#	B1	
PIRQB#	C1	
GNT2#	D2	
REQ0#	D3	
AD28	D1	
GNT1#	E3	
REQ4#	E4	
AD26	E2	
AD30	E1	

Pin Name	Ball #	Notes
AD16	F5	
REQ1#	F4	
AD24	F3	
AD22	F2	
FRAME#	F1	
PAR	G5	
AD18	G4	
AD9	G2	
AD20	G1	
AD4	H5	
AD11	H4	
AD6	H3	
STOP#	H2	
TRDY#	H1	
AD2	J4	
AD13	J3	
AD0	J2	
AD15	J1	
C/BE1#	K5	
AD5	K4	
AD3	K3	
C/BE0#	K2	
AD1	K1	
SERR#	L5	
AD10	L4	
		XOR Chain #1
AC_SDIN1	**C11**	**OUTPUT**

Table 18-4. XOR Chain #2 (RTCRST# Asserted for 5 PCI Clocks While PWROK Active)

Pin Name	Ball #	Notes
AD8	L2	Top of XOR Chain
AD7	L1	2nd signal in XOR
AD14	M5	
AD12	M4	
DEVSEL#	M3	
PERR#	M2	
PLOCK#	M1	
AD27	N4	
IRDY#	N3	
AD17	N2	
C/BE2#	N1	
AD31	P5	
AD29	P4	
AD23	P3	
AD19	P2	

Pin Name	Ball #	Notes
AD21	P1	
AD25	R1	
C/BE3#	R2	
REQ3#	R4	
LDRQ0#	T2	
LAD2/FWH2	T3	
LFRAME#	U1	
LAD3/FWH3	U2	
LAD1/FWH1	U3	
LDRQ1#	U4	
LAD0/FHW0	V1	
GPIO7	V2	
GPIO[6]	V4	
THRM#	U5	
GPIO21	V5	
		XOR Chain #2
TP[0]#	**AB3**	**OUTPUT**

Table 18-5. XOR Chain #3 (RTCRST# asserted for 6 PCI Clocks While PWROK Active)

Pin Name	Ball #	Notes
PDD10	W9	Top of XOR Chain
PDD5	Y9	2nd signal in XOR
PDD7	AA9	
PDD6	AB9	
PDD8	AC9	
PDD9	Y10	
PDD2	AA10	
PDD12	AB10	
PDD3	AC10	
PDD4	W11	
PDD11	Y11	
PDD14	AA11	
PDD1	AB11	
PDD13	AC11	
PDD0	W12	
PDIOW#	Y12	
PDDREQ	AB12	
PDD15	AC12	
PDDACK#	Y13	
PIORDY	AB13	
PDIOR#	AC13	
PDA0	AA14	
IRQ14	AB14	
PDA1	AC14	
PDA2	AA15	
PDCS3#	AB15	
PDCS1#	AC15	
IRQ15	W19	

Pin name	Ball #	Notes
GPIO[19]	W20	
GPIO[20]	V21	
VRMPWRGD	V19	
GPIO[22]	Y20	
GPIO[18]	U21	
GPIO[23]	U20	
A20GATE	Y22	
RCIN#	U22	
CPUPWRGD	W23	
NC	AB21	
NC	AB22	
INIT#	AB23	
SMI#	Y23	
CPU_SLP#	W21	
IGNNE#	AA21	
NMI	Y21	
INTR	AA23	
A20M#	V23	
STPCLK#	U23	
HI_STBF	P23	
GPIO32	H20	
GPIO35	G19	
GPIO33	G22	
GPIO34	F21	
GPIO37	E21	
GPIO36	E22	Last in XOR Chain
		XOR Chain #3
RI#	**AA1**	**OUTPUT**

Table 18-6. XOR Chain #4 (RTCRST# Asserted for 7 PCI Clocks While PWROK Active)

Pin Name	Ball #	Notes
SDD8	W13	Top of XOR Chain
SDD6	AA13	2nd signal in XOR
SDD5	Y14	
SDD7	W15	
SDD10	Y15	
SDD11	AC16	
SDD3	AB16	
SDD9	Y16	
SDD12	AB17	
SDD15	AC18	
SDD4	W16	
SDIOW#	AA18	
SDD2	AC17	
SDD0	Y17	
SDDREQ	AB18	
SDD14	Y18	
SDD13	AA17	
SDD1	W17	
SIORDY	AB19	
SDIOR#	AC19	
SDDACK#	Y19	
SDA1	AA19	
SDA2	AB20	
SDA0	AC20	
SDCS3#	AC22	
SDCS1#	AC21	
HI7	T23	
HI11	R19	
HI6	R20	
HI5	R22	
HI9	P19	
HI4	P21	
HI_STBS	N22	
HI10	N19	
HI3	N20	
HI8	M19	
HI1	M21	
HI2	M23	

Pin Name	Ball #	Notes
GPIO42	D23	
GPIO8	W2	
PME#	W1	
GPIO25	W3	
PCIRST#	Y1	
GPIO13	Y2	
GPIO28	Y3	
GPIO12	Y4	
SLP_S5#	AA2	
GPIO27	W4	
SMLINK1	AB2	
PWRBTN#	AB1	
GPIO[24]	AC2	
SMLINK0	AC3	
SUSCLK	AA4	
SUS_STAT#	AB4	
SMBCLK	AC4	
SLP_S3#	AA5	
SMBDATA	AB5	
SMBALERT#/ GPIO11	AC5	
OC4#	A12	
OC3#	B12	
OC2#	C12	
OC1#	D12	
OC5#	A11	
AC_SDIN0	B11	
AC_RST#	D11	
USBP0P	D19	
USBP0N	D18	
USBP1P	A19	
USBP1N	A18	
USBP2P	E17	
USBP2N	E16	
USBP3P	B17	
USBP3N	B16	
USBP4P	D15	
USBP4N	D14	
USBP5P	A15	

Table 18-6. XOR Chain #4 (RTCRST# Asserted for 7 PCI Clocks While PWROK Active)

Pin Name	Ball #	Notes
HI0	L22	
HICOMP	K19	
APICD0	J20	
APICD1	J21	
FERR#	J22	
SERIRQ	H22	
GPIO38	H21	
SPKR	H23	
GPIO41	G21	
GPIO39	G23	
GPIO40	F23	
GPIO43	E23	

Pin Name	Ball #	Notes
USBP5N	A14	
LAN_TXD2	A10	
LAN_TXD1	C10	
EE_SHCLK	D10	
LAN_RXD2	A9	
LAN_TXD0	B9	
EE_CS	E9	
LAN_RXD1	A8	
LAN_RXD0	C8	
EE_DIN	D8	
EE_DOUT	E8	
LAN_RSTSYNC	D7	Last in XOR Chain
		XOR Chain #4
OC0#	**E12**	**OUTPUT**

Table 18-7. Signals Not in XOR Chain

Pin Name	Ball #	Notes
RSMRST#	AA7	
PWROK	AA6	
RTCX1	AC7	
RTCX2	AC6	
VBIAS	AB7	
RTCRST#	Y7	
LAN_CLK	C9	
AC_BIT_CLK	B7	

Pin Name	Ball #	Notes
CLK14	J23	
CLK48	F20	
CLK66	T19	
APICCLK	J19	
PCICLK	T5	
INTRUDER#	Y6	
LAN_RST#	Y5	

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Register Index A

Table A-1. Intel® ICH3 PCI Configuration Registers

Register Name	Offset	Datasheet Section and Location
LAN Controller (B1:D8:F0)		
Vendor Identification	00–01h	Section 7.1.1, “VID—Vendor ID Register (LAN Controller—B1:D8:F0)” on page 7-236
Device Identification	02–03h	Section 7.1.2, “DID—Device ID Register (LAN Controller—B1:D8:F0)” on page 7-236
PCI Command	04–05h	Section 7.1.3, “PCICMD—PCI Command Register (LAN Controller—B1:D8:F0)” on page 7-236
PCI Device Status	06–07h	Section 7.1.4, “PCISTS—PCI Status Register (LAN Controller—B1:D8:F0)” on page 7-237
Revision Identification	08h	Section 7.1.5, “REVID—Revision ID Register (LAN Controller—B1:D8:F0)” on page 7-237
Programming Interface	09h	
Sub Class Code	0Ah	Section 7.1.6, “SCC—Sub Class Code Register (LAN Controller—B1:D8:F0)” on page 7-238
Base Class Code	0Bh	Section 7.1.7, “BCC—Base Class Code Register (LAN Controller—B1:D8:F0)” on page 7-238
Cache Line Size	0Ch	Section 7.1.8, “CLS—Cache Line Size Register (LAN Controller—B1:D8:F0)” on page 7-238
Master Latency Timer	0Dh	Section 7.1.9, “PMLT—PCI Master Latency Timer Register (LAN Controller—B1:D8:F0)” on page 7-238
Header Type	0Eh	Section 7.1.10, “HEADTYP—Header Type Register (LAN Controller—B1:D8:F0)” on page 7-239
CSR Memory-Mapped Base Address	10–13h	Section 7.1.11, “CSR_MEM_BASE CSR—Memory-Mapped Base Address Register (LAN Controller—B1:D8:F0)” on page 7-239
CSR I/O-Mapped Base Address	14–17h	Section 7.1.12, “CSR_IO_BASE—CSR I/O-Mapped Base Address Register (LAN Controller—B1:D8:F0)” on page 7-239
Subsystem Vendor ID	2C–2Dh	Section 7.1.13, “SVID—Subsystem Vendor ID Register (LAN Controller—B1:D8:F0)” on page 7-240
Subsystem ID	2E–2Fh	Section 7.1.14, “SID—Subsystem ID Register (LAN Controller—B1:D8:F0)” on page 7-240
Capabilities Pointer	34h	Section 7.1.15, “CAP_PTR—Capabilities Pointer Register (LAN Controller—B1:D8:F0)” on page 7-240
Interrupt Line Register	3Ch	Section 7.1.16, “INT_LN—Interrupt Line Register (LAN Controller—B1:D8:F0)” on page 7-241
Interrupt Pin Register	3Dh	Section 7.1.17, “INT_PN—Interrupt Pin Register (LAN Controller—B1:D8:F0)” on page 7-241
Minimum Grant Register	3Eh	Section 7.1.18, “MIN_GNT—Minimum Grant Register (LAN Controller—B1:D8:F0)” on page 7-241
Maximum Latency Register	3Fh	Section 7.1.19, “MAX_LAT—Maximum Latency Register (LAN Controller—B1:D8:F0)” on page 7-241

Table A-1. Intel® ICH3 PCI Configuration Registers (Continued)

Register Name	Offset	Datasheet Section and Location
Capability ID Register	DCh	Section 7.1.20, “CAP_ID—Capability ID Register (LAN Controller—B1:D8:F0)” on page 7-242
Next Item Pointer	DDh	Section 7.1.21, “NXT_PTR—Next Item Pointer Register (LAN Controller—B1:D8:F0)” on page 7-242
Power Management Capabilities	DE–DFh	Section 7.1.22, “PM_CAP—Power Management Capabilities Register (LAN Controller—B1:D8:F0)” on page 7-242
Power Management Control/Status Register	E0–E1h	Section 7.1.23, “PMCSR—Power Management Control/ Status Register (LAN Controller—B1:D8:F0)” on page 7-243
Data Register	E2h	Section 7.1.24, “PCIDATA—PCI Power Management Data Register (LAN Controller—B1:D8:F0)” on page 7-244
Hub Interface to PCI Bridge D30:F0		
Vendor ID	00–01h	Section 8.1.1, “VID—Vendor ID Register (HUB-PCI—D30:F0)” on page 8-260
Device ID	02–03h	Section 8.1.2, “DID—Device ID Register (HUB-PCI—D30:F0)” on page 8-260
PCI Device Command Register	04–05h	Section 8.1.3, “CMD—Command Register (HUB-PCI—D30:F0)” on page 8-261
PCI Device Status Register	06–07h	Section 8.1.4, “PD_STS—Primary Device Status Register (HUB-PCI—D30:F0)” on page 8-262
Revision ID	08h	Section 8.1.5, “REVID—Revision ID Register (HUB-PCI—D30:F0)” on page 8-263
Sub Class Code	0Ah	Section 8.1.6, “SCC—Sub Class Code Register (HUB-PCI—D30:F0)” on page 8-263
Base Class Code	0Bh	Section 8.1.7, “BCC—Base-Class Code Register (HUB-PCI—D30:F0)” on page 8-263
Primary Master Latency Timer	0Dh	Section 8.1.8, “PMLT—Primary Master Latency Timer Register (HUB-PCI—D30:F0)” on page 8-263
Header Type	0Eh	Section 8.1.9, “HEADTYP—Header Type Register (HUB-PCI—D30:F0)” on page 8-264
Primary Bus Number	18h	Section 8.1.10, “PBUS_NUM—Primary Bus Number Register (HUB-PCI—D30:F0)” on page 8-264
Secondary Bus Number	19h	Section 8.1.11, “SBUS_NUM—Secondary Bus Number Register (HUB-PCI—D30:F0)” on page 8-264
Subordinate Bus Number	1Ah	Section 8.1.12, “SUB_BUS_NUM—Subordinate Bus Number Register (HUB-PCI—D30:F0)” on page 8-264
Secondary Master Latency Timer	1Bh	Section 8.1.13, “SMLT—Secondary Master Latency Timer Register (HUB-PCI—D30:F0)” on page 8-265
I/O Base Register	1Ch	Section 8.1.14, “IOBASE—I/O Base Register (HUB-PCI—D30:F0)” on page 8-265
I/O Limit Register	1Dh	Section 8.1.15, “IOLIM—I/O Limit Register (HUB-PCI—D30:F0)” on page 8-265
Secondary Status Register	1E–1Fh	Section 8.1.16, “SECSTS—Secondary Status Register (HUB-PCI—D30:F0)” on page 8-266
Memory Base	20–21h	Section 8.1.17, “MEMBASE—Memory Base Register (HUB-PCI—D30:F0)” on page 8-267

Table A-1. Intel® ICH3 PCI Configuration Registers (Continued)

Register Name	Offset	Datasheet Section and Location
Memory Limit	22–23h	Section 8.1.18, “MEMLIM—Memory Limit Register (HUB-PCI—D30:F0)” on page 8-267
Prefetchable Memory Base	24–25h	Section 8.1.19, “PREF_MEM_BASE—Prefetchable Memory Base Register (HUB-PCI—D30:F0)” on page 8-267
Prefetchable Memory Limit	26–27h	Section 8.1.20, “PREF_MEM_MLT—Prefetchable Memory Limit Register (HUB-PCI—D30:F0)” on page 8-268
I/O Base Upper 16 Bits	30–31h	Section 8.1.21, “IOBASE_HI—I/O Base Upper 16 Bits Register (HUB-PCI—D30:F0)” on page 8-268
I/O Limit Upper 16 Bits	32–33h	Section 8.1.22, “IOLIM_HI—I/O Limit Upper 16 Bits Register (HUB-PCI—D30:F0)” on page 8-268
Interrupt Line	3Ch	Section 8.1.23, “INT_LINE—Interrupt Line Register (HUB-PCI—D30:F0)” on page 8-268
Bridge Control	3E–3Fh	Section 8.1.24, “BRIDGE_CNT—Bridge Control Register (HUB-PCI—D30:F0)” on page 8-269
ICH3 Configuration Register	50–51h	Section 8.1.27, “CNF—ICH3 Configuration Register (HUB-PCI—D30:F0)” on page 8-271
Multi-Transaction Timer	70h	Section 8.1.28, “MTT—Multi-Transaction Timer Register (HUB-PCI—D30:F0)” on page 8-271
PCI Master Status	82h	Section 8.1.29, “PCI_MAST_STS—PCI Master Status Register (HUB-PCI—D30:F0)” on page 8-272
Error Command Register	90h	Section 8.1.30, “ERR_CMD—Error Command Register (HUB-PCI—D30:F0)” on page 8-272
Error Status Register	92h	Section 8.1.31, “ERR_STS—Error Status Register (HUB-PCI—D30:F0)” on page 8-273
LPC Bridge D31:F0		
Vendor ID	00–01h	Section 9.1.1, “VID—Vendor ID Register (LPC I/F—D31:F0)” on page 9-276
Device ID	02–03h	Section 9.1.2, “DID—Device ID Register (LPC I/F—D31:F0)” on page 9-276
PCI Command Register	04–05h	Section 9.1.3, “PCICMD—PCI COMMAND Register (LPC I/F—D31:F0)” on page 9-277
PCI Device Status Register	06–07h	Section 9.1.4, “PCISTA—PCI Device Status Register (LPC I/F—D31:F0)” on page 9-278
Revision ID	08h	Section 9.1.5, “REVID—Revision ID Register (LPC I/F—D31:F0)” on page 9-278
Programming Interface	09h	Section 9.1.6, “PI—Programming Interface Register (LPC I/F—D31:F0)” on page 9-279
Sub Class Code	0Ah	Section 9.1.7, “SCC—Sub Class Code Register (LPC I/F—D31:F0)” on page 9-279
Base Class Code	0Bh	Section 9.1.8, “BCC—Base Class Code Register (LPC I/F—D31:F0)” on page 9-279
Header Type	0Eh	Section 9.1.9, “HEADTYP—Header Type Register (LPC I/F—D31:F0)” on page 9-279
ACPI Base Address Register	40–43h	Section 9.1.10, “PMBASE—ACPI Base Address Register (LPC I/F—D31:F0)” on page 9-280

Table A-1. Intel® ICH3 PCI Configuration Registers (Continued)

Register Name	Offset	Datasheet Section and Location
ACPI Control	44h	Section 9.1.11, “ACPI_CNTL—ACPI Control Register (LPC I/F—D31:F0)” on page 9-280
BIOS Control Register	4E–4Fh	Section 9.1.12, “BIOS_CNTL Register (LPC I/F—D31:F0)” on page 9-281
TCO Control	54h	Section 9.1.13, “TCO_CNTL—TCO Control Register (LPC I/F—D31:F0)” on page 9-281
GPIO Base Address Register	58–5Bh	Section 9.1.14, “GPIOBASE—GPIO Base Address Register (LPC I/F—D31:F0)” on page 9-282
GPIO Control Register	5Ch	Section 9.1.15, “GPIO_CNTL—GPIO Control Register (LPC I/F—D31:F0)” on page 9-282
PIRQ[A–D] Routing Control	60–63h	Section 9.1.16, “PIRQ[n]_ROUT—PIRQ[A,B,C,D] Routing Control Register (LPC I/F—D31:F0)” on page 9-283
Serial IRQ Control Register	64h	Section 9.1.17, “SERIRQ_CNTL—Serial IRQ Control Register (LPC I/F—D31:F0)” on page 9-283
PIRQ[E–H] Routing Control	68–6Bh	Section 9.1.18, “PIRQ[n]_ROUT—PIRQ[E,F,G,H] Routing Control Register (LPC I/F—D31:F0)” on page 9-284
Device 31 Error Configuration Register	88h	Section 9.1.19, “D31_ERR_CFG—Device 31 Error Configuration Register (LPC I/F—D31:F0)” on page 9-284
Device 31 Error Status Register	8Ah	Section 9.1.20, “D31_ERR_STS—Device 31 Error Status Register (LPC I/F—D31:F0)” on page 9-285
PCI DMA Configuration Registers	90–91h	Section 9.1.21, “PCI_DMA_CFG—PCI DMA Configuration Register (LPC I/F—D31:F0)” on page 9-285
General Power Management Configuration 1	A0h	Section 9.8.1.1, “GEN_PMCON_1—General PM Configuration 1 Register (PM—D31:F0)” on page 9-331
General Power Management Configuration 2	A2h	Section 9.8.1.2, “GEN_PMCON_2—General PM Configuration 2 Register (PM—D31:F0)” on page 9-331
General Power Management Configuration 3	A4h	Section 9.8.1.3, “GEN_PMCON_3—General PM Configuration 3 Register (PM—D31:F0)” on page 9-332
GPI_ROUT	B8–BBh	Section 9.8.1.5, “GPI_ROUT—GPI Routing Control Register (PM—D31:F0)” on page 9-333
I/O Monitor Trap Forwarding Enable Register	C0h	Section 9.8.1.6, “TRP_FWD_EN—I/O Monitor Trap Forwarding Enable Register (PM—D31:F0)” on page 9-333
I/O Monitor [4:7] Trap Range Registers	C4h, C6h, C8h, CAh	Section 9.8.1.7, “MON[n]_TRP_RNG—I/O Monitor [4:7] Trap Range Register for Devices 4–7 (PM—D31:F0)” on page 9-334
I/O Monitor [4:7] Trap Mask Register	CCh	Section 9.8.1.8, “MON_TRP_MSK—I/O Monitor Trap Range Mask Register for Devices 4-7 (PM—D31:F0)” on page 9-334
General Control	D0–D3h	Section 9.1.22, “GEN_CNTL—General Control Register (LPC I/F—D31:F0)” on page 9-286
General Status	D4–D7h	Section 9.1.23, “GEN_STA—General Status Register (LPC I/F—D31:F0)” on page 9-288
Real Time Clock Configuration	D8h	Section 9.1.24, “RTC_CONF—RTC Configuration Register (LPC I/F—D31:F0)” on page 9-289

Table A-1. Intel® ICH3 PCI Configuration Registers (Continued)

Register Name	Offset	Datasheet Section and Location
LPC COM Port Decode Ranges	E0h	Section 9.1.25, “COM_DEC—LPC I/F Communication Port Decode Ranges Register (LPC I/F—D31:F0)” on page 9-289
LPC FDD & LPT Decode Ranges	E1h	Section 9.1.26, “FDD/LPT_DEC—LPC I/F FDD & LPT Decode Ranges Register (LPC I/F—D31:F0)” on page 9-290
LPC Sound Decode Ranges	E2h	Section 9.1.27, “SND_DEC—LPC I/F Sound Decode Ranges Register (LPC I/F—D31:F0)” on page 9-290
FWH Decode Enable 1 Register	E3h	Section 9.1.28, “FWH_DEC_EN1—FWH Decode Enable 1 Register (LPC I/F—D31:F0)” on page 9-291
LPC Generic Decode Range 1	E4–E5h	Section 9.1.29, “GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0)” on page 9-292
LPC Enables	E6–E7h	Section 9.1.30, “LPC_EN—LPC I/F Enables Register (LPC I/F—D31:F0)” on page 9-292
FWH Select 1 Register	E8h	Section 9.1.31, “FWH_SEL1—FWH Select 1 Register (LPC I/F—D31:F0)” on page 9-294
LPC Generic Decode Range 2	EC–EDh	Section 9.1.32, “GEN2_DEC—LPC I/F Generic Decode Range 2 Register (LPC I/F—D31:F0)” on page 9-295
FWH Select 2 Register		Section 9.1.33, “FWH_SEL2—FWH Select 2 Register (LPC I/F—D31:F0)” on page 9-295
FWH Decode Enable 2 Register		Section 9.1.34, “FWH_DEC_EN2—FWH Decode Enable 2 Register (LPC I/F—D31:F0)” on page 9-296
Function Disable Register	F2h	Section 9.1.35, “FUNC_DIS—Function Disable Register (LPC I/F—D31:F0)” on page 9-297
IDE Controller (D31:F1)		
Vendor ID	00–01h	Section 10.1.1, “VID—Vendor ID Register (IDE—D31:F1)” on page 10-366
Device ID	02–03h	Section 10.1.2, “DID—Device ID Register (IDE—D31:F1)” on page 10-366
Command Register	04–05h	Section 10.1.3, “CMD—Command Register (IDE—D31:F1)” on page 10-366
Device Status	06–07h	Section 10.1.4, “STS—Device Status Register (IDE—D31:F1)” on page 10-367
Revision ID	08h	Section 10.1.5, “RID—Revision Identification Register (IDE—D31:F1)” on page 10-367
Programming Interface	09h	Section 10.1.6, “PI—Programming Interface Register (IDE—D31:F1)” on page 10-368
Sub Class Code	0Ah	Section 10.1.7, “SCC—Sub Class Code Register (IDE—D31:F1)” on page 10-368
Base Class Code	0Bh	Section 10.1.8, “BCC—Base Class Code Register (IDE—D31:F1)” on page 10-368
Master Latency Timer	0Dh	Section 10.1.9, “MLT—Master Latency Timer Register (IDE—D31:F1)” on page 10-368
Header Type	0Eh	
Bus Master Base Address Register	20–23h	Section 10.1.12, “SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1)” on page 10-369

Table A-1. Intel® ICH3 PCI Configuration Registers (Continued)

Register Name	Offset	Datasheet Section and Location
Primary/Secondary IDE Timing	40–43h	Section 10.1.18, “INTR_LN—Interrupt Line Register (IDE—D31:F1)” on page 10-371
Slave IDE Timing	44h	Section 10.1.21, “SLV_IDETIM—Slave (Drive 1) IDE Timing Register (IDE—D31:F1)” on page 10-373
Synchronous DMA Control Register	48h	Section 10.1.22, “SDMA_CNT—Synchronous DMA Control Register (IDE—D31:F1)” on page 10-374
Synchronous DMA Timing Register	4A–4Bh	Section 10.1.23, “SDMA_TIM—Synchronous DMA Timing Register (IDE—D31:F1)” on page 10-375
IDE I/O Configuration Register	54h	Section 10.1.24, “IDE_CONFIG—IDE I/O Configuration Register” on page 10-376
USB Controller (D31:F2)		
Vendor ID	00–01h	Section 11.1.1, “VID—Vendor Identification Register (USB—D29:F0/F1/F2)” on page 11-381
Device ID	02–03h	Section 11.1.2, “DID—Device Identification Register (USB—D29:F0/F1/F2)” on page 11-382
Command Register	04–05h	Section 11.1.3, “CMD—Command Register (USB—D29:F0/F1/F2)” on page 11-382
Device Status	06–07h	Section 11.1.4, “STA—Device Status Register (USB—D29:F0/F1/F2)” on page 11-383
Revision ID	08h	Section 11.1.5, “RID—Revision Identification Register (USB—D29:F0/F1/F2)” on page 11-383
Programming Interface	09h	Section 11.1.6, “PI—Programming Interface Register (USB—D29:F0/F1/F2)” on page 11-383
Sub Class Code	0Ah	Section 11.1.7, “SCC—Sub Class Code Register (USB—D29:F0/F1/F2)” on page 11-384
Base Class Code	0Bh	Section 11.1.8, “BCC—Base Class Code Register (USB—D29:F0/F1/F2)” on page 11-384
Base Address Register	20–23h	Section 11.1.10, “BASE—Base Address Register (USB—D29:F0/F1/F2)” on page 11-385
Interrupt Line	3Ch	Section 11.1.13, “INTR_LN—Interrupt Line Register (USB—D29:F0/F1/F2)” on page 11-385
Interrupt Pin	3Dh	Section 11.1.14, “INTR_PN—Interrupt Pin Register (USB—D29:F0/F1/F2)” on page 11-386
Serial Bus Release Number	60h	Section 11.1.15, “SB_RELNUM—Serial Bus Release Number Register (USB—D29:F0/F1/F2)” on page 11-386
USB Legacy Keyboard/Mouse Cotrol	C0–C1h	Section 11.1.16, “USB_LEGKEY—USB Legacy Keyboard/Mouse Control Register (USB—D29:F0/F1/F2)” on page 11-386
USB Resume Enable	C4h	Section 11.1.17, “USB_RES—USB Resume Enable Register (USB—D29:F0/F1/F2)” on page 11-388
SMBus Controller (D31:F3)		
Vendor ID	00–01h	Section 12.1.1, “VID—Vendor Identification Register (SMBUS—D31:F3)” on page 12-399
Device ID	02–03h	Section 12.1.2, “DID—Device Identification Register (SMBUS—D31:F3)” on page 12-399
Command Register	04–05h	Section 12.1.3, “CMD—Command Register (SMBUS—D31:F3)” on page 12-400

Table A-1. Intel® ICH3 PCI Configuration Registers (Continued)

Register Name	Offset	Datasheet Section and Location
Device Status	06–07h	Section 12.1.4, “STA—Device Status Register (SMBUS—D31:F3)” on page 12-400
Revision ID	08h	Section 12.1.5, “RID—Revision Identification Register (SMBUS—D31:F3)” on page 12-401
Programming Interface	09h	
Sub Class Code	0Ah	Section 12.1.6, “SCC—Sub Class Code Register (SMBUS—D31:F3)” on page 12-401
Base Class Code	0Bh	Section 12.1.7, “BCC—Base Class Code Register (SMBUS—D31:F3)” on page 12-401
SMB Base Address Register	20–23h	Section 12.1.8, “SMB_BASE—SMBus Base Address Register (SMBUS—D31:F3)” on page 12-401
Interrupt Line	3Ch	Section 12.1.11, “INTR_LN—Interrupt Line Register (SMBUS—D31:F3)” on page 12-402
Interrupt Pin	3Dh	Section 12.1.12, “INTR_PN—Interrupt Pin Register (SMBUS—D31:F3)” on page 12-402
Host Configuration	40h	Section 12.1.13, “HOSTC—Host Configuration Register (SMBUS—D31:F3)” on page 12-403
AC’97 Audio Controller (D31:F5)		
Vendor Identification	00–01h	Section 13.1.1, “VID—Vendor Identification Register (Audio—D31:F5)” on page 13-413
Device Identification	02–03h	Section 13.1.2, “DID—Device Identification Register (Audio—D31:F5)” on page 13-414
PCI Command	04–05h	Section 13.1.3, “PCICMD—PCI Command Register (Audio—D31:F5)” on page 13-414
PCI Device Status	06–07h	Section 13.1.4, “PCISTS—PCI Device Status Register (Audio—D31:F5)” on page 13-415
Revision Identification	08h	Section 13.1.5, “RID—Revision Identification Register (Audio—D31:F5)” on page 13-415
Programming Interface	09h	Section 13.1.6, “PI—Programming Interface Register (Audio—D31:F5)” on page 13-415
Sub Class Code	0Ah	Section 13.1.7, “SCC—Sub Class Code Register (Audio—D31:F5)” on page 13-416
Base Class Code	0Bh	Section 13.1.8, “BCC—Base Class Code Register (Audio—D31:F5)” on page 13-416
Header Type	0Eh	Section 13.1.9, “HEDT—Header Type Register (Audio—D31:F5)” on page 13-416
Native Audio Mixer Base Address	10–13h	Section 13.1.10, “NAMBAR—Native Audio Mixer Base Address Register (Audio—D31:F5)” on page 13-417
Native Audio Bus Mastering Base Address	14–17h	Section 13.1.11, “NABMBAR—Native Audio Bus Mastering Base Address Register (Audio—D31:F5)” on page 13-417
Subsystem Vendor ID	2C–2Dh	Section 13.1.12, “SVID—Subsystem Vendor ID Register (Audio—D31:F5)” on page 13-418
Subsystem ID	2E–2Fh	Section 13.1.13, “SID—Subsystem ID Register (Audio—D31:F5)” on page 13-418
Interrupt Line	3Ch	Section 13.1.14, “INTR_LN—Interrupt Line Register (Audio—D31:F5)” on page 13-418

Table A-1. Intel® ICH3 PCI Configuration Registers (Continued)

Register Name	Offset	Datasheet Section and Location
AC'97 Modem Controller (D31:F6)		
Vendor Identification	00–01h	Section 14.1.1, "VID—Vendor Identification Register (Modem—D31:F6)" on page 14-431
Device Identification	02–03h	Section 14.1.2, "DID—Device Identification Register (Modem—D31:F6)" on page 14-432
PCI Command	04–05h	Section 14.1.3, "PCICMD—PCI Command Register (Modem—D31:F6)" on page 14-432
PCI Device Status	06–07h	Section 14.1.4, "PCISTA—Device Status Register (Modem—D31:F6)" on page 14-433
Revision Identification	08h	Section 14.1.5, "RID—Revision Identification Register (Modem—D31:F6)" on page 14-433
Programming Interface	09h	Section 14.1.6, "PI—Programming Interface Register (Modem—D31:F6)" on page 14-433
Sub Class Code	0Ah	Section 14.1.7, "SCC—Sub Class Code Register (Modem—D31:F6)" on page 14-434
Base Class Code	0Bh	Section 14.1.8, "BCC—Base Class Code Register (Modem—D31:F6)" on page 14-434
Header Type	0Eh	Section 14.1.9, "HEDT—Header Type Register (Modem—D31:F6)" on page 14-434
Modem Mixer Base Address	10–13h	Section 14.1.10, "MMBAR—Modem Mixer Base Address Register (Modem—D31:F6)" on page 14-435
Modem Base Address	14–17h	Section 14.1.11, "MBAR—Modem Base Address Register (Modem—D31:F6)" on page 14-435
Subsystem Vendor ID	2C–2Dh	Section 14.1.12, "SVID—Subsystem Vendor ID (Modem—D31:F6)" on page 14-436
Subsystem ID	2E–2Fh	Section 14.1.13, "SID—Subsystem ID (Modem—D31:F6)" on page 14-436
Interrupt Line	3C	Section 14.1.14, "INTR_LN—Interrupt Line Register (Modem—D31:F6)" on page 14-436
Interrupt Pin	3Dh	Section 14.1.15, "INT_PIN—Interrupt Pin (Modem—D31:F6)" on page 14-436

Table A-2. Intel® ICH3 Fixed I/O Registers

Register Name	Port	Datasheet Section and Location
Channel 0 DMA Base & Current Address Register	00h	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Channel 0 DMA Base & Current Count Register	01h	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Channel 1 DMA Base & Current Address Register	02h	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Channel 1 DMA Base & Current Count Register	03h	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Channel 2 DMA Base & Current Address Register	04h	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Channel 2 DMA Base & Current Count Register	05h	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Channel 3 DMA Base & Current Address Register	06h	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Channel 3 DMA Base & Current Count Register	07h	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Channel 0–3 DMA Command Register Channel 0–3 DMA Status Register	08h	Section 9.2.4, “DMACMD—DMA Command Register” on page 9-301 Section 9.2.5, “DMASTA—DMA Status Register” on page 9-301
Channel 0–3 DMA Write Single Mask Register	0Ah	Section 9.2.6, “DMA_WRSMSK—DMA Write Single Mask Register” on page 9-302
Channel 0–3 DMA Channel Mode Register	0Bh	Section 9.2.7, “DMACH_MODE—DMA Channel Mode Register” on page 9-302
Channel 0–3 DMA Clear Byte Pointer Register	0Ch	Section 9.2.8, “DMA Clear Byte Pointer Register” on page 9-303
Channel 0–3 DMA Master Clear Register	0Dh	Section 9.2.9, “DMA Master Clear Register” on page 9-303
Channel 0–3 DMA Clear Mask Register	0Eh	Section 9.2.10, “DMA_CLMSK—DMA Clear Mask Register” on page 9-303
Channel 0–3 DMA Write All Mask Register	0Fh	Section 9.2.11, “DMA_WRMSK—DMA Write All Mask Register” on page 9-304
Aliased at 00–0Fh	10–1Fh	
Master PIC ICW1 Init. Cmd Word 1 Register Master PIC OCW2 Op Ctrl Word 2 Register Master PIC OCW3 Op Ctrl Word 3 Register	20h	Section 9.4.2, “ICW1—Initialization Command Word 1 Register” on page 9-309 Section 9.4.8, “OCW2—Operational Control Word 2 Register” on page 9-312 Section 9.4.9, “OCW3—Operational Control Word 3 Register” on page 9-313
Master PIC ICW2 Init. Cmd Word 2 Register Master PIC ICW3 Init. Cmd Word 3 Register Master PIC ICW4 Init. Cmd Word 4 Register Master PIC OCW1 Op Ctrl Word 1 Register	21h	Section 9.4.3, “ICW2—Initialization Command Word 2 Register” on page 9-310 Section 9.4.4, “ICW3—Master Controller Initialization Command Word 3 Register” on page 9-310 Section 9.4.6, “ICW4—Initialization Command Word 4 Register” on page 9-311 Section 9.4.7, “OCW1—Operational Control Word 1 (Interrupt Mask) Register” on page 9-311

Table A-2. Intel® ICH3 Fixed I/O Registers (Continued)

Register Name	Port	Datasheet Section and Location
Aliased at 20–21h	24–25h	
Aliased at 20–21h	28–29h	
Aliased at 20–21h	24–25h	
Aliased at 20–21h	2C–2Dh	
Aliased at 20–21h	30–31h	
Aliased at 20–21h	34–35h	
Aliased at 20–21h	38–39h	
Aliased at 20–21h	3C–3Dh	
Counter 0 Interval Time Status Byte Format Counter 0 Counter Access Port Register	40h	Section 9.3.2, “SBYTE_FMT—Interval Timer Status Byte Format Register” on page 9-307 Section 9.3.3, “Counter Access Ports Register” on page 9-307
Counter 1 Interval Time Status Byte Format Counter 1 Counter Access Port Register	41h	Section 9.3.2, “SBYTE_FMT—Interval Timer Status Byte Format Register” on page 9-307 Section 9.3.3, “Counter Access Ports Register” on page 9-307
Counter 2 Interval Time Status Byte Format Counter 2 Counter Access Port Register	42h	Section 9.3.2, “SBYTE_FMT—Interval Timer Status Byte Format Register” on page 9-307 Section 9.3.3, “Counter Access Ports Register” on page 9-307
Timer Control Word Register Timer Control Word Register Read Back Counter Latch Command	43h	Section 9.3.1, “TCW—Timer Control Word Register” on page 9-305 Section 9.3.1.1, “RDBK_CMD—Read Back Command” on page 9-306 Section 9.3.1.2, “LTCH_CMD—Counter Latch Command” on page 9-306
Aliased at 40–43h	50–53h	
NMI Status and Control Register	61h	Section 9.7.1, “NMI_SC—NMI Status and Control Register” on page 9-327
NMI Enable Register	70h	Section 9.7.2, “NMI_EN—NMI Enable (and Real Time Clock Index) Register” on page 9-328
Real-Time Clock (Standard RAM) Index Register	70h	Table 9-7 “RTC (Standard) RAM Bank” on page 9-323 Section 9.7.2, “NMI_EN—NMI Enable (and Real Time Clock Index) Register” on page 9-328
Real-Time Clock (Standard RAM) Target Register	71h	Table 9-7 “RTC (Standard) RAM Bank” on page 9-323
Extended RAM Index Register	72h	
Extended RAM Target Register	73h	
Aliased at 70–71h	74–75h	Aliased if U128E bit in RTC Configuration Register is enalbed Section 9.1.24, “RTC_CONF—RTC Configuration Register (LPC I/F—D31:F0)” on page 9-289
Aliased at 72–73h or 70–71h	76–77h	Aliased to 70–71h if U128E bit in RTC Configuration Register is enalbed Section 9.1.24, “RTC_CONF—RTC Configuration Register (LPC I/F—D31:F0)” on page 9-289

Table A-2. Intel® ICH3 Fixed I/O Registers (Continued)

Register Name	Port	Datasheet Section and Location
Channel 2 DMA Memory Low Page Register	81h	Section 9.2.3, “DMAMEM_LP—DMA Memory Low Page Registers” on page 9-300
Channel 3 DMA Memory Low Page Register	82h	Section 9.2.3, “DMAMEM_LP—DMA Memory Low Page Registers” on page 9-300
Channel 1 DMA Memory Low Page Register	83h	Section 9.2.3, “DMAMEM_LP—DMA Memory Low Page Registers” on page 9-300
Reserved Page Registers	84–86h	
Channel 0 DMA Memory Low Page Register	87h	Section 9.2.3, “DMAMEM_LP—DMA Memory Low Page Registers” on page 9-300
Reserved Page Register	88h	
Channel 6 DMA Memory Low Page Register	89h	Section 9.2.3, “DMAMEM_LP—DMA Memory Low Page Registers” on page 9-300
Channel 7 DMA Memory Low Page Register	8Ah	Section 9.2.3, “DMAMEM_LP—DMA Memory Low Page Registers” on page 9-300
Channel 5 DMA Memory Low Page Register	8Bh	Section 9.2.3, “DMAMEM_LP—DMA Memory Low Page Registers” on page 9-300
Reserved Page Registers	8C–8Eh	
Refresh Low Page Register	8Fh	
Aliased at 81–8Fh	91–9Fh (except 92h)	
Fast A20 and INIT Register	92h	Section 9.7.3, “PORT92—Fast A20 and Init Register” on page 9-328
Slave PIC ICW1 Init. Cmd Word 1 Register Slave PIC OCW2 Op Ctrl Word 2 Register Slave PIC OCW3 Op Ctrl Word 3 Register	A0h	Section 9.4.2, “ICW1—Initialization Command Word 1 Register” on page 9-309 Section 9.4.8, “OCW2—Operational Control Word 2 Register” on page 9-312 Section 9.4.9, “OCW3—Operational Control Word 3 Register” on page 9-313
Slave PIC ICW2 Init. Cmd Word 2 Register Slave PIC ICW3 Init. Cmd Word 3 Register Slave PIC ICW4 Init. Cmd Word 4 Register Slave PIC OCW1 Op Ctrl Word 1 Register	A1	Section 9.4.3, “ICW2—Initialization Command Word 2 Register” on page 9-310 Section 9.4.4, “ICW3—Master Controller Initialization Command Word 3 Register” on page 9-310 Section 9.4.6, “ICW4—Initialization Command Word 4 Register” on page 9-311 Section 9.4.7, “OCW1—Operational Control Word 1 (Interrupt Mask) Register” on page 9-311
Aliased at A0–A1h	A4–A5h	
Aliased at A0–A1h	A8–A9h	
Aliased at A0–A1h	AC–ADh	
Aliased at A0–A1h	B0–B1h	
Advanced Power Management Control Port Register	B2h	Section 9.8.2.1, “APM_CNT—Advanced Power Management Control Port Register” on page 9-335
Advanced Power Management Status Port Register	B3h	Section 9.8.2.2, “APM_STS—Advanced Power Management Status Port Register” on page 9-335
Aliased at A0–A1h	B4–B5h	
Aliased at A0–A1h	B8–B9h	
Aliased at A0–A1h	BC–BDh	

Table A-2. Intel® ICH3 Fixed I/O Registers (Continued)

Register Name	Port	Datasheet Section and Location
Channel 4 DMA Base & Current Address Register	C0h	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Aliased at C0h	C1h	
Channel 4 DMA Base & Current Count Register	C2h	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Aliased at C2h	C3h	
Channel 5 DMA Base & Current Address Register	C4h	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Aliased at C4h	C5h	
Channel 5 DMA Base & Current Count Register	C6h	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Aliased at C6h	C7h	
Channel 6 DMA Base & Current Address Register	C8h	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Aliased at C8h	C9h	
Channel 6 DMA Base & Current Count Register	CAh	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Aliased at CAh	CBh	
Channel 7 DMA Base & Current Address Register	CCh	Section 9.2.1, “DMABASE_CA—DMA Base and Current Address Registers” on page 9-299
Aliased at CCh	CDh	
Channel 7 DMA Base & Current Count Register	CEh	Section 9.2.2, “DMABASE_CC—DMA Base and Current Count Registers” on page 9-300
Aliased at CEh	CFh	
Channel 4–7 DMA Command Register Channel 4–7 DMA Status Register	D0h	Section 9.2.4, “DMACMD—DMA Command Register” on page 9-301 Section 9.2.5, “DMASTA—DMA Status Register” on page 9-301
Aliased at D0h	D1h	
Channel 4–7 DMA Write Single Mask Register	D4h	Section 9.2.6, “DMA_WRSMSK—DMA Write Single Mask Register” on page 9-302
Aliased at D4h	D5h	
Channel 4–7 DMA Channel Mode Register	D6h	Section 9.2.7, “DMACH_MODE—DMA Channel Mode Register” on page 9-302
Aliased at D6h	D7h	
Channel 4–7 DMA Clear Byte Pointer Register	D8h	Section 9.2.8, “DMA Clear Byte Pointer Register” on page 9-303
Aliased at D8h	D9h	
Channel 4–7 DMA Master Clear Register	DAh	Section 9.2.9, “DMA Master Clear Register” on page 9-303
Aliased at DAh	DBh	
Channel 4–7 DMA Clear Mask Register	DCh	Section 9.2.10, “DMA_CLMSK—DMA Clear Mask Register” on page 9-303
Aliased at DCh	DEh	

Table A-2. Intel® ICH3 Fixed I/O Registers (Continued)

Register Name	Port	Datasheet Section and Location
Channel 4–7 DMA Write All Mask Register	DEh	Section 9.2.11, “DMA_WRMSK—DMA Write All Mask Register” on page 9-304
Aliased at DEh	DFh	
Coprocessor Error Reigster	F0h	Section 9.7.4, “COPROC_ERR—Coprocessor Error Register” on page 9-328
PIO Mode Command Block Offset for Secondary Drive	170–177h	See ATA Specification for detailed register description
PIO Mode Command Block Offset for Primary Drive	1F0–1F7h	See ATA Specification for detailed register description
PIO Mode Control Block Offset for Secondary Drive	376h	See ATA Specification for detailed register description
PIO Mode Control Block Offset for Primary Drive	3F6h	See ATA Specification for detailed register description
Master PIC Edge/Level Triggered Register	4D0h	Section 9.4.10, “ELCR1—Master Controller Edge/Level Triggered Register” on page 9-314
Slave PIC Edge/Level Triggered Register	4D1h	Section 9.4.11, “ELCR2—Slave Controller Edge/Level Triggered Register” on page 9-315
Reset Control Register	CF9h	Section 9.7.5, “RST_CNT—Reset Control Register” on page 9-329

NOTE: When the POS_DEC_EN bit is set, additional I/O ports get positively decoded by the ICH3.

Table A-3. Intel® ICH3 Variable I/O Registers

Register Name	Offset	Datasheet Section and Location
LAN Control/Status Registers (CSR) may be mapped to either I/O space or memory space. LAN CSR at CSR_IO_BASE + Offset or CSR_MEM_BASE + Offset. CSR_MEM_BASE set in Section 7.1.11, "CSR_MEM_BASE CSR—Memory-Mapped Base Address Register (LAN Controller—B1:D8:F0)" on page 7-239 CSR_IO_BASE set in Section 7.1.12, "CSR_IO_BASE—CSR I/O-Mapped Base Address Register (LAN Controller—B1:D8:F0)" on page 7-239		
SCB Status Word	01–00h	Section 7.2.1, "System Control Block Status Word Register" on page 7-246
SCB Command Word	03–02h	Section 7.2.2, "System Control Block Command Word Register" on page 7-247
SCB General Pointer	07–04h	Section 7.2.3, "System Control Block General Pointer Register" on page 7-249
PORT	OB–08h	Section 7.2.4, "PORT" on page 7-249
EEPROM Control Register	0F–0Eh	Section 7.2.5, "EEPROM Control Register" on page 7-250
MDI Control Register	13–10h	Section 7.2.6, "Management Data Interface (MDI) Control Register" on page 7-251
Receive DMA Byte Count	17–14h	Section 7.2.7, "Receive DMA Byte Count Register" on page 7-251
Early Receive Interrupt	18h	Section 7.2.8, "Early Receive Interrupt Register" on page 7-252
Flow Control Register	1A–19h	Section 7.2.9, "Flow Control Register" on page 7-253
PMDR	1Bh	Section 7.2.10, "Power Management Driver (PMDR) Register" on page 7-254
General Control	1Ch	Section 7.2.11, "General Control Register" on page 7-254
General Status	1Dh	Section 7.2.12, "General Status Register" on page 7-255
Power Management I/O Registers at PMBASE+Offset PMBASE set in **Section 9.1.10, "PMBASE—ACPI Base Address Register (LPC I/F—D31:F0)" on page 9-280**		
PM1 Status	00–01h	Section 9.8.3.1, "PM1_STS—Power Management 1 Status Register" on page 9-337
PM1 Enable	02–03h	Section 9.8.3.2, "PM1_EN—Power Management 1 Enable Register" on page 9-339
PM1 Control	04–07h	Section 9.8.3.3, "PM1_CNT—Power Management 1 Control Register" on page 9-340
PM1 Timer	08–0Bh	Section 9.8.3.4, "PM1_TMR—Power Management 1 Timer Register" on page 9-340
Processor Control	10–13h	Section 9.8.3.5, "PROC_CNT—Processor Control Register" on page 9-341
Level 2 Register	14h	Section 9.8.3.6, "LV2—Level 2 Register" on page 9-342
General Purpose Event 0 Status	28–29h	Section 9.8.3.7, "GPE0_STS—General Purpose Event 0 Status Register" on page 9-342
General Purpose Event 0 Enables	2A–2Bh	Section 9.8.3.8, "GPE0_EN—General Purpose Event 0 Enables Register" on page 9-344

Table A-3. Intel® ICH3 Variable I/O Registers (Continued)

Register Name	Offset	Datasheet Section and Location
General Purpose Event 1 Status	2C–2D	Section 9.8.3.9, “GPE1_STS—General Purpose Event 1 Status Register” on page 9-345
General Purpose Event 1 Enables	2E–2F	Section 9.8.3.10, “GPE1_EN—General Purpose Event 1 Enable Register” on page 9-345
SMI# Control and Enable	30–31h	Section 9.8.3.11, “SMI_EN—SMI Control and Enable Register” on page 9-346
SMI Status Register	34–35h	Section 9.8.3.12, “SMI_STS—SMI Status Register” on page 9-347
Monitor SMI Status	40h	Section 9.8.3.13, “MON_SMI—Device Monitor SMI Status and Enable Register” on page 9-348
Device Activity Status	44h	Section 9.8.3.14, “DEVACT_STS—Device Activity Status Register” on page 9-349
Device Trap Enable	48h	Section 9.8.3.15, “DEVTRAP_EN— Device Trap Enable Register” on page 9-350
Bus Address Tracker	4Ch	Section 9.8.3.16, “BUS_ADDR_TRACK— Bus Address Tracker Register” on page 9-351
Bus Cycle Tracker	4Eh	Section 9.8.3.17, “BUS_CYC_TRACK— Bus Cycle Tracker Register” on page 9-351
TCO I/O Registers at TCOBASE + Offset TCOBASE = PMBASE + 40h PMBASE is set in **Section 9.1.10, “PMBASE—ACPI Base Address Register (LPC I/F—D31:F0)” on page 9-280**		
TCO_RLD: TCO Timer Reload and Current Value	00h	Section 9.9.2, “TCO1_RLD—TCO Timer Reload and Current Value Register” on page 9-352
TCO_TMR: TCO Timer Initial Value	01h	Section 9.9.3, “TCO1_TMR—TCO Timer Initial Value Register” on page 9-353
TCO_DAT_IN: TCO Data In	02h	Section 9.9.4, “TCO1_DAT_IN—TCO Data In Register” on page 9-353
TCO_DAT_OUT: TCO Data Out	03h	Section 9.9.5, “TCO1_DAT_OUT—TCO Data Out Register” on page 9-353
TCO1_STS : TCO Status	04–05h	Section 9.9.6, “TCO1_STS—TCO1 Status Register” on page 9-354
TCO2_STS : TCO Status	06–07h	Section 9.9.7, “TCO2_STS—TCO2 Status Register” on page 9-355
TCO1_CNT: TCO Control	08–09h	Section 9.9.8, “TCO1_CNT—TCO1 Control Register” on page 9-356
TCO2_CNT: TCO Control	0A–0Bh	Section 9.9.9, “TCO2_CNT—TCO2 Control Register” on page 9-356

Table A-3. Intel® ICH3 Variable I/O Registers (Continued)

Register Name	Offset	Datasheet Section and Location
GPIO I/O Registers at GPIOBASE + Offset GPIOBASE is set in **Section 9.1.14, "GPIOBASE—GPIO Base Address Register (LPC I/F—D31:F0)" on page 9-282**		
GPIO Use Select	00–03h	Section 9.10.2, "GPIO_USE_SEL—GPIO Use Select Register" on page 9-360
GPIO Input/Output Select	04–07h	Section 9.10.3, "GP_IO_SEL—GPIO Input/Output Select Register" on page 9-361
GPIO Level for Input or Output	0C–0Fh	Section 9.10.4, "GP_LVL—GPIO Level for Input or Output Register" on page 9-361
GPIO Blink Enable	18–1Bh	Section 9.10.5, "GPO_BLINK—GPO Blink Enable Register" on page 9-362
GPIO Signal Invert	2C–2Fh	Section 9.10.6, "GPI_INV—GPIO Signal Invert Register" on page 9-362
BMIDE I/O Registers at BM_BASE + Offset BM_BASE is set at **Section 10.1.12, "SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1)" on page 10-369**		
Command Register Primary	00h	Section 10.2.1, "BMIC[P,S]—Bus Master IDE Command Register" on page 10-378
Status Register Primary	02h	Section 10.2.2, "BMIS[P,S]—Bus Master IDE Status Register" on page 10-379
Descriptor Table Pointer Primary	04–07h	Section 10.2.3, "BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register" on page 10-379
Command Register Secondary	08h	Section 10.2.1, "BMIC[P,S]—Bus Master IDE Command Register" on page 10-378
Status Register Secondary	0Ah	Section 10.2.2, "BMIS[P,S]—Bus Master IDE Status Register" on page 10-379
Descriptor Table Pointer Secondary	0C–0Fh	Section 10.2.3, "BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register" on page 10-379
USB I/O Registers at Base Address + Offset **USB Base Address is set at Section 11.1.10, "BASE—Base Address Register (USB—D29:F0/F1/F2)" on page 11-385**		
USB Command Register	00–01h	Section 11.2.1, "USBCMD—USB Command Register" on page 11-390
USB Status Register	02–03h	Section 11.2.2, "USBSTA—USB Status Register" on page 11-393
USB Interrupt Enable	04–05h	Section 11.2.3, "USBINTR—Interrupt Enable Register" on page 11-394
USB Frame Number	06–07h	Section 11.2.4, "FRNUM—Frame Number Register" on page 11-394
USB Frame List Base Address	08–0Bh	Section 11.2.5, "FRBASEADD—Frame List Base Address Register" on page 11-395
USB Start of Frame Modify	0Ch	Section 11.2.6, "SOFMOD—Start of Frame Modify Register" on page 11-395
Port 0, 2 Status/Control	10–11h	Section 11.2.7, "PORTSC[0,1]—Port Status and Control Register" on page 11-396
Port 1, 3 Status/Control	12–13h	Section 11.2.7, "PORTSC[0,1]—Port Status and Control Register" on page 11-396
Loop Back Test Data	18h	

Table A-3. Intel® ICH3 Variable I/O Registers (Continued)

Register Name	Offset	Datasheet Section and Location
SMBus I/O Registers at SMB_BASE + Offset SMB_BASE is set at Section 12.1.8, “SMB_BASE—SMBus Base Address Register (SMBUS—D31:F3)” on page 12-401		
Host Status	00h	Section 12.2.1, “HST_STS—Host Status Register” on page 12-405
Host Control	02h	Section 12.2.2, “HST_CNT—Host Control Register” on page 12-406
Host Command	03h	Section 12.2.3, “HST_CMD—Host Command Register” on page 12-407
Transmit Slave Address	04h	Section 12.2.4, “XMIT_SLVA—Transmit Slave Address Register” on page 12-407
Host Data 0	05h	Section 12.2.5, “HST_D0—Data 0 Register” on page 12-407
Host Data 1	06h	Section 12.2.6, “HST_D1—Data 1 Register” on page 12-407
Block Data Byte	07h	Section 12.2.7, “BLOCK_DB—Block Data Byte Register” on page 12-408
Receive Slave Address	09h	Section 12.2.9, “RCV_SLVA—Receive Slave Address Register” on page 12-408
Receive Slave Data	0Ah	Section 12.2.10, “SLV_DATA—Receive Slave Data Register” on page 12-409
AC’97 Audio I/O Registers at NAMBAR + Offset **NAMBAR is set at Section 13.1.11, “NABMBAR—Native Audio Bus Mastering Base Address Register (Audio—D31:F5)” on page 13-417**		
PCM In Buffer Descriptor list Base Address Register	00h	Section 13.2.1, “x_BDBAR—Buffer Descriptor Base Address Register” on page 13-422
PCM In Current Index Value	04h	Section 13.2.2, “x_CIV—Current Index Value Register” on page 13-423
PCM In Last Valid Index	05h	Section 13.2.3, “x_LVI—Last Valid Index Register” on page 13-423
PCM In Status Register	06h	Section 13.2.4, “x_SR—Status Register” on page 13-424
PCM In Position In Current Buffer	08h	Section 13.2.5, “x_PICB—Position In Current Buffer Register” on page 13-425
PCM In Prefetched Index Value	0Ah	Section 13.2.6, “x_PIV—Prefetched Index Value Register” on page 13-425
PCM In Control Register	0Bh	Section 13.2.7, “x_CR—Control Register” on page 13-426
PCM Out Buffer Descriptor list Base Address Register	10h	Section 13.2.1, “x_BDBAR—Buffer Descriptor Base Address Register” on page 13-422
PCM Out Current Index Value	14h	Section 13.2.2, “x_CIV—Current Index Value Register” on page 13-423
PCM Out Last Valid Index	15h	Section 13.2.3, “x_LVI—Last Valid Index Register” on page 13-423
PCM Out Status Register	16h	Section 13.2.4, “x_SR—Status Register” on page 13-424
PCM Out Position In Current Buffer	18h	Section 13.2.5, “x_PICB—Position In Current Buffer Register” on page 13-425

Table A-3. Intel® ICH3 Variable I/O Registers (Continued)

Register Name	Offset	Datasheet Section and Location
PCM Out Prefetched Index Value	1Ah	Section 13.2.6, “x_PIV—Prefetched Index Value Register” on page 13-425
PCM Out Control Register	1Bh	Section 13.2.7, “x_CR—Control Register” on page 13-426
Mic. In Buffer Descriptor list Base Address Register	20h	Section 13.2.1, “x_BDBAR—Buffer Descriptor Base Address Register” on page 13-422
Mic. In Current Index Value	24h	Section 13.2.2, “x_CIV—Current Index Value Register” on page 13-423
Mic. In Last Valid Index	25h	Section 13.2.3, “x_LVI—Last Valid Index Register” on page 13-423
Mic. In Status Register	26h	Section 13.2.4, “x_SR—Status Register” on page 13-424
Mic In Position In Current Buffer	28h	Section 13.2.5, “x_PICB—Position In Current Buffer Register” on page 13-425
Mic. In Prefetched Index Value	2Ah	Section 13.2.6, “x_PIV—Prefetched Index Value Register” on page 13-425
Mic. In Control Register	2Bh	Section 13.2.7, “x_CR—Control Register” on page 13-426
Global Control	2Ch	Section 13.2.8, “GLOB_CNT—Global Control Register” on page 13-427
Global Status	30h	Section 13.2.9, “GLOB_STA—Global Status Register” on page 13-428
Codec Access Semaphore Register	34h	Section 13.2.10, “CAS—Codec Access Semaphore Register” on page 13-429
AC’97 Modem I/O Registers at MBAR + Offset MBAR is set in Section 14.1.11, “MBAR—Modem Base Address Register (Modem—D31:F6)” on page 14-435		
Modem In Buffer Descriptor List Base Address Register	00h	Section 14.2.1, “x_BDBAR—Buffer Descriptor List Base Address Register” on page 14-439
Modem In Current Index Value Register	04h	Section 14.2.2, “x_CIV—Current Index Value Register” on page 14-439
Modem In Last Valid Index Register	05h	Section 14.2.3, “x_LVI—Last Valid Index Register” on page 14-439
Modem In Status Register	06h	Section 14.2.4, “x_SR—Status Register” on page 14-440
Modem In Position In Current Buffer Register	08h	Section 14.2.5, “x_PICB—Position In Current Buffer Register” on page 14-441
Modem In Prefetch Index Value Register	0Ah	Section 14.2.6, “x_PIV—Prefetch Index Value Register” on page 14-441
Modem In Control Register	0Bh	Section 14.2.7, “x_CR—Control Register” on page 14-442
Modem Out Buffer Descriptor List Base Address Register	10h	Section 14.2.1, “x_BDBAR—Buffer Descriptor List Base Address Register” on page 14-439
Modem Out Current Index Value Register	14h	Section 14.2.2, “x_CIV—Current Index Value Register” on page 14-439
Modem Out Last Valid Register	15h	Section 14.2.3, “x_LVI—Last Valid Index Register” on page 14-439

Table A-3. Intel® ICH3 Variable I/O Registers (Continued)

Register Name	Offset	Datasheet Section and Location
Modem Out Status Register	16h	Section 14.2.4, “x_SR—Status Register” on page 14-440
Modem In Position In Current Buffer Register	18h	Section 14.2.5, “x_PICB—Position In Current Buffer Register” on page 14-441
Modem Out Prefetched Index Register	1Ah	Section 14.2.6, “x_PIV—Prefetch Index Value Register” on page 14-441
Modem Out Control Register	1Bh	Section 14.2.7, “x_CR—Control Register” on page 14-442
Global Control	3Ch	Section 14.2.8, “GLOB_CNT—Global Control Register” on page 14-443
Global Status	40h	Section 14.2.9, “GLOB_STA—Global Status Register” on page 14-444
Codec Access Semaphore Register	44h	Section 14.2.10, “CAS—Codec Access Semaphore Register” on page 14-445

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