National Semiconductor

ADVANCE INFORMATION
September 2007

ADC12DC080/ADC12DC105 Dual 12-Bit, 80/105 MSPS A/D Converter with CMOS Outputs

General Description

NOTE: This is Advance Information for products currently in development. ALL specifications are design targets and are subject to change.

The ADC12DC080 and ADC12DC105 are high-performance CMOS analog-to-digital converters capable of converting two analog input signals into 12-bit digital words at rates up to 80/105 Mega Samples Per Second (MSPS) respectively. These converters use a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1 GHz. The ADC12DC080/105 may be operated from a single +3.3V power supply. A power-down feature reduces the power consumption to very low levels while still allowing fast wake-up time to full operation. The differential inputs provide a 2V full scale differential input swing. A stable 1.2V internal voltage reference is provided, or the ADC12DC080/105 can be operated with an external 1.2V reference. Output data format (offset binary versus 2's complement) and duty cycle stabilizer are pin-selectable. The duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

The ADC12DC080/105 is available in a 60-lead LLP package and operates over the industrial temperature range of −40°C to +85°C.

Features

- 1 GHz Full Power Bandwidth
- Internal sample-and-hold circuit and precision reference
- Low power consumption
- Clock Duty Cycle Stabilizer
- Single +3.3V supply operation
- Power-down mode
- Offset binary or 2's complement output data format
- 60-pin LLP package, (9x9x0.8mm, 0.5mm pin-pitch)

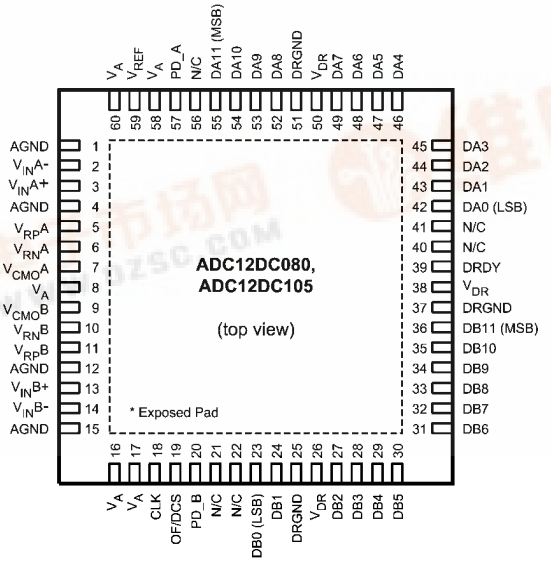
Key Specifications

- **For ADC12DC105**
- Resolution — 12 Bits
- Conversion Rate — 105 MSPS
- SNR (f_{IN} = 240 MHz) — 67 dBFS (typ)
- SFDR (f_{IN} = 240 MHz) — 83 dBFS (typ)
- Full Power Bandwidth — 1 GHz (typ)
- Power Consumption — 800 mW (typ)

Applications

- High IF Sampling Receivers
- Wireless Base Station Receivers
- Test and Measurement Equipment
- Communications Instrumentation
- Portable Instrumentation

Connection Diagram



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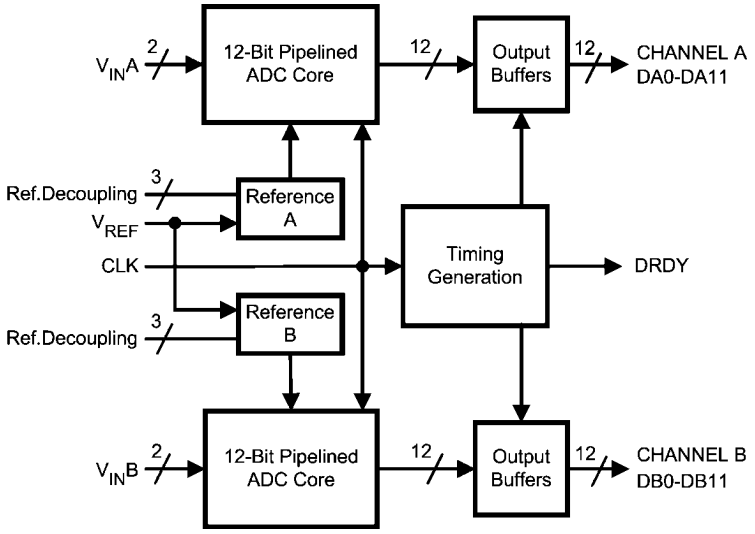
Block Diagram



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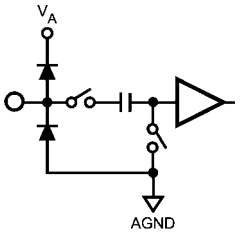
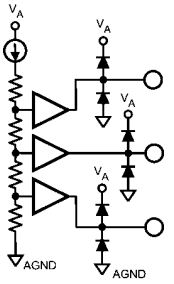
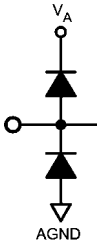
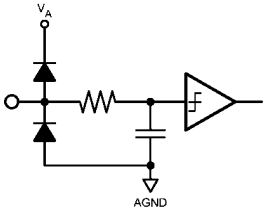
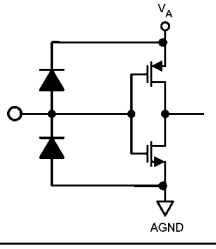
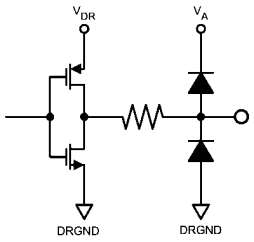
Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC12DC080CISQ	60 Pin LLP
ADC12DC105CISQ	60 Pin LLP

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
3 13	$V_{IN}A+$ $V_{IN}B+$		Differential analog input pins. The differential full-scale input signal level is $2V_{P-P}$ with each input pin signal centered on a common mode voltage, V_{CM}.
2 14	$V_{IN}A-$ $V_{IN}B-$		
5 11	$V_{RP}A$ $V_{RP}B$		These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. An 0201 size 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible, and a 1 µF capacitor should be placed in parallel. V_{RP} and V_{RN} should not be loaded. V_{CMO} may be loaded to 1mA for use as a temperature stable 1.5V reference. It is recommended to use V_{CMO} to provide the common mode voltage, V_{CM}, for the differential analog inputs.
7 9	$V_{CMO}A$ $V_{CMO}B$		
6 10	$V_{RN}A$ $V_{RN}B$		
59	V_{REF}		Reference Voltage. This device provides an internally developed 1.2V reference. When using the internal reference, V_{REF} should be decoupled to AGND with a 0.1 µF and a 1µF, low equivalent series inductance (ESL) capacitor. This pin may be driven with an external 1.2V reference voltage. This pin should not be used to source or sink current.
DIGITAL I/O			
19	OF/DCS		This is a four-state pin controlling the input clock mode and output data format. OF/DCS = V_A, output data format is 2's complement without duty cycle stabilization applied to the input clock OF/DCS = AGND, output data format is offset binary, without duty cycle stabilization applied to the input clock. OF/DCS = (2/3)*V_A, output data is 2's complement with duty cycle stabilization applied to the input clock OF/DCS = (1/3)*V_A, output data is offset binary with duty cycle stabilization applied to the input clock.
18	CLK		The clock input pin. The analog inputs are sampled on the rising edge of the clock input.
57 20	PD_A PD_B		This is a two-state input controlling Power Down. PD = V_A, Power Down is enabled and power dissipation is reduced. PD = AGND, Normal operation.

Pin No.	Symbol	Equivalent Circuit	Description
42-49, 52-55	DA0-DA7, DA8-DA11		Digital data output pins that make up the 12-bit conversion result for Channel A. DA0 (pin 42) is the LSB, while DA11 (pin 55) is the MSB of the output word. Output levels are CMOS compatible.
23-24, 27-36	DB0-DB1, DB3-DB11		Digital data output pins that make up the 12-bit conversion result for Channel B. DB0 (pin 23) is the LSB, while DB11 (pin 36) is the MSB of the output word. Output levels are CMOS compatible.
39	DRDY		Data Ready Strobe. The data output transition is synchronized with the falling edge of this signal. This signal switches at the same frequency as the CLK input.
ANALOG POWER			
8, 16, 17, 58, 60	V_A		Positive analog supply pins. These pins should be connected to a quiet source and be bypassed to AGND with 0.1 µF capacitors located close to the power pins.
1, 4, 12, 15, Exposed Pad	AGND		The ground return for the analog supply.
DIGITAL POWER			
26, 38,50	V_{DR}		Positive driver supply pin for the output drivers. This pin should be connected to a quiet voltage source and be bypassed to DRGND with a 0.1 µF capacitor located close to the power pin.
25, 37, 51	DRGND		The ground return for the digital output driver supply. This pins should be connected to the system digital ground, but not be connected in close proximity to the ADC's AGND pins.

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_{DR})	−0.3V to 4.2V
Voltage on Any Pin (Not to exceed 4.2V)	−0.3V to (V_A +0.3V)
Input Current at Any Pin other than Supply Pins (Note 4)	±5 mA
Package Input Current (Note 4)	±50 mA
Max Junction Temp (T_J)	+150°C
Thermal Resistance (θ_{JA})	30°C/W
ESD Rating	
Human Body Model (Note 6)	2500V
Machine Model (Note 6)	250V
Storage Temperature	−65°C to +150°C

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 7)

Operating Ratings (Notes 1, 3)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A)	+2.7V to +3.6V
Output Driver Supply (V_{DR})	+2.4V to V_A
Clock Duty Cycle	
(DCS Enabled)	30/70 %
(DCS disabled)	45/55 %
V_{CM}	1.4V to 1.6V
|AGND-DRGND|	≤100mV

ADC12DC080 Converter Electrical Characteristics

This product is currently under development. As such, the parameters specified are DESIGN TARGETS. The specifications cannot be guaranteed until device characterization has taken place.

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.0V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for T_{MIN} ≤ T_A ≤ T_{MAX}.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity (Note 11)			±0.5		LSB (max) LSB (min)
DNL	Differential Non Linearity			±0.4		LSB (max) LSB (min)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CMO}	Common Mode Output Voltage			1.5	1.45 1.55	V (min) V (max)
V_{CM}	Analog Input Common Mode Voltage			1.5	1.4 1.6	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND) (Note 12)	V_{IN} = 1.5 Vdc ± 0.5 V	(CLK LOW)	8.5		pF
			(CLK HIGH)	3.5		pF
V_{REF}	External Reference Voltage			1.20	1.176 1.224	V (min) V (max)

ADC12DC080 Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.0V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin, . Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1dBFS					
FPBW	Full Power Bandwidth	-1 dBFS Input, –3 dB Corner	1.0		GHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz	71.2		dBFS
		f_{IN} = 70 MHz	70		dBFS
		f_{IN} = 170 MHz	68		dBFS
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz	90		dBFS
		f_{IN} = 70 MHz	88		dBFS
		f_{IN} = 170 MHz	83		dBFS
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	11.5		Bits
		f_{IN} = 70 MHz	11.3		Bits
		f_{IN} = 170 MHz	11		Bits
THD	Total Harmonic Disortion	f_{IN} = 10 MHz	–88		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 170 MHz	–80		dBFS
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	–100		dBFS
		f_{IN} = 70 MHz	–95		dBFS
		f_{IN} = 170 MHz	–85		dBFS
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	–90		dBFS
		f_{IN} = 70 MHz	–88		dBFS
		f_{IN} = 170 MHz	–83		dBFS
SINAD	Signal-to-Noise and Distortion Ratio	f_{IN} = 10 MHz	71.1		dBFS
		f_{IN} = 70 MHz	69.8		dBFS
		f_{IN} = 170 MHz	67.7		dBFS

ADC12DC080 Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.0V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
DIGITAL INPUT CHARACTERISTICS (CLK, PD_A,PD_B)					
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 3.6V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 3.0V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 3.3V	10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	–10		µA
C_{IN}	Digital Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (DA0-DA11,DB0-DB11,DRDY)					
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = –0.5 mA , V_{DR} = 2.4V		**1.2**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 2.4V		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	–10		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}	10		mA
C_{OUT}	Digital Output Capacitance		5		pF
POWER SUPPLY CHARACTERISTICS					

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
I_A	Analog Supply Current	Full Operation	200		mA (max)
I_{DR}	Digital Output Supply Current	Full Operation (Note 13)	26		mA
	Power Consumption	Excludes I_{DR} (Note 13)	600		mW (max)
	Power Down Power Consumption	PD_A=PD_B=V_A	30		mW

ADC12DC080 Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.0V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 80 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symb	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
	Maximum Clock Frequency			**80**	MHz (max)
	Minimum Clock Frequency			**20**	MHz (min)
t_{CH}	Clock High Time		6		ns
t_{CL}	Clock Low Time		6		ns
t_{CONV}	Conversion Latency			**7**	Clock Cycles
t_{OD}	Output Delay of CLK to DATA	Relative to rising edge of CLK	4	2 6	ns (min) ns (max)
t_{SU}	Data Output Setup Time	Relative to DRDY	5		ns (min)
t_H	Data Output Hold Time	Relative to DRDY	5		ns (min)
t_{AD}	Aperture Delay		0.6		ns
t_{AJ}	Aperture Jitter		0.1		ps rms

ADC12DC105 Converter Electrical Characteristics

This product is currently under development. As such, the parameters specified are DESIGN TARGETS. The specifications cannot be guaranteed until device characterization has taken place.

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity (Note 11)			±0.5		LSB (max) LSB (min)
DNL	Differential Non Linearity			±0.4		LSB (max) LSB (min)
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CMO}	Common Mode Output Voltage			1.5	1.45 1.55	V (min) V (max)
V_{CM}	Analog Input Common Mode Voltage			1.5	1.4 1.6	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 1.5 Vdc	(CLK LOW)	8.5		pF
	(Note 12)	± 0.5 V	(CLK HIGH)	3.5		pF
V_{REF}	External Reference Voltage			1.20	1.176 1.224	V (min) V (max)

ADC12DC105 Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, $V_{CM} = V_{CMO}$, C_L = 5 pF/pin, . Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1dBFS					
FPBW	Full Power Bandwidth	-1 dBFS Input, –3 dB Corner	1.0		GHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz	70.1		dBFS
		f_{IN} = 70 MHz	69.1		dBFS
		f_{IN} = 240 MHz	67		dBFS
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz	88		dBFS
		f_{IN} = 70 MHz	85		dBFS
		f_{IN} = 240 MHz	83		dBFS
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	11.3		Bits
		f_{IN} = 70 MHz	11.2		Bits
		f_{IN} = 240 MHz	10.8		Bits
THD	Total Harmonic Disortion	f_{IN} = 10 MHz	–86		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 240 MHz	–80		dBFS
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	–95		dBFS
		f_{IN} = 70 MHz	–90		dBFS
		f_{IN} = 240 MHz	–85		dBFS

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits) (Note 2)
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	–88		dBFS
		f_{IN} = 70 MHz	–85		dBFS
		f_{IN} = 240 MHz	–83		dBFS
SINAD	Signal-to-Noise and Distortion Ratio	f_{IN} = 10 MHz	70		dBFS
		f_{IN} = 70 MHz	69		dBFS
		f_{IN} = 240 MHz	66.8		dBFS

ADC12DC105 Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
DIGITAL INPUT CHARACTERISTICS (CLK, PD_A,PD_B)					
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 3.6V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 3.0V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 3.3V	10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	–10		µA
C_{IN}	Digital Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (DA0-DA11,DB0-DB11,DRDY)					
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = –0.5 mA , V_{DR} = 2.4V		**1.2**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 2.4V		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V	–10		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}	10		mA
C_{OUT}	Digital Output Capacitance		5		pF
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	Full Operation	242		mA (max)
I_{DR}	Digital Output Supply Current	Full Operation (Note 13)	32		mA
	Power Consumption	Excludes I_{DR} (Note 13)	800		mW (max)
	Power Down Power Consumption	PD_A=PD_B=V_A	33		mW

ADC12DC105 Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DRGND = 0V, V_A = +3.3V, V_{DR} = +2.5V, Internal V_{REF} = +1.2V, f_{CLK} = 105 MHz, V_{CM} = V_{CMO}, C_L = 5 pF/pin. Typical values are for T_A = 25°C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25°C (Notes 8, 9)

Symb	Parameter	Conditions	Typical (Note 10)	Limits	Units (Limits)
	Maximum Clock Frequency			**105**	MHz (max)
	Minimum Clock Frequency			**20**	MHz (min)
t_{CH}	Clock High Time		4		ns
t_{CL}	Clock Low Time		4		ns
t_{CONV}	Conversion Latency			**7**	Clock Cycles
t_{OD}	Output Delay of CLK to DATA	Relative to rising edge of CLK	4	2 6	ns (min) ns (max)
t_{SU}	Data Output Setup Time	Relative to DRDY	3		ns (min)
t_H	Data Output Hold Time	Relative to DRDY	3		ns (min)
t_{AD}	Aperture Delay		0.6		ns
t_{AJ}	Aperture Jitter		0.1		ps rms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: This parameter is specified in units of dBFS - indicating the value that would be attained with a full-scale input signal.

Note 3: All voltages are measured with respect to GND = AGND = DRGND = 0V, unless otherwise specified.

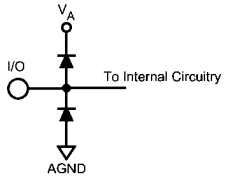
Note 4: When the input voltage at any pin exceeds the power supplies (that is, $V_{IN} < AGND$, or $V_{IN} > V_A$), the current at that pin should be limited to ±5 mA. The ±50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of ±5 mA to 10.

Note 5: The maximum allowable power dissipation is dictated by $T_{J,max}$, the junction-to-ambient thermal resistance, (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_{D,max} = (T_{J,max} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

Note 6: Human Body Model is 100 pF discharged through a 1.5 kΩ resistor. Machine Model is 220 pF discharged through 0 Ω

Note 7: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 8: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 4). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



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Note 9: With a full scale differential input of $2V_{P-P}$, the 12-bit LSB is 488 µV.

Note 10: Typical figures are at T_A = 25°C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 11: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

Note 12: The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

Note 13: I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR}=V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ...C_{11} \times f_{11})$ where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

Note 14: This parameter is guaranteed by design and/or characterization and is not tested in production.

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error
NGE = Offset Error - Negative Full Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a best fit straight line. The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN}-)] required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the falling edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_7^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagrams

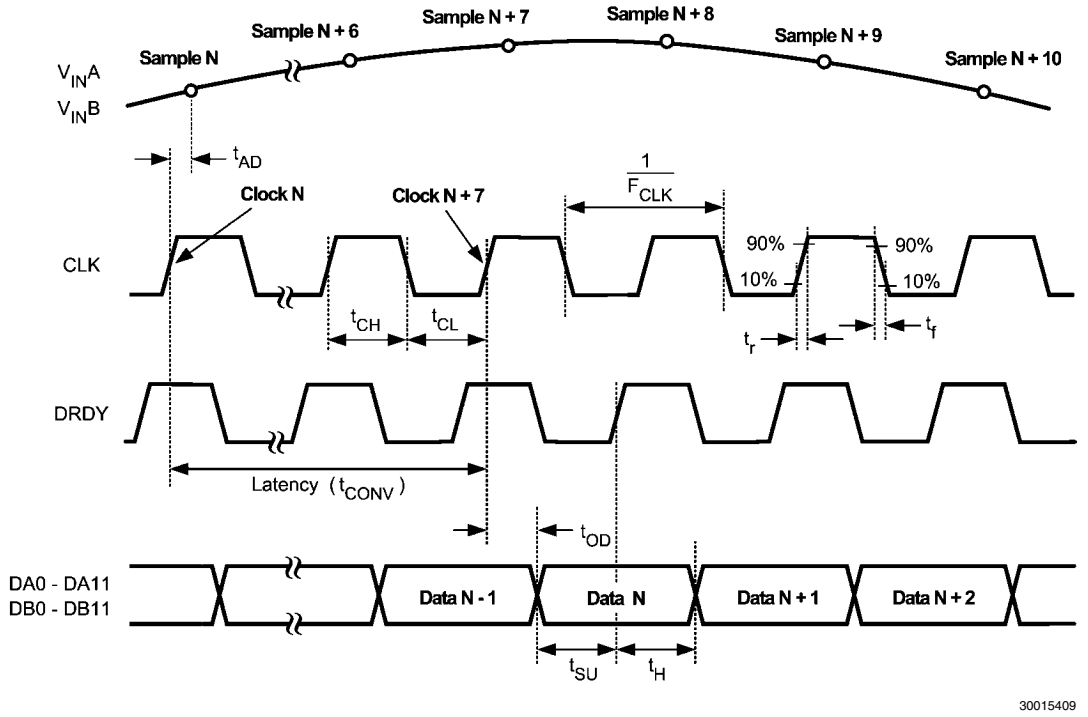


FIGURE 1. Output Timing

Transfer Characteristic

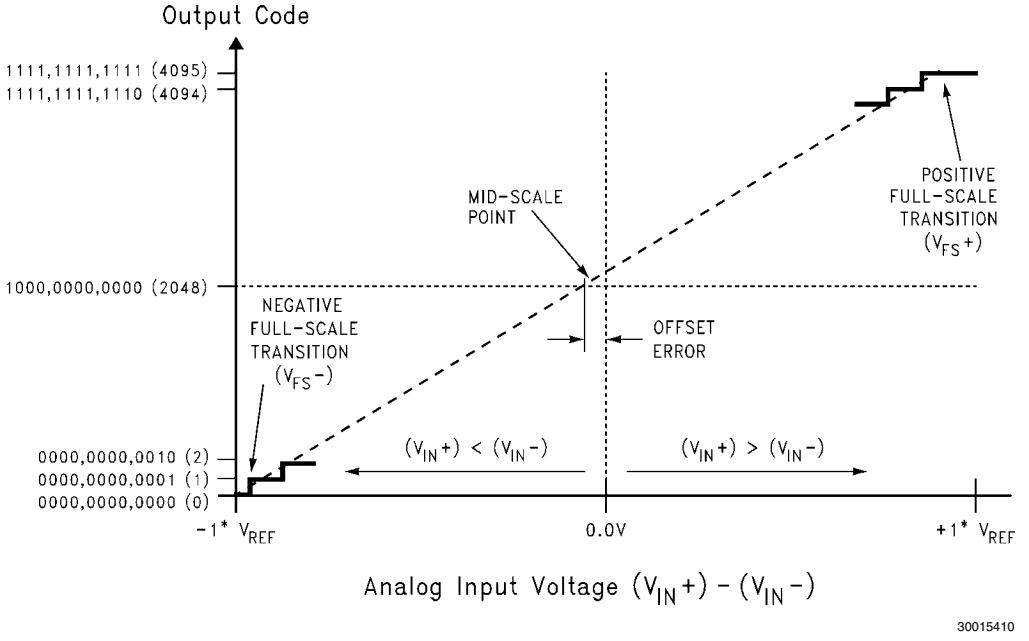
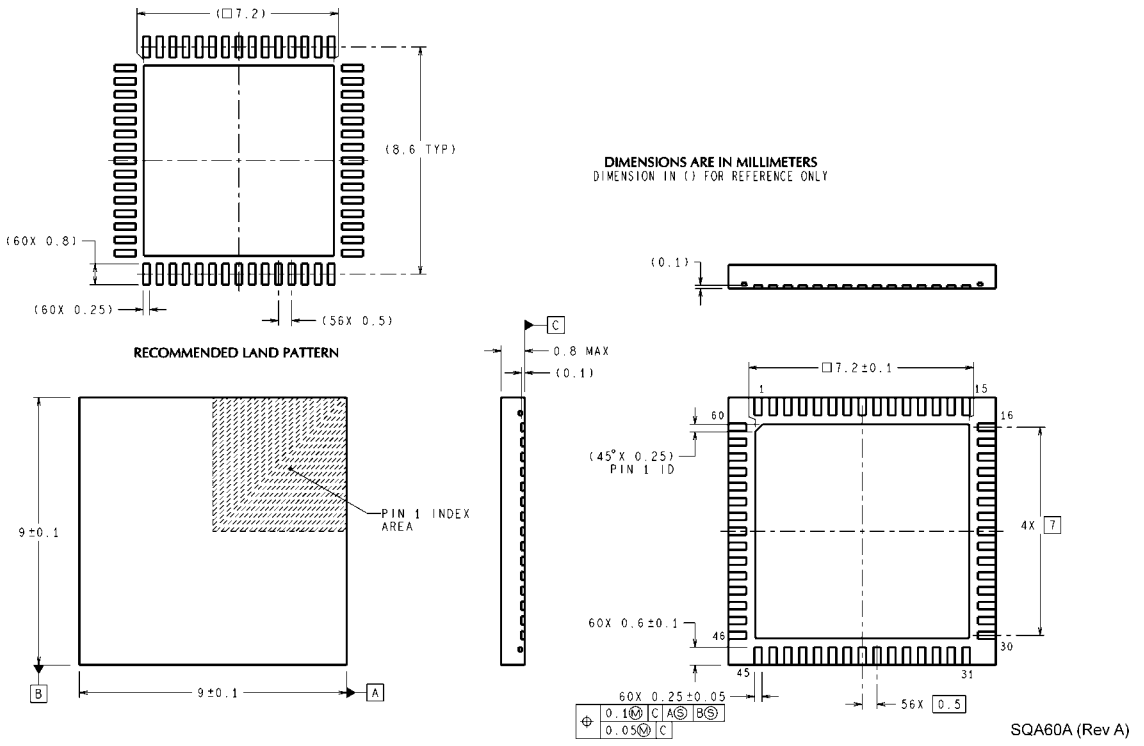


FIGURE 2. Transfer Characteristic

Physical Dimensions inches (millimeters) unless otherwise noted



TOP View.....SIDE View.....BOTTOM View
60-Lead LLP Package
Ordering Numbers:
ADC12DC080CISQ / ADC12DC105CISQ
NS Package Number SQA60A

Notes

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