



**ANALOG  
DEVICES**

# Single Channel, 12/16-Bit, Serial Input, Current Source & Voltage Output DAC

Preliminary Technical Data

**AD5412/AD5422**

## FEATURES

- 12/16-Bit Resolution and Monotonicity**
- Current Output Ranges: 4–20mA, 0–20mA or 0–24mA**
- 0.1% typ Total Unadjusted Error (TUE)**
- 5ppm/°C Output Drift**
- Voltage Output Ranges: 0–5V, 0–10V, ±5V, ±10V,**
- 10% over-range**
- 0.05% Total Unadjusted Error (TUE)**
- 3ppm/°C Output Drift**
- Flexible Serial Digital Interface**
- On-Chip Output Fault Detection**
- On-Chip Reference (10 ppm/°C Max)**
- Asynchronous CLEAR Function**
- Power Supply Range**
- AV<sub>DD</sub> : 10.8V to 40 V**
- AV<sub>SS</sub> : -26.4V to -3V/0V**
- Output Loop Compliance to AV<sub>DD</sub> – 2.5 V**
- Temperature Range: -40°C to +85°C**
- TSSOP and LFCSP Packages**

## APPLICATIONS

- Process Control
- Actuator Control
- PLC

## GENERAL DESCRIPTION

The AD5412/AD5422 is a low-cost, precision, fully integrated 12/16-bit converter offering a programmable current source and programmable voltage output designed to meet the requirements of industrial process control applications. The output current range is programmable to 4mA to 20 mA, 0mA to 20mA or an overrange function of 0mA to 24mA. Voltage output is provided from a separate pin that can be configured to provide 0V to 5V, 0V to 10V, ±5V or ±10V output ranges, an over-range of 10% is available on all ranges. Analog outputs are short and open circuit protected and can drive capacitive loads of 1uF and inductive loads of 1H. The device is specified to operate with a power supply range from 10.8 V to 40 V. Output loop compliance is 0 V to AV<sub>DD</sub> – 2.5 V. The flexible serial interface is SPI and MICROWIRE compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications. The device also includes a power-on-reset function ensuring that the device powers up in a known state and an asynchronous CLEAR pin which sets the outputs to zero-scale / mid-scale voltage output or the low end of the selected current range. The total output error is typically ±0.1% in current mode and ±0.05% in voltage mode.

Table 1. Pin Compatible Devices

Part Number	Description
AD5420	Single Channel, 16-Bit, Serial Input Current Source DAC
AD5410	Single Channel, 12-Bit, Serial Input Current Source DAC



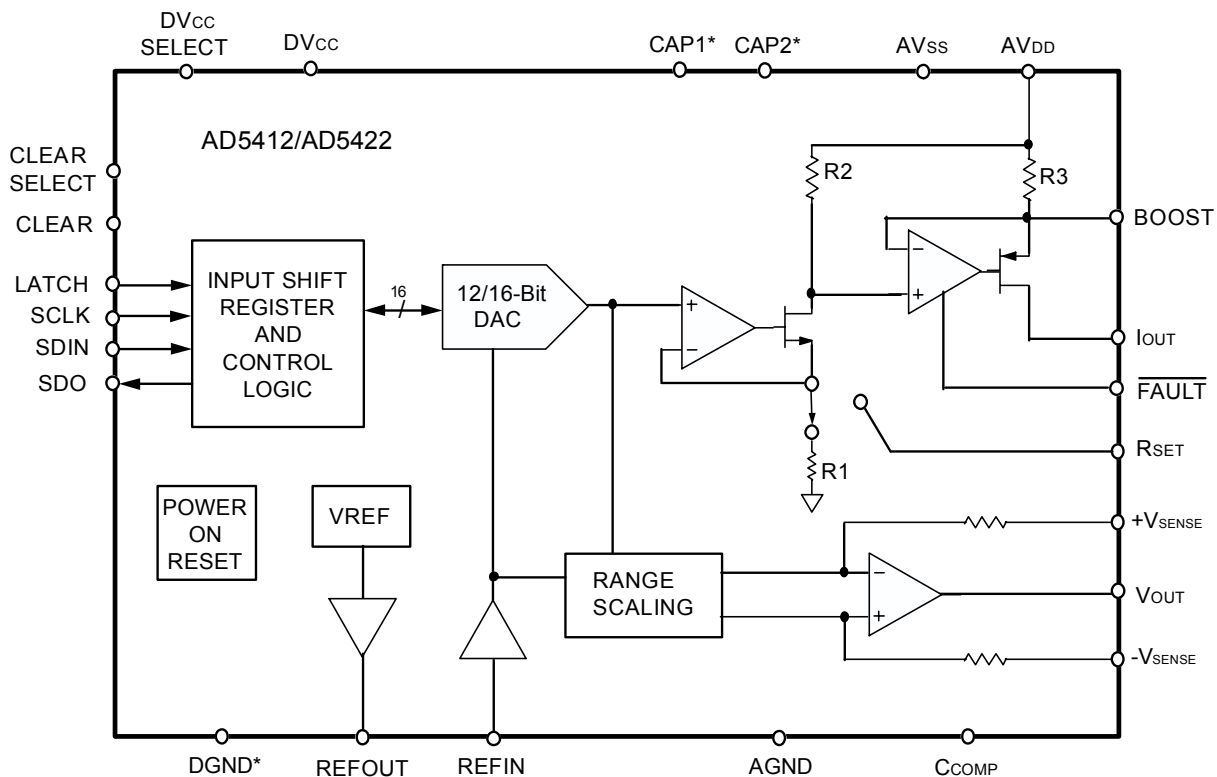
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## REVISION HISTORY

PrF – Preliminary Version, April 25, 2008

### FUNCTIONAL BLOCK DIAGRAM



\*LFCSP Package

Figure 1.

## SPECIFICATIONS

$AV_{DD} = 10.8V$  to  $40V$ ,  $AV_{SS} = -26.4V$  to  $-3V/0V$ ,  $AV_{DD} + |AV_{SS}| < 52.8V$ ,  $AGND = DGND = 0V$ ,  $REFIN = +5V$  external;

$DV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{OUT} : R_L = 1k\Omega$ ,  $C_L = 200pF$ ,  $I_{OUT} : R_L = 300\Omega$ ,  $H_L = 50mH$ ;

all specifications  $T_{MIN}$  to  $T_{MAX}$ ,  $\pm 10V / 0$  to  $24mA$  range unless otherwise noted.

Table 2.

Parameter	Value <sup>1</sup>	Unit	Test Conditions/Comments
<b>VOLTAGE OUTPUT</b>			
Output Voltage Ranges	0 to 5	V	
	0 to 10	V	
	-5 to +5	V	
	-10 to +10	V	
<b>ACCURACY</b>			
Output unloaded			
<b>Bipolar Output</b>			
Resolution	16	Bits	AD5422
	12	Bits	AD5412
Total Unadjusted Error (TUE)	0.1	% FSR max	Over temperature, supplies, and time, typically 0.05% FSR
TUE TC <sup>2</sup>	$\pm 3$	ppm typ	
Relative Accuracy (INL)	$\pm 0.012$	% FSR max	AD5422
	$\pm 0.024$	% FSR max	AD5412
Differential Nonlinearity (DNL)	$\pm 1$	LSB max	Guaranteed monotonic
Bipolar Zero Error	$\pm 5$	mV max	@ 25°C, error at other temperatures obtained using bipolar zero TC
Bipolar Zero TC <sup>2</sup>	$\pm 3$	ppm FSR/°C max	
Zero-Scale Error	$\pm 1$	mV max	@ 25°C, error at other temperatures obtained using zero scale TC
Zero-Scale TC <sup>2</sup>	$\pm 3$	ppm FSR/°C max	
Gain Error	$\pm 0.05$	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Gain TC <sup>2</sup>	$\pm 8$	ppm FSR/°C max	
Full-Scale Error	0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Full-Scale TC <sup>2</sup>	$\pm 3$	ppm FSR/°C max	
<b>Unipolar Output</b>			
$AV_{SS} = 0V$			
Resolution	16	Bits	AD5422
	12	Bits	AD5412
Total Unadjusted Error (TUE)	0.1	% FSR max	Over temperature, supplies, and time, typically 0.05% FSR
Relative Accuracy (INL)	$\pm 0.012$	% FSR max	AD5422
	$\pm 0.024$	% FSR max	AD5412
Differential Nonlinearity (DNL)	$\pm 1$	LSB max	Guaranteed monotonic (at 16 bit-resolution)
Zero Scale Error	+10	mV max	@ 25°C, error at other temperatures obtained using gain TC
Zero Scale TC <sup>2</sup>	$\pm 3$	ppm FSR/°C max	
Offset Error	$\pm 10$	mV max	
Gain Error	$\pm 0.05$	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Gain TC <sup>2</sup>	$\pm 3$	ppm FSR/°C max	
Full-Scale Error	0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Full-Scale TC <sup>2</sup>	$\pm 3$	ppm FSR/°C max	
<b>OUTPUT CHARACTERISTICS<sup>2</sup></b>			
Headroom	0.8	V max	0.5V typ. Output Unloaded
	TBD	V max	TBD typ. 1K $\Omega$ Load on Output

Parameter	Value <sup>1</sup>	Unit	Test Conditions/Comments
Output Voltage TC	±3	ppm FSR/°C max	Vout = ¾ of Full-Scale
Output Voltage Drift vs. Time	±12 ±15	ppm FSR/500 hr typ ppm FSR/1000 hr typ	
Short-Circuit Current	20	mA typ	For specified performance
Load	2	kΩ min	
Capacitive Load Stability			External compensation capacitor of 4nF connected.
R <sub>L</sub> = ∞	20	nF max	
R <sub>L</sub> = 2 kΩ	TBD	nF max	
R <sub>L</sub> = ∞	1	μF max	
DC Output Impedance	0.3	Ω typ	
Power-On Time	10	μs typ	
DC PSRR	TBD	μV/V	
<b>CURRENT OUTPUT</b>			
Output Current Ranges	0 to 24 0 to 20 4 to 20	mA mA mA	
<b>ACCURACY</b>			
Resolution	16 12	Bits Bits	AD5422 AD5412
Total Unadjusted Error (TUE)	±0.3	% FSR max	Over temperature, supplies, and time, typically 0.1% FSR
TUE TC <sup>2</sup>	±5	ppm/°C typ	
Relative Accuracy (INL)	±0.012 ±0.024	% FSR max % FSR max	AD5422 AD5412
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Offset Error	±0.05	% FSR max	
Offset Error Drift	±5	μV/°C typ	
Gain Error	±0.02	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Gain TC <sup>2</sup>	±8	ppm FSR/°C max	
Full-Scale Error	0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Full-Scale TC <sup>2</sup>	±8	ppm FSR/°C	
<b>OUTPUT CHARACTERISTICS<sup>2</sup></b>			
Current Loop Compliance Voltage	AVDD - 2.5	V max	
Output Current Drift vs. Time	TBD TBD	ppm FSR/500 hr typ ppm FSR/1000 hr typ	
Resistive Load	1200	Ω max	
Inductive Load	1	H max	
DC PSRR	1	μA/V max	
Output Impedance	50	MΩ typ	
<b>REFERENCE INPUT/OUTPUT</b>			
Reference Input <sup>2</sup>			
Reference Input Voltage	5	V nom	±1% for specified performance Typically 40 kΩ
DC Input Impedance	30	kΩ min	
Reference Range	4 to 5	V min to V max	
Reference Output			
Output Voltage	4.998 to 5.002	V min to V max	@ 25°C
Reference TC	±10	ppm/°C max	
Output Noise (0.1 Hz to 10 Hz) <sup>2</sup>	18	μV p-p typ	@ 10 kHz
Noise Spectral Density <sup>2</sup>	120	nV/√Hz typ	
Output Voltage Drift vs. Time <sup>2</sup>	±40 ±50	ppm/500 hr typ ppm/1000 hr typ	
Capacitive Load	TBD	nF max	

Parameter	Value <sup>1</sup>	Unit	Test Conditions/Comments
Load Current	5	mA typ	
Short Circuit Current	7	mA typ	
Line Regulation <sup>2</sup>	10	ppm/V typ	
Load Regulation <sup>2</sup>	TBD	ppm/mA	
Thermal Hysteresis <sup>2</sup>	TBD	ppm	
<b>DIGITAL INPUTS<sup>2</sup></b>			DV <sub>CC</sub> = 2.7 V to 5.5 V, JEDEC compliant
V <sub>IH</sub> , Input High Voltage	2	V min	
V <sub>IL</sub> , Input Low Voltage	0.8	V max	
Input Current	±1	μA max	Per pin
Pin Capacitance	10	pF typ	Per pin
<b>DIGITAL OUTPUTS<sup>2</sup></b>			
SDO			
V <sub>OL</sub> , Output Low Voltage	0.4	V max	sinking 200 μA
V <sub>OH</sub> , Output High Voltage	DV <sub>CC</sub> – 0.5	V min	sourcing 200 μA
High Impedance Leakage Current	±1	μA max	
High Impedance Output Capacitance	5	pF typ	
<b>FAULT</b>			
V <sub>OL</sub> , Output Low Voltage	0.4	V max	10kΩ pull-up resistor to DV <sub>CC</sub>
V <sub>OL</sub> , Output Low Voltage	0.6	V typ	@ 2.5 mA
V <sub>OH</sub> , Output High Voltage	3.6	V min	10kΩ pull-up resistor to DV <sub>CC</sub>
<b>POWER REQUIREMENTS</b>			
AV <sub>DD</sub>	10.8 to 40	V min to V max	
AV <sub>SS</sub>	-26.4 to 0	V min to V max	
AV <sub>SS</sub>   + AV <sub>DD</sub>	10.8 to 52.8	V min to V max	
DV <sub>CC</sub>			
Input Voltage	2.7 to 5.5	V min to V max	Internal supply disabled
Output Voltage	4.5	V typ	DV <sub>CC</sub> can be overdriven up to 5.5V
Output Load Current	5	mA typ	
Short Circuit Current	20	mA typ	
AI <sub>DD</sub>	TBD	mA	Output unloaded
AI <sub>SS</sub>	TBD	mA	Output unloaded
DI <sub>CC</sub>	1	mA max	V <sub>IH</sub> = DV <sub>CC</sub> , V <sub>IL</sub> = GND, TBD mA typ
Power Dissipation	TBD	mW typ	AV <sub>DD</sub> = 40V, AV <sub>SS</sub> = 0 V, V <sub>OUT</sub> unloaded
	TBD	mW typ	AV <sub>DD</sub> = 40V, AV <sub>SS</sub> = -15 V, V <sub>OUT</sub> unloaded
	TBD	mW typ	AV <sub>DD</sub> = 15V, AV <sub>SS</sub> = -15 V, V <sub>OUT</sub> unloaded

<sup>1</sup> Temperature range: -40°C to +85°C; typical at +25°C.

<sup>2</sup> Guaranteed by characterization. Not production tested.

**AC PERFORMANCE CHARACTERISTICS**

$AV_{DD} = 10.8V$  to  $40V$ ,  $AV_{SS} = -26.4V$  to  $-3V/0V$ ,  $AV_{DD} + |AV_{SS}| < 52.8V$ ,  $AGND = DGND = 0V$ ,  $REFIN = +5V$  external;  
 $DV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{OUT} : R_L = 1k\Omega$ ,  $C_L = 200pF$ ,  $I_{OUT} : R_L = 300\Omega$ ,  $H_L = 50mH$ ;  
 all specifications  $T_{MIN}$  to  $T_{MAX}$ ,  $\pm 10V / 0$  to  $24mA$  range unless otherwise noted.

Table 3.

Parameter <sup>1</sup>		Unit	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE</b>			
<b>VOLTAGE OUTPUT</b>			
Output Voltage Settling Time	8	$\mu s$ typ	Full-scale step (10V) to $\pm 0.03\%$ FSR
	10	$\mu s$ max	
	5	$\mu s$ max	512 LSB step settling (16-Bit LSB)
Slew Rate	1	V/ $\mu s$ typ	
Power-On Glitch Energy	10	nV-sec typ	
Digital-to-Analog Glitch Energy	10	nV-sec typ	
Glitch Impulse Peak Amplitude	20	mV typ	
Digital Feedthrough	1	nV-sec typ	
Output Noise (0.1 Hz to 10 Hz Bandwidth)	0.1	LSB p-p typ	16-Bit LSB
Output Noise (100 kHz Bandwidth)	80	$\mu V$ rms max	
1/f Corner Frequency	1	kHz typ	
Output Noise Spectral Density	100	nV/ $\sqrt{Hz}$ typ	Measured at 10 kHz
AC PSRR	TBD	dB	200mV 50/60Hz Sinewave superimposed on power supply voltage.
<b>CURRENT OUTPUT</b>			
Output Current Settling Time	TBD	$\mu s$ typ	To 0.1% FSR, L = 1H
	TBD	$\mu s$ typ	To 0.1% FSR, L < 1mH
AC PSRR	TBD	dB	200mV 50/60Hz Sinewave superimposed on power supply voltage.

<sup>1</sup> Guaranteed by characterization, not production tested.

**TIMING CHARACTERISTICS**

$AV_{DD} = 10.8V$  to  $40V$ ,  $AV_{SS} = -26.4V$  to  $-3V/0V$ ,  $AV_{DD} + |AV_{SS}| < 52.8V$ ,  $AGND = DGND = 0V$ ,  $REFIN = +5V$  external;  
 $DV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{OUT} : R_L = 1k\Omega$ ,  $C_L = 200pF$ ,  $I_{OUT} : R_L = 300\Omega$ ,  $H_L = 50mH$ ;  
 all specifications  $T_{MIN}$  to  $T_{MAX}$ ,  $\pm 10V / 0$  to  $24mA$  range unless otherwise noted.

Table 4.

Parameter <sup>1, 2, 3</sup>	Limit at $T_{MIN}$ , $T_{MAX}$	Unit	Description
<b>Write Mode</b>			
$t_1$	33	ns min	SCLK cycle time
$t_2$	13	ns min	SCLK low time
$t_3$	13	ns min	SCLK high time
$t_4$	13	ns min	LATCH delay time
$t_5$	40	ns min	LATCH high time
$t_5$	5	$\mu s$ min	LATCH high time (After a write to the CONTROL register)
$t_6$	5	ns min	Data setup time
$t_7$	5	ns min	Data hold time
$t_8$	40	ns min	LATCH low time
$t_9$	20	ns min	CLEAR pulsewidth
$t_{10}$	5	$\mu s$ max	CLEAR activation time
<b>Readback Mode</b>			
$t_{11}$	82	ns min	SCLK cycle time
$t_{12}$	33	ns min	SCLK low time
$t_{13}$	33	ns min	SCLK high time
$t_{14}$	13	ns min	LATCH delay time
$t_{15}$	40	ns min	LATCH high time
$t_{16}$	5	ns min	Data setup time
$t_{17}$	5	ns min	Data hold time
$t_{18}$	40	ns min	LATCH low time
$t_{19}$	40	ns max	Serial output delay time ( $C_{LSDO}^4 = 15pF$ )
$t_{20}$	33	ns max	LATCH rising edge to SDO tri-state
<b>Daisychain Mode</b>			
$t_{21}$	82	ns min	SCLK cycle time
$t_{22}$	33	ns min	SCLK low time
$t_{23}$	33	ns min	SCLK high time
$t_{24}$	13	ns min	LATCH delay time
$t_{25}$	40	ns min	LATCH high time
$t_{26}$	5	ns min	Data setup time
$t_{27}$	5	ns min	Data hold time
$t_{28}$	40	ns min	LATCH low time
$t_{29}$	40	ns max	Serial output delay time ( $C_{LSDO}^4 = 15pF$ )

<sup>1</sup> Guaranteed by characterization. Not production tested.

<sup>2</sup> All input signals are specified with  $t_R = t_F = 5ns$  (10% to 90% of  $DV_{CC}$ ) and timed from a voltage level of 1.2V.

<sup>3</sup> See Figure 2, Figure 3, and Figure 4.

<sup>4</sup>  $C_{LSDO}$  = Capacitive load on SDO output.



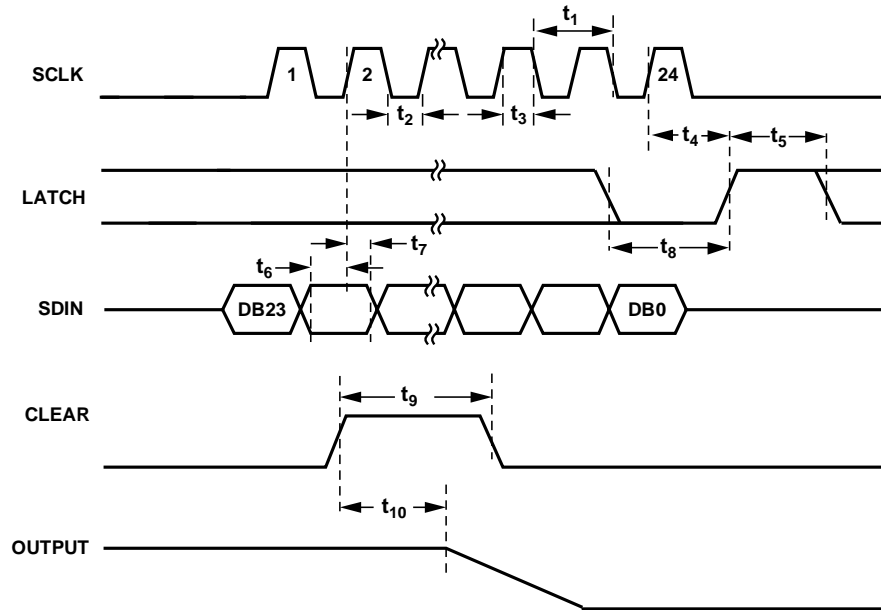


Figure 2. Write Mode Timing Diagram

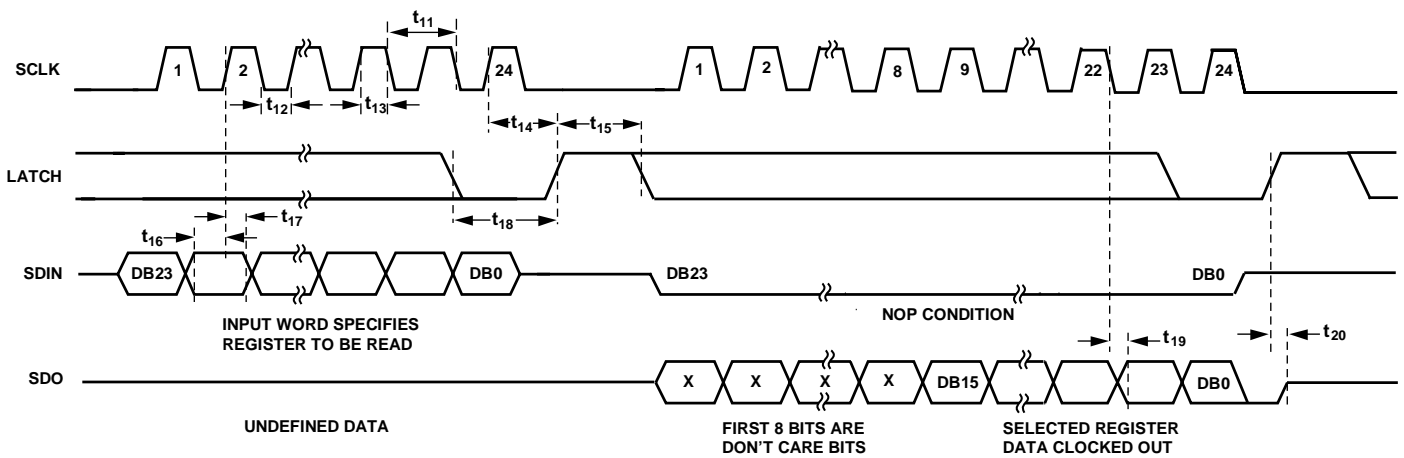


Figure 3. Readback Mode Timing Diagram

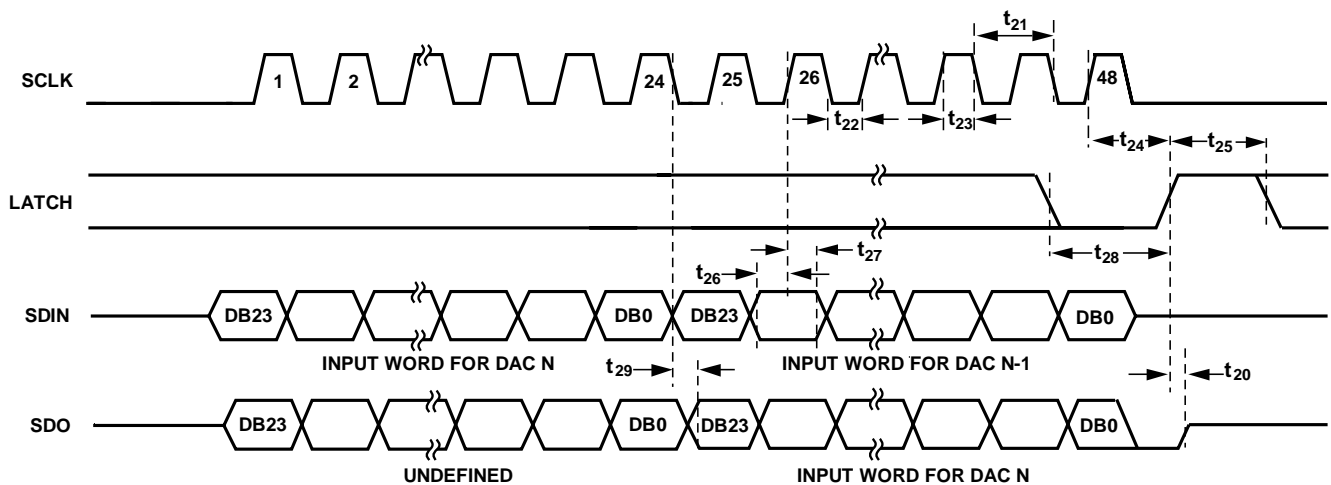


Figure 4. Daisychain Mode Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
$AV_{DD}$ to AGND, DGND	-0.3V to 48V
$AV_{SS}$ to AGND, DGND	+0.3 V to -48 V
$AV_{DD}$ to $AV_{SS}$	-0.3V to 60V
$DV_{CC}$ to AGND, DGND	-0.3 V to +7 V
Digital Inputs to AGND, DGND	-0.3 V to $DV_{CC} + 0.3$ V or 7 V (whichever is less)
Digital Outputs to AGND, DGND	-0.3 V to $DV_{CC} + 0.3$ V or 7V (whichever is less)
REFIN/REFOUT to AGND, DGND	-0.3 V to +7 V
$V_{OUT}$ to AGND, DGND	$AV_{SS}$ to $AV_{DD}$
$I_{OUT}$ to AGND, DGND	-0.3V to $AV_{DD}$
AGND to DGND	-0.3V to +0.3V
Operating Temperature Range ( $T_A$ )	
Industrial	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature ( $T_J$ max)	125°C
24-Lead TSSOP Package	
$\theta_{JA}$ Thermal Impedance	42°C/W
40-Lead LFCSP Package	
$\theta_{JA}$ Thermal Impedance	28°C/W
Power Dissipation	$(T_J \text{ max} - T_A) / \theta_{JA}$
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

<sup>1</sup> Power dissipated on chip must be de-rated to keep junction temperature below 125°C. Assumption is max power dissipation condition is sourcing 24mA into Ground from  $AV_{DD}$  with a 3mA on-chip current.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

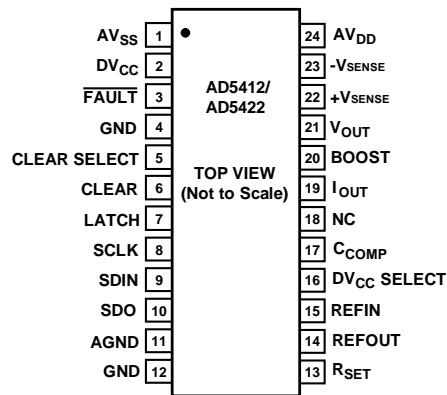


Figure 5. TSSOP Pin Configuration

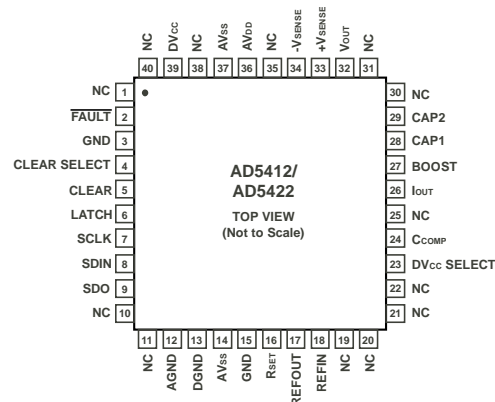


Figure 6. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1	14,37	AV <sub>SS</sub>	Negative Analog Supply Pin. Voltage ranges from -3 V to -24 V. This pin can be connected to 0V if output voltage range is unipolar.
2	39	DV <sub>CC</sub>	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
3	2	FAULT	Fault alert, This pin is asserted low when an open circuit is detected in current mode or an over temperature is detected. Open drain output, must be connected to a pull-up resistor.
4,12	3,15	GND	These pins must be connected to 0V.
18	1,10,11,19, 20,21,22,25,30, 31,35,38,40	NC	No Connection. Do not connect to this pin.
5	4	CLEAR SELECT	Selects the voltage output clear value, either zero-scale or mid-scale code. See Table 21
6	5	CLEAR	Active High Input. Asserting this pin will set the current output to the bottom of the selected range or will set the voltage output to the user selected value (zero-scale or mid-scale).
7	6	LATCH	Positive edge sensitive latch, a rising edge will parallel load the input shift register data into the DAC register, also updating the output.
8	7	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds up to 30 MHz.
9	8	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK.
10	9	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is valid on the rising edge of SCLK. See Figure 3 and Figure 4.
11	12	AGND	Ground reference pin for analog circuitry.
N/A	13	DGND	Ground reference pin for digital circuitry. (AGND and DGND are internally connected in TSSOP package).
13	16	R <sub>SET</sub>	An external, precision, low drift 15kΩ current setting resistor can be connected to this pin to improve the I <sub>OUT</sub> temperature drift performance. Refer to Features section.
14	17	REFOUT	Internal Reference Voltage Output. REFOUT = 5 V ± 2 mV.
15	18	REFIN	External Reference Voltage Input. Reference input range is 4 V to 5 V. REFIN = 5 V for specified performance.
16	23	DV <sub>CC</sub> SELECT	This pin when connected to GND disables the internal supply and an external supply must be connected to the DV <sub>CC</sub> pin. Leave this pin unconnected to enable the internal supply. Refer to features section.
17	24	C <sub>COMP</sub>	Optional compensation capacitor connection for the voltage output buffer. Connecting a 4nF capacitor between this pin and the V <sub>OUT</sub> pin will allow the voltage output to drive up to 1μF. It should be noted that the addition of this capacitor will reduce the

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
			bandwidth of the output amplifier increasing the settling time.
19	26	I <sub>OUT</sub>	Current output pin.
20	27	BOOST	Optional external transistor connection. Connecting an external transistor will reduce the power dissipated in the AD5412/AD5422. Refer to the features section.
N/A	28	CAP1	Connection for optional output filtering capacitor. Refer to Features section.
N/A	29	CAP2	Connection for optional output filtering capacitor. Refer to Features section.
21	32	V <sub>OUT</sub>	Buffered Analog Output Voltage. The output amplifier is capable of directly driving a 1 k $\Omega$ , 2000 pF load.
22	33	+V <sub>SENSE</sub>	Sense connection for the positive voltage output load connection.
23	34	-V <sub>SENSE</sub>	Sense connection for the negative voltage output load connection.
24	36	AV <sub>DD</sub>	Positive Analog Supply Pin. Voltage ranges from 10.8V to 60V.
Paddle	Paddle	AV <sub>SS</sub>	Negative Analog Supply Pin. Voltage ranges from -3 V to -24 V. This pin can be connected to 0V if output voltage range is unipolar.

## TYPICAL PERFORMANCE CHARACTERISTICS

### VOLTAGE OUTPUT

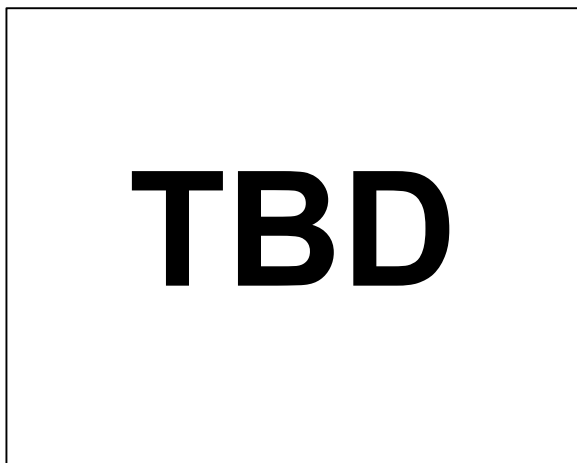


Figure 7. Integral Non Linearity Error vs DAC Code (Four Traces)

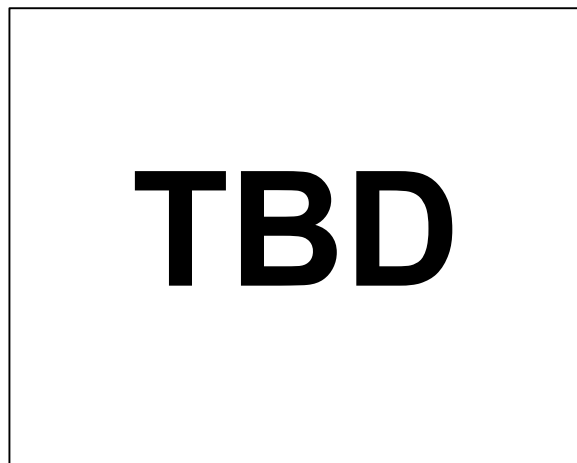


Figure 10. Integral Non Linearity vs. Temperature (Four Traces)

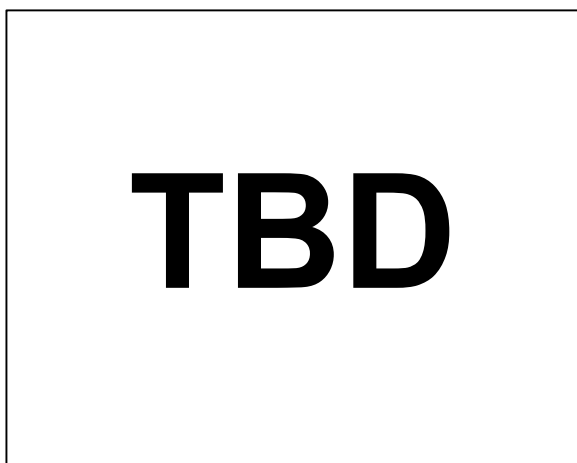


Figure 8. Differential Non Linearity Error vs. DAC Code (Four Traces)

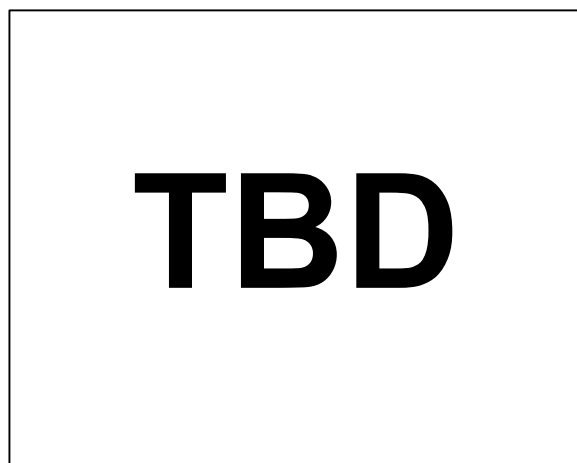


Figure 11. Differential Non Linearity vs. Temperature (Four Traces)

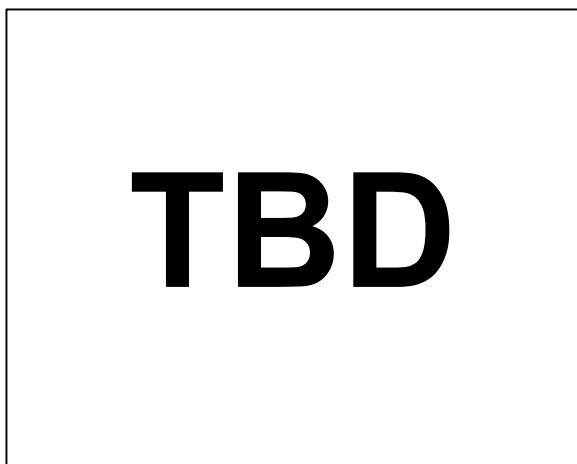


Figure 9. Total Unadjusted Error vs. DAC Code (Four Traces)

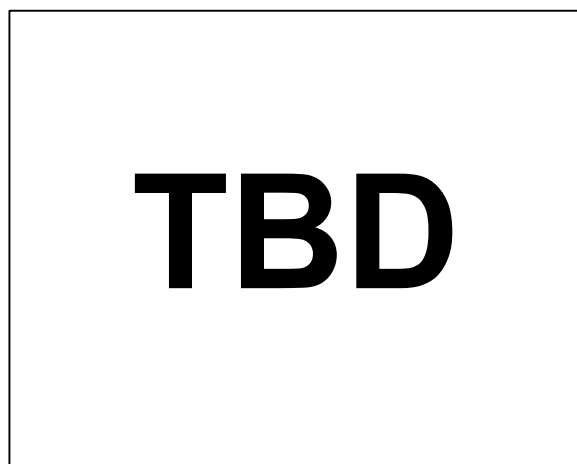


Figure 12. Integral Non Linearity vs. Supply Voltage (Four Traces)

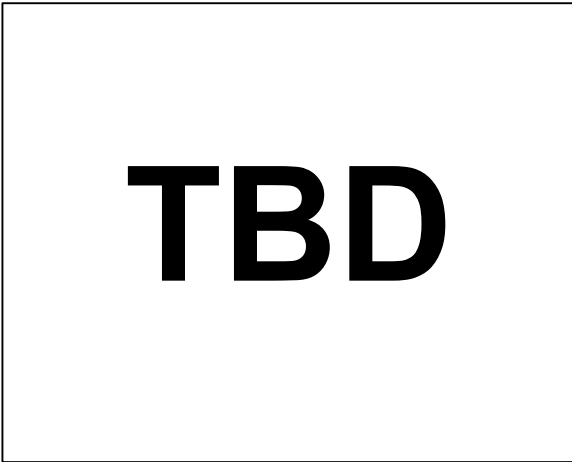


Figure 13. Differential Non Linearity Error vs. Supply Voltage (Four Traces)

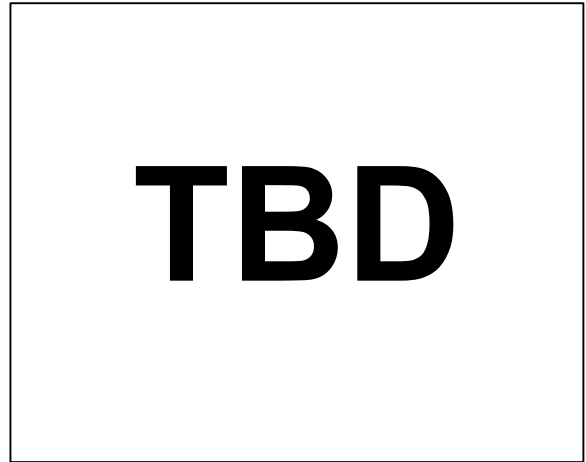


Figure 16. Total Unadjusted Error vs. Reference Voltage (Four Traces)

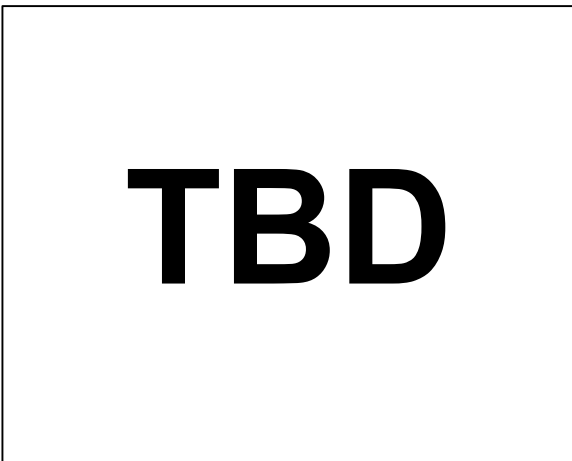


Figure 14. Integral Non Linearity Error vs. Reference Voltage (Four traces)

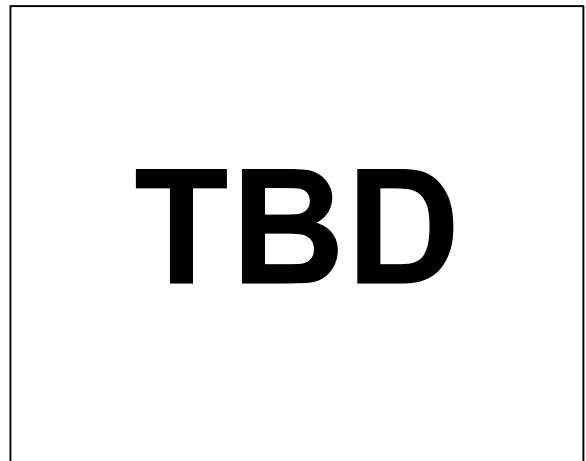


Figure 17. Total Unadjusted Error vs. Supply Voltage (Four Traces)

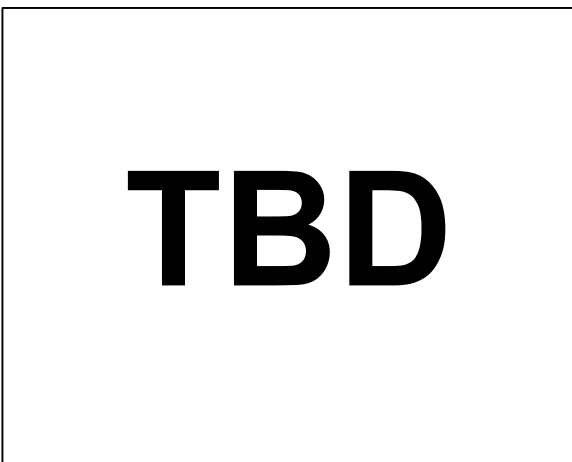


Figure 15. Differential Non Linearity Error vs. Reference Voltage (Four Traces)

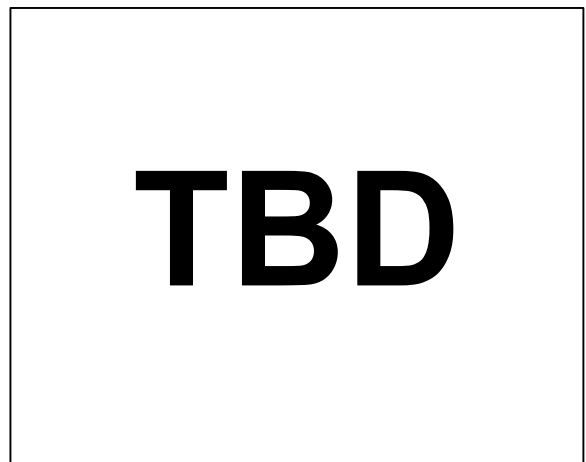


Figure 18. Offset Error vs. Temperature

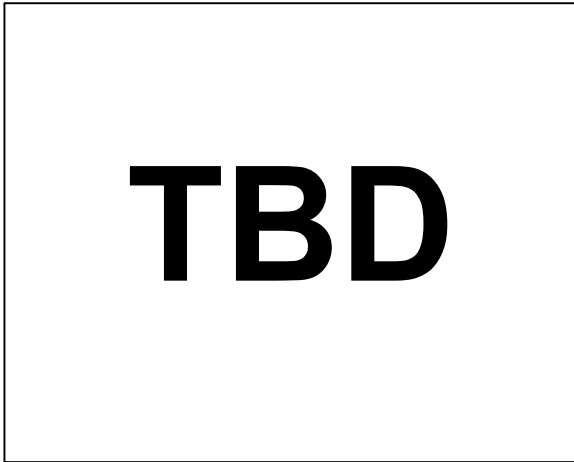


Figure 19. Bipolar Zero Error vs. Temperature

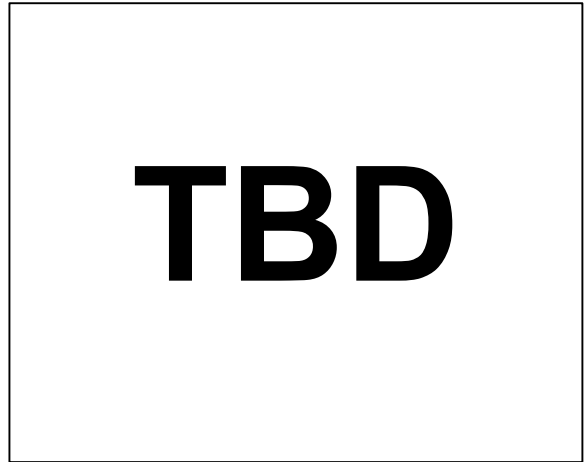


Figure 22. Source and Sink Capability of Output Amplifier Zero-Scale Loaded

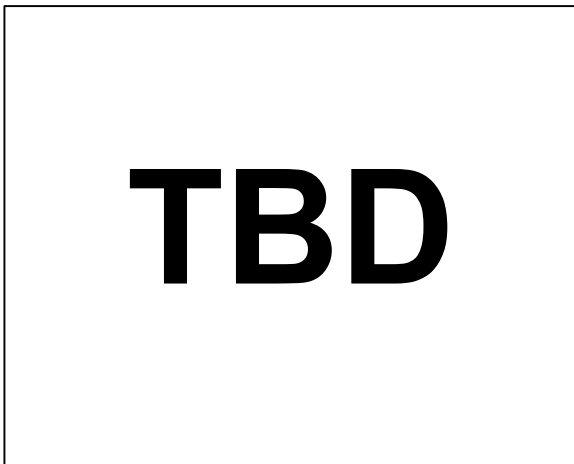


Figure 20. Gain Error vs. Temperature

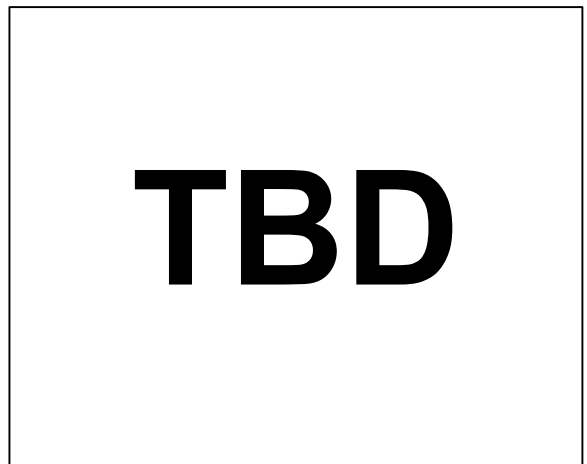


Figure 23. Full-Scale Positive Step

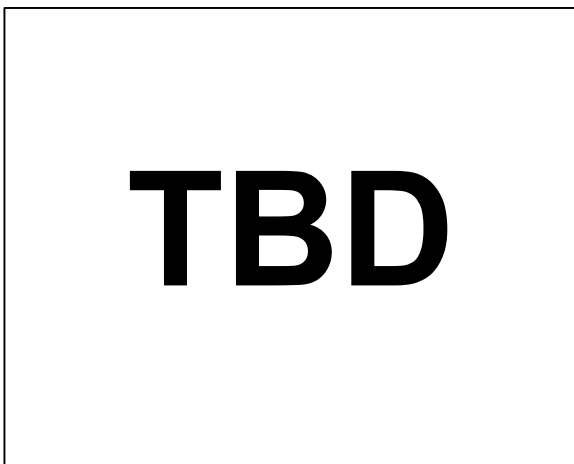


Figure 21. Source and Sink Capability of Output Amplifier Full-Scale Code Loaded

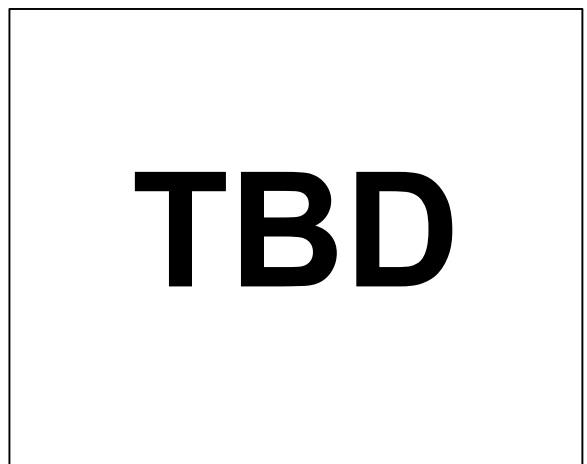


Figure 24. Full-Scale Negative Step

**TBD**

Figure 25. Digital-to-Analog Glitch Energy

**TBD**

Figure 28.  $V_{OUT}$  vs. Time on Power-up

**TBD**

Figure 26. Peak-to-Peak Noise (0.1Hz to 10Hz Bandwidth)

**TBD**

Figure 29.  $V_{OUT}$  vs. Time on Output Enabled

**TBD**

Figure 27. Peak-to-Peak Noise (100kHz Bandwidth)



**TYPICAL PERFORMANCE CHARACTERISTICS**  
**CURRENT OUTPUT**

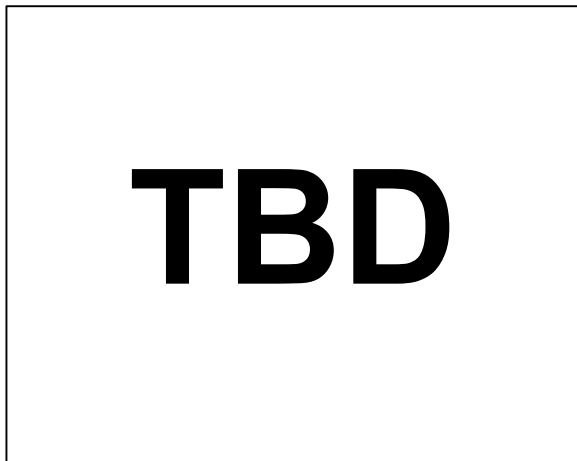


Figure 30. Integral Non Linearity vs. Code

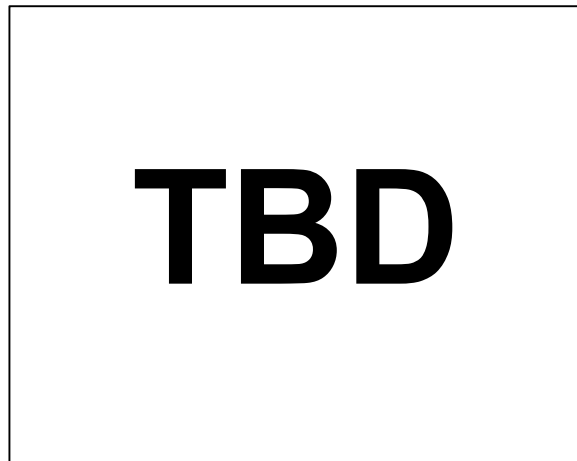


Figure 33. Integral Non Linearity vs. Temperature

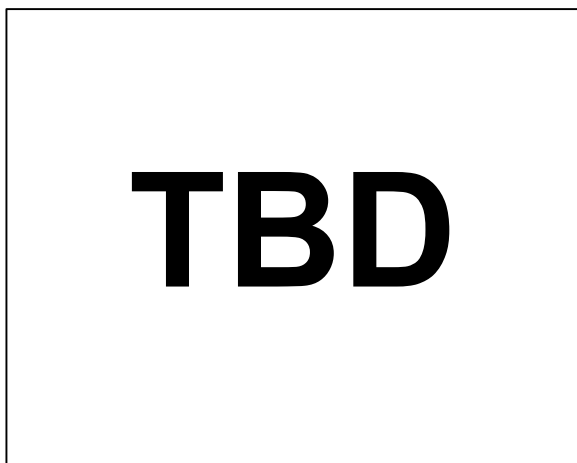


Figure 31. Differential Non Linearity vs. Code

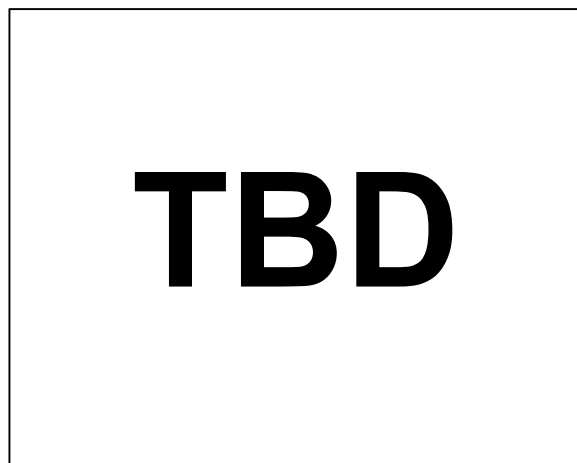


Figure 34. Differential Non Linearity vs. Temperature

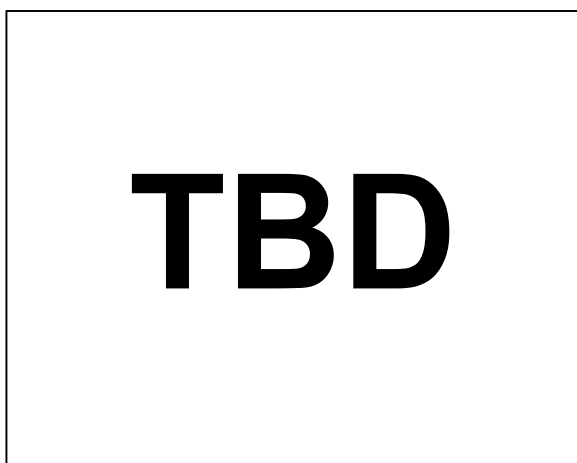


Figure 32. Total Unadjusted Error vs. Code

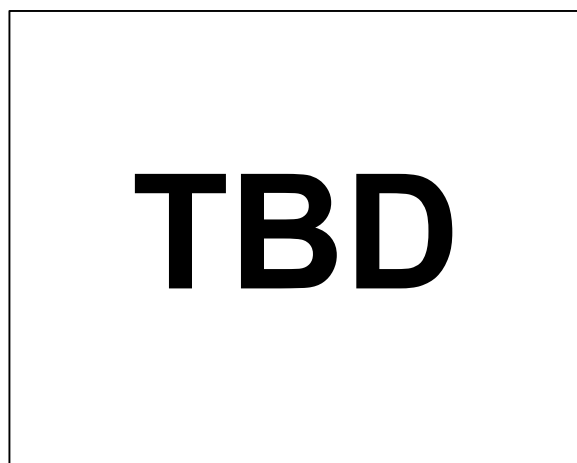


Figure 35. Integral Non Linearity vs. Supply

**TBD**

Figure 36. Differential Non Linearity vs. Supply Voltage

**TBD**

Figure 39. Total Unadjusted Error vs. Reference Voltage

**TBD**

Figure 37. Integral Non Linearity vs. Reference Voltage

**TBD**

Figure 40. Total Unadjusted Error vs. Supply Voltage

**TBD**

Figure 38. Differential Non Linearity vs. Reference Voltage

**TBD**

Figure 41. Offset Error vs. Temperature

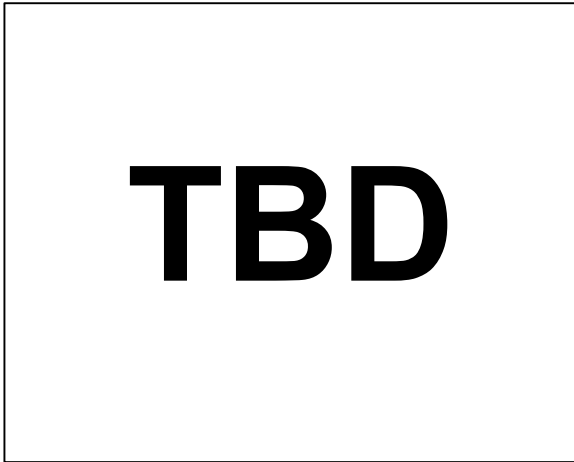


Figure 42. Gain Error vs. Temperature

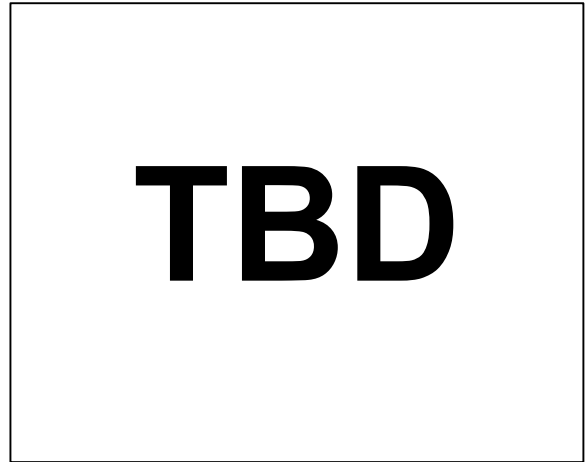


Figure 44.  $I_{OUT}$  vs. Time on Power-up

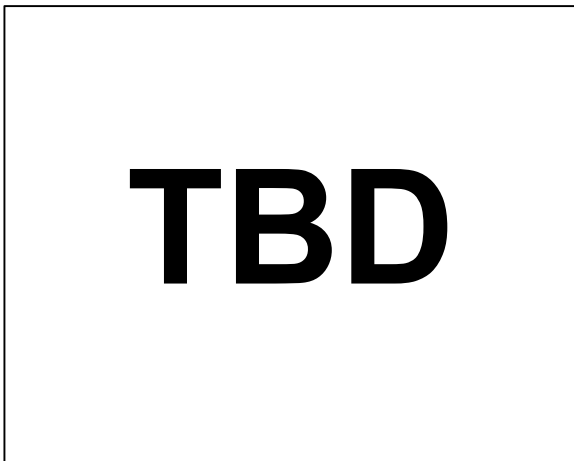


Figure 43. Voltage Compliance vs. Temperature



Figure 45.  $I_{OUT}$  vs. Time on Output Enabled

### TYPICAL PERFORMANCE CHARACTERISTICS

#### GENERAL

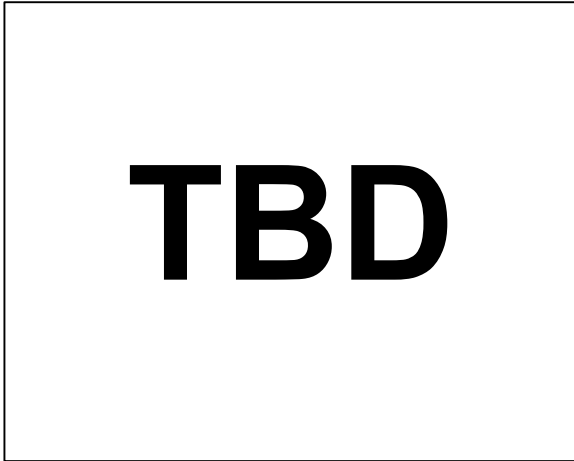


Figure 46.  $D_{CC}$  vs. Logic Input Voltage

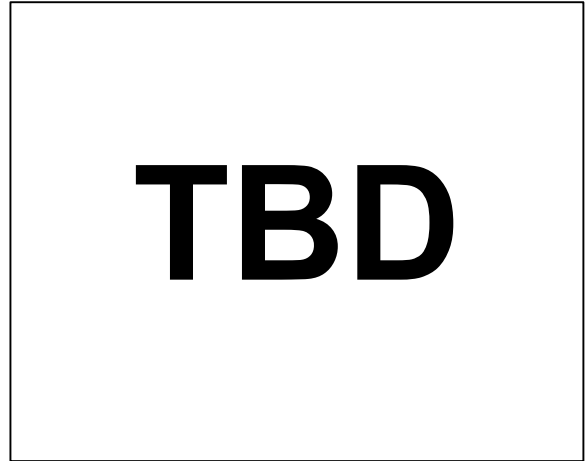


Figure 49.  $DV_{CC}$  Output Voltage vs.  $D_{CC}$  Load Current

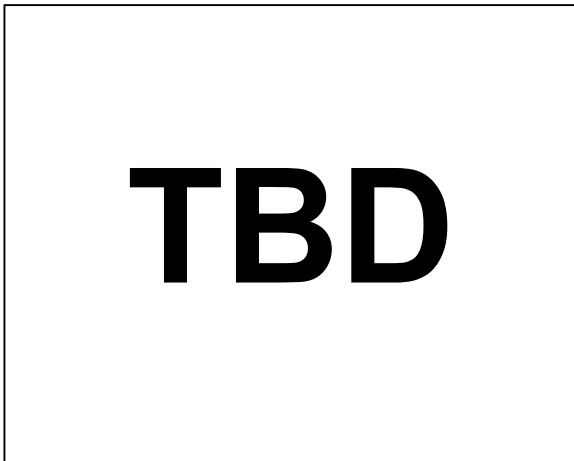


Figure 47.  $A_{I_{DD}}/A_{I_{SS}}$  vs  $A_{V_{DD}}/A_{V_{SS}}$

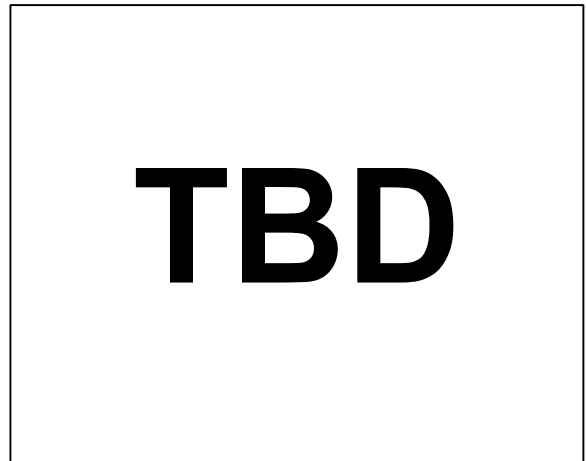


Figure 50. Refout Turn-on Transient

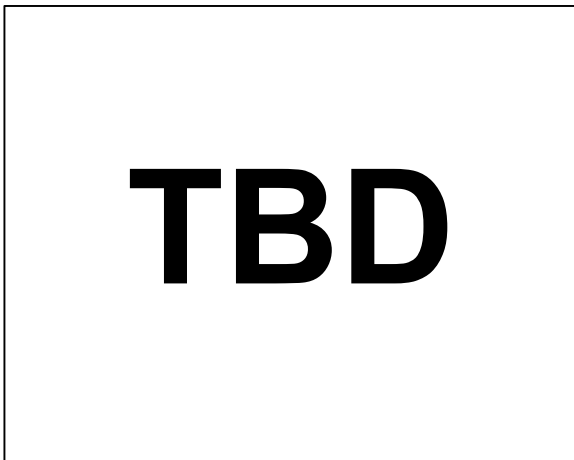


Figure 48.  $A_{I_{DD}}$  vs  $A_{V_{DD}}$

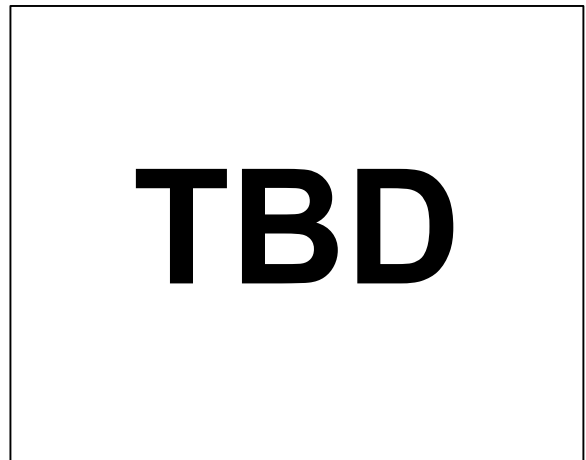


Figure 51. Refout Output Noise (0.1Hz to 10Hz Bandwidth)

**TBD**

Figure 52. Refout Output Noise (100kHz Bandwidth)

**TBD**

Figure 55. Refout Histogram of Thermal Hysteresis

**TBD**

Figure 53. Refout Line Transient

**TBD**

Figure 56. Refout Voltage vs. Load Current

**TBD**

Figure 54. Refout Load Transient

## TERMINOLOGY

### Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 7.

### Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 10.

### Monotonicity

A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5724R/AD5734R/AD5754R are monotonic over their full operating temperature range.

### Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure TBD.

### Bipolar Zero TC

Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/ $^{\circ}$ C.

### Full-Scale Error

Full-Scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be full-scale  $- 1$  LSB. Full-scale error is expressed in percent of full-scale range (% FSR).

### Negative Full-Scale Error/Zero-Scale Error

Negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage should be negative full-scale  $- 1$  LSB. A plot of zero-scale error vs. temperature can be seen in Figure TBD

### Zero-Scale TC

This is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/ $^{\circ}$ C.

### Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. A plot of settling time can be seen in Figure TBD

### Slew Rate

The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/ $\mu$ s.

### Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed in % FSR. A plot of gain error vs. temperature can be seen in Figure TBD

### Gain TC

This is a measure of the change in gain error with changes in temperature. Gain Error TC is expressed in ppm FSR/ $^{\circ}$ C.

### Total Unadjusted Error

Total unadjusted error (TUE) is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

### Current Loop Voltage Compliance

The maximum voltage at the I<sub>OUT</sub> pin for which the output current will be equal to the programmed value.

### Power-On Glitch Energy

Power-on glitch energy is the impulse injected into the analog output when the AD5412/AD5422 is powered-on. It is specified as the area of the glitch in nV-sec. See Figure TBD

### Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state, but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure TBD

### Glitch Impulse Peak Amplitude

Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure TBD.

### Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

### Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

### Reference TC

Reference TC is a measure of the change in the reference output voltage with a change in temperature. It is expressed in ppm/°C.

**Line Regulation**

Line regulation is the change in reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

**Load Regulation**

Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

**Thermal Hysteresis**

Thermal hysteresis is the change of reference output voltage after the device is cycled through temperatures from +25°C to

–40°C to +85°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle. See Figure TBD for a histogram of thermal hysteresis.

$$V_{O\_HYS} = V_O(25^\circ\text{C}) - V_{O\_TC}$$

$$V_{O\_HYS}(\text{ppm}) = \frac{V_O(25^\circ\text{C}) - V_{O\_TC}}{V_O(25^\circ\text{C})} \times 10^6$$

where:

$$V_O(25^\circ\text{C}) = V_O \text{ at } 25^\circ\text{C}$$

$$V_{O\_TC} = V_O \text{ at } 25^\circ\text{C after temperature cycle}$$

## THEORY OF OPERATION

The AD5412/AD5422 is a precision digital to current loop and voltage output converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop and unipolar/bipolar voltage outputs. The current ranges available are; 0 to 20mA, 0 to 24mA and 4 to 20mA, the voltage ranges available are; 0 to 5V,  $\pm 5V$ , 0 to 10V and  $\pm 10V$ , a 10% over-range is available on all voltage output ranges. The current and voltage outputs are available on separate pins and only one is active at any one time. The desired output configuration is user selectable via the CONTROL register.

## ARCHITECTURE

The DAC core architecture of the AD5412/AD5422 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 57. The 4 MSBs of the 12/16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects 1 of 15 matched resistors to either ground or the reference buffer output. The remaining 8/12 bits of the data-word drive switches S0 to S7/S11 of a 8/12-bit voltage mode R-2R ladder network.

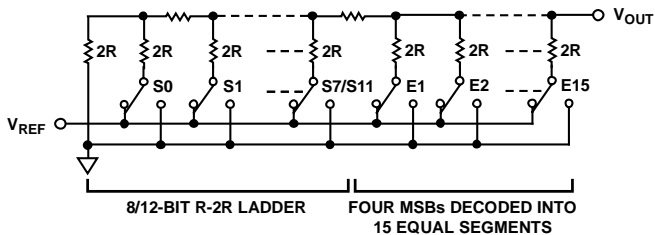


Figure 57. DAC Ladder Structure

The voltage output from the DAC core is either converted to a current (see diagram, Figure 58) which is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground or it is buffered and scaled to output a software selectable unipolar or bipolar voltage range (See diagram, Figure 59). The current and voltage are output on separate pins and cannot be output simultaneously.

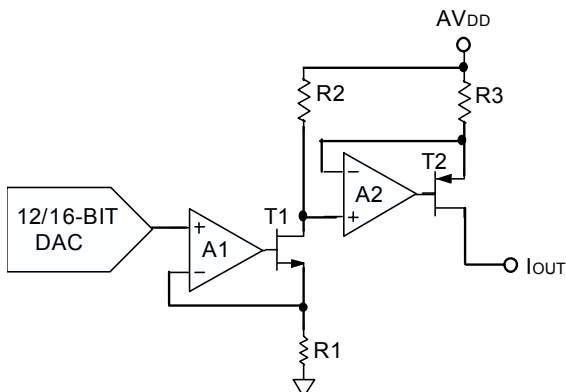


Figure 58. Voltage to Current conversion circuitry

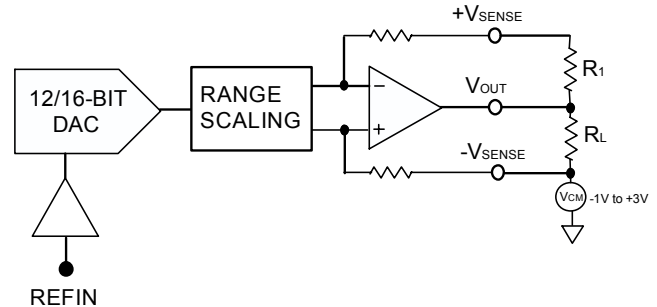


Figure 59. Voltage Output

### Voltage Output Amplifier

The voltage output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 1 k $\Omega$  in parallel with 1  $\mu F$  (with addition of external compensation capacitor) to AGND. The source and sink capabilities of the output amplifier can be seen in Figure 22. The slew rate is 1 V/ $\mu s$  with a full-scale settling time of 10  $\mu s$ , (10V step). Figure 59 shows the voltage output driving a load,  $R_L$  on top of a common mode voltage, ( $V_{CM}$ ) of -1V to +3V. In output module applications where a cable could possibly become disconnected from + $V_{SENSE}$  resulting in the amplifier loop being broken and possibly resulting in large destructive voltages on  $V_{OUT}$ , a resistor,  $R_1$ , of value 2k $\Omega$  to 5k $\Omega$  should be included as shown to ensure the amplifier loop is kept closed. If remote sensing of the load is not required, + $V_{SENSE}$  should be connected to  $V_{OUT}$  and - $V_{SENSE}$  should be connected to GND. When changing ranges on the voltage output a glitch may occur, for this reason it is recommended that the output is disabled by setting the OUTEN bit of the Control register to logic low before changing the output voltage range, this will prevent a glitch from occurring.

### Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacitive loads of up to 1 $\mu F$  with the addition of a non-polarised 4nF compensation capacitor between the  $C_{COMP}$  and  $V_{OUT}$  pins. Without the compensation capacitor, up to 20nF capacitive loads can be driven.

### Reference Buffers

The AD5412/AD5422 can operate with either an external or internal reference. The reference input has an input range of 4 V to 5 V, 5 V for specified performance. This input voltage is then buffered before it is applied to the DAC.

### SERIAL INTERFACE

The AD5412/AD5422 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with SPI<sup>®</sup>, QSPI<sup>™</sup>, MICROWIRE<sup>™</sup>, and DSP standards.



**Input Shift Register**

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the rising edge of SCLK. The input register consists of 8 address bits and 16 data bits as shown in Table 7. The 24 bit word is unconditionally

latched on the rising edge of LATCH. Data will continue to be clocked in irrespective of the state of LATCH, on the rising edge of LATCH the data that is present in the input register will be latched, in other words the last 24 bits to be clocked in before the rising edge of LATCH is the data that is latched. The timing diagram for this operation is shown in Figure 2.

**Table 7. Input Shift Register Format**

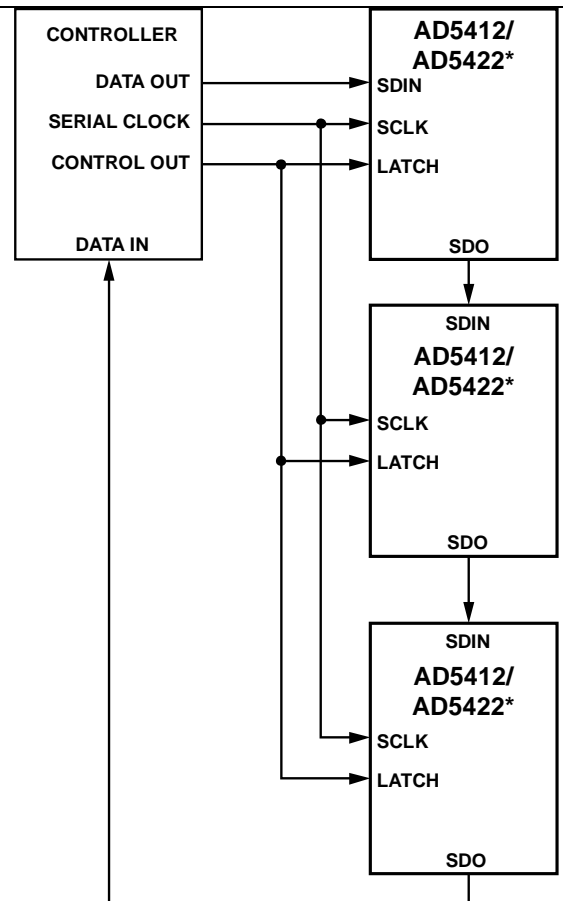
MSB																								LSB
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
ADDRESS WORD								DATA WORD																

**Table 8. Control Word Functions**

Address Word	Function
00000000	No Operation (NOP)
00000001	DATA Register
00000010	Readback register value as per Read Address (See Table 10)
01010101	CONTROL Register
01010110	RESET Register

**Standalone Operation**

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if LATCH is taken high after the correct number of data bits have been clocked in. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. The rising edge of SCLK that clocks in the MSB of the dataword marks the beginning of the write cycle. Exactly 24 rising clock edges must be applied to SCLK before LATCH is brought high. If LATCH is brought high before the 24<sup>th</sup> rising SCLK edge, the data written will be invalid. If more than 24 rising SCLK edges are applied before LATCH is brought high, the input data will also be invalid.



\*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 60. Daisy Chaining the AD5412/AD5422

**Daisy-Chain Operation**

For systems that contain several devices, the SDO pin can be used to daisy chain the devices together as shown in Figure 60. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. Daisychain mode is enabled by setting the DCEN bit of the CONTROL register. The first rising edge of SCLK that clocks in the MSB of the dataword marks the beginning of the write cycle. SCLK is continuously applied to the input shift register. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is valid on the rising edge of SCLK, having been clocked out on the previous falling SCLK edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal  $24 \times N$ , where  $N$  is the total number of AD5412/AD5422 devices in the chain. When the serial transfer to all devices is complete, LATCH is taken high. This latches the input data in each device in the daisy chain. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can only be used if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles

must be used, and LATCH must be taken high after the final clock to latch the data. See Figure 4 for a timing diagram.

**Readback Operation**

Readback mode is invoked by setting the address word and read address as shown in Table 9 and Table 10 when writing to the input register. The next write to the AD5412/AD5422 should be a NOP command which will clock out the data from the previously addressed register as shown in Figure 3.

By default the SDO pin is disabled, after having addressed the AD5412/AD5422 for a read operation, a rising edge on LATCH will enable the SDO pin in anticipation of data being clocked out, after the data has been clocked out on SDO, a rising edge on LATCH will disable (tri-state) the SDO pin once again. To read back the data register for example, the following sequence should be implemented:

1. Write 0x020001 to the input register. This configures the part for read mode with the data register selected.
2. Follow this with a second write, a NOP condition, 0x000000. During this write, the data from the register is clocked out on the SDO line.

**Table 9. Input Shift Register Contents for a read operation**

MSB																				LSB			
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Address

**Table 10. Read Address Decoding**

Read Address	Function
00	Read Status Register
01	Read Data Register
10	Read Control Register

**POWER-ON STATE**

On power-up of the AD5412/AD5422, the power-on-reset circuit ensures that all registers are loaded with zero-code, as such both outputs will be disabled. ( $V_{OUT}$  and  $I_{OUT}$  in tri-state).

**TRANSFER FUNCTION****Voltage Output**

For a unipolar voltage output range, the output voltage can be expressed as:

$$V_{OUT} = V_{REFIN} \times Gain \left[ \frac{D}{2^N} \right]$$

For a bipolar voltage output range, the output voltage can be expressed as:

$$V_{OUT} = V_{REFIN} \times Gain \left[ \frac{D}{2^N} \right] - \frac{Gain \times V_{REFIN}}{2}$$

where:

$D$  is the decimal equivalent of the code loaded to the DAC.

$N$  is the bit resolution of the DAC.

$V_{REFIN}$  is the reference voltage applied at the REF<sub>IN</sub> pin.

$Gain$  is an internal gain whose value depends on the output range selected by the user as shown in Table 11.

**Table 11.**

Output Range	Gain Value
+5V	1
+10V	2
±5V	2
±10V	4

**Current Output**

For the 0 to 20mA, 0 to 24mA and 4 to 20mA current output ranges the output current is respectively expressed as:

$$I_{OUT} = \left[ \frac{20mA}{2^N} \right] \times D$$

$$I_{OUT} = \left[ \frac{24mA}{2^N} \right] \times D$$

$$I_{OUT} = \left[ \frac{16mA}{2^N} \right] \times D + 4mA$$

where:

$D$  is the decimal equivalent of the code loaded to the DAC.

$N$  is the bit resolution of the DAC.

## DATA REGISTER

The DATA register is addressed by setting the address word of the input shift register to 0x01. The data to be written to the DATA register is entered in positions D15 to D4 for the AD5412 and D15 to D0 for the AD5422 as shown in Table 12 and Table 13.

**Table 12. Programming the AD5412 Data Register**

MSB												LSB			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12-BIT DATA WORD												X	X	X	X

**Table 13. Programming the AD5422 Data Register**

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16-BIT DATA WORD															

## CONTROL REGISTER

The CONTROL register is addressed by setting the address word of the input shift register to 0x55. The data to be written to the CONTROL register is entered in positions D15 to D0 as shown in Table 14. The CONTROL register functions are shown in Table 15.

**Table 14. Programming the CONTROL Register**

MSB												LSB			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CLRSEL	OVRNG	REXT	OUTEN	SR CLOCK				SR STEP			SREN	DCEN	R2	R1	R0

**Table 15. Control Register Functions**

Option	Description
CLRSEL	See Table 21 for a description of the CLRSEL operation
OVRNG	Setting this bit increases the voltage output range by 10%. Further details in Features section
REXT	Setting this bit selects the external current setting resistor, Further details in Features section
OUTEN	Output enable. This bit must be set to enable the outputs, The range bits select which output will be functional.
SR CLOCK	See Features Section. Digital Slew Rate Control
SR STEP	See Features Section. Digital Slew Rate Control
SREN	Digital Slew Rate Control enable
DCEN	Daisychain enable
R2,R1,R0	Output range select. See Table 16

**Table 16. Output Range Options**

R2	R1	R0	Output Range Selected
0	0	0	0 to +5V Voltage Range
0	0	1	0 to 10V Voltage Range
0	1	0	±5V Voltage Range
0	1	1	±10V Voltage Range
1	0	1	4 to 20 mA Current Range
1	1	0	0 to 20 mA Current Range
1	1	1	0 to 24 mA Current Range

## RESET REGISTER

The RESET register is addressed by setting the address word of the input shift register to 0x56. The data to be written to the RESET register is entered in positions D15 to D0 as shown in Table 17. The RESET register options are shown in Table 17 and Table 18.

**Table 17. Programming the RESET Register**

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															RESET

**Table 18. RESET register Functions**

Option	Description
RESET	Setting this bit performs a reset operation, restoring the AD5412/AD5422 to its power-on state

**STATUS REGISTER**

The STATUS register is a read only register. The STATUS register functionality is shown in Table 19 and Table 20.

**Table 19. Decoding the STATUS Register**

MSB												LSB			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												I <sub>OUT</sub> FAULT	SLEW ACTIVE	OVER TEMP	

**Table 20. STATUS Register Functions**

Option	Description
I <sub>OUT</sub> FAULT	This bit will be set if a fault is detected on the I <sub>OUT</sub> pin.
SLEW ACTIVE	This bit will be set while the output value is slewing (slew rate control enabled)
OVER TEMP	This bit will be set if the AD5412/AD5422 core temperature exceeds approx. 150°C.

## FEATURES

### FAULT ALERT

The AD5412/AD5422 is equipped with a FAULT pin, this is an open-drain output allowing several AD5412/AD5422 devices to be connected together to one pull-up resistor for global fault detection. The FAULT pin is forced active by any one of the following fault scenarios;

- 1) The Voltage at  $I_{OUT}$  attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The  $I_{OUT}$  current is controlled by a PMOS transistor and internal amplifier as shown in Figure 58. The internal circuitry that develops the fault output avoids using a comparator with “window limits” since this would require an actual output error before the FAULT output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately one volt of remaining drive capability (when the gate of the output PMOS transistor nearly reaches ground). Thus the FAULT output activates slightly before the compliance limit is reached. Since the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain and an output error does not occur before the FAULT output becomes active.
- 2) If the core temperature of the AD5412/AD5422 exceeds approx. 150°C.

The  $I_{OUT}$  FAULT and OVER TEMP bits of the STATUS register are used in conjunction with the FAULT pin to inform the user which one of the fault conditions caused the FAULT pin to be asserted. See Table 19 and Table 20.

### VOLTAGE OUTPUT SHORT CIRCUIT PROTECTION

Under normal operation the voltage output will sink/source 10mA and maintain specified operation. The maximum current that the voltage output will deliver is approx. 20mA, this is the short circuit current.

### VOLTAGE OUTPUT OVER-RANGE

An over-range facility is provided on the voltage output. When enabled via the CONTROL register, the selected output range will be over-ranged by 10%.

### VOLTAGE OUTPUT FORCE-SENSE

The  $+V_{SENSE}$  and  $-V_{SENSE}$  pins are provided to facilitate remote sensing of the load connected to the voltage output. If the load is connected at the end of a long or high impedance cable, sensing the voltage at the load will allow the output amplifier to compensate and ensure the correct voltage is applied across the load. This function is limited only by the available power supply headroom.

### ASYNCHRONOUS CLEAR (CLEAR)

CLEAR is an active high clear that allows the voltage output to be cleared to either zero-scale code or mid-scale code, user-selectable via the CLEAR SELECT pin or the CLRSEL bit of the CONTROL register as described in Table 21. (The Clear select feature is a logical OR function of the CLEAR SELECT pin and the CLRSEL bit). The Current output will clear to the bottom of its programmed range. It is necessary to maintain CLEAR high for a minimum amount of time (see Figure 2) to complete the operation. When the CLEAR signal is returned low, the output remains at the cleared value. The pre-clear value can be restored by pulsing the LATCH signal low without clocking any data. A new value cannot be programmed until the CLEAR pin is returned low.

Table 21. CLEAR SELECT Options

CLRSEL	Output Value	
	Unipolar Output Range	Bipolar Output Range
0	0V	0V
1	Mid-Scale	Negative Full-Scale

As well as defining the output value for a clear operation, the CLRSEL bit and CLEAR SELECT pin also define the default output value. On selection of a new voltage range the output value will be as defined in Table 21. It is recommended, to avoid glitches on the output, that before changing voltage ranges the output be disabled by setting the OUTEN bit of the Control register to logic low. When OUTEN is set to logic high the output will go to the default value as defined by CLRSEL and CLEAR SELECT.

### INTERNAL REFERENCE

The AD5412/AD5422 contains an integrated +5V voltage reference with initial accuracy of  $\pm 2\text{mV}$  max and a temperature drift coefficient of  $\pm 10$  ppm/°C max. The reference voltage is buffered and externally available for use elsewhere within the system. See Figure 56 for a load regulation graph of the Integrated reference.

### EXTERNAL CURRENT SETTING RESISTOR

Referring to Figure 58, R1 is an internal sense resistor as part of the voltage to current conversion circuitry. The stability of the output current over temperature is dependent on the stability of the value of R1. As a method of improving the stability of the output current over temperature an external precision 15k $\Omega$  low drift resistor can be connected to the RSET pin of the AD5412/AD5422 to be used instead of the internal resistor R1. The external resistor is selected via the CONTROL register. See Table 14.

### DIGITAL POWER SUPPLY

By default, the DVCC pin accepts a power supply of 2.7V to 5.5V, alternatively, via the DVCC SELECT pin an internal 4.5V power supply may be output on the DVCC pin for use as a digital power

supply for other devices in the system or as a termination for pull-up resistors. This facility offers the advantage of not having to bring a digital supply across an isolation barrier. The internal power supply is enabled by leaving the DV<sub>CC</sub> SELECT pin unconnected. To disable the internal supply DV<sub>CC</sub> SELECT should be tied to 0V. DV<sub>CC</sub> is capable of supplying up to 5mA of current, for a load regulation graph see Figure 49.

**EXTERNAL BOOST FUNCTION**

The addition of an external boost transistor as shown in Figure 61 will reduce the power dissipated in the AD5412/AD5422 by reducing the current flowing in the on-chip output transistor (dividing it by the current gain of the external circuit). A discrete NPN transistor with a breakdown voltage, BV<sub>CEO</sub>, greater than 60V can be used. The external boost capability has been developed for those users who may wish to use the AD5412/AD5422 at the extremes of the supply voltage, load current and temperature range. The boost transistor can also be used to reduce the amount of temperature induced drift in the part. This will minimise the temperature induced drift of the on-chip voltage reference, which improves on drift and linearity.

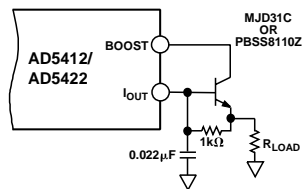


Figure 61. External Boost Configuration

**EXTERNAL COMPENSATION CAPACITOR**

The voltage output can ordinarily drive capacitive loads of up to 20nF, if there is a requirement to drive greater capacitive loads, of up to 1µF, an external compensation capacitor can be connected between the C<sub>COMP</sub> and V<sub>OUT</sub> pins. The addition of the capacitor will keep the output voltage stable but will also reduce the bandwidth and increase the settling time of the voltage output.

**DIGITAL SLEW RATE CONTROL**

The Slew Rate Control feature of the AD5412/AD5422 allows the user to control the rate at which the output value changes. This feature is available on both the current and voltage outputs. With the slew rate control feature disabled the output value will change at a rate limited by the output drive circuitry and the attached load. If the user wishes to reduce the slew rate this can be achieved by enabling the slew rate control feature. With the feature enabled via the SREN bit of the CONTROL register, (See Table 14) the output, instead of slewing directly between two values, will step digitally at a rate defined by two parameters accessible via the CONTROL register as shown in Table 14. The parameters are SR CLOCK and SR STEP. SR CLOCK defines the rate at which the digital slew will be updated. SR STEP defines by how much the output value will change at each update. Together both parameters

define the rate of change of the output value. Table 22 and Table 23 outline the range of values for both the SR CLOCK and SR STEP parameters.

Table 22. Slew Rate Step Size options

SR STEP	AD5412 Step Size (LSBs)	AD5422 Step Size (LSBs)
000	1/16	1
001	1/8	2
010	1/4	4
011	1/2	8
100	1	16
101	2	32
110	4	64
111	8	128

Table 23. Slew Rate Update Clock Options

SR CLOCK	Update Clock Frequency (Hz)
0000	257732
0001	198413
0010	152439
0011	131579
0100	115741
0101	69444
0110	37594
0111	25773
1000	20161
1001	16026
1010	10288
1011	8278
1100	6897
1101	5525
1110	4237
1111	3300

The time it will take for the output to slew over a given output range can be expressed as follows;

$$SlewTime = \frac{OutputChange}{StepSize \times UpdateClockFrequency \times LSBSize}$$

Where:

Slew Time is expressed in seconds

Output Change is expressed in Amps for I<sub>OUT</sub> or Volts for V<sub>OUT</sub>

When the slew rate control feature is enabled, all output changes will change at the programmed slew rate, for example if the CLEAR pin is asserted the output will slew to the clear value at the programmed slew rate. The output can be halted at its current value with a write to the CONTROL register. To avoid halting the output slew, the SLEW ACTIVE bit can be read to check that the slew has completed before writing to the AD5412/AD5422 registers. See Table 19. The update clock frequency for any given value will be the same for all output ranges, the step size however will vary across output ranges for a given value of step size as the LSB size will be different for each output range. Table 24 shows the range of programmable slew times for a full-scale change on any of the output ranges. The values were obtained using the Slew Time equation above.

Table 24. Programmable Slew Time values in seconds for a full-scale change on any output range.

		Step Size (LSBs)							
		1	2	4	8	16	32	64	128
Update Clock Frequency (Hz)	257732	0.25	0.13	0.06	0.03	0.016	0.008	0.004	0.0020
	198413	0.33	0.17	0.08	0.04	0.021	0.010	0.005	0.0026
	152439	0.43	0.21	0.11	0.05	0.027	0.013	0.007	0.0034
	131579	0.50	0.25	0.12	0.06	0.031	0.016	0.008	0.0039
	115741	0.57	0.28	0.14	0.07	0.035	0.018	0.009	0.0044
	69444	0.9	0.47	0.24	0.12	0.06	0.03	0.015	0.007
	37594	1.7	0.87	0.44	0.22	0.11	0.05	0.03	0.014
	25773	2.5	1.3	0.64	0.32	0.16	0.08	0.04	0.020
	20161	3.3	1.6	0.81	0.41	0.20	0.10	0.05	0.025
	16026	4.1	2.0	1.0	0.51	0.26	0.13	0.06	0.03
	10288	6.4	3.2	1.6	0.80	0.40	0.20	0.10	0.05
	8278	7.9	4.0	2.0	1.0	0.49	0.25	0.12	0.06
	6897	9.5	4.8	2.4	1.2	0.59	0.30	0.15	0.07
	5525	12	5.9	3.0	1.5	0.74	0.37	0.19	0.09
	4237	15	7.7	3.9	1.9	0.97	0.48	0.24	0.12
3300	20	9.9	5.0	2.5	1.24	0.62	0.31	0.16	

**I<sub>OUT</sub> FILTERING CAPACITORS (LFCSP PACKAGE)**

Two capacitors may be placed between the pins CAP1, CAP2 and AV<sub>DD</sub> as shown in Figure 62.

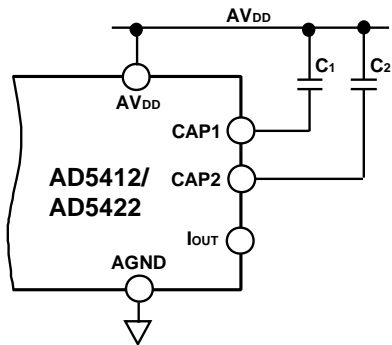


Figure 62. I<sub>OUT</sub> Filtering Capacitors

These two pins are only available on the LFCSP package. The capacitors form a filter on the current output circuitry as shown in Figure 63 reducing the bandwidth and the rate of change of the output current. These capacitors can be used as an

alternative to the Digital Slew Rate Control feature or in addition to it as a means of smoothing out the steps caused by the digital code increments.

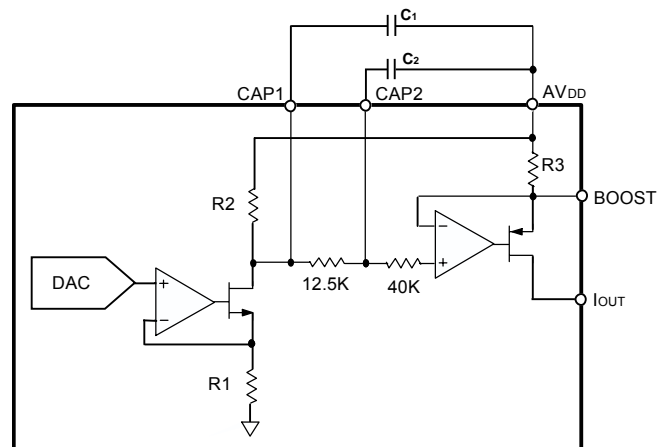


Figure 63. I<sub>OUT</sub> Filter Circuitry



## APPLICATIONS INFORMATION

### DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads connect a 0.01 $\mu$ F capacitor between I<sub>OUT</sub> and GND. This will ensure stability with loads beyond 50mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling. The Digital Slew Rate Control feature may also prove useful in this situation.

### TRANSIENT VOLTAGE PROTECTION

The AD5412/AD5422 contains ESD protection diodes which prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. In order to protect the AD5412/AD5422 from excessively high voltage transients, external power diodes and a surge current limiting resistor is required, as shown in Figure 64. The constraint on the resistor value is that during normal operation the output level at I<sub>OUT</sub> must remain within its voltage compliance limit of  $AV_{DD} - 2.5V$  and the two protection diodes and resistor must have appropriate power ratings. Further protection can be provided with Transient Voltage Suppressors or Transorbs, these are available as both unidirectional (protects against positive high voltage transients) and bidirectional (protects against both positive and negative high voltage transients) and are available in a wide range of standoff and breakdown voltage ratings. It is recommended that all field connected nodes are protected.

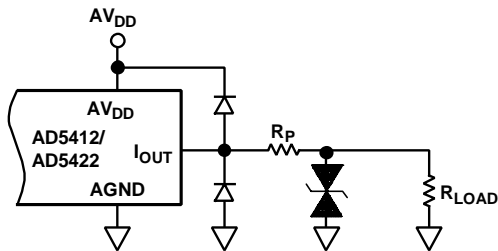


Figure 64. Output Transient Voltage Protection

### SINGLE CONNECTOR FOR I<sub>OUT</sub> AND V<sub>OUT</sub>

Typically in analog output modules that facilitate both current and voltage outputs there is a separate connector for each current output and for each voltage output even though either the voltage output or the current output can be used at any one time, this results in a redundant connector. For instance in an 8 channel current and voltage output module there will be 16 connectors and only 8 of these will be in use at any one time resulting in 8 redundant connectors. The AD5412/AD5422 can be configured with the I<sub>OUT</sub> and V<sub>OUT</sub> pins connected together and to one connector, thus removing the redundant connector and allowing for a reduced sized connector block. Figure 65 shows that with an external buffer amplifier the AD5412/AD5422 can be configured with a single output connector for current and voltage output.

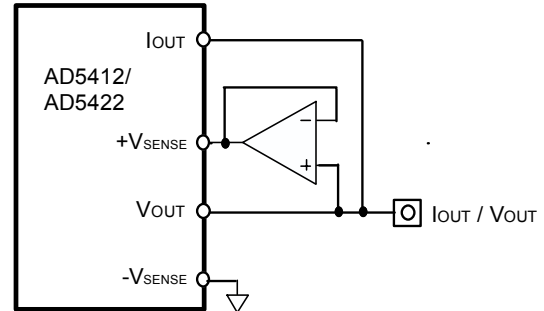
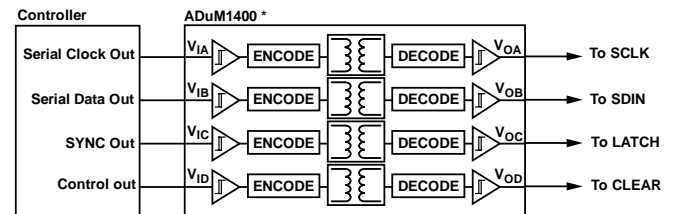


Figure 65. Connecting I<sub>OUT</sub> and V<sub>OUT</sub> to one connector

When the AD5412/AD5422 is configured for a voltage output the I<sub>OUT</sub> pin will be in tri-state, when configured for a current output the V<sub>OUT</sub> pin will be in tri-state, the function of the buffer is to prevent current leakage to ground through the +V<sub>SENSE</sub> pin when the current output is enabled, the +V<sub>SENSE</sub> pin is internally connected to AGND through a resistance of approx. 40k $\Omega$ .

### GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. The iCoupler<sup>®</sup> family of products from Analog Devices provides voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5412/AD5422 make it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 66 shows a 4-channel isolated interface to the AD5412/AD5422 using an ADuM1400. For further information, visit <http://www.analog.com/icouplers>.



\*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 66. Isolated Interface

### MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5412/AD5422 is via a serial bus that uses protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a latch signal. The AD5412/AD5422 require a 24-bit data-word with data valid on the rising edge of SCLK.

For all interfaces, the DAC output update is initiated on the rising edge of LATCH. The contents of the registers can be read using the readback function.

### LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5412/AD5422 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5412/AD5422 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The AD5412/AD5422 should have ample supply bypassing of 10  $\mu\text{F}$  in parallel with 0.1  $\mu\text{F}$  on each supply located as close to the package as possible, ideally right up against the device. The 10  $\mu\text{F}$  capacitors are the tantalum bead type. The 0.1  $\mu\text{F}$  capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5412/AD5422 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

**THERMAL AND SUPPLY CONSIDERATIONS**

The AD5412/AD5422 is designed to operate at a maximum junction temperature of 125°C. It is important that the device is not operated under conditions that will cause the junction temperature to exceed this value. Excessive junction temperature can occur if the AD5412/AD5422 is operated from the maximum AV<sub>DD</sub> and driving the maximum current (24mA) directly to ground. In this case the ambient temperature should be controlled or AV<sub>DD</sub> should be reduced. The conditions will depend on the device package.

At maximum ambient temperature of 85°C the 24-lead TSSOP package can dissipate 950mW and the 40-lead LFCSP package can dissipate 1.42W.

To ensure the junction temperature does not exceed 125°C while driving the maximum current of 24mA directly into ground (also adding an on-chip current of 3mA), AV<sub>DD</sub> should be reduced from the maximum rating to ensure the package is not required to dissipate more power than stated above. See Table 25, Figure 67 and Figure 68.

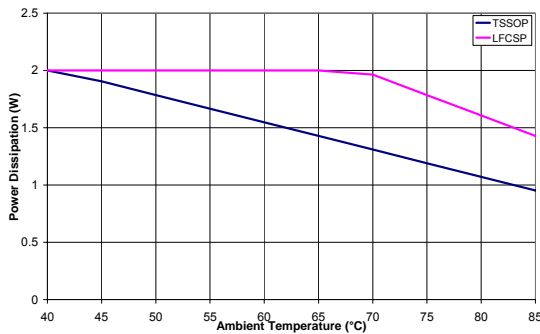


Figure 67. Maximum Power Dissipation Vs Ambient Temperature

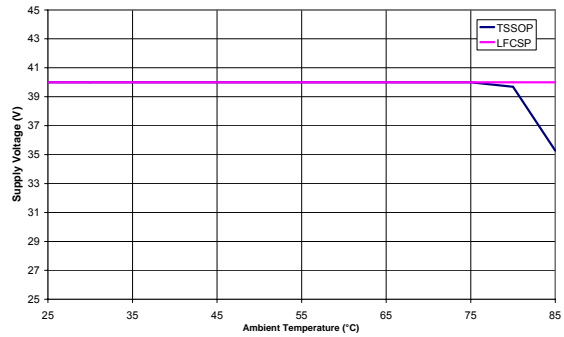
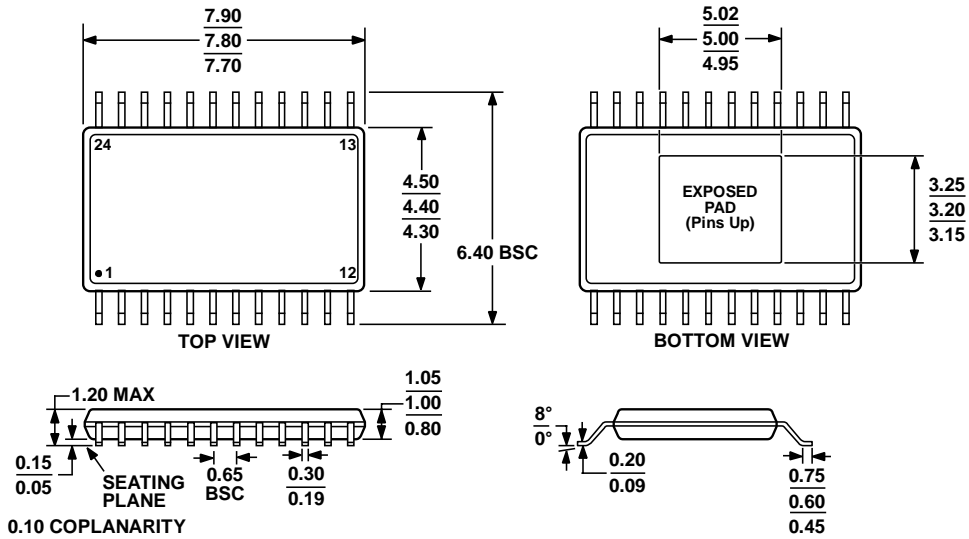


Figure 68. Maximum Supply Voltage Vs Ambient Temperature

**Table 25. Thermal and Supply considerations for each package**

	<b>TSSOP</b>	<b>LFCSP</b>
Maximum allowed power dissipation when operating at an ambient temperature of 85°C	$\frac{T_J \text{ max} - T_A}{\Theta_{JA}} = \frac{125 - 85}{42} = 950mW$	$\frac{T_J \text{ max} - T_A}{\Theta_{JA}} = \frac{125 - 85}{28} = 1.42W$
Maximum allowed ambient temperature when operating from a supply of 40V and driving 24mA directly to ground.	$T_J \text{ max} - P_D \times \Theta_{JA} = 125 - (40 \times 0.027) \times 42 = 79^\circ C$	$T_J \text{ max} - P_D \times \Theta_{JA} = 125 - (40 \times 0.027) \times 28 = 85^\circ C$
Maximum allowed supply voltage when operating at an ambient temperature of 85°C and driving 24mA directly to ground.	$\frac{T_J \text{ max} - T_A}{AI_{DD} \times \Theta_{JA}} = \frac{125 - 85}{0.027 \times 42} = 35V$	$\frac{T_J \text{ max} - T_A}{AI_{DD} \times \Theta_{JA}} = \frac{125 - 85}{0.027 \times 28} = 53V$

OUTLINE DIMENSIONS

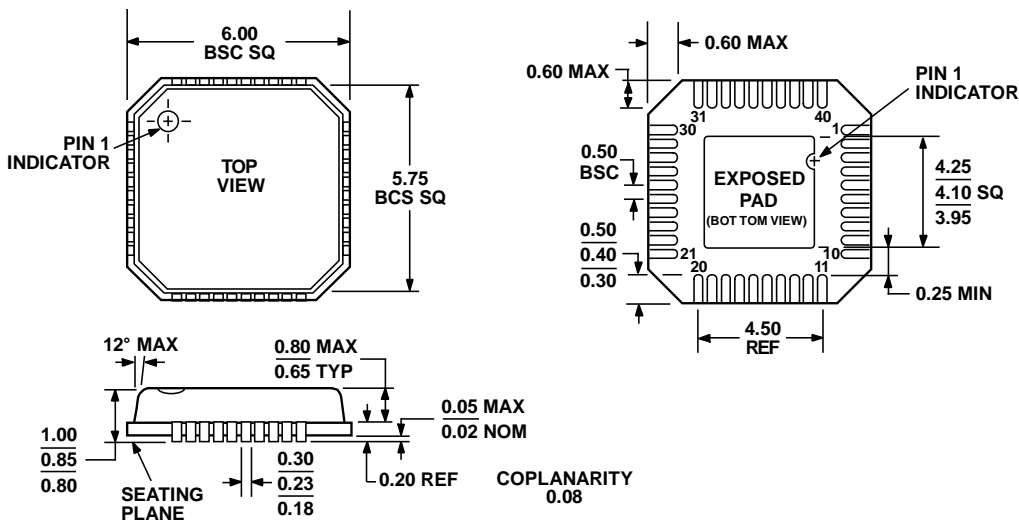


COMPLIANT TO JEDEC STANDARDS MO-153-ADT

Figure 69. 24-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP\_EP] (RE-24)

Dimensions shown in millimeters

050806-A



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-2

Figure 70. 40-Lead Lead Frame Chip Scale Package (CP-40)

Dimensions shown in millimeters

101306-A

**ORDERING GUIDE**

<b>Model</b>	<b>Resolution</b>	<b>Temperature Range</b>	<b>Package Description</b>	<b>Package Option</b>
AD5412AREZ	12 Bits	-40°C to 85°C	24 Lead TSSOP_EP	RE-24
AD5412BREZ	12 Bits	-40°C to 85°C	24 Lead TSSOP_EP	RE-24
AD5412ACPZ	12 Bits	-40°C to 85°C	40 Lead LFCSP	CP-40
AD5412BCPZ	12 Bits	-40°C to 85°C	40 Lead LFCSP	CP-40
AD5422AREZ	16 Bits	-40°C to 85°C	24 Lead TSSOP_EP	RE-24
AD5422BREZ	16 Bits	-40°C to 85°C	24 Lead TSSOP_EP	RE-24
AD5422ACPZ	16 Bits	-40°C to 85°C	40 Lead LFCSP	CP-40
AD5422BCPZ	16 Bits	-40°C to 85°C	40 Lead LFCSP	CP-40

**NOTES**