3.2 Gbps Single Buffered Switch

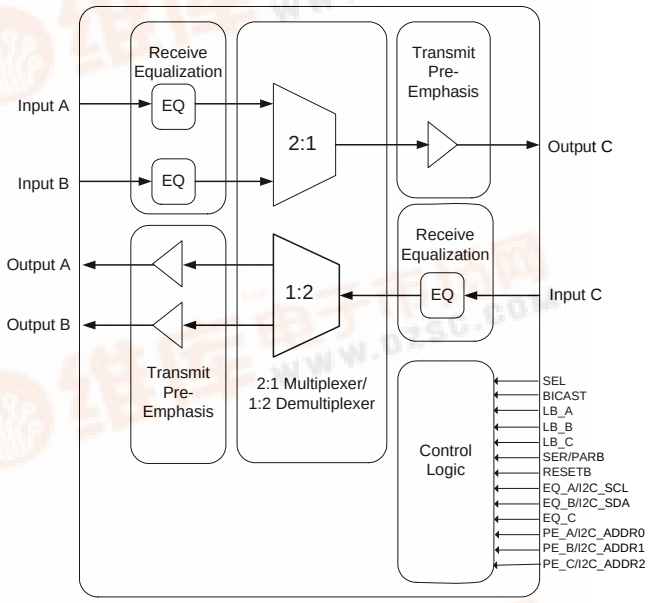
Xstream™

Preliminary Technical Data

AD8153

FEATURES

- Single lane 2:1 mux/1:2 demux
- 3.2 Gbps to DC data rates
- Compensates over 40 inches of FR4 at 3.2 Gbps through
  - Two levels of input equalization, or
  - Four levels of output pre-emphasis
- Accepts ac- or dc-coupled differential inputs
- Low deterministic jitter, typically 20 ps p-p
- Low random jitter, typically 1 ps RMS
- BER < 10^{-16}
- On-chip terminations
- Unicast or bicast on 1:2 demux function
- Loopback capability on all ports
- 3.3 V core supply
- Flexible I/O supply
- Low power, typically 200 mW in basic configuration[1]
- 32-lead QFN package
- –40°C to +85°C operating temperature range



APPLICATIONS

- Low cost redundancy switch
- SONET OC48/SDH16 and lower data rates
- Gigabit Ethernet over backplane
- Fibre channel 1.06 Gbps and 2.12 Gbps over backplane
- Serial RapidIO
- PCI Express
- Infiniband over backplane

GENERAL DESCRIPTION

The AD8153 is an asynchronous, protocol agnostic, single-lane 2:1 switch with three differential PECL/CML-compatible inputs and three differential CML outputs. The AD8159, another member of the *Xstream*™ line of products, is suitable for similar applications that require more than one lane.

The AD8153 is optimized for NRZ signaling with data rates of up to 3.2 Gbps per port. Each port offers two levels of input equalization and four levels of output pre-emphasis.

The device consists of a 2:1 multiplexer and a 1:2 demultiplexer. There are three operating modes: pin mode, serial mode, and mixed mode. In pin mode, switching and equalization/pre-emphasis are controlled exclusively using external pins. In serial mode, an I²C interface is used exclusively to control the device, and to provide access to advanced features, such as additional pre-emphasis settings and output disable. In the mixed mode mode, the user accesses the advanced features using I²C, but controls device switching using the external pins.

The main application of the AD8153 is to support redundancy on both the backplane side and the line interface side of a serial link. The device has unicast and bicast capability, so it is capable of supporting either 1 + 1 or 1:1 redundancy.

Another application for AD8153 is testing high speed serial links by duplicating incoming data and sending it to the destination port and to test equipment simultaneously.

One Technology Way, P.O Box 9106, Norwood, MA 02062-9106, U.S.A.

[1] Two ports active with minimum pre-emphasis.

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REVISION HISTORY

4/06—Revision 0: Initial version.

6/12—Revision 0.1: Updated pin configuration and package mechanical drawings.

SPECIFICATIONS

V_{CC} = +3.3 V, V_{EE} = 0 V, R_L = 50 Ω, two outputs active with minimum pre-emphasis, data rate= 3.2 Gbps, V_{ICM} = 2.7 V[1], V_{ID} = 800 mV p-p[2], T_A = +25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Data Rate/Channel (NRZ)		DC		3.2	Gbps
Deterministic Jitter	Data rate = 3.2 Gbps		20		ps p-p
Random Jitter	RMS		1		ps
Propagation Delay	Input to output		600		ps
Lane-to-Lane Skew			100		ps
Switching Time			5		ns
Output Rise/Fall Time	20% to 80%		100		ps
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential, V_{ICM} = 2.7 V[1]	100		2000	mV p-p
Input Voltage Range	Common mode, V_{ID} = 800 mV p-p[2]	V_{EE} + 1.0		V_{CC} + 0.3	V
Input Bias Current			4		µA
Input Capacitance			2		pF
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential, PE = 0		800		mV p-p
Output Voltage Range	Single-ended absolute voltage level	V_{cc} – 1.6		V_{cc} + 0.6	V
Output Current	Minimum pre-emphasis		16		mA
Output Current	Maximum pre-emphasis, all ports		28		mA
Output Capacitance			2		pF
TERMINATION CHARACTERISTICS					
Resistance	Differential	90	100	110	Ω
Temperature Coefficient			0.15		Ω/°C
POWER SUPPLY					
Operating Range					
V_{CC}	V_{EE} = 0 V	3.0	3.3	3.6	V
Supply Current	Two outputs active, minimum pre-emphasis, dc-coupled inputs/outputs, 400 mV I/O swings (800 mV p-p differential), 50 Ω far end terminations				
I_{CC}			28		mA
$I_{I/O} = I_{TTO} + I_{TTI}$			32		mA
Supply Current	Three outputs active, maximum pre-emphasis, dc-coupled inputs/outputs, 400 mV I/O swings (800 mV p-p differential), 50 Ω far end terminations				
I_{CC}			80		mA
$I_{I/O} = I_{TTO} + I_{TTI}$			84		mA
THERMAL CHARACTERISTICS					
Operating Temperature Range		–40		+85	°C
Θ_{JA}	Still air		30.0		°C/W
LOGIC INPUT CHARACTERISTICS					
Input High (VIH)		2.4		V_{CC}	V
Input Low (VIL)		V_{EE}		0.8	V

[1] V_{ICM}: Input common-mode voltage.
[2] V_{ID}: Input differential peak-to-peak voltage swing.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} to V_{EE}	3.7 V
V_{TTI}	V_{CC} + 0.6 V
V_{TTO}	V_{CC} + 0.6 V
Internal Power Dissipation	4.1 W
Differential Input Voltage	2.0 V
Logic Input Voltage	V_{EE} − 0.3V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Lead Temperature	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

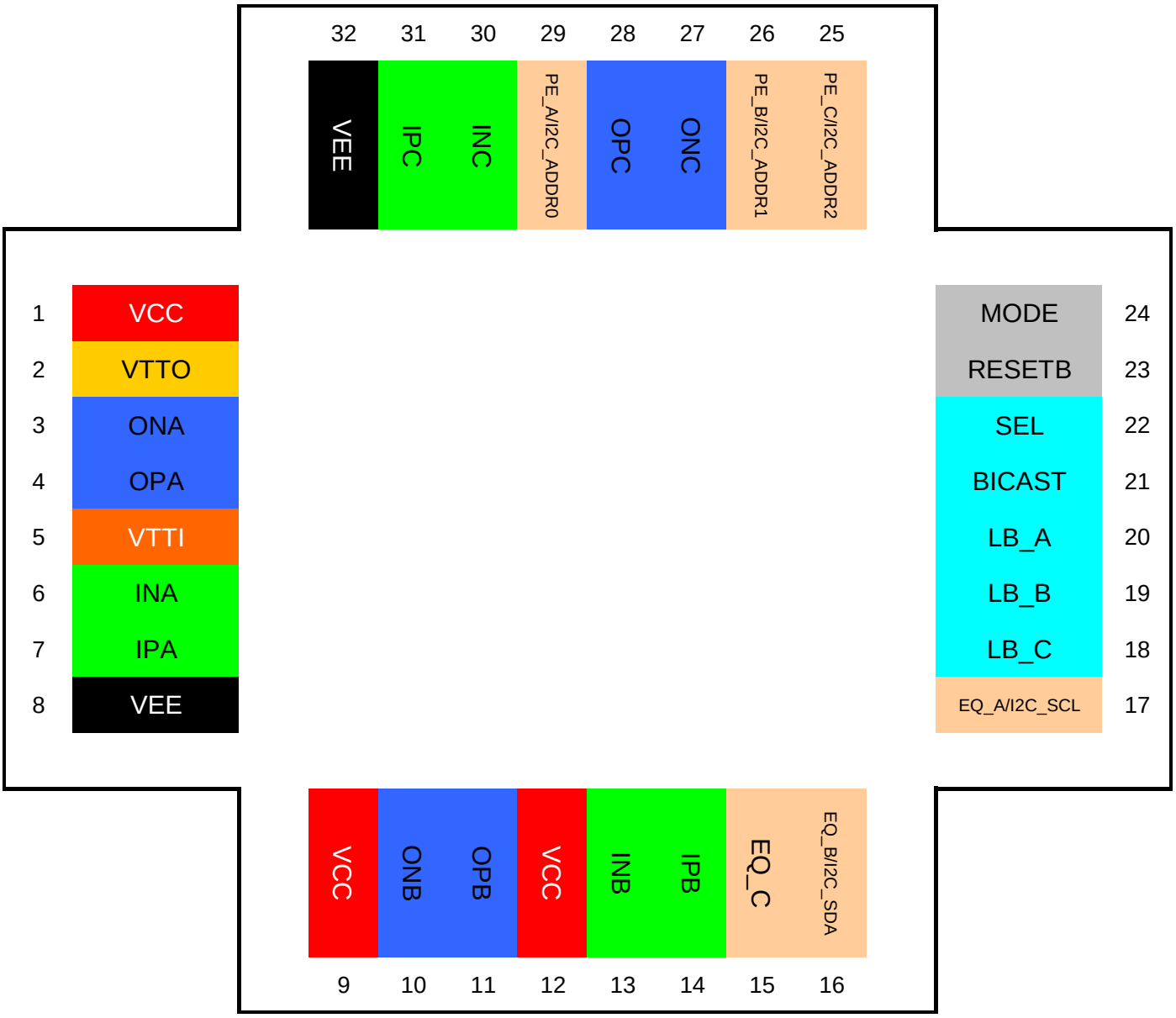


Figure 2: Pin Configuration

Table 3. Pin Function Descriptions

Pin	Mnemonic	Type	Description
1,9,12	VCC	Power	Positive Supply
2	VTTO	Power	Output termination supply
3	ONA	I/O	High speed output complement
4	OPA	I/O	High speed output
5	VTTI	Power	Input termination supply
6	INA	I/O	High speed input complement
7	IPA	I/O	High speed input
8,32	VEE	Power	Negative Supply
10	ONB	I/O	High speed output complement
11	OPB	I/O	High speed output
13	INB	I/O	High speed input complement
14	IPB	I/O	High speed input
15	EQ_C	Control	Port C input equalization control
16	EQ_B/I2C_SDA	Control	Port B input equalization control/I2C data
17	EQ_A/I2C_SCL	Control	Port A input equalization control/I2C clock
18	LB_C	Control	Port C loopback enable
19	LB_B	Control	Port B loopback enable
20	LB_A	Control	Port A loopback enable
21	BICAST	Control	Bicast enable
22	SEL	Control	A/B select
23	RESETB	Control	Configuration registers reset
24	MODE	Control	Configuration mode
25	PE_C/I2C_ADDR2	Control	Port C pre-emphasis control/I2C address bit 2
26	PE_B/I2C_ADDR1	Control	Port B pre-emphasis control/I2C address bit 1
27	ONC	I/O	High speed output complement
28	OPC	I/O	High speed output
29	PE_A/I2C_ADDR0	Control	Port A pre-emphasis control/I2C address bit 0
30	INC	I/O	High speed input complement
31	IPC	I/O	High speed output

THEORY OF OPERATION

On the demultiplexer side, the AD8153 relays received data on Input Port C to Output Port A and/or Output Port B, depending on the state of the BICAST and SEL bits. On the multiplexer side, the device relays received data on either Input Port A or Input Port B to Output Port C, depending on the state of the SEL bit.

When bicast mode is off, the outputs of either Port A or Port B are in an *idle* state. In the *idle* state, the output tail current is set to 0, and the P and N sides of the lane are pulled up to the output termination voltage through the on-chip termination resistors.

The device also supports loopback on all ports, illustrated in Figure 3. Enabling loopback on any port will override configurations set by the BICAST and SEL control bits.

Table 7 summarizes the possible device switching configurations.

INPUT EQUALIZATION (EQ) AND OUTPUT PRE-EMPHASIS (PE)

In backplane applications, the AD8153 needs to compensate for signal degradation over potentially long traces. The device supports two levels of input equalization, configured on a per-port basis. line **card.**

Table 4 summarizes the high-frequency gain boost for each control setting as well as the typical length of backplane trace that can be compensated using each setting.

The device also has four levels of output pre-emphasis, configured for each port. The pre-emphasis circuitry adds a controlled amount of overshoot to the output waveform to compensate for the high frequency loss in a backplane trace.

Tables Table 5-Table 6 summarize the high-frequency gain boost, amount of overshoot, and the typical backplane channel length (including two connectors) that can be compensated using each setting. A typical backplane is made of FR4 material with 8 mil wide trace and 8 mil spaced loosely coupled differential traces. Each channel consists of a backplane segment, two connectors, and two line cards. The total length of the channel includes 3 inches of trace on each line card.

Table 4. Input Equalization Settings

EQ_x	Boost	Typical Backplane Length
0	6 dB	0 to 20 in.
1	12 dB	20 to 40+ in.

Table 5. Output Pre-Emphasis Settings (Pin Mode)

PE_x	Boost	Overshoot	Typical Backplane Length
0	0 dB	0 %	0 to 10 in.
1	3.5 dB	35 %	20 to 30 in.

Table 6. Output Pre-Emphasis Settings (Serial Mode)

PE_x[1]	PE_x[0]	Boost	Overshoot	Typical Backplane Length
0	0	0 dB	0 %	0 to 10 in.
0	1	1.9 dB	15 %	10 to 20 in.
1	0	3.5 dB	35 %	20 to 30 in.
1	1	4.9 dB	60 %	30 to 40+ in.

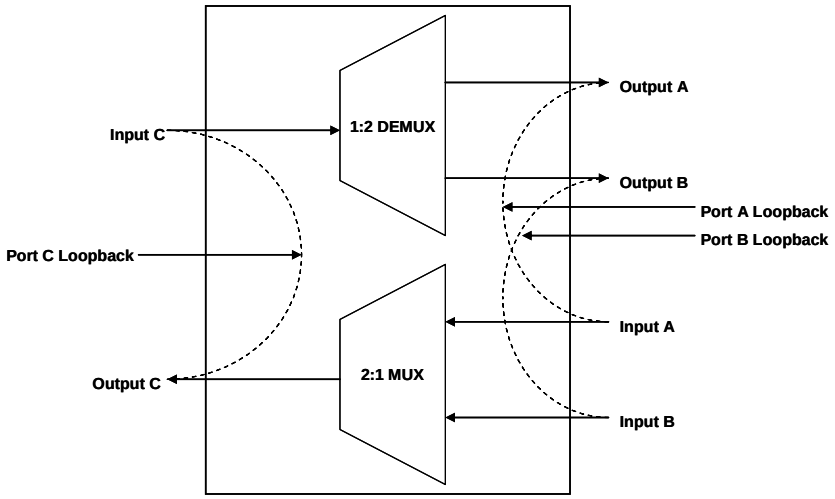


Figure 3. Loopback Configurations

Table 7. Switching Configurations

LB_A	LB_B	LB_C	SEL	BICAST	Output A	Output B	Output C
0	0	0	0	0	Input C	Idle	Input A
0	0	0	0	1	Input C	Input C	Input A
0	0	0	1	0	Idle	Input C	Input B
0	0	0	1	1	Input C	Input C	Input B
0	0	1	0	0	Input C	Idle	Input C
0	0	1	X	1	Input C	Input C	Input C
0	0	1	1	0	Idle	Input C	Input C
0	1	0	0	X	Input C	Input B	Input A
0	1	0	1	0	Idle	Input B	Input B
0	1	0	1	1	Input C	Input B	Input B
0	1	1	0	X	Input C	Input B	Input C
0	1	1	1	0	Idle	Input B	Input C
0	1	1	X	1	Input C	Input B	Input C
1	0	0	0	0	Input A	Idle	Input A
1	0	0	0	1	Input A	Input C	Input A
1	0	0	1	X	Input A	Input C	Input B
1	0	1	0	0	Input A	Idle	Input C
1	0	1	X	1	Input A	Input C	Input C
1	0	1	1	X	Input A	Input C	Input C
1	1	0	0	X	Input A	Input B	Input A
1	1	0	1	X	Input A	Input B	Input B
1	1	1	X	X	Input A	Input B	Input C

SERIAL CONTROL INTERFACE

REGISTER SET

The AD8153 can be controlled in one of three modes: pin mode, serial mode, and mixed mode. In pin mode, the AD8153 control is derived from the package pins, whereas in serial mode a set of internal registers controls the AD8153. There is also a mixed mode where switching is controlled via external pins and equalization and pre-emphasis are controlled via the internal registers. The method for writing data to and reading data from the AD8153 are described in sections 0 to 0.

The mode is controlled via the MODE pin. To set the part in pin mode, MODE should be driven low to VEE. When MODE is driven high to VCC, the part is set to serial or mixed mode.

In pin mode, all controls are derived from the external pins. In serial mode, each channel's equalization and pre-emphasis are solely controlled through the registers as described in Table 8. Additionally, further functionality is available in serial mode as each channel's output can be enabled/disabled with the Output Enable control bits, which is not possible in pin mode. In order to change the switching in the AD8153 in serial mode, the mask bits (register 0x00) must be set to 1 by writing the value 0x1F to this register as explained in the following sections. Once all the mask bits are set to 1, switching is controlled via the LB A, LB B, LB C, BICAST and SEL bits in the register set.

In mixed mode, each channel's equalization and pre-emphasis are controlled through the registers as described above. The switching, however, can be controlled using either the external pins or the internal register set. The source of the control is selected using the mask bits (0x00). If a mask bit is set to 0, the external pin acts as the source for that specific control. If a mask bit is set to 1, the associated internal register acts as the source for that specific control. As an example, if one were to set register 0x00 to the value 0x0C, the SEL and LB C controls would come from the internal register set (bit 0 of register 0x04 and bit 3 of register 0x03 respectively), and BICAST, LB A and LB B controls would come from the external pins.

Table 8: Register Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
00000000 (0x00)				BICAST MASK	SEL MASK	LB_C MASK	LB_B MASK	LB_A MASK	00000000 (0x00)
00000001 (0x01)				OUTPUT ENABLE A	LB A	EQ A	PE A [1]	PE A [0]	00010000 (0x10)
00000010 (0x02)				OUTPUT ENABLE B	LB B	EQ B	PE B [1]	PE B [0]	00010000 (0x10)
00000011 (0x03)				OUTPUT ENABLE C	LB C	EQ C	PE C [1]	PE C [0]	00010000 (0x10)
0000100 (0x04)							BICAST	SEL	00000000 (0x00)

GENERAL FUNCTIONALITY

The AD8153 register set is controlled through a two-wire I²C interface. The AD8153 acts only as an I²C slave device. Therefore, the I²C bus in the system needs to include an I²C master in order to configure the AD8153 and other I²C devices that may be on the bus. Data transfers are controlled through the use of the two I²C wires: the SCL input clock pin and the SDA bi-directional data pin. In order to set the AD8153 part in I²C Mode the MODE input needs to be set high to VCC.

The AD8153 I²C interface can be run in the standard (100 kHz) and fast (400 kHz) modes. The SDA line only changes value when the SCL pin is low with two exceptions. In order to indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high, and in order to indicate the end of a transfer, the SDA line is driven high while the SCL line is high. Therefore, it is important to control the SCL clock to only toggle when the SDA line is stable unless indicating a *start*, *repeated start* or *stop* condition.

I²C DATA WRITE

In order to write data to the AD8153 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the AD8153 slave device. The steps that need to be followed are listed below, where the signals are controlled by the I²C master unless otherwise specified. A diagram of the procedure can be seen in Figure 4.

1. Send a start condition (while holding the SCL line high, pull the SDA line low)
2. Send the AD8153 part address (7 bits) whose upper 4 bits are the static value b1001 and whose lower 3 bits are controlled by the input pins I2C_ADDR[2:0]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8153 to acknowledge the request.
5. Send the register address (8 bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the AD8153 to acknowledge the request.
7. Send the data (8 bits) to be written to the register whose address was set in step 5. This transfer should be MSB first.
8. Wait for the AD8153 to acknowledge the request.

9a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.

9b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with step 2 in this procedure to perform another write.

9c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with step 2 of the read procedure (in the next section) to perform a read from a another address.

9d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with step 8 of the read procedure (in the next section) to perform a read from the same address set in step 5.

In Figure 4, the AD8153 write process is shown. The SCL signal is shown along with a general write operation and a specific example. In the example, data 0x92 is written to address 0x6D of an AD8153 part with a part address of 0x4B. The part address is 7 bits wide and is composed of the AD8153 static upper 4 bits (b1001) and the pin programmable lower 3 bits (I2C_ADDR[2:0]). In this example, the I2C_ADDR bits are set to b011. In the figure, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the AD8153 slave. As for the SDA line, the data in the shaded polygons is driven by the AD8153, whereas the data in the non-shaded polygons is driven by the I²C master. The end phase case shown is that of 9a.

It is important to note that the SDA line only changes when the SCL line is low, except for the case of sending a *start*, *stop*, or *repeated start* condition, steps 1 and 9 in this case.

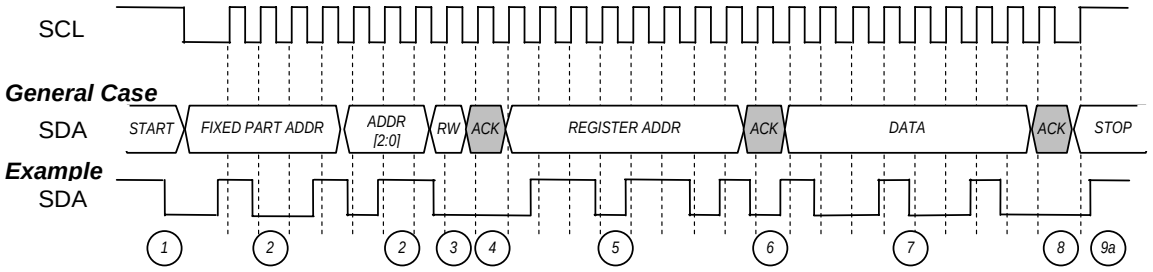


Figure 4: I²C Write Diagram

I²C DATA READ

To read data from the AD8153 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the AD8153 slave device. The steps that need to be followed are listed below, where the signals are controlled by the I²C master unless otherwise specified. A diagram of the procedure can be seen in Figure 5.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the AD8153 part address (7 bits) whose upper 4 bits are the static value b1001 and whose lower 3 bits are controlled by the input pins I2C_ADDR[2:0]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8153 to acknowledge the request.

5. Send the register address (8 bits) from which data is to be read. This transfer should be MSB first. The register address will be kept in memory in the AD8153 until the part is reset or the register address is written over with the same procedure (steps 1-6).
6. Wait for the AD8153 to acknowledge the request.
7. Send a repeated start condition (while holding the SCL line high, pull the SDA line low).
8. Send the AD8153 part address (7 bits) whose upper 4 bits are the static value b1001 and whose lower 3 bits are controlled by the input pins I2C_ADDR[1:0]. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the AD8153 to acknowledge the request.
11. The AD8153 will then serially transfer the data (8 bits) held in the register indicated by the address set in step 5.
12. Acknowledge the data.

13a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.

13b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with step 2 of the write procedure (previous section) to perform a write.

13c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with step 2 of this procedure to perform a read from a another address.

13d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with step 8 of this procedure to perform a read from the same address.

In Figure 5, the AD8153 read process is shown. The SCL signal is shown along with a general read operation and a specific example. In the example, data 0x49 is read from address 0x6D of an AD8153 part with a part address of 0x4B. The part address is 7 bits wide and is composed of the AD8153 static upper 4 bits (b1001) and the pin programmable lower 3 bits (I2C_ADDR[2:0]). In this example, the I2C_ADDR bits are set to b011. In the figure, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I^2C master and never by the AD8153 slave. As for the SDA line, the data in the shaded polygons is driven by the AD8153, whereas the data in the non-shaded polygons is driven by the I^2C master. The end phase case shown is that of 13a.

It is important to note that the SDA line only changes when the SCL line is low, except for the case of sending a *start*, *stop*, or *repeated start* condition, as in steps 1, 7, and 13. In Figure 5, A is the same as ACK in Figure 4. Equally, Sr represents a repeated start where the SDA line is brought high before SCL is raised. SDA is then dropped while SCL is still high.

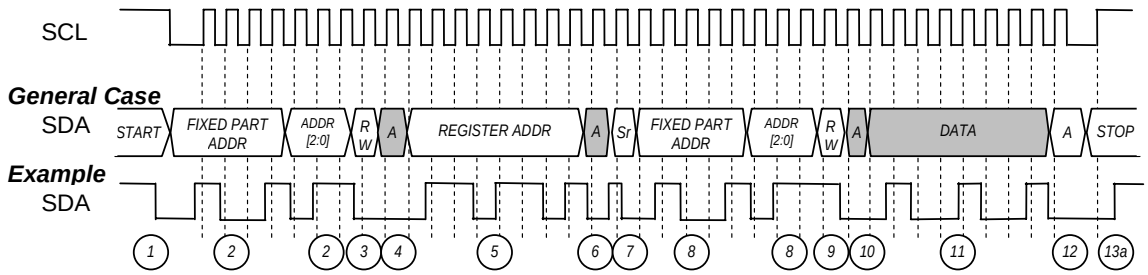


Figure 5: I^2C Read Diagram

I^2C TIMING SPECIFICATIONS

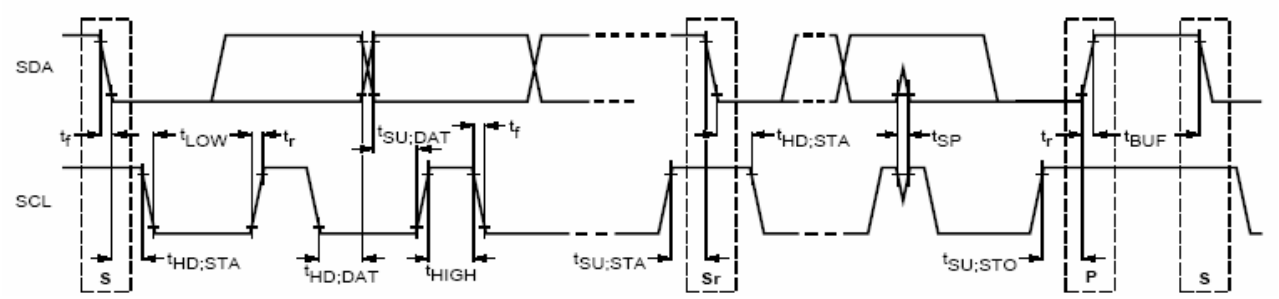


Figure 6: I²C Timing Diagram

Table 9: I²C Timing Parameters

Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400+	kHz
Hold time for a *start* condition	$t_{HD;STA}$	0.6	-	µs
Set-up time for a *repeated start* condition	$t_{SU;STA}$	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	µs
Data hold time	$t_{HD;DAT}$	0	-	µs
Data set-up time	$t_{SU;DAT}$	10	-	Ns
Rise time for both SDA and SCL	t_r	1	300	Ns
Fall time for both SDA and SCL	t_f	1	300	Ns
Set-up time for *stop* condition	$t_{SU;STO}$	0.6	-	µs
Bus free time between a *stop* and a *start* condition	t_{BUF}	1	-	Ns
Capacitance for each I/O pin	C_i	5	7	Pf

APPLICATIONS

The main application of the AD8153 is to support redundancy on both the backplane side and the line interface side of a serial link. Figure 7 illustrates redundancy in a typical backplane system. Each line card is connected to two switch fabrics (primary and redundant). The device can be configured to support either 1 + 1 or 1:1 redundancy.

Another application for the AD8153 is in test equipment for evaluating high speed serial links. Figure 9 illustrates a possible application of the AD8153 in a simple link tester.

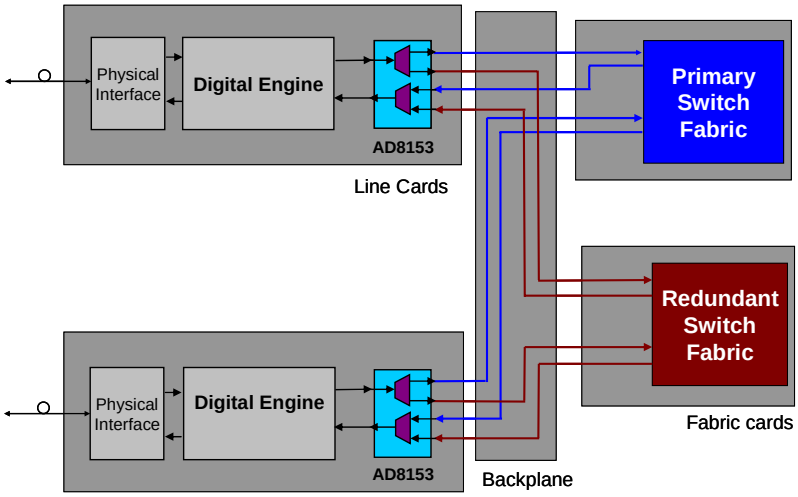


Figure 7. Switch Redundancy Application

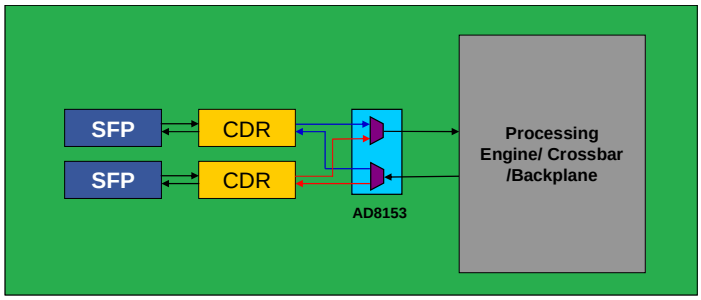


Figure 8. Line Interface Redundancy Application

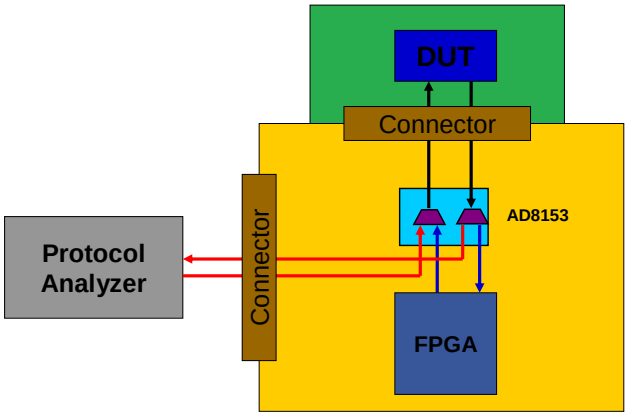
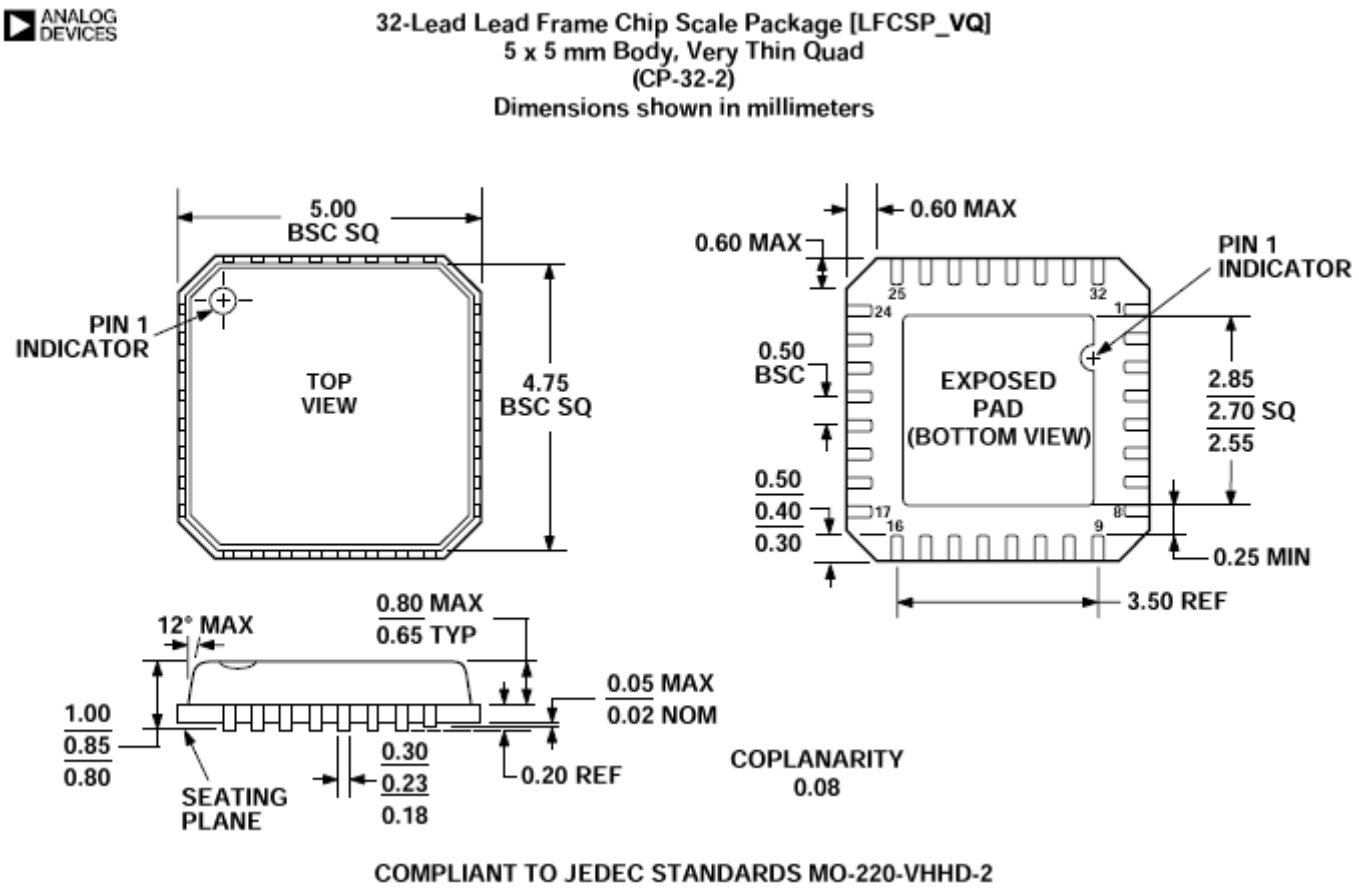


Figure 9. Test Equipment Application

OUTLINE DIMENSIONS



Notes

The 8153 has a conductive heat slug to help dissipate heat and ensure reliable operation of the device over the full industrial temperature range. The slug is exposed on the bottom of the package and is electrically connected to V_{EE}. It is recommended that no PCB signal traces or vias be located under the package that could come into contact with the slug.

Figure 10. 32-Lead QFN, Exposed Paddle
Dimensions shown in millimeters

NOTES

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