ANALOG DEVICES

2 GHz Ultralow Distortion Differential RF/IF Amplifier

AD8352

FEATURES

- −3 dB bandwidth of 2.2 GHz (A_V = 10 dB)
- Single resistor gain adjust 3 dB ≤ A_V ≤ 21 dB
- Single resistor and capacitor distortion adjust
- Input resistance 3 kΩ, independent of gain (A_V)
- Differential or single-ended input to differential output
- Low noise input stage 2.7 nV/√Hz RTI @ A_V = 10 dB
- Low broadband distortion
  - 10 MHz: −86 dBc HD2, −82 dBc HD3
  - 70 MHz: −84 dBc HD2, −82 dBc HD3
  - 190 MHz: −81 dBc HD2, −87 dBc HD3
- OIP3 of 41 dBm @ 150 MHz
- Slew rate 8 V/ns
- Fast settling and overdrive recovery of 2 ns
- Single-supply operation: 3 V to 5.0 V
- Low power dissipation: 37 mA @ 5 V
- Power down capability: 5 mA @ 5 V
- Fabricated using the high speed XFCB3 SiGe process

APPLICATIONS

- Differential ADC drivers
  - Single-ended to differential conversion
  - RF/IF gain blocks
  - SAW filter interfacing

FUNCTIONAL BLOCK DIAGRAM

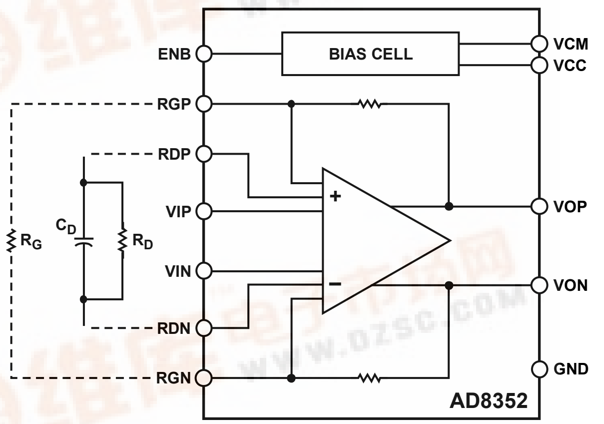

Figure 1.

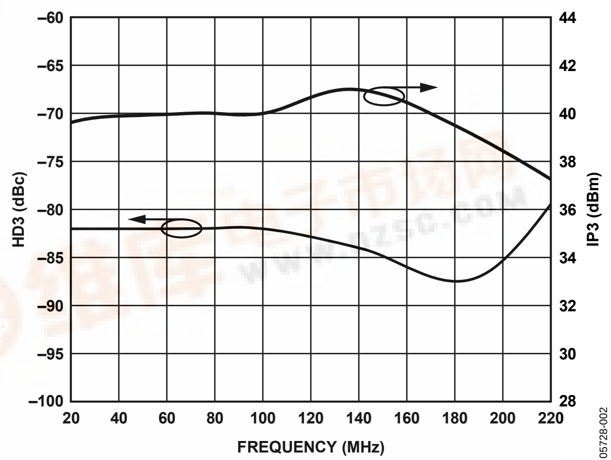

Figure 2. IP3 and Third Harmonic Distortion vs. Frequency, Measured Differentially

GENERAL DESCRIPTION

The AD8352 is a high performance differential amplifier optimized for RF and IF applications. It achieves better than 80 dB SFDR performance at frequencies up to 200 MHz, and 65 dB beyond 500 MHz, making it an ideal driver for high speed 12- to 16-bit analog-to-digital converters (ADCs).

Unlike other wideband differential amplifiers, the AD8352 has buffers that isolate the Gain Setting Resistor R_G from the signal inputs. As a result, the AD8352 maintains a constant 3 kΩ input resistance for gains of 3 dB to 24 dB, easing matching and input drive requirements. The AD8352 has a nominal 100 Ω differential output resistance.

The device is optimized for wide band, low distortion performance at frequencies beyond 500 MHz. These attributes, together with its wide gain adjust capability, make this device the amplifier of choice for general-purpose IF and broadband applications where low distortion, noise, and power are critical. In particular, it is ideally suited for driving not only ADCs, but also mixers, pin diode attenuators, SAW filters, and multielement discrete devices. The device comes in a compact 3 mm × 3 mm, 16-lead LFCSP package and operates over a temperature range of −40°C to +85°C.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

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REVISION HISTORY

1/06—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, R_L = 200 Ω differential, R_G = 118 Ω (A_V = 10 dB), *f* = 100 MHz, T = 25°C; parameters specified differentially (in/out), unless otherwise noted. C_D and R_D are selected for differential broadband operation (see Table 6 and Table 7).

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	A_V = 6 dB, V_{OUT} ≤ 1.0 V p-p		2500		MHz
	A_V = 10 dB, V_{OUT} ≤ 1.0 V p-p		2200		MHz
	A_V = 14 dB, V_{OUT} ≤ 1.0 V p-p		1800		MHz
Bandwidth for 0.1 dB Flatness	3 dB ≤ A_V ≤ 20 dB, V_{OUT} ≤ 1.0 V p-p		190		MHz
Bandwidth for 0.2 dB Flatness	3 dB ≤ A_V ≤ 20 dB, V_{OUT} ≤ 1.0 V p-p		300		MHz
Gain Accuracy	Using 1% resistor for R_G, 0 dB ≤ A_V ≤ 20 dB		±1		dB
Gain Supply Sensitivity	V_S ± 5%		.06		dB/V
Gain Temperature Sensitivity	−40°C to +85°C		4		mdB/°C
Slew Rate	R_L = 1 kΩ, V_{OUT} = 2 V step		9		V/ns
	R_L = 200 Ω, V_{OUT} = 2 V step		8		V/ns
Settling Time	2 V step to 1%		<2		ns
Overdrive Recovery Time	V_{IN} = 4 V to 0 V step, V_{OUT} ≤ ±10 mV		<3		ns
Reverse Isolation (S12)			−80		dB
INPUT/OUTPUT CHARACTERISTICS					
Common-Mode Nominal			VCC/2		V
Voltage Adjustment Range			1.2 to 3.8		V
Maximum Output Voltage Swing	1 dB compressed		6		V p-p
Output Common-Mode Offset	Referenced to VCC/2	−100		+20	mV
Output Common-Mode Drift	−40°C to +85°C		.25		mV/°C
Output Differential Offset Voltage		−20		+20	mV
CMRR			57		dB
Output Differential Offset Drift	−40°C to +85°C		.15		mV/°C
Input Bias Current			±5		μA
Input Resistance			3		kΩ
Input Capacitance (Single-Ended)			0.9		pF
Output Resistance			100		Ω
Output Capacitance			3		pF
POWER INTERFACE					
Supply Voltage		3	5	5.5	V
ENB Threshold			1.5		V
ENB Input Bias Current	ENB at 3 V		75		nA
	ENB at 0.6 V		−125		μA
Quiescent Current	ENB at 3 V	35	37	39	mA
	ENB at 0.6 V		5.3		mA

NOISE DISTORTION SPECIFICATIONS

V_S = 5 V, R_L=200 Ω differential, R_G=118 Ω (A_V = 10 dB), V_{OUT} = 2 V p-p composite, T = 25°C; parameters specified differentially, unless otherwise noted. C_D and R_D are selected for differential broadband operation (see Table 6 and Table 7).

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
10 MHz					
Second/Third Harmonic Distortion[1]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		−88/−95		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		−86/−82		dBc
Output Third-Order Intercept	R_L = 200 Ω, f_1 = 9.5 MHz, f_2 = 10.5 MHz		+38		dBm
Third-Order IMD	R_L = 1 kΩ, f_1 = 9.5 MHz, f_2 = 10.5 MHz, V_{OUT} = 2 V p-p composite		−86		dBc
	R_L = 200 Ω, f_1 = 9.5 MHz, f_2 = 10.5 MHz, V_{OUT} = 2 V p-p composite		−81		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+15.7		dBm
70 MHz					
Second/Third HarmonicDistortion[1]	R_L = 1 kΩ, R_G = 178 Ω, V_{OUT} = 2 V p-p		−83/−84		dBc
	R_L = 200 Ω, R_G = 115 Ω, V_{OUT} = 2 V p-p		−84/−82		dBc
Output Third-Order Intercept	R_L = 200 Ω f_1 = 69.5 MHz, f_2 = 70.5 MHz		+40		dBm
Third-Order IMD	R_L = 1 kΩ, f_1 = 69.5 MHz, f_2 = 70.5 MHz, V_{OUT} = 2 V p-p composite		−91		dBc
	R_L = 200 Ω, f_1 = 69.5 MHz, f_2 = 70.5 MHz, V_{OUT} = 2 V p-p composite		−83		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+15.7		dBm
100 MHz					
Second/Third Harmonic Distortion	R_L = 1 kΩ, V_{OUT} = 2 V p-p		−83/−83		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		−84/−82		dBc
Output Third-Order Intercept	R_L = 200 Ω, f_1 = 99.5 MHz, f_2 = 100.5 MHz		+40		dBm
Third-Order IMD	R_L = 1 kΩ, f_1 = 99.5 MHz, f_2 = 100.5 MHz, V_{OUT} = 2 V p-p composite		−91		dBc
	R_L = 200 Ω, f_1 = 99.5 MHz, f_2 = 100.5 MHz, V_{OUT} = 2 V p-p composite		−84		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+15.6		dBm
140 MHz					
Second/Third Harmonic Distortion[2]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		−83/−82		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		−82/−84		dBc
Output Third-Order Intercept	R_L = 200 Ω, f_1 = 139.5 MHz, f_2 = 140.5 MHz		+41		dBm
Third-Order IMD	R_L = 1 kΩ, f_1 = 139.5 MHz, f_2 = 140.5 MHz, V_{OUT} = 2 V p-p composite		−89		dBc
	R_L = 200 Ω, f_1 = 139.5 MHz, f_2 = 140.5 MHz, V_{OUT} = 2 V p-p composite		−85		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+15.5		dBm

[1] When using the evaluation board at frequencies below 50 MHz, replace the Output Balun T1 with a transformer such as Mini-Circuits® ADT1-1WT to obtain the low frequency balance required for differential HD2 cancellation.
[2] C_D and R_D can be optimized for broadband operation below 180 MHz. For operation above 300 MHz, C_D and R_D components are not required.

V_S = 5 V, R_L = 200 Ω differential, R_G = 118 Ω (A_V = 10 dB), V_{OUT} = 2 V p-p composite, T = 25°C; parameters specified differentially, unless otherwise noted. C_D and R_D are selected for differential broadband operation (see Table 6 and Table 7). See the Applications section for single-ended to differential performance characteristics.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
190 MHz					
Second/Third Harmonic Distortion[1]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		−82/−85		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		−81/−87		dBc
Output Third-Order Intercept	R_L = 200 Ω, f_1 = 180.5 MHz, f_2 = 190.5 MHz		+39		dBm
Third-Order IMD	R_L = 1 kΩ, f_1 = 180.5 MHz, f_2 = 190.5 MHz, V_{OUT} = 2 V p-p composite		−83		dBc
	R_L = 200 Ω, f_1 = 180.5 MHz, f_2 = 190.5 MHz, V_{OUT} = 2 V p-p composite		−81		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+15.4		dBm
240 MHz					
Second/Third Harmonic Distortion[1]	R_L = 1 kΩ, V_{OUT} = 2 V p-p		−82/−76		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		−80/−73		dBc
Output Third-Order Intercept	R_L = 200 Ω, f_1 = 239.5 MHz, f_2 = 240.5 MHz		+36		dBm
Third-Order IMD	R_L = 1 kΩ, f_1 = 239.5 MHz, f_2 = 240.5 MHz, V_{OUT} = 2 V p-p composite		−85		dBc
	R_L = 200 Ω, f_1 = 239.5 MHz, f_2 = 240.5 MHz, V_{OUT} = 2 V p-p composite		−77		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+15.3		dBm
380 MHz					
Second/Third Harmonic Distortion	R_L = 1 kΩ, V_{OUT} = 2 V p-p		−72/−68		dBc
	R_L = 200 Ω, V_{OUT} = 2 V p-p		−74/−69		dBc
Output Third-Order Intercept	R_L = 200 Ω, f_1 = 379.5 MHz, f_2 = 380.5 MHz		+33		dBm
Third-Order IMD	R_L = 1 kΩ, f_1 = 379.5 MHz, f_2 = 380.5 MHz, V_{OUT} = 2 V p-p composite		−74		dBc
	R_L = 200 Ω, f_1 = 379.5 MHz, f_2 = 380.5 MHz, V_{OUT} = 2 V p-p composite		−70		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+14.6		dBm
500 MHz					
Second/Third Harmonic Distortion[2]	R_L = 200 Ω, V_{OUT} = 2 V p-p		−71/−64		dBc
Output Third-Order Intercept	R_L = 200 Ω, f_1 = 499.5 MHz, f_2 = 500.5 MHz		+28		dBm
Third-Order IMD	R_L = 200 Ω, f_1 = 499.5 MHz, f_2 = 500.5 MHz, V_{OUT} = 2 V p-p composite		−61		dBc
Noise Spectral Density (RTI)			+2.7		nV/√Hz
1 dB Compression Point (RTO)			+13.9		dBm

[1] When using the evaluation board at frequencies below 50 MHz, replace the Output Balun T1 with a transformer such as Mini-Circuits ADT1-1WT to obtain the low frequency balance required for differential HD2 cancellation.

[2] C_D and R_D can be optimized for broadband operation below 180 MHz. For operation above 300 MHz, C_D and R_D components are not required.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage VCC	5.5 V
VIP, VIN	±5 V
Internal Power Dissipation	210 mW
θ_{JA}	91.4°C/W
Maximum Junction Temperature	104°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

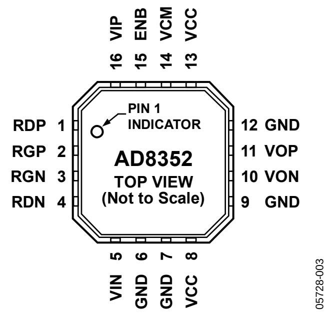


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RDP	Positive Distortion Adjust.
2	RGP	Positive Gain Adjust.
3	RGN	Negative Gain Adjust.
4	RDN	Negative Distortion Adjust.
5	VIN	Balanced Differential Input. Biased to VCM, typically ac-coupled.
6, 7, 9, 12	GND	Ground. Connect to low impedance GND.
8, 13	VCC	Positive Supply.
10	VON	Balanced Differential Output. Biased to VCM, typically ac-coupled.
11	VOP	Balanced Differential Output. Biased to VCM, typically ac-coupled.
14	VCM	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the input and output. Typically decoupled to ground with a 0.1 μF capacitor. With no reference applied, input and output common mode floats to midsupply = VCC/2.
15	ENB	Enable. Apply positive voltage (1.3 V < ENB < VCC) to activate device.
16	VIP	Balanced Differential Input. Biased to VCM, typically ac-coupled.

TYPICAL PERFORMANCE CHARACTERISTICS

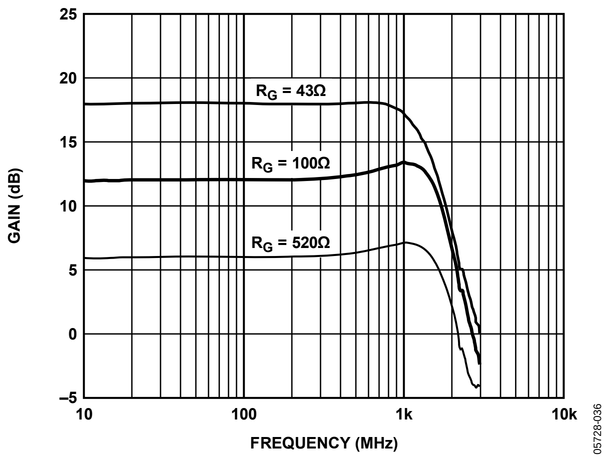


Figure 4. Gain vs. Frequency for a 200 Ω Differential Load with Baluns, A_V = 18 dB, 12 dB, and 6 dB

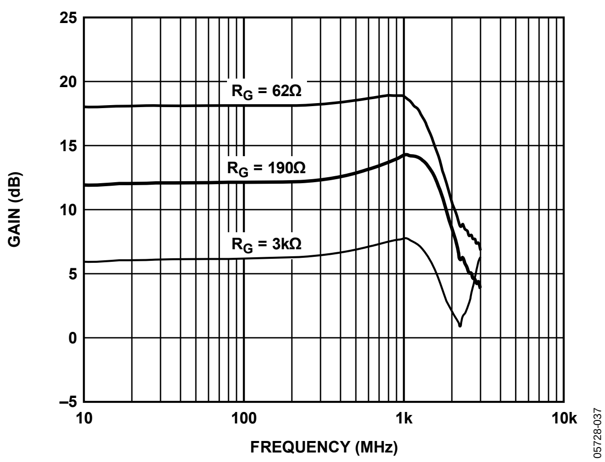


Figure 5. Gain vs. Frequency for a 1 kΩ Differential Load with Baluns, A_V = 18 dB, 12 dB, and 6 dB

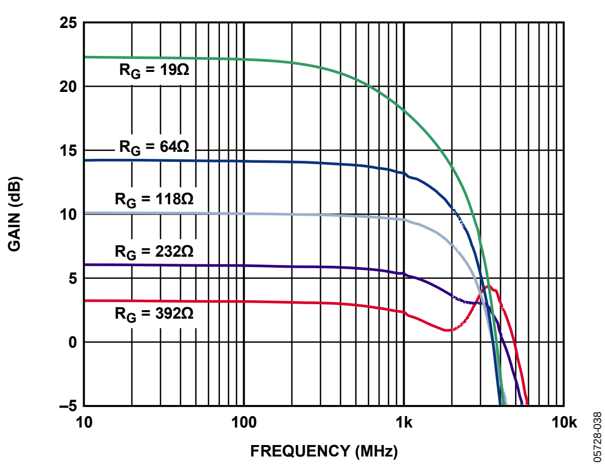


Figure 6. Gain vs. Frequency for a 200 Ω Differential Load Without Baluns, R_D/C_D Open, A_V = 22 dB, 14 dB, 10 dB, 6 dB, and 3 dB

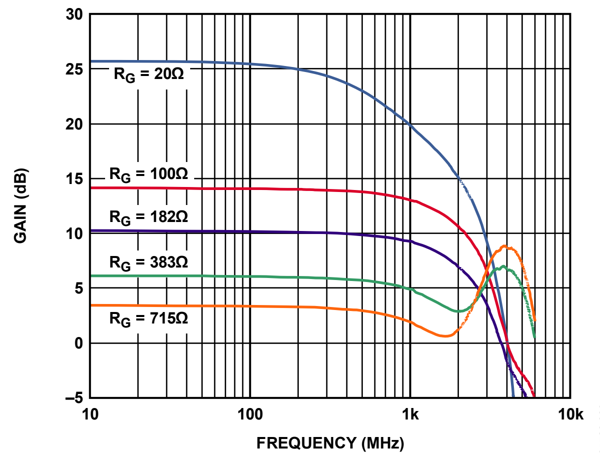


Figure 7. Gain vs. Frequency for a 1 kΩ Differential Load Without Baluns, R_D/C_D Open, A_V = 25 dB, 14 dB, 10 dB, 6 dB, and 3 dB

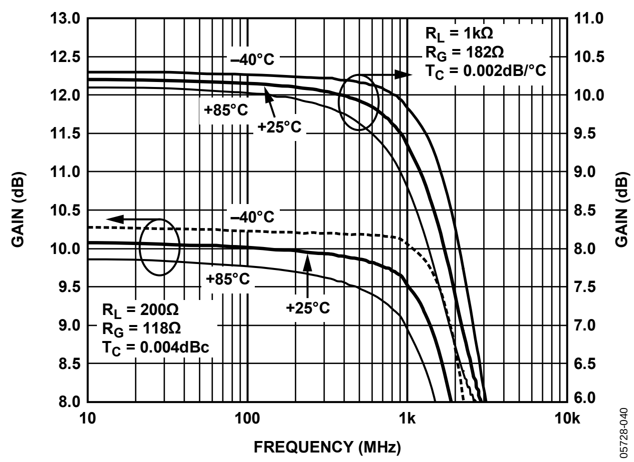


Figure 8. Gain vs. Frequency over Temperature (−40°C, +25°C, +85°C) Without Baluns, A_V = 10 dB, R_L = 200 Ω and 1 kΩ

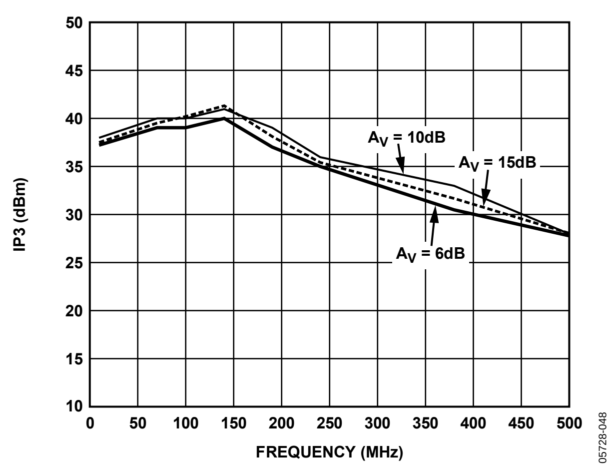


Figure 9. OIP3 vs. Frequency in dB, 2 V p-p Composite, R_L = 200 Ω A_V = 15 dB, 10 dB, and 6 dB

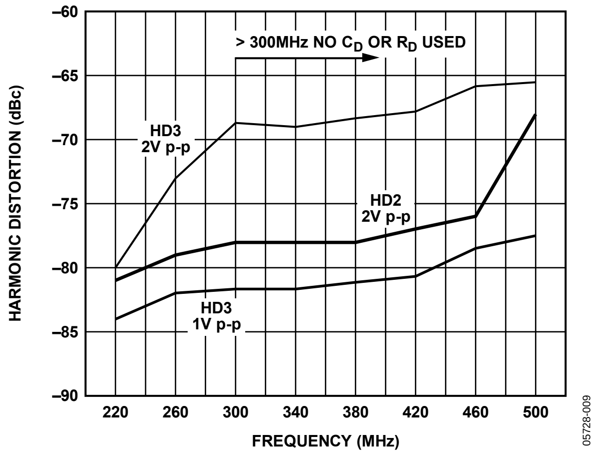


Figure 10. Third-Order Harmonic Distortion HD3 vs. Frequency, A_V = 10 dB, R_L = 200 Ω

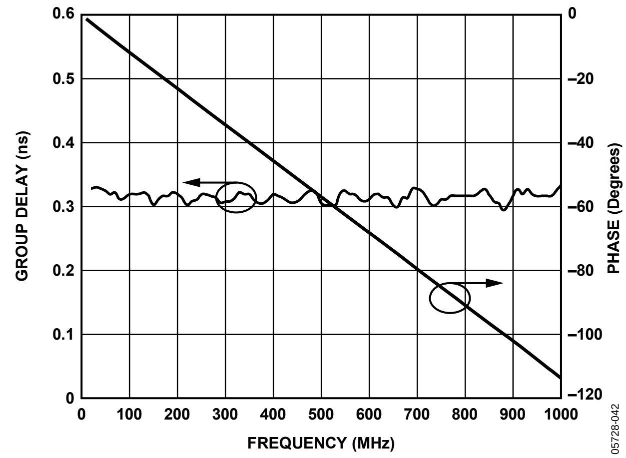


Figure 13. Phase and Group Delay vs. Frequency, A_V = 10 dB, R_L = 200 Ω

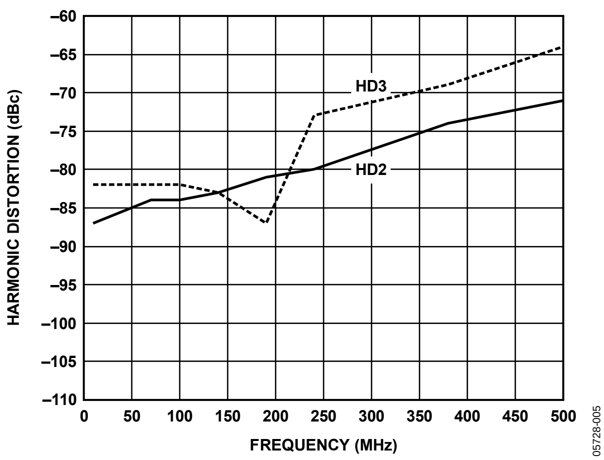


Figure 11. Harmonic Distortion vs. Frequency for 2 V p-p into R_L = 200 Ω, A_V = 10 dB, R_G = 115 Ω, R_D = 4.3 kΩ, C_D = 0.2 pF

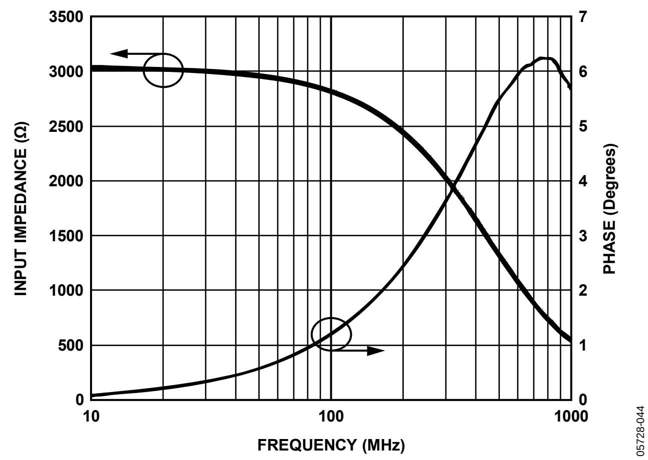


Figure 14. S11 Magnitude and Phase

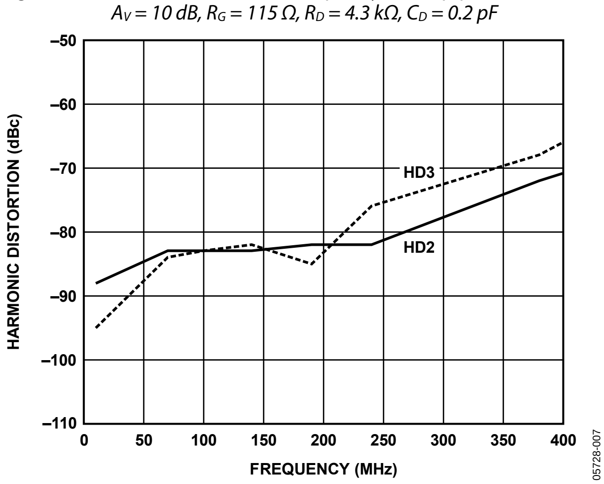


Figure 12. Harmonic Distortion vs. Frequency for 2 V p-p into R_L =1 kΩ, A_V = 10 dB, 5 V Supply, R_G = 180 Ω, R_D = 6.8 kΩ, C_D = 0.1 pF

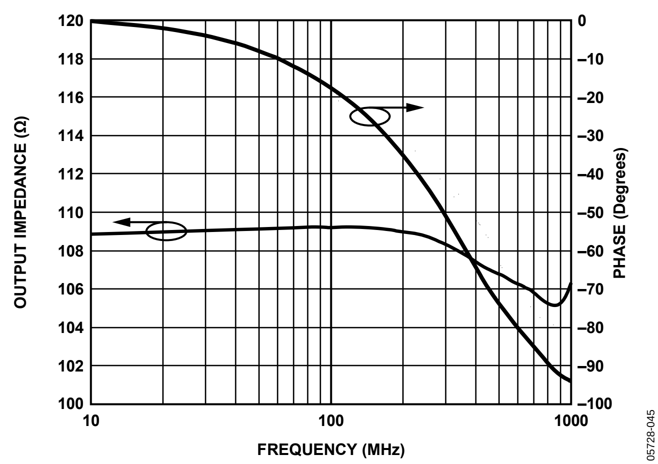


Figure 15. S22 Magnitude and Phase

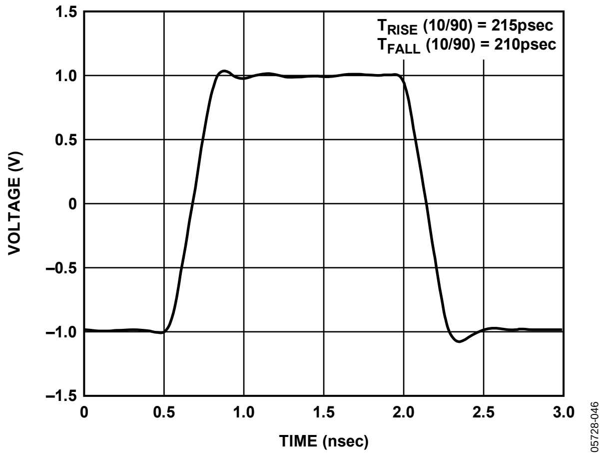


Figure 16 Large Signal Output Transient Response, R_L = 200 Ω, A_V = 10 dB

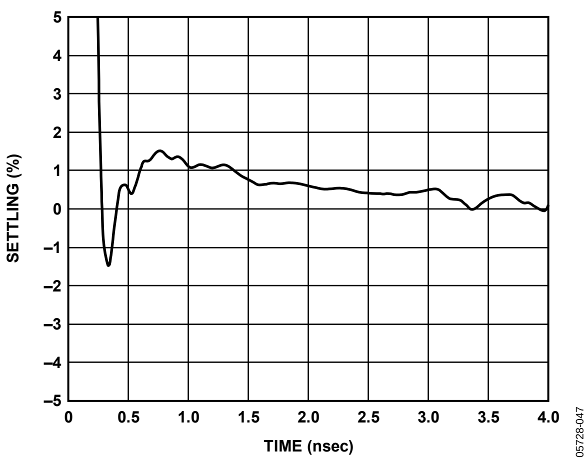


Figure 17. 1% Settling Time for a 2 V p-p Step Response, A_V = 10 dB, R_L = 200 Ω

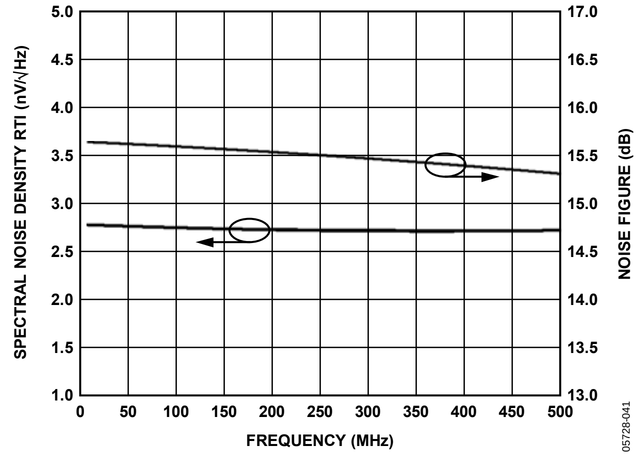


Figure 18. Noise Figure and Noise Spectral Density RTI vs. Frequency, A_V = 10 dB, R_L = 200 Ω and 1 kΩ

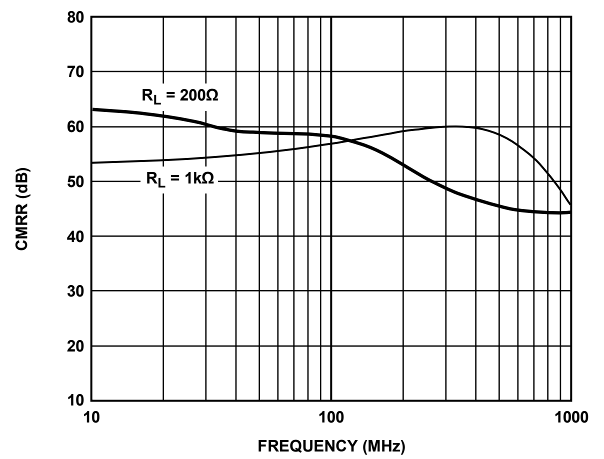


Figure 19. CMRR vs. Frequency, R_L = 200 Ω and 1 kΩ, Differential Source Resistance

APPLICATIONS

GAIN AND DISTORTION ADJUSTMENT (DIFFERENTIAL INPUT)

Table 6 and Table 7 show the required value of R_G for the gains specified at 200 Ω and 1 kΩ loads. Figure 20 and Figure 22 plot R_G vs. gain up to 18 dB for both load conditions. For other output loads (R_L), use Equation 1 to compute gain vs. R_G.

$$A_{VDifferential} = \left(\frac{R_G + 500}{(R_G + 5)(R_L + 53) + 430} \right) R_L \quad (1)$$

where:

R_L = single-ended load.
R_G = gain setting resistor.

The third-order harmonic distortion can be reduced by using external components R_D and C_D. Table 6 and Table 7 show the required values for R_D and C_D vs. the specified gains to achieve (single tone) third-order distortion reduction at 180 MHz. Figure 21 and Figure 23 show C_D vs. any gain (up to 18 dB) for 200 Ω and 1 kΩ loads, respectively. When these values are selected, they result in minimum single tone, third-order distortion at 180 MHz. This frequency point provides the best overall broadband distortion for the specified frequencies below and above this value. For applications above approximately 300 MHz, C_D and R_D are not required. See the Specifications section and third-order harmonic plots in the Typical Performance Characteristics section for more details.

C_D can be further optimized for narrow-band tuning requirements below 180 MHz that result in relatively lower third-order (in-band) intermodulation distortion terms. See the Narrow-Band, Third-Order Intermodulation Cancellation section for more information. Though not shown, single tone, third-order optimization can also be improved for narrow-band frequency applications below 180 MHz with the proper selection of C_D, and 3 dB to 6 dB of relative third-order improvement can be realized at frequencies below approximately 140 MHz.

Using the information listed in Table 6 and Table 7, an extrapolated value for R_D can be determined for loads between 200 Ω and 1 kΩ. For loads above 1 kΩ, use the 1 kΩ R_D values listed in Table 7.

Table 6. Broadband Selection of R_G, C_D, and R_D: 200 Ω Load

A_V (dB)	R_G (Ω)	C_D (pF)	R_D (kΩ)
3	390	0 (DNP)	6.8
6	220	0 (DNP)	4.3
9	140	0.1	4.3
10	115	0.2	4.3
12	86	0.3	4.3
15	56	0.6	4.3
18	35	1	4.3

Table 7. Broadband Selection of R_G, C_D, and R_D: 1 kΩ Load

A_V (dB)	R_G (Ω)	C_D (pF)	R_D (kΩ)
3	750	0 (DNP)	6.8
6	360	0 (DNP)	6.8
9	210	0 (DNP)	6.8
10	180	0.05	6.8
12	130	0.1	6.8
15	82	0.3	6.8
18	54	0.5	6.8

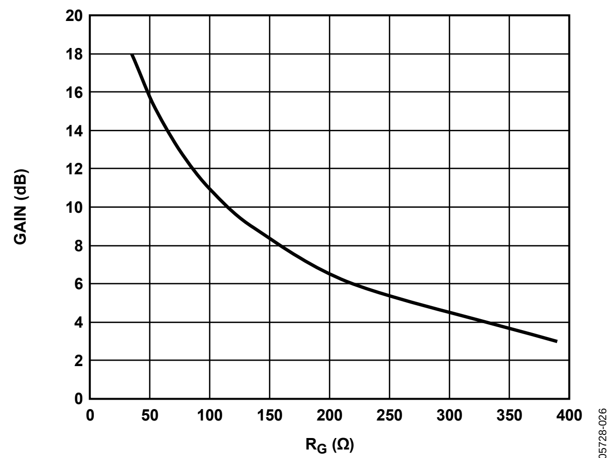


Figure 20. R_G vs. Gain, R_L = 200 Ω

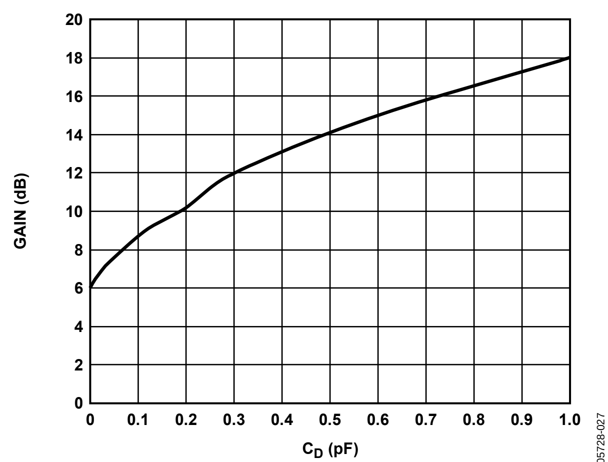


Figure 21. C_D vs. Gain, R_L = 200 Ω

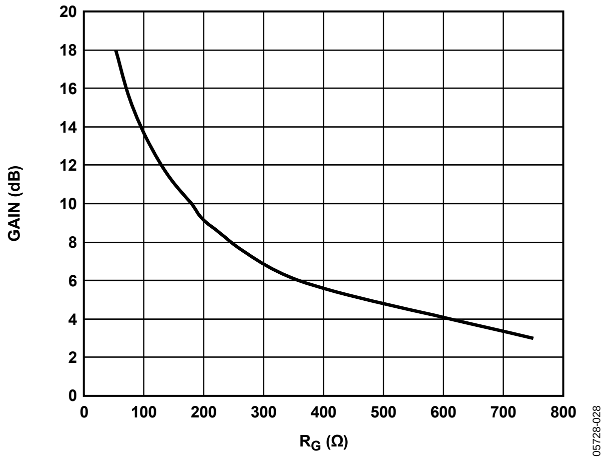


Figure 22. R_G vs. Gain, R_L = 1 kΩ

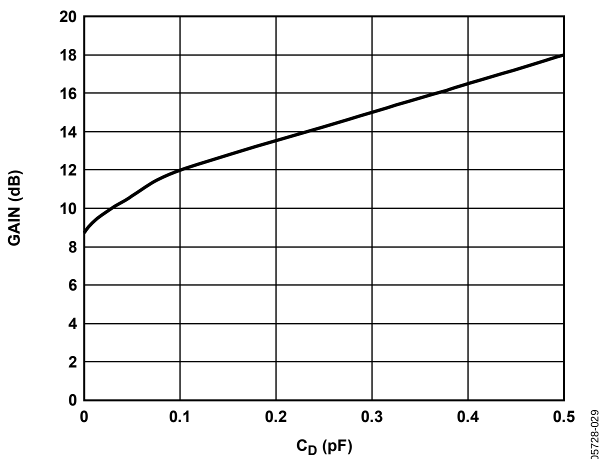


Figure 23. C_D vs. Gain, R_L = 1 kΩ

SINGLE-ENDED INPUT OPERATION

The AD8352 can be configured as a single-ended to differential amplifier as shown in Figure 24. To balance the outputs when driving only the VIP input, an external resistor (R_N) of 200 Ω is added between VIP and RGN. See Equation 2 to determine the single-ended input gain ($A_{VSingle\text{-}ended}$) for a given R_G or R_L.

$$A_{VSingle-ended} = \left(\frac{R_G + 500}{(R_G + 5)(R_L + 53) + 430} \right) R_L + \frac{R_L}{R_L + 30} \quad (2)$$

where:

R_L = single-ended load.

R_G = gain setting resistor.

Figure 25 plots gain vs. R_G for 200 Ω and 1 kΩ loads. Table 8 and Table 9 show the values of C_D and R_D required (for 180 MHz broadband third-order, single tone optimization) for 200 Ω and 1 kΩ loads, respectively. This single-ended configuration provides −3 dB bandwidths similar to input differential drive. Figure 26 through Figure 28 show distortion levels at a gain of 12 dB for both 200 Ω and 1 kΩ loads. Gains from 3 dB to 18 dB, using optimized C_D and R_D values, obtain similar distortion levels.

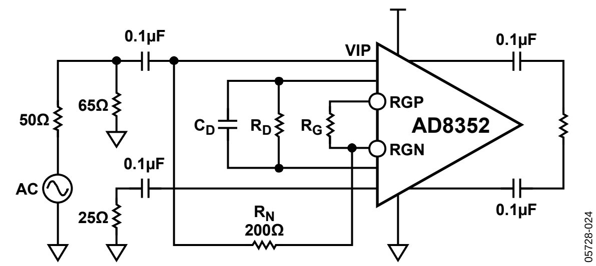


Figure 24. Single-Ended Schematic

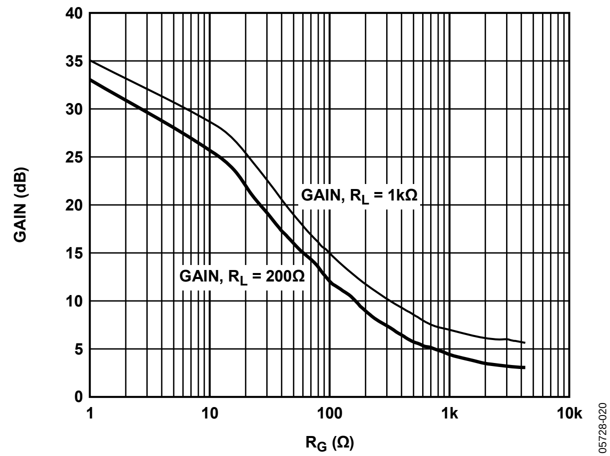


Figure 25. Gain vs. R_G

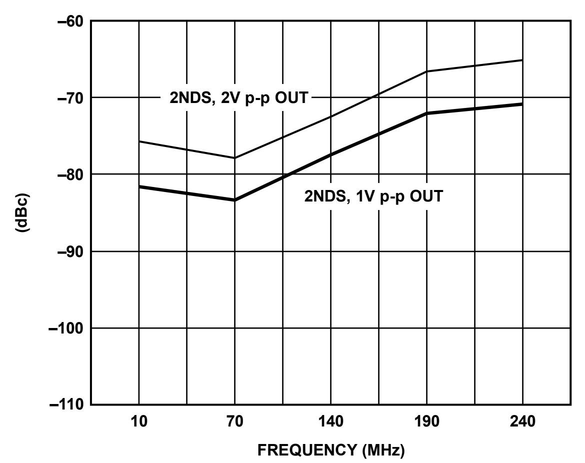


Figure 26. Single-Ended, Second-Order Harmonic Distortion, 200 Ω Load

This broadband optimization was also performed at 180 MHz. As with differential input drive, the resulting distortion levels at lower frequencies are based on the C_D and R_D specified in Table 8 and Table 9. As with differential input drive, relative third-order reduction improvement at frequencies below 140 MHz are realized with proper selection of C_D and R_D.

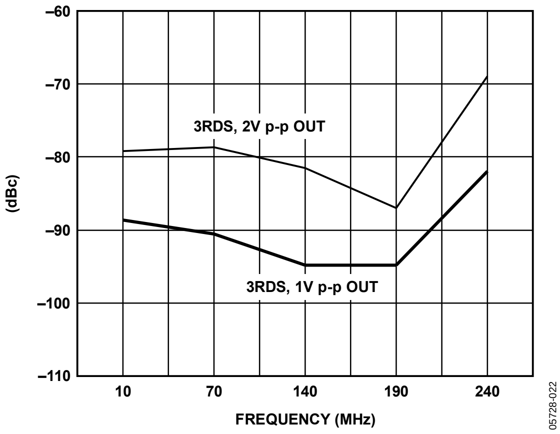


Figure 27. Single-Ended, Third-Order Harmonic Distortion, 200 Ω Load

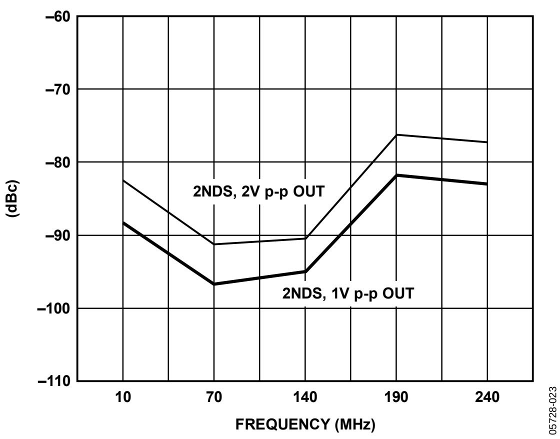


Figure 28. Single-Ended, Second-Order Harmonic Distortion, 1 kΩ Load

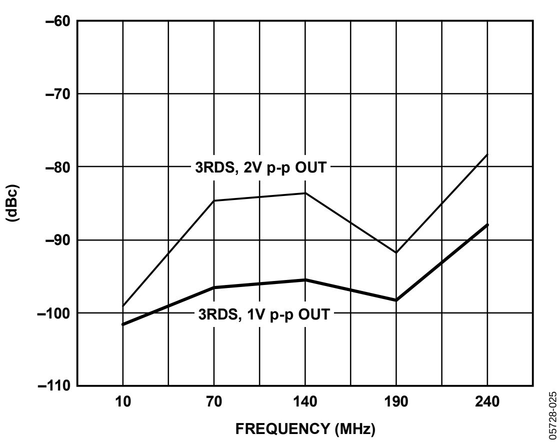


Figure 29. Single-Ended, Third-Order Harmonic Distortion, 1 kΩ Load

Table 8. Distortion Cancellation Selection Components (R_D and C_D) for Required Gain, 200 Ω Load

A_V (dB)	R_G (Ω)	C_D (pF)	R_D (kΩ)
3	4.3 k	0 (DNP)	4.3
6	540	0 (DNP)	4.3
9	220	0.1	4.3
12	120	0.3	4.3
15	68	0.6	4.3
18	43	0.9	4.3

Table 9. Distortion Cancellation Selection Components (R_D and C_D) for Required Gain, 1 kΩ Load

A_V (dB)	R_G (Ω)	CD (pF)	R_D (kΩ)
6	3 k	0 (DNP)	4.3
9	470	0 (DNP)	4.3
12	210	0.2	4.3
15	120	0.3	4.3
18	68	0.5	4.3

NARROW-BAND, THIRD-ORDER INTERMODULATION CANCELLATION

Broadband, single tone, third-order harmonic optimization does not necessarily result in optimum (minimum) two tone, third-order intermodulation levels. The specified values for C_D and R_D in Table 6 and Table 7 were determined for minimizing broadband single tone, third-order levels.

Due to phase-related distortion coefficients, optimizing single tone, third-order distortion does not result in optimum in band ($2f_1 - f_2$ and $2f_2 - f_1$), third-order distortion levels. By proper selection of C_D (using a fixed 4.3 kΩ R_D), IP3s of better than 45 dBm are achieved. This results in degraded out-of-band, third-order frequencies ($f_2 + 2f_1$, $f_1 + 2f_2$, $3f_1$ and $3f_2$). Thus, careful frequency planning is required to determine the tradeoffs.

Figure 30 shows narrow band (2 MHz spacing) OIP3 levels optimized at 32 MHz, 70 MHz, 100 MHz, and 180 MHz using the C_D values specified in Figure 31. These four data points (the C_D value and associated IP3 levels) are extrapolated to provide close estimates of IP3 levels for any specific frequency between 30 MHz and 180 MHz. For frequencies below approximately 140 MHz, narrow-band tuning of IP3 results in relatively higher IP3s (vs. the broadband results shown in Table 2 specifications). Though not shown, frequencies below 30 MHz also result in improved IP3s when using proper values for C_D.

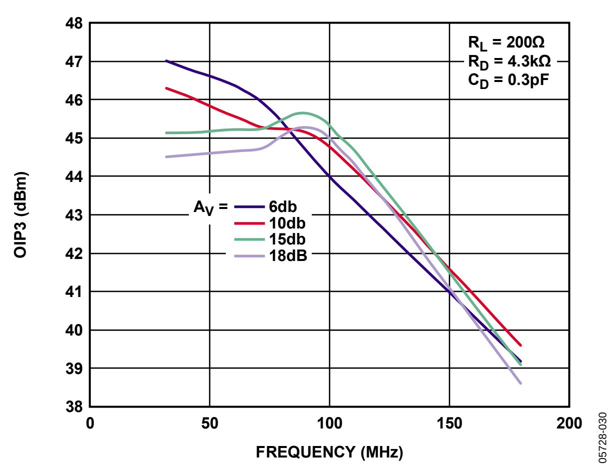


Figure 30. Third-Order Intermodulation Distortion vs. Frequency for Various Gain Settings

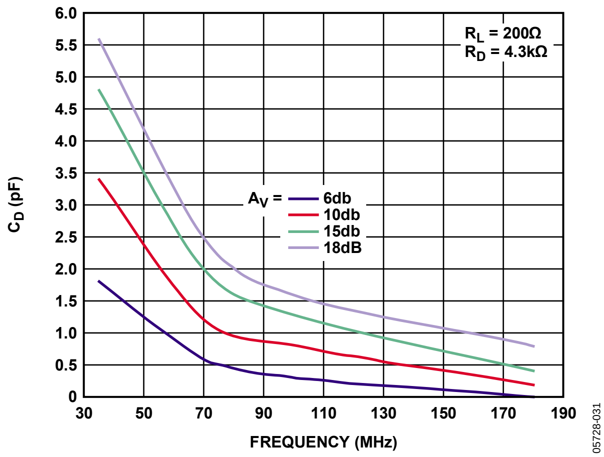


Figure 31. Narrow-Band C_D vs. Frequency for Various Gain Settings

HIGH PERFORMANCE ADC DRIVING

The AD8352 provides the gain, isolation, and balanced low distortion output levels for efficiently driving wideband ADCs such as the AD9445.

Figure 32 and Figure 33 (single and differential input drive) illustrate the typical front-end circuit interface for the AD8352 differentially driving the AD9445 14-bit ADC at 105 MSPS. The AD8352, when used in the single-ended configuration shows little or no degradation in overall third-order harmonic performance (vs. differential drive). See the Single-Ended Input Operation section. The 100 MHz FFT plots shown in Figure 34 and Figure 35 display the results for the differential configuration. Though not shown, the single-ended third-order levels are similar.

The 50 Ω resistor shown in Figure 32 provides a 50 Ω differential input impedance to the source for matching considerations. When the driver is less than one eighth of the wavelength from the AD8352, impedance matching is not required thereby negating the need for this termination resistor. The output 24 Ω resistors provide isolation from the analog-to-digital input. Refer to the Layout and Transmission Line Effects section for more information. The circuit in Figure 33 represents a single-ended input to differential output configuration for driving the AD9445. In this case, the input 50 Ω resistor with R_N (typically 200 Ω) provide the input impedance match for a 50 Ω system. Again, if input reflections are minimal, this impedance match is not required. A fixed 200 Ω resistor (R_N) is required to balance the output voltages that are required for second-order distortion cancellation. R_G is the gain-setting resistor for the AD8352 with the R_D and C_D components providing distortion cancellation. The AD9445 presents approximately 2 kΩ in parallel with 5 pF/differential load to the AD8352 and requires a 2.0 V p-p differential signal (V_{REF} = 1 V) between VIN+ and VIN− for a full-scale output operation.

These AD8352 simplified circuits provide the gain, isolation, and distortion performance necessary for efficiently driving high linearity converters such as the AD9445. This device also provides balanced outputs whether driven differentially or single-ended, thereby maintaining excellent second-order distortion levels. Though at frequencies above approximately 100 MHz, due to phase related errors, single-ended, second-order distortion is relatively higher. The output of the amplifier is ac-coupled to allow for an optimum common-mode setting at the ADC input. Input ac-coupling can be required if the source also requires a common-mode voltage that is outside the optimum range of the AD8352. A VCM common-mode pin is provided on the AD8352 that equally shifts both input and output common-mode levels. Increasing the gain of the AD8352 increases the system noise and, thus, decreases the SNR (3.5 dB at 100 MHz input for Av=10 dB) of the AD9445 when no filtering is used. Note that amplifier gains from 3 dB to 18 dB, with proper selection of C_D and R_D, do not appreciably affect distortion levels. These circuits, when configured properly, can result in SFDR performance of better than 87 dBc at 70 MHz and 82 dBc at 180 MHz input. Single-ended drive, with appropriate C_D and R_D, give similar results for SFDR and third-order intermodulation levels shown in these figures.

Placing antialiasing filters between the ADC and the amplifier is a common approach for improving overall noise and broadband distortion performance for both band-pass and low-pass applications. For high frequency filtering, matching to the filter is required. The AD8352 maintains a 100 Ω output impedance well beyond most applications and is well-suited to drive most filter configurations with little or no degradation in distortion.

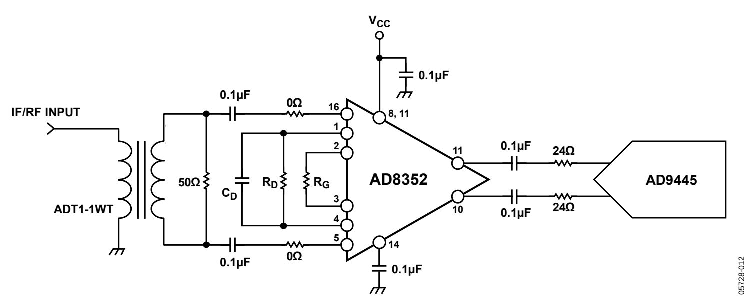


Figure 32. Differential Input to the AD8352 Driving the AD9445

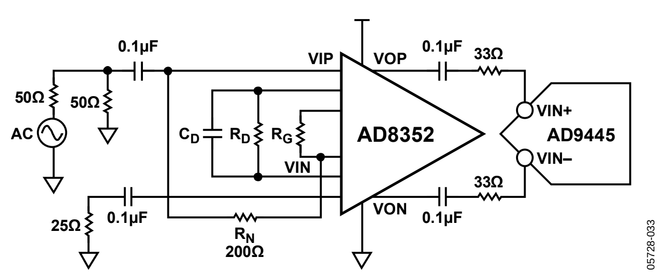


Figure 33. Single-Ended Input to the AD8352 Driving the AD9445

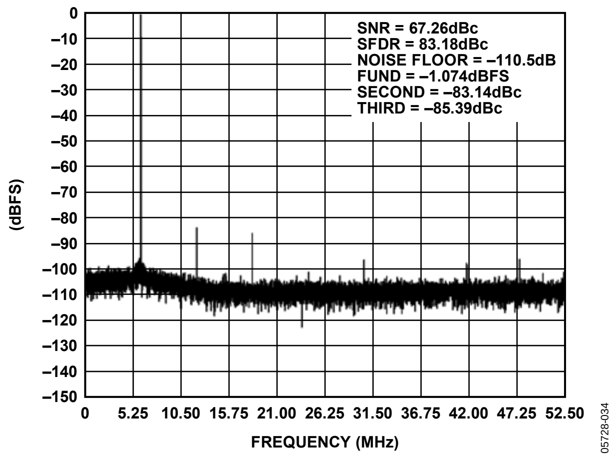


Figure 34. Single Tone Distortion AD8352 Driving AD9445, Encode Clock @ 105 MHz with Fc @ 100 MHz (A_V = 10 dB), See Figure 32

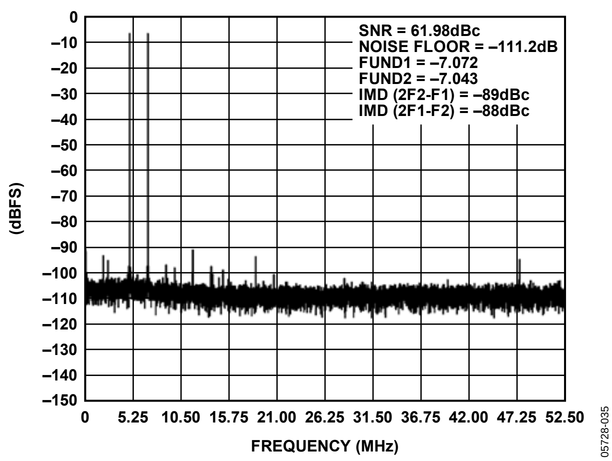


Figure 35. Two Tone Distortion AD8352 Driving AD9445, Encode Clock @ 105 MHz with Fc @ 100 MHz (A_V = 10 dB), Analog In = 98 MHz and 101 MHz, See Figure 32

LAYOUT AND TRANSMISSION LINE EFFECTS

High Q inductive drives and loads, as well as stray transmission line capacitance in combination with package parasitics, can potentially form a resonant circuit at high frequencies resulting in excessive gain peaking or possible oscillation. If RF transmission lines connecting the input or output are used, they should be designed such that stray capacitance at the I/O pins is minimized. In many board designs, the signal trace widths should be minimal where the driver/receiver is less than one-eighth of the wavelength from the AD8352. This non-transmission line configuration requires that underlying and adjacent ground and low impedance planes be far removed from the signal lines. In a similar fashion, stray capacitance should be minimized near the R_G, C_D, and R_D components and associated traces. This also requires not placing low impedance planes near these components. Refer to the evaluation board layout (Figure 37 and Figure 38) for more information. Excessive stray capacitance at these nodes results in unwanted high frequency distortion. The 0.1 µF supply decoupling capacitors need to be close to the amplifier. This includes Signal Capacitor C2 through Signal Capacitor C5.

Parasitic suppressing resistors (R5, R6, R7, and R11) can be used at the device I/O pins. Use 25 Ω series resistors (Size 0402) to adequately de-Q the input and output system from most parasitics without a significant decrease in gain. In general, if proper board layout techniques are used, the suppression resistors may not be required. Output Parasitic Suppression Resistor R7 and Output Parasitic Suppression Resistor R11 may be required for driving some switch cap ADCs. These suppressors, with Input C of the converter (and possibly added External Shunt C), help provide charge kickback isolation and improve overall distortion at high encode rates.

EVALUATION BOARD

An evaluation board is available for experimentation of various parameters such as gain, common-mode level, and distortion. The output network can be configured for different loads via minor output component changes. The schematic and evaluation board artwork are presented in Figure 36, Figure 37, and Figure 38. All discrete capacitors and resistors are Size 0402, except for C1 (3528-B).

Table 10. Evaluation Board Circuit Components and Functions

Component	Name	Function	Additional Information
Pin 8 and Pin 13	VCC	Supply VCC = +5 V.	
Pin 6, Pin 7, Pin 9, Pin 12	GND	Connect to Low Impedance GND.	
Pin 14, C9	VCM, Capacitor	Common-Mode Offset Pin. Allows for monitoring or adjustment of the output common-mode voltage. C9 is a bypass capacitor.	C9 = 0.1 µF
R_D/C_D	Distortion Tuning Components	Distortion Adjustment Components. Allows for third-order distortion adjustment HD3.	Typically, both are open above 300 MHz C_D = 0.2 pF, R_D = 4.32 kΩ C_D is Panasonic High Q (microwave) Multilayer Chip 402 capacitor
Pin 15, C8	ENB, Capacitor	Enable. Apply positive voltage (1.3 V < ENB < VCC) to activate device. Pull down to disable. Can be bypassed and float high (1.8 V) for on state. C8 is a bypass capacitor.	Floats to 1.8 V to maintain device in power-up mode C8 = 0.1 µF
R1, R2, R3, R4, R5, R6, T2, C2, C3	Resistors, Transformer, Capacitors	Input Interface. R1 and R4 ground one side of the differential drive interface for single-ended applications. T2 is a 1-to-1 impedance ratio balun to transform a single-ended input into a balanced differential signal. R2 and R3 provide a differential 50 Ω input termination. R5 and R6 can be increased to reduce gain peaking when driving from a high source impedance. The 50 Ω termination provides an insertion loss of 6 dB. C2 and C3 provide ac-coupling.	T2 = Macom™ ETC1-1-13 R1 = open, R2 = 25 Ω, R3 = 25 Ω, R4 = 0 Ω, R5 = 0 Ω, R6 = 0 Ω, C2 = 0.1 µF, C3 = 0.1 µF
R7, R8, R9, R11, R12, R13, R14, T1, C4, C5	Resistors, Transformer, Capacitors	Output Interface. R13 and R14 ground one side of the differential output interface for single-ended applications. T1 is a 1-to-1 impedance ratio balun to transform a balanced differential signal to a single-ended signal. R8, R9, and R12 are provided for generic placement of matching components. R7 and R11 allow additional output series resistance when driving capacitive loads. The evaluation board is configured to provide a 150 Ω to 50 Ω impedance transformation with an insertion loss of 11.6 dB. C4 and C5 provide ac-coupling. R7 and R11 provide additional series resistance when driving capacitive loads.	T1= Macom ETC1-1-13 R7 = 0 Ω, R8 = 86.6 Ω, R9 = 57.6 Ω, R11 = 0 Ω, R12 = 86.6 Ω, R13 = 0 Ω, R14 = open C4 = 0.1 µF, C5 = 0.1 µF
R_G	Resistor	Gain Setting Resistor. Resistor R_G is used to set the gain of the device. Refer to Table 6 and Table 7 when selecting the gain resistor.	R_G = 115 Ω (Size 0402) for a gain of 10 dB
C1, C6, C7	Capacitors	Power Supply Decoupling. The supply decoupling consists of a 10 µF capacitor to ground. C6 and C7 are bypass capacitors.	C1 = 10 µF C6, C7 = 0.1 µF
Pin 14	VCM	Common-Mode Offset Adjustment. Use Pin 14 to trim common-mode input/output levels. By applying a voltage to Pin 14, the input and output, common-mode voltage can be directly adjusted.	Typically decoupled to ground using a 0.1 µF capacitor with ac-coupled input/output ports

EVALUATION BOARD LOADING SCHEMES

The AD8352 evaluation board is characterized with two load configurations representing the most common ADC input resistance. The loads chosen are 200 Ω and 1000 Ω using a broadband resistive match. The loading can be changed via R8, R9, and R12 giving the flexibility to characterize the AD8352 evaluation board for the load in any given application. These loads are inherently lossy and thus must be accounted for in overall gain/loss for the entire evaluation board. Measure the gain of the AD8352 with an oscilloscope using the following procedure to determine the actual gain:

1. Measure the peak-to-peak voltage at the input node (C2 or C3), and
2. Measure the peak-to-peak voltage at the output node (C4 or C5), then
3. Compute gain using the formula

   $Gain = 20\log V_{OUT}/V_{IN}$

Table 11. Values Used for 200 Ω and 1000 Ω Loads

Component	200 Ω Load	1000 Ω Load
R8	86.6	487
R9	57.6	51.1
R12	86.6	487

EVALUATION BOARD SCHEMATICS

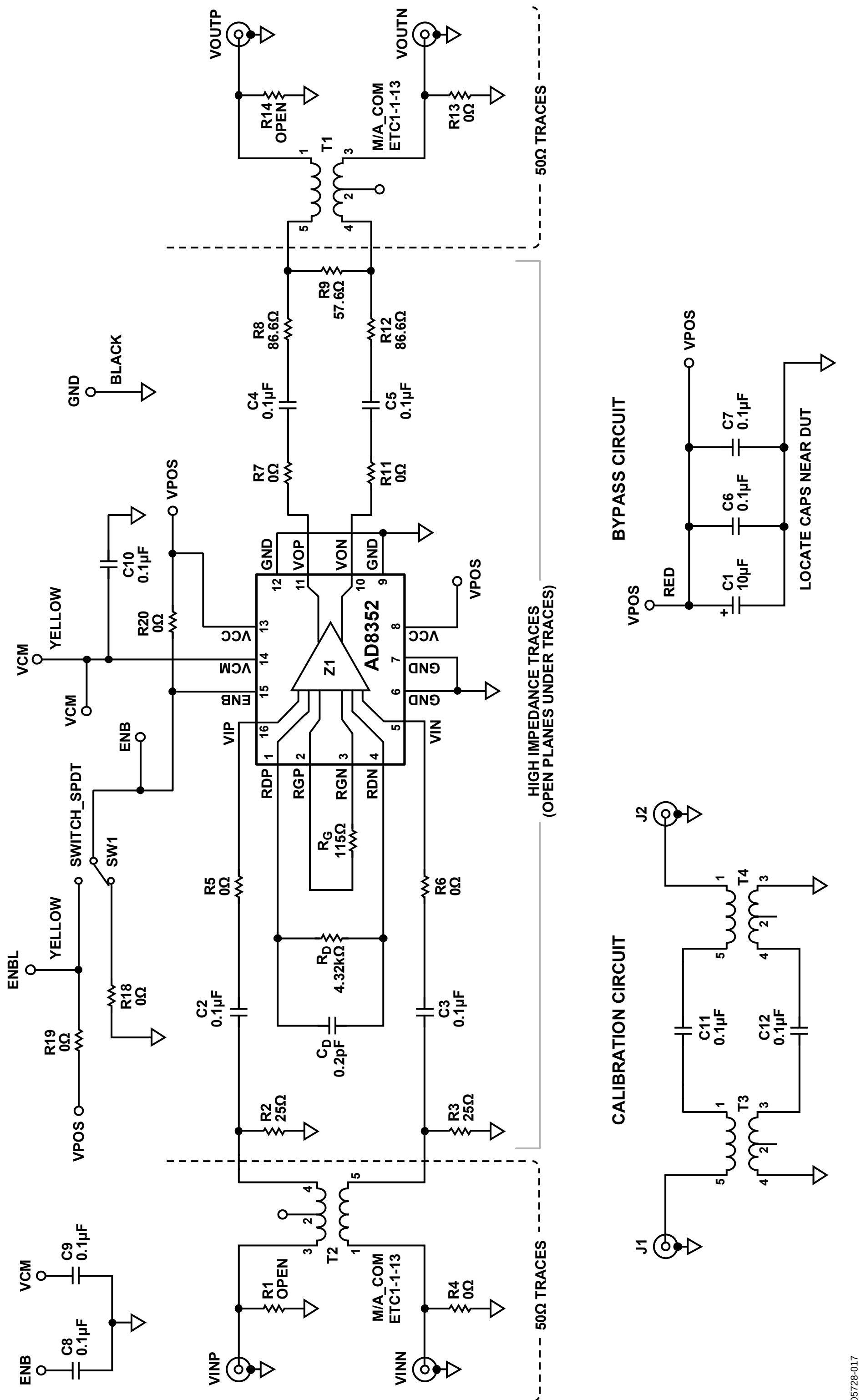


Figure 36. Preliminary Characterization Board v.A01212A

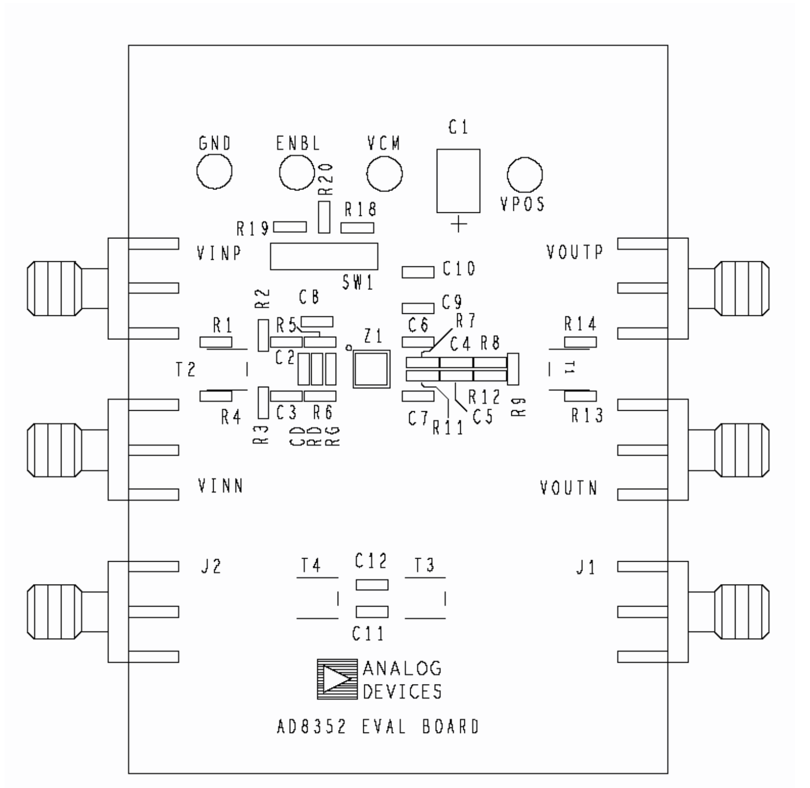


Figure 37. Component Side Silk Screen

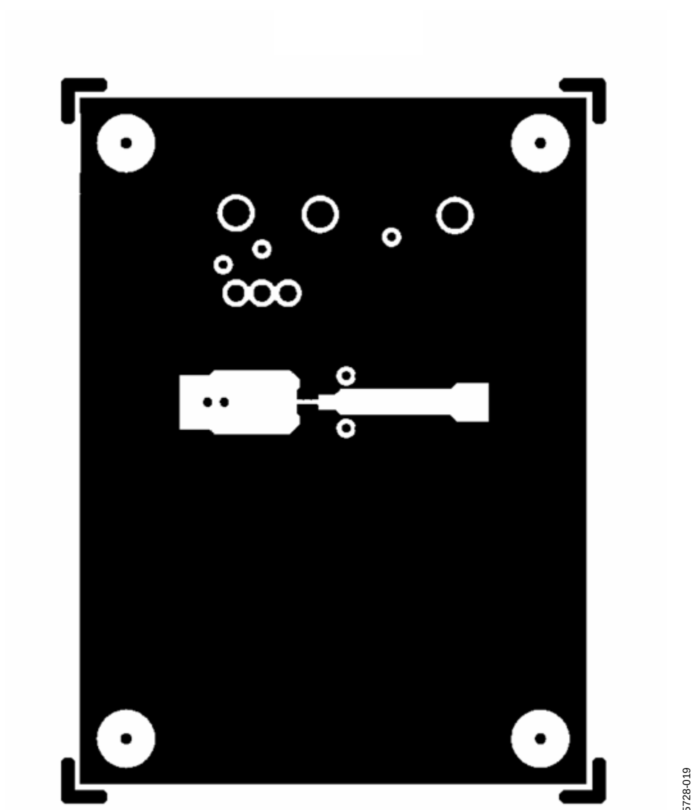
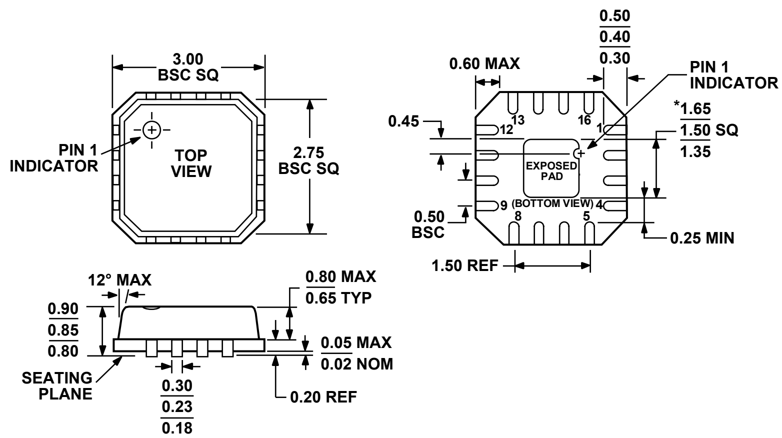


Figure 38. Far Side Showing Ground Plane Pull Back Around Critical Features

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 39. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8352ACPZ-WP[1]	–40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3
AD8352ACPZ-R7[1]	–40°C to +85°C	16-Lead LFCSP_VQ, 7" Tape and Reel	CP-16-3
AD8352-EVAL		Evaluation Board	

[1] Z = Pb-free part.