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LF to 2.7 GHz Dual 60 dB TruPwr™ Detector

AD8364

FEATURES

- RMS measurement of high crest-factor signals
- Dual-channel and channel difference outputs ports
- Integrated accurately scaled temperature sensor
- Wide dynamic range ±1 dB over 60 dB
- ±0.5 dB temperature-stable linear-in-dB response
- Low log conformance ripple
- +5 V operation at 70 mA, –40°C to +85°C
- Small footprint, 5 mm x 5 mm, LFCSP

APPLICATIONS

- Wireless infrastructure power amplifier linearization/control
- Antenna VSWR monitor
- Gain and power control and measurement
- Transmitter signal strength indication (TSSI)
- Dual-channel wireless infrastructure radios

FUNCTIONAL BLOCK DIAGRAM

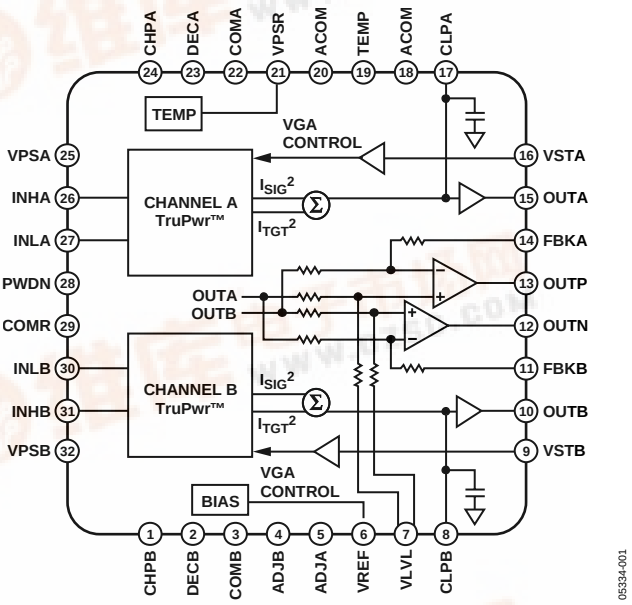

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD8364 is a true rms, responding, dual-channel RF power measurement subsystem for the precise measurement and control of signal power. The flexibility of the AD8364 allows communications systems, such as RF power amplifiers and radio transceiver AGC circuits, to be monitored and controlled with ease. Operating on a single 5 V supply, each channel is fully specified for operation up to 2.7 GHz over a dynamic range of 60 dB. The AD8364 provides accurately scaled, independent, rms outputs of both RF measurement channels. Difference output ports, which measure the difference between the two channels, are also available. The on-chip channel matching makes the rms channel difference outputs extremely stable with temperature and process variations. The device also includes a useful temperature sensor with an accurately scaled voltage proportional to temperature, specified over the device operating temperature range. The AD8364 can be used with input signals having rms values from −55 dBm to +5 dBm referred to 50 Ω and large crest factors with no accuracy degradation.

Integrated in the AD8364 are two matched AD8362 channels (see the AD8362 data sheet for more information) with improved temperature performance and reduced log conformance ripple. Enhancements include improved temperature performance and reduced log-conformance ripple compared to the AD8362. On-chip wide bandwidth output op amps are connected to accommodate flexible configurations that support many system solutions.

The device can easily be configured to provide four rms measurements simultaneously. Linear-in-dB rms measurements are supplied at OUTA and OUTB, with conveniently scaled slopes of 50 mV/dB. The rms difference between OUTA and OUTB is available as differential or single-ended signals at OUTP and OUTN. An optional voltage applied to VLVL provides a common mode reference level to offset OUTP and OUTN above ground.

The AD8364 is supplied in a 32-lead, 5 mm × 5 mm LFCSP, for the operating temperature of –40°C to +85°C.

Rev. 0
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REVISION HISTORY

4/05—Revision 0: Initial Version

SPECIFICATIONS

V_S = VPSA = VPSB = VPSR = 5 V, T_A = 25°C, Channel A frequency = Channel B frequency, VLVL = VREF, VST[A, B] = OUT[A, B], OUT[P, N] = FBK[A, B], differential input via Balun, CW input $f \leq 2.7$ GHz, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION	Channel A and Channel B, CW sine wave input				
Signal Input Interface	INH[A, B] (Pins 26, 31) INL[A, B] (Pins 27, 30)				
Specified Frequency Range		LF		2.7	GHz
DC Common-Mode Voltage			2.5		V
Signal Output Interface	OUT[A, B] (Pins 15, 10)				
Wideband Noise	CLP[A, B] = 0.1µF, f_{SPOT} = 100 kHz, RF input = 2140 MHz, ≥−40 dBm		40		nV/√Hz
MEASUREMENT MODE, 450 MHz OPERATION	ADJA = ADJB = 0 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = M/A-Com ETK4-2T				
±1 dB Dynamic Range[1]	Pins OUT[A, B]		69		dB
	−40°C < T_A < +85°C		65		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/59		dB
	−40°C < T_A < +85°C, (Channel A/Channel B)		50/52		dB
Maximum Input Level	±1 dB error		12		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope			51.6		mV/dB
Intercept			−59		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.53		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.99		V
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		−0.1, +0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		−0.2, +0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		−0.3, +0.4		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		±0.25		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		±0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		±0.2		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		71		dB
Input A to OUTB Isolation	Freq separation = 1 kHz				
Input B to OUTA Isolation[2]	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		54		dB
	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		54		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		210||0.1		Ω||pF
Input Return Loss	With recommended balun		−12		dB
MEASUREMENT MODE, 880 MHz OPERATION	ADJA = ADJB = 0 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Mini-Circuits® JTX-4-10T				
±1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		66/57		dB
	−40°C < T_A < +85°C		58/40		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/54		dB
	−40°C < T_A < +85°C		20/20		dB
Maximum Input Level	±1 dB error, (Channel A/Channel B)		8/0		dBm
Minimum Input Level	±1 dB error, (Channel A/Channel B)		−58/−57		dBm
Slope			51.6		mV/dB
Intercept			−59.2		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.54		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.99		V

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		+0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		+0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		+0.5		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		+0.1, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		+0.1, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		+0.1, −0.2		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		64		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		35		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		35		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		200||0.3		Ω||pF
Input Return Loss	With recommended balun		−9		dB
MEASUREMENT MODE, 1880 MHz OPERATION	ADJA = ADJB = 0.75 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Murata LDB181G8820C-110				
±1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		69/61		dB
	−40°C < T_A < +85°C		60/50		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/51		dB
	−40°C < T_A < +85°C		58/51		dB
Maximum Input Level	±1 dB error, (Channel A/Channel B)		11/3		dBm
Minimum Input Level	±1 dB error		−58		dBm
Slope			50		mV/dB
Intercept			−62		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A,B]}$ = −10 dBm		2.49		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A,B]}$ = −40 dBm		0.98		V
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		+0.5, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		+0.5, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		+0.5, −0.2		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		±0.3		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		61		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		33		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		33		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		167||0.14		Ω||pF
Input Return Loss	With recommended balun		−8		dB
MEASUREMENT MODE, 2.14 GHz OPERATION	ADJA = ADJB = 1.02 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Murata LDB212G1020C-001				
±1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		66/57		dB
	−40°C < T_A < +85°C		58/40		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		62/54		dB
	−40°C < T_A < +85°C		30/30		dB
Maximum Input Level	±1 dB Error, (Channel A/Channel B)		−2/−4		dBm
Minimum Input Level	±1 dB Error, (Channel A/Channel B)		−57−51		dBm
Slope	Channel A/Channel B		49.5/52.1		mV/dB
Intercept	Channel A/Channel B		−58.3/−57.1		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.42		V

Parameter	Conditions	Min	Typ	Max	Unit
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.90		V
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		+0.1, −0.4		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		+0.1, −0.4		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		+0.1, −0.4		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		+0.1, −0.4		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		+0.2, −0.2		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		+0.1, −0.2		dB
Deviation from CW Response	5.5 dB peak-to-rms ratio (WCDMA one channel)		0.2		dB
	12 dB peak-to-rms ratio (WCDMA three channels)		0.3		dB
	18 dB peak-to-rms ratio (WCDMA four channels)		0.3		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		58		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		33		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		33		dB
Input Impedance	INHA/INLA, INHB/INLB differential drive		150||1.9		Ω||pF
Input Return Loss	With recommended balun		−10		dB
MEASUREMENT MODE, 2.5 GHz OPERATION	ADJA = ADJB = 1.14 V, error referred to best fit line using linear regression @ $P_{INH[A, B]}$ = −40 dBm and −20 dBm, T_A = 25°C, balun = Murata LDB182G4520C-110				
± 1 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		69/63		dB
	−40°C < T_A < +85°C		58		dB
±0.5 dB Dynamic Range[1]	Pins OUT[A, B], (Channel A/Channel B)		55/50		dB
	−40°C < T_A < +85°C		25		dB
Maximum Input Level	±1 dB error, (Channel A/Channel B)		17/11		dBm
Minimum Input Level	±1 dB error		−52		dBm
Slope			50		mV/dB
Intercept			−52.7		dBm
Output Voltage—High Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −10 dBm		2.14		V
Output Voltage—Low Power In	Pins OUT[A, B] @ $P_{INH[A, B]}$ = −40 dBm		0.65		V
Temperature Sensitivity	Deviation from OUT[A, B] @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm		±0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm		±0.5		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm		±0.5		dB
	Deviation from OUTP to OUTN @ 25°C				
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −10 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −25 dBm, −25 dBm		±0.3		dB
	−40°C < T_A < 85°C; $P_{INH[A, B]}$ = −40 dBm, −25 dBm		±0.3		dB
Input A to Input B Isolation	Baluns = Macom ETC1.6-4-2-3 (both channels)		54		dB
Input A to OUTB Isolation	P_{INHB} = −50 dBm, OUTB = $OUTB_{PINHB}$ ± 1 dB		31		dB
Input B to OUTA Isolation[2]	P_{INHA} = −50 dBm, OUTA = $OUTA_{PINHA}$ ± 1 dB		31		
Input Impedance	INHA/INLA, INHB/INLB differential drive		150||1.7		Ω||pF
Input Return Loss	With recommended balun		−11.5		dB
OUTPUT INTERFACE	Pin OUTA and OUTB				
Voltage Range Min	R_L ≥ 200 Ω to ground		0.09		V
Voltage Range Max	R_L ≥ 200 Ω to ground		V_S − 0.15		V
Source/Sink Current	OUTA and OUTB held at V_S/2, to 1% change		70		mA

Parameter	Conditions	Min	Typ	Max	Unit
SETPOINT INPUT	Pin VSTA and VSTB				
Voltage Range	Law conformance error ≤1 dB	0.5		3.75	V
Input Resistance			68		kΩ
Logarithmic Scale Factor	f = 450 MHz, −40°C ≤ T_A ≤ +85°C		50		mV/dB
Logarithmic Intercept	f = 450 MHz, −40°C ≤ T_A ≤ +85°C, referred to 50 Ω		−55		dBm
CHANNEL DIFFERENCE OUTPUT	Pin OUTP and OUTN				
Voltage Range Min	R_L ≥ 200 Ω to ground		0.1		V
Voltage Range Max	R_L ≥ 200 Ω to ground		V_S − 0.15		V
Source/Sink Current	OUTP and OUTN held at V_S/2, to 1% change		70		mA
DIFFERENCE LEVEL ADJUST	Pin VLVL				
Voltage Range[3]	OUT[P, N] = FBK[A, B]	0		5	V
OUT[P,N] Voltage Range	OUT[P, N] = FBK[A, B]	0		V_S − 0.15	V
Input Resistance			1		kΩ
TEMPERATURE COMPENSATION	Pin ADJA and ADJB				
Input Voltage Range		0		2.5	V
Input Resistance			>1		MΩ
VOLTAGE REFERENCE	Pin VREF				
Output Voltage	RF in = −55 dBm		2.5		V
Temperature Sensitivity	−40°C ≤ T_A ≤ +85°C		0.4		mV/°C
Current Limit Source/Sink	1% change		10/3		mA
TEMPERATURE REFERENCE	Pin TEMP				
Output Voltage	T_A = 25°C, R_L ≥ 10 kΩ		0.62		V
Temperature Coefficient	−40°C ≤ T_A ≤ +85°C, R_L ≥ 10 kΩ		2		mV/°C
Current Source/Sink	T_A = 25°C to 1% change		1.6/2		mA
POWER-DOWN INTERFACE	Pin PWDN				
Logic Level to Enable	Logic LO enables			1	V
Logic Level to Disable	Logic HI disables	3			V
Input Current	Logic HI PWDN = 5 V		95		µA
	Logic LO PWDN = 0 V		<100		µA
Enable Time	PWDN LO to OUTA/OUTB at 100% final value, $C_{LPA/B}$ = Open, $C_{HPA/B}$ = 10 nF, RF in = 0 dBm		2		µs
Disable Time	PWDN HI to OUTA/OUTB at 10% final value, $C_{LPA/B}$ = Open, $C_{HPA/B}$ = 10nF, RF in = 0 dBm		1.6		µs
POWER INTERFACE	Pin VPS[A, B], VPSR				
Supply Voltage		4.5		5.5	V
Quiescent Current	RF in = −55 dBm, V_S = 5 V		70		mA
	−40°C ≤ T_A ≤ +85°C			90	mA
Supply Current	PWDN enabled, V_S = 5 V		500		µA
	−40°C ≤ T_A ≤ +85°C			900	µA

[1] Best fit line, linear regression.
[2] See Figure 75 for a plot of isolation vs. frequency for a ±1 dB error.
[3] VLVL + OUTA/2 should not exceed VPSA − 1.31 V. Likewise, VLVL + OUTB/2 should not exceed VPSB − 1.31 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPSA, VPSB, VPSR	5.5 V
PWDN, VSTA, VSTB, ADJA, ADJB, FBKA, FBKB	0 V, 5.5 V
Input Power (Referred to 50 Ω)	23 dBm
Internal Power Dissipation	600 mW
θ_{JA}	39.8°C/W[1, 2]
θ_{JC}	3.9°C/W[2]
θ_{JB}	22.8°C/W[2]
Ψ_{JT}	0.4°C/W[1, 2]
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Still air.
[2] All values are modeled using a standard 4-layer JEDEC test board with the pad soldered to the board and thermal vias in the board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

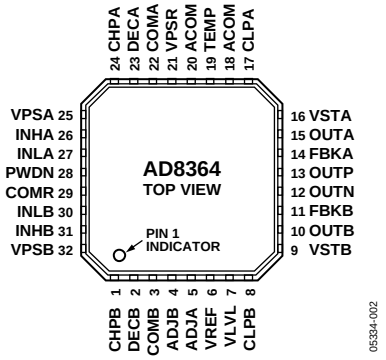


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equiv. Circuit
1	CHPB	Connect to common via a capacitor to determine 3 dB point of Channel B input signal high-pass filter.	
2, 23	DECB, DECA	Decoupling Terminals for INHA/INLA and INHB/INLB. Connect to common via a large capacitance to complete input circuit.	Figure 52
3, 22, 29	COMB, COMA, COMR	Input System Common Connection. Connect via low impedance to system common.	
4, 5	ADJB, ADJA	Temperature Compensation for Channel B and Channel A. An external voltage is connected to these pins to improve temperature drift. This voltage can be derived from VREF, that is, connect a resistor from VREF to ADJ[A, B] and another resistor from ADJ[A, B] to ground. The value of these resistors change as the frequency changes.	Figure 68
6	VREF	General-Purpose Reference Voltage Output of 2.5 V.	Figure 54
7	VLVL	Reference Level Input for OUTP and OUTN. (Usually connected to VREF through a voltage divider or left open).	Figure 58
8, 17	CLPB, CLPA	Channel B and Channel A Connection for Loop Filter Integration (Averaging) Capacitor. Connect a ground-referenced capacitor to this pin. A resistor can be connected in series with this capacitor to improve loop stability and response time.	
9	VSTB	The voltage applied to this pin sets the decibel value of the required RF input voltage to Channel B that results in zero current flow in the loop integrating capacitor pin, CLPB.	Figure 56
10	OUTB	Channel B Output of Error Amplifier. In measurement mode, normally connected directly to VSTB.	Figure 57
11	FBKB	Feedback Through 1 kΩ to the Negative Terminal of the Integrated Op Amp Driving OUTN.	
12	OUTN	Channel Differencing Op Amp Output. In measurement mode, normally connected directly to FBKB and follows the equation OUTN = OUTA − OUTB + VLVL.	Figure 58
13	OUTP	Channel Differencing Op Amp Output. In measurement mode, normally connected directly to FBKA and follows the equation OUTP = OUTA − OUTB + VLVL.	Figure 58
14	FBKA	Feedback Through 1kΩ to the Negative Terminal of the Integrated Op Amp Driving OUTP.	
15	OUTA	Channel A Output of Error Amplifier. In measurement mode, normally connected directly to VSTA.	Figure 57
16	VSTA	The voltage applied to this pin sets the decibel value of the required RF input voltage to Channel A that results in zero current flow in the loop integrating capacitor pin, CLPA.	Figure 56
18, 20	ACOM	Analog Common for Channels A and B. Connect via low impedance to common.	
21, 25, 32	VPSR, VPSA, VPSB	Supply for the Input System of Channels A and B. Supply for the internal references. Connect to +5 V power supply.	
19	TEMP	Temperature Sensor Output.	Figure 53
24	CHPA	Connect to common via a capacitor to determine 3 dB point of Channel A input signal high-pass filter.	
26, 27	INHA, INLA	Channel A High and Low RF Signal Input Terminal.	Figure 52
28	PWDN	Disable/Enable Control Input. Apply logic high voltage to shut down the AD8364.	Figure 55
30, 31	INLB, INHB	Channel B Low and High RF Signal Input Terminal.	Figure 52
Under Package	Exposed Paddle	The exposed paddle on the under side of the package should be soldered to a ground plane with low thermal and electrical characteristics.	

TYPICAL PERFORMANCE CHARACTERISTICS

V_P = 5 V; T_A = +25°C, −40°C, +85°C; CLPA/B = OPEN. Colors: +25°C black, −40°C blue, +85°C red.

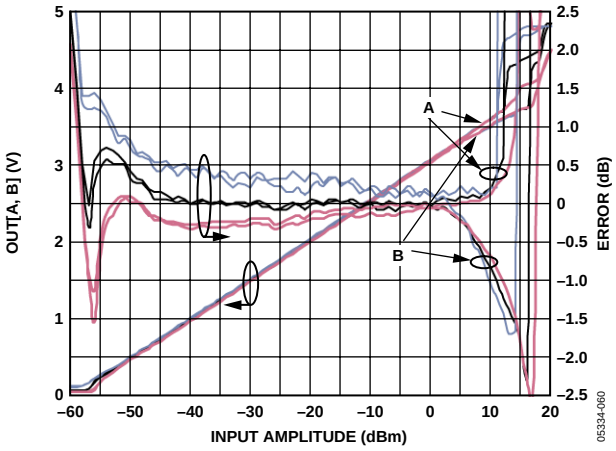


Figure 3. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 450 MHz, Typical Device, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T

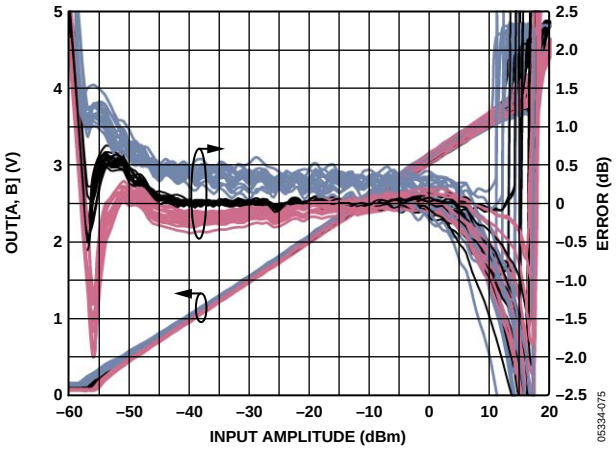


Figure 4. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 30 Devices from Multiple Lots, Frequency = 450 MHz, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T

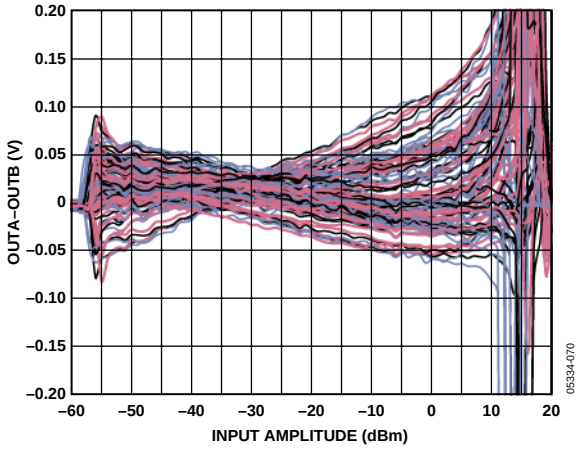


Figure 5. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 30 Devices from Multiple Lots, Frequency = 450 MHz, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T

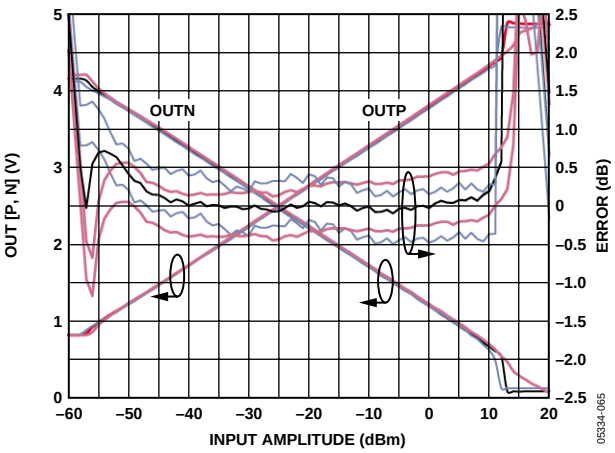


Figure 6. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 450 MHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, Balun = Macom ETK4-2T (Note that the OUTP and OUTN Error Curves Overlap)

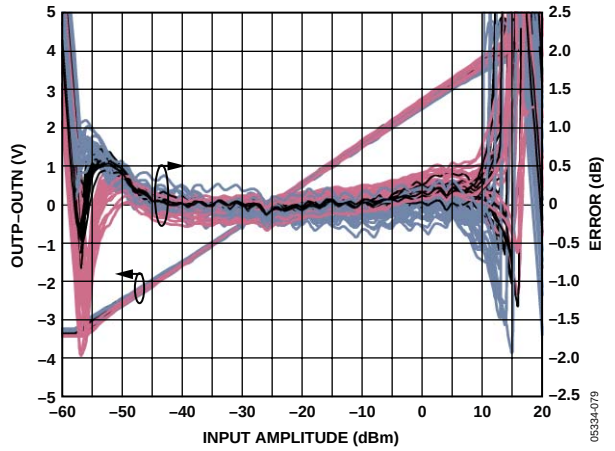


Figure 7. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 30 Devices from Multiple Lots, Frequency = 450 MHz, ADJ[A, B] = 0 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

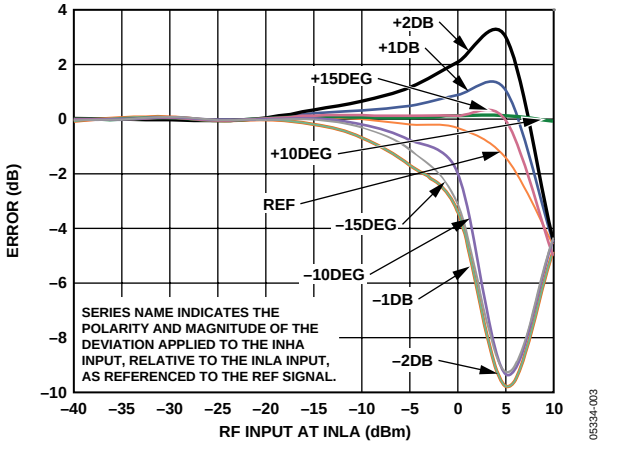


Figure 8. Log Conformance vs. Input Amplitude at various Amplitude and Phase Balance points, 450 MHz, Typical Device, ADJ[A, B] = 0 V, Sine Wave, Differential Drive

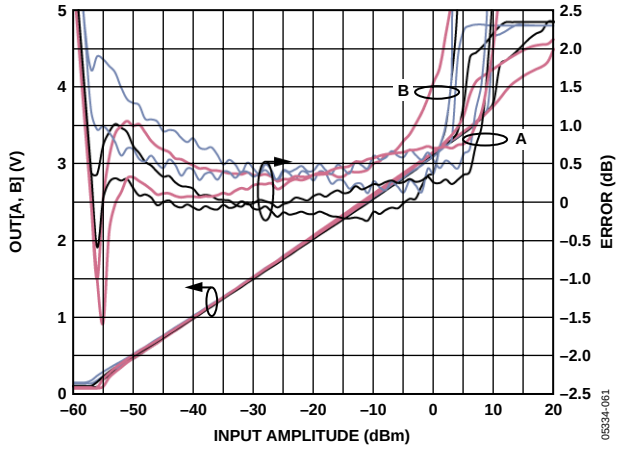


Figure 9. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 880 MHz, Typical Device, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun = Mini-Circuits JTX-4-10T

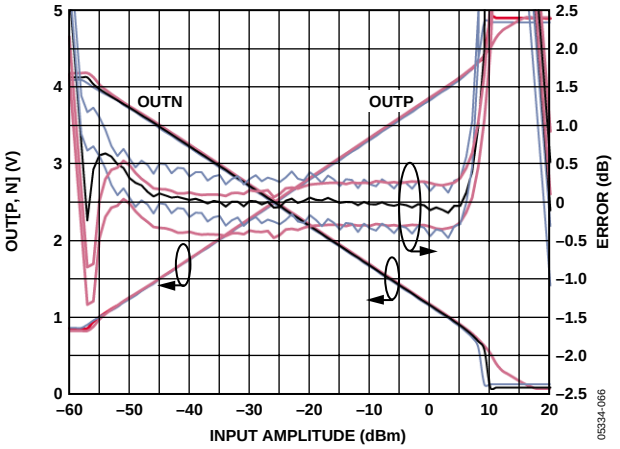


Figure 12. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 880 MHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun = JTX-4-10T (Note that the OUTP and OUTN Error Curves Overlap)

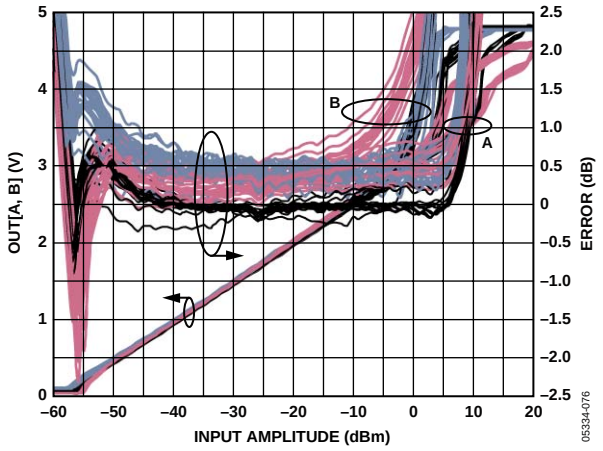


Figure 10. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 880 MHz, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun =JTX-4-10T

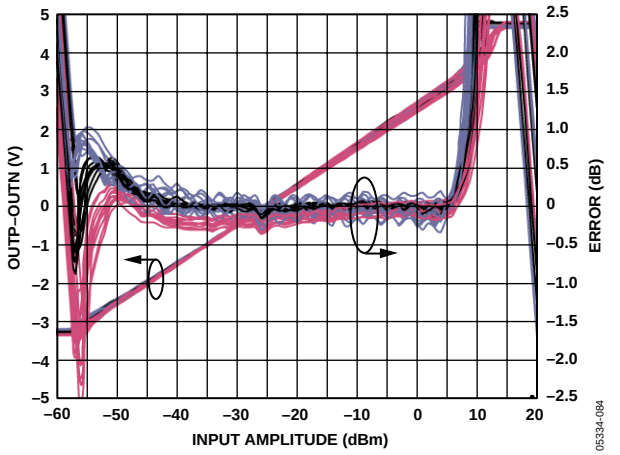


Figure 13. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 880 MHz, ADJ[A, B] =0.5 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

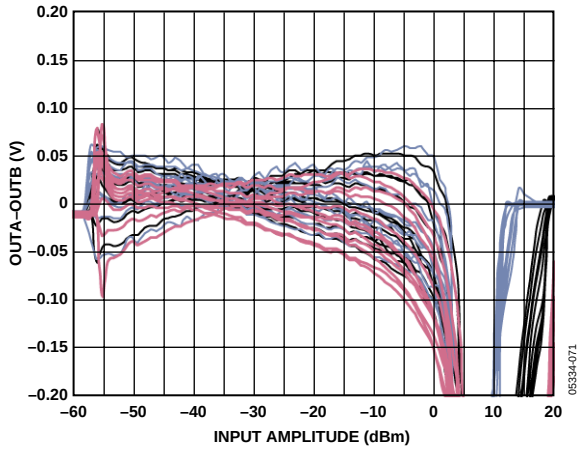


Figure 11. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 15 Devices from Multiple Lots, Frequency = 880 MHz, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive, Balun =JTX-4-10T

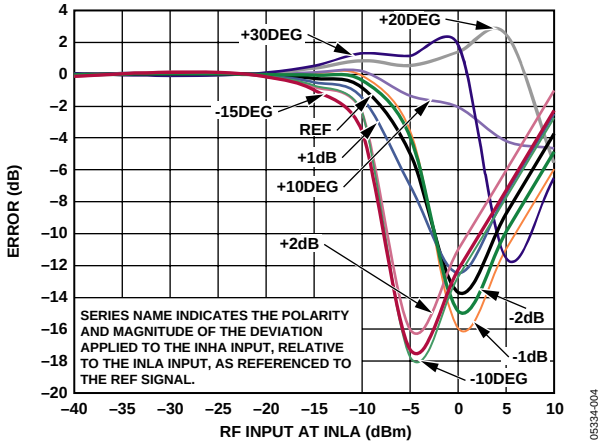


Figure 14. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance points, 880 MHz, Typical Device, ADJ[A, B] = 0.5 V, Sine Wave, Differential Drive

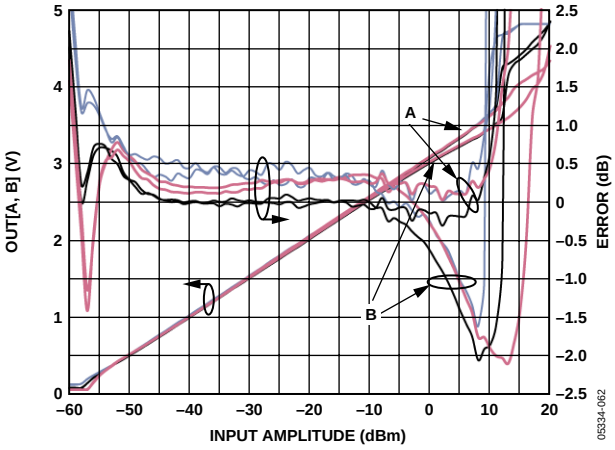


Figure 15. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 1.88 GHz, Typical Device, TADJ[A, B]= 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110

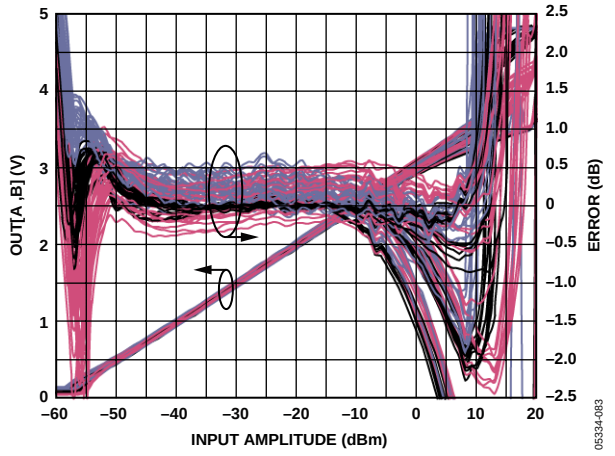


Figure 16. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 20 Devices from Multiple Lots, Frequency = 1.88 GHz, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110

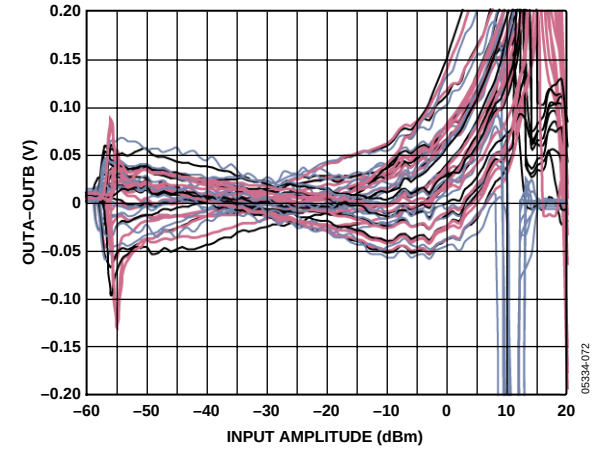


Figure 17. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 20 Devices from Multiple Lots, Frequency = 1.88 GHz, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110

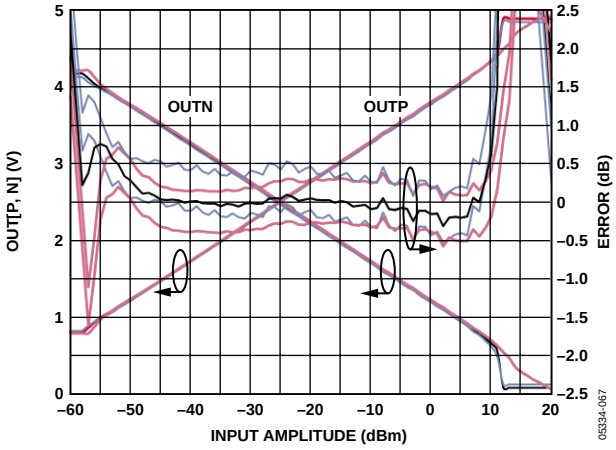


Figure 18. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 1.88 GHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive, Balun = Murata LDB181G8820C-110 (Note that the OUTP and OUTN Error Curves Overlap)

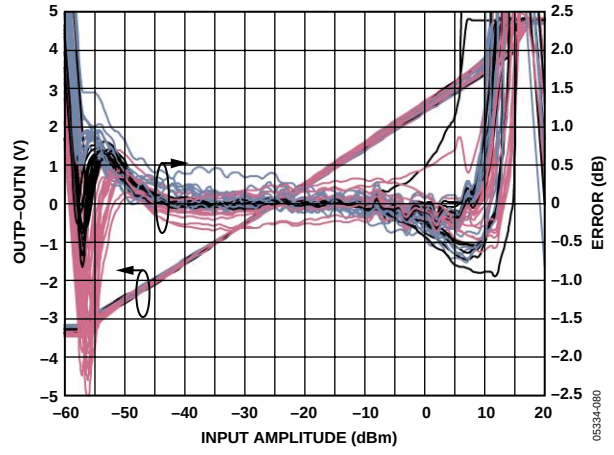


Figure 19. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 20 Devices from Multiple Lots, Frequency = 1.88 GHz, ADJ[A, B] =0.65 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

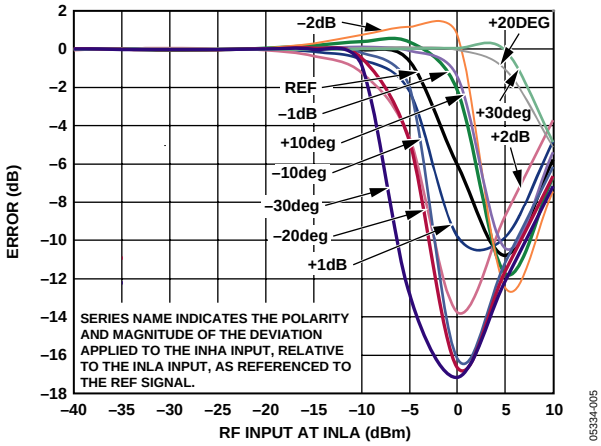


Figure 20. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance Points, 1.880 GHz, Typical Device, ADJ[A, B] = 0.65 V, Sine Wave, Differential Drive

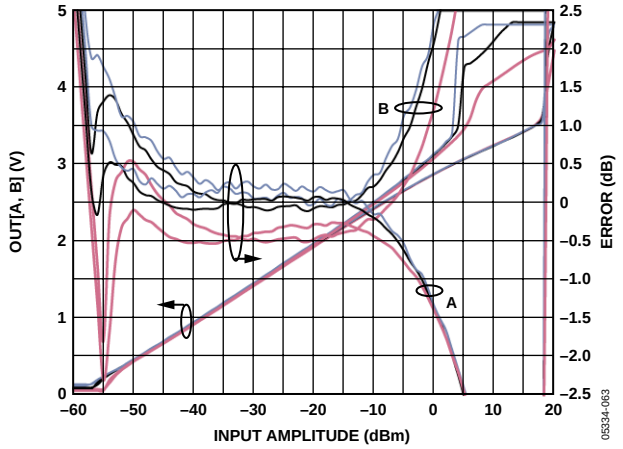


Figure 21. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 2.14 GHz, Typical Device, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001

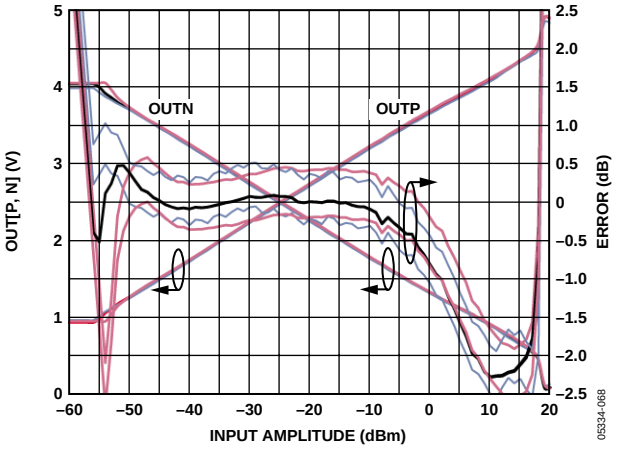


Figure 24. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 2.14 GHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001 (Note that the OUTP and OUTN Error Curves Overlap)

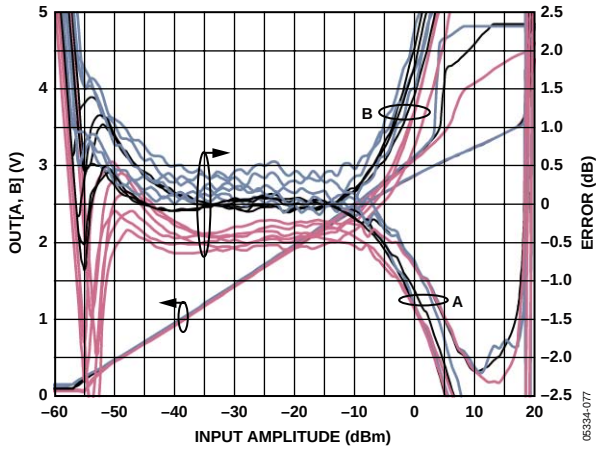


Figure 22. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 3 Devices from Multiple Lots, Frequency = 2.14 GHz, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001

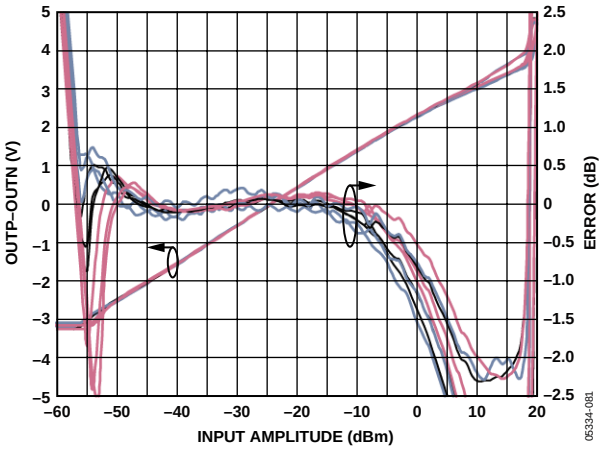


Figure 25. Distribution of [OUTP − OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 3 Devices from Multiple Lots, Frequency = 2.14 GHz, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

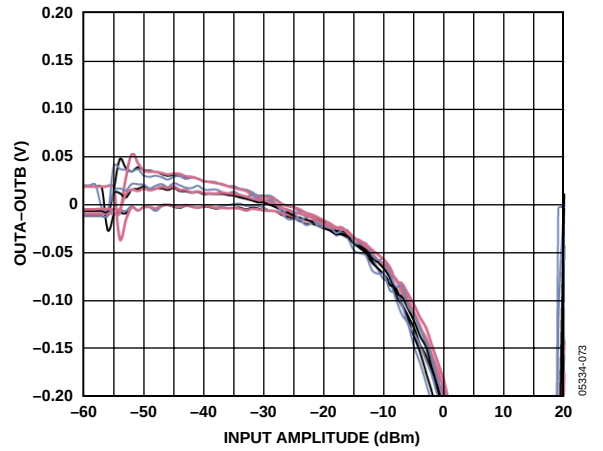


Figure 23. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for 3 Devices from Multiple Lots, Frequency = 2.14 GHz, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive, Balun = Murata LDB212G1020C-001

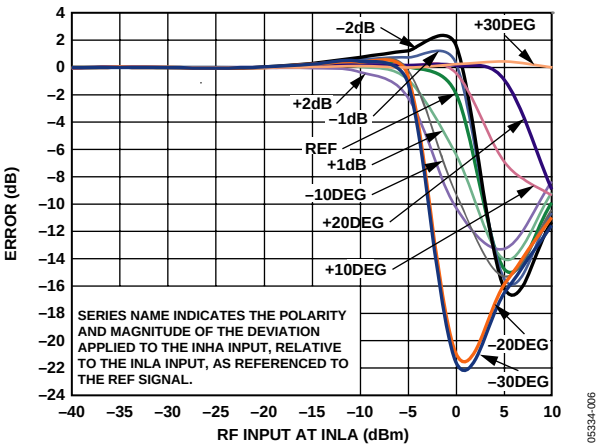


Figure 26. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance Points, 2.140 GHz, Typical Device, ADJ[A, B] = 0.85 V, Sine Wave, Differential Drive

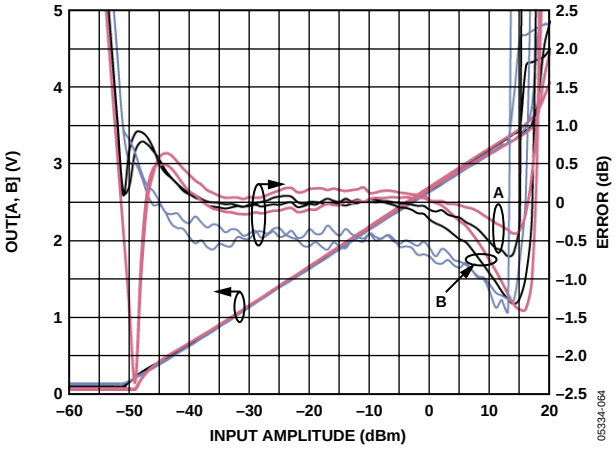


Figure 27. OUT[A, B] Voltage and Log Conformance vs. Input Amplitude at 2.5 GHz, Typical Device, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110

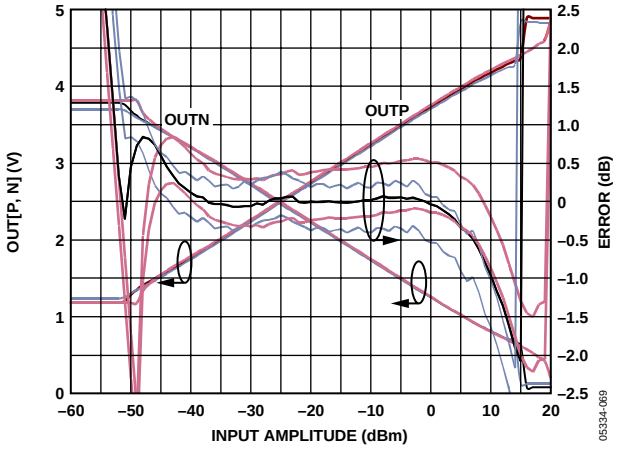


Figure 30. OUT[P, N] Voltage and Log Conformance vs. Input Amplitude at 2.5 GHz, with B Input Held at −25 dBm and A Input Swept, Typical Device, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110 (Note that the OUTP and OUTN Error Curves Overlap)

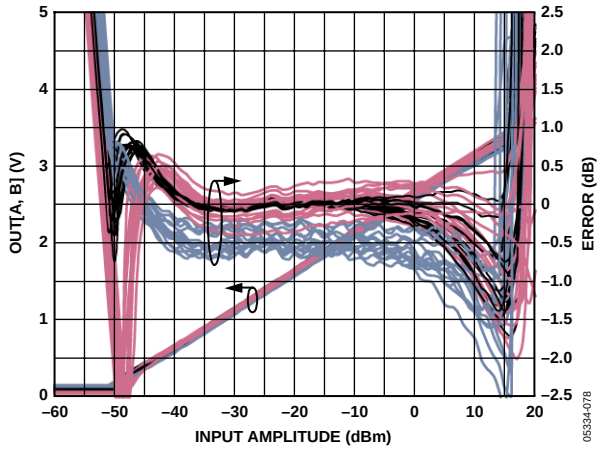


Figure 28. Distribution of OUT[A, B] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 2.5 GHz, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110

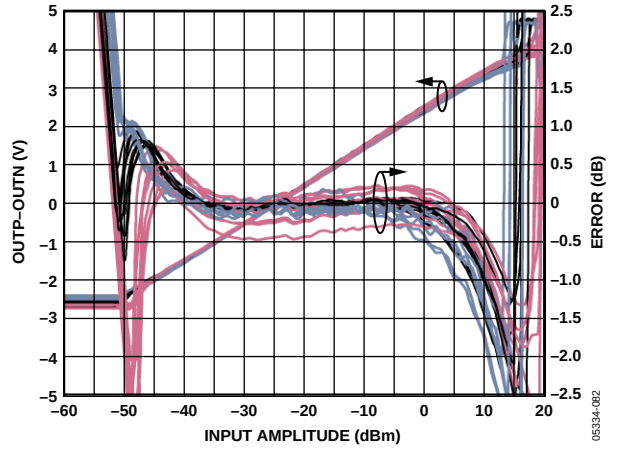


Figure 31. Distribution of [OUTP – OUTN] Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 2.5 GHz, ADJ[A, B] =1.1 V, Sine Wave, Differential Drive, P_{IN} Ch. B = −25 dBm, Channel A Swept

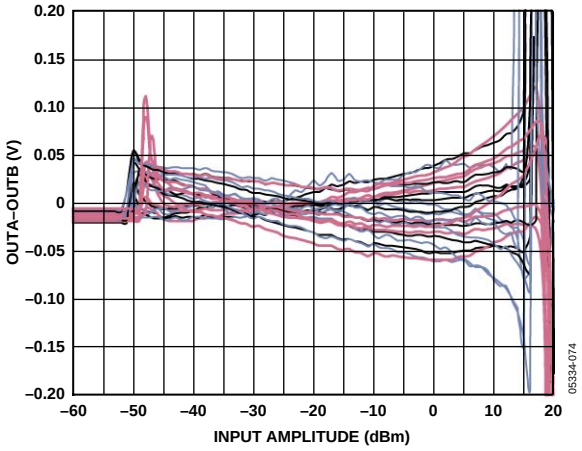


Figure 29. Distribution of [OUTA – OUTB] Voltage vs. Input Amplitude over Temperature for at Least 15 Devices from Multiple Lots, Frequency = 2.5 GHz, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive, Balun = Murata LDB182G4520C-110

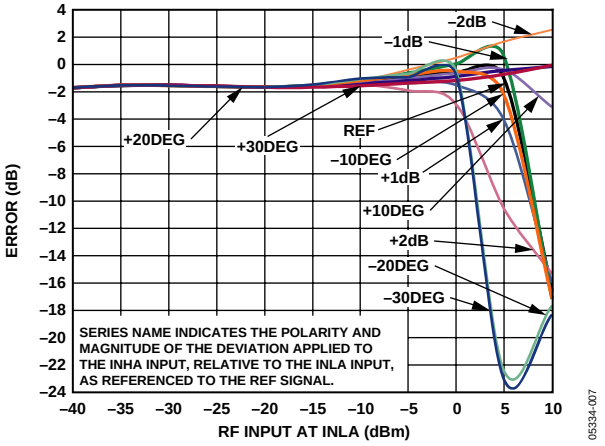


Figure 32. Log Conformance vs. Input Amplitude at Various Amplitude and Phase Balance Points, 2.500 GHz, Typical Device, ADJ[A, B] = 1.1 V, Sine Wave, Differential Drive

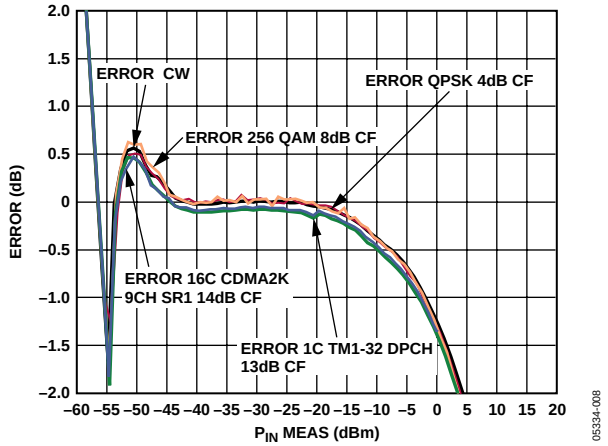


Figure 33. Output Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, QPSK, 256QAM, WCDMA 1-Carrier Test Model 1 with 32 DPCH, CDMA2000, 16-Carrier, 9-Channel SR1 Frequency 2.140 GHz, CLP[A, B] = 1 µF, Balun = Murata LDB212G1020C-001

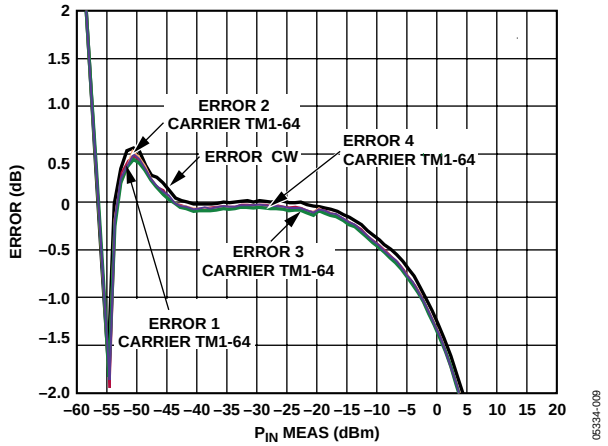


Figure 34. Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, WCDMA1, 2-, 3-, and 4-Carrier, Test Model 1 with 64 DPCH, Frequency 2.14 GHz, Balun = Murata LDB212G1020C-001

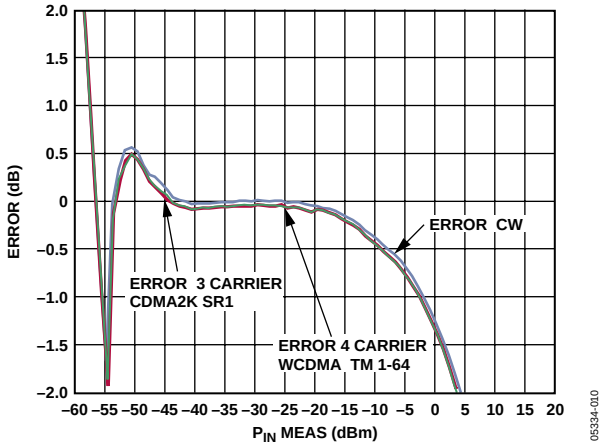


Figure 35. Output Voltage and Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, 3-Carrier CDMA2000 SR1, 4-Carrier WCDMA, Test Model 1 with 64 DPCH, Frequency 2.140 GHz, Balun = Murata LDB212G1020C-001

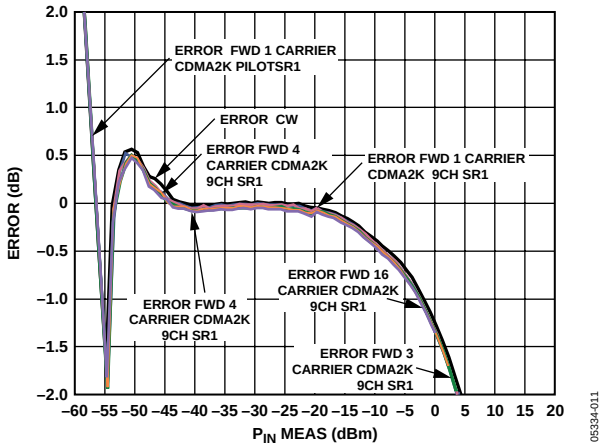


Figure 36. Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, CW, 1-Carrier CDMA2000 Pilot CH SR1, 1-Carrier CDMA2000 9CH SR1, 3-Carrier CDMA2000 9CH SR1, 4-Carrier CDMA2000 9CH SR1 Frequency 16-Carrier CDMA2000 9CH SR1, Frequency 2.140 GHz, Balun = Murata LDB212G1020C-001

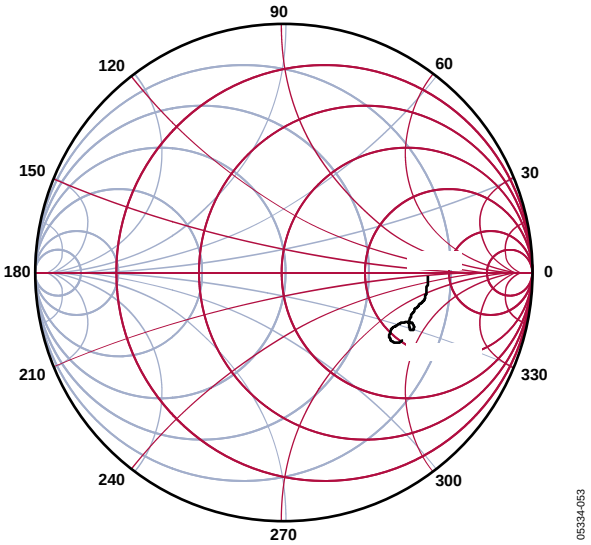


Figure 37. Differential Input Impedance (S11) vs. Frequency; $Z_O = 50\ \Omega$

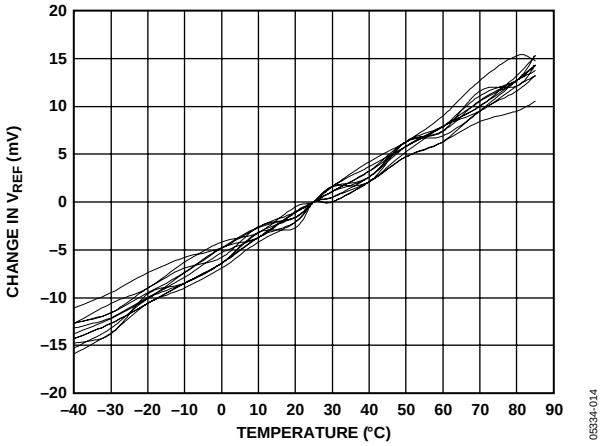


Figure 40. Change in VREF vs. Temperature for 11 Devices

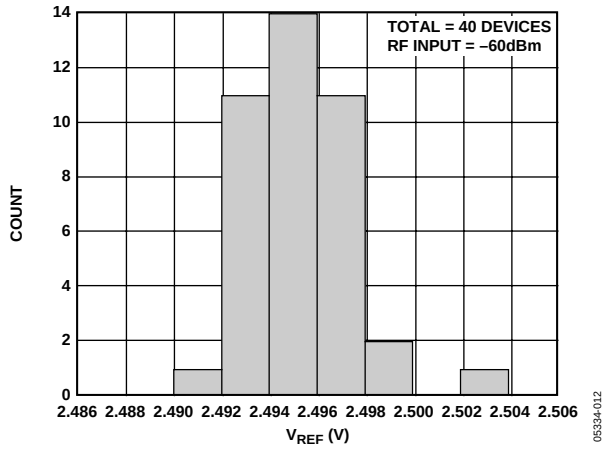


Figure 38. Distribution of VREF for 40 Devices

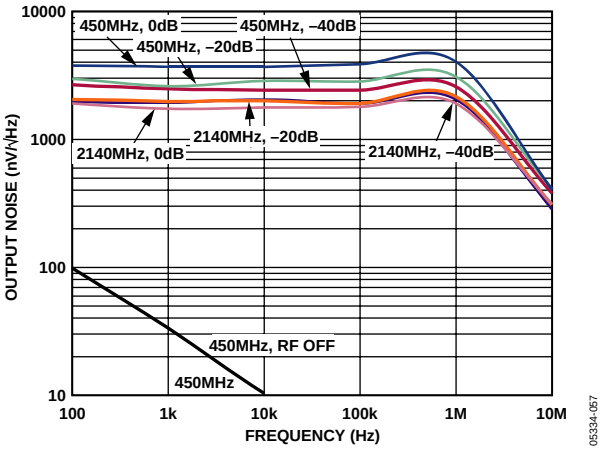


Figure 41. Noise Spectral Density of OUT[A, B]; CLP[A, B] = Open

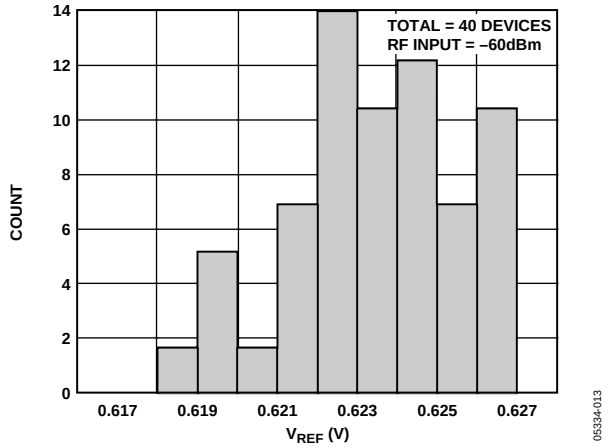


Figure 39. Distribution of TEMP Voltage for 40 Devices

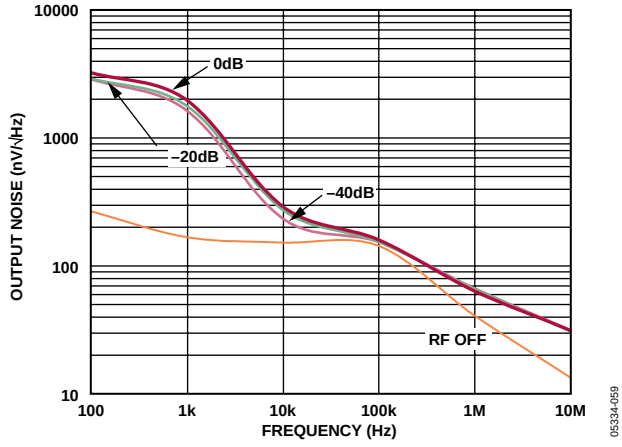


Figure 42. Noise Spectral Density of OUT[P, N]; CLP[A, B] = 0.1 µF, Frequency = 2140 MHz

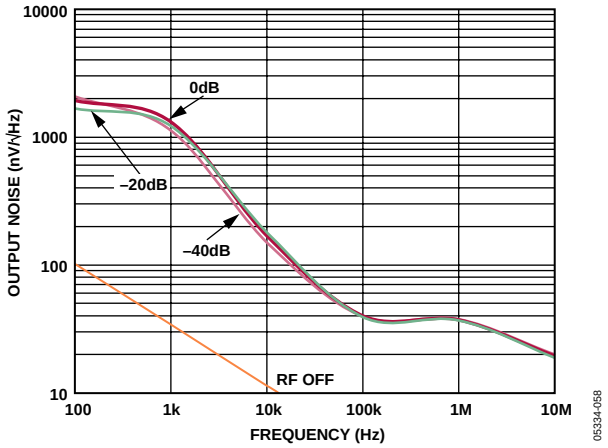


Figure 43. Noise Spectral Density of OUT[A, B]; CLP[A, B] = 0.1 µF, Frequency = 2140 MHz

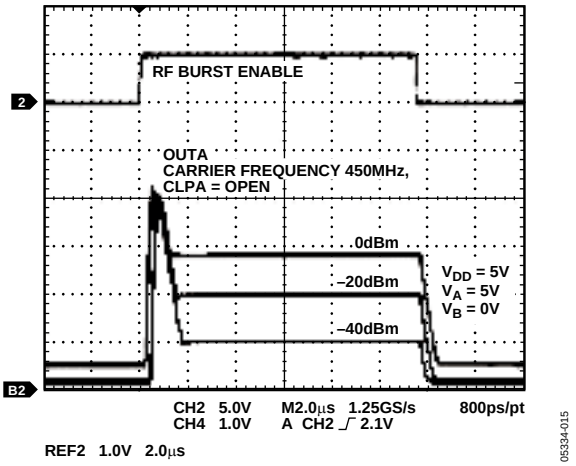


Figure 44. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = Open

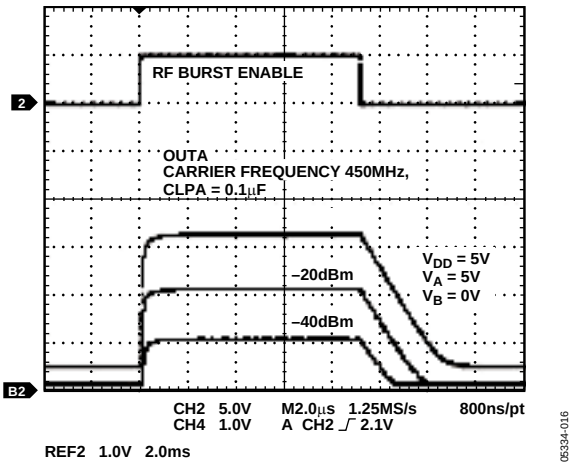


Figure 45. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = 0.1 µF

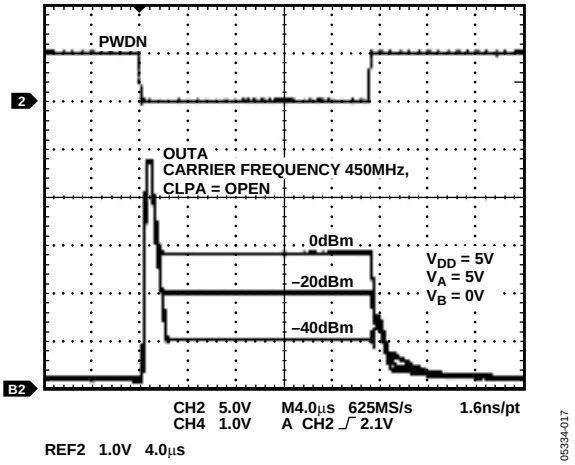


Figure 46. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = Open

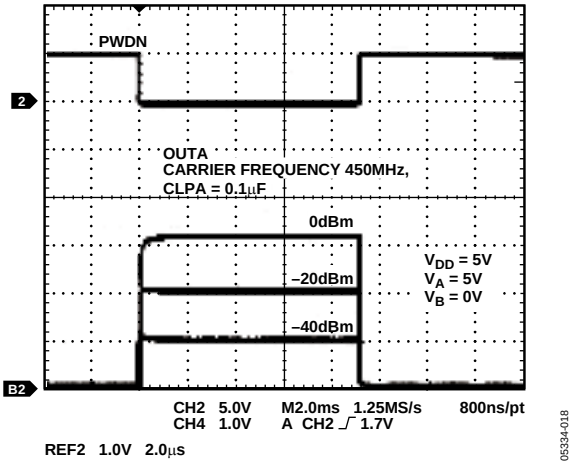


Figure 47. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 450 MHz, CLPA = 0.1 µF, CHPA = 10 nF

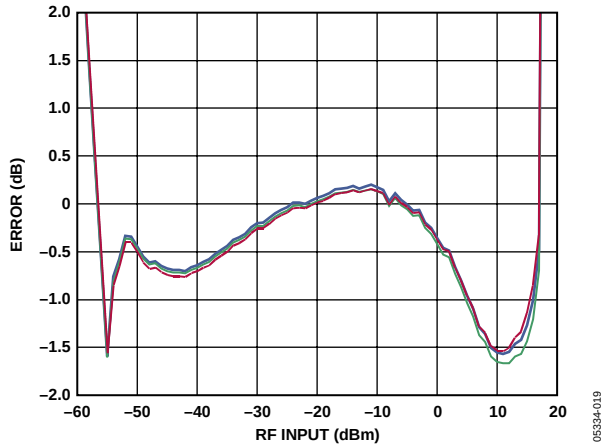


Figure 48. Output Voltage Stability vs. VP (Supply Voltage) at 2.14 GHz, When VP Varies by 10%,ADJ[A, B] =0.85 V, Sine Wave, Differential Drive, Murata LDB212G1020C-001

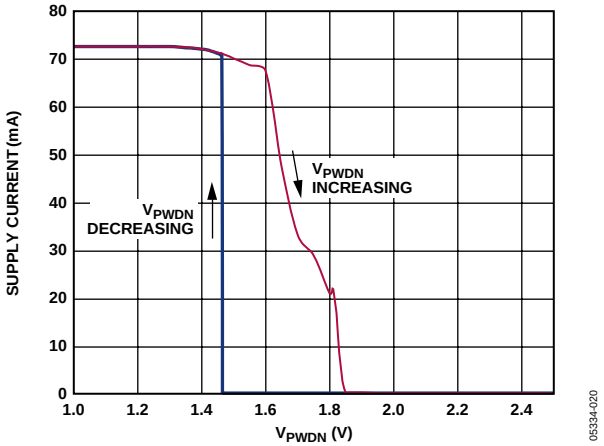


Figure 49. Supply Current vs. V_{PWDN}

GENERAL DESCRIPTION AND THEORY

The AD8364 is a dual-channel, 2.7 GHz, true rms responding detector with 60 dB measurement range. It incorporates two AD8362 channels with shared reference circuitry (See the AD8362 datasheet for more information). Multiple enhancements have been made to the AD8362 cores to improve measurement accuracy. Log-conformance peak-to-peak ripple has been reduced to <±0.2 dB over the entire dynamic range. Temperature stability of the rms output measurements provides <±0.5 dB error over the specified temperature range of −40°C to 85°C through proprietary techniques. The use of well-matched channels offers extremely temperature-stable difference outputs, OUTP and OUTN. Given well-matched channels through IC integration, the rms measurement outputs, OUTA and OUTB, drift in the same manner. With OUTP shorted to FBKA, the function at OUTP is

$$OUTP = OUTA - OUTB + VLVL \quad (1)$$

When OUTN is shorted to FBKB, the function at OUTN is

$$OUTN = OUTB - OUTA + VLVL \quad (2)$$

OUTP and OUTN are insensitive to the common drift due to the difference cancellation of OUTA and OUTB.

The AD8364 is a fully calibrated rms-to-dc converter capable of operating on signals of a few hertz to 2.7 GHz or more. Unlike logarithmic amplifiers, the AD8364 response is waveform independent. The device accurately measures waveforms that have a high peak-to-rms ratio (crest factor). Figure 50 shows a block diagram.

A single channel of the AD8364 consists of a high performance AGC loop. As shown in Figure 51, the AGC loop comprises a wide bandwidth variable gain amplifier (VGA), square law detectors, an amplitude target circuit, and an output driver. For a more detailed description of the functional blocks, see the AD8362 data sheet.

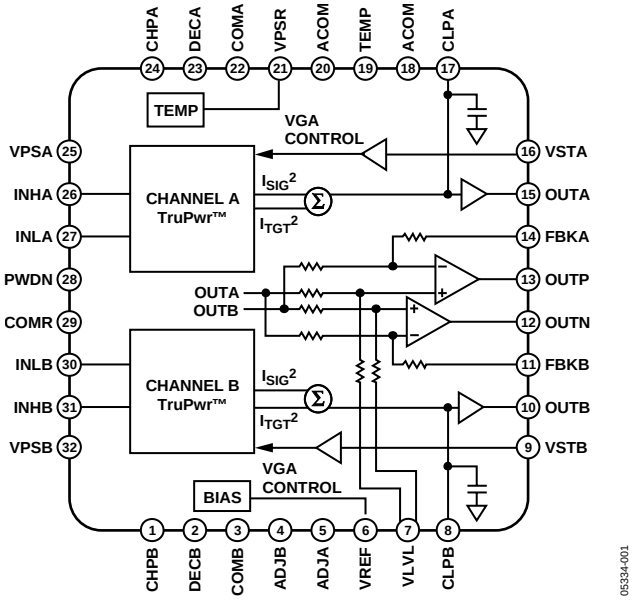


Figure 50. Block Diagram

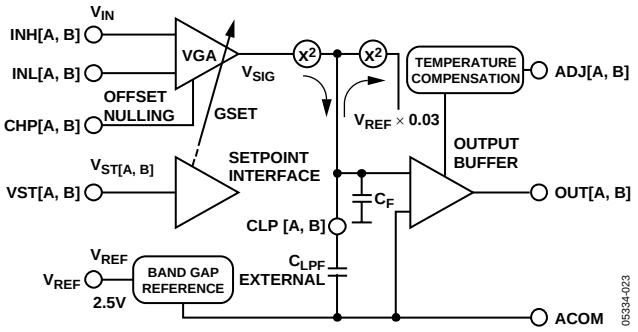


Figure 51. Single-Channel Details

SQUARE LAW DETECTOR AND AMPLITUDE TARGET

The output of the VGA, called V_{SIG}, is applied to a wideband square law detector. The detector provides the true rms response of the RF input signal, independent of waveform, up to a crest factor of 6. The detector output, called I_{SQU}, is a fluctuating current with positive mean value. The difference between I_{SQU} and an internally generated current, $I_{TGT[A, B]}$, is integrated by C_F and a capacitor attached to CLP[A, B]. CF is the on-chip 25 pF filter capacitor. CLP[A, B] can be used to arbitrarily increase the averaging time while trading off response time. When the AGC loop is at equilibrium,

$$MEAN(I_{SQU}) = I_{TGT[A, B]} \quad (3)$$

This equilibrium occurs only when

$$MEAN(V_{SIG}^2) = V_{TGT[A, B]}^2 \quad (4)$$

where V_{TGT} is an attenuated version of the VREF voltage.

Because the square law detectors are electrically identical and well matched, process and temperature dependant variations are effectively cancelled.

By forcing the above identity through varying the VGA setpoint, it is apparent that

$$RMS(V_{SIG}) = \sqrt{}(MEAN(V_{SIG}^2)) = \sqrt{}(V_{TGT}^2) = V_{TGT} \quad (5)$$

Substituting the value of V_{SIG}, we have

$$RMS(G0 \times RF_{IN} \exp(-VST[A, B]/V_{GNS})) = V_{TGT} \quad (6)$$

When connected as a measurement device VST[A, B] = OUT[A, B]. Solving for OUT[A, B] as a function of RF_{IN},

$$OUT[A, B] = V_{SLOPE} \times \text{Log10}(RMS(RF_{IN})/V_Z) \quad (7)$$

where V_{SLOPE} is laser trimmed to 1 V/decade (or 50 mV/dB) at 100 MHz. V_Z is the intercept voltage, since Log 10(1) = 0 when $RMS(RF_{IN}) = V_Z$. If desired, the effective value of V_{SLOPE} may be altered by using a resistor divider from OUT[A, B] to drive VST[A, B]. The intercept, V_Z, is also laser trimmed to 180 µV (−62 dBm, referred to 50 Ω) with a CW signal at 100 MHz. This value is extrapolated, because OUT[A, B] do not respond to input of less than approximately −55 dBm with differential drive.

In most applications, the AGC loop is closed through the setpoint interface, VST[A, B]. In measurement mode, OUT[A, B] are tied to VST[A, B], respectively. In controller mode, a control voltage is applied to VST[A, B]. Pins OUT[A, B] drive the control input of a system. The RF feedback signal to the input pins is forced to have an rms value determined by VSTA or VSTB.

RF INPUT INTERFACE

The AD8364's RF inputs are connected as shown in Figure 52. There are 100 Ω resistors connected between DEC[A, B] and INH[A, B] and also between DEC[A, B] and INL[A, B]. The DEC[A, B] pins have a dc level established as (7 × VPS[A, B] + 55 × V_{BE})/30. With a 5 V supply, DEC[A, B] is approximately 2.5 V.

Signal-coupling capacitors must be connected from the input signal to the INH[A, B] and INL[A, B] pins. The high-pass corner is

$$f_{high\text{-}pass} = 1/(2 \times \pi \times 100 \times C) \quad (8)$$

A decoupling capacitor should be connected from DEC[A, B] to ground to attenuate any signal at the midpoint. A 100 pF and 0.1 µF cap from DEC[A, B] to ground are recommended, with a 1 nF coupling capacitor such that signals greater than 1.6 MHz can be measured. For coupling signals less than 1.6 MHz, 100 × $C_{coupling}$ for the DEC[A, B] capacitor generally can be used.

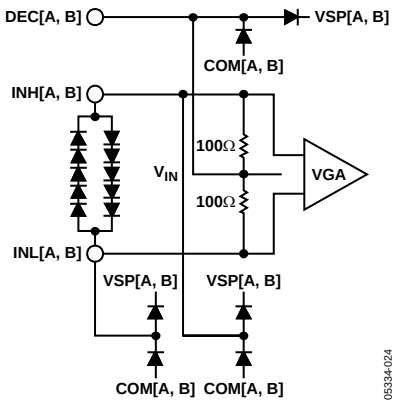


Figure 52. AD8364 RF Inputs

OFFSET COMPENSATION

An offset-nulling loop is used to address small dc offsets in the VGA. The high-pass corner frequency of this loop is internally preset to about 1 MHz using an on-chip capacitor of 25 pF (1/(2 × 5K × 25 pF)), which is sufficiently low for most HF applications. The high-pass corner can be reduced by a capacitor from CHP[A, B] to ground. The input offset voltage varies depending on the actual gain at which the VGA is operating and, thus, on the input signal amplitude. When an excessively large value of CHP[A, B] is used, the offset correction process may lag the more rapid changes in the VGA's gain, which may increase the time required for the loop to fully settle for a given steady input amplitude.

TEMPERATURE SENSOR INTERFACE

The AD8364 provides a temperature sensor output capable of driving about 1.6 mA. A 330 Ω-equivalent internal resistance is connected from TEMP to COMR to provide current sink capability. The temperature scaling factor of the output voltage is approximately 2 mV/°C. The typical absolute voltage at 25°C is about 620 mV.

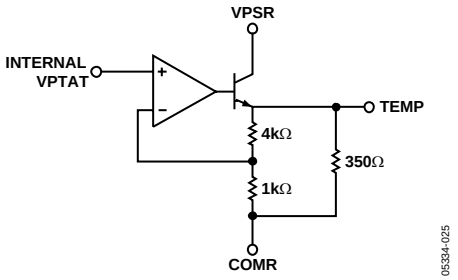


Figure 53. TEMP Interface Simplified Schematic

VREF INTERFACE

An internal voltage reference is provided to the user at Pin VREF. The VREF voltage is a temperature stable 2.5 V reference that can drive about 18 mA. An 830 Ω equivalent internal resistance is connected from VREF to ACOM for 3 mA sink capability.

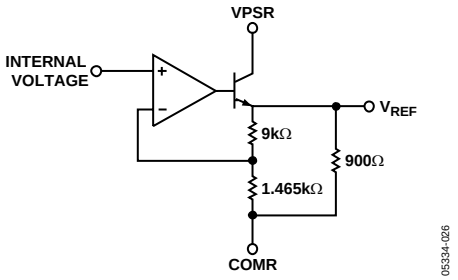


Figure 54. VREF Interface Simplified Schematic

POWER-DOWN INTERFACE

The operating and stand-by currents for the AD8364 at 25°C are approximately 70 mA and 500 µA, respectively. The PWDN pin is connected to an internal resistor divider made with two 42 kΩ resistors. The divider voltage is applied to the base of an NPN transistor to force a power-down condition when the device is active. Typically when PWDN is pulled greater than 2 V, the device is powered down. Figure 46 and Figure 47 show typical response times for various RF input levels. The output reaches to within 0.1 dB of its steady-state value in about 1.6 µs; the reference voltage is available to full accuracy in a much shorter time. This wake-up response vary depending on the input coupling means and the capacitances CDEC[A, B], CHP[A, B], and CLP[A, B].

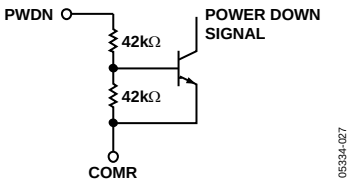


Figure 55. PWDN Interface Simplified Schematic

VST[A, B] INTERFACE

The VST[A, B] interface has a high input impedance of 72 kΩ. The voltage at VST[A, B] is converted to an internal current used to steer the VGA gain. The VGA attenuation control is set to 20 dB/V.

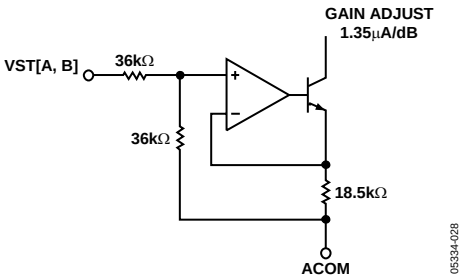


Figure 56. VST[A, B] Interface Simplified Schematic

OUT[A, B, P, N] OUTPUTS

The output drivers used in the AD8364 are different than the output stage on the AD8362. The AD8364 incorporates rail-to-rail output drivers with pull-up and pull-down capabilities. The output noise is approximately 40 nV/√Hz at 100 kHz. OUT[A, B, P, N] can source and sink up to 70 mA. There is also an internal load from both OUTA and OUTB to ACOM of 2.5 kΩ.

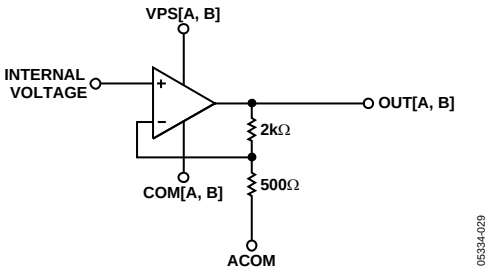


Figure 57. OUT[A, B] Interface Simplified Schematic

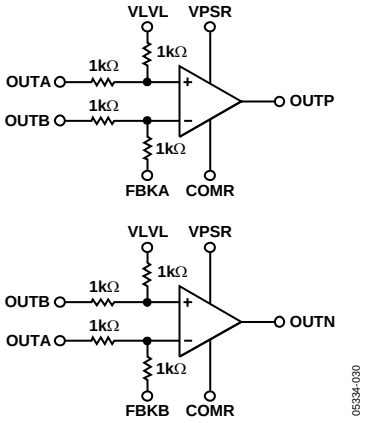


Figure 58. OUT[P, N] Interface Simplified Schematic

MEASUREMENT CHANNEL DIFFERENCE OUTPUT USING OUT[P, N]

The AD8364 incorporates two operational amplifiers with rail-to-rail output capability to provide a channel difference output. As in the case of the output drivers for OUT[A, B], the output stages have the capability of driving 70 mA. The output noise is approximately 40 nV/√Hz at 100 kHz. OUTA and OUTB are internally connected through 1 kΩ resistors to the inputs of each op amp. The pin VLVL is connected to the positive terminal of both op amps through 1 kΩ resistors to provide level shifting. The negative feedback terminal is also made available through a 1 kΩ resistor. The input impedance of VLVL is 1 kΩ and FBK[A, B] is 2 kΩ. See Figure 59 for the connections of these pins.

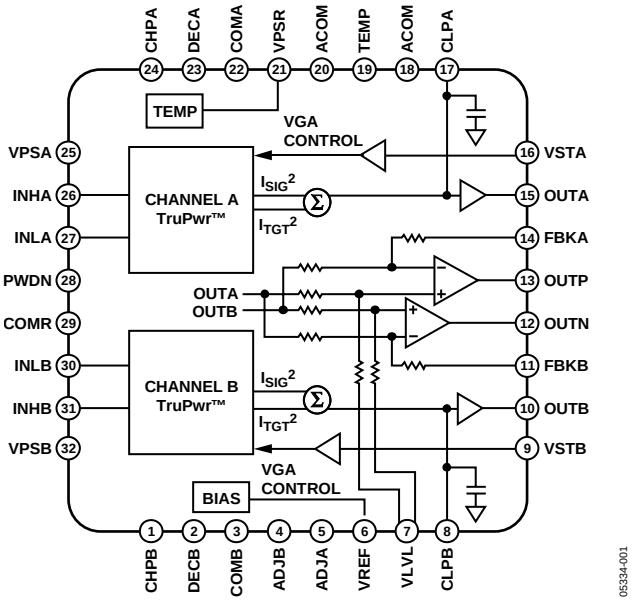


Figure 59. Op Amp Connections (All Resistors are 1 kΩ ± 20%)

If OUTP is connected to FBKA, then OUTP is given as

$$OUTP = OUTA - OUTB + VLVL \quad (9)$$

If OUTN is connected to FBKB, then OUTN is given as

$$OUTN = OUTB - OUTA + VLVL \quad (10)$$

In this configuration, all four measurements, OUT[A, B, P, N], are made available simultaneously. A differential output can be taken from OUTP − OUTN, and VLVL can be used to adjust the common-mode level for an ADC connection.

CONTROLLER MODE

The channel difference outputs can be used for controlling a feedback loop to the AD8364's RF inputs. A capacitor connected between FBKA and OUTP forms an integrator, keeping in mind that the on-chip 1 kΩ feedback resistor forms a zero. (The value of the on-chip resistors can vary as much as ±20% with manufacturing process variation.) If Channel A is driven and Channel B has a feedback loop from OUTP through a PA, then OUTP integrates to a voltage value such that

$$OUTB = (OUTA + VLVL)/2 \quad (11)$$

The output value from OUTN may or may not be useful. It is given by

$$OUTN = 0 \text{ V} \quad (12)$$

For VLVL < OUTA/3,

Otherwise,

$$OUTN = (3 \times VLVL - OUTA)/2 \quad (13)$$

If VLVL is connected to OUTA, then OUTB is forced to equal OUTA through the feedback loop. This flexibility provides the user with the capability to measure one channel operating at a given power level and frequency while forcing the other channel to a desired power level at another frequency. ADJA and ADJB should be set to different voltage levels to reduce the temperature drift of the output measurement. The temperature drift will be statistical sum of the drift from Channel A and Channel B. As stated before, VLVL can be used to force the slaved channel to operate at a different power than the other channel. If the two channels are forced to operate at different power levels, then some static offset occurs due to voltage drops across metal wiring in the IC.

If an inversion is necessary in the feedback loop, OUTN can be used as the integrator by placing a capacitor between OUTN and OUTP. This changes the output equation for OUTB and OUTP to

$$OUTB = 2 \times OUTA - VLVL \quad (14)$$

For VLVL < OUTA/2,

$$OUTN = 0 \text{ V} \quad (15)$$

Otherwise,

$$OUTN = 2 \times VLVL - OUTA \quad (16)$$

The previous equations are valid when Channel A is driven and Channel B is slaved through a feedback loop. When Channel B is driven and Channel A is slaved, the above equations can be altered by changing OUTB to OUTA and OUTN to OUTP.

RF MEASUREMENT MODE BASIC CONNECTIONS

The AD8364 requires a single supply of nominally 5 V. The supply is connected to the three supply pins, VPSA, VPSB, and VPSR. Each pin should be decoupled using the two capacitors with values equal or similar to those shown in Figure 60. These capacitors must provide a low impedance over the full frequency range of the input, and they should be placed as close as possible to the VPOS pins. Two different capacitors are used in parallel to provide a broadband ac short to ground.

The input signals are applied to the input differentially. The RF inputs of the AD8364 have a differential input impedance of 200 Ω. When the AD8364 RF inputs are driven from a 50 Ω source, a 4:1 balun transformer is recommended to provide the necessary impedance transformation. The inputs can be driven single-ended, however, this reduces the measurement range of the rms detectors (see the Single-Ended Input Operation section).

Table 4. Baluns Used to Characterize the AD8364

Frequency	Balun
450 MHz	MIA-COM ETK4-2T
880 MHz	Mini-Circuits JTX-4-10T
1880 MHz	Murata LDB181G8820C-110
2140 MHz	Murata LDB212G1020C-001
2500 MHz	Murata LDB182G4520C-110

The device is placed in measurement mode by connecting OUTA and/or OUTB to VSTA and/or VSTB, respectively. This closes the AGC loop within the device with OUT[A, B] representing the VGA control voltage, which is required to present the correct rms voltage at the input of the internal square law detector.

As the input signal to Channel A and Channel B are swept over their nominal input dynamic range of +10 dBm to −50 dBm, the output swings from 0 V to 3.5 V. The voltages OUTA and OUTB are also internally applied to a difference amplifier with a gain of two. So as the dB difference between INA and INB ranges from approximately −30 dB to +30 dB, the difference voltage on OUTP and OUTN swings from −3.5 V to +3.5 V. Input differences larger than ±30 dB can be measured as long as the absolute input level at INA and INB are within their nominal ranges of +10 dBm to −50 dBm. However, measurement of large differences between INA and INB are affected by on-chip signal leakage (see the Channel Isolation section). The common-mode level of OUTP and OUTN is set by the voltage applied to VLVL. These output can be easily biased up to a common-mode voltage of 2.5 V by connecting VREF to VLVL. As the gain range is swept, OUTP swings from approximately 1 V to 4.5 V and OUTN swings from 4.5 V to 1 V.

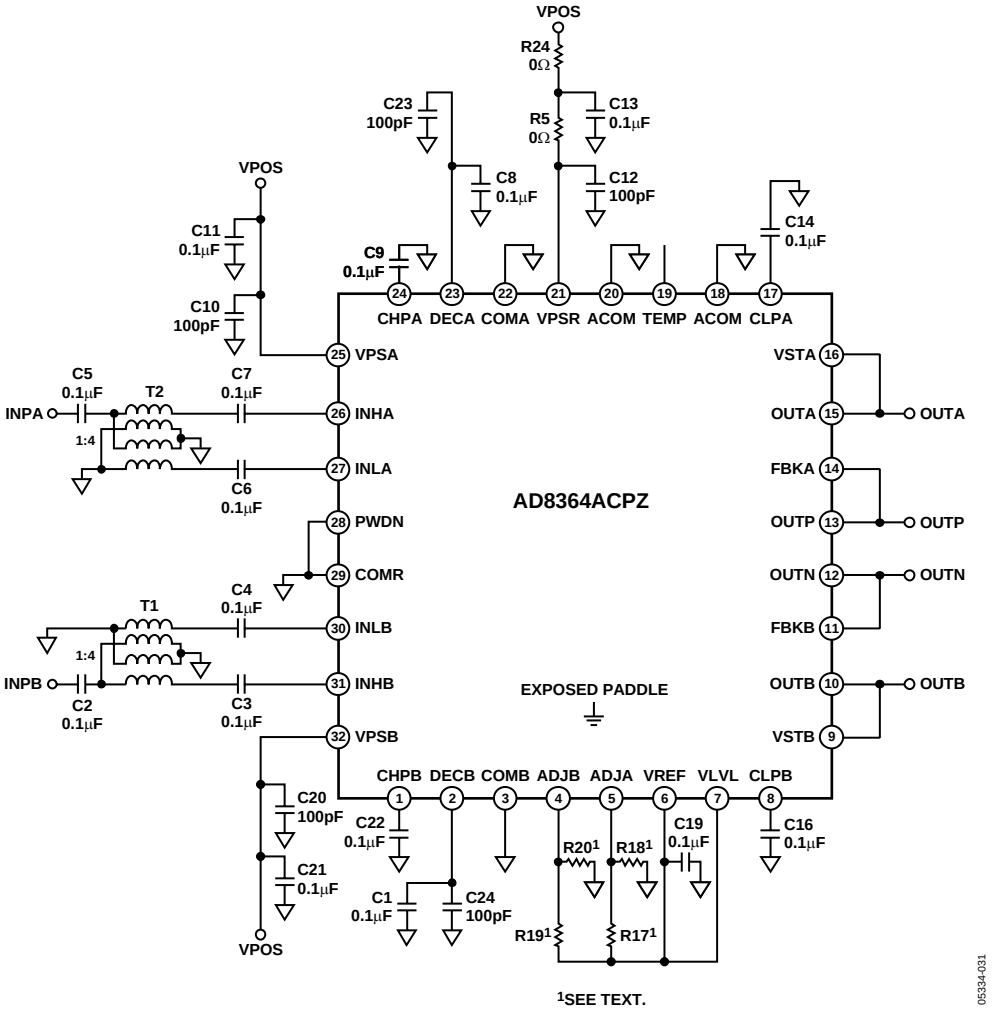


Figure 60. Basic Connections for Operation in Measurement Mode

CONTROLLER MODE BASIC CONNECTIONS

In addition to being a measurement device, the AD8364 can also be configured to measure and control rms signal levels. The AD8364 has two controller modes. Each of the two rms log detectors can be separately configured to set and control the output power level of a variable gain amplifier (VGA) or variable voltage attenuator (VVA). Alternatively, the two rms log detectors can be configured to measure and control the *gain* of an amplifier or signal chain.

Automatic Power Control

Figure 61 shows how the device should be reconfigured to control output *power*.

The RF input to the device is configured as before. A directional coupler taps off some of the power being generated by the VGA (typically a 10 dB to 20 dB coupler is used). A power splitter can be used instead of a directional coupler if there are no concerns about reflected energy from the next stage in the signal chain. Some additional attenuation may be required to set the maximum input signal at the AD8364 to be equal to the recommended maximum input level for optimum linearity and temperature stability at the frequency of operation.

VSTA and OUTA are no longer shorted together. OUTA now provides a bias or gain control voltage to the VGA. The gain control sense of the VGA must be negative and monotonic, that is, increasing voltage tends to decrease gain. However, the gain control transfer function of the device does not need to be well controlled or particularly linear. If the gain control sense of the VGA is positive, an inverting op amp circuit with a dc offset shift can be used between the AD8364 and the VGA to keep the gain control voltage in the 0 V to 5 V range.

VSTA becomes the setpoint input to the system. This can be driven by a DAC, as shown in Figure 61, if the output power is expected to vary, or it can simply be driven by a stable reference voltage if constant output power is required. This DAC should have an output swing that covers the 0 V to 3.5 V range. The AD7391 and AD7393 serial-input and parallel-input 10-bit DACs provide adequate resolution (4 mV/bit) and an output swing up to 4.5 V.

When VSTA is set to a particular value, the AD8364 compares this value to the equivalent input power present at the RF input. If these two values do not match, OUTA increases or decreases in an effort to balance the system. The dominant pole of the error amplifier/integrator circuit that drives OUTA is set by the capacitance on Pin CLPA; some experimentation may be necessary to choose the right value for this capacitor. In general, CLPA should be chosen to provide stable loop operation for the complete output power control range. If the slope (in dB/V) of the gain control transfer function of the VGA is not constant, CLPA must be chosen to guarantee a stable loop when the gain control slope is at its maximum. On the other hand, CLPA must provide adequate averaging to the internal low range squaring detector so that the rms computation is valid. Larger values of CLPA tend to make the loop less responsive.

The relationship between VSTA and the RF input follows from the measurement mode behavior of the device. For example, from Figure 9, which shows the measurement mode transfer function at 880 MHz, it can be seen that an input power of −10 dBm yields an output voltage of 2.5 V. Therefore, in controller mode, VSTA should be set to 2.5 V, which results in an input power of −10 dBm to the AD8364.

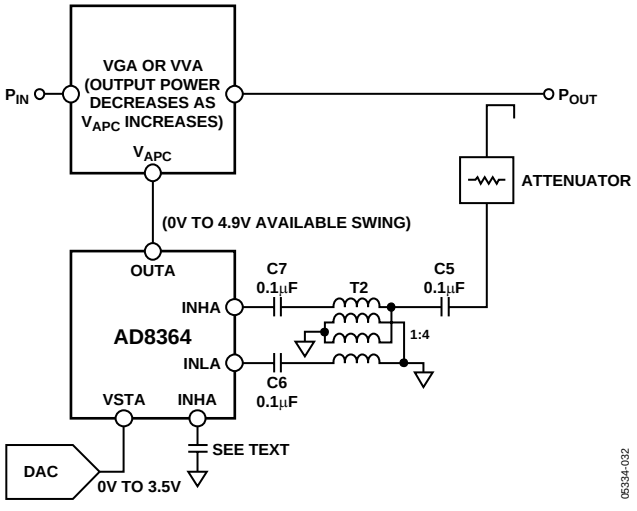


Figure 61. Operation in Controller Mode for Automatic Power Control

Automatic Gain Control

Figure 62 shows how the AD8364 can be connected to provide automatic *gain* control to an amplifier or signal chain. Additional pins are omitted for clarity. In this configuration, both rms detectors are connected in measurement mode with appropriate filtering being used on CLP[A, B] to effect a valid rms computation on both channels. OUTA, however, is also connected to the VLVL pin of the on-board difference amplifier. Also, the OUTP output of the difference amplifier drives a variable gain element (either VVA or VGA) and is connected back to the FBKA input via a capacitor so that it is operating as an integrator.

Assume that OUTA is much bigger than OUTB. Because OUTA also drives VLVL, this voltage is also present on the noninverting input of the op amp driving OUTP. This results in a net current flow from OUTP through the integrating capacitor into the FBKA input. This results in the voltage on OUTP increasing. If the gain control transfer function of the VVA/VGA is positive, this increases the gain, which in turn increases the input signal to INHB. The output voltage on the integrator continues to increase until the power on the two input channels is equal, resulting in a signal chain gain of unity.

If a gain other than 0 dB is required, an attenuator can be used in one of the RF paths, as shown in Figure 62. Alternatively, power splitters or directional couplers of different coupling factors can be used. Another convenient option is to apply a voltage on VLVL other than OUTA. Refer to Equation 11 and the Controller Mode section for more detail.

If the VGA/VVA has a negative gain control sense, the OUTN output of the difference amplifier can be used with the integrating capacitor tied back to FBKB.

The choice of the integrating capacitor affects the response time of the AGC loop. Small values give a faster response time but can result in instability, whereas larger values reduce the response time. Note that in this mode, the capacitors on CLPA and CLPB, which perform the rms averaging function, must still be used and also affect the loop response time.

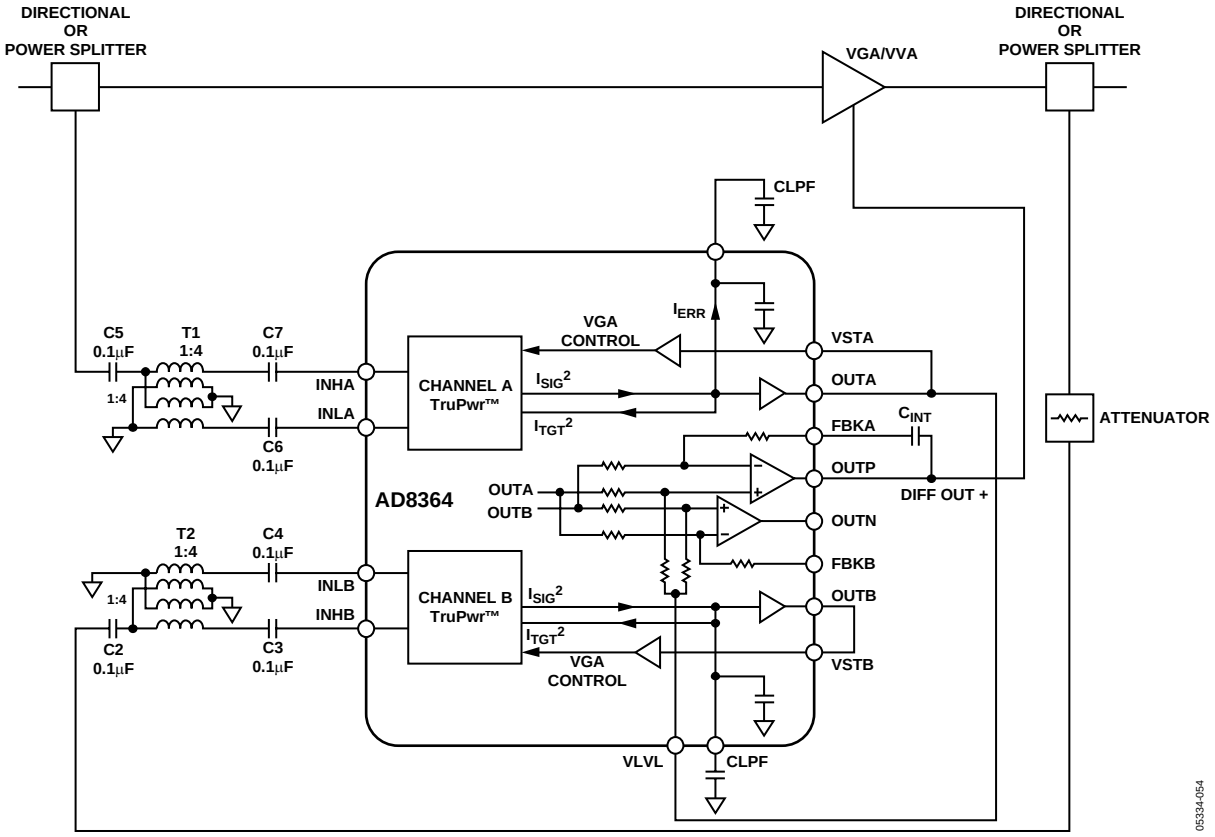


Figure 62. Operation in Controller Mode for Automatic Gain Control

CONSTANT OUTPUT POWER OPERATION

In controller mode, the AD8364 can be used to hold the output power stable over a broad temperature/input power range. This can be very useful in systems, such as a transmit module driving a high power amplifier (HPA) in a basestation, that connect multiple power sensitive modules together. In applications where stable output power is needed, the RF output is connected to Channel B using a coupler, VLVL is connected to VREF, VSTB is used to set the power to a particular level and can be controlled using a DAC or a dc voltage, OUTB is used to drive the gain control of an amplifier that is capable of negative-gain law conformance (such as the AD8367), and ADJB (set at 0 V in this example) is used to control the temperature drift. Using this configuration, the RF input signal is down converted to 80 MHz using the AD8343 and amplified using the AD8367. The signal then splits and part of it is fed back to the AD8364 through Channel B, and a setpoint voltage is applied to VSTB. This voltage corresponds to a particular power level, which is determined by the slope of the AD8364. The power detected at the input of the AD8364 is compared with this voltage, and the voltage present at OUTB is adjusted up or down to match the setpoint voltage, with the power detected on the input. The OUTB voltage is connected to the gain control of the AD8367 VGA and increases or decreases the gain of the AD8367, resulting in the output power being held constant, regardless of variations in the input power. The AD8364 is able to maintain a fixed output power from the AD8367 even though its input power is changing. The input power can vary over a 36 dB range, while the output power remains constant and the drift over temperature is less than 0.2 dB

Figure 64 shows a constant output power circuit using the AD8364 and the AD8367 VGA. The input power was swept from +3 dBm to −35 dBm, the output power was measured at multiple temperatures between −40°C and +85°C, and the power changed less than ±0.07 dB (Figure 63).

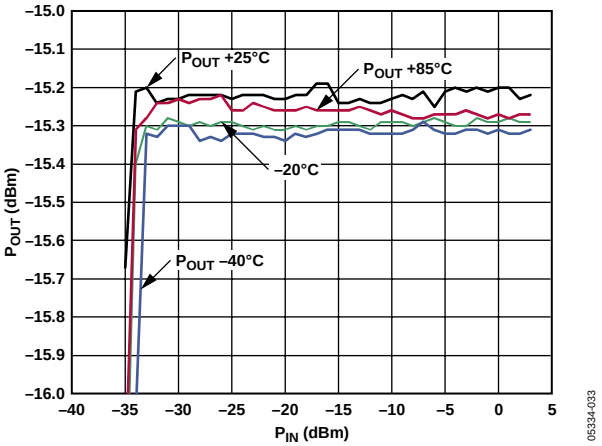


Figure 63. AD8364 Constant Power Performance

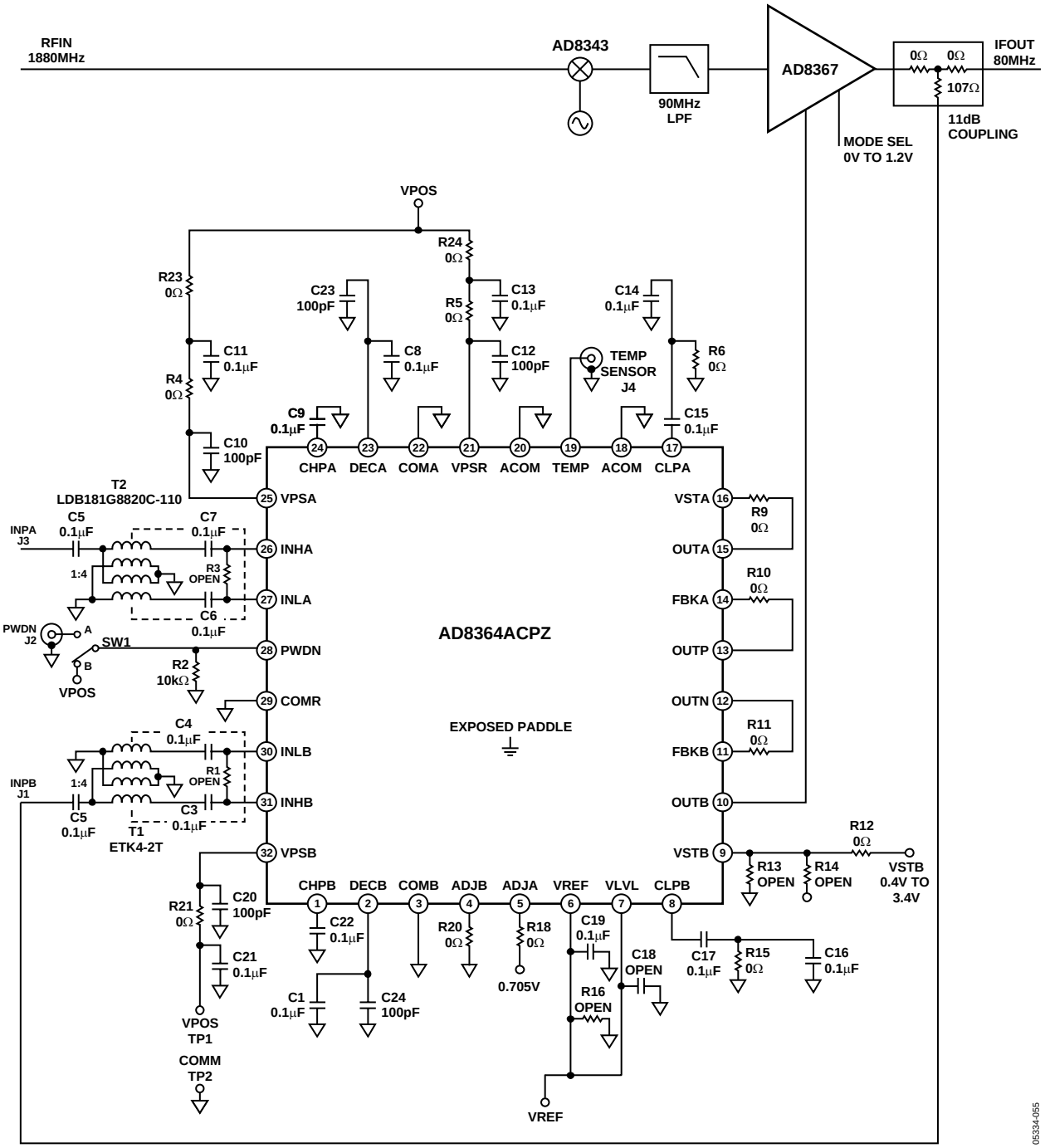


Figure 64. Constant Output Power Circuit

GAIN-STABLE TRANSMITTER/RECEIVER

There are many applications for a transmitter or receiver with a highly accurate temperature-stable gain. For example, a multicarrier basestation high power amplifier (HPA) using digital predistortion has a power detector and an auxiliary receiver. The power detector and all parts associated with it can be removed if the auxiliary receiver has a highly accurate temperature-stable gain. With a set gain receiver, the ADC on the auxiliary receiver can not only determine the overall power being transmitted but can also determine the power in each carrier for a multicarrier HPA.

In controller mode, the AD8364 can be used to hold the receiver gain constant over a broad input power/temperature range. In this application, the difference outputs are used to hold the receiver gain constant.

The RF input is connected to INPA, using a 19.1 dB coupler, and the down converted output from our signal chain is connected to INPB, using a 10.78 dB coupler. A 0.1 µF capacitor is connected between FBKA and OUTP, forming an integrator. OUTA is connected to VLVL, forcing OUTP to adjust the VGA so that OUTB is equal to OUTA. The circuit gain is set by the difference in the coupling values of the input and output couplers. As noted, OUTP is used to drive the gain control of the ADL5330 by adjusting the gain up or down as needed to force the power at the AD8364 inputs to be equal in amplitude. Since operating at different frequencies, the appropriate voltages on the ADJ[A, B] pins must be supplied. Because INPA is operating at 1880 MHz, ADJA is set to 0.75 V. Likewise, because INPB is operating at 80 MHz, ADJB is set to 0 V.

Because the difference in the coupler values is 8.32 dB, a fixed gain of −8.32 dB is expected. In practice, there is a gain of −13 dB. This is caused by the intercept shift of the AD8364 due to its frequency response, the insertion loss of the output coupler, and the insertion loss differences of the baluns used on the input of the AD8364. In this configuration, approximately 33 dB of control range with 0.5 dB drift over temperature is obtained.

Figure 66 shows a gain-stable receiver amplifier circuit using the AD8364 to control an ADL5330 VGA and the AD8343 mixer. The input power was swept from +3 dBm to −35 dBm, the output power was measured, and the gain was calculated at multiple temperatures between −40°C and +85°C. Note that the gain changed less than ±0.45 dB over this range (Figure 65). Most of the gain change was caused by performance differences at different frequencies.

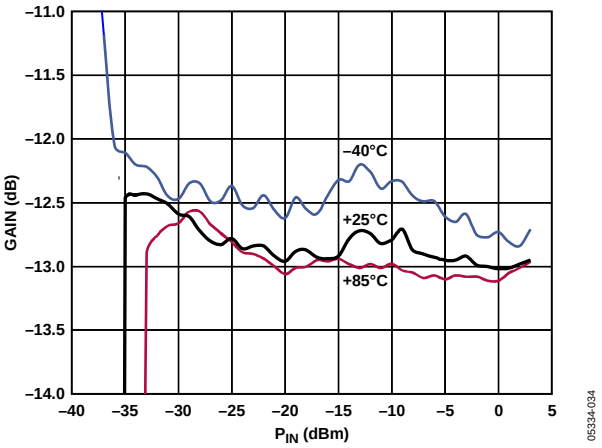


Figure 65. Performance of Gain-Stable Receiver

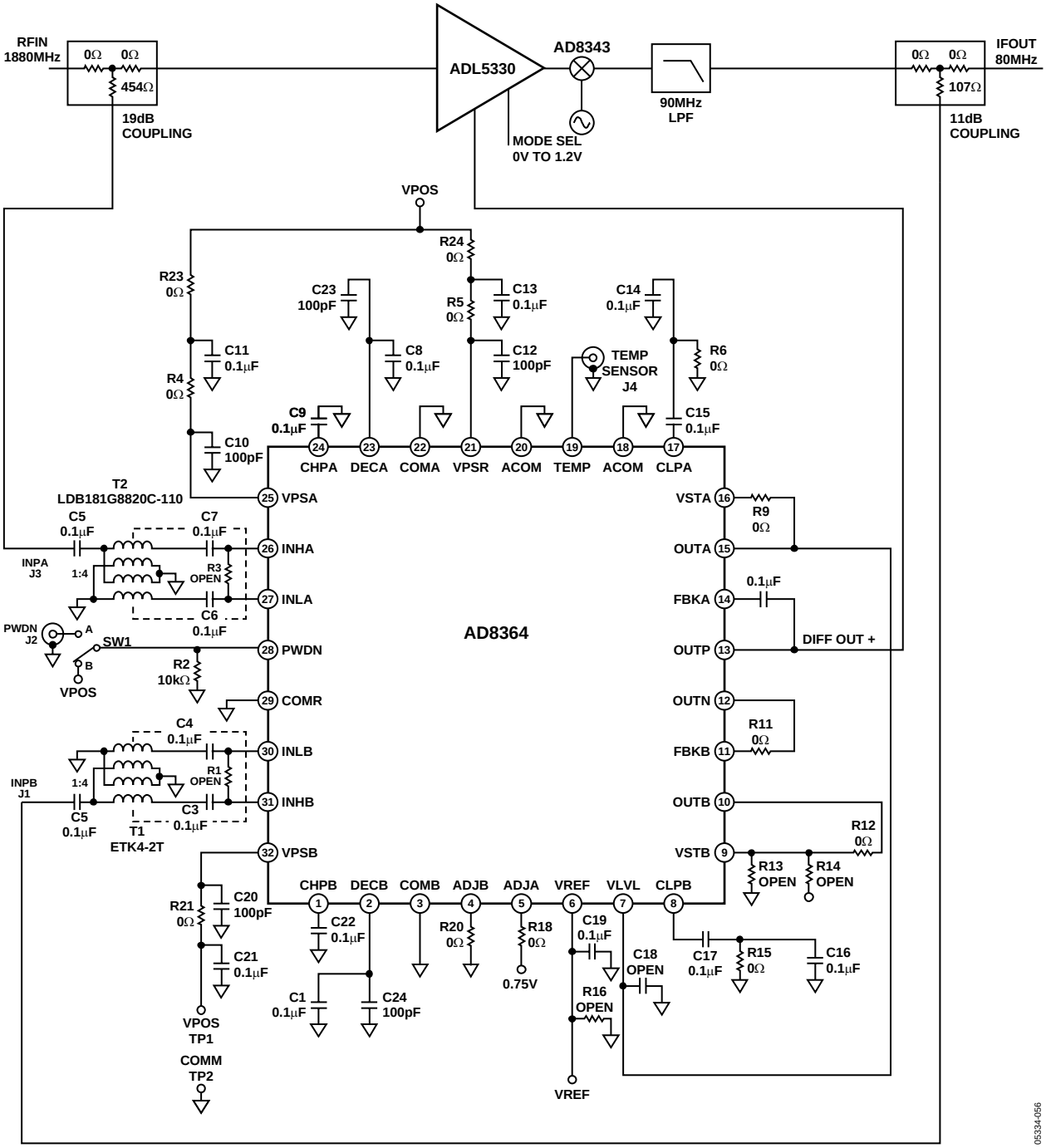


Figure 66. Gain-Stable Receiver Circuit

TEMPERATURE COMPENSATION ADJUSTMENT

The AD8364 has a highly stable measurement output with respect to temperature. However, when the RF inputs exceed a frequency of 600 MHz, the output temperature drift must be compensated for using ADJ[A, B] for optimal performance. Proprietary techniques are used to compensate for the temperature drift. The absolute value of compensation varies with frequency, balun choice, and circuit board material. Table 5 shows recommended voltages for ADJ[A, B] to maintain a temperature drift error of typically ±0.5 dB or better over the entire rated temperature range with the recommended baluns.

Table 5. Recommended Voltages for ADJ[A, B]

Frequency (MHz)	450	880	1880	2140	2500
ADJ[A, B] (V)	0	0.5	0.65	0.85	1.10

Compensating the device for temperature drift using ADJ[A, B] allows for great flexibility. If the user requires minimum temperature drift at a given input power or subset of the dynamic range, the ADJ[A, B] voltage can be swept while monitoring OUT[A, B] over temperature. Figure 67 shows the result of such an exercise with a broadband balun, one that is not the recommended balun at 1880 MHz. The value of ADJ[A, B] where the output has minimum movement (approximately 0.77 V for the example in Figure 67) is the recommended voltage for ADJ[A, B] to achieve minimum temperature drift at a given power and frequency.

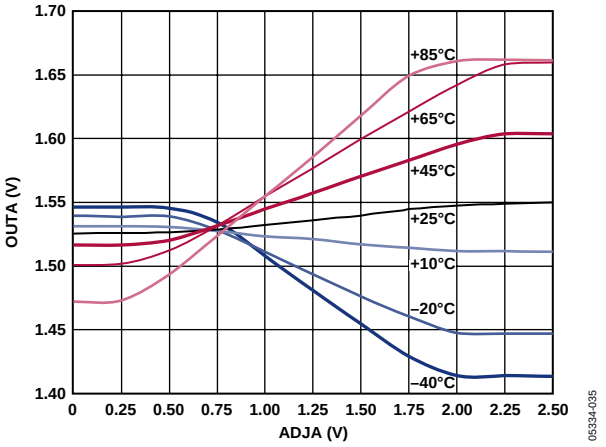


Figure 67. OUTA vs. ADJA over Temp. Pin = –30 dBm, 1.9 GHz

The ADJ[A, B] input has high input impedance. The input can be conveniently driven from an attenuated value of VREF using a resistor divider, if desired.

Figure 68 shows a simplified schematic representation of the ADJ[A, B] interface.

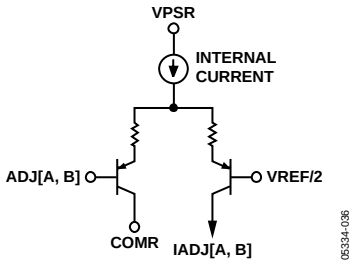


Figure 68. ADJ[A, B] Interface Simplified Schematic

DEVICE CALIBRATION AND ERROR CALCULATION

The measured transfer function of the AD8364 at 2.14 GHz is shown in Figure 69. The figure shows plots of both output voltage vs. input power and calculated error vs. input power. As the input power varies from −50 dBm to 0 dBm, the output voltage varies from 0.4 V to about 2.8 V.

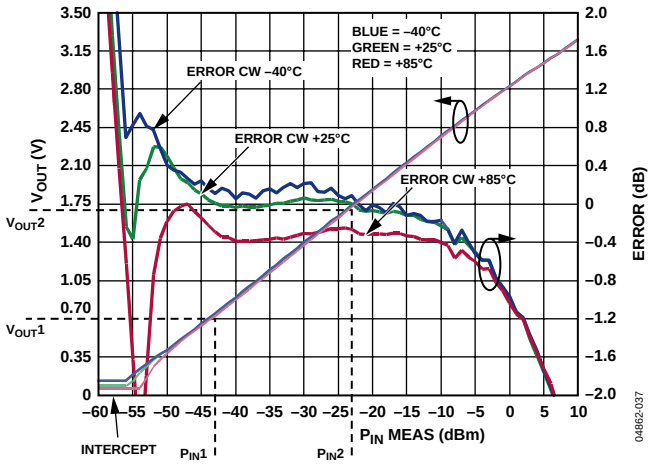


Figure 69. Transfer Function at 2.14 GHz.

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. The equation for output voltage can be written as

$$V_{OUT} = Slope \times (P_{IN} - Intercept)$$

Where *Slope* is the change in output voltage divided by the change in power (dB), and *Intercept* is the calculated power at which the output voltage would be 0 V. (Note that *Intercept* is a theoretical value; the output voltage can never achieve 0 V).

In general, the calibration is performed by applying two known signal levels to the AD8364's input and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear-in-dB operating range of the device (see the Specifications section for more details).

Calculation of the slope and intercept is done using the equations:

$$Slope = (V_{OUT1} - V_{OUT2})/(P_{IN1} - P_{IN2})$$

$$Intercept = P_{IN1} - (V_{OUT1}/Slope)$$

Once slope and intercept have been calculated, an equation can be written that will allow calculation of the input power based on the output voltage of the detector.

$$P_{IN}\ (unknown) = (V_{OUT1(measured)}/Slope) + Intercept$$

The log conformance error of the calculated power is given by

$$Error\ (\text{dB}) = (V_{OUT(\text{MEASURED})} - V_{OUT(IDEAL)})/Slope$$

Figure 69 includes a plot of the error at 25°C, the temperature at which the log amp is calibrated. Note that the error is not zero. This is because the log amp does not perfectly follow the ideal V_{OUT} vs. P_{IN} equation, even within its operating region. The error at the calibration points (−43 dBm and −23 dBm in this case) will, however, be equal to zero by definition.

Figure 69 also includes error plots for the output voltage at −40°C and +85 °C. These error plots are calculated using the slope and intercept at 25°C. This is consistent with calibration in a mass-production environment, where calibration at temperature is not practical.

SELECTING CALIBRATION POINTS TO IMPROVE ACCURACY OVER A REDUCED RANGE

In some applications, very high accuracy is required at one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power.

Figure 70 shows the same measured data as Figure 69. Notice that accuracy is very high from −10 dBm to −25 dBm. At approximately −45 dBm, the error increases to about −0.3 dB because the calibration points have been changed to −15 dBm and −25 dBm.

Calibration points should be chosen to suit the application at hand. In general, though, do not choose calibration points in the nonlinear portion of the log amp's transfer function (above 0 dBm or below −50 dBm in this case).

Figure 71 shows how calibration points can be adjusted to increase dynamic range, but at the expense of linearity. In this case, the calibration points for slope and intercept are set at −1 dBm and −50 dBm. These points are at the end of the device's linear range. At 25°C, there is an error of 0 dB at the calibration points. Note also that the range over which the AD8364 maintains an error of <±0.4 dB is extended to 57 dB at 25°C. The disadvantage of this approach is that linearity suffers, especially at the top end of the input range.

Another way of presenting the error function of a log amp detector is shown in Figure 72. In this case, the dB error at hot and cold temperatures is calculated with respect to the *output voltage* at ambient. This is a key difference in comparison to the previous plots, in which all errors have been calculated with respect to the *ideal transfer function* at ambient.

When the alternative technique, the error at ambient becomes by definition equal to 0 (see Figure 72).

This would be valid if the device transfer function perfectly followed the ideal V_{OUT} = Slope × (P_{IN} − Intercept) equation. However, since an rms amp, in practice, never perfectly follows this equation (especially outside of its linear operating range), this plot tends to artificially improve linearity and extend the dynamic range, unless enough calibration points were taken to remove the error. This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) output voltage at ambient.

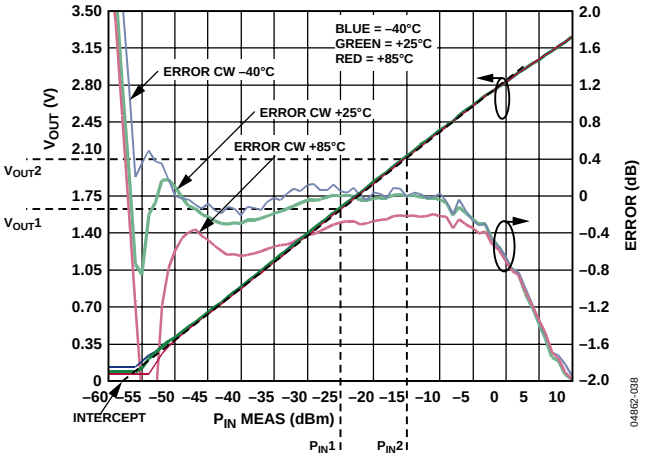


Figure 70. Output Voltage and Error vs. P_{IN} with 2-Point Calibration at –15 dBm and –25 dBm, 2.14 GHz

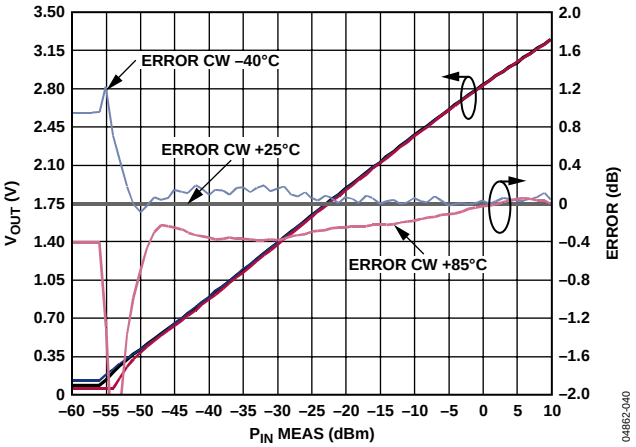


Figure 72. Error vs. Temperature with Respect to Output Voltage at 25 °C, 2.14 GHz (Does Not Account for Transfer Function Nonlinearities at 25°C)

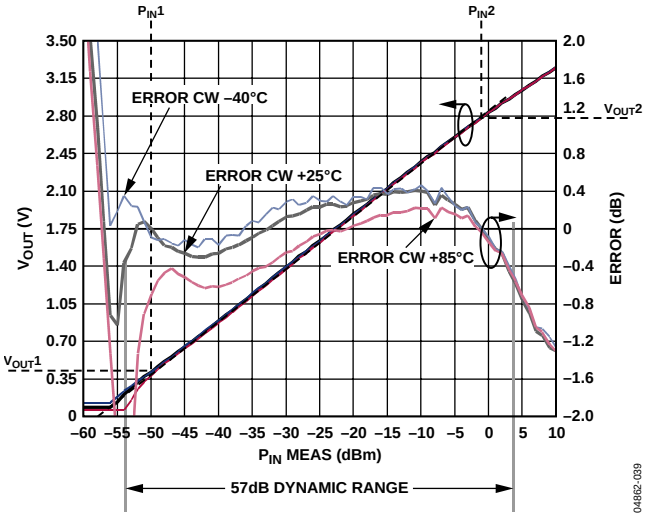


Figure 71. Dynamic Range Extension by Choosing Calibration Points that are Close to the End of the Linear Range, 2.14 GHz

ALTERING THE SLOPE

None of the changes to operating conditions discussed so far affect the logarithmic slope, V_{SLOPE}, in Equation 7. The slope can readily be altered by controlling the fraction of OUT[A, B] that is fed back to the setpoint interface at the VST[A, B] pin. When the full signal from OUT[A, B] is applied to VST[A, B], the slope assumes its nominal value of 50 mV/dB. It can be increased by including a voltage divider between these pins, as shown in Figure 73. Moderately low resistance values should be used to minimize scaling errors due to the approximately 70 kΩ input resistance at the VST[A, B] pin. Keep in mind that this resistor string also loads the output, and it eventually reduces the load-driving capabilities if very low values are used. Equation 17 can be used to calculate the resistor values.

$$R1 = R2' (S_D/50 - 1) \quad (17)$$

where:
S_D is the desired slope, expressed in mV/dB.
$R2'$ is the value of R2 in parallel with 70 kΩ.

For example, using R1 = 1.65 kΩ and R2 = 1.69 kΩ ($R2'$ = 1.649 kΩ), the nominal slope is increased to 100 mV/dB. This choice of scaling is useful when the output is applied to a digital voltmeter because the displayed number directly reads as a decibel quantity with only a decimal point shift.

Operating at a high slope is useful when it is desired to measure a particular section of the input range in greater detail. A measurement range of 60 dB would correspond to a 6 V change in VOUT at this slope, exceeding the capacity of the AD8364's output stage when operating on a 5 V supply. This requires that the intercept is repositioned to place the desired input range section within a window corresponding to an output range of 0.1 V ≤ VOUT ≤ 4.8 V, a 47 dB range.

Using the arrangement shown in Figure 74, an output of 0.4 V corresponds to the lower end of the desired range, and an output of 3.5 V corresponds to the upper limit with 3 dB of margin at each end of the range, nominally −32 dBm to −1 dBm with the intercept at −35.6 dBm. Note that R2 is connected to VREF rather than ground. R3 is needed to ensure that the AD8364's reference buffer is correctly loaded.

When the slope is raised by some factor, the loop capacitor, CLP[A, B], should be raised by the same factor to ensure stability and to preserve a chosen averaging time. The slope can be lowered by placing a voltage divider after the output pin, following standard practice.

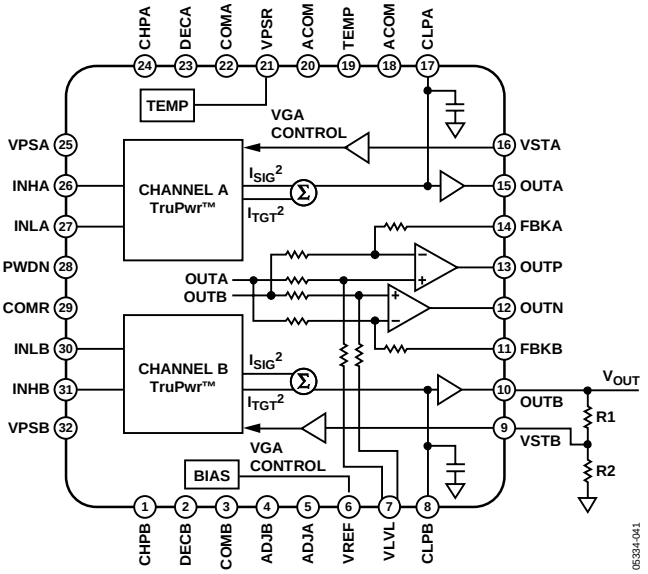


Figure 73. External Network to Raise Slope

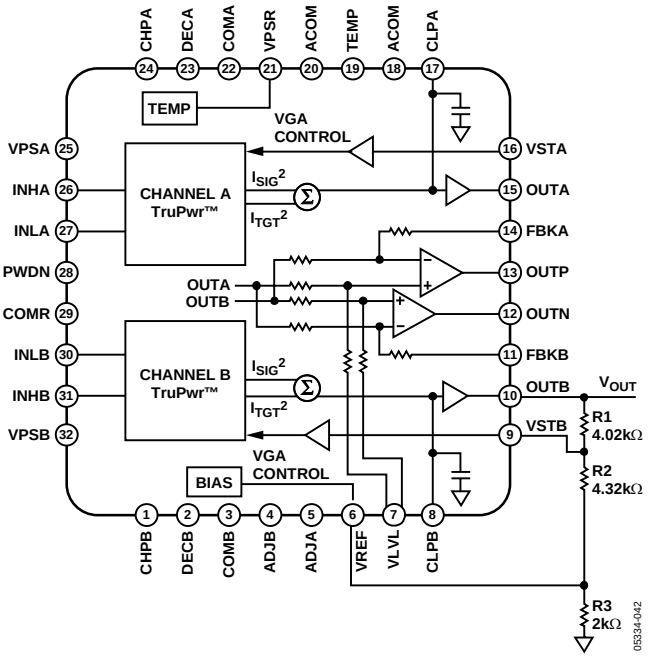


Figure 74. Scheme Providing 100 mV/dB Slope for Operation over a 3 mV to 300 mV Input Range

CHANNEL ISOLATION

Isolation must be considered when using both channels of the AD8364 at the same time. The two isolation requirements that should be considered are the isolation from one RF channel input to the other RF channel input and the isolation from one RF channel input to the other channel output. When using both channels of the AD8364, care should be taken in the layout to isolate the RF inputs from each other. Coupling on the PC board affects both types of isolation.

In most applications, the designer has the ability to adjust the power going into the AD8364 through the use of different valued temperature-stable couplers and accurate temperature-stable attenuators. When isolation is a concern, it is useful to adjust the input power so the lowest expected detectable power is not far from the lowest detectable power of the AD8364 at the frequency of operation. The AD8364's lowest detectable power point has little variation from part to part and is not affected by the balun. This equalizes the signals on both channels at their lowest possible power level, which reduces the overall isolation requirements and possibly adds attenuators to the RF inputs of the device, reducing the RF channel input isolation requirements.

Measuring the RF channel input to the other RF channel input isolation is straight forward, and the result of such an exercise is shown in Figure 75. Note that adding an attenuator in series with the RF signal increases the channel input-to-input isolation by the value of the attenuator.

The isolation between one RF channel input and the other channel output is a little more complicated. Do not assume that worst-case isolation happens when one RF channel has high power and the other RF channel is set at its lowest detectable power. Worst-case isolation happens when the low power channel is at a nominally low power level, as chosen in Figure 76. If the inputs to both RF channels are at the same frequency, the isolation also depends on the phase shift between the RF signals put into the AD8364. This can be seen by placing a high power signal on one RF channel input and another signal (low power) slightly offset in frequency to the other RF channel. If the output of the low power channel is observed with an oscilloscope, it would have a ripple that would look similar to a full-wave rectified sine wave with a frequency equal to the frequency difference between the two channels, that is, a beat tone. The magnitude of the ripple reflects the isolation at a specific phase offset (note that two signals of slightly different frequencies act like two signals with a constantly changing phase), and the frequency of that ripple is directly related to the frequency offset. The data taken in Figure 76 assumes worst-case amplitude and phase offset. If the RF signals on Channel A and Channel B are at significantly different frequencies, the input-to-output isolation increase, depending on the capacitors placed on CLP[A, B] and CHP[A, B] and the frequency offset of the two signals (Figure 77), due to the response roll-off within AD8364.

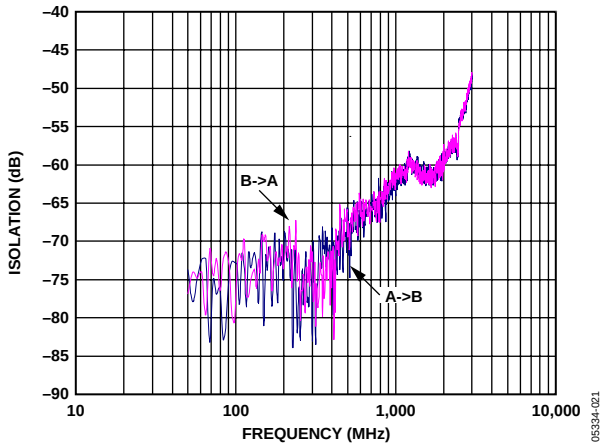


Figure 75. RF Channel Input-to-Input Isolation

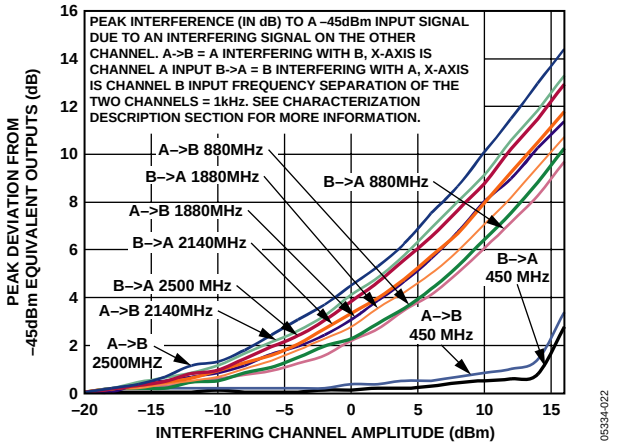


Figure 76. Apparent Measurement Error Due to Overall Channel-to-Channel Cross-Coupling

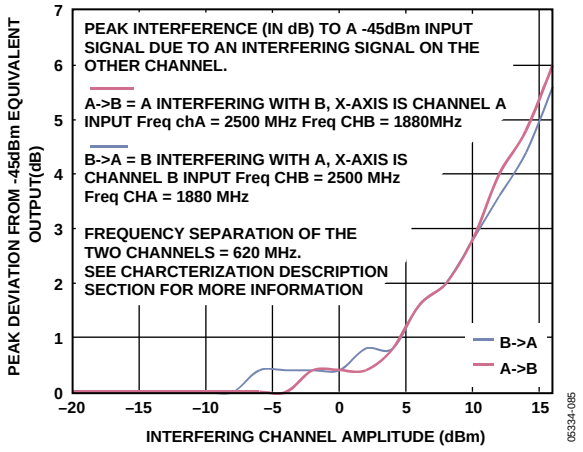


Figure 77. Improved Measurement Error with Increased Frequency Separation

CHOOSING THE RIGHT VALUE FOR CHP[A, B] AND CLP[A, B]

The AD8364's VGA includes an offset cancellation loop, which introduces a high-pass filter effect in its transfer function. The corner frequency, f_{HP}, of this filter must be below that of the lowest input signal in the desired measurement bandwidth frequency to properly measure the amplitude of the input signal. The required value of the external capacitor is given by

$$CHP[A, B] = 200\ \mu F/(2 \times \pi \times f_{HP})(f_{HP}\ in\ Hz) \quad (18)$$

Thus, for operation at frequencies down to 100 kHz, CHP[A, B] should be 318 pF.

In the standard connections for the measurement mode, the VST[A, B] pin is tied to OUT[A, B]. For small changes in input amplitude (a few decibels), the time-domain response of this loop is essentially linear with a 3 dB low-pass corner frequency of nominally $f_{LP} = 1/(2 \times \pi \times CLP[A, B] \times 1.1\ k\Omega)$. Internal time delays around this local loop set the minimum recommended value of this capacitor to about 300 pF, making f_{LP} = 482 kHz.

For operation at lower signal frequencies, or whenever the averaging time needs to be longer, use

$$CLP[A, B] = 900\ \mu F/2 \times \pi \times f_{LP}\ (f_{LP}\ in\ Hz) \quad (19)$$

When the input signal exhibits large crest factors, such as a WCDMA signal, CLP[A, B] must be much larger than might at first seem necessary. This is due to the presence of significant low frequency components in the complex, pseudo random modulation, which generates fluctuations in the output of the AD8364.

RF BURST RESPONSE TIME

RF burst response time is important for modulated signals that have large steps in power, such as a single carrier EVDO that has the potential for a greater than 20 dB burst of power (for approximately 200 µs out of every 800 µs).

Accurate power detection for signals with RF bursts is achieved when the AD8364 is able to respond quickly to the change in RF power; however, the response time is limited by the capacitors placed on Pins CLP[A, B], CHP[A, B], and DEC[A, B].

Capacitors placed on the DEC[A, B] pins affect the response time the least and should be chosen as stated in the RF Input Interface section. Capacitors placed on CHP[A, B] and CLP[A, B] should be chosen according to the equations in the Choosing the Right Value for CHP[A, B] and CLP[A, B] section and the response time for the AD8364 should be evaluated. If the response time is not fast enough to follow the burst response, the values for CLP[A, B] should be decreased. The capacitor values placed on the CLP[A, B] have the largest effect on the rise and fall times. The capacitor values placed on CHP[A, B] affect the rising and falling corner of the response (overshoot or under-shoot); however, the falling corner is most likely swamped out by the effect of CLP[A, B].

Once the response time is set so that the AD8364 is just able to follow the RF burst requirements (within the tolerance of the capacitors), the output of the AD8364 should be evaluated with an oscilloscope. If there is ripple on the output (due to the modulated signal), averaging may need to be performed on the DSP to achieve a true rms response. Figure 44 and Figure 45 may help in determining the proper CLP[A, B] values to use.

SINGLE-ENDED INPUT OPERATION

For optimum operation, the RF inputs to the AD8364 should be driven differentially. However, the AD8364 RF inputs can also be driven in a single-ended configuration with reduced dynamic range. Figure 78 shows a recommended input configuration for a single channel.

Figure 79 shows the performance obtained with the configuration shown in Figure 78. The user should note that the dynamic range performance suffers in single-ended configuration due to the inherent amplitude and phase imbalance at the RF inputs. However, at low frequency the dynamic range is quite good and users trying to detect low frequency or baseband signals may want to consider this as an option. At frequencies greater than 450 MHz, the dynamic range decreases to about 20 dB, reducing the AD8364's usefulness for many applications. Performance in single-ended configuration is subject to circuit board layout (see the Printed Circuit Board Considerations section).

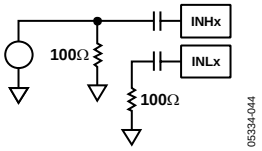


Figure 78. Recommended Input Configuration for Single-Ended Input Drive

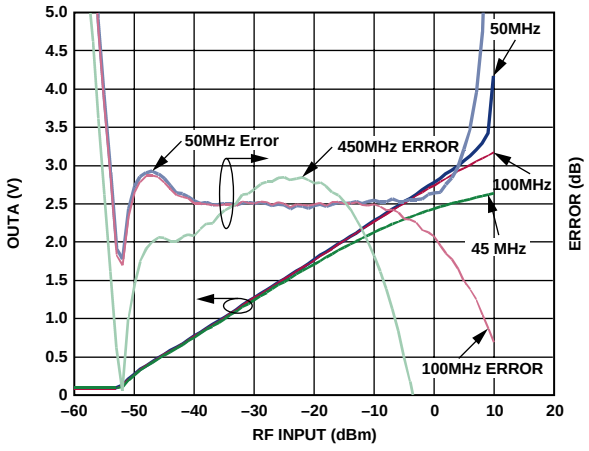


Figure 79. Single-Ended Performance for the Configuration Shown in Figure 78

PRINTED CIRCUIT BOARD CONSIDERATIONS

Each RF input pin of the AD8364 presents 100 Ω impedance relative to their respective ac grounds. To ensure that signal integrity is not seriously impaired by the printed circuit board (PCB), the relevant connection traces should provide appropriate characteristic impedance to the ground plane. This can be achieved through proper layout. When laying out an RF trace with controlled impedance, consider the following:

- When calculating the RF line impedance, take into account the spacing between the RF trace and the ground on the same layer.
- Ensure that the width of the microstrip line is constant and that there are as few discontinuities, such as component pads, as possible along the length of the line. Width variations cause impedance discontinuities in the line and may result in unwanted reflections.
- Do not use silkscreen over the signal line because it can alter the line impedance.
- Keep the length of the RF input traces as short as possible.

Figure 80 shows the cross section of a PC board, and Table 6 shows two possible sets of dimensions that provide a 100 Ω line impedance for FR-4 board material with ε_r = 4.6 and Rodgers 4003 board material with ε_r = 3.38.

Table 6. Possible Trace Dimensions for Z_O = 100 Ω

Dimension	FR-4 (mil)	Rodgers 4003 (mil)
W	22	6
H	53	11
T	2	0.7

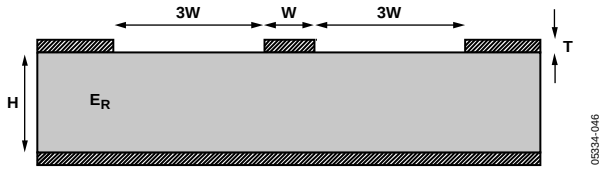


Figure 80. Cross-Section View of a PC Board

It is possible to approximate a 100 Ω trace on a board designed with the 50 Ω dimensions above by removing the ground plane within three line widths of the area directly below the trace. However, more predictable performance may be obtained with precise ground plane spacing. It is possible to design a circuit board with two ground planes, one plane for areas with 50 Ω characteristic impedance and another for areas with 100 Ω characteristic impedance. If the 100 Ω plane is placed below the 50 Ω plane, then an opening can be made in the 50 Ω plane to allow the 100 Ω traces to work against the 100 Ω ground plane. The two ground planes should be connected together with as many vias as possible.

The accurate measurement range (that is, the dynamic range) of AD8364's detectors is sensitive to amplitude and phase matching of the signals presented at the differential inputs. Care should be taken to ensure matching of these parameters and to minimize parasitic capacitance on the RF inputs when laying out the PC board. It is also suggested that the two traces associated with each differential input be mirror images, or duplicates, of one another where possible. A high quality balun with known output magnitude and phase characteristics is recommended to perform single-ended to balanced conversions. It is possible to improve the dynamic range by skewing the amplitude and phase matching at the input. See the Typical Performance Characteristics section for more details.

Stable, low ESR capacitors are *mandatory* in the RF circuitry of the AD8364. This corresponds to capacitors connected to Pins INH[A, B], INL[A, B], DEC[A, B], and CHP[A, B]. High ESR capacitors may result in amplitude and phase mismatch at the differential inputs, which in turn results in low dynamic range. Capacitors with poor aging characteristics under temperature cycling have been shown to accentuate the temperature drift during operation of the AD8364. Use of Samsung CL10 series multilayer ceramic capacitors (or similar) in the RF area are recommended.

High transient and noise levels on the power supply, ground, and inputs should be avoided. This reinforces the need for proper supply bypassing and decoupling. See the Evaluation Boards for suggestions.

A solder appropriate for either the lead-free or leaded version of the AD8364 should be chosen. After the circuit board has been soldered, it is important to thoroughly clean all excess solder flux and residues from the board. Any residual material may act as stray parasitic capacitance, which could result in degraded performance.

PACKAGE CONSIDERATIONS

The AD8364 uses a compact 32-lead LFCSP. A large exposed paddle on the bottom of the device provides both a thermal benefit and a low inductance path to ground for the circuit. To make proper use of this packaging feature, the PCB RF/dc common ground reference needs to make contact directly under the device with as many vias as possible to lower the inductance and thermal impedance.

DESCRIPTION OF CHARACTERIZATION

The general hardware configuration used for most of the AD8362 characterization is shown in Figure 81. The signal sources used in this example are the Rohde & Schwarz SMIQ03B and Agilent E4438C. Input-matching baluns are used to transform the single-ended RF signal to its differential form. Due to the differential inputs' sensitivity to amplitude and phase mismatch, specific baluns were used for each characterization frequency to achieve the best performance.

Other selected configurations are shown in Figure 82 and Figure 83 as well.

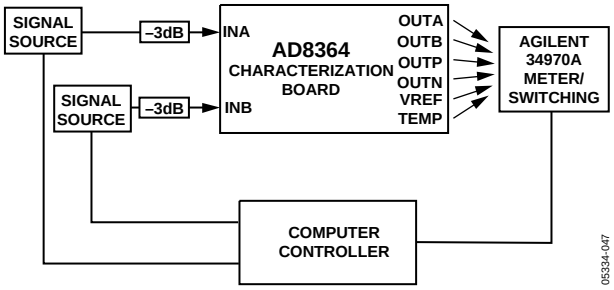


Figure 81. General Characterization Configuration

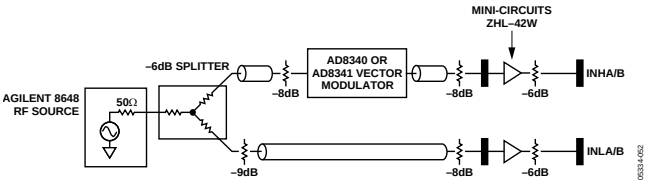


Figure 82. Configuration for Amplitude and Phase Mismatch Characterization

BASIS FOR ERROR CALCULATIONS

The slope and intercept are derived using the coefficients of a linear regression performed on data collected in its central operating range. Error is stated in two forms: (1) error from linear response to CW waveform and (2) output delta from 25°C performance.

The error from linear response to CW waveform is the decibel difference in output from the ideal output defined by the conversions gain and output reference. This is a measure of the linearity of the device response to both CW and modulated waveforms. The error in dB is calculated by

$$\text{Error (dB)} = \frac{V_{OUT} - Slope \times \left(P_{IN} - P_Z\right)}{Slope}$$

where P_Z is the x-axis intercept expressed in dBm. This is analogous to the input amplitude that would produce an output of 0 V, if such an output was possible.

Error from the linear response to the CW waveform is not a measure of absolute accuracy, since it is calculated using the slope and intercept of each device. However, it verifies the linearity and the effect of modulation on the device's response. Similarly, error from 25°C performance uses the 25°C performance of a given device and waveform type as the reference from which all other performance parameters shown alongside it are compared. It is predominantly (and most often) used as a measurement of output variation with temperature.

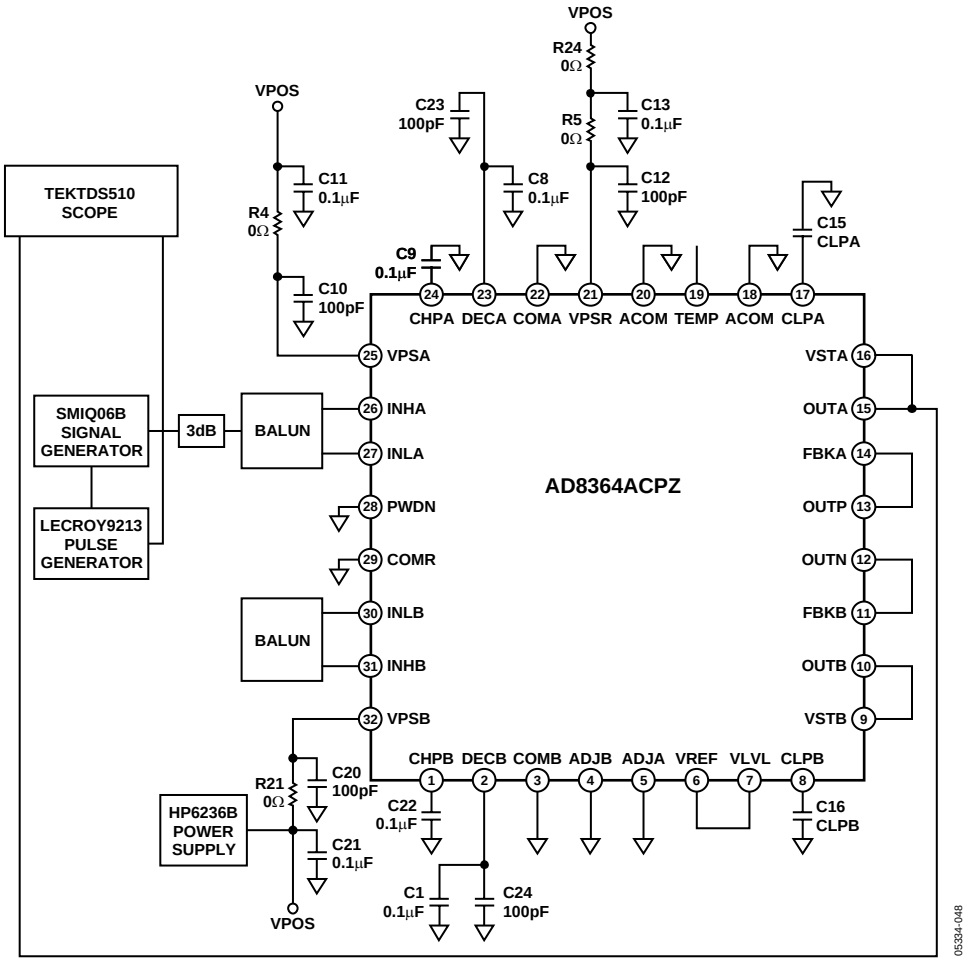


Figure 83. Configuration for RF Burst Measurement

EVALUATION AND CHARACTERIZATION CIRCUIT BOARD LAYOUTS

There are two evaluation boards for the AD8364, one appropriate for low frequency work (AD8364-EVAL-500) and another one designed for use at 2140 MHz (AD8364-EVAL-2140). Each board has a balun specific to operation in the designated frequency range. The RF area layout of the circuit board used for characterization work at 880 MHz is included in this section, showing the footprint of the recommended balun (Mini-Circuits JTX-4-10T) and trace lengths used. The user may obtain different performance than shown in this data sheet if their layout dimensions and style differ.

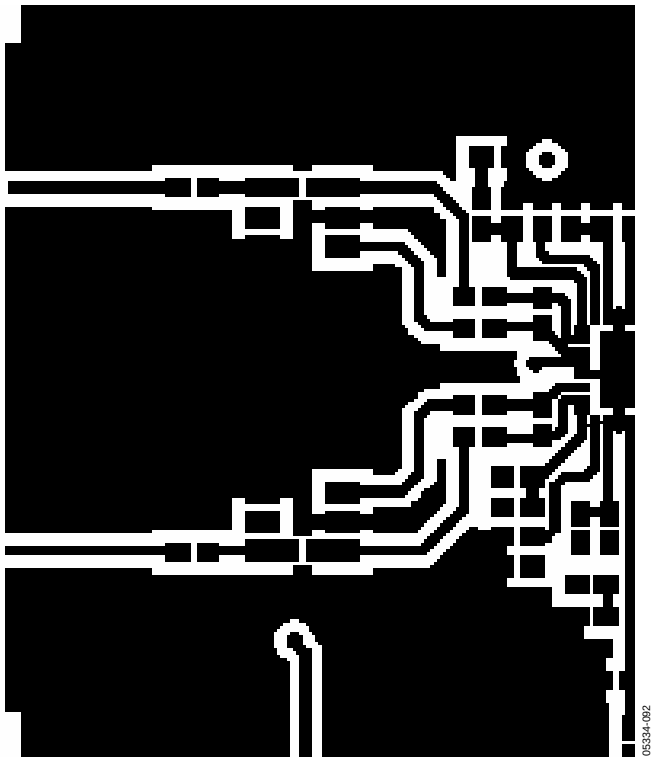


Figure 84. AD8364-EVAL-500 Evaluation Board RF Area Layout

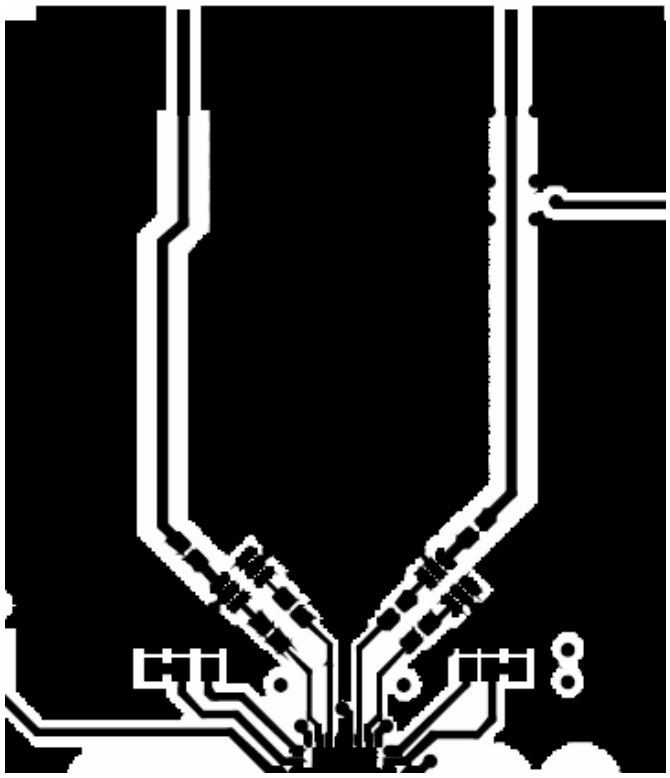


Figure 85. AD8364_EVAL-2140 Evaluation Board RF Area Layout

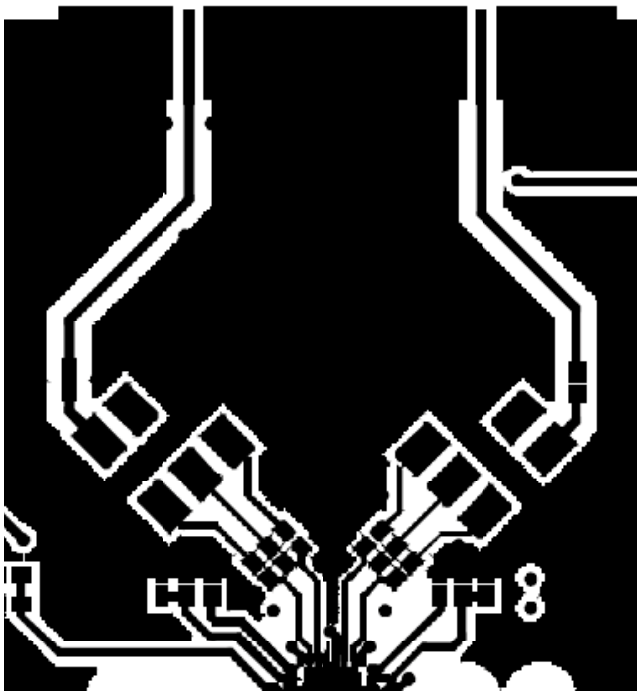


Figure 86. 880 MHz Characterization Board RF Area Layout

Table 7. AD8364-EVAL-500 Evaluation Board Configuration Options (10 MHz to 650 MHz)

Component	Function/Notes	Part Number	Default Value
T1, T2	The dynamic range of the AD8364 is directly related to the magnitude and phase balance of the balun feeding the RF signal to the part. The evaluation board includes M/A-COM ETK4-2T soldered to the board and two unsoldered M/A-COM ETC1.6-4-2-3. The ETK4-2T has good magnitude and phase balance between 10 MHz and 650 MHz, but slowly degrades above 650 MHz due to the balun. The M/A-COM ETC1.6-4-2-3 broadband baluns allow limited dynamic range performance between 500 MHz and 2500 MHz. Better dynamic range can be achieved by using narrow band baluns with better magnitude and phase performance.	M/A-COM ETK4-2T	
C11, C13, C21	Supply filtering/decoupling capacitors.		0.1 µF
C10, C12, C20	Supply filtering/decoupling capacitors.		100 pF
C19	VREF filtering/decoupling capacitor.		0.1 µF
C18	Optional VLVL filtering/decoupling capacitor.		OPEN
C15, C17	Output low-pass filter capacitors (CLPA/B).		0.1 µF
C14, C16	Output low-pass filter capacitors, which can be activated by removing jumpers R6 and R15.		0.1 µF
C23, C24	Input bias-point decoupling capacitors (DECA/B).	Samsung CL10B101KONC	100 pF
C1, C8	Input bias-point decoupling capacitors (DECA/B).	Samsung CL10B104KONC	0.1 µF
C2, C3, C4, C5, C6, C7	Stable, low ESR capacitors are *mandatory* in the RF input area of the AD8364. This corresponds to capacitors connected to Pins INH[A, B], INL[A, B], DEC[A, B], and CHP[A, B]. Poor quality capacitors may result in amplitude and phase mismatch at the differential inputs, which in turn results in low dynamic range. Capacitors with poor aging characteristics under temperature cycling have been shown to accentuate the temperature drift during operation of the AD8364. Using Samsung CL10 series multilayer ceramic capacitors (or similar) in the RF area is suggested.	Samsung CL10B104KONC	0.1 µF
C9, C22	Input high-pass filter capacitor (CHPA/B).	Samsung CL10B104KONC	0.1 µF
R17, R18, R19, R20	R17/R19 are usually jumpers and R18/R20 are usually left open. The pads for R17/R18 or R19/R20 can be used to make voltage dividers to set the ADJA/B voltages for temperature compensation at different frequencies.		R17/R19 = 0 Ω R18/R20 = OPEN
R12, R13	R12 is usually a jumper and R13 is usually open, but the pads can also be used to make a voltage divider to adjust the slope of Channel B.		R12 = 0 Ω R13 = OPEN
DUT	AD8364.	AD8364ACPZ	
R4, R5, R6, R9, R15, R21, R24, R23	Jumpers.		0 Ω
R10, R11	Capacitors can be installed for controller mode.		0 Ω
R2, R16	Optional pull-down resistors.		10 kΩ/OPEN
R1, R3	100 Ω resistor to be added when input coupling from a single-ended source (not installed).		OPEN/100 Ω
R14	To be added for use in slope adjustment (not installed).		OPEN
SW1	Power-down/enable or external power-down selector, open is enable (Position A, unloaded).		
SW2, SW3	Measurement mode (Position A)/controller mode (Position B) selector.		
SW4	VLVL VREF (Position A)/external control (Position B) selector.		
SW5	ADJA VREF (Position A)/external control (Position B) selector.		
SW6	ADJB VREF (Position B)/external control (Position A) selector.		

Table 7. AD8364-EVAL-2140 Evaluation Board Configuration Options (2140 MHz)

Component	Function/Notes	Part Number	Default Value
T1, T2	The dynamic range of the AD8364 is directly related to the magnitude and phase balance of the balun feeding the RF signal to the part. At 2140 MHz, we have found it necessary to use a narrow band balun and have used the Murata LDB212G1020C-001.	Murata LDB212G1020C-00	
C11, C13, C21	Supply filtering/decoupling capacitors.		0.1 µF
C10, C12, C20	Supply filtering/decoupling capacitors.		100 pF
C19	VREF filtering/decoupling capacitor.		0.1 µF
C18	Optional VLVL filtering/decoupling capacitor.		OPEN
C15, C17	Output low-pass filter capacitors (CLPA/B).		0.1 µF
C14, C16	Output low-pass filter capacitors, which can be activated by removing jumpers R6 and R15.		0.1 µF
C23, C24	Input bias-point decoupling capacitors (DECA/B).	Samsung CL10B101KONC	100 pF
C1, C8	Input bias-point decoupling capacitors (DECA/B).	Samsung CL10B104KONC	0.1 µF
C2, C3, C4, C5, C6, C7	Stable, low ESR capacitors are *mandatory* in the RF input area of the AD8364. This corresponds to capacitors connected to Pins INH[A, B], INL[A, B], DEC[A, B], and CHP[A, B]. Poor quality capacitors may result in amplitude and phase mismatch at the differential inputs, which in turn results in low dynamic range. Capacitors with poor aging characteristics under temperature cycling have been shown to accentuate the temperature drift during operation of the AD8364. Using Samsung CL10 series multilayer ceramic capacitors (or similar) in the RF area is suggested.	Samsung CL10B104KONC	0.1 µF
C9, C22	Input high-pass filter capacitor (CHPA/B).	Samsung CL10B104KONC	0.1 µF
R17, R18, R19, R20	R17/R19 are usually jumpers and R18/R20 are usually left open. The pads for R17/R18 or R19/R20 can be used to make voltage dividers to set the ADJA/B voltages for temperature compensation at different frequencies.		R17/R19 = 0 Ω R18/R20 = OPEN
DUT	AD8364.	AD8364ACPZ	
R4, R5, R6, R9, R12, R15, R21	Jumpers.		0 Ω
R10, R11	Capacitors can be installed for controller mode.		0 Ω
R24	Optional loading resistor for TEMP.		1 kΩ
R2, R16	Optional pull-down resistors.		OPEN
R14, R27	To be added for use in slope adjustment (not installed).		OPEN
SW1	Power-down/enable or external power-down selector, open is enable (Position A, unloaded).		
SW2, SW3	Measurement mode (Position A)/controller mode (Position B) selector.		
SW4	VLVL VREF (Position A)/external control (Position B) selector.		
SW5	ADJA VREF (Position A)/external control (Position B)l selector.		
SW6	ADJB VREF (Position B)/external control (Position A) selector.		

EVALUATION BOARDS

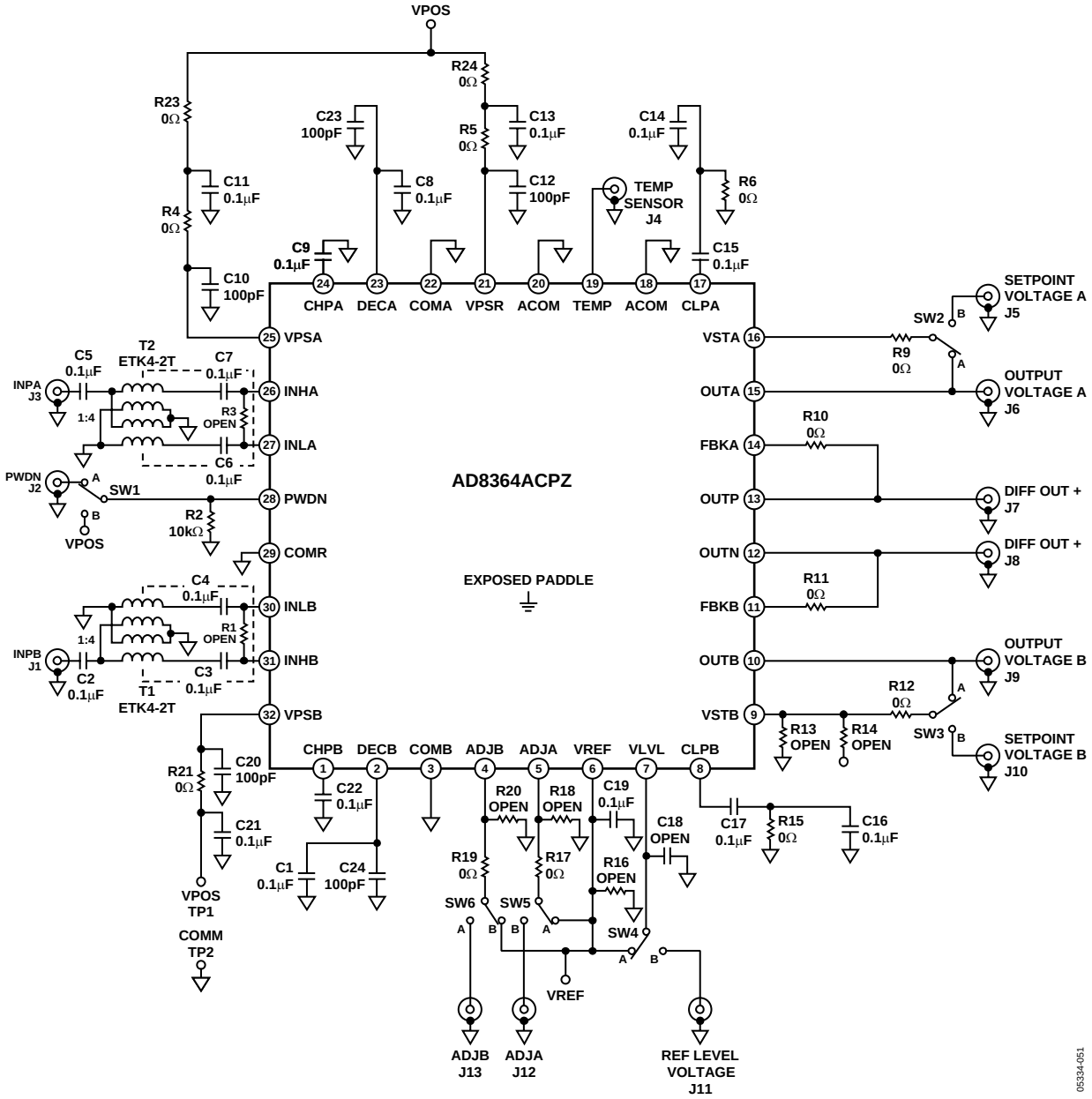


Figure 87. AD8364-EVA-500 Evaluation Board

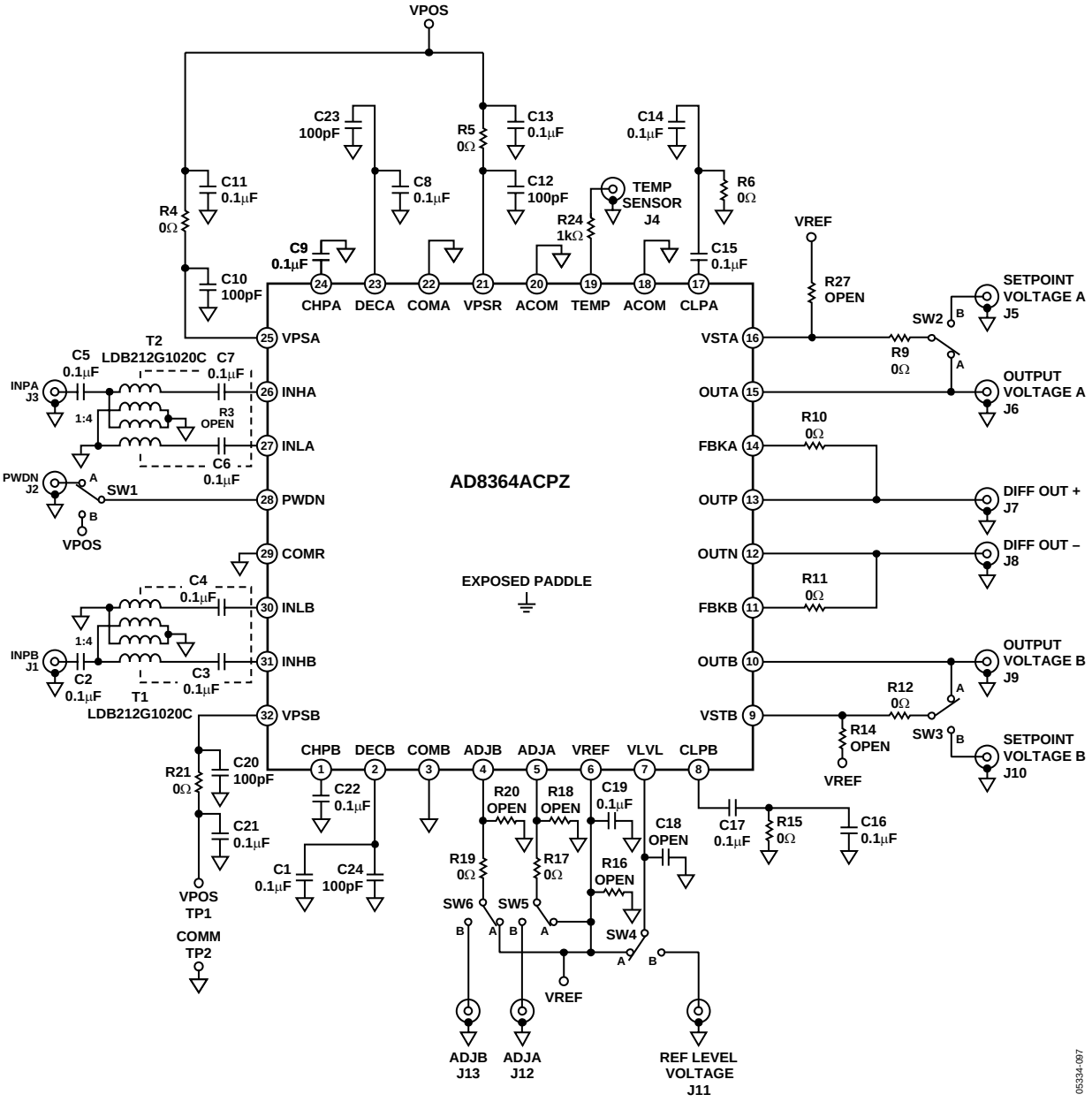


Figure 88. AD8364-EVAL-2140 Evaluation Board

ASSEMBLY DRAWINGS

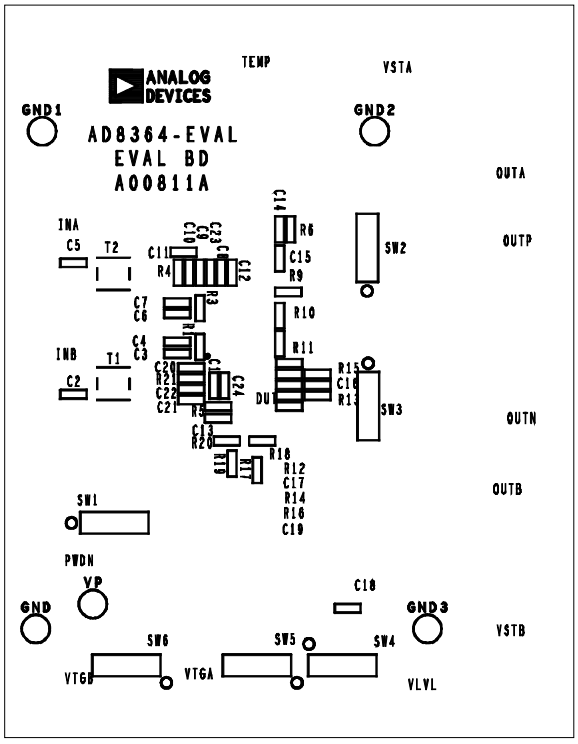


Figure 89. AD8364-EVAL-500 Assembly Drawing

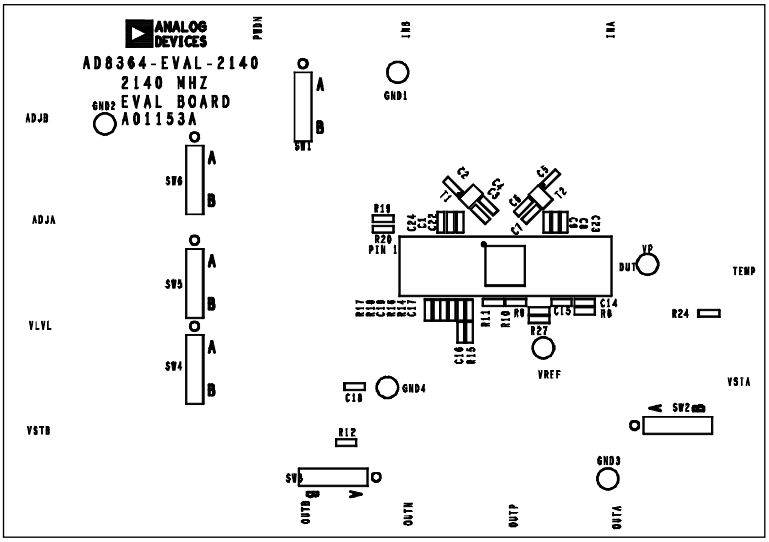
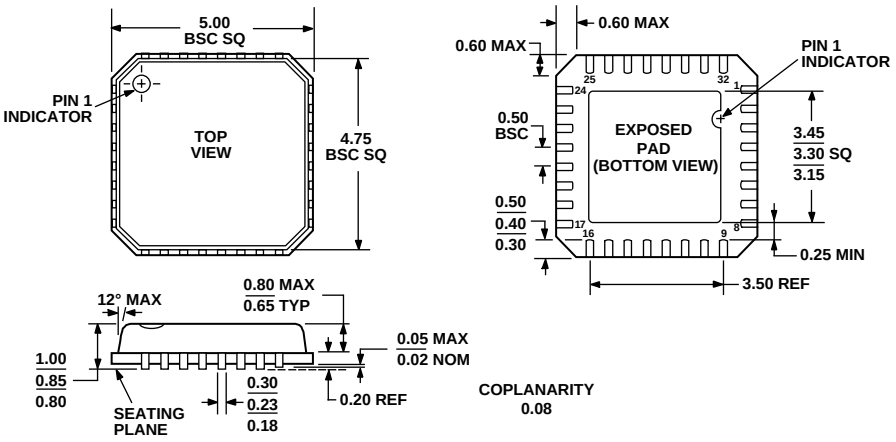


Figure 90. AD8364-EVAL-2140 Assembly Drawing

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 91. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8364ACPZ-WP[1, 2]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3	36 Units
AD8364ACPZ-REEL7[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3	1,500 Units
AD8364ACPZ-RL2[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3	250 Units
AD8364ACP-REEL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3	1,500 Units
AD8364-EVAL-500		Evaluation Board, Low Frequency to 500 MHz		
AD8364-EVAL-2140		Evaluation Board, 2140 MHz only		

[1] Z = Pb-free part.
[2] WP = Waffle Pack

NOTES

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