24dB Range, 1dB Step Size Programmable VGA

Preliminary Technical Data

AD8375

FEATURES

-4 to 20dB Gain Range
1 dB Step Size ± 0.2 dB
Differential input and output
150 Ω Differential Input
Open Collector Differential Output
8dB noise figure @ maximum gain
OIP3 of ~50dBm at 140MHz
–3 dB bandwidth of 690 MHz
Parallel 5-bit Control Interface
Wide input dynamic range
Power-down feature
Single 5V Supply Operation
24 Lead LFCSP 4 x 4 mm Package

APPLICATIONS

Differential ADC drivers
High IF Sampling Receivers
High Output Power IF Amplification
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

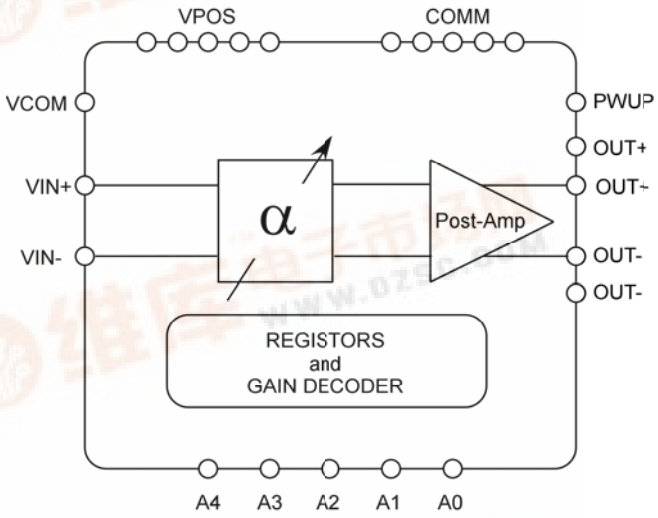

Figure 1.

GENERAL DESCRIPTION

The AD8375 is a digitally controlled, variable gain wide bandwidth amplifier that provides precise gain control, high IP3 and low noise figure. The excellent distortion performance and high signal bandwidth makes the AD8375 an excellent gain control device for a variety of receiver applications.

For wide input dynamic range applications, the AD8375 provides a broad 24dB gain range with 1 dB resolution. The gain is adjusted through a 5-pin control interface and can be driven using standard TTL levels. The open-collector outputs provide a flexible interface, allowing the overall signal gain to be set by the loading resistance. The AD8375 offers a maximum transconductance gain of 67 $m\Omega^{-1}$'s, resulting in a signal gain of 20dB when driving a 150-Ohm load. The maximum signal gain increases to ~24dB when driving a 250-Ohm differential load.

Using a high speed SiGe process and incorporating proprietary distortion cancellation techniques, the AD8375 achieves 50 dBm output IP3 at 140 MHz.

The AD8375 is powered on by applying the appropriate logic level to the PWUP pin. The quiescent current of the AD8375 is typically 130mA. When powered down, the AD8375 consumes less than 5mA and offers excellent input to output isolation. The gain setting is preserved when powered down.

Fabricated on an ADI's high speed SiGe process, the AD8375 provides precise gain adjustment capabilities with good distortion performance. The AD8375 amplifier comes in a compact, thermally enhanced 4 x 4mm 24-lead LFCSP package and operates over the temperature range of –40°C to +85°C.

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SPECIFICATIONS

V_S = 5 V, T = 25°C, Z_S = Z_L = 150Ω at 100MHz, 2 V p-p differential output unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} < 2 V p-p (5.2dBm)		690		MHz
Slew Rate			TBD		V/nsec
INPUT STAGE	Pins VIN+ and VIN-				
Maximum Input Swing	For linear operation (A_V = 0dB)		TBD		V p-p
Differential Input Resistance	Differential		150		Ω
Common-Mode Input Voltage			2		V
CMRR	Gain Code = 00000		TBD		dB
GAIN					
Amplifier Transconductance		0.58	0.067	0.076	Ω^{-1}
Maximum Voltage Gain	Gain Code = 00000		20		dB
Minimum Voltage Gain	Gain Code ≥11000	-5.5	−4	-2.5	dB
Gain Step Size	From Gain Code 00000 to 11000	0.8	1.0	1.2	dB
Gain Flatness	Gain Code = 00000 over 20% fractional bandwidth for f_C < 200MHz		TBD		dB
Gain Temperature Sensitivity	Gain Code = 00000		TBD		mdB/°C
Gain Step Response	For V_{IN} = 0.2V, Gain Code 10100 to 00000		TBD		ns
OUTPUT STAGE	Pins OUT+ and OUT-				
Output Voltage Swing	At P1dB, Gain Code = 00000		10		V p-p
Output impedance	Differential		5k//1		Ω/pF
NOISE/HARMONIC PERFORMANCE					
46 MHz	Gain Code = 00000				
Noise Figure			8.5		dB
Second Harmonic	V_{OUT} = 2 V p-p		-94		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-92		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			19		dBm
70 MHz	Gain Code = 00000				
Noise Figure			8.5		dB
Second Harmonic	V_{OUT} = 2 V p-p		-94		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-92		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			19		dBm
140 MHz	Gain Code = 00000				
Noise Figure			8.5		dB
Second Harmonic	V_{OUT} = 2 V p-p		-86		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-91		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			19		dBm

Parameter	Conditions	Min	Typ	Max	Unit
200 MHz	Gain Code = 00000				
Noise Figure			8.5		dB
Second Harmonic	V_{OUT} = 2 V p-p		-85		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-88		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			18		dBm
POWER-INTERFACE					
Supply Voltage		4.5		5.5	V
Quiescent Current per Channel	thermal connection made to exposed paddle under device		130	140	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C			165	mA
Power Down Current	PWUP Low		3		mA
vs. Temperature	−40°C ≤T_A ≤ +85°C			TBD	mA
ENABLE INTERFACE	Pin PWUP				
Enable Threshold	Minimum voltage to enable the device			1.6	V
PWUP Input Bias Current			0.5		nA
GAIN CONTROL INTERFACE	Pins A0, A1, A2, A3, A4				
V_{IH}	Minimum voltage for a logic high	1.6			V
V_{IL}	Maximum voltage for a logic low			0.8	
Maximum Input Bias Current			900		nA

Table 2. Gain-Code versus Voltage Gain Look-Up Table

5-Bit Binary Gain Code	Voltage Gain (dB)	5-Bit Binary Gain Code	Voltage Gain (dB)
00000	20	01101	7
00001	19	01110	6
00010	18	01111	5
00011	17	10000	4
00100	16	10001	3
00101	15	10010	2
00110	14	10011	1
00111	13	10100	0
01000	12	10101	-1
01001	11	10110	-2
01010	10	10111	-3
01011	9	11000	-4
01100	8	>11000	-4

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
PWUP, A0, A1, A2, A3, A4	-0.6 to (V_{POS} + 0.6V)
Input Voltage, V_{IN+} ,V_{IN-}	-0.6 to +3.1V
Internal Power Dissipation	TBD mW
θ_{JA} (Exposed paddle soldered down)	TBD°C/W
θ_{JA} (Exposed paddle not soldered down)	TBD°C/W
θ_{JC} (At exposed paddle)	TBD°C/W
Maximum Junction Temperature	TBD°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	TBD°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

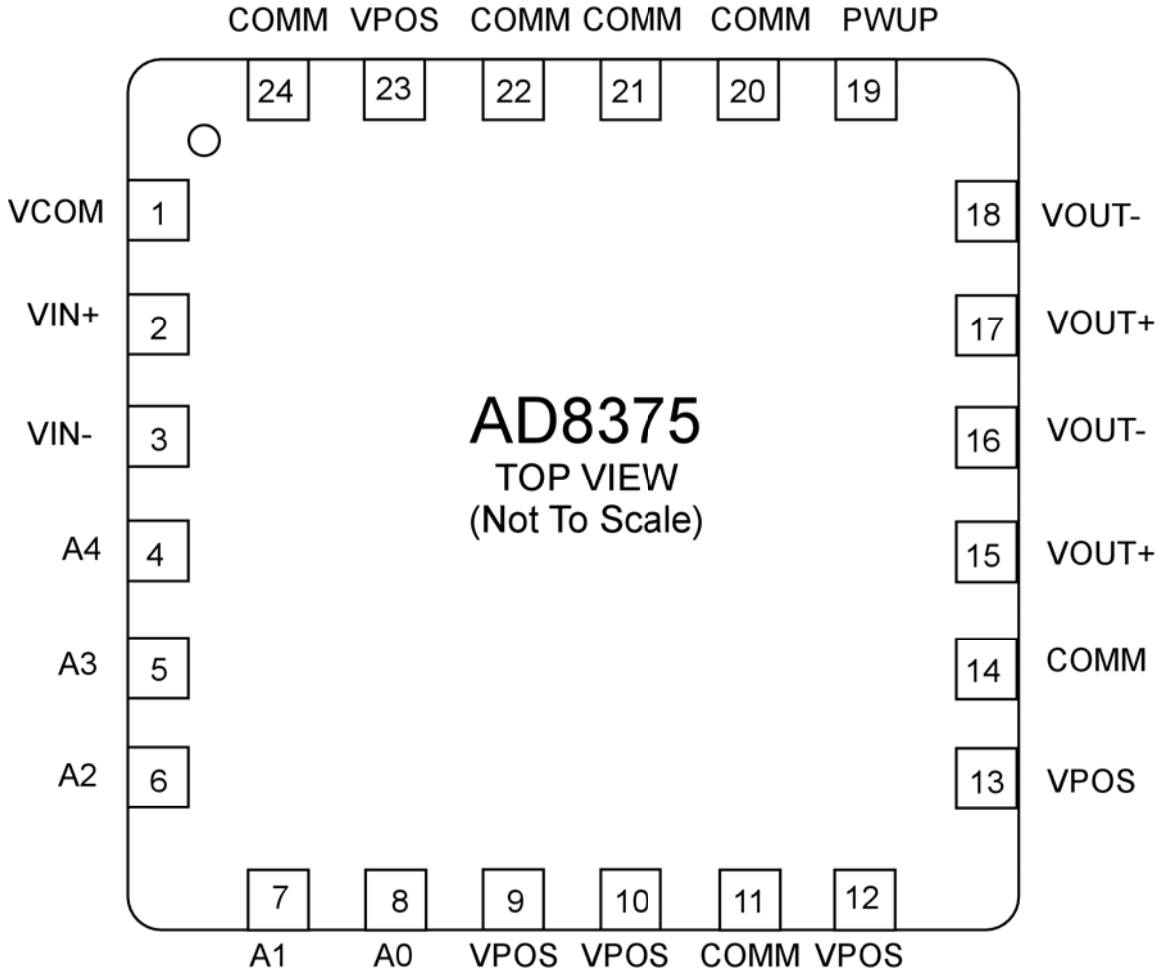

Figure 2. 24 Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCOM	Common Mode Pin. Typically bypassed to ground using external capacitor.
2	VIN+	Voltage Input Positive.
3	VIN-	Voltage Input Negative.
4	A4	The Most Significant Bit (MSB) for the 5-bit Gain Control Interface.
5	A3	MSB-1 for the Gain Control Interface.
6	A2	MSB-2 for the Gain Control Interface.
7	A1	LSB+1 for the Gain Control Interface.
8	A0	The Least Significant Bit (LSB) for the 5-bit Gain Control Interface.
9, 10,12, 13, 23	VPOS	Positive Supply Pins. Should be bypassed to Ground using suitable bypass capacitor.
11, 14, 20, 21, 22, 24	COMM	Device Common (DC Ground).
15, 17	VOUT+	Positive Ouptut Pins (Open Collector). Require DC bias of +5V nominal.
16, 18	VOUT-	Negative Ouptut Pins (Open Collector). Require DC bias of +5V nominal.
19	PWUP	Chip Enable Pin.

OUTLINE DIMENSIONS

24-Lead Frame Chip Scale Package [LFCSP]
4 mm x 4 mm Body
(CP-24)
Dimensions shown in millimeters

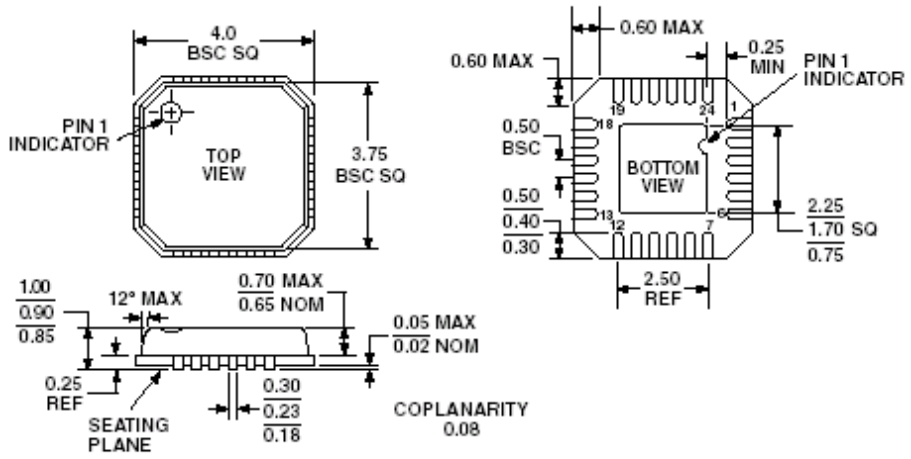

Figure2. 24-Lead LFCSP)

ORDERING GUIDE

Model	Temperature	Package Description	Package Option
AD8375ACPZ-WP	–40°C to +85°C	Waffle Pack, 24 Lead Frame Chip Scale Package	CP-24
AD8375ACPZ-REEL7	–40°C to +85°C	7" Reel, 24 Lead Frame Chip Scale Package	CP-24
AD8375-EVALZ		Evaluation Board	

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