Ultra Low Distortion IF Dual VGA

Preliminary Technical Data

AD8376

FEATURES

Dual Independent Digitally Controlled VGAs
-4 to 20dB Gain Range
1 dB Step Size ± 0.2 dB
Differential input and output
150 Ω Differential Input
Open Collector Differential Output
8.7 dB noise figure @ maximum gain
OIP3 of ~50dBm at 140MHz
–3 dB bandwidth of 700 MHz
Excellent Channel to Channel Isolation
Two Parallel 5-bit Control Interfaces
Wide input dynamic range
Power-down Control
Single 5V Supply Operation
32 Lead LFCSP 5 x 5 mm Package

APPLICATIONS

Differential ADC drivers
Main and Diverstiy IF Sampling Receivers
High Output Power IF Amplification
Multi-channel Receivers
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

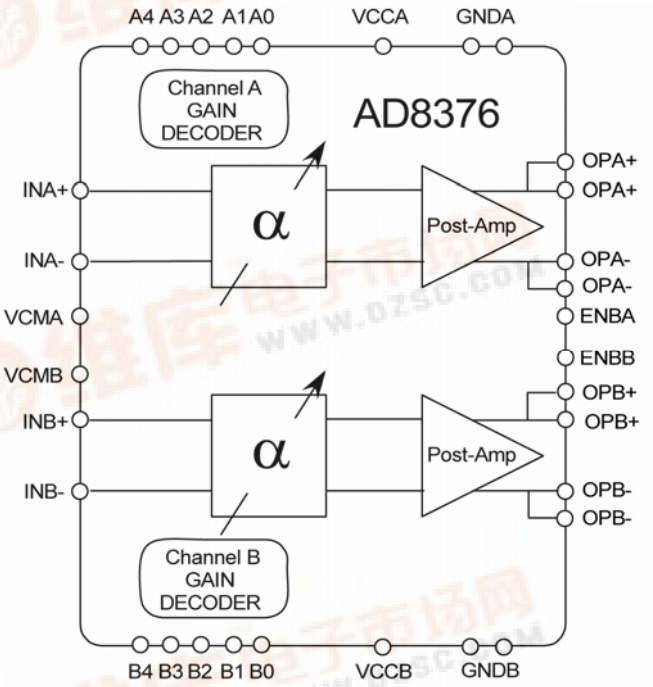

Figure 1.

GENERAL DESCRIPTION

The AD8376 is a dual channel digitally controlled, variable gain wide bandwidth amplifier that provides precise gain control, high IP3 and low noise figure. The excellent distortion performance and high signal bandwidth makes the AD8376 an excellent gain control device for a variety of receiver applications.

For wide input dynamic range applications, the AD8376 provides a broad 24 dB gain range with 1 dB resolution. The gain of each channel is adjusted through dedicated 5-pin control interfaces and can be driven using standard TTL levels. The open-collector outputs provide a flexible interface, allowing the overall signal gain to be set by the loading resistance. The AD8376 offers a maximum trans-conductance gain of 67 $m\Omega^{-1}$'s. This results in a signal voltage gain proportional to the load resistance. When driving a 150 Ω differential load, the maximum signal gain will be 20 dB.

Using a high speed SiGe process and incorporating proprietary distortion cancellation techniques, the AD8376 achieves 50 dBm output IP3 at 140 MHz.

Each channel of the AD8376 can be individually powered on by applying the appropriate logic level to the ENBA and ENBB power enable pins. The quiescent current of the AD8376 is typically 130 mA per channel. When powered down, the AD8376 consumes less than 5mA and offers excellent input to output isolation, lower than -50 dB at 200 MHz.

Fabricated on an ADI's high speed SiGe process, the AD8376 provides precise gain adjustment capabilities with good distortion performance. The AD8376 amplifier comes in a compact, thermally enhanced 5 x 5mm 32-lead LFCSP package and operates over the temperature range of –40°C to +85°C.

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SPECIFICATIONS

V_S = 5 V, T = 25°C, R_S = R_L = 150Ω at 100MHz, 2 V p-p differential output, both channels enabled, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	V_{OUT} < 2 V p-p (5.2dBm)		700		MHz
Slew Rate			TBD		V/nsec
INPUT STAGE	Pins IPA+ and IPA-, IPB+ and IPB-				
Maximum Input Swing	For linear operation (A_V = -4 dB)		TBD	TBD	V p-p
Differential Input Resistance	Differential		150		Ω
Common-Mode Input Voltage			1.9		V
CMRR	Gain Code = 00000		TBD		dB
GAIN					
Amplifier Transconductance	Gain Code = 00000	0.058	0.067	0.076	Ω^{-1}
Maximum Voltage Gain	Gain Code = 00000		20		dB
Minimum Voltage Gain	Gain Code ≥11000		–4		dB
Gain Step Size	From Gain Code 00000 to 11000	0.8	1.0	1.2	dB
Gain Flatness	Gain Code = 00000 over 20% fractional bandwidth for f_C < 200MHz		TBD		dB
Gain Temperature Sensitivity	Gain Code = 00000		TBD		mdB/°C
Gain Step Response	For V_{IN} = 100mVp-p, Gain Code 10100 to 00000		TBD		ns
OUTPUT STAGE	Pins OPA+ and OPA-, OPB+ and OPB-				
Output Voltage Swing	At P1dB, Gain Code = 00000		10		V p-p
Output impedance	Differential		5k/1		Ω/pF
Channel Isolation (Worst Case)	Measured at differential output for differential input applied to alternate channel		-53		dB
NOISE/HARMONIC PERFORMANCE					
46 MHz	Gain Code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		-94		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-92		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			19		dBm
70 MHz	Gain Code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		-94		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-92		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			19		dBm
140 MHz	Gain Code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		-86		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-91		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			19		dBm

Parameter	Conditions	Min	Typ	Max	Unit
200 MHz	Gain Code = 00000				
Noise Figure			8.7		dB
Second Harmonic	V_{OUT} = 2 V p-p		-85		dBc
Third Harmonic	V_{OUT} = 2 V p-p		-87		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			18		dBm
POWER-INTERFACE					
Supply Voltage		4.5	5.0	5.5	V
Quiescent Current Per Channel	Thermal connection made to exposed paddle under device, both channels enabled	TBD	130	140	mA
vs. Temperature	$-40°C \le T_A \le +85°C$			155	mA
Power Down Current Per Channel	PWUP Low		3		mA
vs. Temperature	$-40°C \le T_A \le +85°C$			TBD	mA
POWER-UP/GAIN CONTROL	Pins A0 – A4, B0 – B4, PUPA, and PUPB				
V_{IH}	Minimum voltage for a logic high	1.6			V
V_{IL}	Maximum voltage for a logic low			0.8	
Logic Input Bias Current			900		nA

Table 2. Gain-Code versus Voltage Gain Look-Up Table

5-Bit Binary Gain Code	Voltage Gain (dB)	5-Bit Binary Gain Code	Voltage Gain (dB)
00000	20	01101	7
00001	19	01110	6
00010	18	01111	5
00011	17	10000	4
00100	16	10001	3
00101	15	10010	2
00110	14	10011	1
00111	13	10100	0
01000	12	10101	-1
01001	11	10110	-2
01010	10	10111	-3
01011	9	11000	-4
01100	8	>11000	-4

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
ENBA, ENBB, A0-A4, B0-B4	-0.6 to (V_{POS} + 0.6V)
Input Voltage, V_{IN+} ,V_{IN-}	-0.6 to +3.1V
Internal Power Dissipation	TBD mW
θ_{JA} (Exposed paddle soldered down)	TBD°C/W
θ_{JA} (Exposed paddle not soldered down)	TBD°C/W
θ_{JC} (At exposed paddle)	TBD°C/W
Maximum Junction Temperature	TBD°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	TBD°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

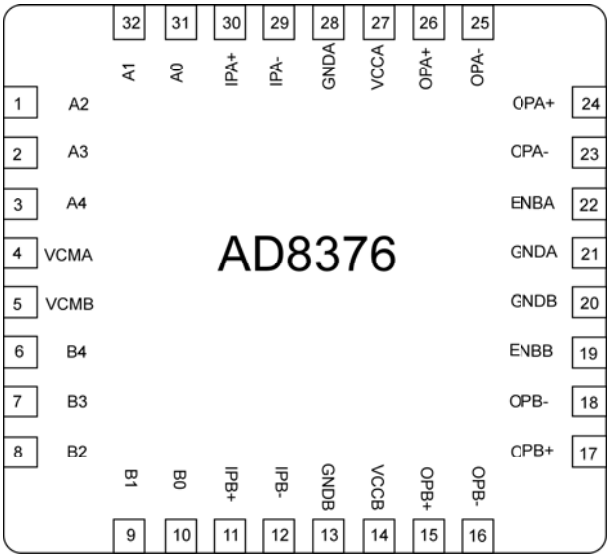

Figure 2. 32 Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A2	MSB-2 for the Gain Control Interface for Channel A.
2	A3	MSB-1 for the Gain Control Interface for Channel A.
3	A4	The MSB for the 5-bit Gain Control Interface for Channel A.
4	VCMA	Channel A Input Common Mode Voltage. Typically bypassed to ground through capacitor
5	VCMB	Channel B Input Common Mode Voltage. Typically bypassed to ground through capacitor
6	B4	The MSB for the 5-bit Gain Control Interface for Channel B.
7	B3	MSB-1 for the Gain Control Interface for Channel B.
8	B2	MSB-2 for the Gain Control Interface for Channel B.
9	B1	LSB+1 for the Gain Control Interface for Channel B.
10	B0	LSB for the Gain Control Interface for Channel B.
11	IPB+	Channel B Positive Input.
12	IPB-	Channel B Negative Input.
13, 20	GNDB	Device Common (DC Ground) for Channel B.
14	VCCB	Positive Supply Pin for Channel B. Should be bypassed to Ground using suitable bypass capacitor.
15, 17	OPB+	Positive Ouptut Pins (Open Collector) for Channel B. Require DC bias of +5V nominal.
16, 18	OPB-	Negative Ouptut Pins (Open Collector) for Channel B. Require DC bias of +5V nominal.
19	ENBB	Power Enable Pin for Channel B.
21, 28	GNDA	Device Common (DC Ground) for Channel A.
22	ENBA	Power Enable Pin for Channel A.
23, 25	OPA-	Negative Ouptut Pins (Open Collector) for Channel A. Require DC bias of +5V nominal.
24. 26	OPA+	Positive Ouptut Pins (Open Collector) for Channel A. Require DC bias of +5V nominal.
27	VCCA	Positive Supply Pins for Channel A. Should be bypassed to Ground using suitable bypass capacitor.
29	IPA-	Channel A Negative Input.
30	IPA+	Channel A Positive Input.
31	A0	LSB for the Gain Control Interface for Channel A.
32	A1	LSB+1 for the Gain Control Interface for Channel A.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, R_{Source} = R_{Load} = 150 Ω, both channels enabled, unless otherwise noted.

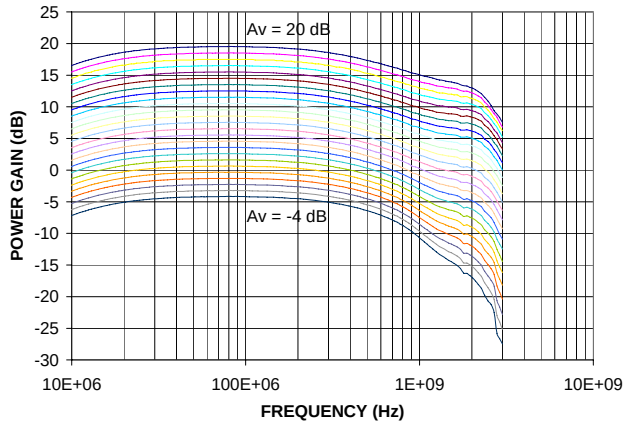

Figure 2. Gain vs. Frequency by Gain Code, (all codes), Differential-in, Differential-out

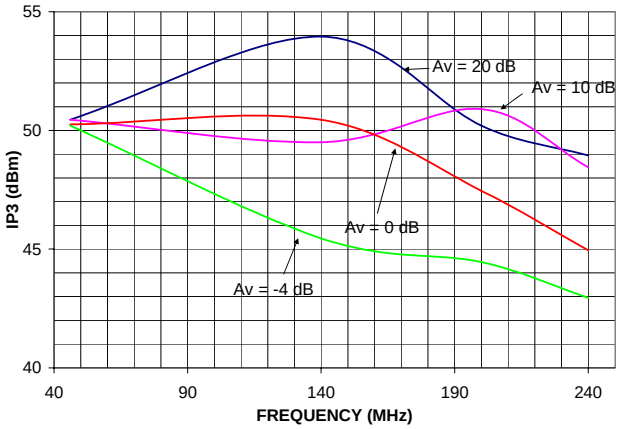

Figure 5. Output IP3 vs. Frequency (20, 10, 0, -4 dB gain codes), 3 dBm tones with 2 MHz spacing

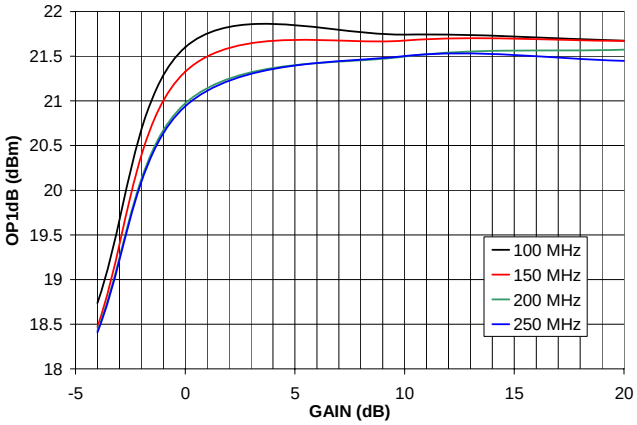

Figure 3. P1dB vs. Gain at Various Frequencies

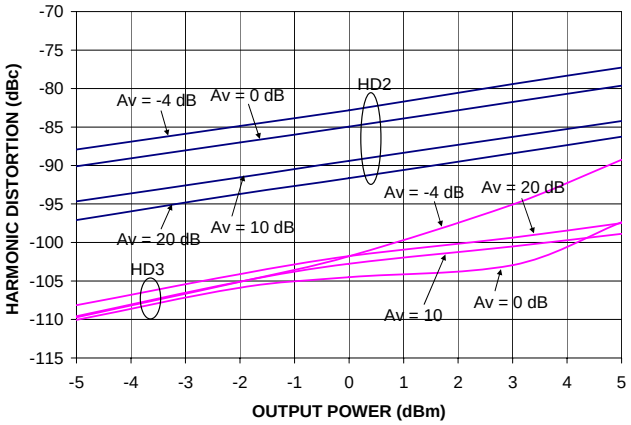

Figure 6. HD2 and HD3 vs. Power Out (20, 10, 0, -4 dB gain codes) at 140 MHz

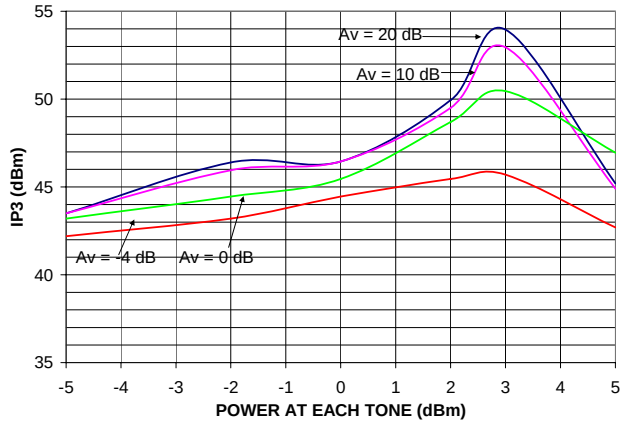

Figure 4. Output IP3 vs. Output Power (20, 10, 0, -4 dB gain codes), Tones at 140 MHz and 142 MHz

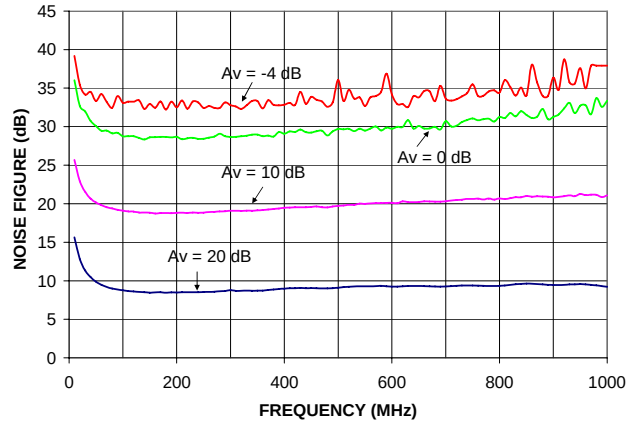

Figure 7. Noise Figure vs. Frequency (20, 10, 0, -4 dB gain codes)

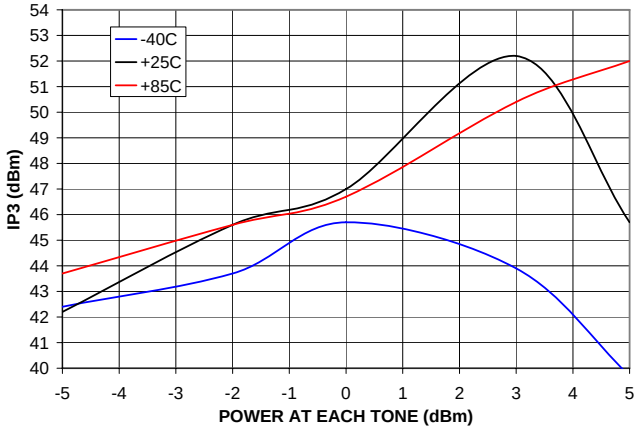

Figure 8. IP3 vs. Power Out over Temperature
20 dB gain code at 110 MHz, 2 MHz spacing

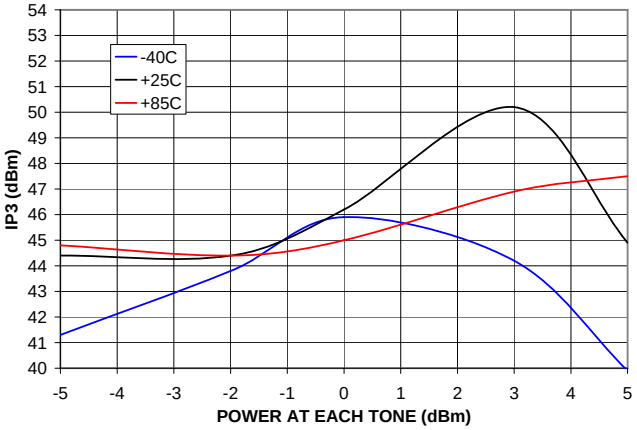

Figure 11. IP3 vs. Power Out over Temperature
0 dB gain code at 110 MHz, 2 MHz spacing

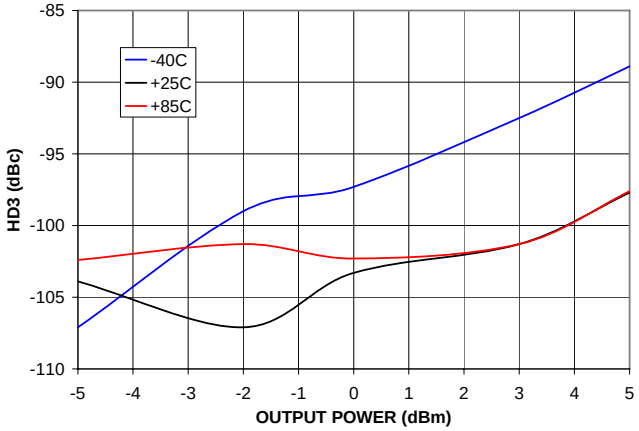

Figure 9. HD3 vs. Power Out over Temperature
20 dB gain code at 110 MHz

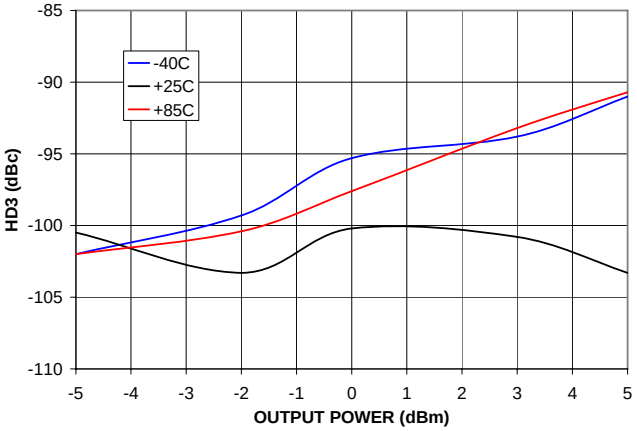

Figure 12. HD3 vs. Power Out over Temperature
0 dB gain code at 110 MHz

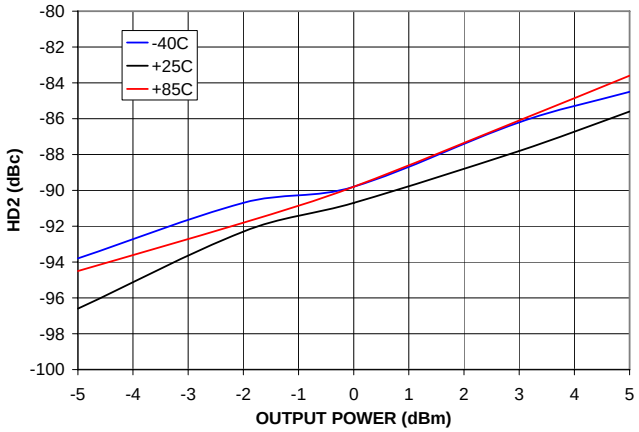

Figure 10.HD2 vs. Power Out over Temperature
20 dB gain code at 110 MHz

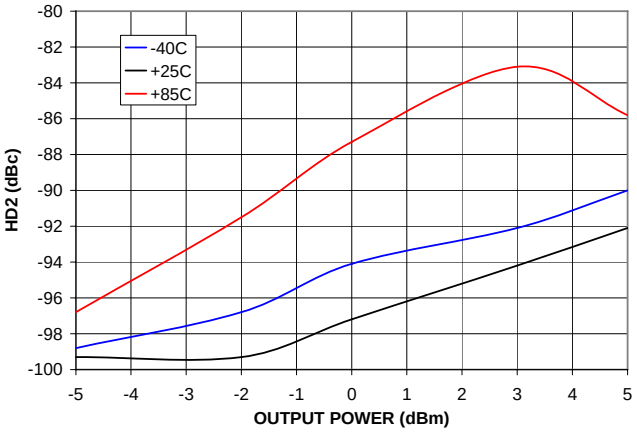

Figure 13. HD2 vs. Power Out over Temperature
0 dB gain code at 110 MHz

APPLICATION

HIGH PERFORMANCE ADC DRIVING

The AD8376 provides the gain, isolation, and balanced low distortion output levels for efficiently driving wideband ADCs such as the AD9445. Figure 9 represents a simplified front end of the AD8376 dual VGA driving two AD9445 14 Bit, 125MSPS A/D converters.

For optimum performance the AD8376 is driven differentially from the input baluns. The input 37.5 Ω resistors in parallel with the 150 Ω input impedance of the AD8376 provide a 50 Ω differential input impedance. The open collector outputs of the AD8376's are biased through the 1 uH inductors and are ac coupled from the 75 Ω load resistors which are required for gain accuracy. The 75 Ω load resistors are also ac coupled from the AD9445 to negate a DC affect on the input common mode voltage of the AD9445. The series 33 Ω resistors improve the SNR by providing isolation. The AD9445 represents a 1 kΩ differential load and requires a 2 V_{p-p} differential signal (VREF=1V) between VIN+ and VIN- for a full scale output.

This circuit provides variable gain, isolation and source matching for the AD9445. Using this circuit with the AD8376 in a gain of 20 dB (Max Gain) an SFDR performance of 86 dBc is achieved at 100 MHz (see Figure 8).

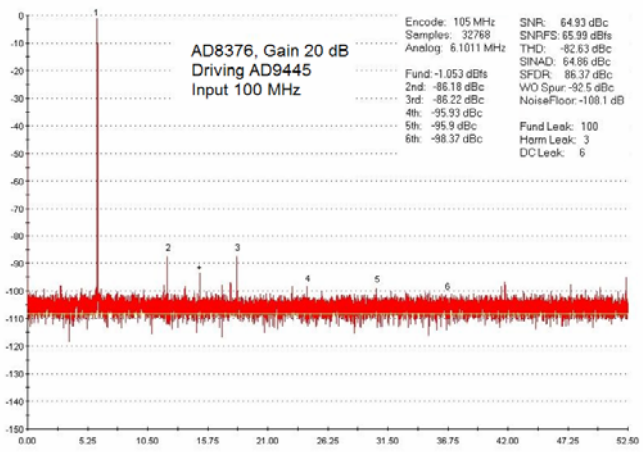

Figure 14. SFDR Performance of the AD8376 Driving the AD9445

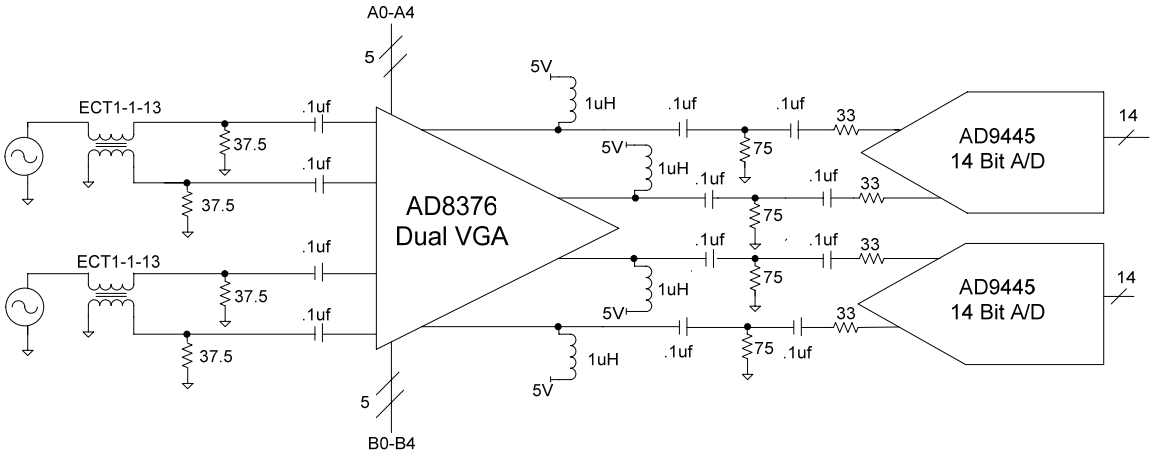

Figure 15. AD8376 Driving the AD9445

EVALUATION BOARD

Figure 10 shows the schematic of the AD8376 evaluation board. The silkscreen and layout of the component and circuit sides are shown in Figure 11 through Figure 14. The board is powered by a single-supply in the 4. 5 V to 5.5 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors at each power supply pin. Additional decoupling, in the form of a series resistor or inductor at the supply pins, can also be added. Table 2 details the various configuration options of the evaluation board.

The output pins of the AD8376 require supply biasing with 1 µH RF chokes. Both the input and output pins must be ac-coupled. These pins are converted to single-ended with a pair of baluns (Mini-Circuits TC3-1T+ and M/A-COM ETC1-1-13). The baluns at the input, T1 and T2, are used to transform 50 Ω source impedances to the desired 150 Ω reference levels. The output baluns, T3 and T4, and the matching components are configured to provide a 150 Ω to 50 Ω impedance transformations with insertion losses of about 10 dB.

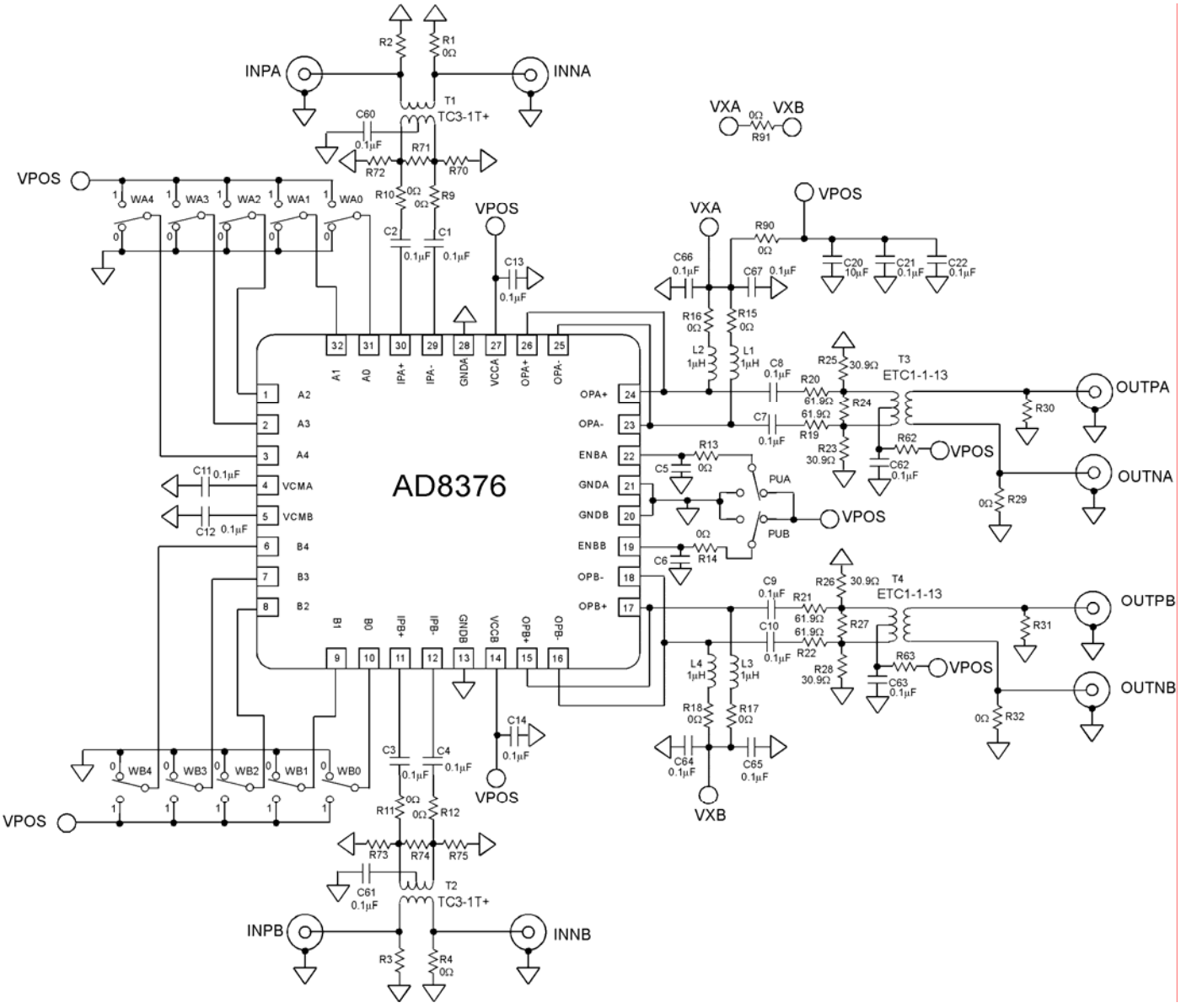

Figure 16. AD8376 Evaluation Board Schematic

Table 2. Evaluation Board Configuration Options

Components	Function	Default Conditions
C13, C14, C20 to C22, C64 to C67, R90, R91	Power Supply Decoupling. Nominal supply decoupling consists a 10 µF capacitor to ground followed by a 0.1 µF capacitor to ground positioned as close to the device as possible.	C20 = 10 µF (size 3528) C13, C14 = 0.1 µF (size 0402) C21, C22, C64 to C67 = 0.1 µF (size 0603) R90, R91 = 0 Ω (size 0603)
T1, T2, C1 to C4, C61, C62, R1 to R4, R9 to R12, R70 to R75	Input Interface. T1 and T2 are 3-to-1 impedance ratio baluns to transform a 50 Ω single-ended input into a 150 Ω balanced differential signal. R1 and R4 ground one side of the differential drive interface for single-ended applications. R9 to R12 and R70 to 75 are provided for generic placement of matching components. C1 to C4 are dc blocks.	T1, T2 = TC3-1+ (Mini-Circuits) C1 to C4, C60, C61 = 0.1 µF (size 0402) R1, R4, R9 to R12 = 0 Ω (size 0402) R2, R3, R70 to R75 = open (size 0402)
T3, T4, C7 to C10, L1 to L4, R15 to R32, R62, R63, C62, C63	Output Interface. C7 to C10 are dc blocks. L1 to L4 provide dc biases for the outputs. R19 to R28 are provided for generic placement of matching components. The evaluation board is configured to provide a 150 Ω to 50 Ω impedance transformation with an insertion loss of about 10 dB. T3 and T4 are 1-to-1 impedance ratio baluns to transform the balanced differential signasl to single-ended signals. R29 and R32 ground one side of the differential output interface for single-ended applications.	C7 to C10= 0.1 µF (size 0402) L1 to L4 = 1 µH (size 0805) T3, T4 = ETC1-1-13 (M/A-COM) R19 to R22 = 61.9 Ω (size 0402) R23, R25, R26, R28 = 30.9 Ω (size 0402) R15 to 18 = 0 Ω (size 0603) R29, R32 = 0 Ω (size 0402) R24, R27, R30, R31, R62, R63 = open (size 0402) C62, C63 = 0.1 µF (size 0402)
PUA, PUB, R13, R14, C5, C6	Enable Interface. The AD8376 is enabled by applying a logic high voltage to the ENBA pin for channel A or the ENBB pin for channel B. Channel A is enabled when the PUA switch is set in the "up" position, connecting the ENBA pin to VPOS. Likewise, Channel B is enabled when the PUB switch is set in the "up" position, connecting the ENBB pin to VPOS. Both channels are disabled by setting the switches to the "down" position, connecting ENBA and ENBB pins to GND.	PUA, PUB = installed R13, R14 = 0 Ω (size 0603) C5, C6 = open (size 0603)
WA0 to WA4, WB0 to WB4	Parallel Interface Control. Used to hardwire A0 through A4 and B0 through B4 to the desired gain. The bank of switches, WA0 to WA4, set the binary gain code for channel A. The bank of switches, WB0 to WB4, set the binary gain code for channel B. WA0 and WB0 represent the LSB for each of the respective channels.	WA0 to WA4, WB0 to WB4 = installed
C11, C12	Voltage Reference. Input Common Mode Voltage ac-coupled to ground by 0.1 µF capacitors, C11 and C12.	C11, C12 = 0.1 µF (size 0402)

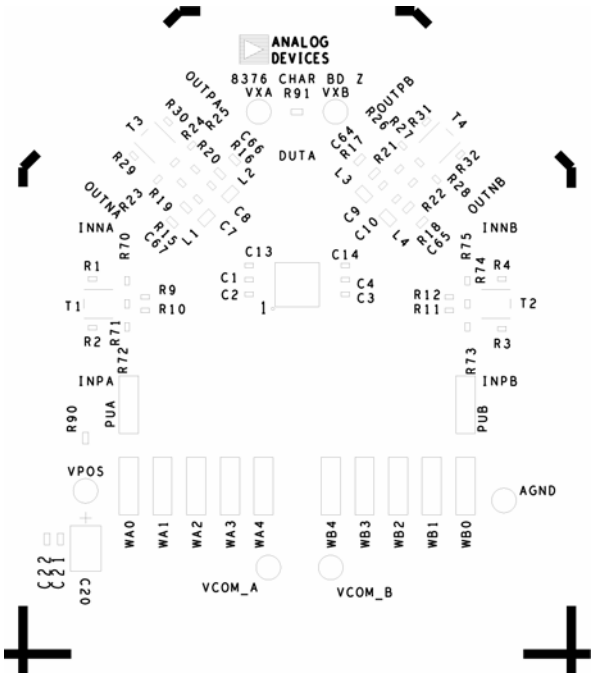

Figure 17. Component Side Silkscreen

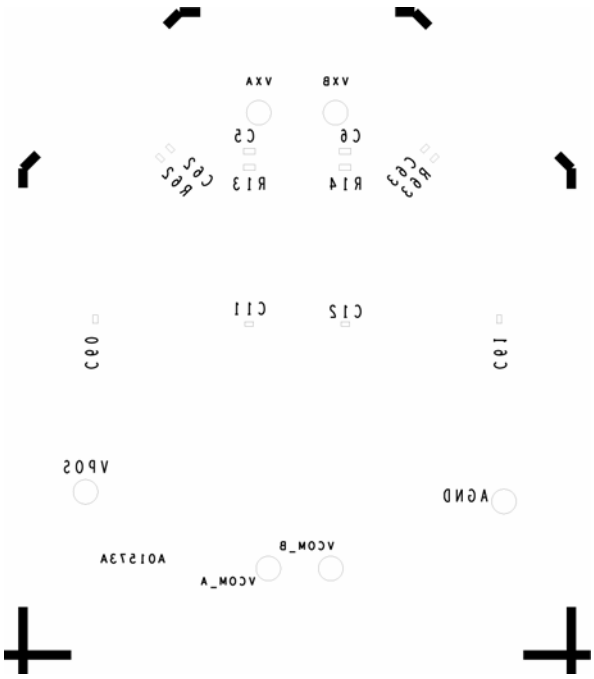

Figure 18. Circuit Side Silkscreen

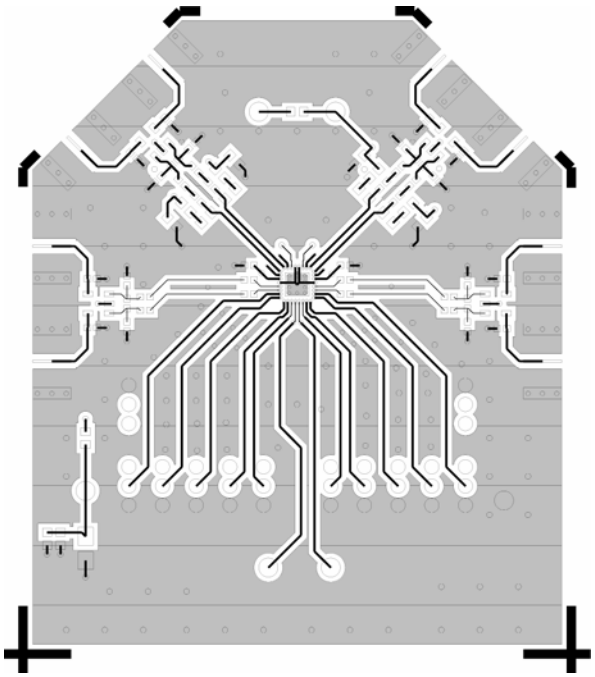

Figure 19. Component Side Layout

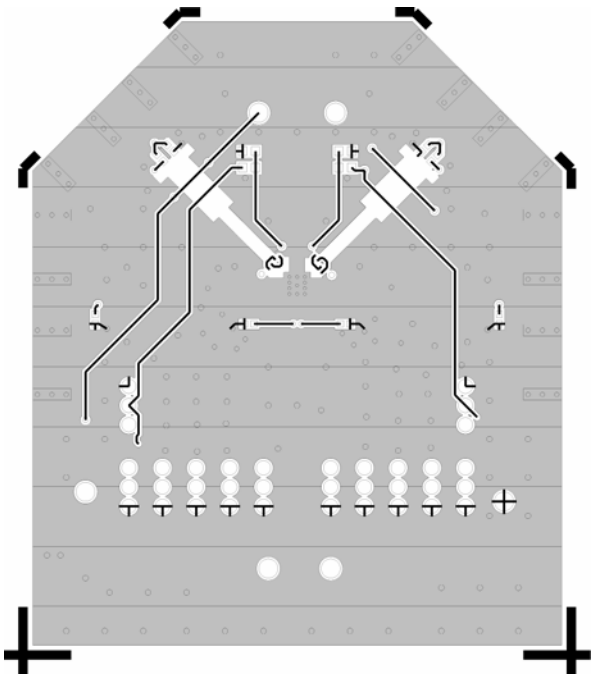

Figure 20. Circuit Side Layout

OUTLINE DIMENSIONS

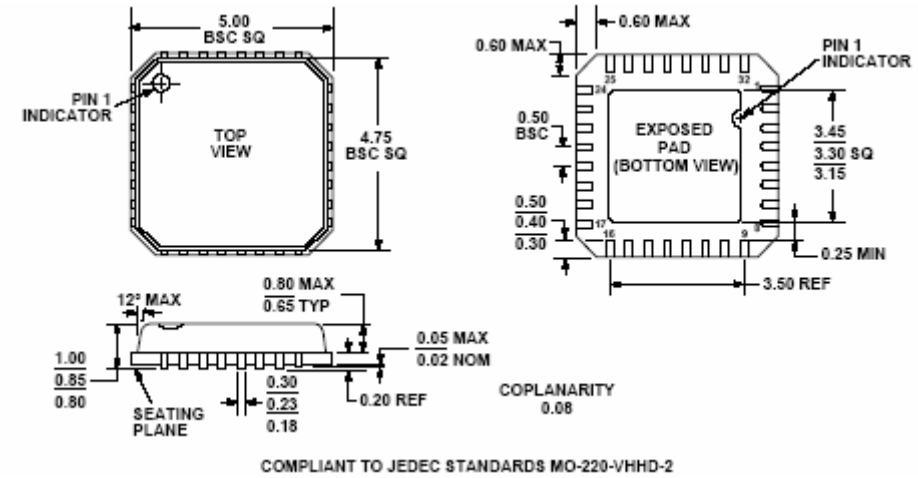

Figure2. 32-Lead LFCSP

ORDERING GUIDE

Model	Temperature	Package Description	Package Option
AD8376ACPZ-WP	–40°C to +85°C	Waffle Pack, 32 Lead Frame Chip Scale Package	CP-32-3
AD8376ACPZ-REEL7	–40°C to +85°C	7" Reel, 32 Lead Frame Chip Scale Package	CP-32-3
AD8376-EVALZ		Evaluation Board	

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